DATABOOK

1991 DEVICES

Systems Logic

Imaging

Storage

Communications

WESTERN DIGITAL

DATABOOK

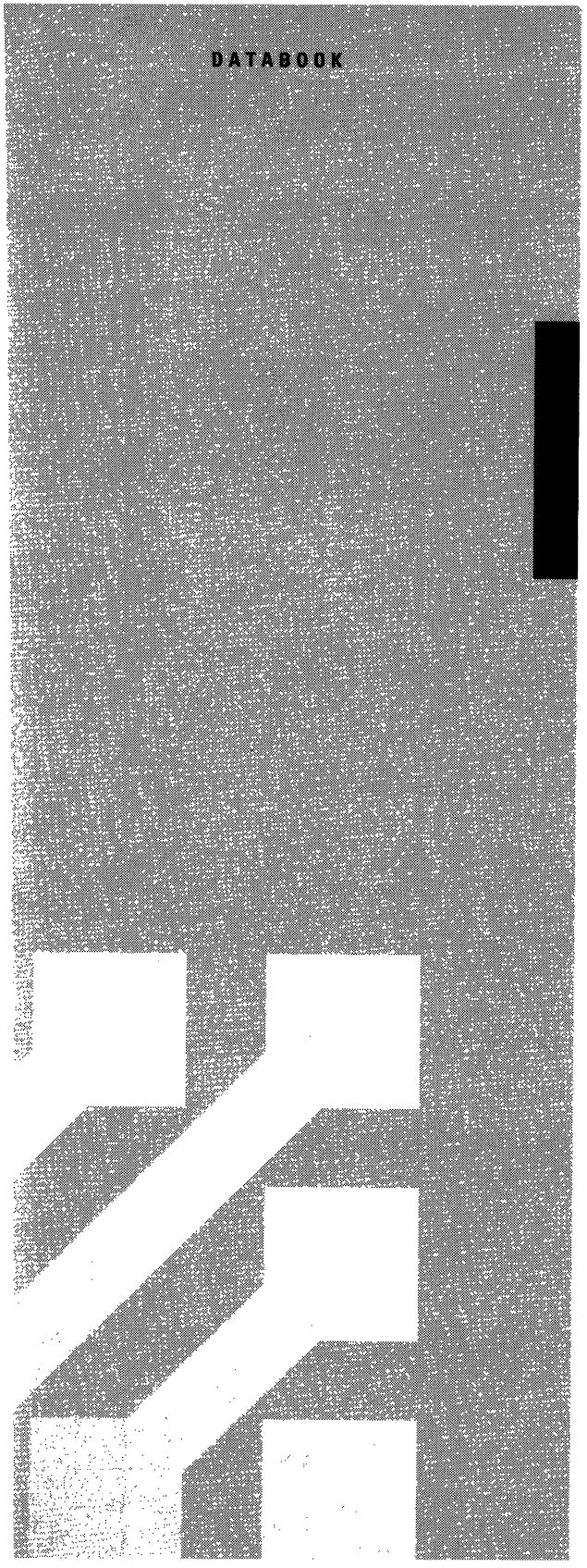
1991 DEVICES

Systems Logic

Imaging

Storage

Communications



WESTERN DIGITAL

Western Digital Corporation
Western Digital Plaza, 8105 Irvine Center Drive, Irvine, CA 92718

For Service and Literature, call:
714.932.4900
800.832.4778 (USA)
800.448.8470 (Canada)

TABLE OF CONTENTS

TABLE OF CONTENTS

ALPHANUMERIC TABLE OF CONTENTS

INTERARCHITECTURE CROSS REFERENCE ACCORDING TO SYSTEM PLATFORM

Device **Section Number**

Data Sheet and Device Status Definitions

Status in Data Sheet Footer	Device Status	Definition
ADVANCED INFORMATION AND DATE	Initial Production	This data sheet contains information prior to device characterization. Western Digital Corporation reserves the right to change specifications at any time without notice in order to improve overall design and operation.
DATE	Full Production	This data sheet contains final specifications. The information has been updated and published as of the date indicated. Western Digital Corporation reserves the right to change specifications at any time without notice in order to improve overall design and operation.

Western Digital's Interarchitecture

Western Digital designs and manufactures a full range of VLSI (very large-scale integration) products that control the fundamental functions of computing: storage control, video, data communications, and systems logic. This diverse technical expertise enables Western Digital to design all components from a systems perspective. And through the Interarchitecture™ products that result from that design process, the company can provide a level of compatibility and performance that other companies can't.

Interarchitecture is not limited to devices only, but extends to drives as well. Western Digital employs this process extensively in designing drives; the controller and drive electronics are designed together to produce an intelligent drive of incomparable performance and reliability. And when, for example, Western Digital's Caviar or Piranha drives are paired with Western Digital's 7600 core logic, the result is even greater performance characteristics and guaranteed compatibility.

Interarchitecture is the process whereby devices are developed "inter"dependently, that is the designer of the core logic, for example, works with the designer of the video device. This interaction produces device solutions that work together better, resulting in matched chip sets with unmatched performance.

The Advantages Of Interarchitecture

Through its Interarchitecture products -- complete platform solutions designed in concert exclusively by Western Digital -- you can realize a number of significant advantages:

- ***Accelerated Time To Market***
  Using Western Digital's Interarchitecture products will reduce your research and design cycle, allowing you to get your product to market faster.

- ***Cost-Effective Solutions***
  The inherent qualities of Western Digital's Interarchitecture products will enable you to design and manufacture your products more cost effectively. Your designers can increase system functionality while simplifying system integration, and by providing full functionality in fewer chips, these solutions will reduce manufacturing, test and maintenance costs.

- ***Increased Design And System Flexibility***
  Interarchitecture products give your systems designers more platform and application choices and more ways to solve specific design problems. Using the same set of chips, designers can upgrade or downgrade their systems utilizing different processors (e.g.: 80286 or 80386SX) and implement a variety of systems software (UNIX, OS/2, DOS).

- ***Optimized Performance***
  Western Digital designs its Interarchitecture chips together, that is, the core logic was developed with the video, etc. Accordingly, when all these pieces are implemented as a total solution, speed enhancements for certain applications can be achieved.

- ***Improved Reliability And Compatibility***
  The process of co-designing across an entire product line increases overall product reliability.

Western Digital guarantees the compatibility of one of its devices to another, and when used in conjunction, Interarchitecture products can help ensure overall system compatibility.

Interarchitecture Solutions For Desktop And Laptop Systems

WD7600 System Chipset for 80286 or 80386SX desktop systems

Components:

WD76C10 single-chip core logic

- memory control, CPU control, DMA interrupts, buffers
- AT-bus control up to 25 MHz
- 1.25 micron CMOS design
- 80286 or 80386SX interface

WD76C20 single-chip storage

- floppy control, IDE control, real-time clock, CMOS RAM, chip select decodes
- 1.25 micron CMOS design
- data transfer in DMA or non-DMA modes
- chip select logic generation

WD76C30 single-chip data communications

- serial/parallel I/O control, programmable coprocessor clock, floppy frequency generator, keyboard clock, baud rate generator, AT-bus clock, interrupt multiplexor
- 1.25 micron CMOS design
- FIFO port operation

WD90C11 (PVGA1C) single chip video

- fully integrated VGA video control
- optional video RAMDAC and video clock
- 8514/A video option

WD90C61 -- video graphics array clock (PCLK2)

*Western Digital Interachitecture Intelligent Drives**

Caviar™ Drives:

- one-inch, 42- and 85-Mbyte formatted capacities, 18 milliseconds
- CacheFlow™, adaptive segmented cache
- Automatic head parking, advanced defect management and embedded sector servo control

Piranha™ Drives:

- 3.5-inch, 106- and 212-Mbyte formatted capacities, 16 milliseconds
- CacheFlow, adaptive segmented cache
- Automatic head parking, advanced defect management and embedded sector servo control

* For more information on Western Digital's intelligent drives, call 1-800-832-4778 in the US, or 1-800-448-8470 in Canada.

WD7600LP System Chipset for 80286 or 80386SX portable systems

Components:

WD76C10LP single-chip core logic

- memory control, CPU control, DMA interrupts, buffers
- special sleep, speed-up modes
- extensive set of power management features
- AT-bus control up to 12.5 MHz

WD76C20 single-chip storage

- floppy control, IDE control, real-time clock, CMOS RAM, chip select decodes
- 1.25 micron CMOS design
- data transfer in DMA or non-DMA
- chip select logic generation

WD76C30 single-chip data communications

- serial/parallel I/O control, programmable coprocessor clock, floppy frequency generator, keyboard clock, baud rate generator, AT-bus clock, interrupt multiplexor
- 1.25 micron CMOS design
- FIFO port operation

WD90C20 (PVGA1F) single-chip video

- full VGA video support with laptop RAMDAC
- optional video clock
- supports 32-color, gray-scale palette

WD90C61 -- video graphics array clock (PCLK2)

*Western Digital Interarchitecture Intelligent Drives**

AB130 Piranha Drive:

- 2.5-inch, 0.6 inches high
- 31.5 Mbyte formatted capacity
- 19 milliseconds average seek time
- CacheFlow multi-segmented, adaptive cache
- 6 power-management modes

AH260 Hornet Drive:

- 2.5-inch, 0.75 inches high
- 62.9 Mbyte formatted capacity
- 19 milliseconds average seek time
- CacheFlow multi-segmented, adaptive cache
- 6 power-management modes

* For more information on Western Digital's intelligent drives, call 1-800-832-4778 in the US, or 1-800-448-8470 in Canada.

Western Digital Quality
Customer Satisfaction Through Relentless Improvement

From its manufacturing, assembly and test facilities throughout the world, Western Digital is committed to producing the highest quality semiconductor, board-level and intelligent disk drive products in the world.

The company's goal is to continually improve the reliability of those products through the implementation of a variety of quality programs, utilization of the most advanced evaluation and analysis tools and the execution of an extensive set of qualification and testing procedures.

Western Digital can deliver unique customer advantages due to the vertically integrated structure of the company, whereby it designs, develops, manufactures, tests and markets all of its products. Accordingly, Western Digital can ensure that the quality and reliability of its designs are translated into products of similar quality for the end user.

Quality starts with employees at Western Digital. Employees undergo thorough training to ensure the most technically-advanced workforce, and those employees then work closely with upper management through customer satisfaction committees, steering committees and executive partnerships to solve problems.

The company then implements its "total quality management" program for every chip, board and drive product. That program begins with a complete quality evaluation of the materials used to make products. Materials must pass a full complement of inspections and audits, and vendors are constantly measured and re-qualified.

An exhaustive product evaluation program is then executed, encompassing a complete battery of characterization and functionality tests from engineering prototypes through unlimited production. An additional set of tests are conducted at the manufacturing phase, with special attention paid to the environmental factors that can adversely affect product quality.

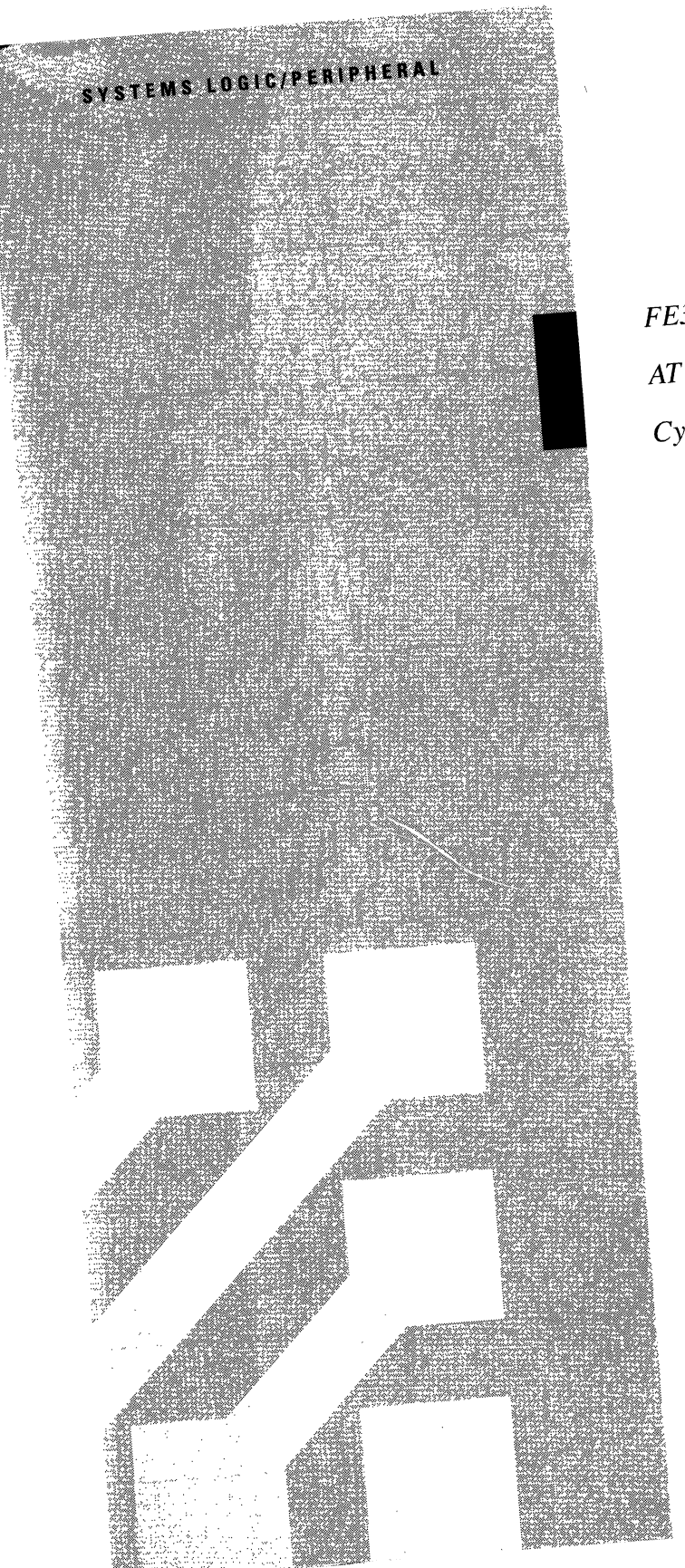
Western Digital's quality process doesn't end after a product is manufactured. The company constantly works to reduce cycle time; it is continually evaluating its certified vendors, while achieving certification by its own customers; and it is always striving for superior customer service and technical support through programs such as its "customer quality alert" program, through which customer quality issues are addressed in less than 48 hours.

From raw materials to finished product, Western Digital is dedicated to quality and to guaranteeing that the result of its design and manufacturing efforts is the most reliable product attainable.

SYSTEMS LOGIC/PERIPHERAL

FE3001

AT Clock Generation and Cycle Control Device



WESTERN DIGITAL

TABLE OF CONTENTS

TABLE OF CONTENTS, Continued

APPENDIX

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

1.1 DESCRIPTION

The FE3001 contains all of the clock generation and cycle control logic necessary to implement an IBM AT compatible computer. It is part of the FE3600 chip set intended to simplify the design of 80286 based AT computers.

Its features include programmable CPU and DMA clock generation, system clock generation, programmable bus timing, programmable wait state generator, refresh and DMA controls, bus arbitration logic, NMI generator and parity error logic, reset/shutdown control, sleep mode, and 80286 interface logic and packaged in an 84-pin PLCC.

1.2 FEATURES

- Programmable CPU and DMA clock generator
- System clock generator
- Programmable bus timing
- Programmable wait state generator
- Refresh and DMA controls
- Bus arbitration logic
- NMI generator and Parity error logic
- Reset/shutdown control
- Sleep mode
- 80286 interface logic
- 1.25 micron HCMOS technology
- 84-Pin PLCC

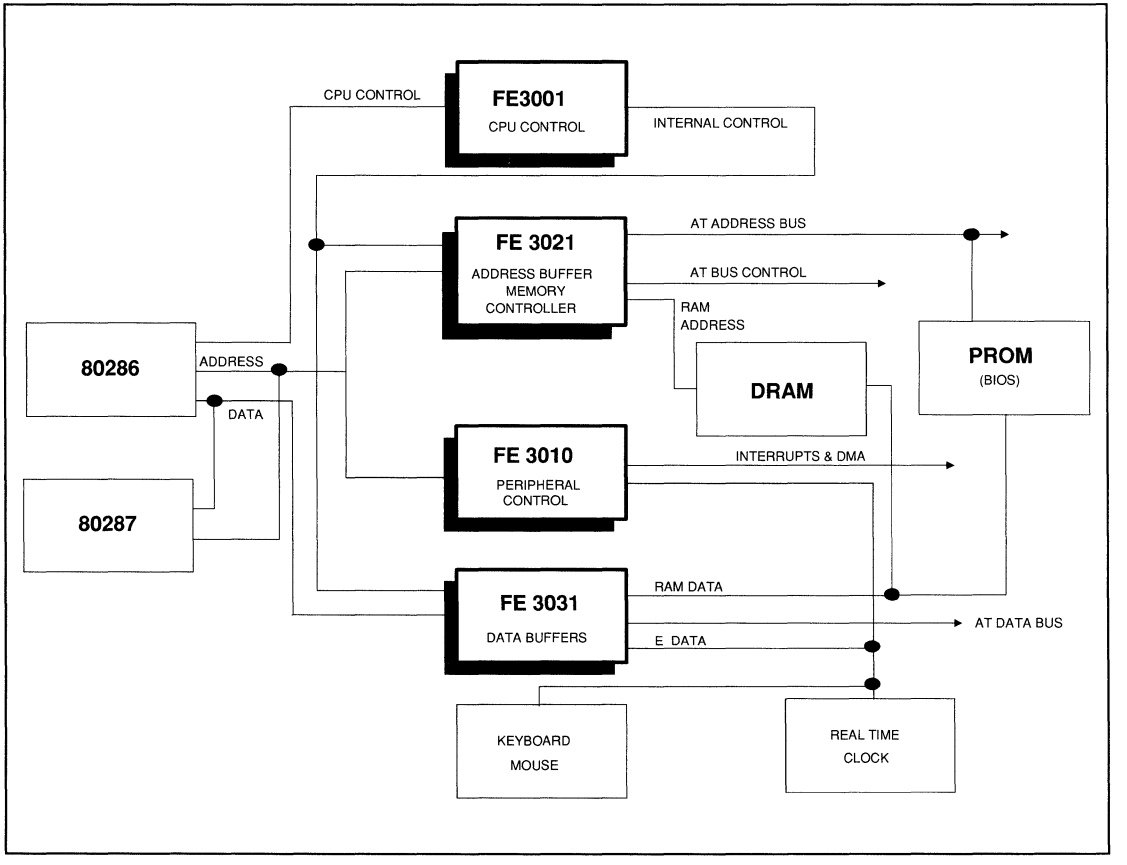


FIGURE 1-1. FE3600 CHIP SET FUNCTIONAL BLOCK DIAGRAM

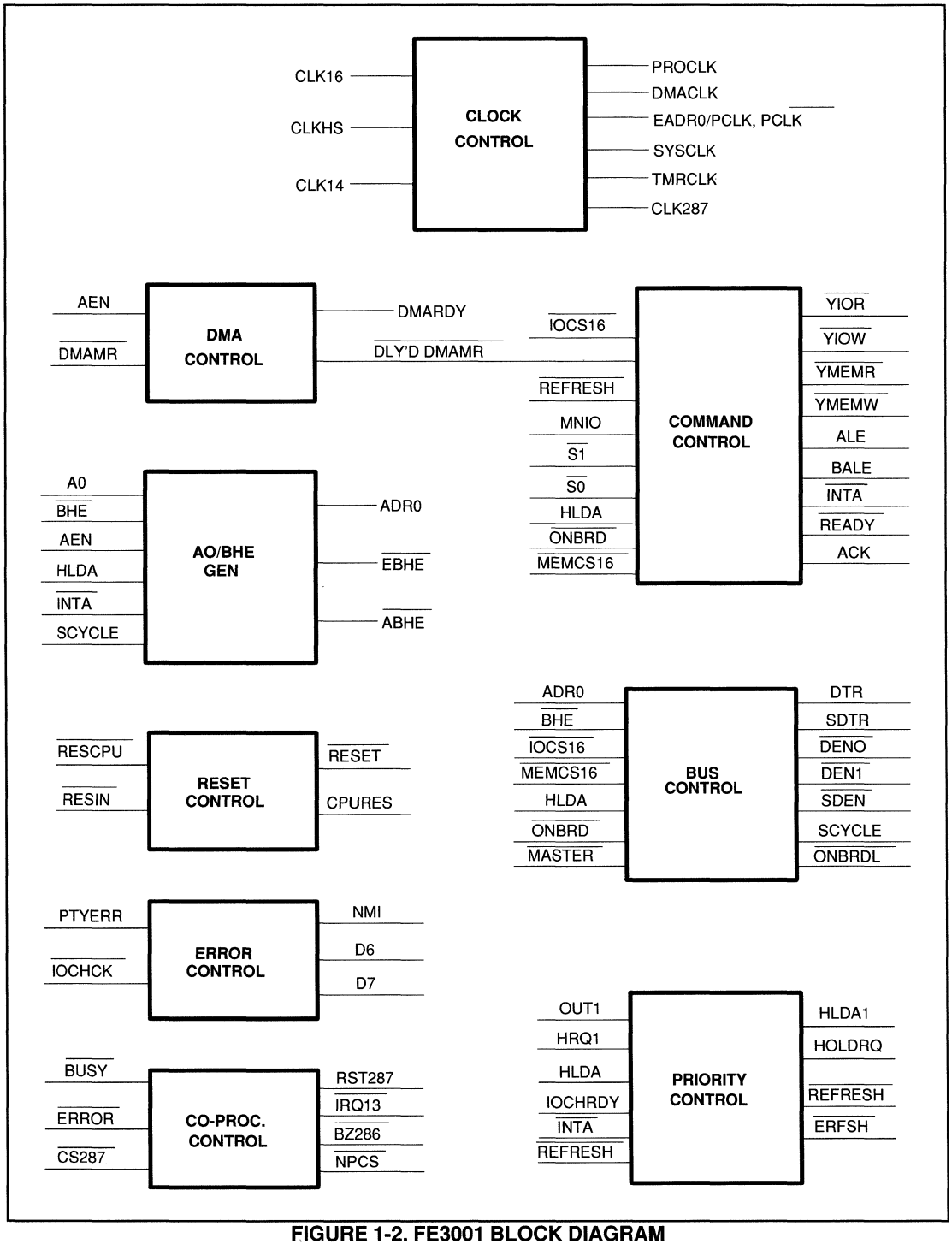


FIGURE 1-2. FE3001 BLOCK DIAGRAM

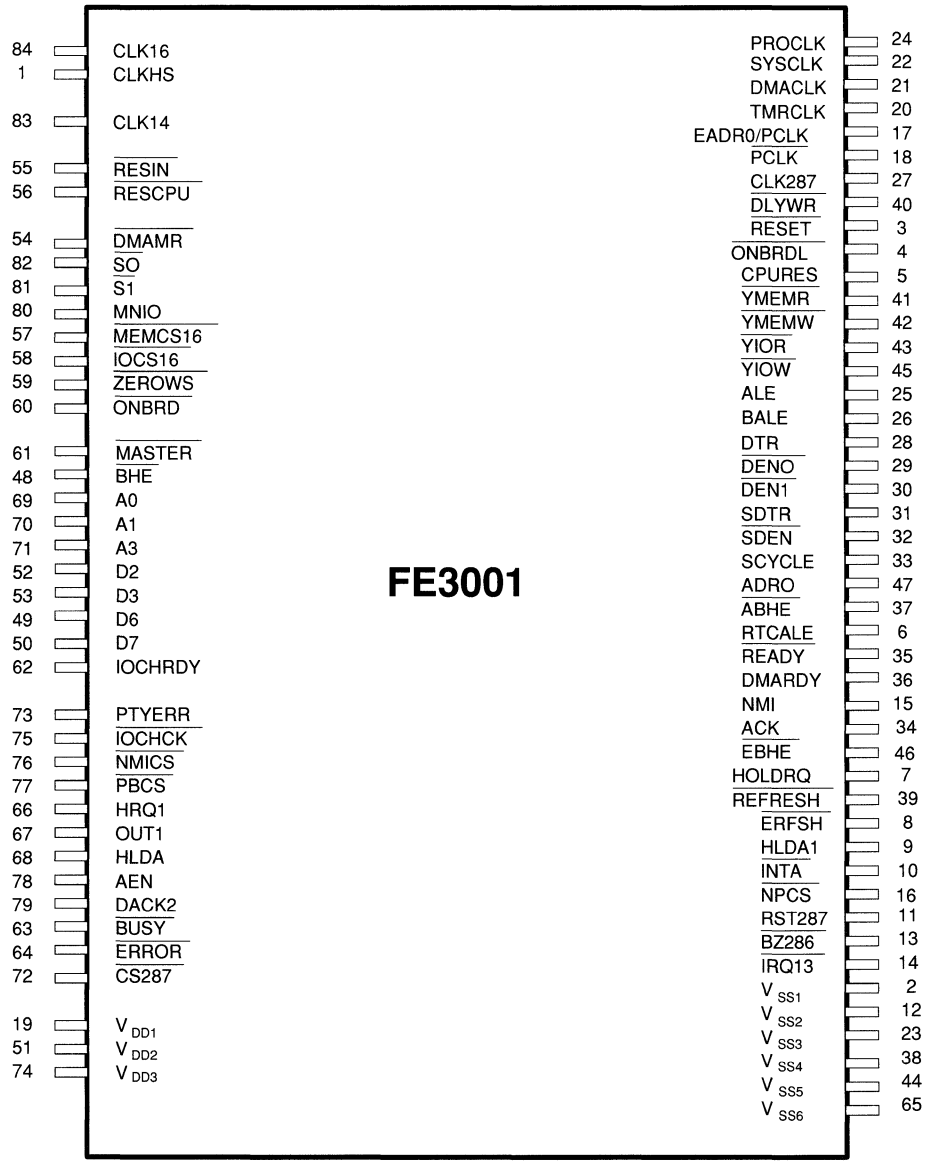


FIGURE 1-3. FE3001 PIN ASSIGNMENTS

PIN#	SIGNAL	TYPE	DESCRIPTION
1	CLKHS	I	High speed clock input. This provides the high speed clock when selected. When CLK16 (pin 84) is pulled high, this input (divided by two) is used as the low speed clock.
2	V_{SS1}		Ground.
3	$\overline{\text{RESET}}$	O	Reset to the system.
4	ONBRDL	O	ONBRD input latched by ALE internally.Follows $\overline{\text{ONBRD}}$ when HLDA high.
5	CPURES	O	Reset to 80286.
6	RTCALE	O	Real Time Clock Address Latch Enable (I/O address 70H).
7	HOLDRQ	O	Hold request to 80286 for DMA or Refresh.
8	$\overline{\text{ERFSH}}$	O	Enable refresh address signal to FE3010. Puts refresh address on address bus.
9	HLDA1	O	DMA hold acknowledge signal to FE3010. Not active during refresh.
10	$\overline{\text{INTA}}$	O	Interrupt acknowledge to FE3010.
11	RST287	O	Reset to 80287 (Write to I/O address F1H or system reset).
12	V_{SS2}		Ground.
13	$\overline{\text{BZ286}}$	O	80287 busy signal to 80286. Latched low by 80287 ERROR signal.
14	$\overline{\text{IRQ13}}$	O	Interrupt request 13 for 80287 error to FE3010.
15	NMI	O	Non-Maskable Interrupt to 80286. Generated in response to a parity error or bus IOCHCK.
16	$\overline{\text{NPCS}}$	O	80287 Co-processor chip select. (I/O Addresses F8H, FAH and FCH).
17	EADR0/PCLK	O	Tristate output to AT bus SA0 & 7.16 MHz clock for keyboard controller.
18	$\overline{\text{PCLK}}$	O	Inverted PCLK.
19	V_{DD1}		+5 V V_{DD}.
20	TMRCLK	O	1.19 MHz timer clock to FE3010.
21	DMACLK	O	Software selectable clock for DMA to FE3010.
22	SYSCLK	O	System clock needed for bus timing. See description in synchronization section.
23	V_{SS3}		Ground.
24	PROCLK	O	Software selectable 80286 clock.
25	ALE	O	Local Address Latch Enable.
26	BALE	O	Bus Address Latch Enable. (Programmable)
27	CLK287	O	Clock for 80287. See clock section for details.
28	DTR	O	Data direction to FE3031 data buffer.
29	$\overline{\text{DEN0}}$	O	Low byte PC/AT Bus data enable to FE3031 data buffer.
30	$\overline{\text{DEN1}}$	O	High byte PC/AT Bus data enable to FE3031 data buffer.
31	SDTR	O	PC/AT Bus byte swap direction to FE3031 data buffer.
32	$\overline{\text{SDEN}}$	O	PC/AT Bus byte swap enable to FE3031 data buffer.
33	SCYCLE	O	Latch low byte during byte swap read.

TABLE 1-1. SIGNAL DESCRIPTIONS

PIN	SIGNAL	TYPE	DESCRIPTION
33	SCYCLE	O	Latch low byte during byte swap read.
34	ACK	O	DMA or Refresh Acknowledge signal to the PC/AT bus.
35	READY	O	Ready to 80286.
36	DMARDY	O	When high allows FE3010 to complete a DMA cycle.
37	ABHE	O	High byte enable for devices on local bus.
38	V_{SS4}		Ground.
39	REFRESH	I/O	Refresh cycle. Generated from FE3010 timer signal OUT1 or externally from the bus.
40	DLYWR	I/O	YIOW delayed to the FE3010, active edge delayed one PROCLK. Input from FE3010 during DMA to generate YIOW.
41	YMEMR	I/O	Memory read. Input during Master cycle.
42	YMEMW	I/O	Memory write. Input during HLDA cycle.
43	YIOR	I/O	I/O read. Input during HLDA cycle.
44	V_{SS5}		Ground.
45	YIOW	I/O	I/O write. Input during Master cycle.
46	EBHE	I/O	High byte enable to expansion bus. Input during Master cycle.
47	ADR0	I/O	Low byte enable. Latched with ALE during a CPU cycle, driven low during 16-Bit DMA cycles.
48	BHE	I/O	High byte enable from the 80286. Output during MASTER and DMA cycles for use by the FE3021.
49	D6	I/O	Peripheral data bus bit 6.
50	D7	I/O	Peripheral data bus bit 7.
51	V_{DD2}		+5 V V_{DD}.
52	D2	I	Peripheral data bus bit 2.
53	D3	I	Peripheral data bus bit 3.
54	DMAMR	I	DMA memory read from DMA controller.
55	RESIN	I	System reset input.
56	RESCPU	I	CPU reset input from keyboard controller.
57	MEMCS16	I	Signals 16 bit memory transfer capability on the PC/AT bus.
58	IOCS16	I	Signals 16 bit I/O transfer capability on the PC/AT bus.
59	ZEROWS	I	Zero wait state bus cycle request. See description for more details.
60	ONBRD	I	16 bit on-board DRAM memory, BIOS, or I/O device. Implies local memory on memory cycles and fast I/O bus timing for I/O cycles.
61	MASTER	I	Master on PC/AT bus has control of the bus when asserted.
62	IOCHRDY	I	Current bus cycle may complete when high. May be used to extend CPU, DMA, or refresh cycles.
63	BUSY	I	80287 co-processor busy.
64	ERROR	I	Error from 80287.
65	V_{SS6}		Ground.
66	HRQ1	I	Hold request from DMA controller in FE3010.

TABLE 1-1. SIGNAL DESCRIPTIONS, Continued

PIN	SIGNAL	TYPE	DESCRIPTION
67	OUT1	I	Refresh timer input from FE3010.
68	HLDA	I	Hold acknowledge from 80286.
69	A0	I	Local 80286 address bus 0.
70	A1	I	Local 80286 address bus 1.
71	A3	I	Local 80286 address bus 3.
72	CS287	I	80287 select decode from FE3021 (0E0H - 0FFH).
73	PTYERR	I	On-board RAM parity error. Sampled on the first falling edge of PROCLK after YMEMR goes high.
74	V_{DD3}		+5 V V_{DD}.
75	IOCHCK	I	Error from PC/AT bus.
76	NMICS	I	NMI port enable decode (07XH). Also used for programming bus control registers.
77	PBCS	I	Port B chip select decode (061H - 06FH, 0DD). See register description for decode definitions.
78	AEN	I	DMA cycle enable from FE3010.
79	DACK2	I	16 bit DMA acknowledge from FE3010.
80	M/IO	I	80286 memory/IO select. High indicates memory halt, or shut-down cycles. Low indicates I/O or interrupt acknowledge cycles.
81	S1	I	80286 Status 1.
82	S0	I	80286 Status 0.
83	CLK14	I	14.318 MHz clock input used to derive TMRCLK, EADR0/PCLK, and PCLK.
84	CLK16	I	16 MHz clock input. This provides the low speed CPU clock for 8 MHz operation. When this pin is pulled high, CLKHS ÷ 2 is used as the low speed clock.

TABLE 1-1. SIGNAL DESCRIPTIONS, Continued

2.0 FUNCTIONAL DESCRIPTION

2.1 OVERVIEW

The FE3001 is designed to run with the FE3010 peripheral controller, and the FE3021 and FE3031 buffers/memory controls to create a 16 MHz or 20 MHz PC/AT compatible system. The basic architecture of an AT compatible system using the FE3600B chip set involves putting the system DRAM on the local data and command bus, allowing high speed access. The BIOS ROM can be put on the local bus or expansion bus; the FE3021 has provisions especially to use the ROM on the higher speed bus. During accesses to local memory, the data buffer controls in the FE3001A prevent data collisions between the local and expansion buses. The FE3021 and FE3031 also inhibit memory read and write signals to the expansion bus for local memory accesses.

The FE3001 generates all of the clocks needed in the system. The CPU clock to the 80286 processor (PROCLK) is programmable, as is the DMA clock for the DMA controller in the FE3010 (DMACLK). The expansion bus clock (SYSCLK) and coprocessor clock for the 80287 (CLK287) automatically adjust to the current operating configuration. The clock for the timers in the FE3010 (TMRCLK) is fixed at 1.19 MHz, and the clocks for the keyboard controller (PCLK and $\overline{\text{PCLK}}$) are fixed at 7.16 MHz.

The FE3001 has registers to delay the five commands (memory read and write, I/O read and write, interrupt acknowledge) during a CPU cycle and control the length of the commands based on various input signals (16-bit memory, 16-bit I/O, on-board memory, fast 16-bit I/O device, and zero wait state device). On power-up, these registers are loaded with values to run the system with a 16 MHz PROCLK (8 MHz system) with full AT compatibility and no register programming necessary. Before switching to high speed operation, it is necessary to program the registers for proper bus emulation. These registers eliminate the need to either slow down the processor for expansion bus operations or run the bus asynchronously. Note that a 16 MHz system can be made to exactly match the bus timing of an 8 MHz system.

2.2 CLOCK GENERATOR

This module generates clocks for the CPU, DMA, 8042 keyboard controller, timer and 80287 Numeric Processor. The CPU clock is software selectable for low speed or high speed CPU operation. The DMA clock is also software selectable between standard and high speed. The 80287 clock is fixed at the low speed CPU clock.

2.2.1 PROCLK

The CLK16 and CLKHS input clocks to the FE3001 are used to create the low speed and high speed clocks to the CPU. The CLKHS input is used when the high speed CPU clock is selected. If the CLK16 input is connected to an oscillator, it will be used when the low speed CPU clock is selected (typically from 6 to 8 MHz CPU speed). Alternatively, if CLK16 is tied high through a pullup resistor, then CLKHS ÷ 2 will be used as the low speed clock, saving an oscillator.

The CPU clock circuitry ensures a glitchless speed switch. PROCLK will be held high at most 1 1/2 clock periods of the clock being selected in order to achieve synchronization. Since SYSCLK and DMACLK are based on PROCLK, they will also switch speeds without glitches.

2.2.2 DMACLK

DMACLK can be software selected between standard speed and a special high speed mode. Standard speed provides a 4 MHz DMA clock to the DMA controller on a 16 MHz system, the same as an 8 MHz IBM PC/AT. This will be the most common selection of DMA speed. Selecting high speed DMA runs the DMA controller at twice standard speed. This would likely be confined to special dedicated systems where only well defined DMA peripherals that can run that fast are used.

DMACLK is PROCLK ÷ 4 when the low speed CPU clock is selected. DMACLK is PROCLK ÷ 8 when the high speed CPU clock is selected. DMACLK will always change on CPU "t" state boundaries, but no other synchronization is attempted. The previous discussion applies to standard speed DMA. If high speed DMA is selected, it runs twice as fast in all cases.

2.2.3 CLK287

CLK287 is always the same as the low speed CPU clock. It is not affected by speed switching. It follows CLK16 if that input is toggling or is CLKHS ÷ 2 if CLK16 is pulled high.

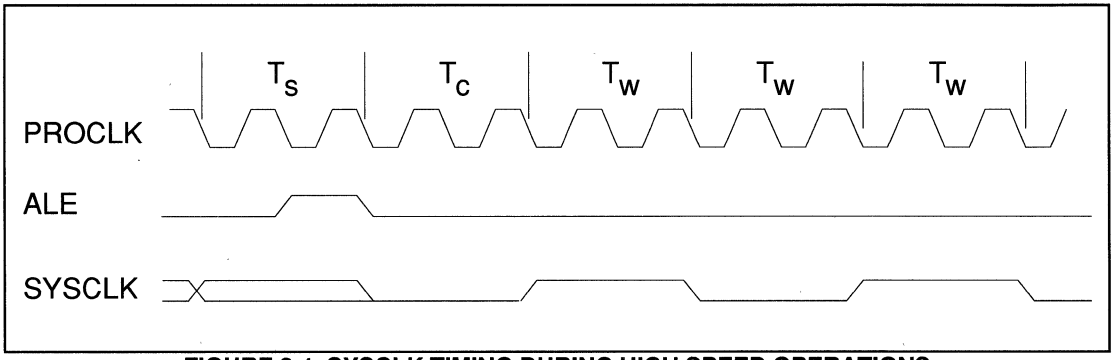


FIGURE 2-1. SYSCLK TIMING DURING HIGH SPEED OPERATIONS

2.2.4 SYSCLK

When the low speed clock is selected, SYSCLK is PROCLK ÷ 2. During high speed operation, SYSCLK is PROCLK ÷ 4. In the high speed case, SYSCLK is brought into sync with the PC/AT bus at the end of ALE. See Figure 2-1 for SYSCLK functional timing.

2.2.5 EADR0/PCLK, $\overline{\text{PCLK}}$, and TMRCLK

The CLK14 input is used to generate EADR0/PCLK, $\overline{\text{PCLK}}$, and TMRCLK. It must be 14.31818 MHz in order for TMRCLK to be 1.1932 MHz, as required for the timers in the FE3010 to be AT compatible. TMRCLK is CLK14 ÷ 12. EADR0/PCLK is CLK14 ÷ 2 (7.16 MHz). $\overline{\text{PCLK}}$ is the complement of EADR0/PCLK. EADR0/PCLK and $\overline{\text{PCLK}}$ can be used to drive the 8042 keyboard controller.

2.2.6 STOPPING THE CLOCKS (SLEEP MODE)

Software may put the FE3001 in sleep mode by setting port 063H bit 6. In sleep mode, PROCLK and DMACLK will be stopped at a high level. SYSCLK will also be stopped, but at an indeterminate logic level. DMACLK and PROCLK will each stop on their first rising edge after HLDA is seen active by the FE3001. Typically, this would be the first refresh cycle after the sleep bit is written. SYSCLK will stop with PROCLK.

By stopping these clocks, power can be conserved in battery operated systems. Note that a static CMOS 80286 must be used in order to stop the CPU clock. EADR0/PCLK, $\overline{\text{PCLK}}$, TMRCLK, and CLK287 will continue to run in sleep mode, allowing the keyboard controller, timers, and coprocessor to operate. Either a keyboard interrupt or a system clock interrupt is a likely choice to wake the CPU up.

To restart the clocks (wake up the CPU), the $\overline{\text{RESCPU}}$ input must be pulsed low. The rising edge of $\overline{\text{RESCPU}}$ will kick off internal synchronization that will restart the clocks roughly 2 EADR0/PCLK periods later. No glitches will occur on the clocks as a result of a restart. Also note that the pulse on $\overline{\text{RESCPU}}$ will not reset the CPU if the FE3001 is in sleep mode. Refer to Application Notes for information on external logic needed to implement sleep mode.

2.3 COMMAND CONTROL

This module generates the I/O read and write commands, memory read and write commands, interrupt acknowledge, ALE and BALE from $\overline{\text{S1}}$, $\overline{\text{S0}}$, and MNIO. It also controls the number of wait states used during each CPU cycle. See the register descriptions for programming information. For recommended program values, refer to Appendix A.

2.3.1 ON-BOARD CYCLES

When the $\overline{\text{ONBRD}}$ signal is active, then this cycle is directed toward 16-bit, high speed local DRAM, BIOS, or I/O. The timing for these cycles is defined by registers R9, R10, and R12. The AT bus timing signals $\overline{\text{MEMCS16}}$ and $\overline{\text{IOCS16}}$ have no effect. IOCHRDY can be used to lengthen the cycle, and indeed is used by the FE3021 to add wait states for a DRAM page miss or EMS cycles.

The wait states for on-board reads and writes are individually programmable by registers R9 and R10 in order to optimize DRAM access speed. Both memory and I/O cycles use these values.

The command delay for on-board I/O cycles is set by register R12. The command delay for on-board memory cycles is always zero.

2.3.2 AT BUS CYCLES

All I/O and memory cycles where ONBRD is inactive will be directed to the AT bus. The command delay and wait states are programmable for each type of AT bus cycle. Refer to section 3 for more details.

Memory cycles use 16-bit timing when MEMCS16 is driven low before either the memory command (YMEMR or YMEMW) is programmed to go active or BALE falls, whichever is earlier. I/O cycles use 16-bit timing when IOCS16 is driven low before the I/O command (YIOR or YIOW) is programmed to go active. Otherwise, all cycles use 8-bit timing.

ZEROWS can be driven low for either 8-bit or 16-bit cycles to terminate the cycle early. As on the AT, it should not be driven until a command is active. It will cause the cycle to end after the prescribed minimum number of wait states in register R8 is met. Note that the FE3001 contains circuitry to ensure that an AT bus cycle will end (command goes high) on a rising edge of SYSCLK and will add a wait state if needed to enforce this. This synchronization circuitry will override register programming and the IOCHRDY and ZEROWS inputs.

2.3.3 OTHER CYCLES

Interrupt acknowledge cycles follow the same command timing as an 8-bit AT bus cycle. HALT cycles do not generate ALE, BALE or cause the READY output to go high. Effectively, the FE3001A does not respond to a HALT cycle. A SHUTDOWN cycle is handled like a HALT, except that it causes the CPURES line to be pulsed, resetting the CPU only.

2.4 BUS CONTROL

This module generates the data buffer controls for CPU, DMA, and refresh cycles. DEN0 and DEN1 are used to enable the lower and upper bytes of the FE3031 AT Bus data buffers, respectively. DTR sets the direction of these buffers. SDEN and SDTR control the enable and direction of a buffer which transfers data between the upper and lower bytes of the AT data bus. The rising edge of SCYCLE latches data on the lower byte of the AT bus into the FE3031, needed for 16-bit to 8-bit bus conversion cycles. ONBRDL is ONBRD latched by ALE to keep it valid throughout the cycle.

The ONBRD signal is used to indicate on-board DRAM and I/O operations. On-board memory and fast on-board I/O devices are assumed to be 16 bit devices. During CPU cycles which access on-board memory, the AT data buffers will be disabled. For Bus Master and DMA cycles, ONBRD must be decoded only for on-board memory.

2.5 A0/BHE GENERATOR

This module generates the system ADR0, ABHE, and EBHE using A0 and BHE from the 80286 CPU and AEN and DACK2 from the DMA controller in the FE3010.

2.5.1 ADR0

During CPU cycles, A0 from the 80286 is latched with ALE to produce ADR0. For 16 bit DMA transfers and interrupt acknowledge cycles, ADR0 is forced low so that the low byte of the data bus is activated. For all other CPU hold conditions ADR0 is tri-stated. The FE3001 performs two cycles when the CPU attempts a 16 bit operation to an 8-bit device on an even address boundary. ADR0 is automatically forced to one at the start of the second cycle to select the second byte.

2.5.2 ABHE

ABHE is the local upper byte select used by the FE3031. During CPU cycles, ABHE is BHE latched with ALE. It is forced low during 16-bit DMA (DACK2 and AEN inputs high) so that the upper byte is always selected. For 8-bit DMA, it is the inversion of ADR0 so that only one byte is selected at a time. During master mode, ABHE follows the EBHE input.

2.5.3 EBHE

EBHE is the upper byte select to the AT bus. During CPU cycles, EBHE is ABHE latched with BALE to provide proper AT bus timing. During DMA, EBHE follows ABHE. During refresh the EBHE output is disabled. It is an input during Master Mode transfers.

2.6 PRIORITY CONTROL

The Priority Control module generates the hold request signal to the CPU in response to a request from the DMA controller or refresh timer.

2.6.1 REFRESH CYCLES

The FE3001 generates a hold request in response to a rising edge on the OUT1 input, sig-

nalling that a refresh cycle is needed. A refresh cycle is initiated when HLDA comes back from the CPU. The FE3001 refresh state machine drives REFRESH low to signal a refresh cycle to the AT bus, and sets ERFSH low to the FE3010 to enable the refresh address onto the CPU address bus. YMEMR will also be strobed low during a refresh cycle. Refer to the timing diagrams for more detail. Note that REFRESH is a bidirectional open-collector signal, and a refresh cycle can be started by an expansion card.

2.6.2 DMA CYCLES AND REQUEST ARBITRATION

Requests for control by the DMA controller are made by taking the HRQ1 input high. The FE3001 grants control to the DMA controller by setting HLDA1 high.

When the FE3001 receives a HLDA, it grants control either to the refresh state machine (REFRESH goes low) or to the DMA controller (HLDA1 goes high). Priority is given to the refresh state machine in the event of simultaneous requests. Note that if simultaneous requests do exist, then HOLDRQ will not be dropped after the first request is satisfied. Instead, the FE3001 will grant control sequentially to both requestors with the same HLDA.

2.7 DMA CONTROL

This module generates the DMARDY signal for the FE3010 peripheral controller. This signal indicates that the DMA may complete its cycle. The module also generates YMEMR during DMA by delaying the leading (falling) edge of the FE3010 DMAMR signal by one DMA clock.

2.8 ERROR CONTROL

This module generates a non-maskable interrupt (NMI) to the 80286 when a parity error or system bus error is encountered. Parity error, system bus error or NMI can be enabled or disabled from software. They are all disabled on system reset.

The PTYERR input is examined each time YMEMR goes high and it is an on-board cycle (ONBRDL low). The state of the PTYERR input is actually latched on the first falling edge of PROCLK after YMEMR goes high. This applies to all on-board reads including CPU, DMA, and Bus Master cycles. If PTYERR was high, it signals a parity failure and will generate an NMI to the CPU if enabled. The parity error latch can be cleared by disabling and then enabling parity errors.

The IOCHCK input is driven low by a device on the AT bus to signal a catastrophic error, such as a parity error on a plug-in RAM card. A low on the IOCHCK input will generate an NMI to the CPU if enabled. The error condition can be cleared by disabling and then enabling IOCHCK. However, the IOCHCK input must also be reset high or it will generate another NMI.

When the CPU receives an NMI, it can interrogate I/O register 061H (PORT B) to determine whether a parity error or an IOCHCK is the source of the interrupt. Note that this is the only time the FE3001 will drive the data bus. All other I/O locations are write only. Also, only bits 6 and 7 will be driven during the read. The FE3010 will supply the 6 lower order bits.

2.9 COPROCESSOR INTERFACE

The Coprocessor Interface module provides the system interface to the 80287 Numeric Processor Extension. The reset and chip select to the 80287 are generated in this module in addition to the busy signal to the CPU and interrupt request 13 to the interrupt controller.

In a FE3600 system, as in any PC/AT compatible system, ERROR from the 80287 coprocessor is not connected to the ERROR input on the 80286. Instead, the ERROR input on the 80286 is tied high, while BUSY and interrupt request 13 are used to flag errors. The FE3001 has a BZ286 output which connects to the BUSY input of the 80286. It also has ERROR and BUSY inputs which hook to those outputs from the 80287.

Normally, BZ286 just follows the BUSY input. However, when ERROR goes low while BUSY is low, IRQ13 will go active to signal the CPU that a coprocessor error has occurred. IRQ13 will stay active until ERROR goes back high. Also, BZ286 will be latched low to prevent another coprocessor instruction from being loaded. BZ286 will stay low until either the 80287 is reset or there is a write to I/O address 0F0H. When either of these occurs, then BZ286 will return to following the BUSY input.

The FE3001 RST287 output connects to the 80287 RESET input. This allows the coprocessor to be reset through software by an I/O write to address 0F1H. It will also be reset when the sys-

M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	TYPE OF BUS CYCLE
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	None, not a status cycle
1	0	0	Halt (if A1 =1) or Shutdown (if A1 = 0)
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	None, not a status cycle

TABLE 2-1. BUS CYCLES

tem $\overline{RESET}$ output is active.

The FE3001 expects the $\overline{CS287}$ input to be active for addresses 0E0H-0FFH. This is used to provide the $\overline{NPCS}$ chip select decode output for the 80287. It will be active for addresses 0E8H-0EFH and 0F8H-0FFH when $\overline{INTA}$ is high and M/$\overline{IO}$ from the CPU was low for this cycle.

2.10 RESET CONTROL

This module generates the CPURES signal which is used to reset only the 80286 and the $\overline{RESET}$ signal which resets the rest of the system (including the FE3001). The $\overline{RESIN}$ input causes a full system reset when driven low. Both CPURES and $\overline{RESET}$ will go active for as long as $\overline{RESIN}$ is low and for at least 30 PROCLK cycles after $\overline{RESIN}$ goes high.

The $\overline{RESCPU}$ input, when driven low, causes only the CPURES output to go high. $\overline{RESCPU}$ would normally be connected to both the 8042 keyboard controller and the FE3021 (to provide "hot" reset). The CPURES output will stay high for at least 4 DMACLK periods, longer if $\overline{RESCPU}$ remains low. CPURES will also go high for 4 DMACLK periods if the 80286 executes a Shutdown cycle.

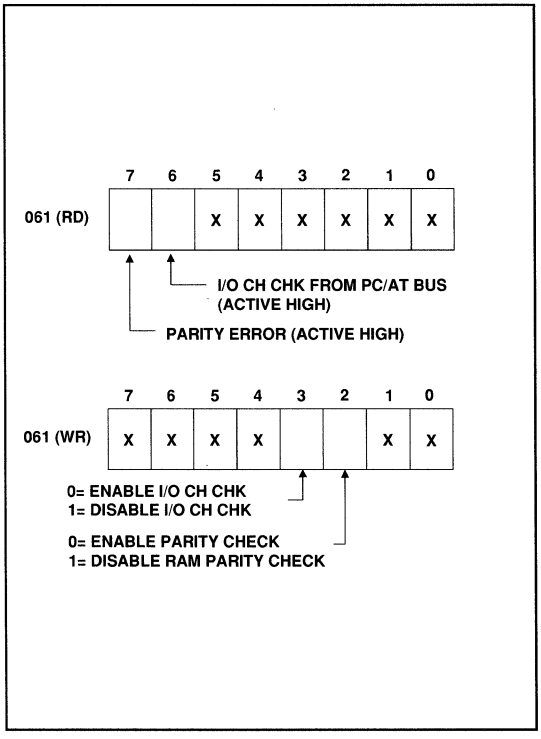
2.11 GENERAL NOTES

- *$\overline{ONBRD}$ must not be active during interrupt acknowledge cycles.*
- *For memory cycles with $\overline{ONBRD}$ asserted, the system will use the MDATA bus of the FE3031 for data transfers. For I/O cycles with $\overline{ONBRD}$ asserted, the system will use the expansion bus (DATA) of the FE3031 for data transfers.*
- *On-board I/O devices must drive $\overline{IOCS16}$ in order for a Bus Master to access them as 16-bit devices. Otherwise, $\overline{SDEN}$ will go low for Bus Master I/O cycles where ADR0 is high.*
- *Inputs CLK16, $\overline{BUSY}$, $\overline{ERROR}$, and $\overline{CS287}$ have internal 100k Ω (approx.) pull-up resistors.*

3.0 REGISTERS

3.1 ERROR CONTROL REGISTER (061H), READ/WRITE

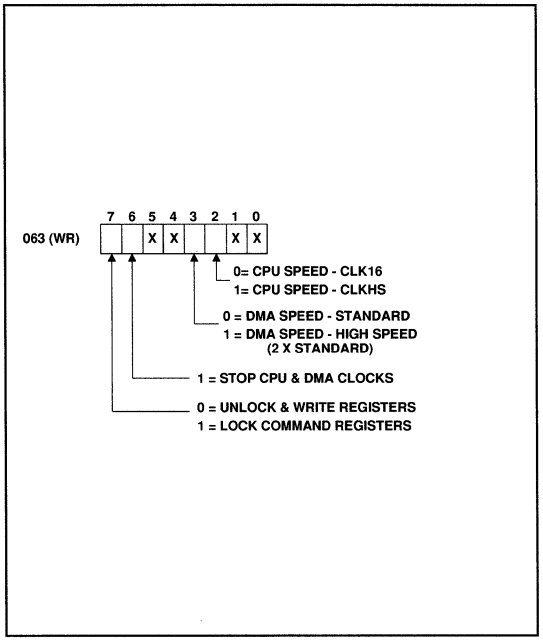
The error control register contains masks for the on-board RAM parity check and I/O channel check signals. It also provides a read port to check the status of these signals.



3.2 SPEED SELECT (063H), WRITE

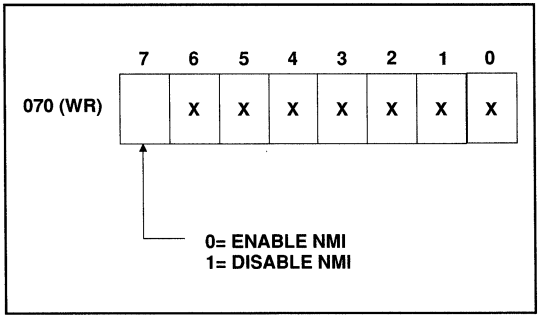
The speed select register controls the speed of the CPU and DMA clocks. This register is also used to stop the CPU (sleep mode) and unlock the command control and speed select registers for access. The lock bit must be reset and D7 must be low to change speed or stop clocks.

The Stop Clock bit stops all the clocks except for the timer clock, coprocessor clock, and keyboard controller clocks. This allows refresh to continue. Bits 2,3, and 6 in the register are cleared and bit 7 is set by system reset.



3.3 NMI ENABLE (070H), WRITE

The NMI enable register contains the mask for NMI to the 80286. Bit 7 is set on power-up.



3.4 COMMAND CONTROL REGISTERS (072H,073H), WRITE

The timing of the command controls on the expansion bus is programmable via the Command Control Registers. These registers control the timing of BALE, YMEMR, YMEMW, YIOR, YIOW, INTA and the number of wait states in a CPU cycle. This section describes the programming of these registers. Recommended program values for CPU clock speeds of 16, 25, and 32 MHz are provided in Appendix A.

The programmable bus signals are shown in Figure 3-1. A summary of the timing registers is shown in Table 3-1.

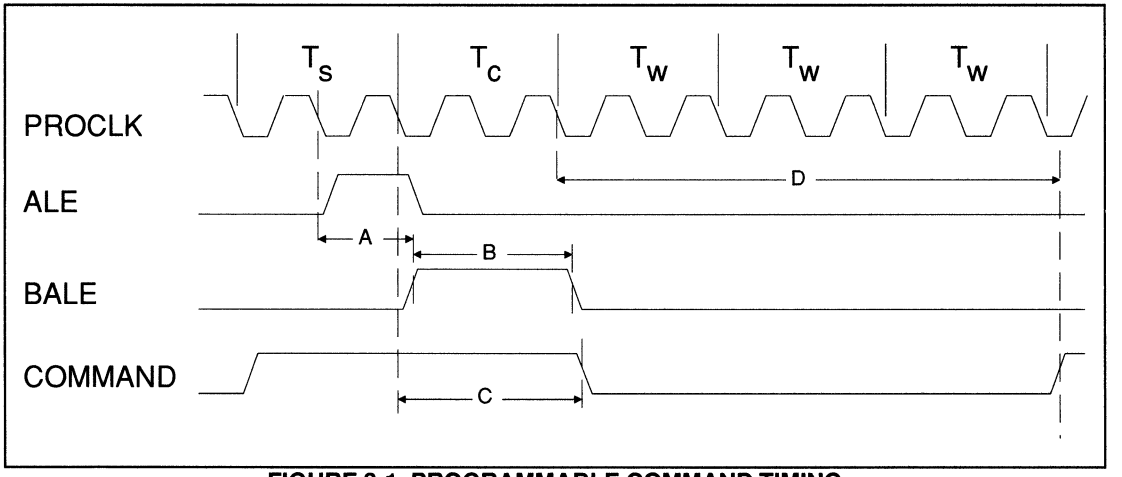


FIGURE 3-1. PROGRAMMABLE COMMAND TIMING

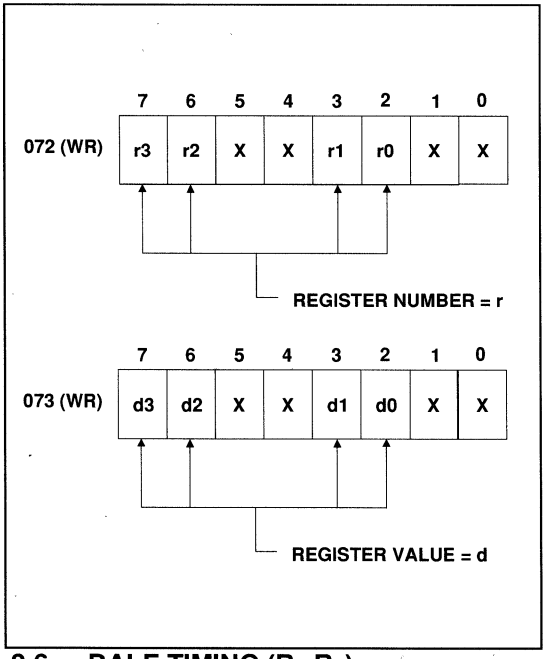
REG	BITS	FUNCTION	WAVEFORM	DEFAULT	RANGE
R_0	2	BALE delay from ALE leading edge	A	0	0 - 3
R_1	2	BALE width	B	1	1 - 3
R_2		Not used			
R_3	4	8-bit memory, 8/16-bit I/O - command delay	C	1	0 - 15
R_4	4	8-bit operation - wait states	D	4	0 - 15
R_5	4	16-bit I/O operation - wait states	D	1	0 - 15
R_6	4	16-bit memory operation - command delay	C	0	0 - 15
R_7	4	16-bit memory operation - wait states	D	1	0 - 15
R_8	4	Minimum number of wait states when ZEROWS is asserted - wait states	D	0	0 - 15
R_9	4	On-board 16-bit read cycle - wait states	D	1	0 - 15
R_{10}	4	On-board 16-bit write cycle - wait states	D	1	0 - 15
R_{11}		Not used			
R_{12}	4	On-Board I/O operation - command delay	C	1	0 - 15

TABLE 3-1. SUMMARY OF COMMAND TIMING REGISTERS

- *Command delay is number of PROCLKs from end of T_S*
- *Each wait state is two PROCLKs.*
- *One wait state may be added in high speed mode for synchronization.*

3.5 COMMAND REGISTER POINTER (072H)

The Command Register Pointer points to one of 11 registers at location 073H. Each register contains a command timing parameter based on the selected CPU clock. Whichever register number is loaded in bits 7,6,3, and 2 in location 072H is the register which is loaded with the next write to address 073H. Refer to Table 3 -1 for details.



3.6 BALE TIMING (R_0,R_1)

The leading edge and width of BALE are controlled by these two registers. BALE delay is defined as the number of PROCLK cycles from the leading edge of ALE. BALE width is the width in PROCLK cycles.

Default values: Delay (R_0) - 0
Width (R_1) - 1

3.7 8-BIT MEMORY AND 8/16-BIT I/O COMMAND DELAY (R_3)

This register controls the command delay for 8-bit memory and 8/16-bit I/O operations. Command delay is defined as the number of PROCLK cycles from the trailing edge of ALE to the start of the command.

Default value: Command Delay (R_3) - 1

3.8 8-BIT MEMORY AND I/O WAIT STATES (R_4)

This register controls the number of wait states for 8-bit operations. The number of wait states is the number of CPU wait states required for these operations.

Default value: Wait States (R_4) - 4

3.9 16-BIT I/O WAIT STATES (R_5)

This register controls the number of wait states for 16-bit I/O cycles. These cycles are indicated by the assertion of $\overline{IOCS16}$. The number of wait states is the number of CPU wait states required for this operation.

Default values: Wait States (R_5) - 1

3.10 16-BIT AT BUS MEMORY TIMING (R_6,R_7)

These registers control the command delay and number of wait states for 16-bit memory operations. These cycles are indicated by the assertion of $\overline{MEMCS16}$. Command delay is defined as the number of PROCLK cycles from the trailing edge of ALE. The number of wait states is the number of CPU wait states required for this operation.

Default values: Command Delay (R_6) - 0
Wait States (R_7) - 1

3.11 $\overline{ZER0WS}$ BUS CYCLE WAIT STATES

This register sets the minimum number of wait states which must occur before the assertion of the $\overline{ZER0WS}$ signal can terminate a cycle.

Default values: Wait States, $\overline{ZWS}$ (R_8) - 0

3.12 ON-BOARD MEMORY TIMING (R_9,R_{10})

These two registers control the number of wait states for on-board operations. These cycles are indicated by the assertion of $\overline{ONBRD}$ during CPU cycles. Command delay is zero for all on board memory operations. The number of wait states is the number of CPU wait states required for this operation. There are separate registers to program the number of wait states for read and write operations to give the system designer added flexibility and potential for greater speed.

Default values: Wait States,Read (R_9) - 1
Wait States,Write (R_{10}) - 1

3.13 ON-BOARD I/O TIMING (R_{12})

This register controls the command delay for 16-bit on-board I/O operations. These cycles are indicated by the assertion of $\overline{ONBRD}$ during CPU I/O cycles. Command delay is defined as the number of PROCLK cycles from the trailing edge of ALE. The number of wait states for on-board I/O is defined by the on-board memory registers described above. Additional wait states can be added by using the IOCHRDY signal.

Default values: Command Delay (R_{12}) - 1

3.14 CLEAR 80287 BUSY (0F0H), WRITE

When an error signal is received from the 80287, the $\overline{BZ286}$ signal is latched low. The latch is cleared by an OUT instruction to this port. The output data is don't care.

3.15 RESET 80287 (0F1H), WRITE

An OUT instruction to this port generates a reset to the 80287.

4.0 PACKAGE

The FE3001 is packaged in a 84-pin PLCC.

5.0 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature (operating): 0° to + 70° C
Storage Temperature: -40° to +125° C
Voltage on any pin to ground: - .5 V to +7 V
Power Dissipation: 400 mW

6.0 DC CHARACTERISTICS

Refer to Table 6-1 below.

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{IL}	Input LOW Voltage		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V	
I_{OL}	LOW V Output Current[1,4]	4		mA	V_{OL}= 0.4 V
I_{OH}	HIGH V Output Current[1]	-4		mA	V_{OH}= 2.4 V
I_{OL}	LOW V Output Current[2]	8,20[3]		mA	V_{OL}= 0.4 V
I_{OH}	HIGH V Output Current[2]	-8		mA	V_{OH}= 2.4 V
V_{OHC}	PROCLK Out HIGH Volt	3.8		V	I_{OH}= -2 mA
V_{DD}	Supply Voltage (Any V_{DD})	4.5	5.5	V	
I_{DD}	Supply Current (Total)			mA	

TABLE 6-1. DC CHARACTERISTICS

- *1. Output currents are for DMACLK, TMRCLK, PCLK, $\overline{PCLK}$, CLK287, CPURES, ALE, RTCALE, DTR, SDTR, $\overline{DEN0}$, $\overline{DEN1}$, $\overline{SDEN}$, SCYCLE, $\overline{READY}$, DMARDY, $\overline{NPCS}$, RST287, $\overline{BZ286}$, IRQ13, NMI, HOLDRQ, $\overline{ERFSH}$, HLDA1, $\overline{INTA}$, $\overline{DLYWR}$, $\overline{ABHE}$, $\overline{BHE}$, $\overline{ONBRDL}$.*
- *2. Output currents are for $\overline{RESET}$, $\overline{YMEMR}$, $\overline{YMEMW}$, $\overline{YIOR}$, $\overline{YIOW}$, D6, D7, ADR0, SYSCLK, BALE, $\overline{EBHE}$, ACK.*
- *3. Output current for $\overline{REFRESH}$ should be 20 mA at 0.4V. This is an I/O pin which is only driven low in output mode. It is in a tri-state condition otherwise. A 300 ohm pull-up resistor is needed to bring the output high.*
- *4. Output low current for PROCLK.*

7.0 TIMING PARAMETERS

(T_a=0° to 70°C, V_{DD}=4.5 to 5.5V,C_L=50pf)

SYMBOL	PARAMETER	16 MHz MIN	16 MHz MAX (NS)
T1	ALE rising edge delay from PROCLK		12
T2	ALE falling edge delay from PROCLK		15
T3	BALE rising edge delay from PROCLK		21
T4	BALE falling edge delay from PROCLK		20
T5	$\overline{YMEMR}$, $\overline{YMEMW}$ fall delay from PROCLK		16
T6	$\overline{YMEMR}$, $\overline{YMEMW}$ rise delay from PROCLK		19
T7	$\overline{YIOR}$, $\overline{YIOW}$ falling delay from PROCLK		20
T8	$\overline{YIOR}$, $\overline{YIOW}$ rising delay from PROCLK		20
T11	$\overline{READY}$ falling edge delay from PROCLK		12
T12	$\overline{READY}$ rising edge delay from PROCLK		16
T13	DTR fall delay from PROCLK; read cycle		20
T16	$\overline{DEN0}$, $\overline{DEN1}$ rise delay from PROCLK; read cycle		18
T17	$\overline{DEN0}$, $\overline{DEN1}$ low delay from PROCLK; write cycle		28
T18	$\overline{DEN0}$, $\overline{DEN1}$ rise delay from PROCLK; write cycle		24
T21	$\overline{S1}$, $\overline{S0}$ setup time to PROCLK	13	
T23	$\overline{ONBRD}$ setup time to PROCLK; memory cycle	22	
T24	$\overline{ONBRD}$ setup time to PROCLK; I/O cycle	32	
T25	$\overline{MEMCS16}$ setup time to PROCLK	32	
T26	$\overline{IOCS16}$ setup time to PROCLK	35	
T27	IOCHRDY setup time to PROCLK	12	
T28	IOCHRDY hold time from PROCLK	0	
T30	$\overline{S1}$, $\overline{S0}$ hold time from PROCLK	1	
T31	A0 setup time to PROCLK	10	
T32	$\overline{BHE}$ setup time to PROCLK	2	
T33	$\overline{BHE}$ hold time from PROCLK	15	
T34	A0 hold time from PROCLK	15	
T35	$\overline{ABHE}$ delay from PROCLK		21
T36	ADR0 delay from PROCLK		20
T37	$\overline{EBHE}$ delay from PROCLK		28
T38	$\overline{ONBRD}$ hold time from PROCLK	10	

TABLE 7-1. TIMING PARAMETERS

SYMBOL	PARAMETER	16 MHz MIN	16 MHz MAX (NS)
T39	$\overline{\text{ONBRDL}}$ delay from $\overline{\text{ONBRD}}$		19
T40	$\overline{\text{ONBRDL}}$ delay from PROCLK		24
T41	CLK14 period	69	
T42	CLK14 low time	27	
T43	CLK14 high time	27	
T44	EADR0 /PCLK rise/fall delay from CLK14 falling		29
T45	$\overline{\text{PCLK}}$ rise/fall delay from CLK14 falling		24
T46	TMRCLK rise/fall delay from CLK14 falling		27
T47	CLKHS period	31	
T48	CLKHS high time	14	
T49	CLKHS low time	14	
T50	PROCLK falling edge delay from CLKHS fall; High speed PROCLK selected		20
T51	PROCLK rising edge delay from CLKHS rising; High speed PROCLK selected		16
T52	PROCLK duty cycle skew (T50 - T51); High speed PROCLK selected. PROCLK low time = T49 - T52 PROCLK high time = T48 + T52	- 2	4
T53	PROCLK rise/fall delay from CLKHS falling; Low speed PROCLK, CLK16 tied to +5V		26
T54	CLK287 rise/fall delay from CLKHS falling; CLK16 input tied to +5V		18
T55	CLK16 period	62	
T56	CLK16 high time	28	
T57	CLK16 low time	28	
T58	PROCLK rise/fall delay from CLK16 ; low speed PROCLK, CLK16 toggling		22
T59	CLK287 rise/fall delay from CLK16 ; CLK16 toggling		18
T60	SYSCLK rise/fall delay from PROCLK; Low speed PROCLK selected		17
T61	SYSCLK rise/fall delay from PROCLK; High speed PROCLK selected		17
T62	DMACLK rise/fall delay from PROCLK; Divide by 2		30
T63	DMACLK rise/fall delay from PROCLK; Divide by 4		37

TABLE 7-1. TIMING PARAMETERS, Continued

SYMBOL	PARAMETER	16 MHz MIN	16 MHz MAX (NS)
T64	DMACLK rise/fall delay from PROCLK; Divide by 8		37
T65	M/$\overline{IO}$ setup time to $\overline{S0}$, $\overline{S1}$ falling edge	4	
T66	M/$\overline{IO}$ hold time from PROCLK (end of Ts)	15	
T67	DTR rise delay from PROCLK; read cycle		24
T68	SDTR rise delay from PROCLK		24
T69	SDTR fall delay from PROCLK		30
T70	PTYERR setup time to PROCLK	11	
T71	PTYERR hold time from PROCLK	4	
T72	$\overline{MEMCS16}$ hold time from PROCLK	17	
T73	$\overline{DEN0}$ low delay from PROCLK; read cycle		27
T74	$\overline{DEN1}$ low delay from PROCLK; read cycle		25
T75	$\overline{ZER0WS}$ setup time to PROCLK	24	
T76	$\overline{ZER0WS}$ hold time from PROCLK	0	
T77	$\overline{DEN0}$, $\overline{DEN1}$ low delay from $\overline{ONBRD}$ high; write cycle		28
T78	$\overline{IOCS16}$ hold time from PROCLK	5	
T79	$\overline{DLYWR}$ falling edge delay from PROCLK		13
T80	$\overline{DLYWR}$ rising edge delay from PROCLK		23
T81	$\overline{SDEN}$ falling edge delay from PROCLK		30
T82	$\overline{SDEN}$ rising edge delay from PROCLK; $\overline{YMEMR}$, $\overline{YMEMW}$, or $\overline{YIOR}$ active		32
T83	$\overline{SDEN}$ rising edge delay from PROCLK; $\overline{YIOW}$ active		16
T84	SCYCLE rising edge delay from PROCLK		17
T85	SCYCLE falling edge delay from PROCLK		22
T86	$\overline{INTA}$ falling edge delay from PROCLK		18
T87	$\overline{INTA}$ rising edge delay from PROCLK		17
T88	ADR0 low delay from PROCLK; interrupt acknowledge cycle		21
T89	$\overline{DEN0}$ low delay from PROCLK; interrupt acknowledge cycle		26
T90	$\overline{DEN0}$ rise delay from PROCLK; interrupt acknowledge cycle		19
T91	CPURES rising edge delay from PROCLK; shutdown cycle		18

TABLE 7-1. TIMING PARAMETERS, Continued

SYMBOL	PARAMETER	16 MHz MIN	16 MHz MAX (NS)
T92	CPURES falling edge delay from PROCLK; shutdown cycle		17
T93	OUT1 setup time to EADR0/PCLK; asynchronous input	15	
T94	HOLDRQ rising edge delay from EADR0/PCLK		12
T95	HOLDRQ falling edge delay from EADR0/PCLK		14
T96	HLDA setup time to EADR0/PCLK; asynchronous input	26	
T97	$\overline{\text{REFRESH}}$ low delay from HLDA high		29
T98	$\overline{\text{REFRESH}}$ output tristate delay from EADR0/PCLK		9
T99	$\overline{\text{ERFSH}}$ falling edge delay from EADR0/PCLK		10
T100	$\overline{\text{ERFSH}}$ rising edge delay from EADR0/PCLK		10
T101	$\overline{\text{YMEMR}}$ falling edge delay from EADR0/PCLK; refresh cycle		10
T102	$\overline{\text{YMEMR}}$ rising edge delay from EADR0/PCLK; refresh cycle		10
T103	IOCHRDY setup time to EADR0/PCLK	19	
T104	HRQ1 setup to EADR0/PCLK; asynchronous input	18	
T105	HLDA1 rising edge delay from EADR0/PCLK		10
T106	HLDA1 high delay from HLDA high		20
T107	HLDA1 falling edge delay from EADR0/PCLK		11
T108	BALE high delay from HLDA high		18
T109	BALE low delay from HLDA low		19
T110	ACK high delay from HLDA high		16
T111	ACK high delay from $\overline{\text{MASTER}}$ high		16
T112	ACK low delay from HLDA low		16
T113	ACK low delay from $\overline{\text{MASTER}}$ low		16
T114	$\overline{\text{ONBRD}}$ setup before $\overline{\text{YIOR}}$ falls	9	
T115	$\overline{\text{ONBRD}}$ to $\overline{\text{ONBRDL}}$ delay; HLDA high		19
T116	HLDA high to ADR0 float delay		20
T117	HLDA low to ADR0 enable delay		20
T118	ADR0 input to $\overline{\text{ABHE}}$ output delay		19
T119	HLDA high to $\overline{\text{EBHE}}$ float delay		23
T120	HLDA low to $\overline{\text{EBHE}}$ enable delay		23
T121	AEN high to $\overline{\text{EBHE}}$ enable delay		23
T122	AEN low to $\overline{\text{EBHE}}$ float delay		22
T123	ADR0 input to $\overline{\text{EBHE}}$ output delay		28
T124	HLDA1 high to $\overline{\text{BHE}}$ enable delay		10
T125	HLDA1 low to $\overline{\text{BHE}}$ float delay		11

TABLE 7-1. TIMING PARAMETERS, Continued

SYMBOL	PARAMETER	16 MHz MIN	16 MHz MAX (NS)
T126	$\overline{EBHE}$ to $\overline{BHE}$ delay		11
T127	HLDA high to $\overline{YIOR}$ float delay		21
T128	HLDA low to $\overline{YIOR}$ enable delay		23
T129	HLDA high to $\overline{YMEMW}$ float delay		21
T130	HLDA low to $\overline{YMEMW}$ enable delay		23
T131	$\overline{YIOR}$ low to $\overline{DEN0}$ low delay		20
T132	$\overline{YIOR}$ high to $\overline{DEN0}$ high delay		19
T 133	$\overline{YIOR}$ low to DTR low delay		18
T134	$\overline{YIOR}$ high to DTR high delay		18
T135	$\overline{YIOR}$ low to SDTR high delay		26
T136	$\overline{YIOR}$ high to SDTR low delay		23
T137	$\overline{ONBRD}$ setup before DMACLK which causes $\overline{YMEMR}$ to go low	22	
T138	$\overline{DMAMR}$ setup time to DMACLK	16	
T139	$\overline{YMEMR}$ falling edge delay from DMACLK		10
T140	$\overline{DMAMR}$ high to $\overline{YMEMR}$ high delay		19
T141	$\overline{DLYWR}$ input low to $\overline{YIOW}$ output low		16
T142	$\overline{DLYWR}$ input high to $\overline{YIOW}$ output high		16
T143	$\overline{YMEMR}$ low to $\overline{DEN1}$ low delay		18
T144	$\overline{YMEMR}$ high to $\overline{DEN1}$ high delay		17
T145	$\overline{YMEMR}$ low to $\overline{SDEN}$ low delay		21
T146	$\overline{YMEMR}$ high to $\overline{SDEN}$ high delay		19
T147	AEN high to ADR0 enable delay; DACK2 high		25
T148	DACK2 low to ADR0 float delay		20
T149	AEN high to $\overline{ABHE}$ low delay; DACK2 high		27
T150	IOCHRDY setup time before DMACLK	14	
T151	$\overline{YIOR}$ low to DMARDY low delay		17
T152	$\overline{DMAMR}$ low to DMARDY low delay		18
T153	DMARDY rising edge delay from DMACLK		11
T154	$\overline{YMEMR}$ setup time before PROCLK	11	
T155	$\overline{ONBRDL}$ hold time from PROCLK	2	
T156	$\overline{EBHE}$ to $\overline{ABHE}$ delay; master mode		22
T157	AEN low to ADR0 float delay; master mode		23
T158	AEN high to $\overline{DLYWR}$ float delay		20
T159	AEN low to $\overline{DLYWR}$ enable delay		21

TABLE 7-1. TIMING PARAMETERS, Continued

SYMBOL	PARAMETER	16 MHz MIN	16 MHz MAX (NS)
T160	$\overline{\text{ONBRD}}$ setup time before memory command falls; master mode	18	
T161	ADR0 setup time before memory command falls; master mode	6	
T162	$\overline{\text{EBHE}}$ setup time before memory command falls; master mode	6	
T163	DTR low delay from memory command low; master mode		17
T164	DTR high delay from memory command high; master mode		17
T165	$\overline{\text{DEN0}}$ low delay from memory command low; master mode		20
T166	$\overline{\text{DEN0}}$ high delay from memory command high; master mode		19
T167	$\overline{\text{DEN1}}$ low delay from memory command low; master mode		19
T168	$\overline{\text{DEN1}}$ high delay from memory command high; master mode		18
T169	$\overline{\text{MEMCS16}}$ setup time before memory command falls; master mode, ADR0 high	9	
T170	SDTR low delay from memory command low; master mode, ADR0 high		21
T171	SDTR high delay from memory command high; master mode, ADR0 high		20
T172	$\overline{\text{SDEN}}$ low delay from memory command low; master mode, ADR0 high		21
T173	$\overline{\text{SDEN}}$ high delay from memory command high; master mode, ADR0 high		20
T174	ADR0 setup time before I/O command falls; master mode	5	
T175	SDTR low delay from I/O command low; master mode, ADR0 high		19
T176	SDTR high delay from I/O command high; master mode, ADR0 high		19
T177	$\overline{\text{SDEN}}$ low delay from I/O command low; master mode, ADR0 high		23
T178	$\overline{\text{SDEN}}$ high delay from I/O command high; master mode, ADR0 high		23
T179	$\overline{\text{IOCS16}}$ setup time before I/O command falls; master mode, ADR0 high	14	

TABLE 7-1. TIMING PARAMETERS, Continued

NOTES:

All delays with respect to PROCLK are with respect to the falling edge of PROCLK.

T22:$\overline{\text{ZEROWS}}$ SETUP TIME NOTES

The $\overline{\text{ZEROWS}}$ signal is sampled by the FE3001 in the middle of every CPU wait state during AT bus cycles. $\overline{\text{ZEROWS}}$ will terminate an AT bus cycle early when it is sampled after the minimum number of wait states programmed into R8 have occurred.

T25: $\overline{\text{MEMCS16}}$ SETUP TIME NOTES

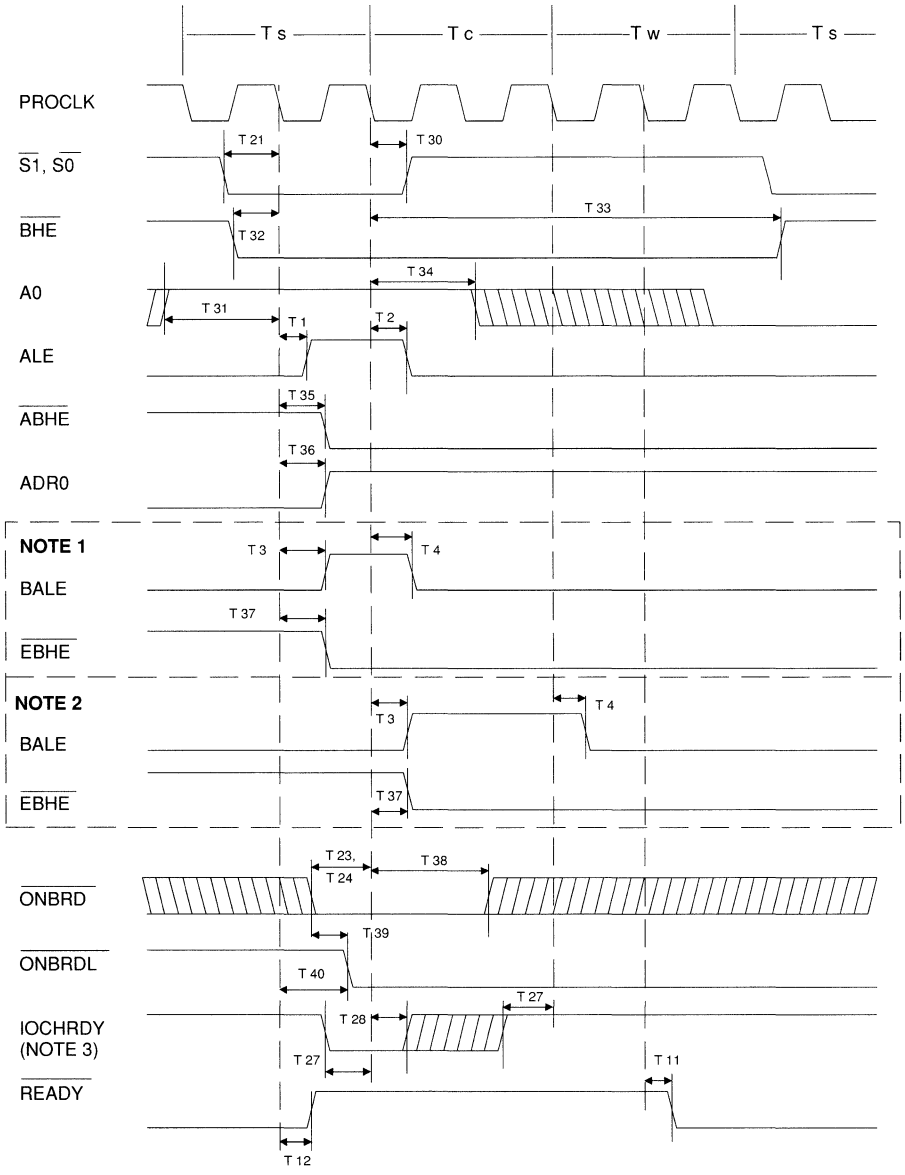
$\overline{\text{MEMCS16}}$ is only examined during AT bus memory cycles. It must be valid before the earlier of either (1) the memory command strobe falls as programmed by R6, or (2) BALE falls as programmed by R0 and R1.

T26: $\overline{\text{IOCS16}}$ SETUP TIME NOTES

$\overline{\text{IOCS16}}$ is only examined during AT bus I/O cycles. It must be valid before the I/O command falls as programmed by R3.

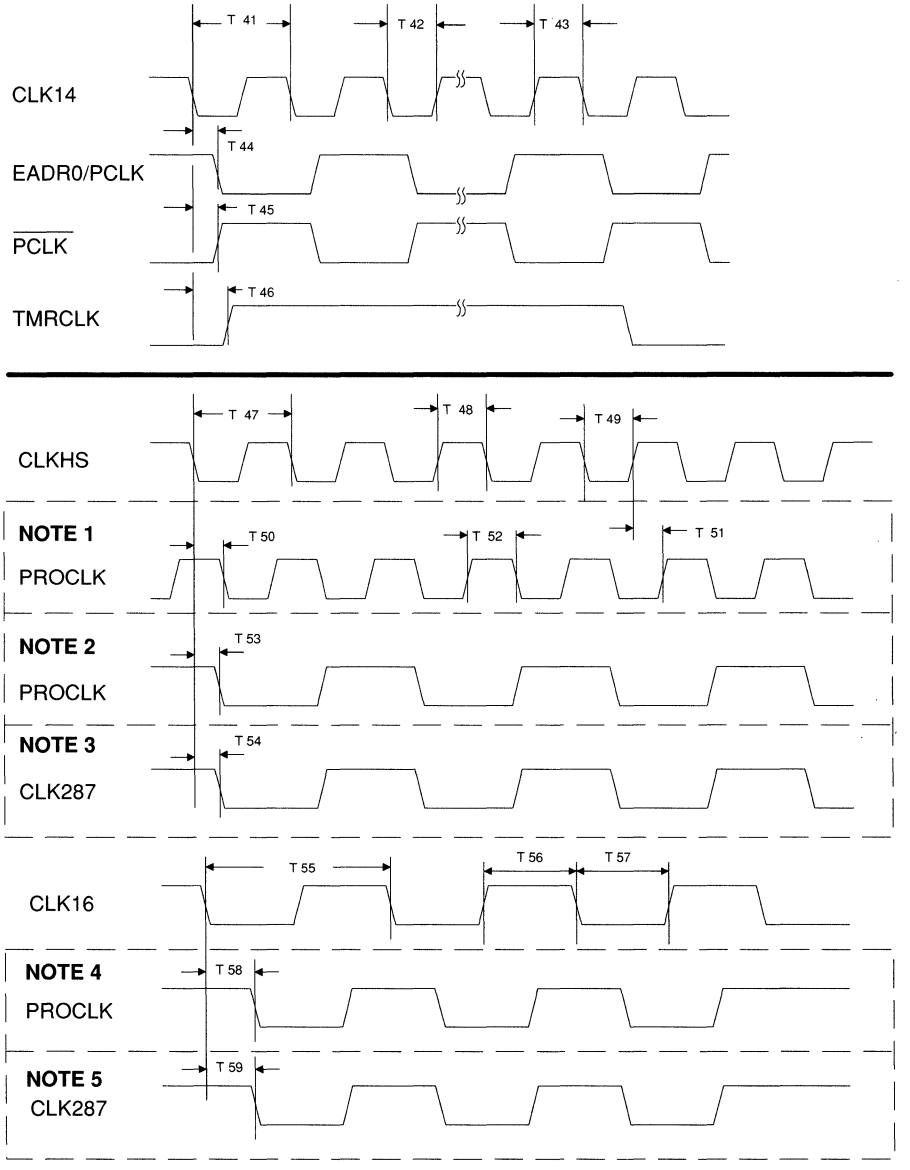
T27: IOCHRDY SETUP TIME NOTES

IOCHRDY is sampled with the falling edge of PROCLK at the end of each CPU "t" state. It must be sampled low one full "t" state before a cycle would normally end in order to extend it.



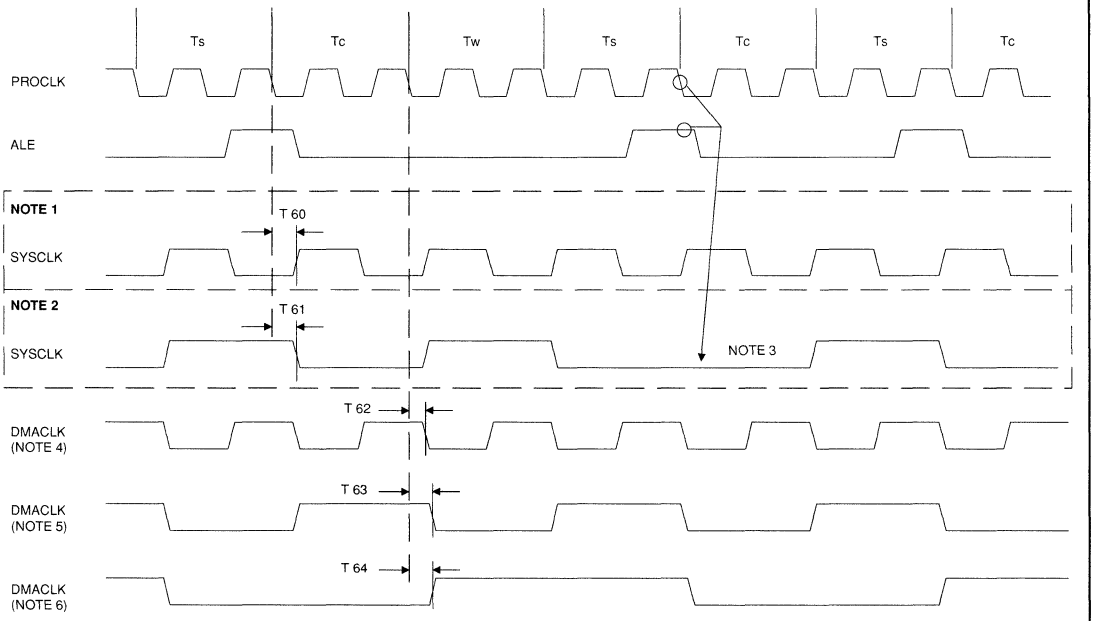
NOTES:
(1) R0 = 0; R1 = 1 (low speed BALE timing)
(2) R0 = 1; R1 = 2 (16MHz BALE timing)
(3) IOCHRDY is being used to add one wait state to this on-board cycle, which is otherwise programmed by R9 or R10 to be 0 wait states

FIGURE 7-1. CPU CYCLE TIMING FOR ALE, BYTE SELECT, ONBRD and READY



NOTES:
(1) Bit 2 of I/O Addr 63 set to 1 (High speed CPU clock)
(2) Bit 2 of I/O Addr 63 set to 0 (low speed CPU clock) and CLK16 input connected to +5V
(3) CLK16 input connected to +5V
(4) Bit 2 of I/O Addr 63 set to 0 (low speed CPU clock) and CLK16 input driven by an oscillator
(5) CLK16 input driven by an oscillator

FIGURE 7-2. CLOCK TIMING (1 of 2)



NOTES:

(1) Bit 2 of I/O Addr 63 set to 0 (low speed CPU clock)

(2) Bit 2 of I/O Addr 63 set to 1 (high speed CPU clock)

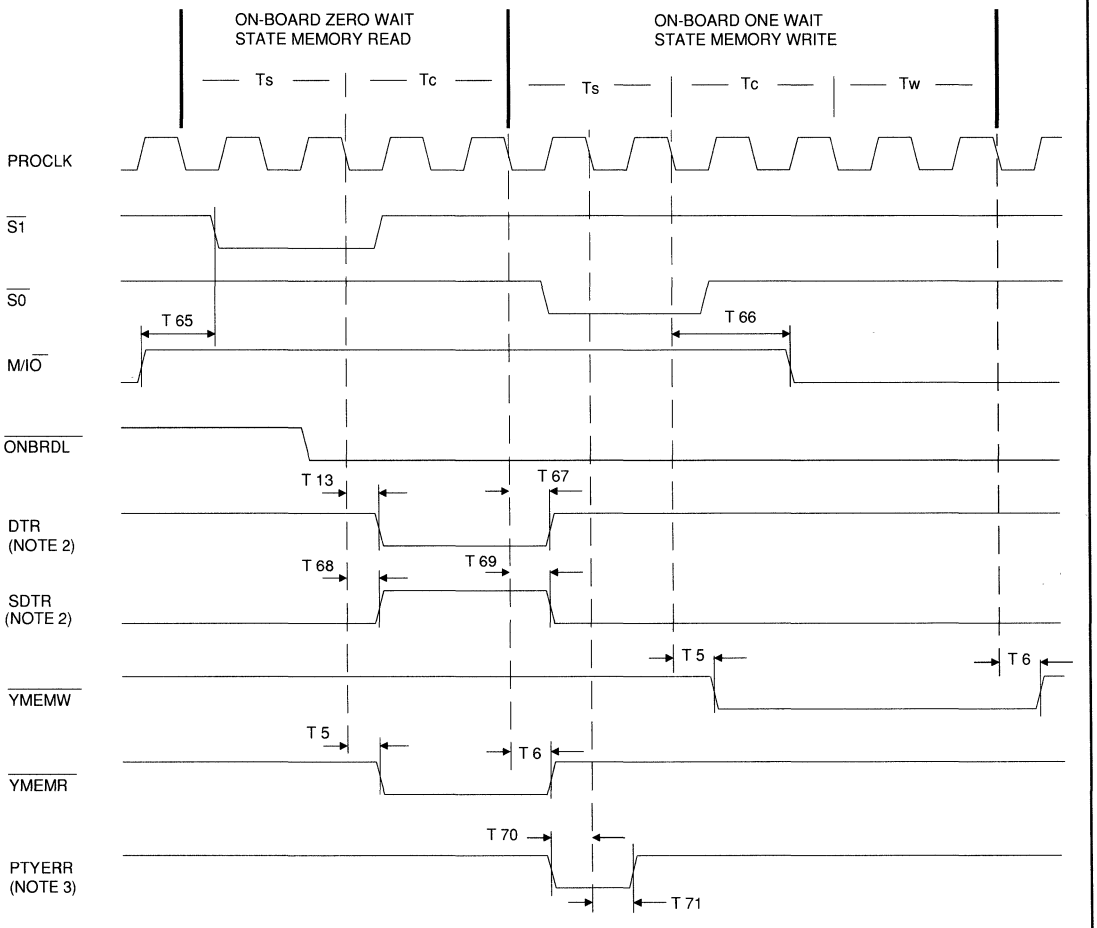
(3) SYSCLK low time extended when SYSCLK is low while ALE is high and the high speed CPU clock has been selected

(4) Bit 2 of I/O Addr 63 set to 0 (low speed CPU clock) and Bit 3 set to 1 (high speed DMA)

(5) I/O Addr 63 Bits 2 and 3 set to the same value; low speed CPU clock and low speed DMA, or high speed CPU clock and high speed DMA

(6) Bit 2 of I/O Addr 63 set to 1 (high speed CPU clock) and Bit 3 set to 0 (low speed DMA)

FIGURE 7-3. CLOCK TIMING (2 of 2)



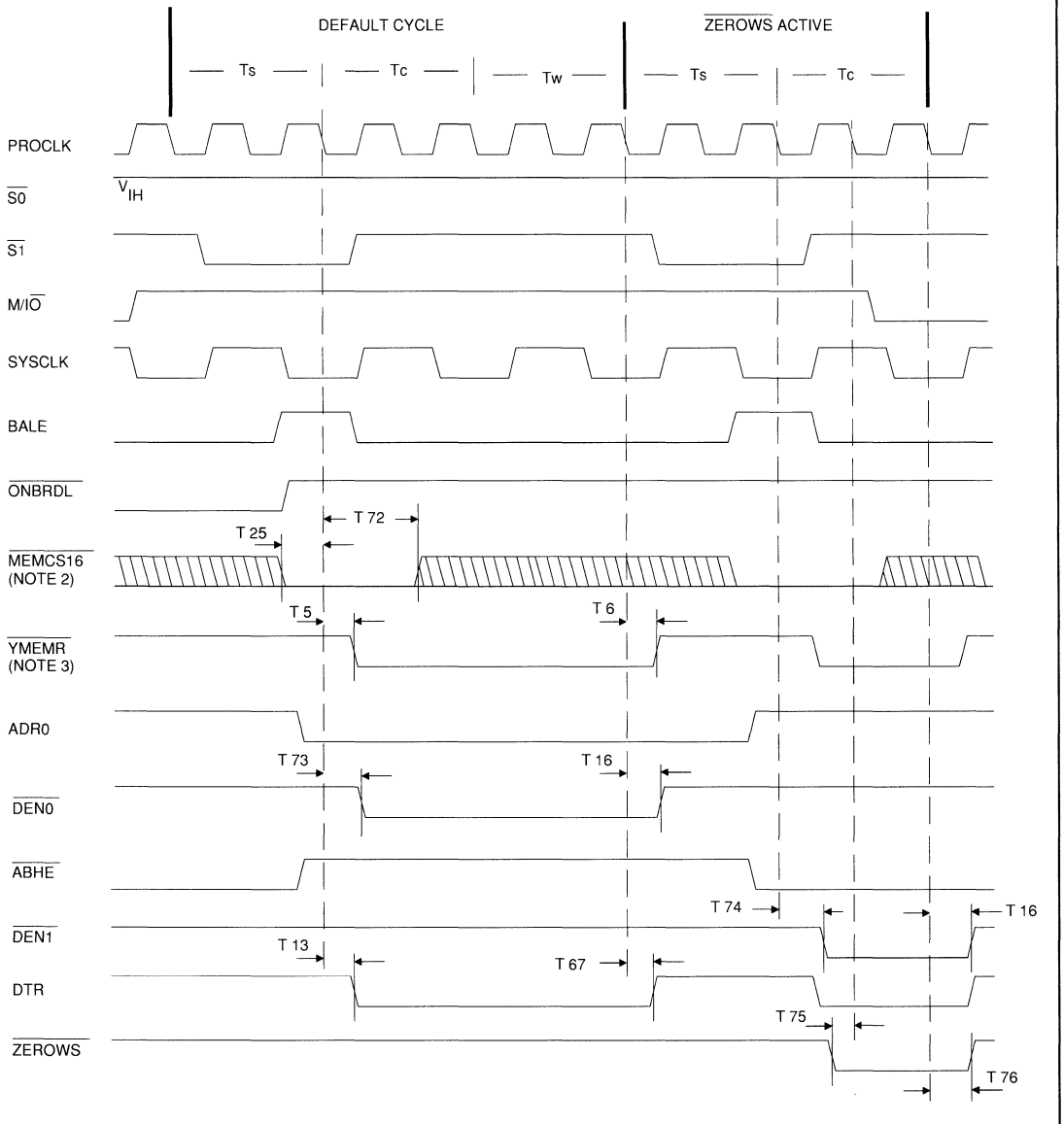
NOTES:

(1) $\overline{DEN0}$, $\overline{DEN1}$, and $\overline{SDEN}$ will remain high and SYSCLE will remain low during on-board memory cycles

(2) NOT USED by the FE3031 during on-board memory cycles; shown for reference only

(3) PTYERR must be low when shown to prevent a parity NMI from being generated (if enabled). PTYERR is sampled one PROCLK ***after*** the end of an on-board memory read

FIGURE 7-4. ON-BOARD MEMORY CYCLE TIMING



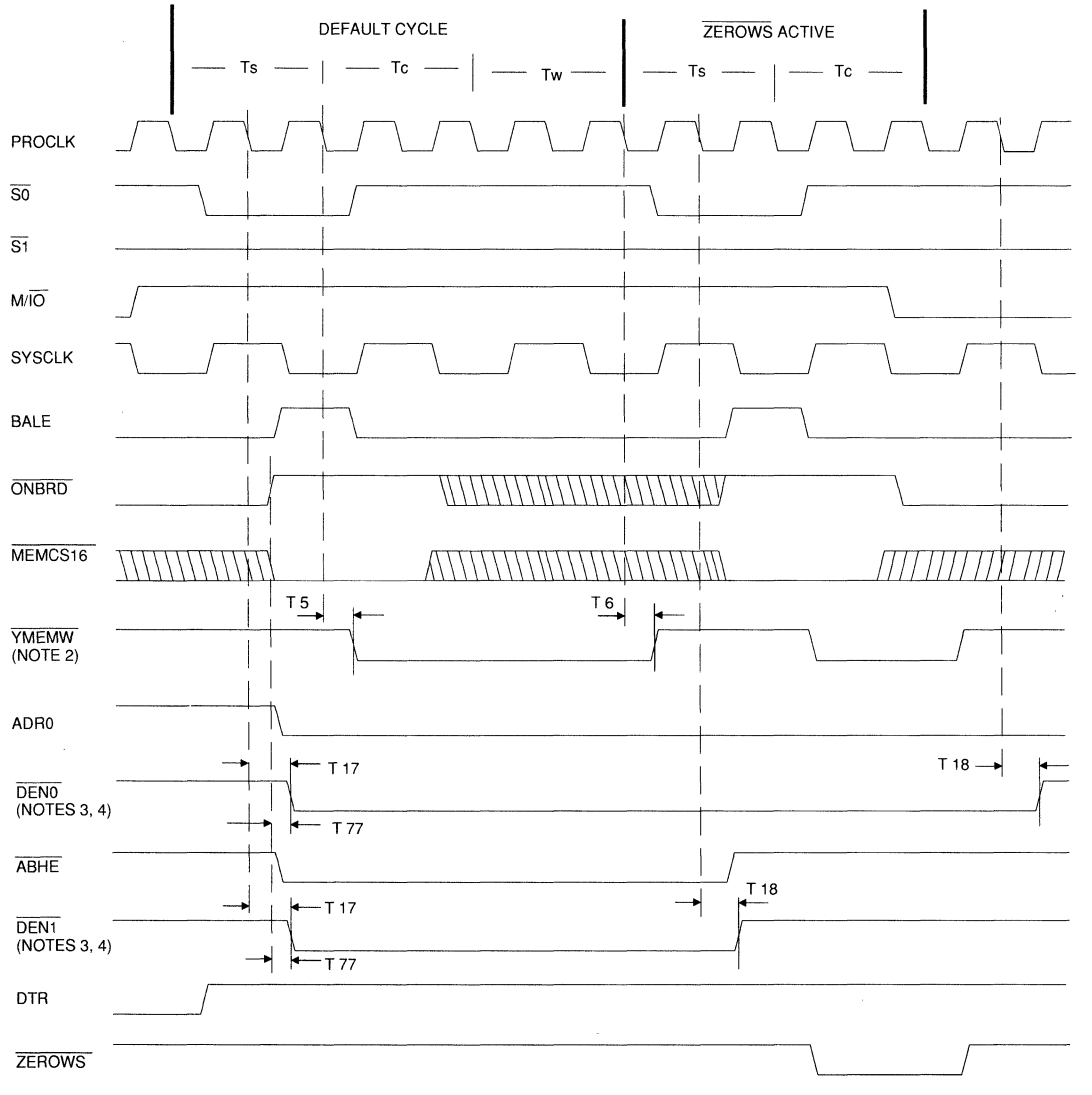
NOTES:

(1) NPCS is high during these cycles

(2) Setup/Hold times referenced to PROCLK edge which is programmed by R6 to cause YMEMR or YMEMW to go low

(3) R6 = 0; R7 = 1; R8 = 0; R0 = 0; R1 = 1

FIGURE 7-5. 16-BIT MEMORY READ TIMING FOR LOW SPEED CPU CLOCK



NOTES:

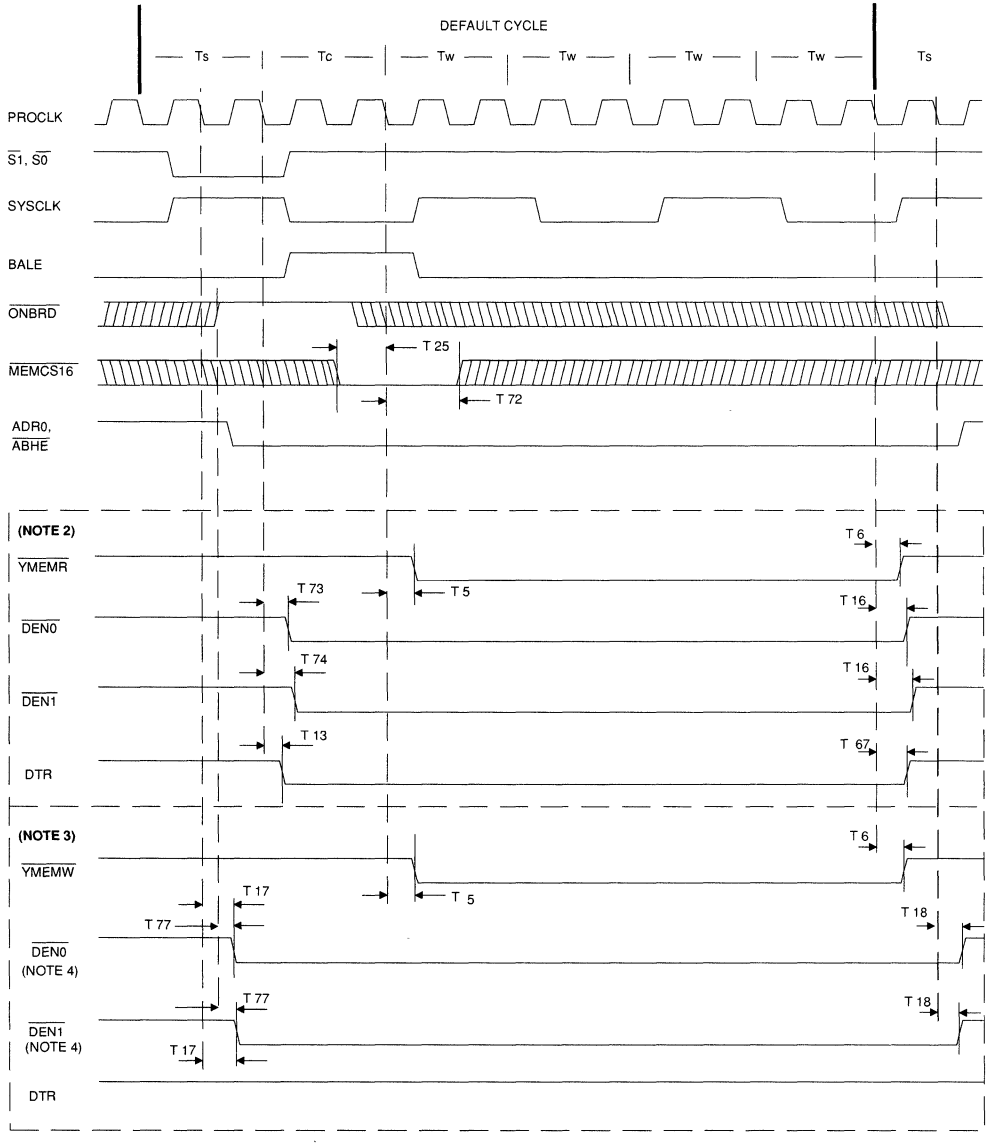
(1) NPCS is high during these cycles

(2) R6 = 0; R7 = 1; R8 = 0; R0 = 0; R1 = 1

(3) DEN0 and DEN1 go high one PROCLK cycle after the write command goes high. However, each will remain low for back to back write cycles when it is active in both cycles.

(4) The falling edge of DEN0 or DEN1 in a write cycle will be controlled by ONBRD if it goes high in the last half of the processor Ts state, or by PROCLK if ONBRD is high earlier.

FIGURE 7-6. 16-BIT MEMORY WRITE TIMING FOR LOW SPEED CPU CLOCK



NOTES:

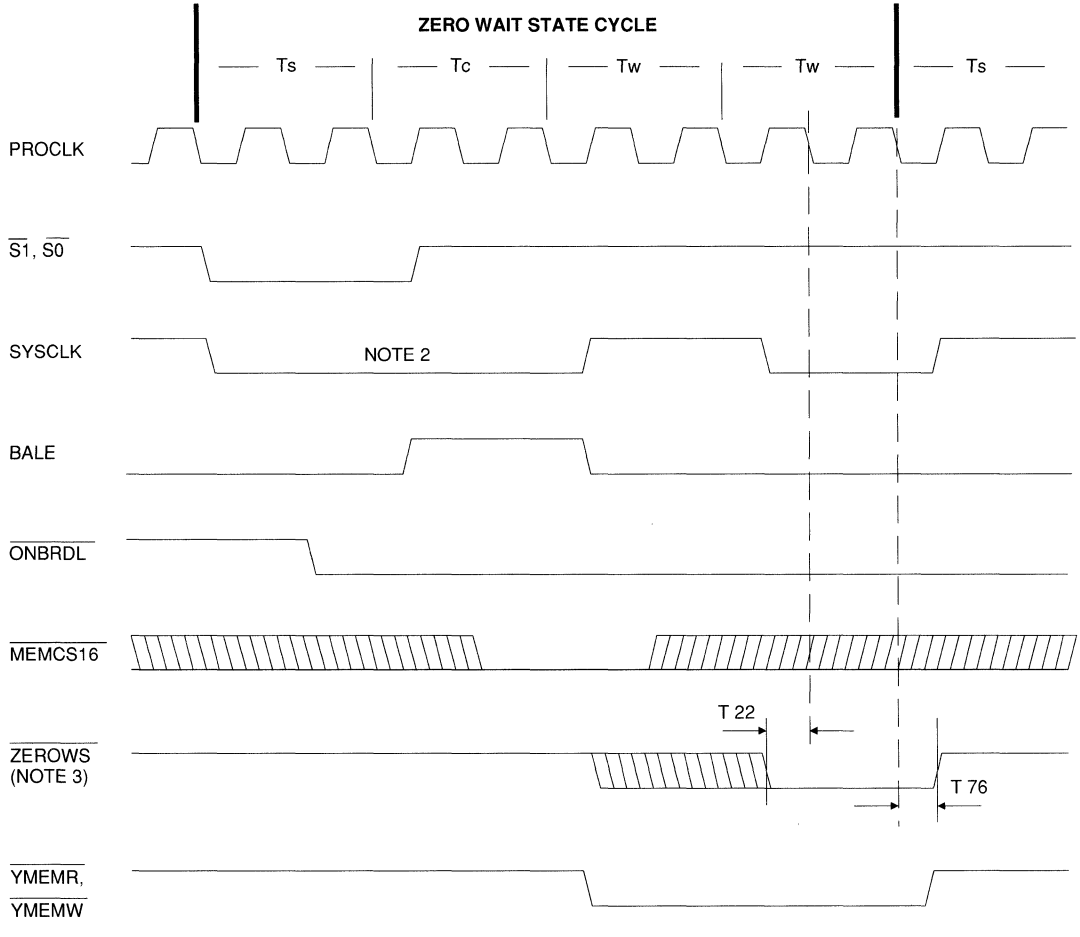
(1) R0 = 1; R1 = 2; R6 = 2; R7 = 4; $\overline{\text{NPCS}}$ is high during these cycles

(2) Memory read cycle timing

(3) Memory write cycle timing

(4) The falling edge of $\overline{\text{DEN0}}$ or $\overline{\text{DEN1}}$ in a write cycle will be controlled by $\overline{\text{ONBRD}}$ if it goes high in the last half of the processor Ts state, or by PROCLK if $\overline{\text{ONBRD}}$ goes high earlier

FIGURE 7-7. 16-BIT MEMORY TIMING FOR HIGH SPEED (16 MHZ) CPU



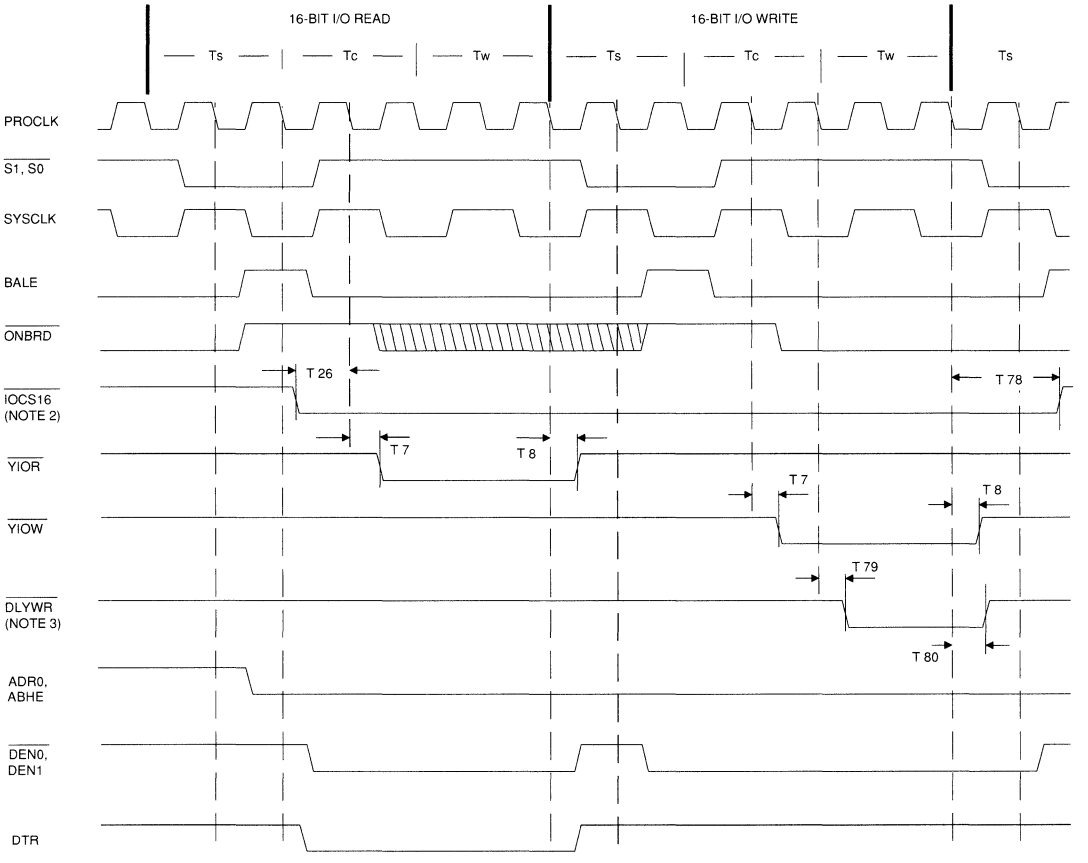
NOTES:

(1) R0 = 1; R1 = 2; R6 = 2; NPCS is high during these cycles

(2) SYSCLK is extended low one extra half period when it is low during the processor's Ts state and the high speed CPU clock is selected

(3) Register R8 = 2. When the high speed CPU clock is selected, no AT bus cycle can terminate until the cycle when SYSCLK goes high. This ensures proper synchronization of the rising edge of the command strobes with SYSCLK

FIGURE 7-8. 16-BIT MEMORY TIMING WITH ZEROWS ASSERTED AND HIGH SPEED (16 MHz) CPU



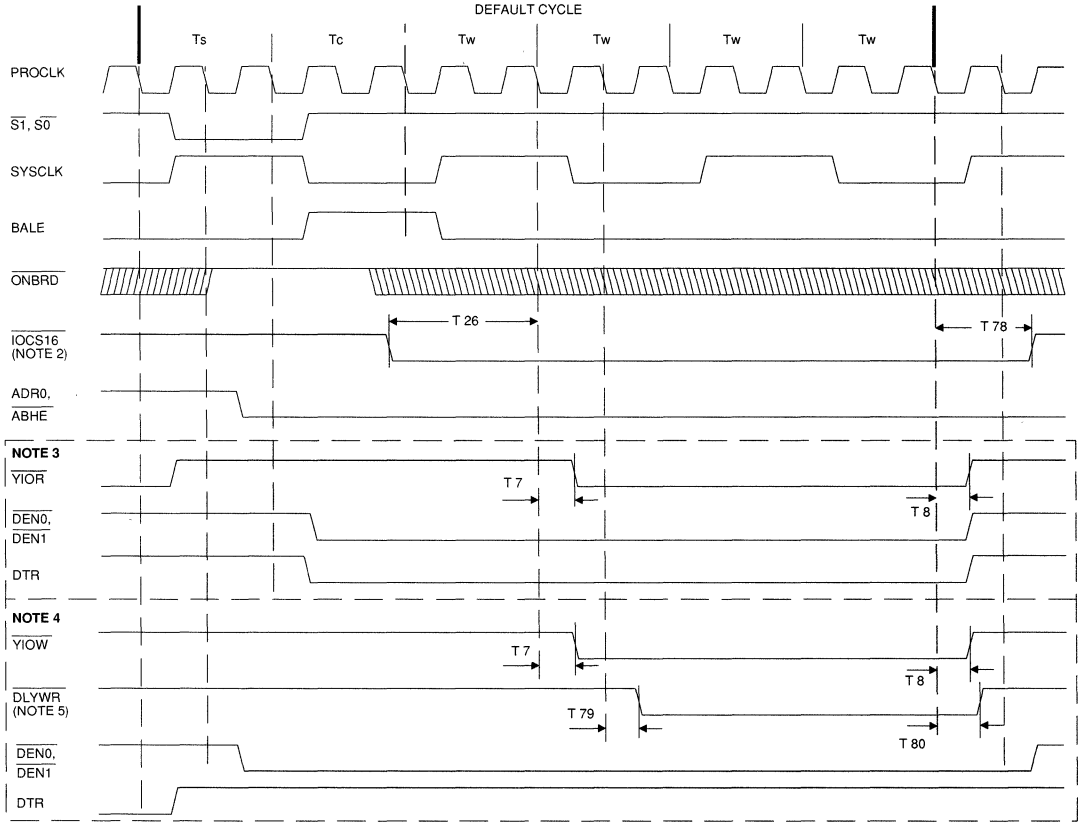
NOTES:

(1) R0 = 0; R1 = 1; R3 = 1; R5 = 1

(2) $\overline{\text{IOCS16}}$ setup time is to the PROCLK which causes $\overline{\text{YIOR}}$ or $\overline{\text{YIOW}}$ to go low as pro-. grammed by R3. Hold time is from the end of the cycle

(3) $\overline{\text{DLYWR}}$ falling edge is one PROCLK later than $\overline{\text{YIOW}}$. $\overline{\text{DLYWR}}$ rising edge is coincident with $\overline{\text{YIOW}}$ rising edge

FIGURE 7-9. 16-BIT I/O TIMING WITH LOW SPEED CPU CLOCK



NOTES:

(1) R0 = 1; R1 = 2; R3 = 4; R5 = 4. NPCS is high during these cycles

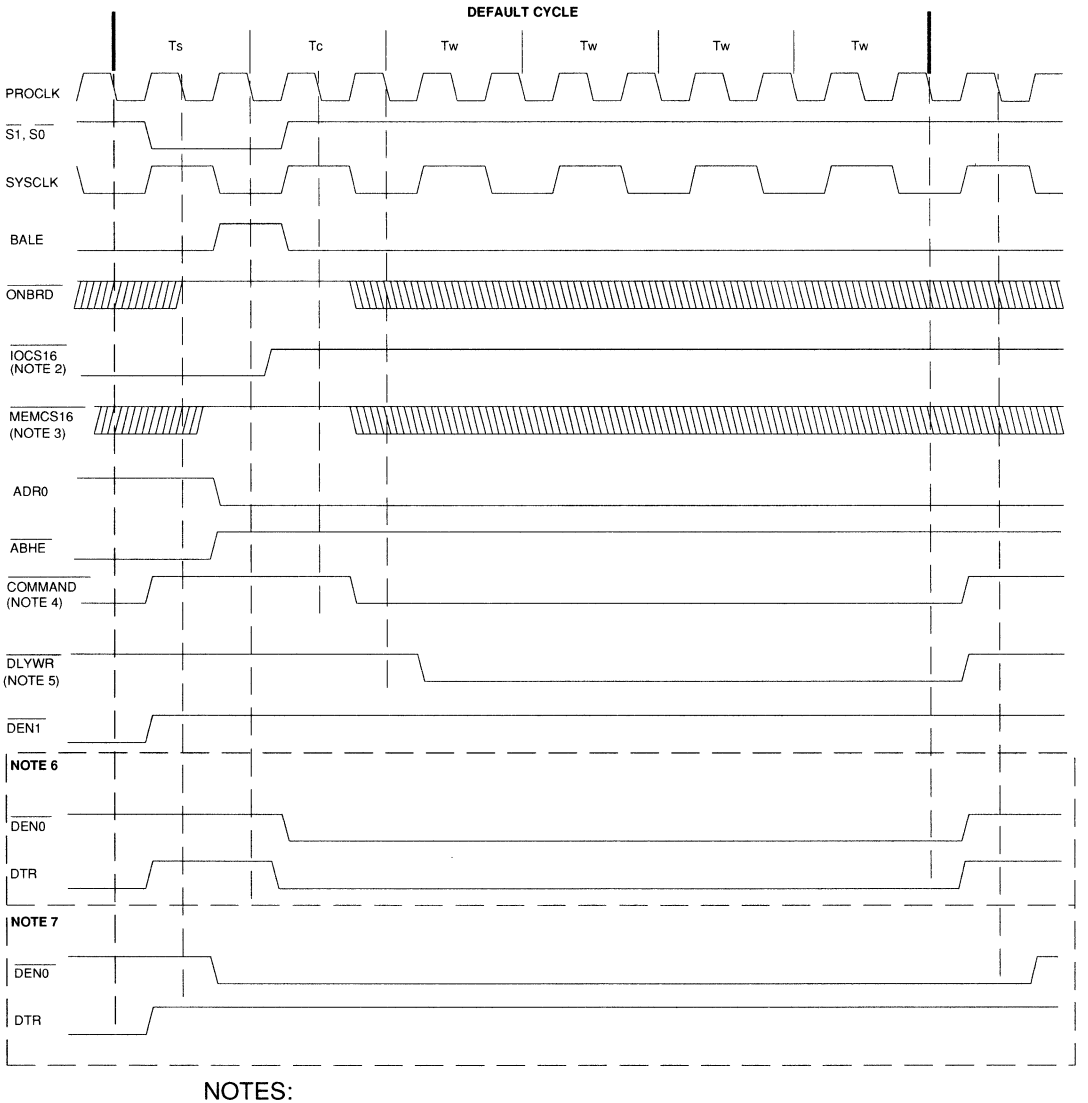
(2) IOCS16 setup time is referenced to the PROCLK which causes IOR or IOW to go low as programmed by R3. Hold time is from the cycle end

(3) I/O read cycle timing

(4) I/O write cycle timing

(5) DLYWR falling edge is one PROCLK later than IOW. DLYWR rising edge is coincident with IOW rising edge

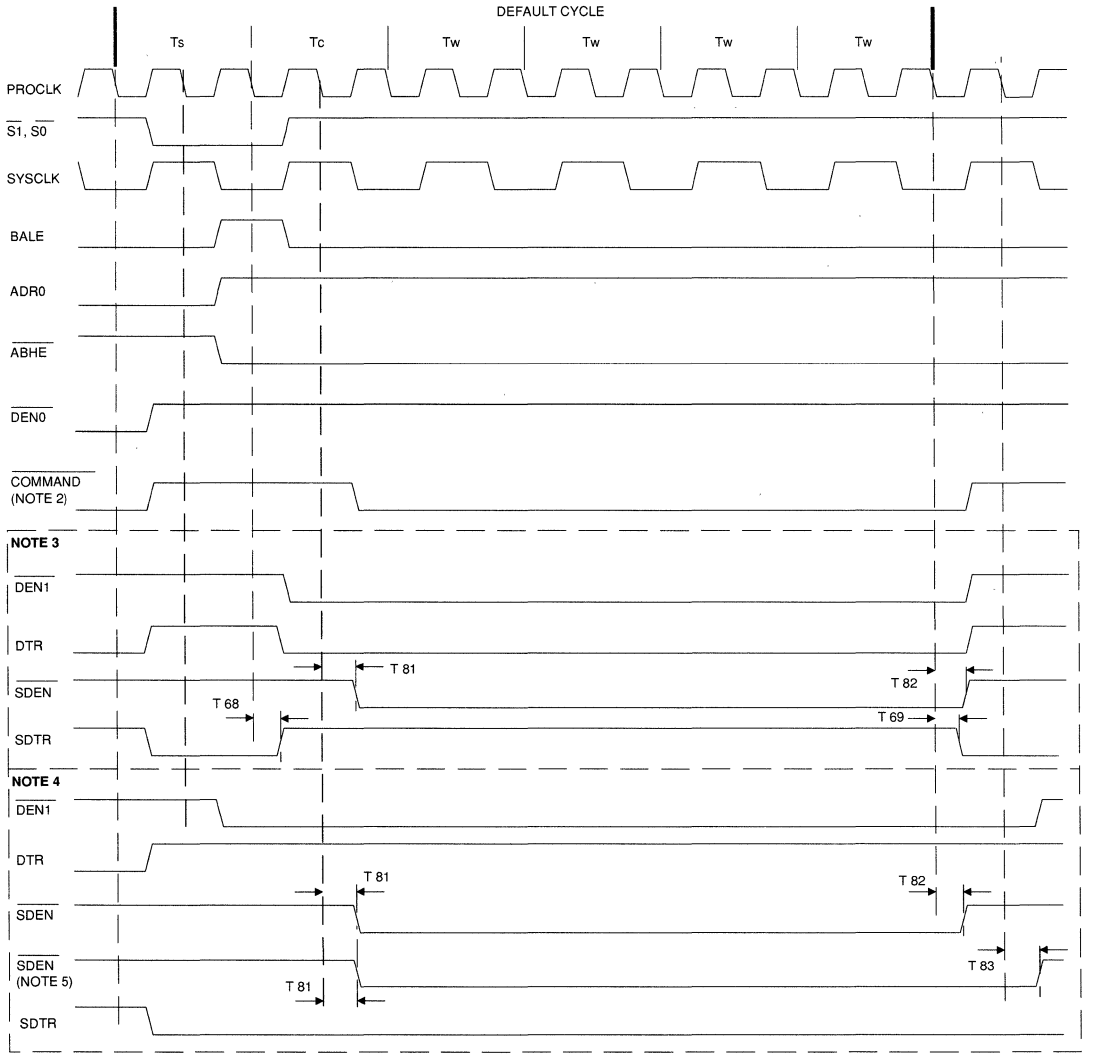
FIGURE 7-10. 16-BIT I/O TIMING WITH HIGH SPEED (16 MHZ) CPU CLOCK



NOTES:

(1) R0 = 0; R1 = 1; R3 = 1; R4 = 4. NPCS is high during this cycle
(2) IOCS16 affects only I/O cycles
(3) MEMCS16 affects only memory cycles
(4) COMMAND means either YIOR, YIOW, YMEMR, or YMEMW
(5) DLYWR is active only in cycles where YIOW is active
(6) Read cycle timing
(7) Write cycle timing

FIGURE 7-11. 8-BIT CYCLE TIMING FOR LOW SPEED CPU CLOCK -- EVEN BYTE ACCESS



NOTES:

(1) R0 = 0; R1 = 1; R3 = 1; R4 = 4. $\overline{\text{NPCS}}$ and $\overline{\text{ONBRD}}$ are inactive. $\overline{\text{IOCS16}}$ is inactive during I/O cycles. $\overline{\text{MEMCS16}}$ is inactive during memory cycles

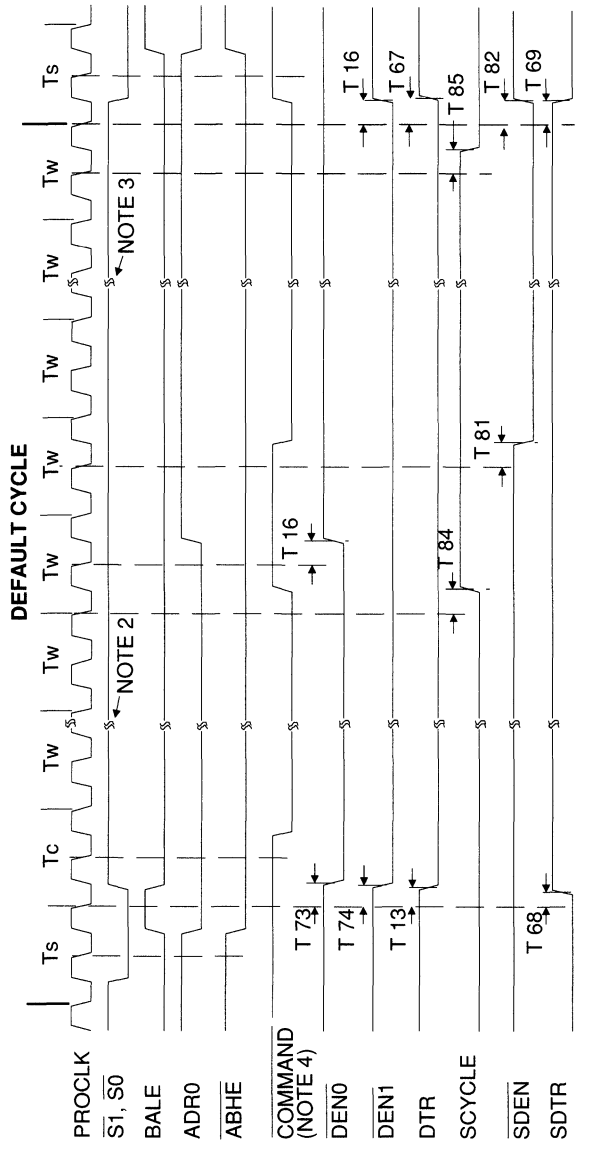
(2) $\overline{\text{COMMAND}}$ means either $\overline{\text{YIOR}}$, $\overline{\text{YIOW}}$, $\overline{\text{YMEMR}}$, or $\overline{\text{YMEMW}}$

(3) Read cycle timing

(4) Write cycle timing

(5) $\overline{\text{SDEN}}$ stays low one additional PROCLK during cycles when $\overline{\text{YIOW}}$ is active

FIGURE 7-12. 8-BIT CYCLE TIMING FOR LOW SPEED CPU CLOCK -- ODD BYTE ACCESS



NOTES:

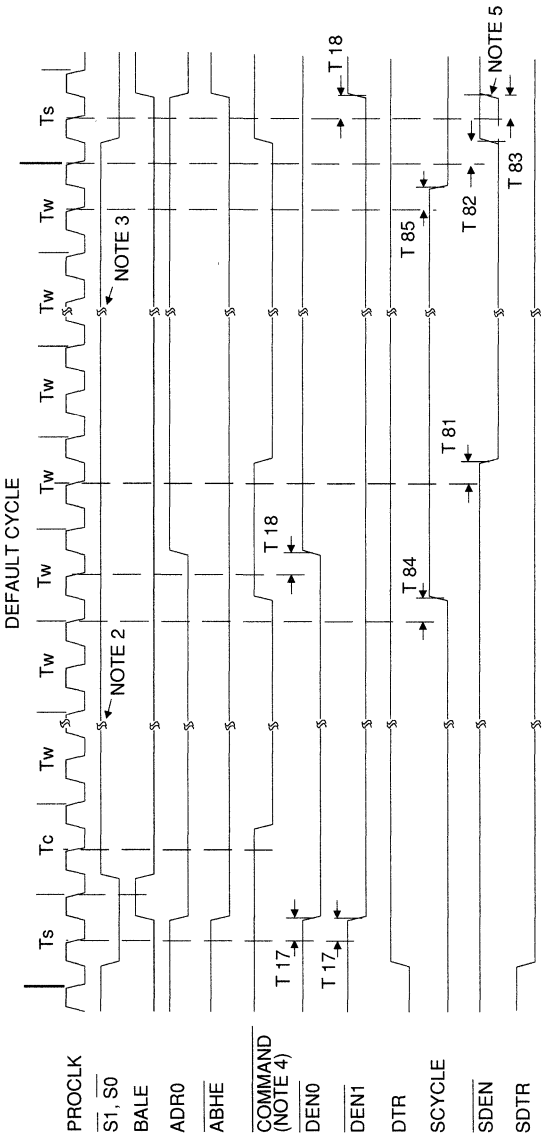
(1) R0 = 0; R1 = 1; R3 = 1; R4 = 4. NPCS and ONBRD are inactive. IOCS16 is inactive during I/O cycles. MEMCS16 is inactive during memory cycles

(2) Two additional wait states are not shown

(3) One additional wait state is not shown

(4) COMMAND means either YIOR or YMEMR

FIGURE 7-13. 8-BIT CYCLE TIMING FOR LOW SPEED CPU CLOCK -- WORD READ FROM EVEN ADDESS



NOTES:

(1) R0 = 0; R1 = 1; R3 = 1; R4 = 4. NPCS and ONBRD are inactive. IOCS16 is inactive during I/O cycles. MEMCS16 is inactive during memory cycles

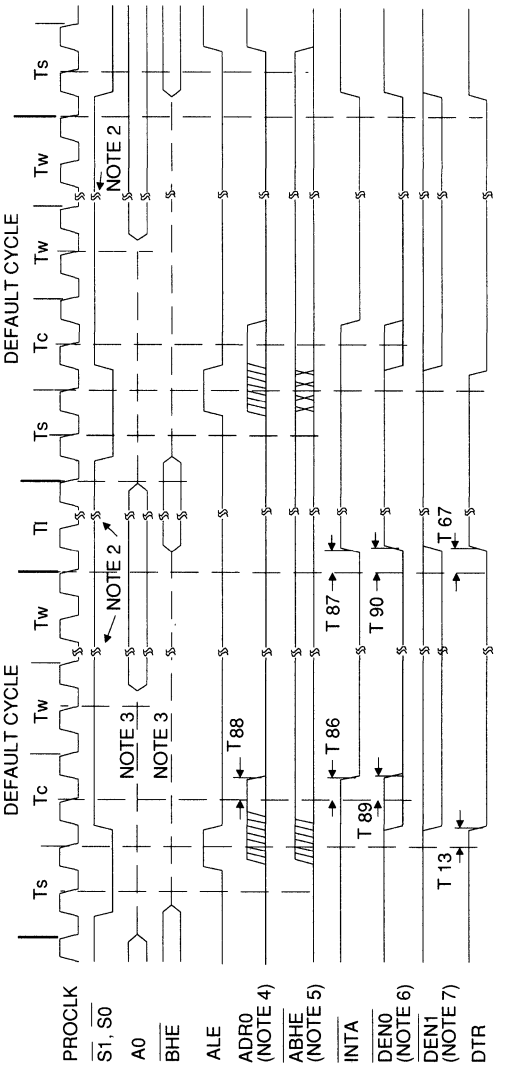
(2) Two additional wait states are not shown

(3) One additional wait state is not shown

(4) COMMAND means either YIOW or YMEMW

(5) SDEN low time extended one PROCLK for I/O write cycles

FIGURE 7-14. 8-BIT CYCLE TIMING FOR LOW SPEED CPU CLOCK -- WORD WRITE TO EVEN ACCESS



NOTES:

(1) R3 = 1; R4 = 4

(2) Two additional processor T states not shown

(3) 80286 floats these lines during interrupt acknowledge cycles

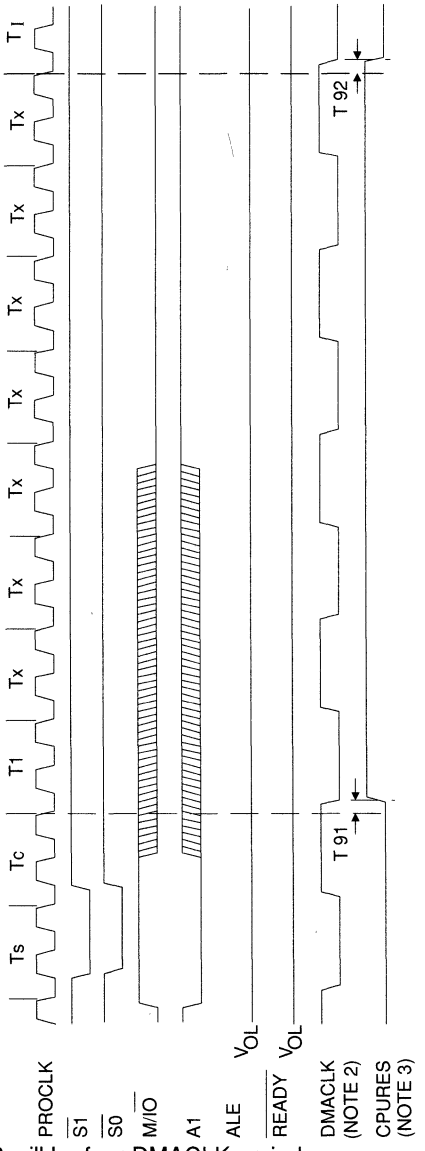
(4) Because A0 is floating, the state of ADR0 is unknown from the rising edge of ALE until INTA falls, when ADR0 is forced low

(5) Because BHE is floating, the state of ABHE (and EBHE) is unknown

(6) DEN0 is forced low when INTA falls. It could have gone low at the end of Ts depending on the state of ADR0

(7) The state of DEN1 follows ABHE and therefore cannot be determined

FIGURE 7-15. INTERRUPT ACKNOWLEDGE CYCLE FOR LOW SPEED CPU CLOCK



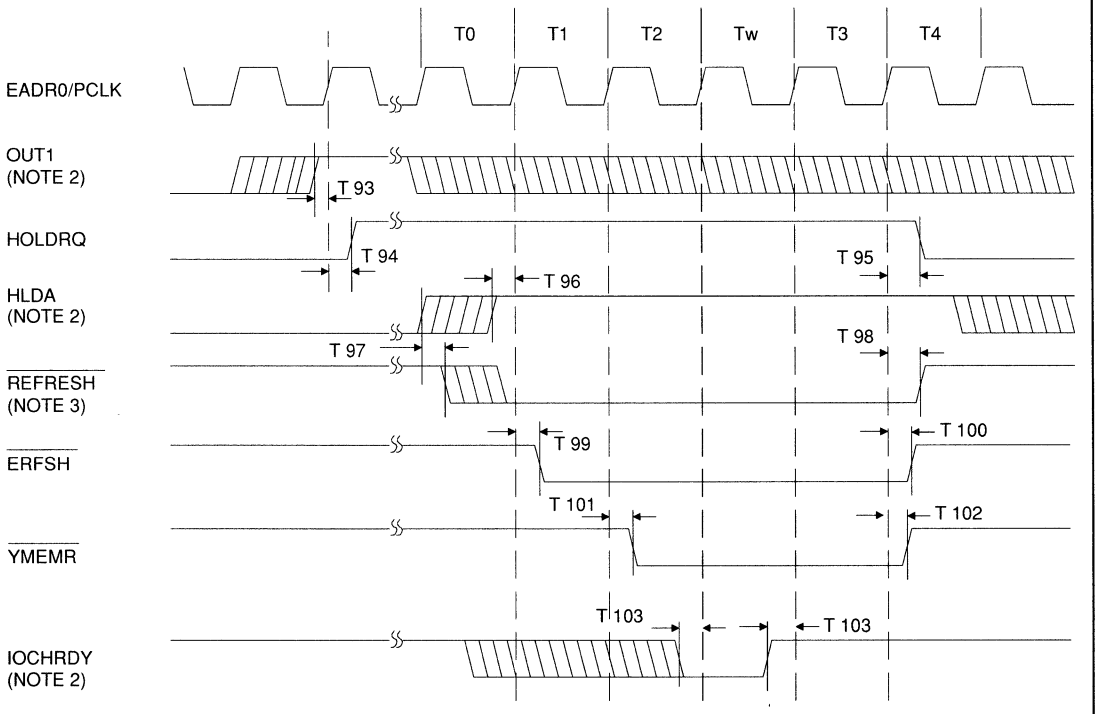
NOTES:

(1) The width of CPURES will be four DMACLK periods

(2) DMACLK is shown as it would be for high speed DMA and a high speed CPU clock or for low speed DMA and a low speed CPU clock. Refer to Figure 8. Note that the phase of DMACLK with respect to Ts is uncertain.

(3) CPURES will be asserted on the first PROCLK edge which begins a T state, after an internal divide by 4 of DMACLK makes a low to high transition. The phase of this internal signal is impossible to determine, although it changes on the rising edge of DMACLK. CPURES is shown going active here as early as possible. It could be delayed up to three more DMACLK periods

FIGURE 7-16. SHUTDOWN CYCLE TIMING



NOTES:

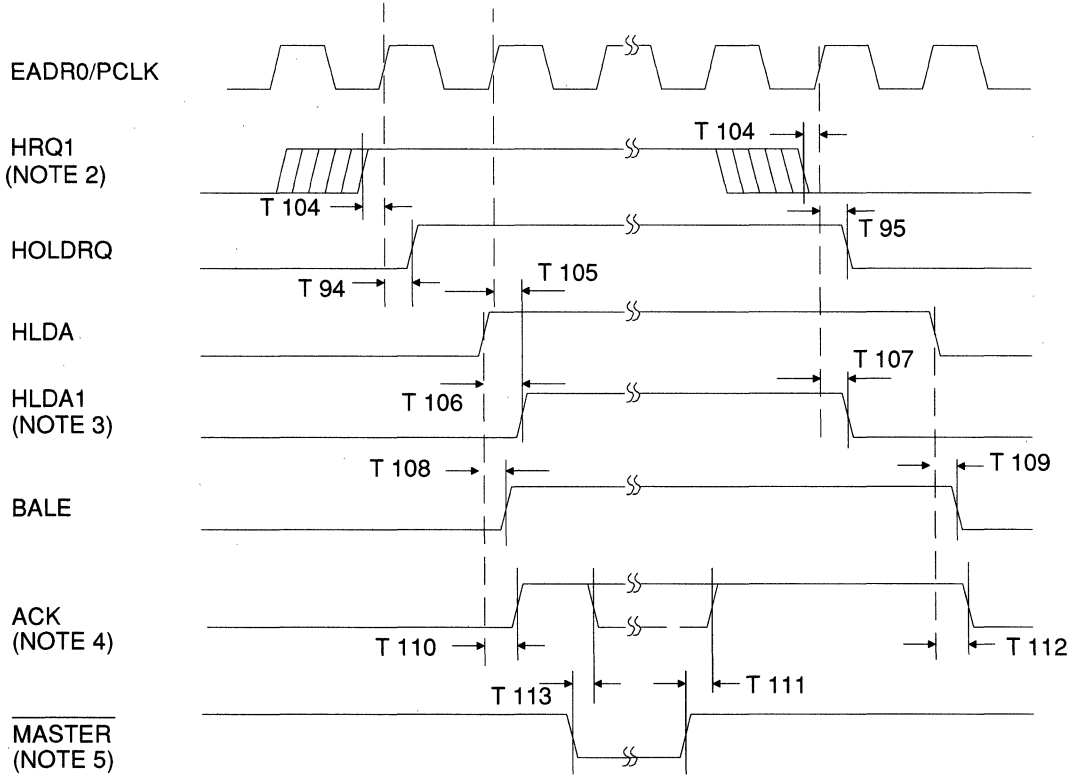
(1) Cycle shown with one wait state (one EADR0/PCLK period) inserted

(2) OUT1, HLDA , and IOCHRDY are asynchronous inputs. Setup times are shown only to guarantee recognition at a particular edge of EADR0/PCLK

(3) The falling edge of REFRESH is combinatorially generated from HLDA. The rising edge is controlled by the FE3001

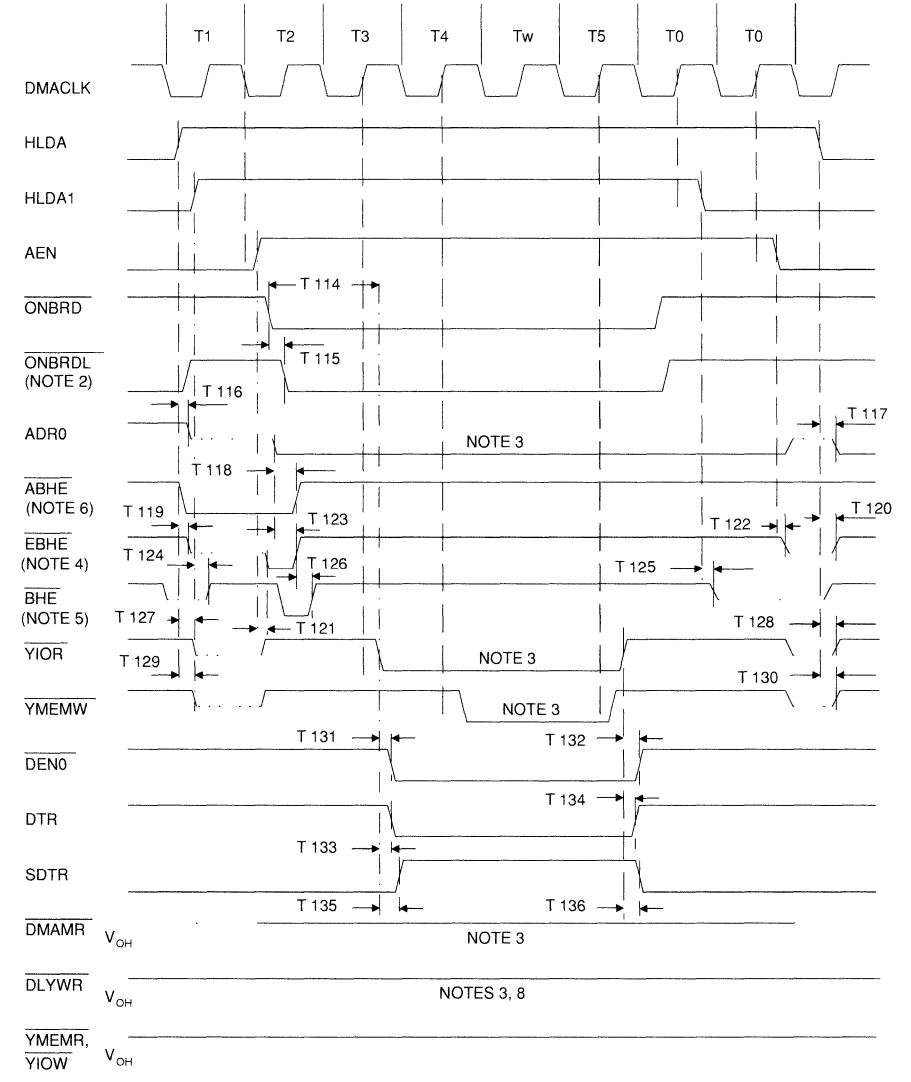
(4) HRQ1 and HLDA1 are not active

FIGURE 7-17. REFRESH CYCLE TIMING



NOTES:
(1) No refresh cycle is pending
(2) HRQ1 is an asynchronous input. Setup time is shown only to guarantee recognition at a particular EADR0/PCLK edge
(3) HLDA1 rising edge will be controlled by the later of the EADR0/PCLK edge shown or HLDA
(4) ACK will follow the dashed lines shown only when $\overline{\text{MASTER}}$ is asserted
(5) Applicable for Bus Master cycles only

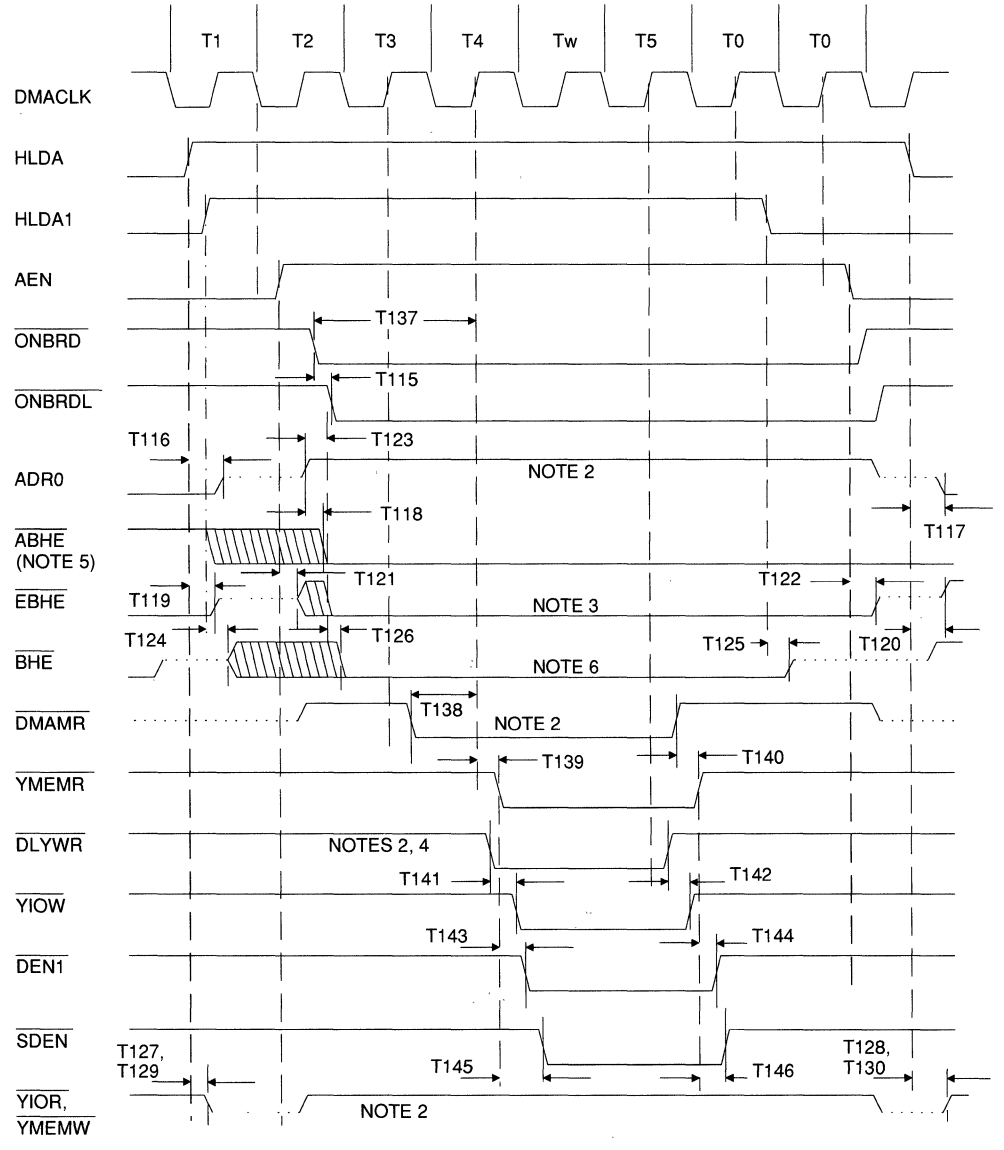
FIGURE 7-18. BASIC HOLD/HDLA TIMING FOR DMA AND MASTER MODE TRANSFERS



NOTES:

(1) No refresh cycles are pending
(2) ONBRDL follow ONBRD when HLDA is high
(3) The FE3010 drives these signals when AEN is high
(4) The FE3001 tri-states EBHE when HLDA goes high, but drives it again when AEN is high. It is the inversion of ADR0
(5) BHE is driven by the FE3001 when HLDA1 is high. It follows EBHE
(6) ABHE is the inversion of ADR0 while HLDA is high (8-Bit DMA)
(7) DEN1 and SDEN remain high during 8-Bit, even byte transfers
(8) The FE3001 tri-states DLYWR when AEN is high

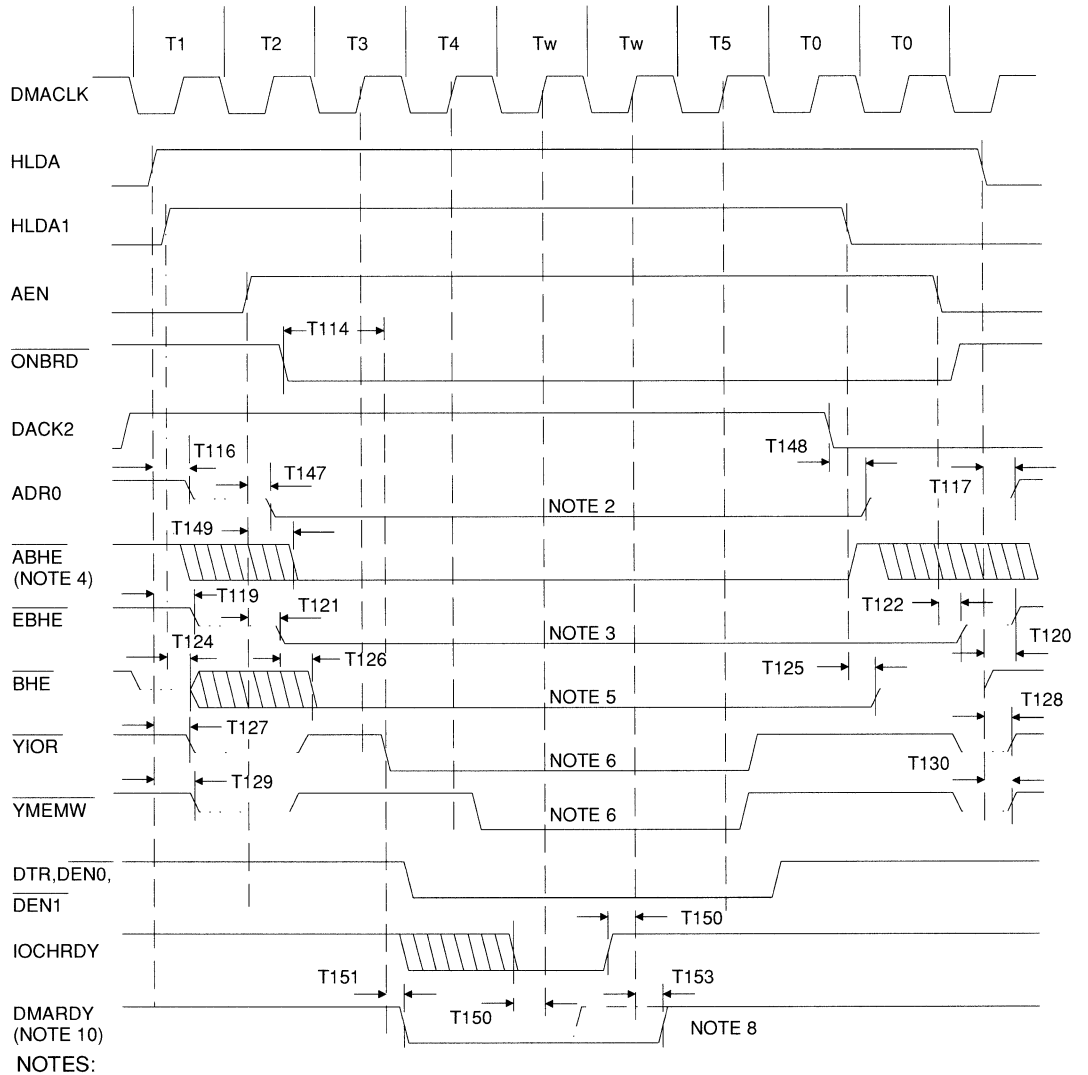
FIGURE 7-19. DMA TRANSFER TIMING: 8-BIT, I/O TO ON-BOARD MEMORY, EVEN BYTE, WITH NO ADDED WAIT STATES



NOTES:

(1) No refresh cycles are pending
(2) The FE3010 drives these signals when AEN is high
(3) The FE3001 tri-states $\overline{EBHE}$ when HLDA goes high, but drives it again when AEN is high
(4) The FE3001 tri-states $\overline{DLYWR}$ when AEN is high
(5) $\overline{ABHE}$ is the inversion of ADR0 when HLDA is high
(6) $\overline{BHE}$ is driven by the FE3001 when HLDA1 is high. It follows $\overline{EBHE}$
(7) $\overline{DEN0}$ and DTR remain high and SDTR remains low during this cycle

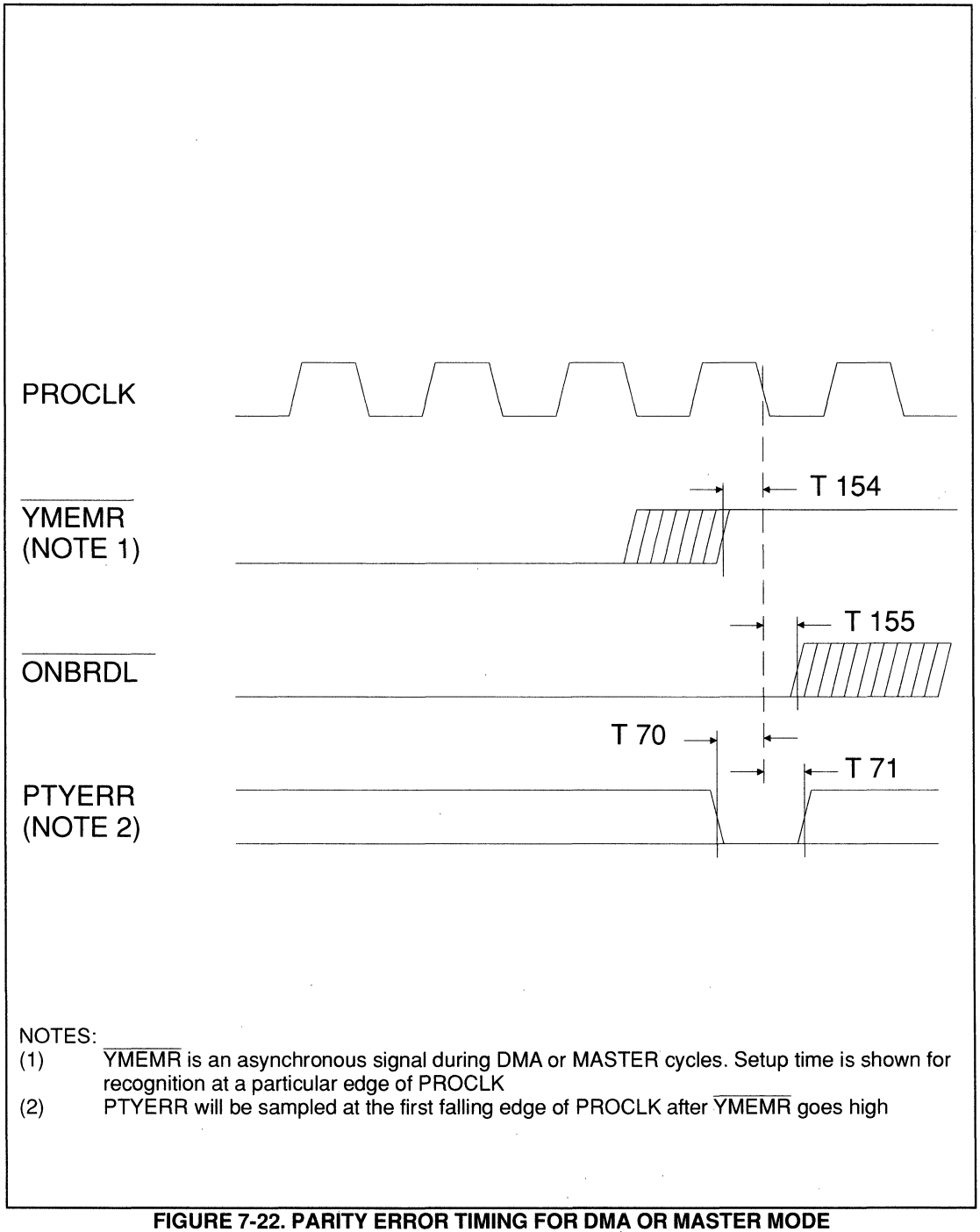
FIGURE 7-20. DMA TRANSFER TIMING: 8-BIT, ON-BOARD MEMORY TO I/O, ODD BYTE, WITH NO ADDED WAIT STATES



NOTES:

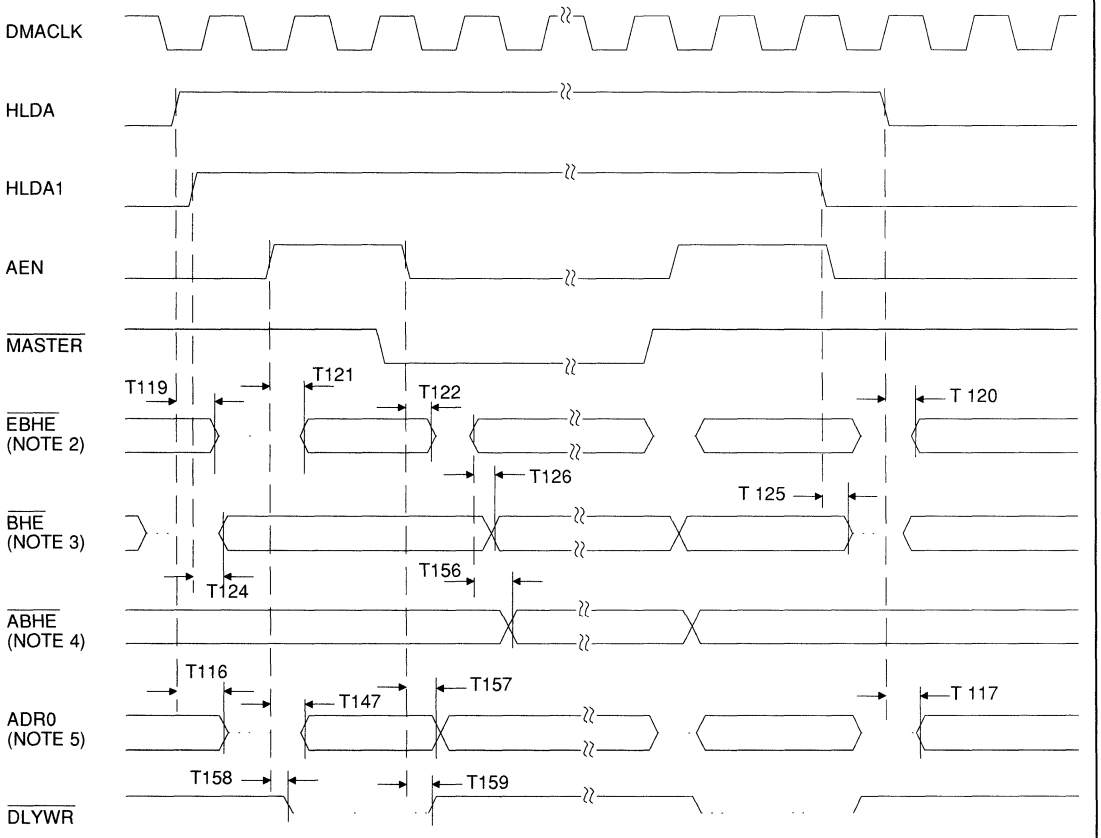
(1) No refresh cycles are pending
(2) ADR0 is tri-stated when HLDA goes high, then driven again when both DACK2 and AEN are high(16-Bit DMA)
(3) EBHE is tri-stated when HLDA goes high, then driven again when AEN is high
(4) ABHE is set low when HLDA, DACK2, and AEN are high
(5) BHE is driven by the FE3001 when HLDA1 is high. It follows EBHE
(6) The FE3010 drives these signals when AEN is high
(7) SDEN is high and SDTR is the inversion of DTR for this cycle
(8) DMARDY would follow the dashed line shown for any DMA cycle where IOCHRDY is not driven low (default timing)
(9) DMAMR, DLYWR, YMEMR, and YIOW timing is the same as for an 8-Bit I/O to memory cycle
(10) DMARDY is driven low by DMAMR in a Memory to I/O DMA cycle

FIGURE 7-21. DMA TRANSFER TIMING: 16-BIT, I/O TO ON-BOARD MEMORY, WAIT STATE ADDED



NOTES:
(1) YMEMR is an asynchronous signal during DMA or MASTER cycles. Setup time is shown for recognition at a particular edge of PROCLK
(2) PTYERR will be sampled at the first falling edge of PROCLK after YMEMR goes high

FIGURE 7-22. PARITY ERROR TIMING FOR DMA OR MASTER MODE TRANSFERS



NOTES:

(1) No refresh cycles are pending

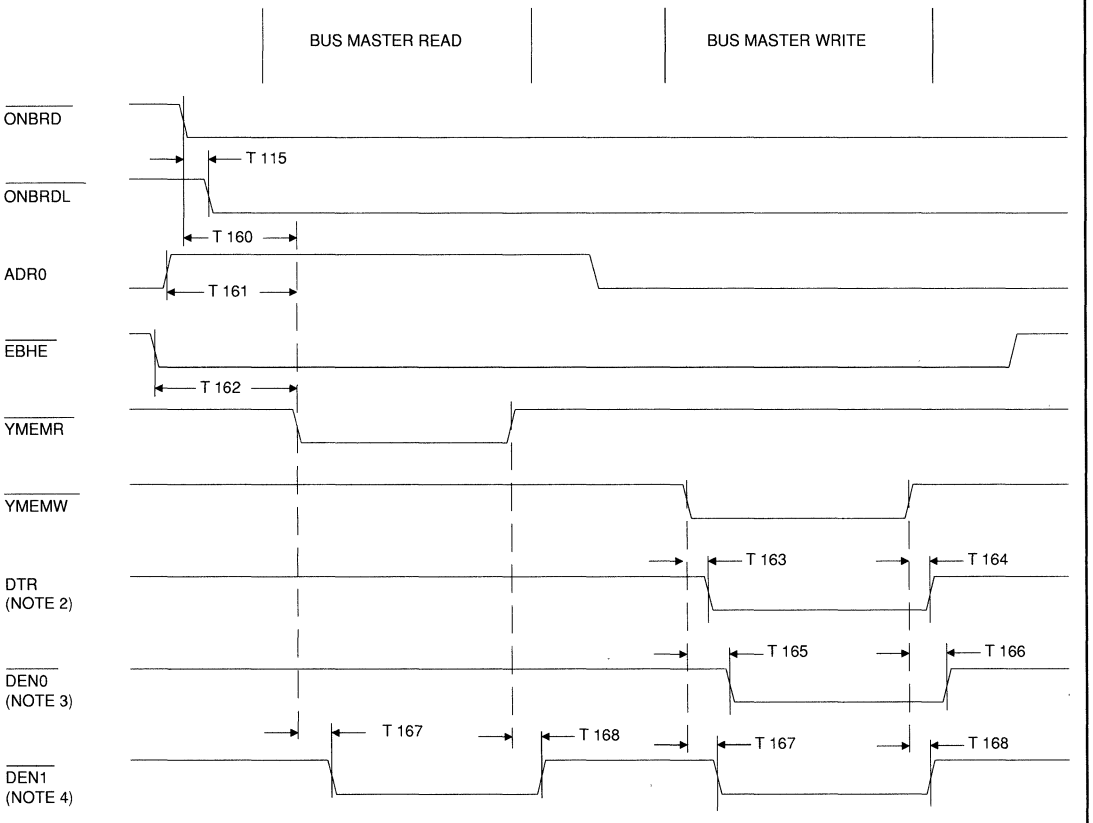
(2) EBHE is driven by the FE3001 when HLDA is low or AEN is high. It is driven by a Bus Master when MASTER is low

(3) BHE is driven by the FE3001 when HLDA1 is high. BHE will follow EBHE during Master mode

(4) ABHE follows EBHE during Master mode

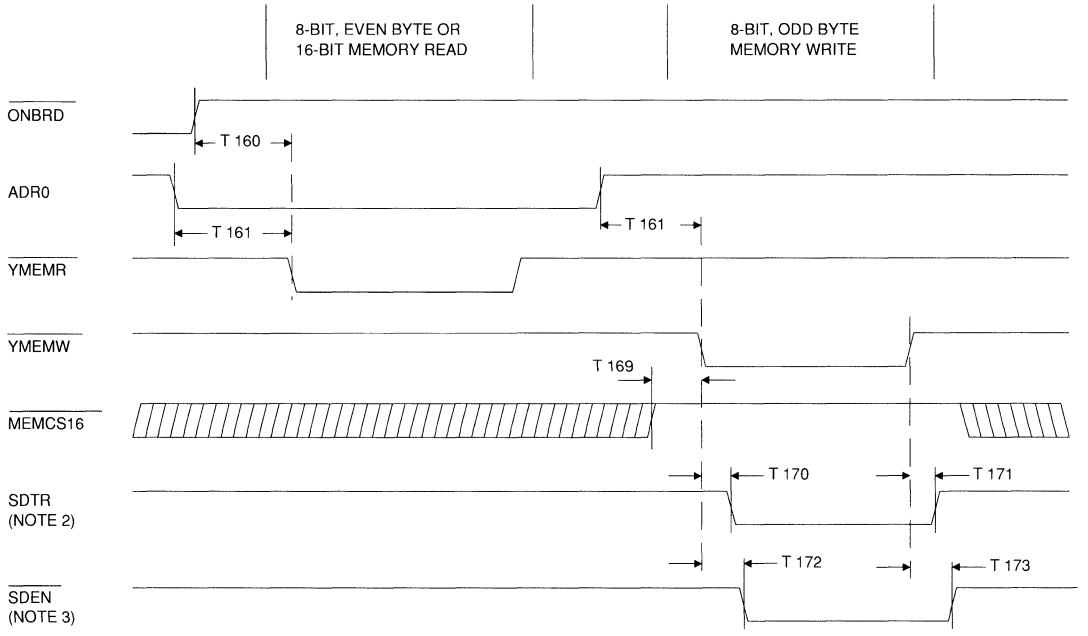
(5) ADR0 is driven by the FE3001 when HLDA is low. It will also be driven by the FE3001 when AEN is high if DACK2 is high (Bus Master uses DMA channel 5 - 7). ADR0 will be driven by the FE3021 when MASTER is low

FIGURE 7-23. BASIC MASTER MODE TRANSFER TIMING



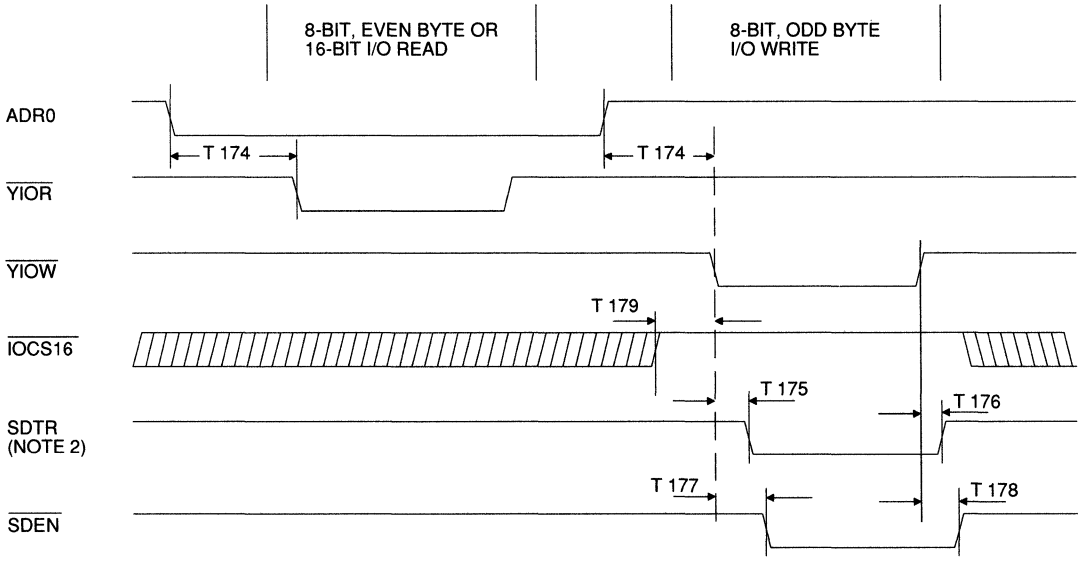
NOTES:
(1) MASTER is low during these cycles
(2) DTR follows YMEMW during Master Mode
(3) DEN0 follows YMEMR or YMEMW if both ONBRD and ADR0 are low
(4) DEN1 follows YMEMR or YMEMW if both ONBRD and EBHE are low
(5) SDEN is high during these cycles

FIGURE 7-24. MASTER MODE TRANSFER TIMING: ON-BOARD MEMORY READ/WRITE



NOTES:
(1) MASTER is low during these cycles
(2) SDTR follows YMEMW when MASTER is low
(3) SDEN follows YMEMR or YMEMW when ADR0, MEMCS16, and ONBRD are high
(4) DEN0 and DEN1 will stay high during these cycles because ONBRD is high

FIGURE 7-25. MASTER MODE TIMING: OFF-BOARD MEMORY READ/WRITE



NOTES:
(1) MASTER is low during these cycles
(2) SDTR follows YIOW
(3) SDEN follows YIOR or YIOW when ADR0 and IOCS16 are high. ONBRD does not affect SDEN for I/O cycles
(4) DEN0 and DEN1 will stay high during I/O cycles

FIGURE 7-26. MASTER MODE TIMING: OFF-BOARD I/O READ/WRITE

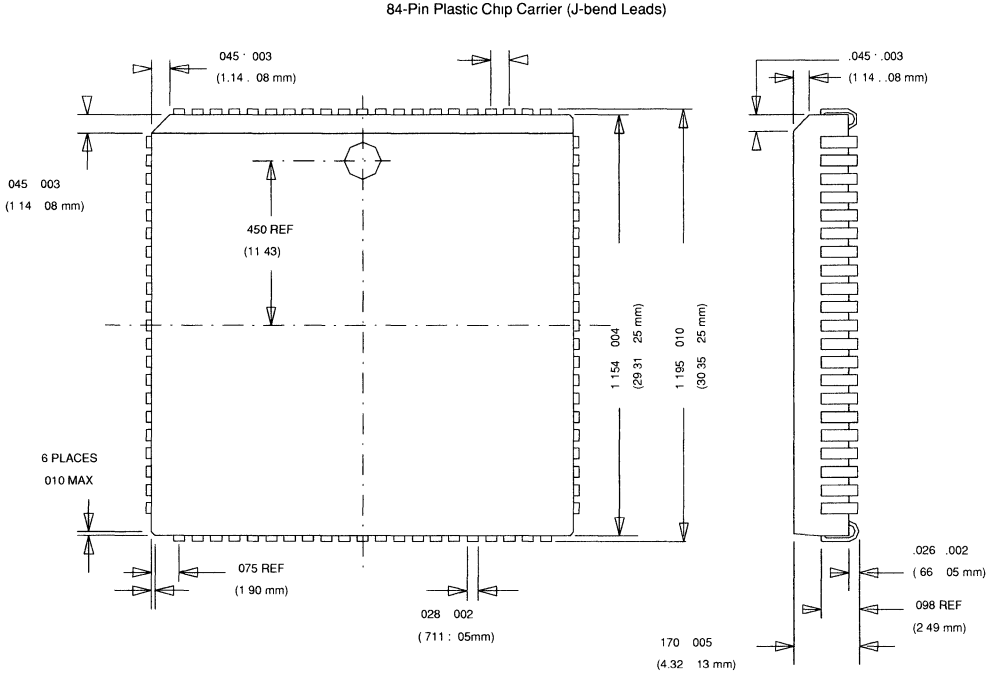


FIGURE 7-27. 84-PIN PLCC PACKAGING DIAGRAM

APPENDIX A
RECOMMENDED BUS CYCLE PROGRAMMING

The following tables give recommended values for programming bus timing registers R0-R8 (see Figure 5 and Table 3). These tables address only AT bus timing parameters, as on-board timing is very application specific. Values are provided for 6.25, 8, 12.5 and 16 MHz system clock speeds. The recommended values in these tables are based on emulating an 8 MHz IBM PC/AT Expansion Bus. Two issues that may affect these recommended values are listed below. Consult application notes for additional details.

(1) If the sum of R0 and R1 is 3 or greater, then an internal BALE logic error in first production FE3001 parts may cause BALE to remain high from a previous on-board cycle and fall one PROCLK cycle too early. Widening BALE by one clock accounts for this.

(2) Some adapter boards decode the SA0-SA19 address lines to generate $\overline{\text{MEMCS16}}$, a dangerous practice. However, widening BALE and delaying the commands relative to an 8 MHz AT provides relaxed $\overline{\text{MEMCS16}}$ setup time, which is needed for some of these boards to function reliably.

When preparing to select a new CPU clock speed, it is important to setup the FE3001 registers in a particular order so that BALE and commands do not become too short during the programming process. The recommended programming order for selecting high speed or low speed CPU clocks are given below:

Selecting High Speed CPU Clock:

R5, R6, R7, R8, R9, R10, R12, R4, R3, R1, R0

Selecting Low Speed CPU Clock:

R5, R6, R7, R8, R9, R10, R12, R0, R1, R3, R4

A.1 6.25 MHz SYSTEM CLOCK SPEED

REGISTER	FUNCTION	VALUE
R0	BALE delay from ALE leading edge	0
R1	BALE width	1
R3	8-bit memory, 8/16-bit I/O - command delay	1
R4	8-bit memory or I/O cycle - wait states	4
R5	16-bit I/O cycle - wait states	1
R6	16-bit memory cycle - command delay	0
R7	16-bit memory cycle - wait states	1
R8	Minimum number of wait states when ZEROWS is asserted	0

A.2 8 MHz SYSTEM CLOCK SPEED

REGISTER	FUNCTION	VALUE
R0	BALE delay from ALE leading edge	0
R1	BALE width	1
R3	8-bit memory, 8/16-bit I/O - command delay	1
R4	8-bit memory or I/O cycle - wait states	4
R5	16-bit I/O cycle - wait states	1
R6	16-bit memory cycle - command delay	0
R7	16-bit memory cycle - wait states	1
R8	Minimum number of wait states when ZEROWS is asserted	0

A.3 12.5 MHz SYSTEM CLOCK SPEED

REGISTER	FUNCTION	VALUE
R0	BALE delay from ALE leading edge	1
R1	BALE width	2
R3	8-bit memory, 8/16-bit I/O - command delay	4
R4	8-bit memory or I/O cycle - wait states	8
R5	16-bit I/O cycle - wait states	4
R6	16-bit memory cycle - command delay	2
R7	16-bit memory cycle - wait states	4
R8	Minimum number of wait states when ZEROWS is asserted	2

A.4 16 MHz SYSTEM CLOCK SPEED

REGISTER	FUNCTION	VALUE
R0	BALE delay from ALE leading edge	1
R1	BALE width	2
R3	8-bit memory, 8/16-bit I/O - command delay	4
R4	8-bit memory or I/O cycle - wait states	10
R5	16-bit I/O cycle - wait states	4
R6	16-bit memory cycle - command delay	2
R7	16-bit memory cycle - wait states	4
R8	Minimum number of wait states when ZEROWS is asserted	2

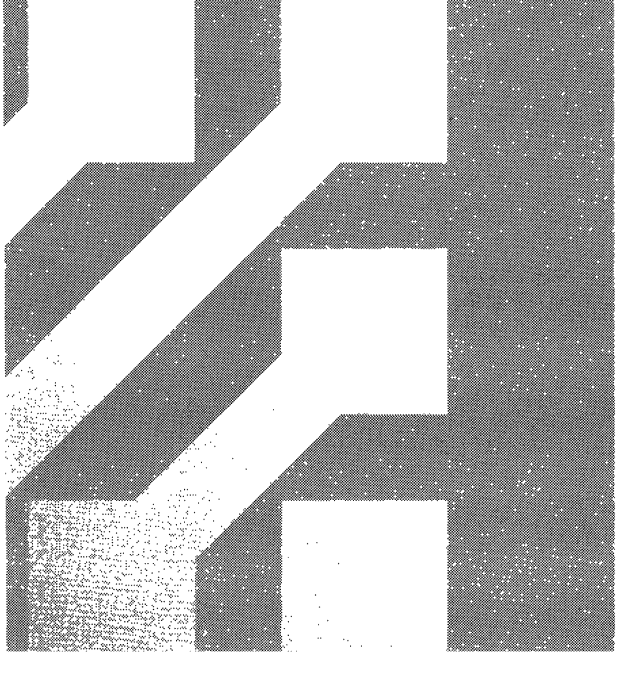
SYSTEMS LOGIC/PERIPHERAL

2

FE3001A

AT Clock Generation and

Cycle Control Device



WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

ADDITIONAL REFERENCES

IBM AT Technical Reference Manual

Intel Microprocessor and Peripheral Handbook

2

1.0 INTRODUCTION

1.1 DESCRIPTION

The FE3001A contains all of the clock generation and cycle control logic necessary to implement an IBM AT compatible computer. It is part of the FE3600B/C chip set intended to simplify the design of 80286/80386SX based AT computers.

Its features include programmable CPU and DMA clock generation, system clock generation, programmable bus timing, programmable wait state generator, refresh and DMA controls, bus arbitration logic, NMI generator and parity error logic, reset/shutdown control, sleep mode, 80286 interface logic and is packaged in an 84-pin PLCC.

1.2 FEATURES

- Programmable CPU and DMA clock generator
- System clock generator
- Programmable bus timing
- Programmable wait state generator
- Refresh and DMA controls
- Bus arbitration logic
- NMI generator and parity error logic
- Reset/shutdown control
- Sleep mode
- 80286 interface logic
- 1.25 micron HCMOS technology
- 84-pin PLCC

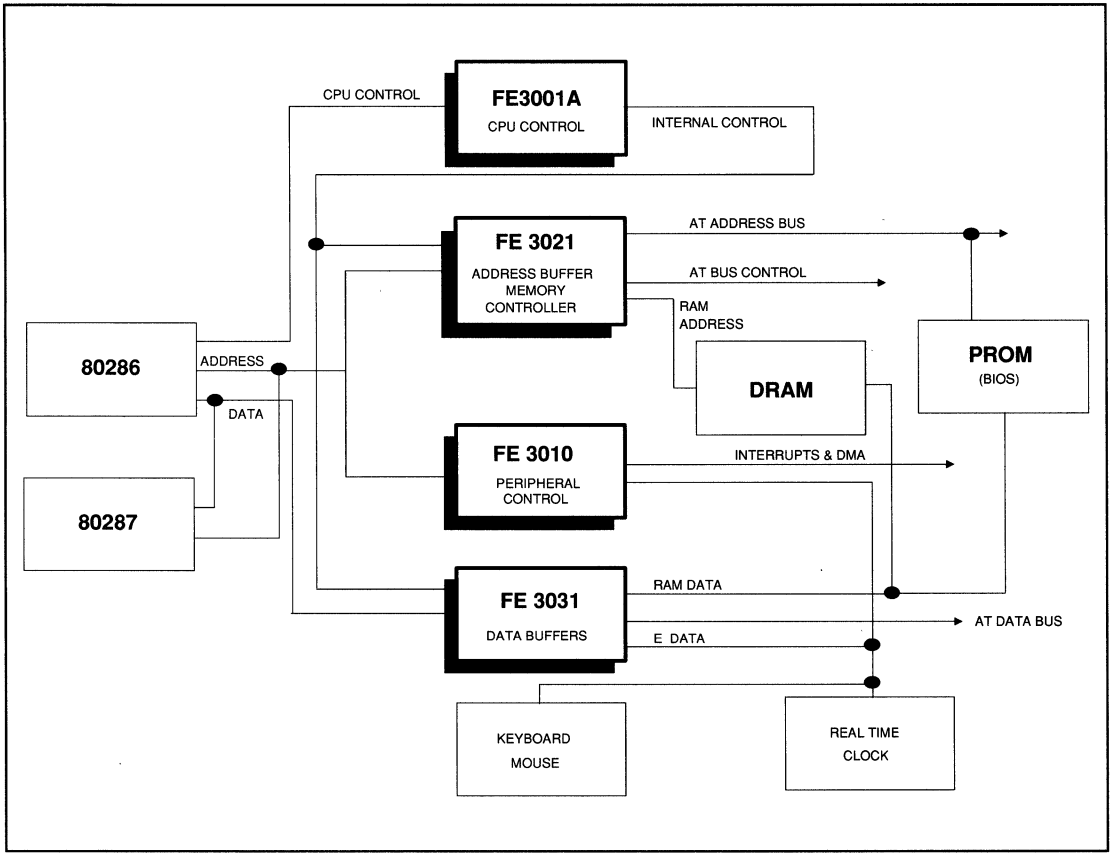


FIGURE 1-1. FE3600B/C CHIP SET FUNCTIONAL BLOCK DIAGRAM

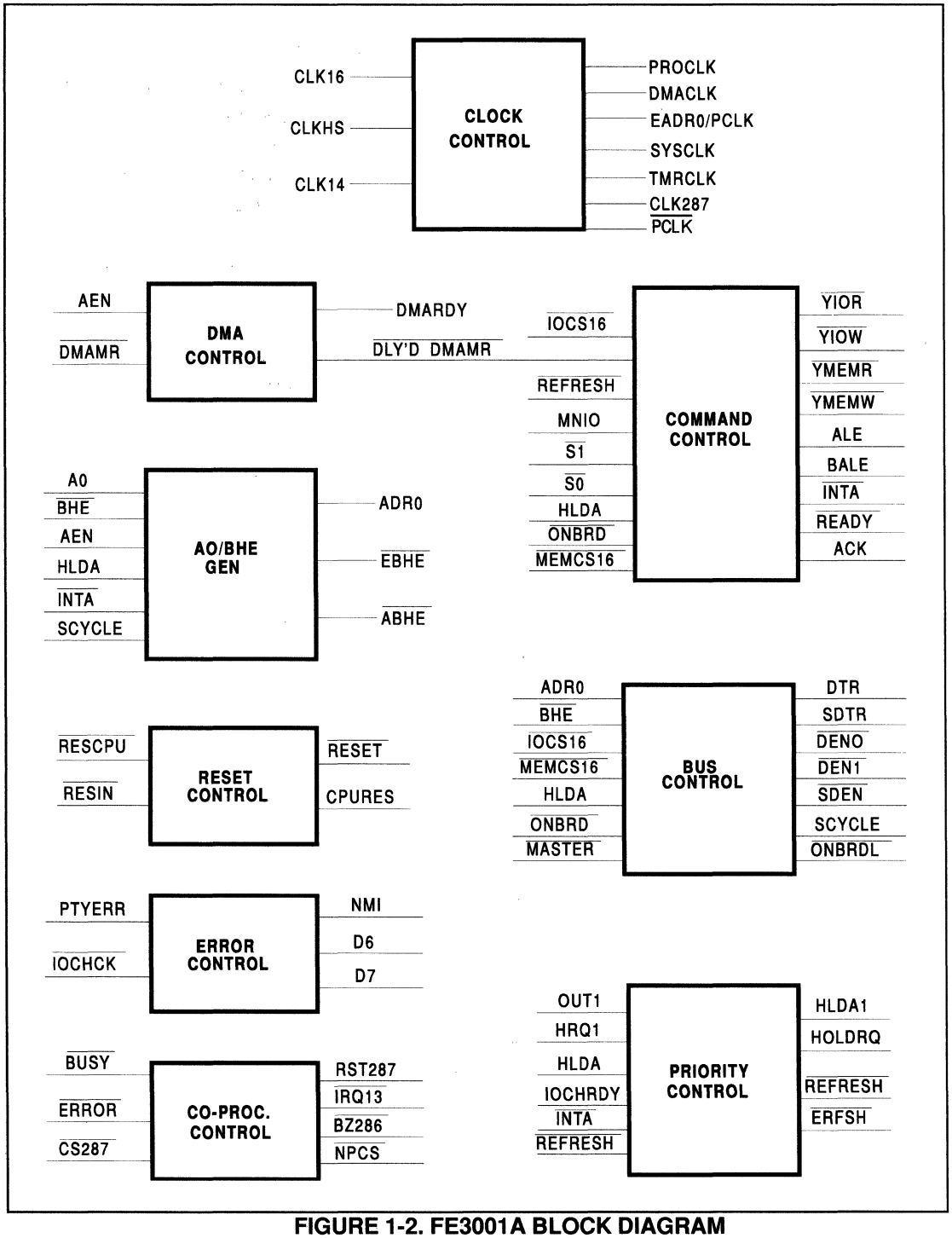


FIGURE 1-2. FE3001A BLOCK DIAGRAM

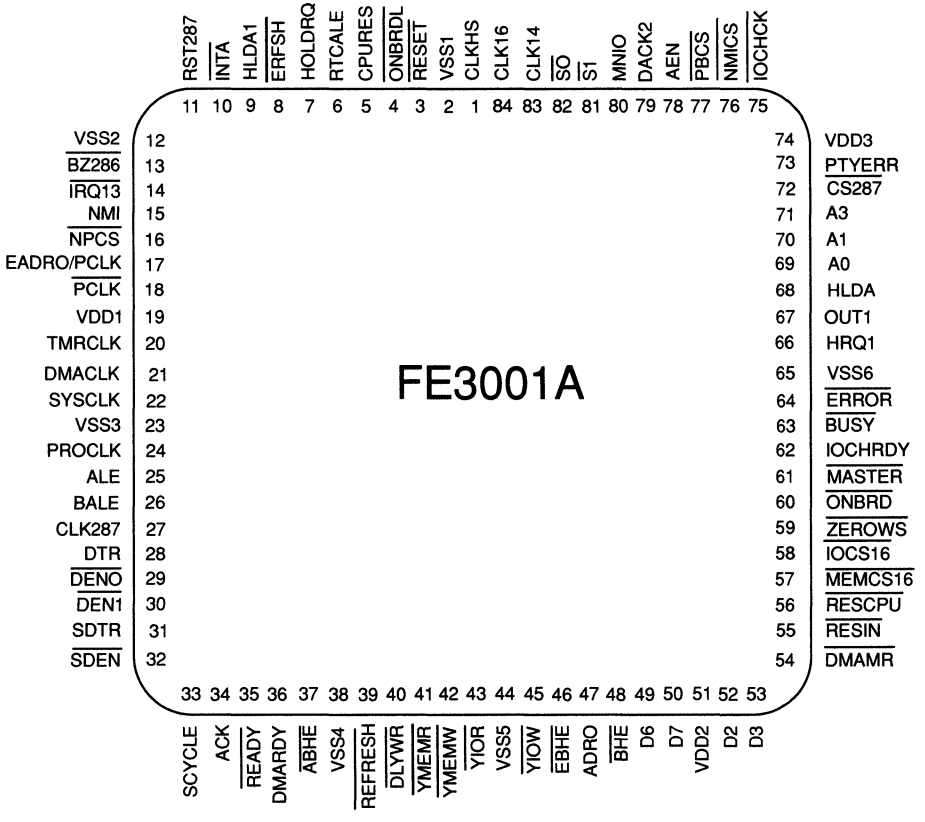


FIGURE 1-3. FE3001A PIN ASSIGNMENTS

PIN#	SIGNAL	TYPE	DESCRIPTION
1	CLKHS	I	High speed clock input. This provides the high speed clock when selected. When CLK16 (pin 84 is pulled high, this input (divided by two) is used as the low speed clock.
2	V_{SS1}		Ground.
3	$\overline{\text{RESET}}$	O	Reset to the system.
4	$\overline{\text{ONBRDL}}$	O	$\overline{\text{ONBRD}}$ input latched by ALE internally. Follows $\overline{\text{ONBRD}}$ when HLDA high.
5	CPURES	O	Reset to 80286.
6	RTCALE	O	Real Time Clock Address Latch Enable (I/O address 70H).
7	HOLDRQ	O	Hold request to 80286 for DMA or Refresh.
8	$\overline{\text{ERFSH}}$	O	Enable refresh address signal to 3010. Puts refresh address on address bus.
9	HLDA1	O	DMA hold acknowledge signal to FE3010. Not active during refresh.
10	$\overline{\text{INTA}}$	O	Interrupt acknowledge to FE3010.
11	RST287	O	Reset to 80287 (Write to I/O address F1H or system reset).
12	V_{SS2}		Ground.
13	$\overline{\text{BZ286}}$	O	80287 busy signal to 80286. Latched low by 80287 ERROR signal.
14	$\overline{\text{IRQ13}}$	O	Interrupt request 13 for 80287 error to FE3010.
15	NMI	O	Non-Maskable Interrupt to 80286. Generated in response to a parity error or bus IOCHCK.
16	$\overline{\text{NPCS}}$	O	80287 Co-processor chip select. (I/O Addresses F8H, FAH and FCH).
17	EADR0/ PCLK	O	7.16 MHz clock for keyboard controller/ EADRO for AT bus.
18	$\overline{\text{PCLK}}$	O	Inverted PCLK for keyboard controller.
19	V_{DD1}		+5 V V_{DD}.
20	TMRCLK	O	1.19 MHz timer clock to FE3010.
21	DMACLK	O	Software selectable clock for DMA to FE3010.

TABLE 1-1. SIGNAL DESCRIPTIONS

PIN#	SIGNAL	TYPE	DESCRIPTION
22	SYSCLK	O	System clock needed for bus timing. See description in synchronization section.
23	V_{SS3}		Ground.
24	PROCLK	O	Software selectable 80286 /80386SX clock.
25	ALE	O	Local Address Latch Enable.
26	BALE	O	Bus Address Latch Enable. (Programmable)
27	CLK287	O	Clock for 80287. See clock section for details.
28	DTR	O	Data direction to FE3031 data buffer.
29	$\overline{\text{DEN0}}$	O	Low byte PC/AT Bus data enable to FE3031 data buffer.
30	$\overline{\text{DEN1}}$	O	High byte PC/AT Bus data enable to FE3031 data buffer.
31	SDTR	O	PC/AT Bus byte swap direction to FE3031 data buffer.
32	$\overline{\text{SDEN}}$	O	PC/AT Bus byte swap enable to FE3031 data buffer.
33	SCYCLE	O	Latch low byte during byte swap read.
34	ACK	O	DMA or Refresh Acknowledge signal to the PC/AT bus.
35	$\overline{\text{READY}}$	O	Ready to 80286.
36	DMARDY	O	When high allows FE3010 to complete a DMA cycle.
37	$\overline{\text{ABHE}}$	O	High byte enable for devices on local bus.
38	V_{SS4}		Ground.
39	$\overline{\text{REFRESH}}$	I/O	Refresh cycle. Generated from FE3010 timer signal OUT1 or externally from the bus.
40	$\overline{\text{DLYWR}}$	I/O	$\overline{\text{YIOW}}$ delayed to the FE3010, active edge delayed one PROCLK. Input from FE3010 during DMA to generate $\overline{\text{YIOW}}$.
41	$\overline{\text{YMEMR}}$	I/O	Memory read. Input during Master cycle.
42	$\overline{\text{YMEMW}}$	I/O	Memory write. Input during HLDA cycle.
43	$\overline{\text{YIOR}}$	I/O	I/O read. Input during HLDA cycle.

TABLE 1-1. SIGNAL DESCRIPTIONS (Continued)

PIN#	SIGNAL	TYPE	DESCRIPTION
44	V_{SS5}		Ground.
45	$\overline{YIOW}$	I/O	I/O write. Input during Master cycle.
46	$\overline{EBHE}$	I/O	High byte enable to expansion bus. Input during Master cycle.
47	ADR0	I/O	Low byte enable. Latched with ALE during a CPU cycle, driven low during 16-Bit DMA cycles.
48	$\overline{BHE}$	I/O	High byte enable from the 80286. Output during Master and DMA cycles for use by the FE3021.
49	D6	I/O	Peripheral data bus bit 6.
50	D7	I/O	Peripheral data bus bit 7.
51	V_{DD2}		+5 V V_{DD}.
52	D2	I	Peripheral data bus bit 2.
53	D3	I	Peripheral data bus bit 3.
54	$\overline{DMAMR}$	I	DMA memory read from DMA controller.
55	$\overline{RESIN}$	I	System reset input.
56	$\overline{RESCPU}$	I	CPU reset input from keyboard controller.
57	$\overline{MEMCS16}$	I	Signals 16-bit memory transfer capability on the PC/AT bus.
58	$\overline{IOCS16}$	I	Signals 16-bit I/O transfer capability on PC/AT bus.
59	$\overline{ZEROWS}$	I	Zero wait state bus cycle request. See description for more details.
60	$\overline{ONBRD}$	I	16-bit on-board DRAM memory, BIOS, or I/O device. Implies local memory on memory cycles and fast I/O bus timing for I/O cycles.
61	$\overline{MASTER}$	I	Master on PC/AT bus has control of the bus when asserted.
62	IOCHRDY	I	Current bus cycle may complete when high. May be used to extend CPU, DMA, or refresh cycles.
63	$\overline{BUSY}$	I	80287/80387SX co-processor busy.
64	$\overline{ERROR}$	I	Error from 80287/80387SX.
65	V_{SS6}		Ground.

TABLE 1-1. SIGNAL DESCRIPTIONS (Continued)

PIN	SIGNAL	TYPE	DESCRIPTION
66	HRQ1	I	Hold request from DMA controller in FE3010.
67	OUT1	I	Refresh timer input from FE3010.
68	HLDA	I	Hold acknowledge from 80286.
69	A0	I	Local 80286 address bus 0.
70	A1	I	Local 80286 address bus 1.
69	A0	I	Local 80286 address bus 0.
70	A1	I	Local 80286 address bus 1.
71	A3	I	Local 80286 address bus 3.
72	$\overline{CS287}$	I	80287 select decode from FE3021 (0E0H - 0FFH) during I/O cycle. ROM chip select decode during memory cycle..
73	PTYERR	I	On-board RAM parity error. Sampled on the first falling edge of PROCLK after YMEMR goes high.
74	V_{DD3}		+5 V V_{DD}.
75	$\overline{IOCHCK}$	I	Error from PC/AT bus.
76	$\overline{NMICS}$	I	NMI port enable decode (07XH). Also used for programming bus control registers.
77	$\overline{PBCS}$	I	Port B chip select decode (061H - 06FH, 0DD). See register description for decode definitions.
78	AEN	I	DMA cycle enable from FE3010.
79	DACK2	I	16-bit DMA acknowledge from FE3010.
80	M/$\overline{IO}$	I	80286 memory/IO select. High indicates memory halt, or shutdown cycles. Low indicates I/O or interrupt acknowledge cycles.
81	$\overline{S1}$	I	80286 Status 1.
82	$\overline{S0}$	I	80286 Status 0.
83	CLK14	I	14.318 MHz clock input used to derive TMRCLK, EADR0/PCLK, and $\overline{PCLK}$.
84	CLK16	I	16 MHz clock input. This provides the low speed CPU clock for 8 MHz operation. When this pin is pulled high, CLKHS ÷ 2 is used as the low speed clock.

TABLE 1-1. SIGNAL DESCRIPTIONS (Continued)

2.0 FUNCTIONAL DESCRIPTION

2.1 FUNCTIONAL OVERVIEW

The FE3001A is designed to run with the FE3010 peripheral controller, and the FE3021 and FE3031 buffers/memory controls to create a 16 MHz or 20 MHz PC/AT compatible system. The basic architecture of an AT compatible system using the FE3600B/C chip set involves putting the system DRAM on the local data and command bus, allowing high speed access. The BIOS ROM can be put on the local bus or expansion bus; the FE3021 has special provisions to use the ROM on the higher speed bus. During accesses to local memory, the data buffer controls in the FE3001A prevent data collisions between the local and expansion buses. The FE3021 and FE3031 also inhibit memory read and write signals to the expansion bus for local memory accesses.

The FE3001A generates all of the clocks needed in the system. The CPU clock to the 80286/80386SX processor (PROCLK) is programmable, as is the DMA clock for the DMA controller in the FE3010 (DMACLK). The expansion bus clock (SYSCLK) and coprocessor clock for the 80287 (CLK287) automatically adjust to the current operating configuration. The clock for the timers in the FE3010 (TMRCLK) is fixed at 1.19 MHz, and the clocks for the keyboard controller (PCLK and $\overline{\text{PCLK}}$) are fixed at 7.16 MHz.

The FE3001A has registers to delay the five commands (memory read and write, I/O read and write, interrupt acknowledge) during a CPU cycle and control the length of the commands based on various input signals (16-bit memory, 16-bit I/O, on-board memory, fast 16-bit I/O device, and zero wait state device). On power-up, these registers are loaded with values to run the system with a 16 MHz PROCLK (8 MHz system) with full AT compatibility and no register programming necessary. Before switching to high speed operation, it is necessary to program the registers for proper bus emulation. These registers eliminate the need to either slow down the processor for expansion bus operations or run the bus asynchronously. Note that a 16 MHz system can be made to exactly match the bus timing of an 8 MHz system.

2.2 CLOCK GENERATOR

This module generates clocks for the CPU, DMA, 8042 keyboard controller, timer and 80287 numeric processor. The CPU clock is software selectable for low speed or high speed CPU operation. The DMA clock is also software selectable between standard and high speed. The 80287 clock is fixed at the low speed CPU clock.

2.2.1 PROCLK

The CLK16 and CLKHS input clocks to the FE3001A are used to create the low speed and high speed clocks to the CPU. The CLKHS input is used when the high speed CPU clock is selected. If the CLK16 input is connected to an oscillator, it will be used when the low speed CPU clock is selected (typically from 6 to 8 MHz CPU speed). Alternatively, if CLK16 is tied high through a pullup resistor, then CLKHS ÷ 2 will be used as the low speed clock, saving an oscillator.

The CPU clock circuitry ensures a glitchless speed switch. PROCLK will be held high at no more than 1 1/2 clock periods of the clock being selected in order to achieve synchronization. Since SYSCLK and DMACLK are based on PROCLK, they will also switch speeds without glitches.

2.2.2 DMACLK

DMACLK can be software selected between standard speed and a special high speed mode. Standard speed provides a 4 MHz DMA clock to the DMA controller on a 16 MHz system, the same as an 8 MHz IBM PC/AT. This will be the most common selection of DMA speed. Selecting high speed DMA runs the DMA controller at twice standard speed. This would likely be confined to special dedicated systems where only well defined DMA peripherals that can run that fast are used.

DMACLK is PROCLK ÷ 4 when the low speed CPU clock is selected. DMACLK is PROCLK ÷ 8 when the high speed CPU clock is selected. When R13 bit 7 is set, DMACLK is PROCLK +12 at high speed. DMACLK will always change on CPU "t" state boundaries, but no other synchronization is attempted. The previous discussion applies to standard speed DMA. If high speed DMA is selected, it runs twice as fast in all cases.

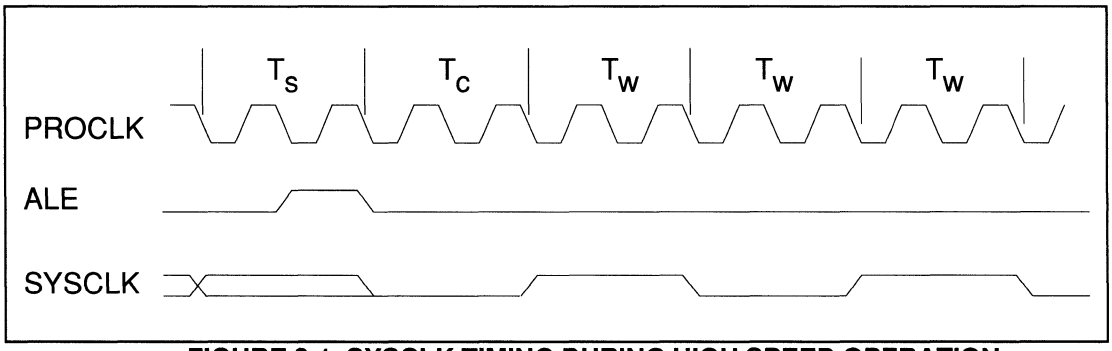


FIGURE 2-1. SYSCLK TIMING DURING HIGH SPEED OPERATION

2.2.3 CLK287

CLK287 is always the same as the low speed CPU clock. It is not affected by speed switching. It follows CLK16 if that input is toggling or is CLKHS ÷ 2 if CLK16 is pulled high.

2.2.4 SYSCLK

When the low speed clock is selected, SYSCLK is PROCLK ÷ 2. During high speed operation, SYSCLK is PROCLK ÷ 4. When R13 bit 7 is set, SYSCLK is PROCLK ÷ 6. In the high speed case, SYSCLK is brought into synchronization with the PC/AT bus at the end of ALE. See Figure 4 for SYSCLK functional timing.

2.2.5 PCLK/EADRO, $\overline{\text{PCLK}}$, and TMRCLK

The CLK14 input is used to generate EADR0/PCLK, $\overline{\text{PCLK}}$, and TMRCLK. It must be 14.31818 MHz in order for TMRCLK to be 1.1932 MHz, as required for the timers in the FE3010 to be AT compatible. TMRCLK is CLK14 ÷ 12. EADR0/PCLK is CLK14 ÷ 2 (7.16 MHz). $\overline{\text{PCLK}}$ is the complement of EADR0/PCLK. EADR0/PCLK and $\overline{\text{PCLK}}$ can be used to drive the 8042 keyboard controller.

During power up, PCLK/EADRO will behave like PCLK. When $\overline{\text{RESIN}}$ goes high while $\overline{\text{RESET}}$ is low, the $\overline{\text{DMAMEMR}}$ input will be sampled. If sampled high, this pin will behave as PCLK until the next rising edge of $\overline{\text{RESIN}}$. If sampled low, this pin will behave as EADRO. See Section 2.5.4 for details.

2.2.6 Stopping the Clocks (Sleep Mode)

Software may put the FE3001A in sleep mode by setting port 063H bit 6. In sleep mode, PROCLK and DMACLK will be stopped at a high level. SYSCLK will also be stopped, but at an indeterminate logic level. DMACLK and PROCLK will each stop on their rising edge of phase 2 after HLDA is seen active by the FE3001. Typically, this would be the first refresh cycle after the sleep bit is written. SYSCLK will stop with PROCLK.

By stopping these clocks, power can be conserved in battery operated systems. Note that a static CMOS 80286 must be used in order to stop the CPU clock. EADR0/PCLK, $\overline{\text{PCLK}}$, TMRCLK, and CLK287 will continue to run in sleep mode, allowing the keyboard controller, timers, and coprocessor to operate. Either a keyboard interrupt or a system clock interrupt is a likely choice to wake the CPU up.

To restart the clocks (wake up the CPU), the $\overline{\text{RESCPU}}$ input must be pulsed low. The rising edge of $\overline{\text{RESCPU}}$ will kick off internal synchronization that will restart the clocks roughly 2 EADR0/PCLK periods later. No glitches will occur on the clocks as a result of a restart. Also note that the pulse on $\overline{\text{RESCPU}}$ will not reset the CPU if the FE3001A is in sleep mode. Refer to Application Notes for information on external logic needed to implement sleep mode.

2.3 COMMAND CONTROL

This module generates the I/O read and write commands, memory read and write commands, interrupt acknowledge, ALE and BALE from S1, S0, and MNIO. It also controls the number of wait states used during each CPU cycle. See the register descriptions for programming information. For recommended program values, refer to Appendix A.

2.3.1 On-Board Cycles

When the ONBRD signal is active, then this cycle is directed toward 16-bit, high speed local DRAM, BIOS, or I/O. The timing for this cycle is defined by registers R9, R10, and R12. The AT bus timing signals MEMCS16 and IOCS16 have no effect. IOCHRDY can be used to lengthen the cycle, and indeed is used by the FE3021 to add wait states for a DRAM page miss or EMS cycles.

The wait states for on-board reads and writes are individually programmable by registers R9 and R10 in order to optimize DRAM access speed. Both memory and I/O cycles use these values. The command delay for on-board I/O cycles is set by register R12. The command delay for on-board memory cycles is always zero.

2.3.2 AT Bus Cycles

All I/O and memory cycles where ONBRD is inactive will be directed to the AT bus. The command delay and wait states are programmable for each type of AT bus cycle.

Memory cycles use 16-bit timing when MEMCS16 is driven low before either the memory command (YMEMR or YMEMW) is programmed to go active or BALE falls, whichever is earlier. I/O cycles use 16-bit timing when IOCS16 is driven low before the I/O command (YIOR or YIOW) is programmed to go active. Otherwise, all cycles use 8-bit timing.

ZEROWS can be driven low for either 8-bit or 16-bit cycles to terminate the cycle early. As on the AT, it should not be driven until a command is active. It will cause the cycle to end after the prescribed minimum number of wait states in register R8 is met. Note that the FE3001A contains circuitry to ensure that an AT bus cycle will end (command goes high) on a rising edge of SYSCLK and will add a wait state if needed to enforce this. This synchronization circuitry will override register programming and the IOCHRDY and ZEROWS inputs.

2.3.3 Other Cycles

Interrupt acknowledge cycles follow the same command timing as an 8-bit AT bus cycle. HALT cycles do not generate ALE, BALE or cause the READY output to go high. Effectively, the FE3001A does not respond to a HALT cycle. A SHUTDOWN cycle is handled like a HALT, except that it causes the CPURES line to be pulsed, resetting the CPU only.

2.4 BUS CONTROL

This module generates the data buffer controls for CPU, DMA, and refresh cycles. DEN0 and DEN1 are used to enable the lower and upper bytes of the FE3031 AT bus data buffers, respectively. DTR sets the direction of these buffers. SDEN and SDTR control the enable and direction of a buffer which transfers data between the upper and lower bytes of the AT data bus. The rising edge of SCYCLE latches data on the lower byte of the AT bus into the FE3031, needed for 16-bit to 8-bit bus conversion cycles. ONBRDL is ONBRD latched by ALE to keep it valid throughout the cycle.

The ONBRD signal is used to indicate on-board DRAM and I/O operations. On-board memory and fast on-board I/O devices are assumed to be 16-bit devices. During CPU cycles which access on-board memory, the AT data buffers will be disabled. For Bus Master and DMA cycles, ONBRD must be decoded only for on-board memory.

2.5 A0/BHE GENERATOR

This module generates the system ADR0, ABHE, EBHE, and EADRO using A0 and BHE from the 80286 CPU and AEN and DACK2 from the DMA controller in the FE3010.

2.5.1 ADR0

During CPU cycles, A0 from the 80286 is latched with ALE to produce ADR0. For 16-bit DMA transfers and interrupt acknowledge cycles, ADR0 is forced low so that the low byte of the data bus is activated. For all other CPU hold conditions ADR0 is tri-stated. The FE3001A performs two cycles when the CPU attempts a 16-bit operation to an 8-bit device on an even address boundary. ADR0 is automatically forced to one at the start of the second cycle to select the second byte.

2.5.2 ABHE

ABHE is the local upper byte select used by the FE3031. During CPU cycles, ABHE is BHE latched with ALE. It is forced low during 16-bit DMA (DACK2 and AEN inputs high) so that the upper byte is always selected. For 8-bit DMA, it is the inversion of ADR0 so that only one byte is selected at a time. During master mode, ABHE follows the EBHE input.

2.5.3 EBHE

EBHE is the upper byte select of the AT bus. During CPU cycles, EBHE is ABHE latched with BALE to provide proper AT bus timing. During DMA, EBHE follows ABHE. During refresh the EBHE output is disabled. It is an input during master mode transfers.

2.5.4 EADRO

EADRO is the lower byte select of the AT bus. During CPU cycles, EADRO is ADRO latched with BALE to provide proper AT bus timing. During DMA and refresh, EADRO follows ADRO. This pin will disable during master mode transfer.

2.6 PRIORITY CONTROL

The priority control module generates the hold request signal to the CPU in response to a request from the DMA controller or refresh timer.

2.6.1 Refresh Cycles

The FE3001A generates a hold request in response to a rising edge on the OUT1 input, signalling that a refresh cycle is needed. A refresh cycle is initiated when HLDA comes back from the CPU. The FE3001A refresh state machine drives REFRESH low to signal a refresh cycle to the AT bus, and sets ERFSH low to the FE3010 to enable the refresh address onto the CPU address bus. YMEMR will also be strobed low during a refresh cycle. Refer to the timing diagrams for more detail. Note that REFRESH is a bidirectional open-collector signal, and a refresh cycle can be started by an expansion card.

2.6.2 DMA Cycles and Request Arbitration

Requests for control by the DMA controller are made by taking the HRQ1 input high. The FE3001A grants control to the DMA controller by setting HLDA1 high.

When the FE3001A receives a HLDA, it grants control either to the refresh state machine (REFRESH goes low) or to the DMA controller (HLDA1 goes high). Priority is given to the refresh state machine in the event of simultaneous requests. Note that if simultaneous requests do exist, then HOLDRQ will not be dropped after the first request is satisfied. Instead, the FE3001A will grant control sequentially to both requestors with the same HLDA.

2.7 DMA CONTROL

This module generates the DMARDY signal for the FE3010 peripheral controller. This signal indicates that the DMA may complete its cycle. The module also generates YMEMR during DMA by delaying the leading (falling) edge of the FE3010 DMAMR signal by one DMA clock.

2.8 ERROR CONTROL

This module generates a non-maskable interrupt (NMI) to the 80286 when a parity error or system bus error is encountered. Parity error, system bus error or NMI can be enabled or disabled from software. They are all disabled on system reset.

The PTYERR input is examined each time YMEMR goes high and it is an on-board cycle (ONBRDL low). The state of the PTYERR input is actually latched on the first falling edge of PROCLK after YMEMR goes high for all on-board CPU reads. When HLDA is active, the PTYERR input is sampled on the riding edge of YMEMR. If PTYERR was high, it signals a parity failure and will generate an NMI to the CPU if enabled. However, when R13 bit 6 is set, FE3001A will disqualify the PTYERR with the CS287 signal. So, NMI will not be generated for ROM cycles. This can eliminate the external glue l ogic. The PTYERR from FE3031 can be connected to PTYERR input of the FE3001A directly. The parity error latch can be cleared by disabling and then enabling parity errors.

The IOCHCK input is driven low by a device on the AT bus to signal a catastrophic error, such as a parity error on a plug-in RAM card. A low on the IOCHCK input will generate an NMI to the CPU if enabled. The error condition can be cleared by disabling and then enabling IOCHCK. However, the IOCHCK input must also be reset high or it will generate another NMI.

When the CPU receives an NMI, it can interrogate I/O register 061H (PORT B) to determine whether a parity error or an IOCHCK is the source of the interrupt. Note that this is the only time the FE3001A will drive the data bus. All other I/O locations are write only. Also, only bits 6 and 7 will be driven during the read. The FE3010 will supply the 6 lower order bits.

2.9 COPROCESSOR INTERFACE

The coprocessor interface module provides the system interface to the 80287 numeric processor extension. The reset and chip select to the 80287 are generated in this module in addition to the busy signal to the CPU and interrupt request 13 to the interrupt controller.

In a FE3600B/C system, as in any PC/AT compatible system, ERROR from the 80287 coprocessor is not connected to the ERROR input on the 80286/80386SX. Instead, the ERROR input on the 80286/80386SX is tied high, while BUSY and interrupt request 13 are used to flag errors. The FE3001A has a BZ286 output which connects to the BUSY input of the 80286/80386SX. It also has ERROR and BUSY inputs which hook to those outputs from the 80287/80387SX.

Normally, BZ286 just follows the BUSY input. However, when ERROR goes low while BUSY is low, IRQ13 will go active to signal the CPU that a coprocessor error has occurred. IRQ13 will stay active until ERROR goes back high. Also, BZ286 will be latched low to prevent another coprocessor instruction from being loaded. BZ286 will stay low until either the 80287/80387SX is reset or there is a write to I/O address 0F0H. When either of these occurs, then BZ286 will return to following the BUSY input.

The FE3001A RST287 output connects to the 80287 RESET input. This allows the coprocessor to be reset through software by an I/O write to address 0F1H. It will also be reset when the system RESET output is active.

The FE3001A expects the CS287 input to be active for addresses 0E0H-0FFH. This is used to provide the NPCS chip select decode output for the 80287. It will be active for addresses 0E8H-0EFH and 0F8H-0FFH when INTA is high and M/ IO from the CPU was low for this cycle.

2.10 RESET ONTROL

This module generates the CPURES signal which is used to reset only the 80286/80386SX and the RESET signal which resets the rest of the system (including the FE3001A). The RESIN input causes a full system reset when driven low. Both CPURES and RESET will go active for as long as RESIN is low and for at least 30 PROCLK cycles after RESIN goes high.

The RESCPU input, when driven low, causes only the CPURES output to go high. RESCPU would normally be connected to both the 8042 keyboard controller and the FE3021 (to provide "hot" reset). The CPURES output will stay high for at least 16 CPUCLK periods, longer if RESCPU remains low. CPURES will also go high for 16 CPUCLK periods if the 80286 executes a shutdown cycle.

M/ IO	S1	S0	TYPE OF BUS CYCLE
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	None, not a status cycle
1	0	0	Halt (if A1 =1) or Shutdown (if A1 = 0)
1	0	1	Memory Read
1	1	0	Memory Write

TABLE 2-1. BUS CYCLES

2.11 GENERAL NOTES

$\overline{ONBRD}$ must not be active during interrupt acknowledge cycles.

For memory cycles with $\overline{ONBRD}$ asserted, the system will use the MDATA bus of the FE3031 for data transfers. For I/O cycles with $\overline{ONBRD}$ asserted, the system will use the expansion bus (DATA) of the FE3031 for data transfers.

On-board I/O devices must drive $\overline{IOCS16}$ in order for a Bus Master to access them as 16-bit devices. Otherwise, $\overline{SDEN}$ will go low for Bus Master I/O cycles where ADR0 is high.

Inputs CLK16, $\overline{BUSY}$, $\overline{ERROR}$, $\overline{DLYWR}$, $\overline{YMEMR}$, $\overline{YMEMW}$, $\overline{YIOR}$, $\overline{YIOW}$, ADR0, $\overline{BHE}$ and $\overline{CS287}$ have internal 100k Ω (approx.) pullup resistors.

2

3.0 FE3001A REGISTERS

3.1 ERROR CONTROL REGISTER (061H), READ/WRITE

The error control register contains masks for the on-board RAM parity check and I/O channel check signals. It also provides a read port to check the status of these signals.

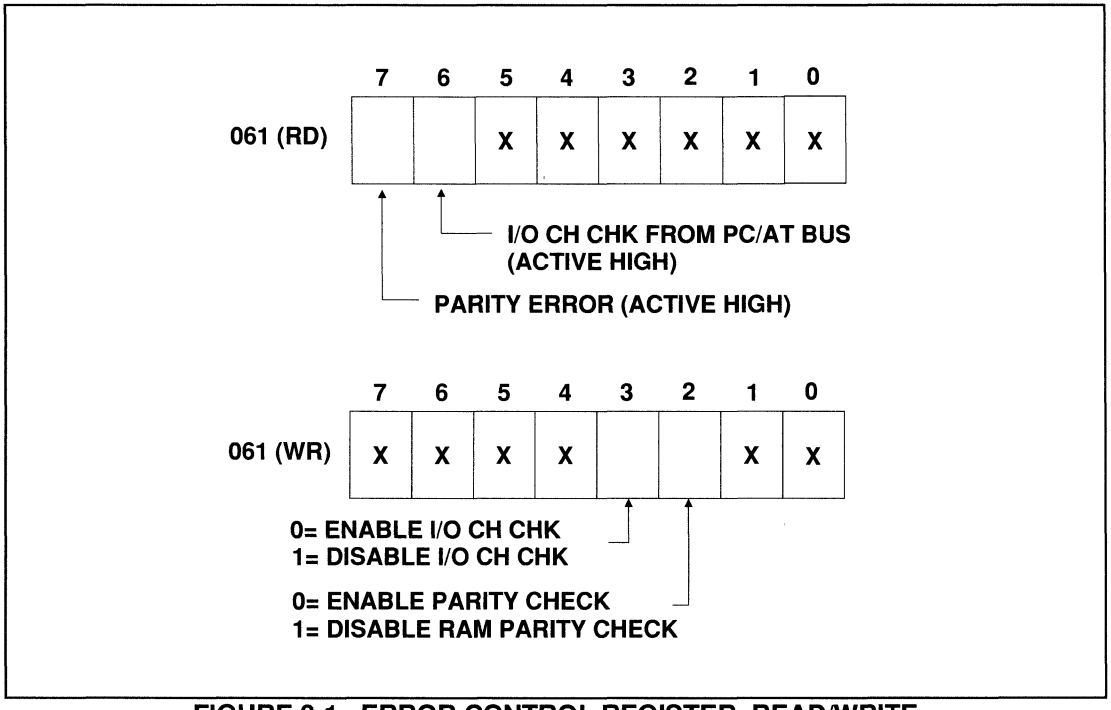


FIGURE 3-1. ERROR CONTROL REGISTER, READ/WRITE

3.2 SPEED SELECT (063H), WRITE

The speed select register controls the speed of the CPU and DMA clocks. This register is also used to stop the CPU (sleep mode) and unlock the command control and speed select registers for access. The lock bit must be reset and D7 must be low to change speed or stop clocks.

The stop clock bit stops all the clocks except for the timer clock, coprocessor clock, and keyboard controller clocks. This allows refresh to continue. Bits 2, 3, and 6 in the register are cleared and bit 7 is set by system reset.

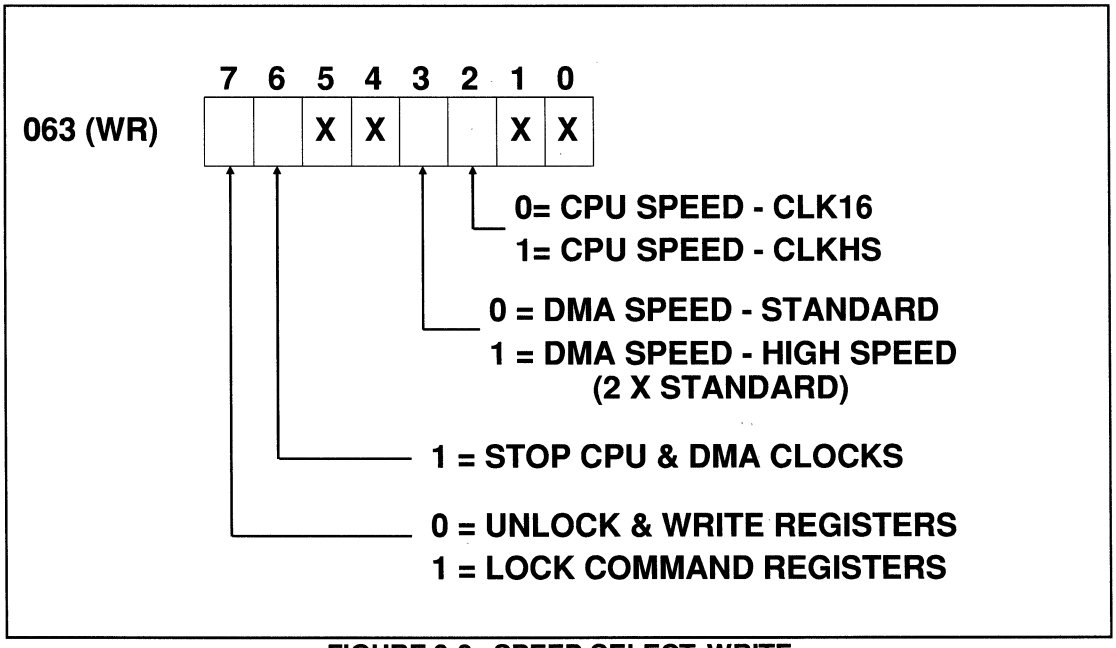


FIGURE 3-2. SPEED SELECT, WRITE

3.3 NMI ENABLE (070H), WRITE

The NMI enable register contains the mask for NMI to the 80286. Bit 7 is set on power-up.

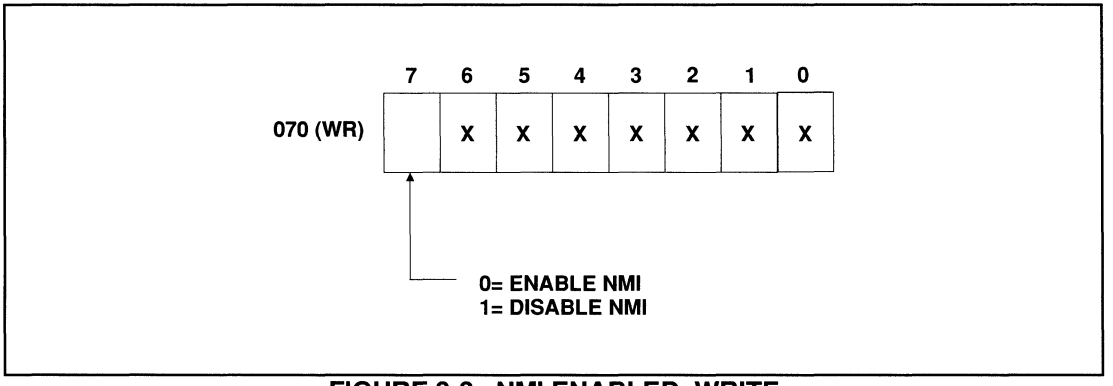


FIGURE 3-3. NMI ENABLED, WRITE

3.4 COMMAND CONTROL REGISTERS (072H,073H), WRITE

The timing of the command controls on the expansion bus is programmable via the command control registers. These registers control the timing of BALE, YMEMR, YMEMW, YIOR, YIOW, INTA and the number of wait states in a CPU cycle. This section describes the programming of these registers. Recommended program values for CPU clock speeds of 16, 25, 32 and 40 MHz are provided in Appendix A.

The programmable bus signals are shown in Figure 3-4. A summary of the timing registers is shown in Table 3-1.

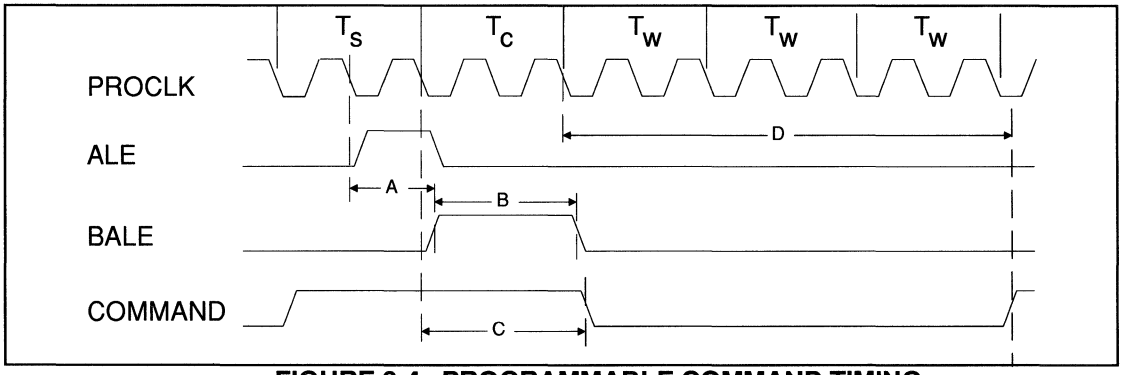


FIGURE 3-4. PROGRAMMABLE COMMAND TIMING

REG	BITS	FUNCTION	WAVEFORM	DEFAULT	RANGE
R_0	2	BALE delay from ALE leading edge	A	0	0 - 3
R1	4	BALE width	B	1	1 - 3
R_2		Not used			
R_3	4	8-bit mem., 8/16 bit I/O-command delay	C	1	0 - 15
R_4	4	8-bit operation - wait states	D	4	0 - 15
R_5	4	16-bit I/O operation - wait states	D	1	0 - 15
R_6	4	16-bit mem. - command delay	C	0	0 - 15
R_7	4	16-bit memory operation - wait states	D	1	0 - 15
R_8	4	Minimum number of wait states when ZEROWS is asserted - wait states	D	0	0 - 15
R_9	4	On-board 16-bit read cycle - wait states	D	1	0 - 15
R_{10}	4	On-board 16-bit write cycle - wait states	D	1	0 - 15
R_{11}		Not used			
R_{12}	4	On-board I/O op. - command delay	C	1	0 - 15
R_{13}	4	Enhanced Features Enable	N/A	OFF	N/A

TABLE 3-1. SUMMARY OF COMMAND TIMING REGISTERS

- Command delay is number of PROCLKs from end of T_S
- Each wait state is two PROCLKs.
- One wait state may be added in high speed mode for synchronization.

2

3.5 COMMAND REGISTER POINTER (072H)

The command register pointer points to one of 11 registers at location 073H. Each register contains a command timing parameter based on the selected CPU clock. Whichever register number is loaded in bits 7, 6, 3, and 2 in location 072H is the register which is loaded with the next write to address 073H. Refer to Table 3-5 for details.

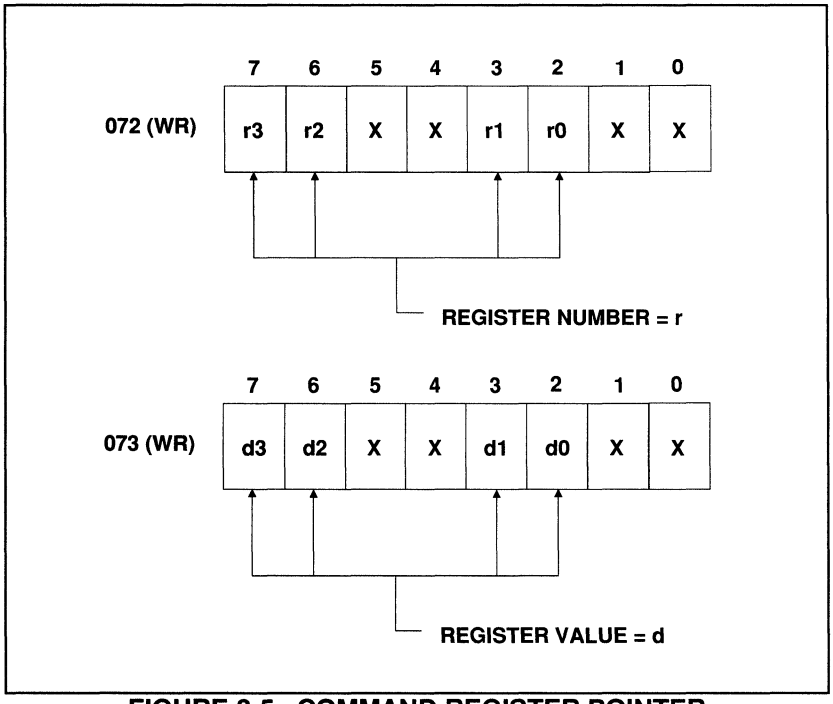


FIGURE 3-5. COMMAND REGISTER POINTER

3.6 BALE TIMING (R_0,R_1)

The leading edge and width of BALE are controlled by these two registers. BALE delay is defined as the number of PROCLK cycles from the leading edge of ALE. BALE width is the width in PROCLK cycles.

Default values: Delay (R_0) - 0
Width (R_1) - 1

3.7 8-BIT MEMORY AND 8/16 BIT (R_3)

This register controls the command delay for 8 bit memory and 8/16 bit I/O operations. Command delay is defined as the number of PROCLK cycles from the trailing edge of ALE to the start of the command.

Default value: Command Delay (R_3) - 1

3.8 8-BIT MEMORY AND I/O WAIT STATES (R_4)

This register controls the number of wait states for 8 bit operations. The number of wait states is the number of CPU wait states required for these operations.

Default value: Wait States (R_4) - 4

3.9 16-BIT I/O WAIT STATES (R_5)

This register controls the number of wait states for 16-bit I/O cycles. These cycles are indicated by the assertion of IOCS16. The number of wait states is the number of CPU wait states required for this operation.

Default values: Wait States (R_5) - 1

3.10 16-BIT AT BUS MEMORY TIMING (R_6,R_7)

These registers control the command delay and number of wait states for 16-bit memory operations. These cycles are indicated by the assertion of MEMCS16. Command delay is defined as the number of PROCLK cycles from the trailing edge of ALE. The number of wait states is the number of CPU wait states required for this operation.

Default values: Command Delay (R_6) - 0
Wait States (R_7) - 1

3.11 $\overline{\text{ZERO WS}}$ BUS CYCLE WAIT STATES

This register sets the minimum number of wait states which must occur before the assertion of the $\overline{\text{ZERO WS}}$ signal can terminate a cycle.

Default values: Wait States, $\overline{\text{ZWS}}$ (R_8) - 0

3.12 ON-BOARD MEMORY TIMING (R_9,R_{10})

These two registers control the number of wait states for on-board operations. These cycles are indicated by the assertion of $\overline{\text{ONBRD}}$ during CPU cycles. Command delay is zero for all on-board memory operations. The number of wait states is the number of CPU wait states required for this operation. There are separate registers to program the number of wait states for read and write operations to give the system designer added flexibility and potential for greater speed.

Default values: Wait States,Read (R_9) - 1
Wait States,Write (R_{10}) - 1

3.13 ON-BOARD I/O TIMING (R_{12})

This register controls the command delay for 16-bit on-board I/O operations. These cycles are indicated by the assertion of ONBRD during CPU I/O cycles. Command delay is defined as the number of PROCLK cycles from the trailing edge of ALE. The number of wait states for on-board I/O is defined by the on-board memory registers described above. Additional wait states can be added by using the IOCHRDY signal.

Default values: Command Delay (R_{12}) - 1

3.14 ENHANCED FEATURES ENABLE (R13)

Bit 2 provides one extra CPU cycle (2 CPUCLKs) data hold time for AT bus cycles at high speed. Bit 3 must be programmed to '0'. When Bit 6 is set, CS287 will be treated as ROMCS for all memory cycles. Bit 7 enables SYSCLK = PROCLK ÷ 6 and DMACLK = PROCLK ÷ 12 option at high speed.

3.15 CLEAR 80287 BUSY (0F0H), WRITE

When an error signal is received from the 80287, the BZ286 signal is latched low. The latch is cleared by an OUT instruction to this port. The output data is don't care.

3.16 RESET 80287 (0F1H), WRITE

An OUT instruction to this port generates a reset to the 80287.

4.0 PACKAGE

The FE3001 is packaged in a 84-pin PLCC.

5.0 ABSOLUTE MAXIMUMRATINGS

Ambient
Temperature (operating): . . . . . 0° to + 70° C

Storage Temperature: . . . . . -40° to +125° C

Voltage on any pin to ground: . . . - .5 V to +7 V

Power Dissipation: . . . . . 400 mW

6.0 DC CHARACTERISTICS

Refer to Table 6-1 below.

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{IL}	Input LOW Voltage		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V	
I_{OL}	LOW V Output Current[1,4]	4		mA	V_{OL}= 0.4 V
I_{OH}	HIGH V Output Current[1]	-4		mA	V_{OH}= 2.4 V
I_{OL}	LOW V Output Current[3]	20		mA	V_{OL}= 0.4 V
I_{OH}	HIGH V Output Current[2]	-8		mA	V_{OH}= 2.4 V
V_{OHC}	PROCLK Out HIGH Volt	3.8		V	I_{OH}= -2 mA
V_{DD}	Supply Voltage (Any V_{DD})	4.75	5.25	V	
I_{DD}	Supply Current (Total)			mA	
I_{OL}	Low V Output Current[2]	8		mA	V_{OL}=0.4V

TABLE 6-1. DC CHARACTERISTICS

- 1. Output currents are for DMACLK, TMRCLK, PCLK, $\overline{PCLK}$, CLK287, CPURES, ALE, RTCALE, DTR, SDTR, *DEN0*, *DEN1*, *SDEN*, SCYCLE, *READY*, DMARDY, *NPCS*, RST287, *BZ286*, *IRQ13*, NMI, HOLDRQ, *ERFSH*, HLDA1, *INTA*, *DLYWR*, *ABHE*, *BHE*, *ONBRDL*.
- 2. Output currents are for *RESET*, *YMEMR*, *YMEMW*, *YIOR*, *YIOW*, D6, D7, ADR0, SYSCLK, BALE, *EBHE*, ACK.
- 3. Output current for *REFRESH* should be 20 mA at 0.4V. This is an I/O pin which is only driven low in output mode. It is in a tri-state condition otherwise. A 300 ohm pullup resistor is needed to bring the output high.
- 4. Output low current for PROCLK.

7.0 FE3001A TIMING PARAMETERS

(T_a=0° to 70°C, V_{DD}=4.5 to 5.5V,C_L=50pf)

SYMBOL	PARAMETER	16 MHz MIN	16 MHz MAX (NS)	20 MHz MIN	20 MHz MAX
T1	ALE rising edge delay from PROCLK		18		18
T2	ALE falling edge delay from PROCLK		18		15
T3	BALE rising edge delay from PROCLK		21		21
T4	BALE falling edge delay from PROCLK		20		20
T5	$\overline{\text{YMEMR}}$, $\overline{\text{YMEMW}}$ fall delay from PROCLK		16		13
T6	$\overline{\text{YMEMR}}$, $\overline{\text{YMEMW}}$ rise delay from PROCLK		19		19
T7	$\overline{\text{YIOR}}$, $\overline{\text{YIOW}}$ falling delay from PROCLK		20		20
T8	$\overline{\text{YIOR}}$, $\overline{\text{YIOW}}$ rising delay from PROCLK		20		20
T11	$\overline{\text{READY}}$ falling edge delay from PROCLK		12		9
T12	$\overline{\text{READY}}$ rising edge delay from PROCLK		12		9
T13	DTR fall delay from PROCLK; read cycle		20		20
T16	$\overline{\text{DEN0}}$, $\overline{\text{DEN1}}$ rise delay from PROCLK; read		16		12
T17	$\overline{\text{DEN0}}$, $\overline{\text{DEN1}}$ low delay from PROCLK; write		28		28
T18	$\overline{\text{DEN0}}$, $\overline{\text{DEN1}}$ rise delay from PROCLK; write		29		29
T21	$\overline{\text{S1}}$, $\overline{\text{S0}}$ setup time to PROCLK	11		8	
T23	$\overline{\text{ONBRD}}$ setup time to PROCLK; memory cycle	22		16	
T24	$\overline{\text{ONBRD}}$ setup time to PROCLK; I/O cycle	32		24	
T25	$\overline{\text{MEMCS16}}$ setup time to PROCLK	32		32	
T26	$\overline{\text{IOCS16}}$ setup time to PROCLK	35		35	
T27	IOCHRDY setup time to PROCLK	11		7	
T28	IOCHRDY hold time from PROCLK	0		0	
T30	$\overline{\text{S1}}$, $\overline{\text{S0}}$ hold time from PROCLK	1		1	
T31	A0 setup time to PROCLK	30		30	
T32	$\overline{\text{BHE}}$ setup time to PROCLK	15		15	
T33	$\overline{\text{BHE}}$ hold time from PROCLK	15		15	

Table 7-1. FE3001A TIMING PARAMETERS

SYMBOL	PARAMETER	16 MHz MIN	16 MHz MAX (NS)	20 MHz MIN	20 MHz MAX
T34	A0 hold time from PROCLK	15		15	
T35	$\overline{ABHE}$ delay from PROCLK		28		26
T36	ADR0 delay from PROCLK		29		26
T37	$\overline{EBHE}$/EADRO delay from PROCLK		30		30
T38	$\overline{ONBRD}$ hold time from PROCLK	10		10	
T39	$\overline{ONBRDL}$ delay from $\overline{ONBRD}$		30		23
T40	$\overline{ONBRDL}$ delay from PROCLK		24		24
T41	CLK14 period	69		69	
T42	CLK14 low time	27		27	
T43	CLK14 high time	27		27	
T44	EADR0 /PCLK rise/fall delay from CLK14 falling		29		29
T45	$\overline{PCLK}$ rise/fall delay from CLK14 falling		33		33
T46	TMRCLK rise/fall delay from CLK14 falling		35		35
T47	CLKHS period	31		31	
T48	CLKHS high time	14		14	
T49	CLKHS low time	14		14	
T54	CLK287 rise/fall delay from CLKHS falling; CLK16 input tied to +5V		27		27
T55	CLK16 period	62		62	
T56	CLK16 high time	28		28	
T57	CLK16 low time	28		28	
T59	CLK287 rise/fall delay from CLK16 ; CLK16 toggling		27		27
T60	SYSCLK rise/fall delay from PROCLK; Low speed PROCLK selected		17		17
T61	SYSCLK rise/fall delay from PROCLK; High speed PROCLK selected		17		17
T62	DMACLK rise/fall delay from PROCLK; Divide by 2		37		37

Table 7-1. FE3001A TIMING PARAMETERS (Continued)

SYMBOL	PARAMETER	16 MHz MIN	16 MHz MAX(NS)	20 MHz MIN	20 MHz MAX
T63	DMACLK rise/fall delay from PROCLK; DIvide by 4		37		37
T64	DMACLK rise/fall delay from PROCLK; Divide by 8		37		37
T65	M/$\overline{IO}$ setup time to $\overline{S0}$, $\overline{S1}$ falling edge	4		4	
T66	M/$\overline{IO}$ hold time from PROCLK (end of Ts)	15		15	
T67	DTR rise delay from PROCLK; read cycle		30		30
T68	SDTR rise delay from PROCLK		28		28
T69	SDTR fall delay from PROCLK		35		35
T70	PTYERR setup time to PROCLK	11		11	
T71	PTYERR hold time from PROCLK	4		4	
T72	$\overline{MEMCS16}$ hold time from PROCLK	17		17	
T73	$\overline{DEN0}$ low delay from PROCLK; read cycle		33		33
T74	$\overline{DEN1}$ low delay from PROCLK; read cycle		33		33
T75	$\overline{ZER0WS}$ setup time to PROCLK	24		24	
T76	$\overline{ZER0WS}$ hold time from PROCLK	0		0	
T77	$\overline{DEN0}$, $\overline{DEN1}$ low delay from $\overline{ONBRD}$ high; write cycle		28		28
T78	$\overline{IOCS16}$ hold time from PROCLK	15		15	
T79	$\overline{DLYWR}$ falling edge delay from PROCLK		13	13	
T80	$\overline{DLYWR}$ rising edge delay from PROCLK		25	25	
T81	$\overline{SDEN}$ falling edge delay from PROCLK		42	42	
T82	$\overline{SDEN}$ rising edge delay from PROCLK; $\overline{YMEMR}$, $\overline{YMEMW}$, or $\overline{YIOR}$ active		47	47	
T83	$\overline{SDEN}$ rising edge delay from PROCLK; $\overline{YIOW}$ active		47	47	
T84	SCYCLE rising edge delay from PROCLK		17	17	
T85	SCYCLE falling edge delay from PROCLK		22	22	
T86	$\overline{INTA}$ falling edge delay from PROCLK		25	25	

Table 7-1. FE3001A TIMING PARAMETERS (Continued)

SYMBOL	PARAMETER	16 MHz MIN	16 MHz MAX (NS)	20 MHz MIN	20 MHz MAX
T87	$\overline{\text{INTA}}$ rising edge delay from PROCLK		25	25	
T88	ADR0 low delay from PROCLK; interrupt acknowledge cycle		21	21	
T89	$\overline{\text{DEN0}}$ low delay from PROCLK; interrupt acknowledge cycle		33	33	
T90	$\overline{\text{DEN0}}$ rise delay from PROCLK; interrupt acknowledge cycle		16	12	
T91	CPURES rising edge delay from PROCLK; shutdown cycle	5	17	5	14
T92	CPURES falling edge delay from PROCLK; shutdown cycle	5	17	5	14
T93	OUT1 to CLK14; asynchronous input	15		15	
T94	HOLDRQ rising edge delay from CLK14		46	46	
T95	HOLDRQ falling edge delay from CLK14		46	46	
T96	HLDA to CLK14; asynchronous input	26		26	
T97	$\overline{\text{REFRESH}}$ low delay from HLDA high		31	31	
T98	$\overline{\text{REFRESH}}$ output tri-state delay from CLK14		9	9	
T99	$\overline{\text{ERFSH}}$ falling edge delay from CLK14		43	43	
T100	$\overline{\text{ERFSH}}$ rising edge delay from CLK14		43	43	
T101	$\overline{\text{YMEMR}}$ falling edge delay from CLK14; refresh cycle		40	40	
T102	$\overline{\text{YMEMR}}$ rising edge delay from CLK14; refresh cycle		40		40
T103	IOCHRDY setup time to CLK14	19			
T104	HRQ1 to CLK14; asynchronous input	18			
T105	HLDA1 rising edge delay from CLK14		43		43
T106	HLDA1 high delay from HLDA high		30		30
T107	HLDA1 falling edge delay from CLK14		43		43
T108	BALE high delay from HLDA high		20		20
T109	BALE low delay from HLDA low		20		20

Table 7-1. FE3001A TIMING PARAMETERS (Continued)

SYMBOL	PARAMETER	16 MHz MIN	16 MHz MAX (NS)	20 MHz MIN	20 MHz MAX
T110	ACK high delay from HLDA high		21		21
T111	ACK high delay from $\overline{\text{MASTER}}$ high		19		19
T112	ACK low delay from HLDA low		21		21
T113	ACK low delay from $\overline{\text{MASTER}}$ low		19		19
T114	$\overline{\text{ONBRD}}$ setup before $\overline{\text{YIOR}}$ falls	9			
T115	$\overline{\text{ONBRD}}$ to $\overline{\text{ONBRDL}}$ delay; HLDA high		30		30
T116	HLDA high to ADR0 float delay		20		20
T117	HLDA low to ADR0 enable delay		20		20
T118	ADR0 input to $\overline{\text{ABHE}}$ output delay		19		19
T119	HLDA high to $\overline{\text{EBHE}}$ float delay		23		23
T120	HLDA low to $\overline{\text{EBHE}}$ enable delay		23		23
T121	AEN high to $\overline{\text{EBHE}}$ enable delay		23		23
T122	AEN low to $\overline{\text{EBHE}}$ float delay		22		22
T123	ADR0 input to $\overline{\text{EBHE}}$ output delay		28		28
T124	HLDA1 high to $\overline{\text{BHE}}$ enable delay		10		10
T125	HLDA1 low to $\overline{\text{BHE}}$ float delay		11		11
T126	$\overline{\text{EBHE}}$ to $\overline{\text{BHE}}$ delay		11		11
T127	HLDA high to $\overline{\text{YIOR}}$ float delay		21		21
T128	HLDA low to $\overline{\text{YIOR}}$ enable delay		23		23
T129	HLDA high to $\overline{\text{YMEMW}}$ float delay		21		21
T130	HLDA low to $\overline{\text{YMEMW}}$ enable delay		23		23
T131	$\overline{\text{YIOR}}$ low to $\overline{\text{DEN0}}$ low delay		25		25
T132	$\overline{\text{YIOR}}$ high to $\overline{\text{DEN0}}$ high delay		25		25
T 133	$\overline{\text{YIOR}}$ low to DTR low delay		23		23
T134	$\overline{\text{YIOR}}$ high to DTR high delay		23		23
T135	$\overline{\text{YIOR}}$ low to SDTR high delay		31		31
T136	$\overline{\text{YIOR}}$ high to SDTR low delay		31		31

Table 7-1. FE3001A TIMING PARAMETERS (Continued)

SYMBOL	PARAMETER	16 MHz MIN	16 MHz MAX (NS)	20 MHz MIN	20 MHz MAX
T137	$\overline{\text{ONBRD}}$ setup before DMACLK which causes $\overline{\text{YMEMR}}$ to go low	22		22	
T138	$\overline{\text{DMAMR}}$ setup time to DMACLK	16		16	
T139	$\overline{\text{YMEMR}}$ falling edge delay from DMACLK		15		15
T140	$\overline{\text{DMAMR}}$ high to $\overline{\text{YMEMR}}$ high delay		19		19
T141	$\overline{\text{DLYWR}}$ input low to $\overline{\text{YIOW}}$ output low		19		19
T142	$\overline{\text{DLYWR}}$ input high to $\overline{\text{YIOW}}$ output high		19		19
T143	$\overline{\text{YMEMR}}$ low to $\overline{\text{DEN1}}$ low delay		25		25
T144	$\overline{\text{YMEMR}}$ high to $\overline{\text{DEN1}}$ high delay		25		25
T145	$\overline{\text{YMEMR}}$ low to $\overline{\text{SDEN}}$ low delay		30		30
T146	$\overline{\text{YMEMR}}$ high to $\overline{\text{SDEN}}$ high delay		30		30
T147	AEN high to ADR0 enable delay; DACK2 high		25		25
T148	DACK2 low to ADR0 float delay		20		20
T149	AEN high to $\overline{\text{ABHE}}$ low delay; DACK2 high		27		27
T150	IOCHRDY setup time before DMACLK	15		15	
T151	$\overline{\text{YIOR}}$ low to DMARDY low delay		27		27
T152	$\overline{\text{DMAMR}}$ low to DMARDY low delay		27		27
T153	DMARDY rising edge delay from DMACLK		25		25
T156	$\overline{\text{EBHE}}$ to $\overline{\text{ABHE}}$ delay; master mode		22		22
T157	AEN low to ADR0 float delay; master mode		23		23
T158	AEN high to $\overline{\text{DLYWR}}$ float delay		20		20
T159	AEN low to $\overline{\text{DLYWR}}$ enable delay		21		21
T160	$\overline{\text{ONBRD}}$ setup time before memory command falls; master mode	18		18	
T161	ADR0 setup time before memory command falls; master mode	6		6	
T162	$\overline{\text{EBHE}}$ setup time before memory command falls; master mode	6		6	

Table 7-1. FE3001A TIMING PARAMETERS (Continued)

SYMBOL	PARAMETER	16 MHz MIN	16 MHz MAX (NS)	20 MHz MIN	20 MHz MAX
T163	DTR low delay from memory command low; master mode		23		23
T164	DTR high delay from memory command high; master mode		23		23
T165	$\overline{\text{DEN0}}$ low delay from memory command low; master mode		25		25
T166	$\overline{\text{DEN0}}$ high delay from memory command high; master mode		25		25
167	$\overline{\text{DEN1}}$ low delay from memory command low; master mode		25		25
T168	$\overline{\text{DEN1}}$ high delay from memory command high; master mode		25		25
T169	$\overline{\text{MEMCS16}}$ setup time before memory command falls; master mode, ADR0 high	10		10	
T170	SDTR low delay from memory command low; master mode, ADR0 high		31		31
T171	SDTR high delay from memory command high; master mode, ADR0 high		31		31
T172	$\overline{\text{SDEN}}$ low delay from memory command low; master mode, ADR0 high		30		30
T173	$\overline{\text{SDEN}}$ high delay from memory command high; master mode, ADR0 high		30		30
T174	ADR0 setup time before I/O command falls; master mode	5		5	
T175	SDTR low delay from I/O command low; master mode, ADR0 high		31		31
T176	SDTR high delay from I/O command high; master mode, ADR0 high		31		31
T177	$\overline{\text{SDEN}}$ low delay from I/O command low; master mode, ADR0 high		30		30
T178	$\overline{\text{SDEN}}$ high delay from I/O command high; master mode, ADR0 high		30		30
T179	$\overline{\text{IOCS16}}$ setup time before I/O command falls; master mode, ADR0 high	14		14	

Table 7-1. FE3001A TIMING PARAMETERS (Continued)

NOTES:

All delays with respect to PROCLK are with respect to the falling edge of PROCLK.

T22: $\overline{\text{ZEROWS}}$ SETUP TIME NOTES

The $\overline{\text{ZEROWS}}$ signal is sampled by the FE3001A in the middle of every CPU wait state during AT bus cycles. $\overline{\text{ZEROWS}}$ will terminate an AT bus cycle early when it is sampled after the minimum number of wait states programmed into R8 have occurred.

T25: $\overline{\text{MEMCS16}}$ SETUP TIME NOTES

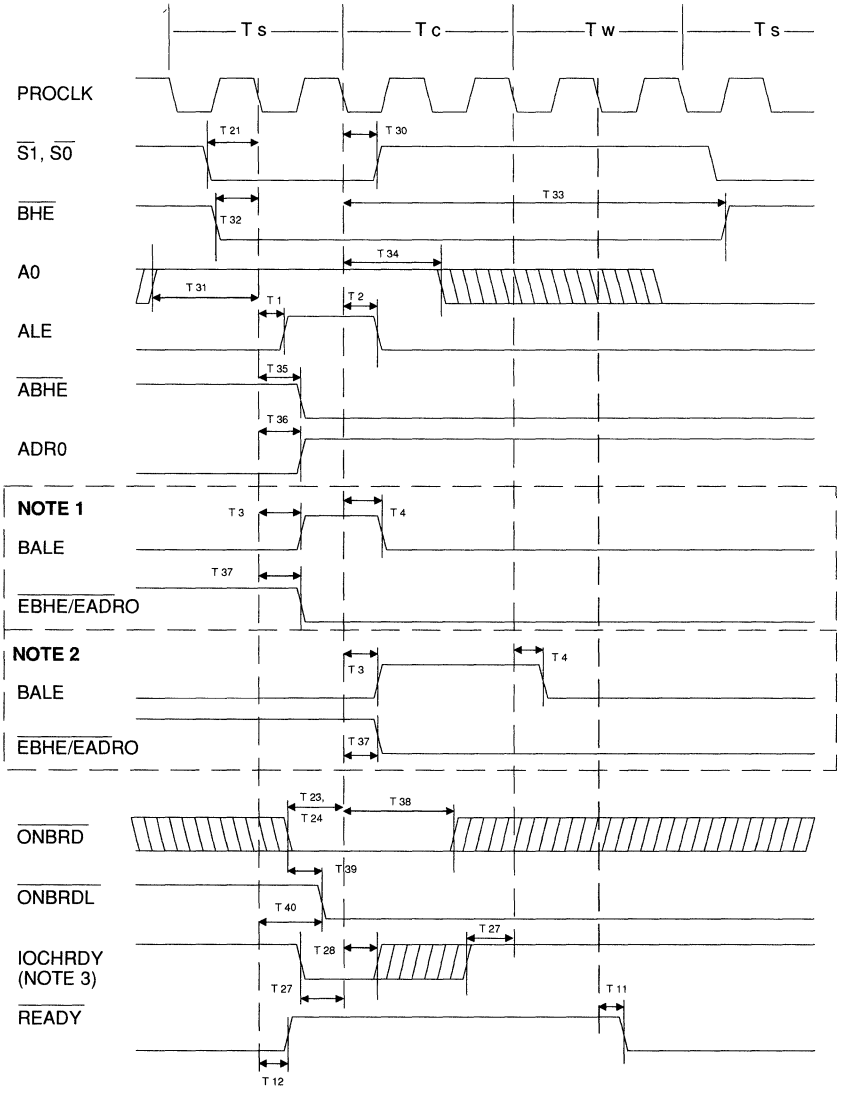
$\overline{\text{MEMCS16}}$ is only examined during AT bus memory cycles. It must be valid before the earlier of either (1) the memory command strobe falls as programmed by R6, or (2) BALE falls as programmed by R0 and R1.

T26: $\overline{\text{IOCS16}}$ SETUP TIME NOTES

IOCS16 is only examined during AT bus I/O cycles. It must be valid before the I/O command falls as programmed by R3.

T27: IOCHRDY SETUP TIME NOTES

IOCHRDY is sampled with the falling edge of PROCLK at the end of each CPU "t" state. It must be sampled low one full "t" state before a cycle would normally end in order to extend it.



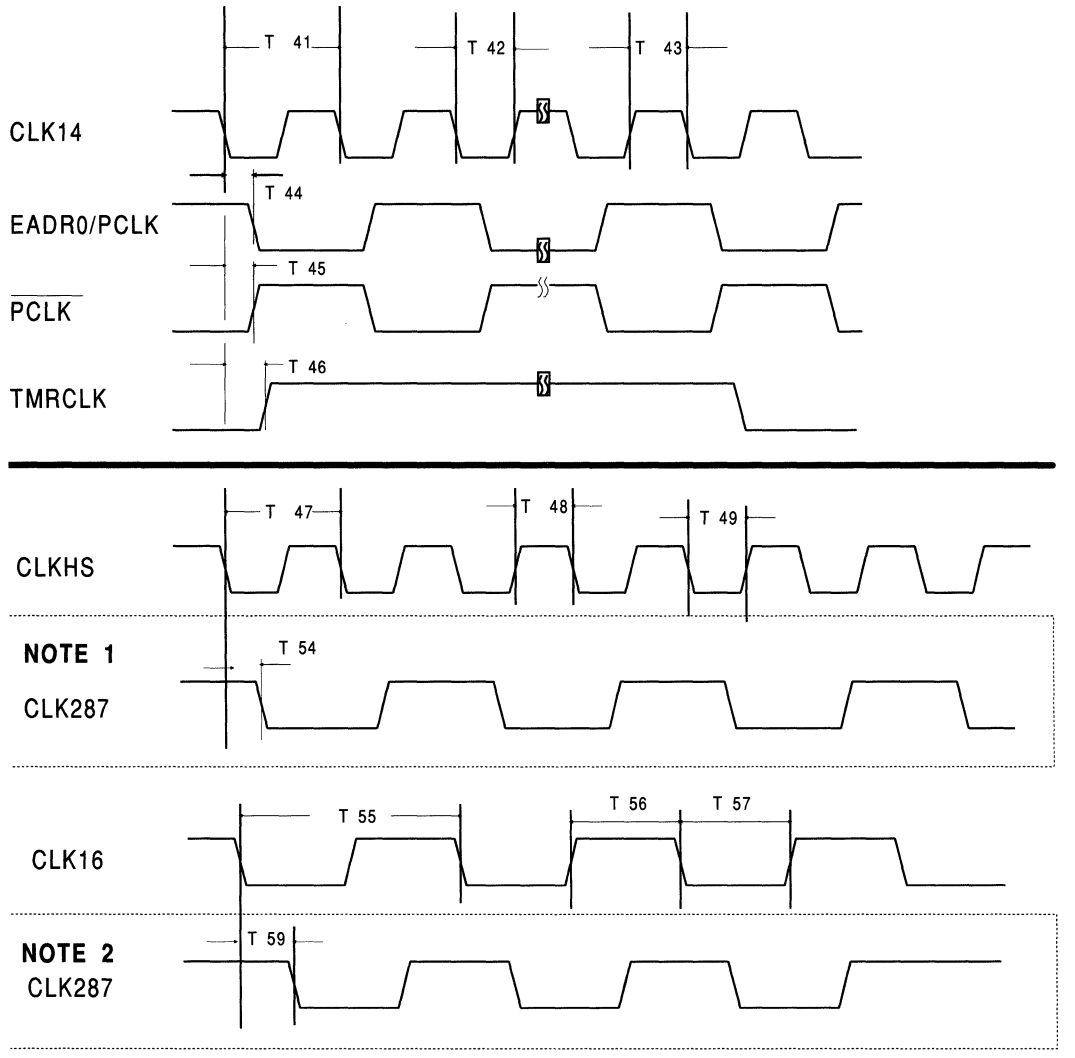
NOTES:

(1) R0 = 0; R1 = 1 (low speed BALE timing)

(2) R0 = 1; R1 = 2 (16MHz BALE timing)

(3) IOCHRDY is being used to add one wait state to this on-board cycle, which is otherwise programmed by R9 or R10 to be 0 wait states

Figure 7-1. CPU Cycle Timing for ALE, Byte Select, ONBRD and READY

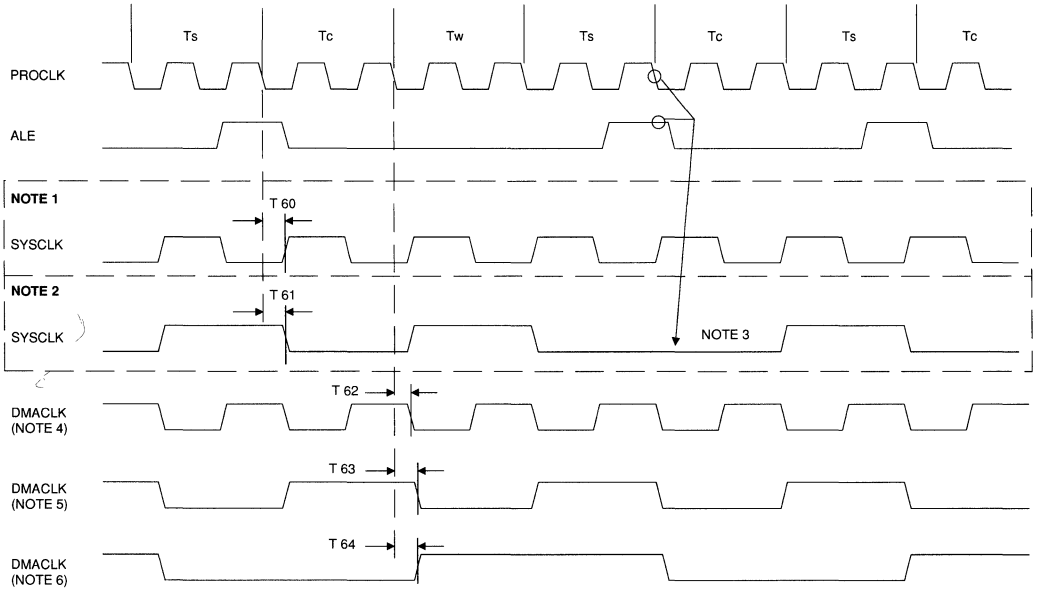


NOTES:

(1) CLK16 input connected to +5V

(2) CLK16 input driven by an oscillator

Figure 7-2. Clock Timing (1 of 2)



NOTES:

(1) Bit 2 of I/O Addr 63 set to 0 (low speed CPU clock)

(2) Bit 2 of I/O Addr 63 set to 1 (high speed CPU clock)

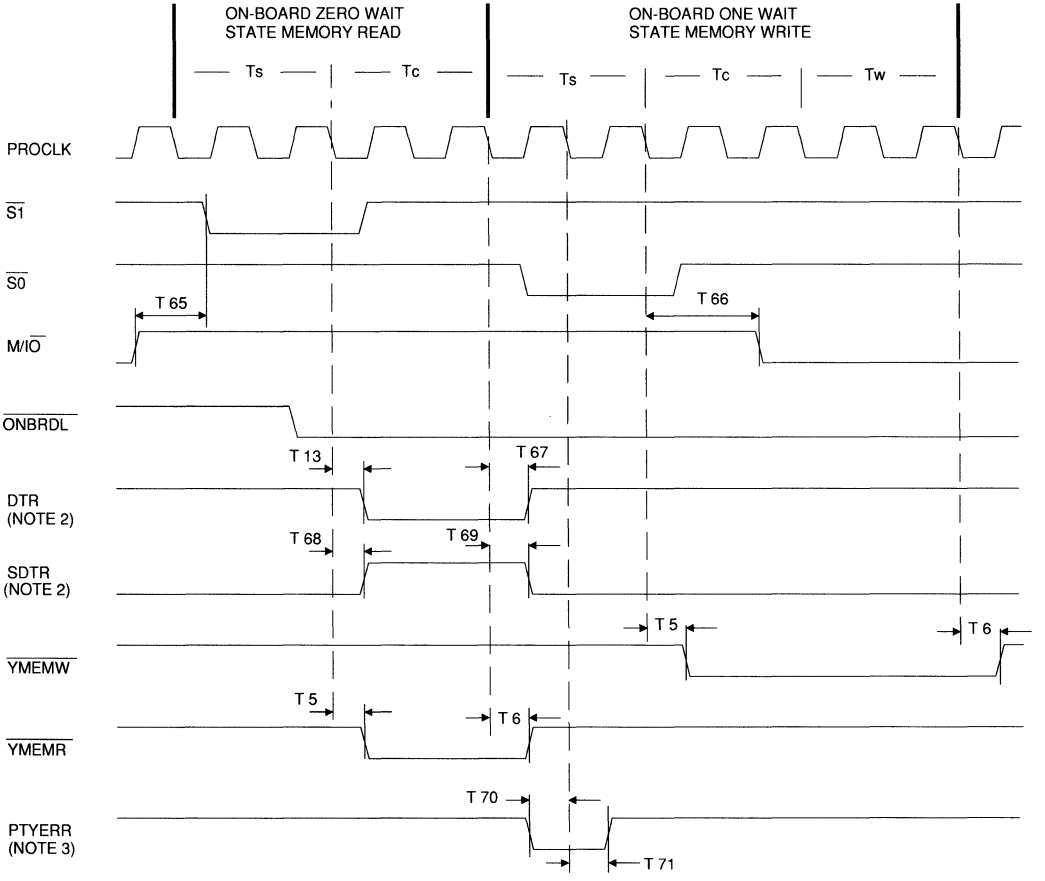
(3) SYSCLK low time extended when SYSCLK is low while ALE is high and the high speed CPU clock has been selected

(4) Bit 2 of I/O Addr 63 set to 0 (low speed CPU clock) and Bit 3 set to 1 (high speed DMA)

(5) I/O Addr 63 Bits 2 and 3 set to the same value; low speed CPU clock and low speed DMA, or high speed CPU clock and high speed DMA

(6) Bit 2 of I/O Addr 63 set to 1 (high speed CPU clock) and Bit 3 set to 0 (low speed DMA)

Figure 7-3. CLOCK TIMING (2 of 2)



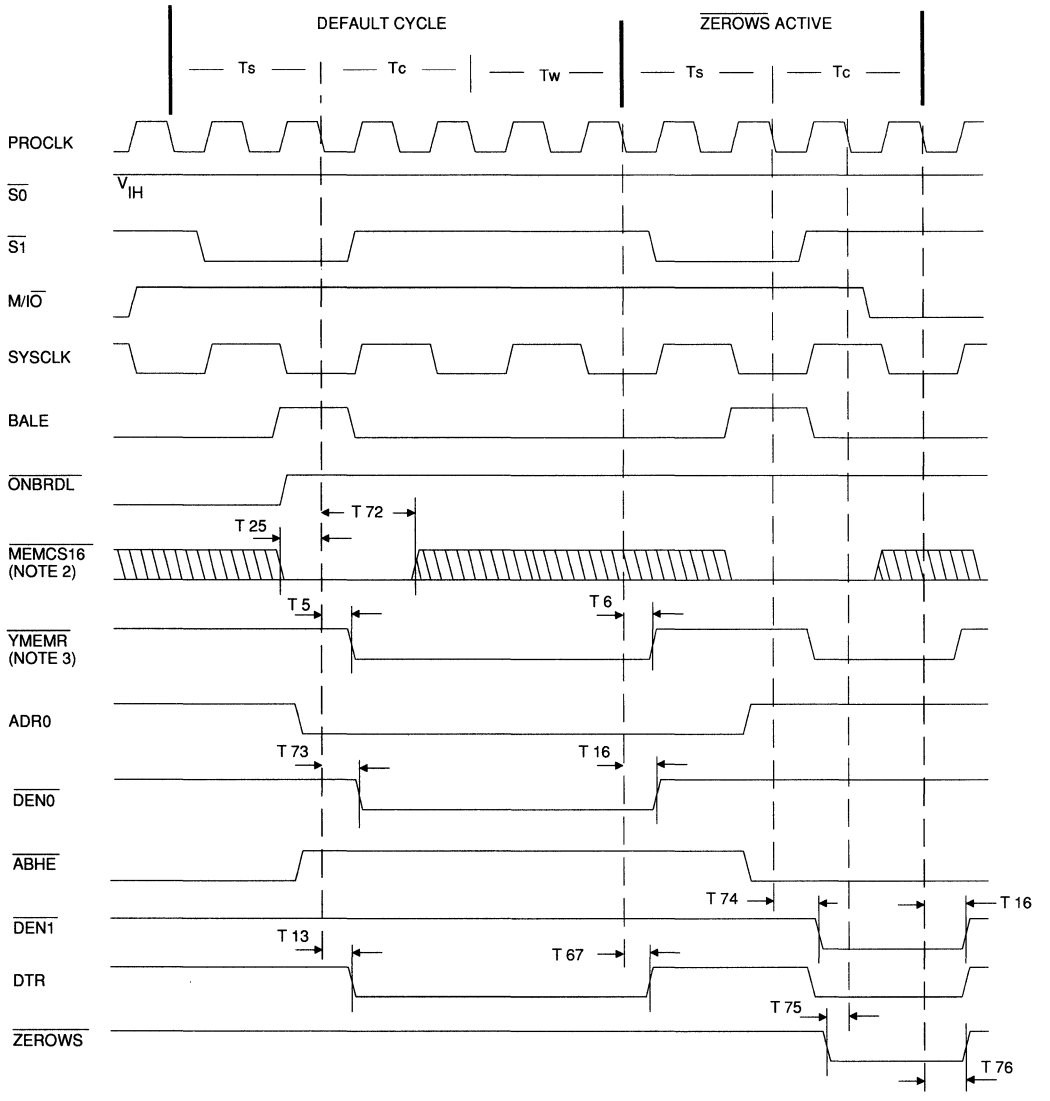
NOTES:

(1) $\overline{DEN0}$, $\overline{DEN1}$, and $\overline{SDEN}$ will remain high and SYSCLE will remain low during on-board memory cycles

(2) NOT USED by the FE3031 during on-board memory cycles; shown for reference only

(3) PTYERR must be low when shown to prevent a parity NMI from being generated (if enabled)
PTYERR is sampled one PROCLK ***after*** the end of an on-board memory read

Figure 7-4. On-board Memory Cycle Timing



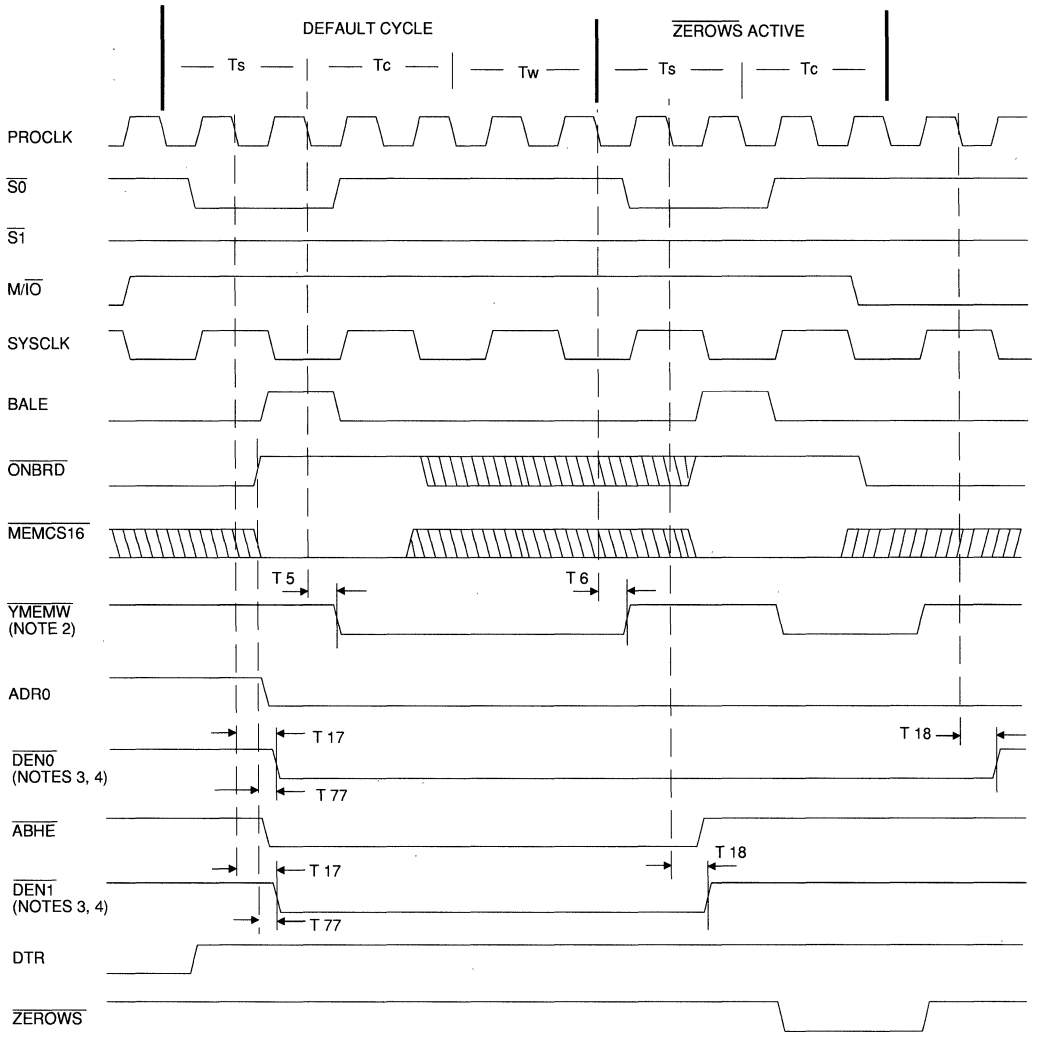
NOTES:

(1) NPCS is high during these cycles

(2) Setup/Hold times referenced to PROCLK edge which is programmed by R6 to cause YMEMR or YMEMW to go low

(3) R6 = 0; R7 = 1; R8 = 0; R0 = 0; R1 = 1

Figure 7-5. 16-Bit Memory Read Timing-Low Speed CPU Clock



NOTES:

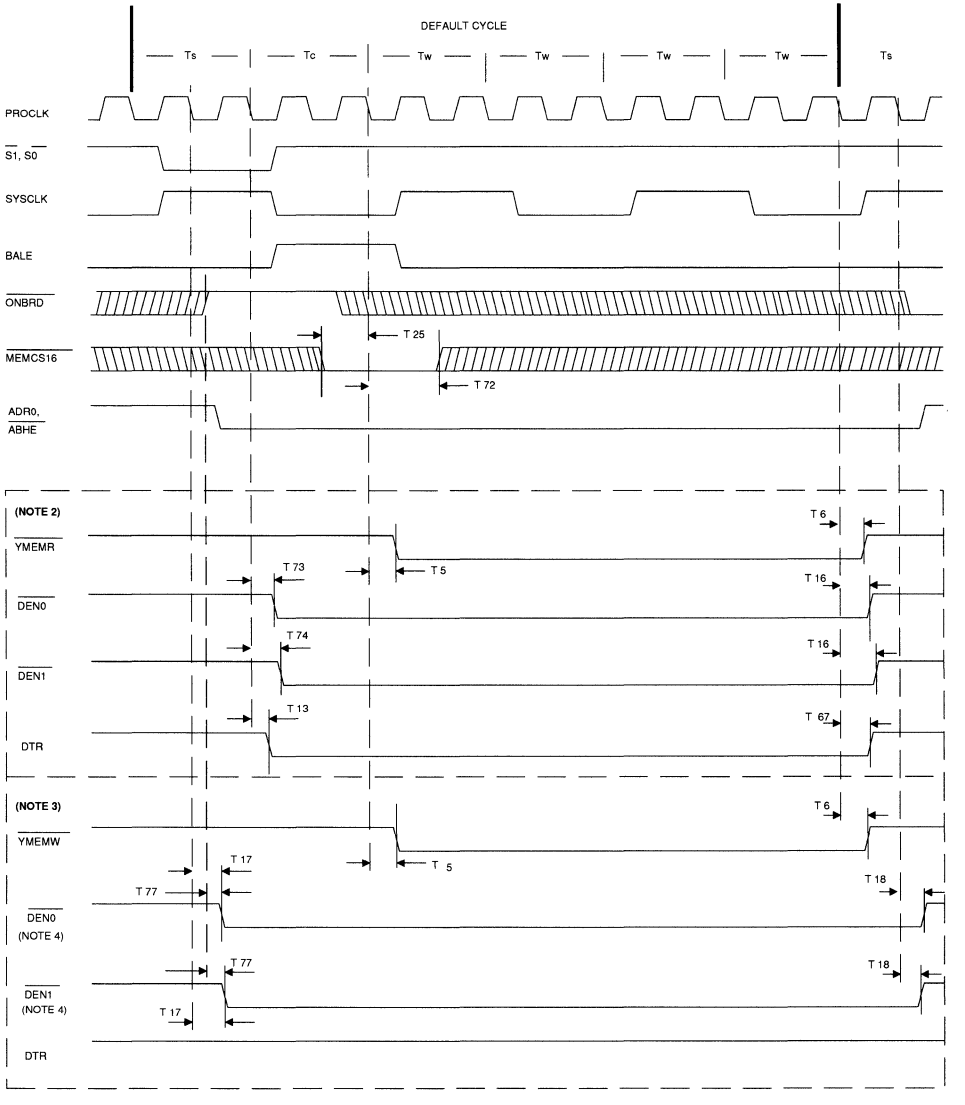
(1) $\overline{\text{NPCS}}$ is high during these cycles

(2) R6 = 0; R7 = 1; R8 = 0; R0 = 0; R1 = 1

(3) $\overline{\text{DEN0}}$ and $\overline{\text{DEN1}}$ go high one PROCLK cycle after the write command goes high. However, each will remain low for back to back write cycles when it is active in both cycles

(4) The falling edge of $\overline{\text{DEN0}}$ or $\overline{\text{DEN1}}$ in a write cycle will be controlled by $\overline{\text{ONBRD}}$ if it goes high in the last half of the processor Ts state, or by PROCLK if $\overline{\text{ONBRD}}$ is high earlier

Figure 7-6. 16-Bit Memory Write Timing-Low Speed CPU Clock



NOTES:

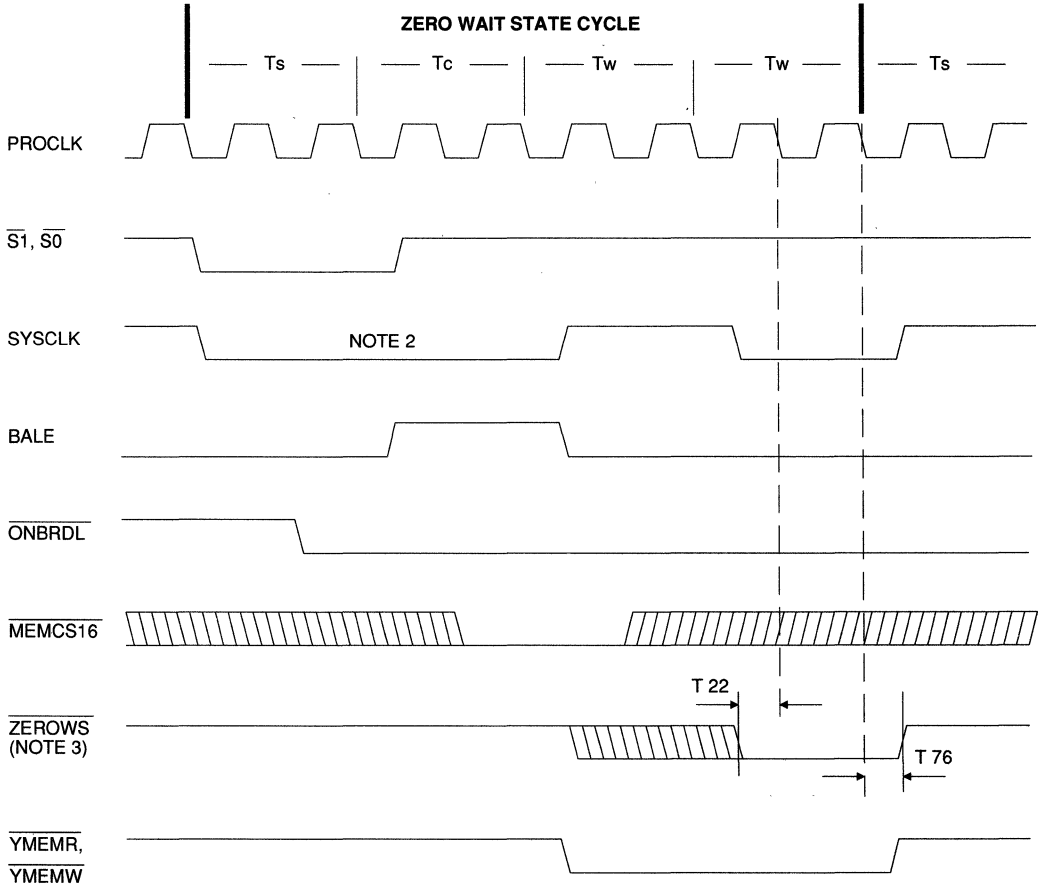
(1) R0 = 1; R1 = 2; R6 = 2; R7 = 4; $\overline{\text{NPCS}}$ is high during these cycles

(2) Memory read cycle timing

(3) Memory write cycle timing

(4) The falling edge of $\overline{\text{DEN0}}$ or $\overline{\text{DEN1}}$ in a write cycle will be controlled by $\overline{\text{ONBRD}}$ if it goes high in the last half of the processor Ts state, or by PROCLK if $\overline{\text{ONBRD}}$ goes high earlier

Figure 7-7. 16-Bit Memory Timing for High Speed(16 MHz) CPU



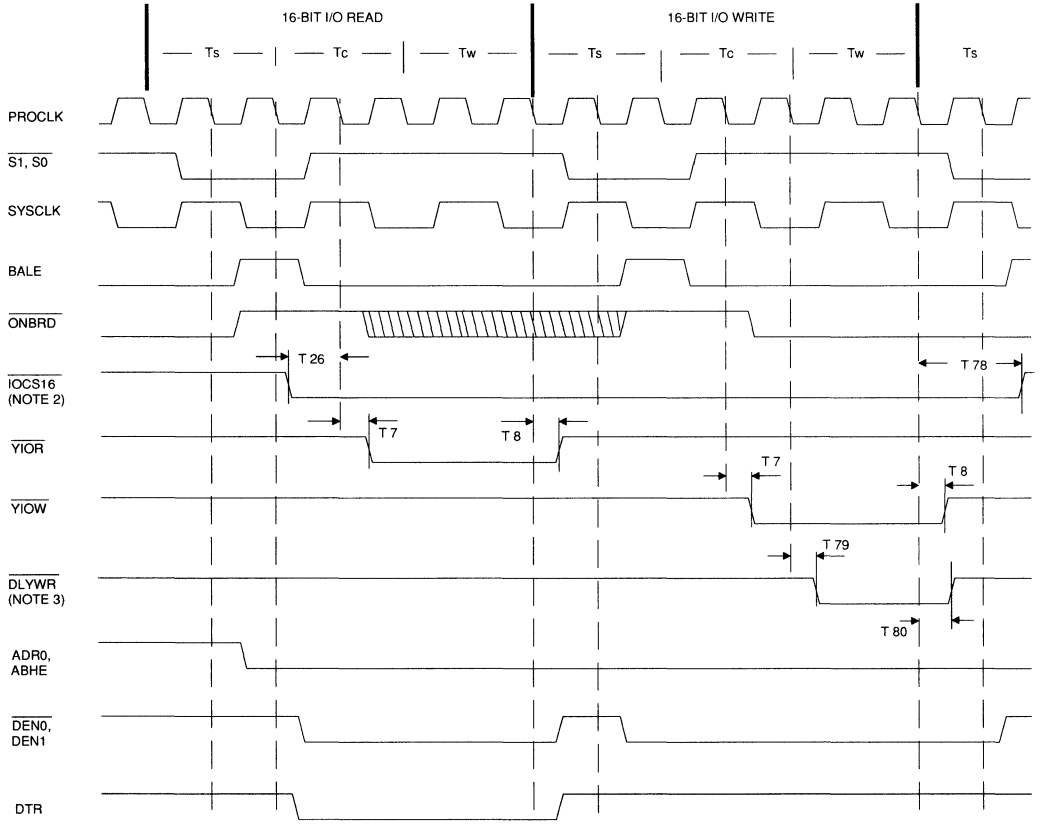
NOTES:

(1) R0 = 1; R1 = 2; R6 = 2; NPCS is high during these cycles

(2) SYSCLK is extended low one extra half period when it is low during the processor's Ts state and the high speed CPU clock is selected

(3) Register R8 = 2. When the high speed CPU clock is selected, no AT bus cycle can terminate until the cycle when SYSCLK goes high. This ensures proper synchronization of the rising edge of the command strobes with SYSCLK

Figure 7-8. 16-Bit Memory Timing with ZEROWS Asserted and High Speed (16 MHz) CPU



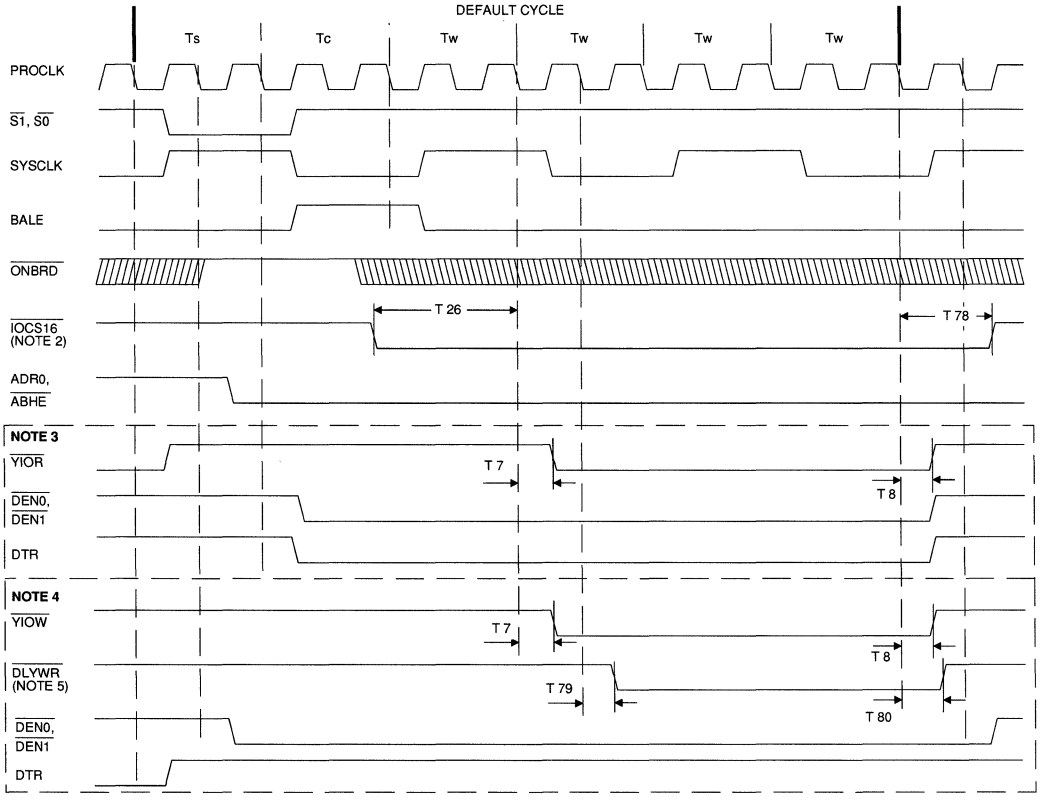
NOTES:

(1) R0 = 0; R1 = 1; R3 = 1; R5 = 1

(2) $\overline{\text{IOCS16}}$ setup time is to the PROCLK which causes $\overline{\text{YIOR}}$ or $\overline{\text{YIOW}}$ to go low as programmed by R3. Hold time is from the end of the cycle

(3) $\overline{\text{DLYWR}}$ falling edge is one PROCLK later than $\overline{\text{YIOW}}$ at low speed. $\overline{\text{DLYWR}}$ rising edge is coincident with $\overline{\text{YIOW}}$ rising edge

Figure 7-9. 16-Bit I/O Timing with Low Speed CPU Clock



NOTES:

(1) R0 = 1; R1 = 2; R3 = 4; R5 = 4. NPCS is high during these cycles

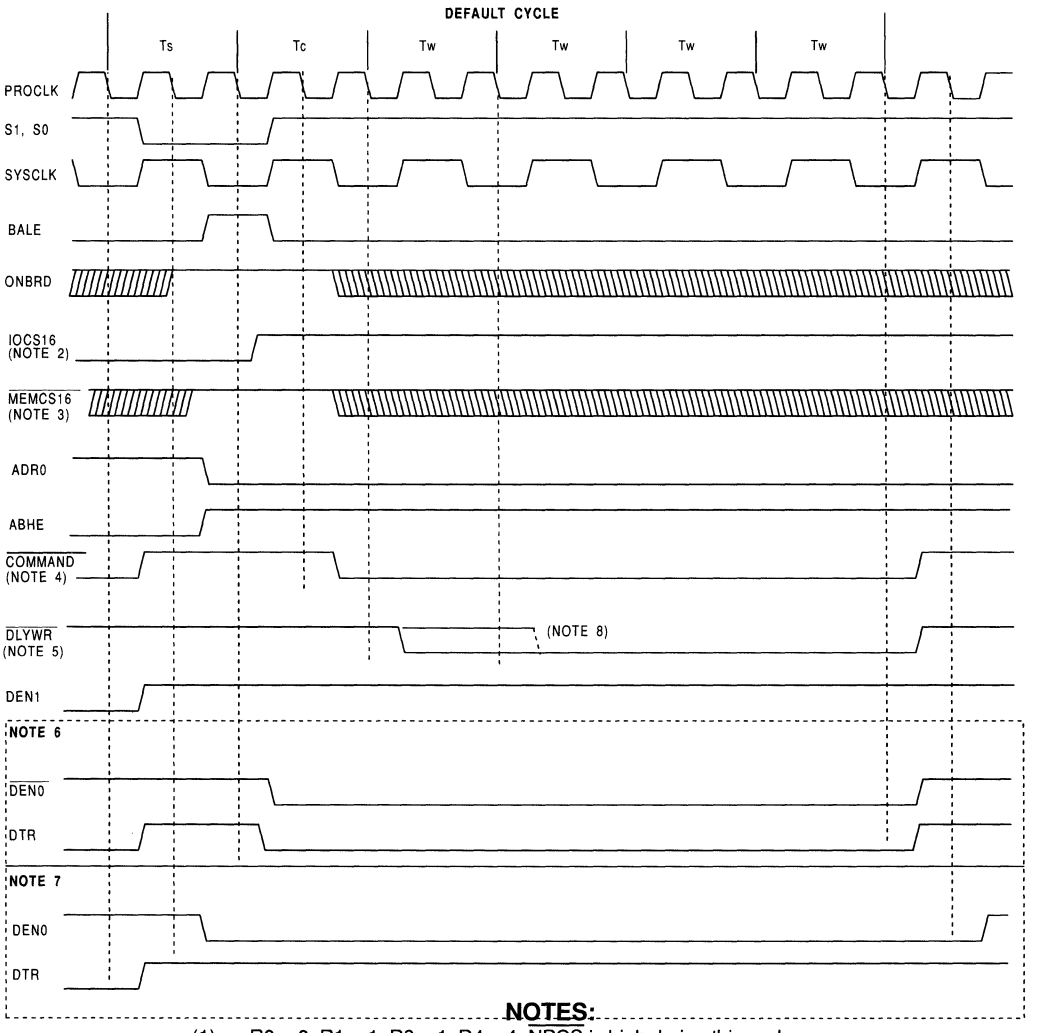
(2) IOCS16 setup time is referenced to the PROCLK which causes IOR or IOW to go low as programmed by R3. Hold time is from the cycle end

(3) I/O read cycle timing

(4) I/O write cycle timing

(5) DLYWR falling edge is one PROCLK later than IOW at low speed. DLYWR rising edge is coincident with IOW rising edge

Figure 7-10. 16-Bit I/O Timing w/High Speed (16 MHz) CPU Clk



NOTES:

(1) R0 = 0; R1 = 1; R3 = 1; R4 = 4. NPCS is high during this cycle

(2) IOCS16 affects only I/O cycles

(3) MEMCS16 affects only memory cycles

(4) COMMAND means either YIOR, YIOW, YMEMR, or YMEMW

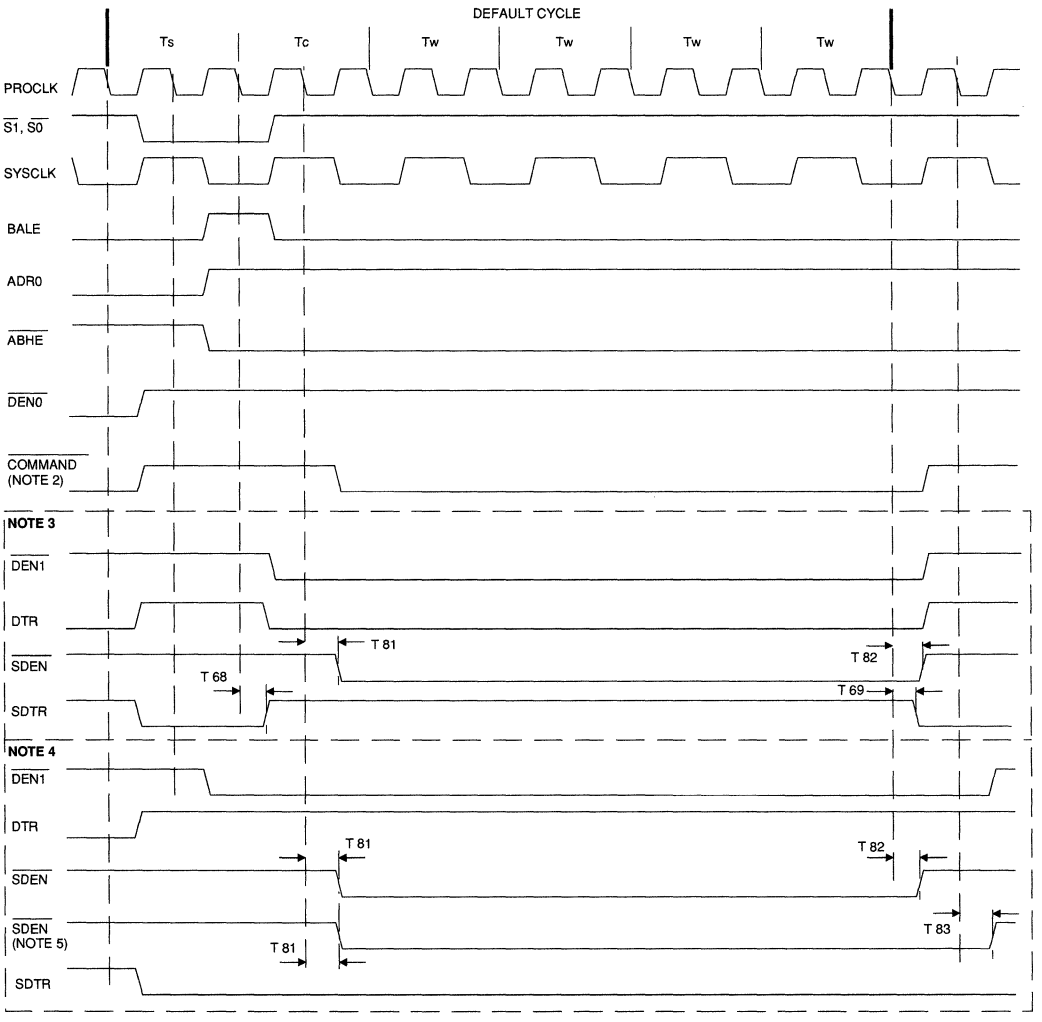
(5) DLYWR is active only in cycles where YIOW is active

(6) Read cycle timing

(7) Write cycle timing

(8) DLYWR will be further delayed by 2 PROCLK at high speed

Figure 7-11. 8-Bit Cycle Timing for Low Speed CPU Clock -- Even Byte Access



NOTES:

(1) R0 = 0; R1 = 1; R3 = 1; R4 = 4. NPCS and ONBRD are inactive. IOCS16 is inactive during I/O cycles. MEMCS16 is inactive during memory cycles

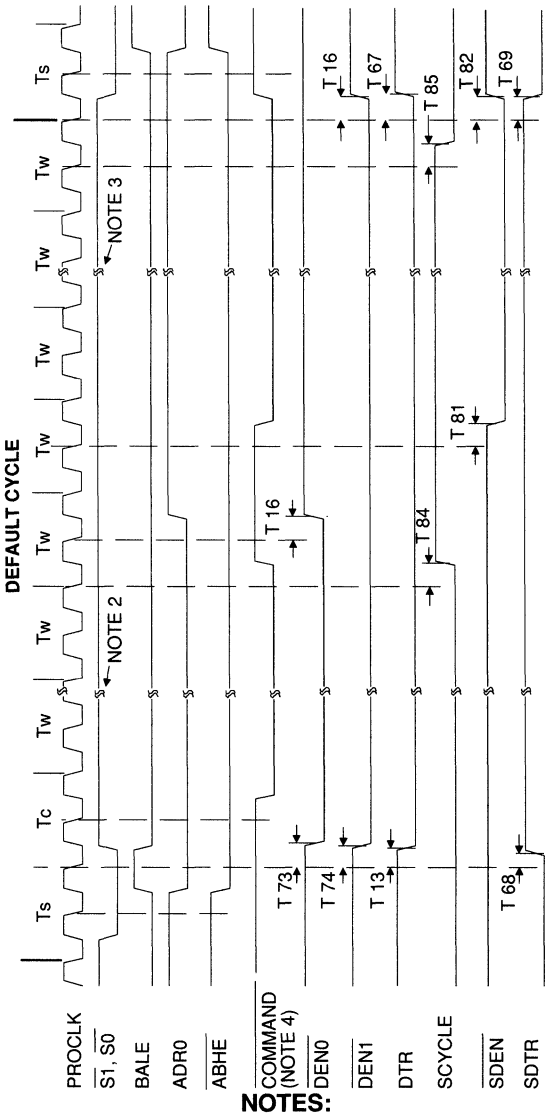
(2) COMMAND means either YIOR, YIOW, YMEMR, or YMEMW

(3) Read cycle timing

(4) Write cycle timing

(5) SDEN stays low one additional PROCLK during cycles when YIOW is active

Figure 7-12. 8-Bit Cycle Timing for Low Speed CPU Clock - - Byte Access



NOTES:

(1) R0 = 0; R1 = 1; R3 = 1; R4 = 4. $\overline{\text{NPCS}}$ and $\overline{\text{ONBRD}}$ are inactive. $\overline{\text{IOCS16}}$ is inactive during I/O cycles. $\overline{\text{MEMCS16}}$ is inactive during memory cycles

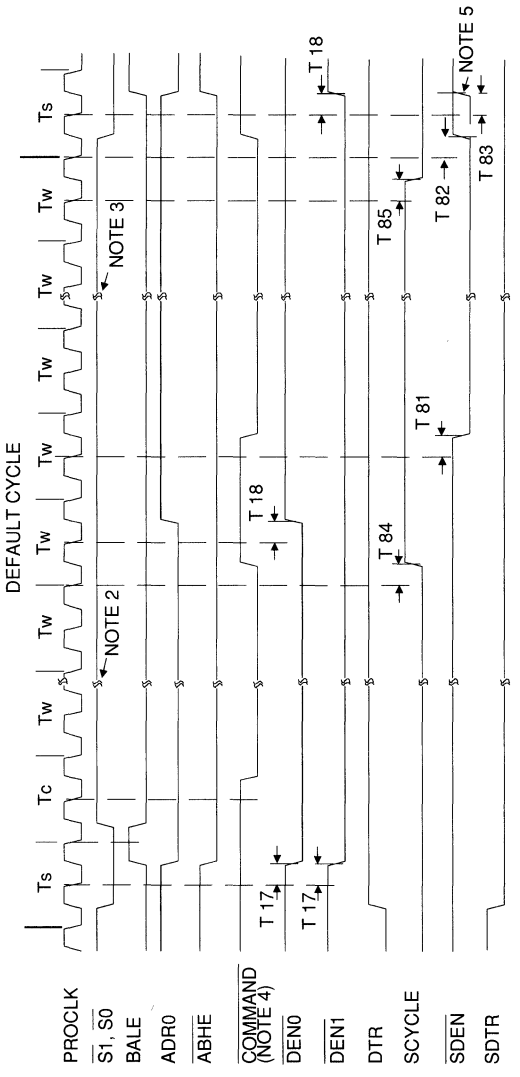
(2) Two additional wait states are not shown

(3) One additional wait state is not shown

(4) $\overline{\text{COMMAND}}$ means either $\overline{\text{YIOR}}$ or $\overline{\text{YMEMR}}$

Figure 7-13. 8-Bit Cycle Timing for Low Speed CPU Clock - -

Word Read from Even Address



NOTES:

(1) R0 = 0; R1 = 1; R3 = 1; R4 = 4. NPCS and ONBRD are inactive. IOCS16 is inactive during I/O cycles. MEMCS16 is inactive during memory cycles

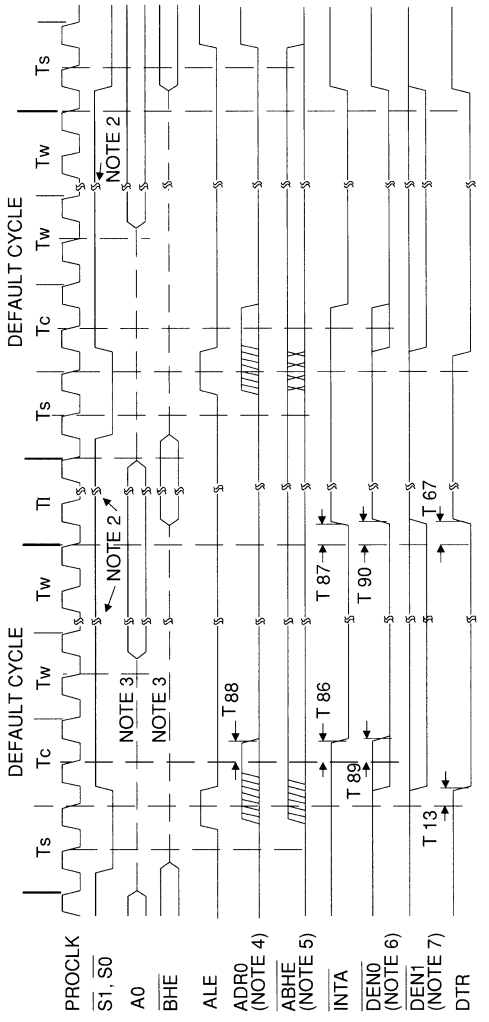
(2) Two additional wait states are not shown

(3) One additional wait state is not shown

(4) COMMAND means either IOW or MEMW

(5) SDEN low time extended one PROCLK for I/O write cycles

Figure 7-14. 8-Bit Cycle Timing for Low Speed CPU Clock -- Word Write to Even Address



NOTES:

(1) R3 = 1; R4 = 4

(2) Two additional processor T states not shown

(3) 80286 floats these lines during interrupt acknowledge cycles

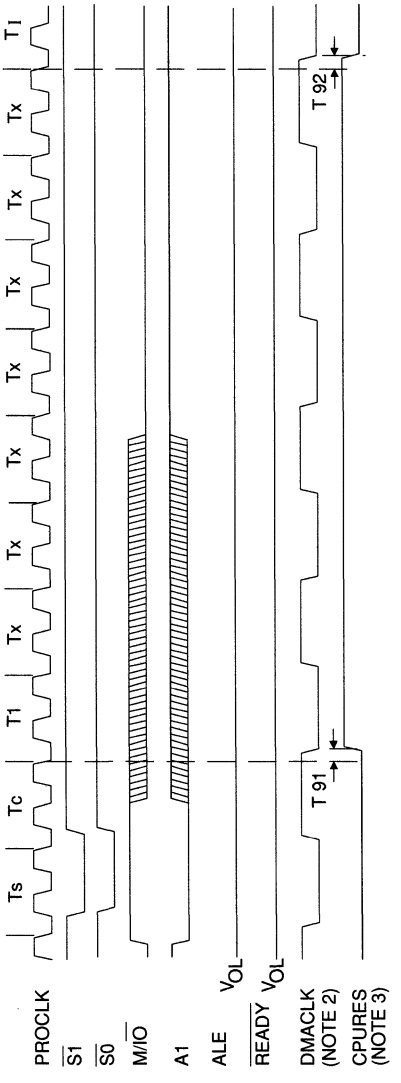
(4) Because A0 is floating, the state of ADR0 is unknown from the rising edge of ALE until INTA falls, when ADR0 is forced low

(5) Because BHE is floating, the state of ABHE (and EBHE) is unknown

(6) DEN0 is forced low when INTA falls. It could have gone low at the end of Ts depending on the state of ADR0

(7) The state of DEN1 follows ABHE and therefore cannot be determined

Figure 7-15. Interrupt Acknowledge Cycle-Low Speed CPU Clock



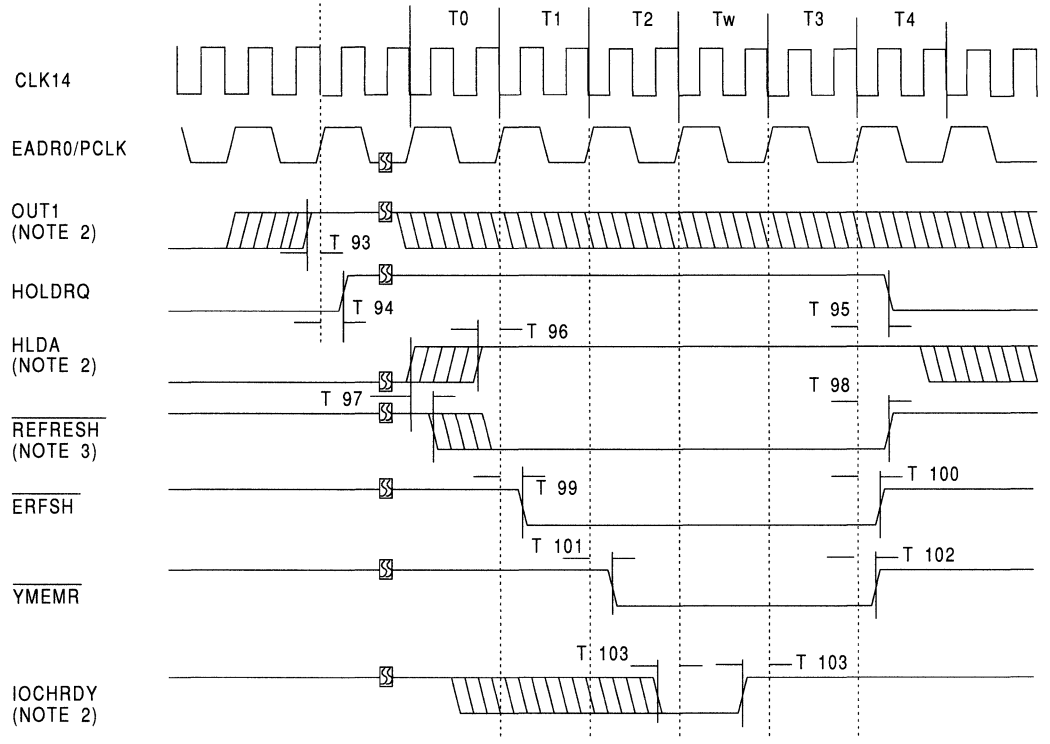
NOTES:

(1) The width of CPURES will be four DMACLK periods

(2) DMACLK is shown as it would be for high speed DMA and a high speed CPU clock or for low speed DMA and a low speed CPU clock. Refer to Figure 8. Note that the phase of DMACLK with respect to Ts is uncertain.

(3) CPURES will be asserted on the first PROCLK edge which begins a T state, after an internal divide by 4 of DMACLK makes a low to high transition. The phase of this internal signal is impossible to determine, although it changes on the rising edge of DMACLK. CPURES is shown going active here as early as possible. It could be delayed up to three more DMACLK periods

Figure 7-16. Shutdown Cycle Timing



NOTES:

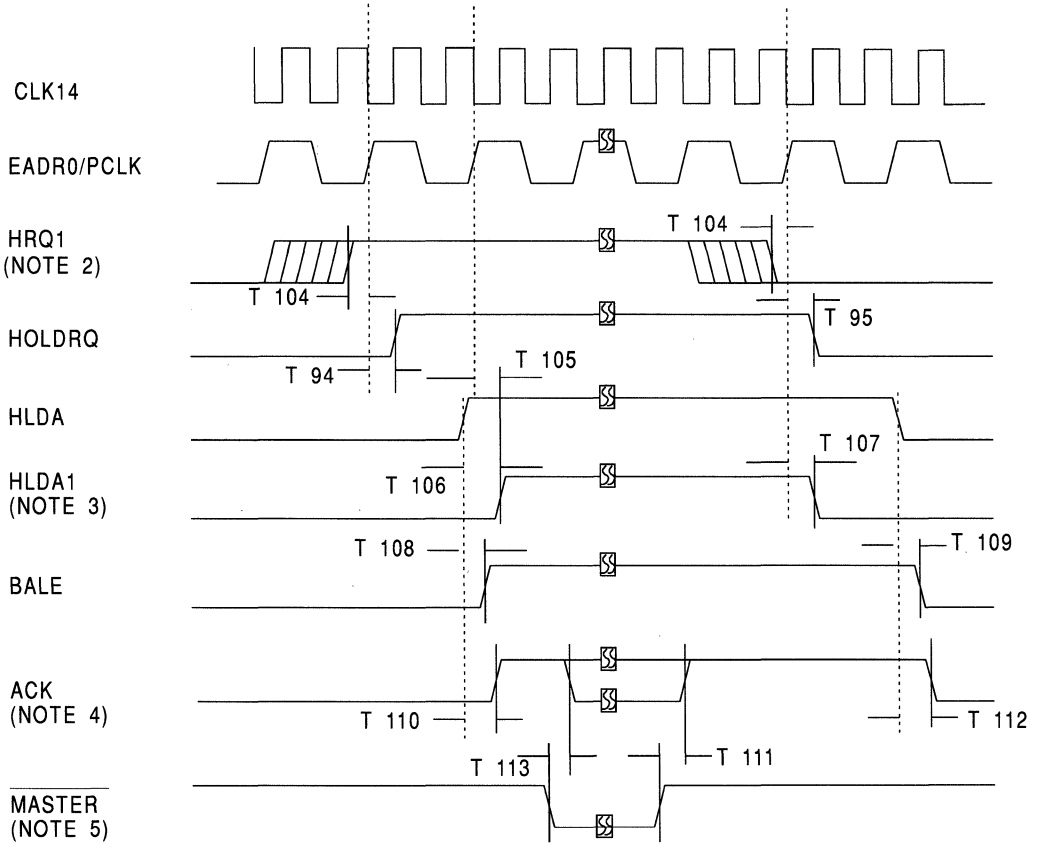
(1) Cycle shown with one wait state (one EADR0/PCLK period) inserted

(2) OUT1, HLDA , and IOCHRDY are asynchronous inputs. Setup times are shown only to guarantee recognition at a particular edge of EADR0/PCLK

(3) The falling edge of $\overline{\text{REFRESH}}$ is combinatorially generated from HLDA. The rising edge is controlled by the FE3001A

(4) HRQ1 and HLDA1 are not active

Figure 7-17. Refresh Cycle Timing



NOTES:

(1) No refresh cycle is pending

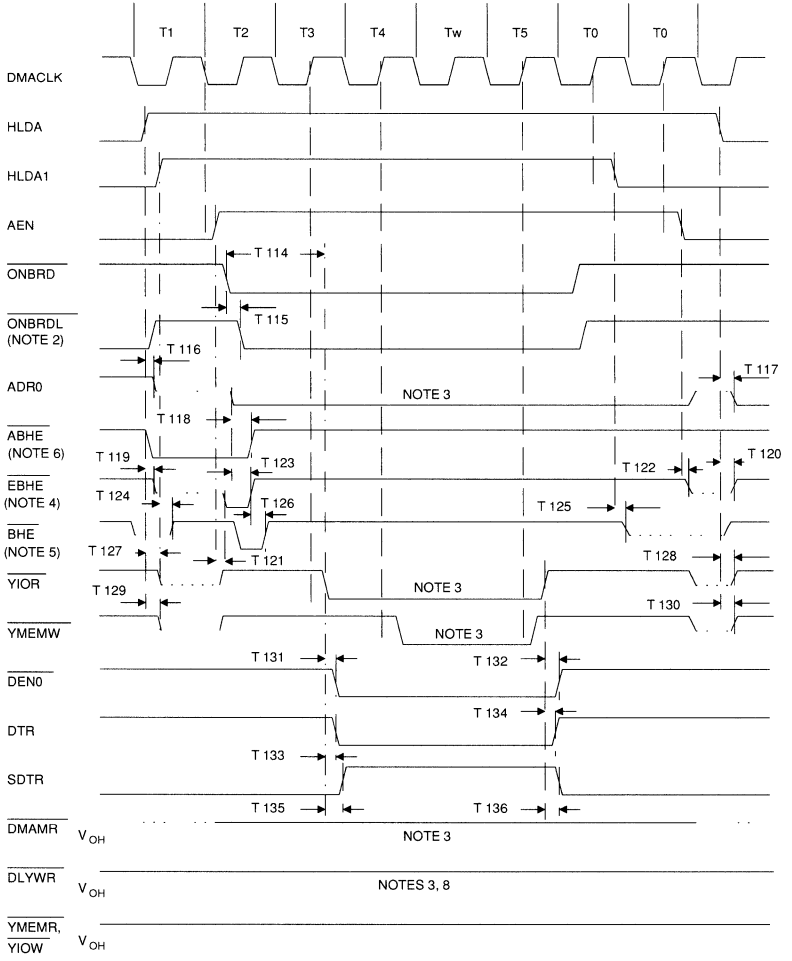
(2) HRQ1 is an asynchronous input. Setup time is shown only to guarantee recognition at a particular EADR0/PCLK edge

(3) HLDA1 rising edge will be controlled by the later of the EADR0/PCLK edge shown or HLDA

(4) ACK will follow the dashed lines shown only when $\overline{\text{MASTER}}$ is asserted

(5) Applicable for Bus Master cycles only

Figure 7-18. Basic HOLD/HDLA-DMA & Master Mode Transfers



NOTES:

(1) No refresh cycles are pending

(2) $\overline{\text{ONBRDL}}$ follow $\overline{\text{ONBRD}}$ when HLDA is high

(3) The FE3010 drives these signals when AEN is high

(4) The FE3001A tri-states $\overline{\text{EBHE}}$ when HLDA goes high, but drives it again when AEN is high. It is the inversion of ADR0

(5) $\overline{\text{BHE}}$ is driven by the FE3001A when HLDA1 is high. It follows $\overline{\text{EBHE}}$

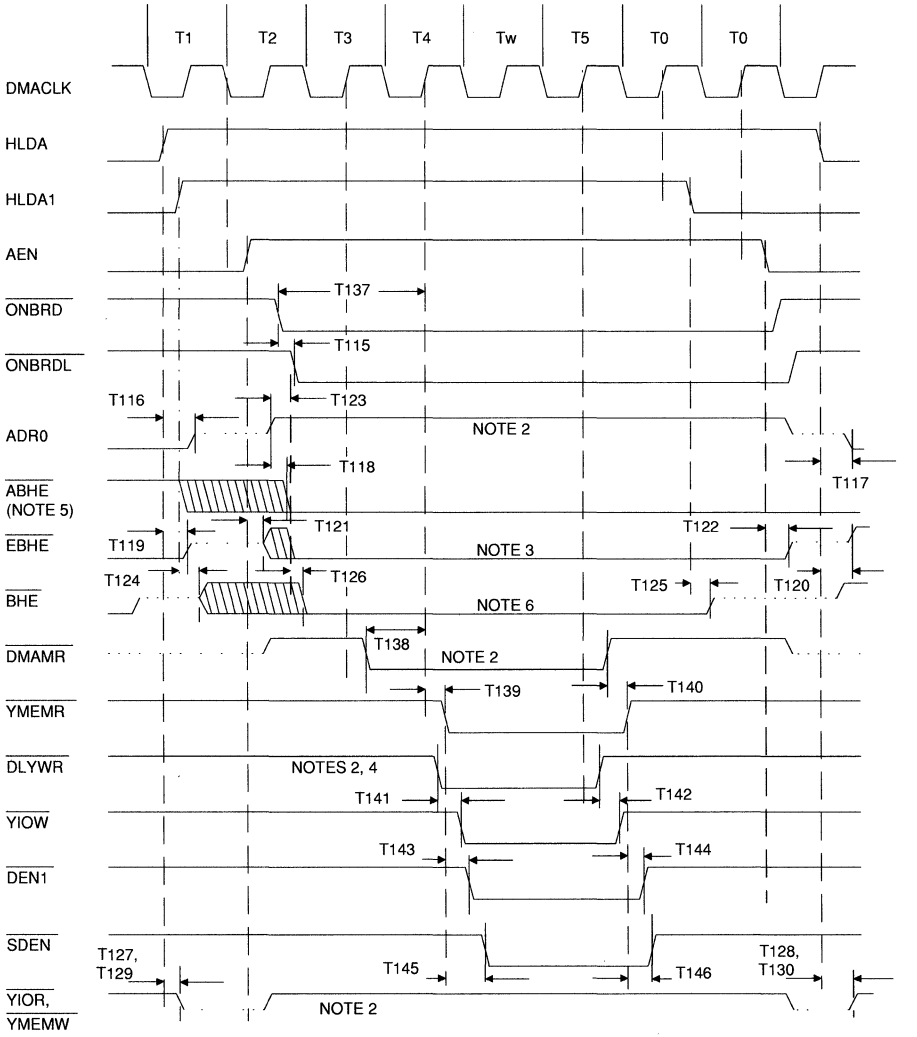
(6) $\overline{\text{ABHE}}$ is the inversion of ADR0 while HLDA is high (8-Bit DMA)

(7) $\overline{\text{DEN1}}$ and $\overline{\text{SDEN}}$ remain high during 8-Bit, even byte transfers

(8) The FE3001A tri-states $\overline{\text{DLYWR}}$ when AEN is high

Figure 7-19. DMA Transfer: 8-Bit, I/O to On-board Memory

Even Byte, with no Added Wait States



NOTES:

(1) No refresh cycles are pending

(2) The FE3010 drives these signals when AEN is high

(3) The FE3001A tri-states $\overline{\text{EBHE}}$ when HLDA goes high, but drives it again when AEN is high

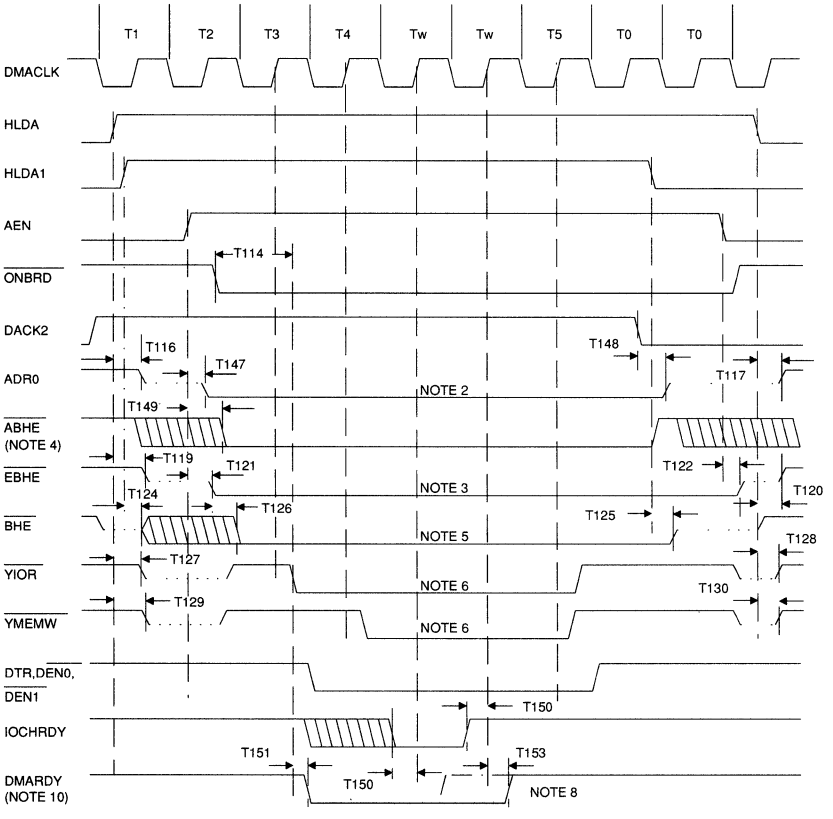
(4) The FE3001A tri-states $\overline{\text{DLYWR}}$ when AEN is high

(5) $\overline{\text{ABHE}}$ is the inversion of ADR0 when HLDA is high

(6) $\overline{\text{BHE}}$ is driven by the FE3001A when HLDA1 is high. It follows $\overline{\text{EBHE}}$

(7) $\overline{\text{DEN0}}$ and DTR remain high and SDTR remains low during this cycle

Figure 7-20. DMA Transfer: 8-Bit, On-board Memory to I/O, Byte, with No Added Wait States



NOTES:

(1) No refresh cycles are pending

(2) ADR0 is tri-stated when HLDA goes high, then driven again when both DACK2 and AEN are high(16-Bit DMA)

(3) $\overline{\text{EBHE}}$ is tri-stated when HLDA goes high, then driven again when AEN is high

(4) $\overline{\text{ABHE}}$ is set low when HLDA, DACK2, and AEN are high

(5) $\overline{\text{BHE}}$ is driven by the FE3001A when HLDA1 is high. It follows $\overline{\text{EBHE}}$

(6) The FE3010B drives these signals when AEN is high

(7) SDEN is high and SDTR is the inversion of DTR for this cycle

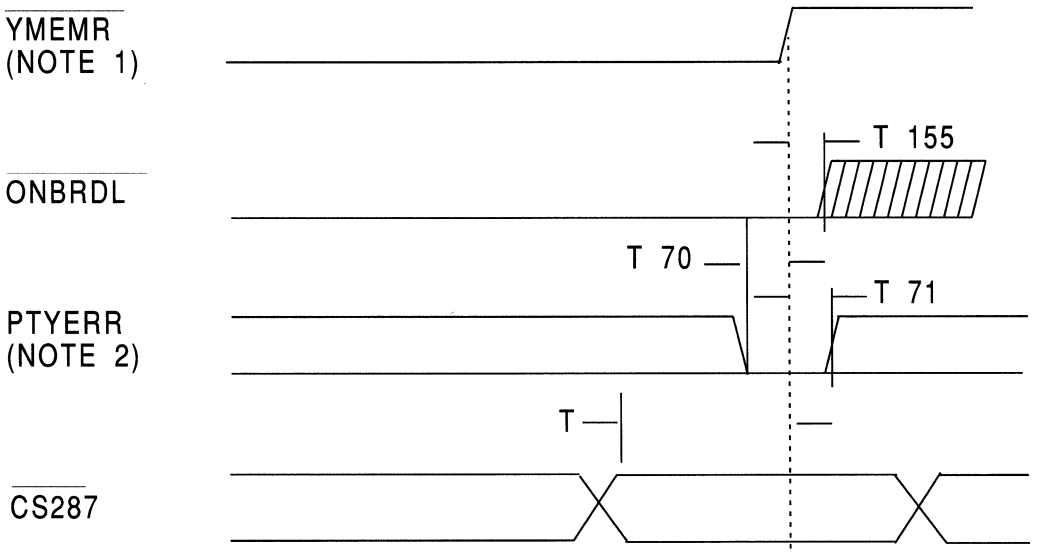
(8) DMARDY would follow the dashed line shown for any DMA cycle where IOCHRDY is not driven low (default timing)

(9) $\overline{\text{DMAMR}}$, $\overline{\text{DLYWR}}$, $\overline{\text{YMEMR}}$, and $\overline{\text{YIOW}}$ timing is the same as for an 8-Bit I/O to memory cycle

(10) DMARDY is driven low by $\overline{\text{DMAMR}}$ in a Memory to I/O DMA cycle

Figure 7-21. DMA Transfer: 16-Bit, I/O to On-board Memory

Wait State Added

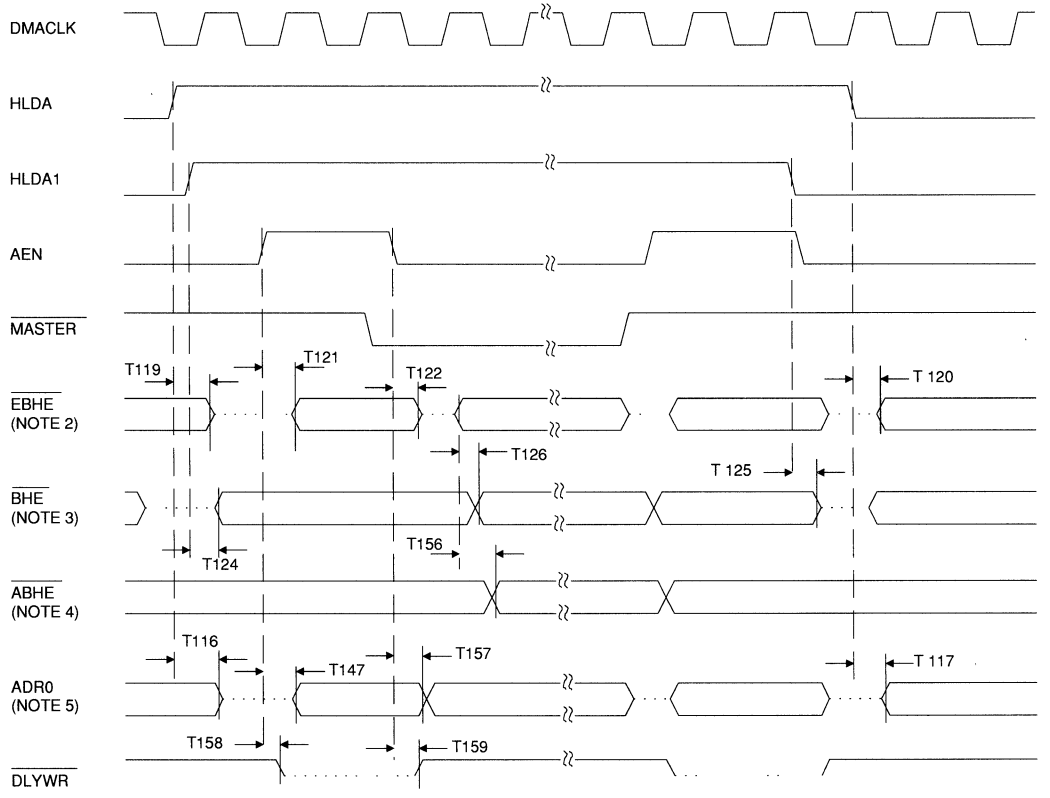


NOTES:

(1) YMEMR is an asynchronous signal during DMA or MASTER cycles. Setup time is shown for recognition at a particular edge of PROCLK

(2) PTYERR will be sampled at the first falling edge of PROCLK after YMEMR goes high

Figure 7-22. Parity Error Timing-DMA or Master Mode Transfer



NOTES:

(1) No refresh cycles are pending

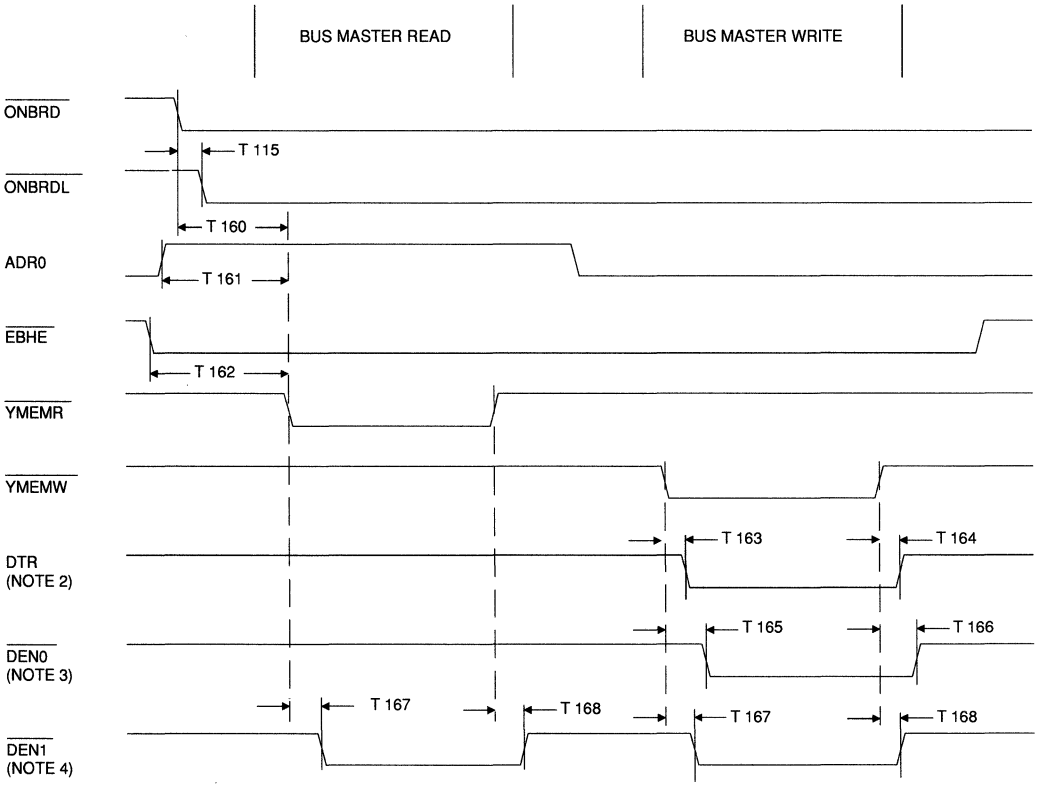
(2) $\overline{\text{EBHE}}$ is driven by the FE3001A when HLDA is low or AEN is high. It is driven by a Bus Master when MASTER is low

(3) $\overline{\text{BHE}}$ is driven by the FE3001A when HLDA1 is high. $\overline{\text{BHE}}$ will follow $\overline{\text{EBHE}}$ during Master mode

(4) $\overline{\text{ABHE}}$ follows $\overline{\text{EBHE}}$ during Master mode

(5) $\overline{\text{ADR0}}$ is driven by the FE3001A when HLDA is low. It will also be driven by the FE3001A when AEN

Figure 7-23. Basic Master Mode Transfer Timing



NOTES:

(1) $\overline{\text{MASTER}}$ is low during these cycles

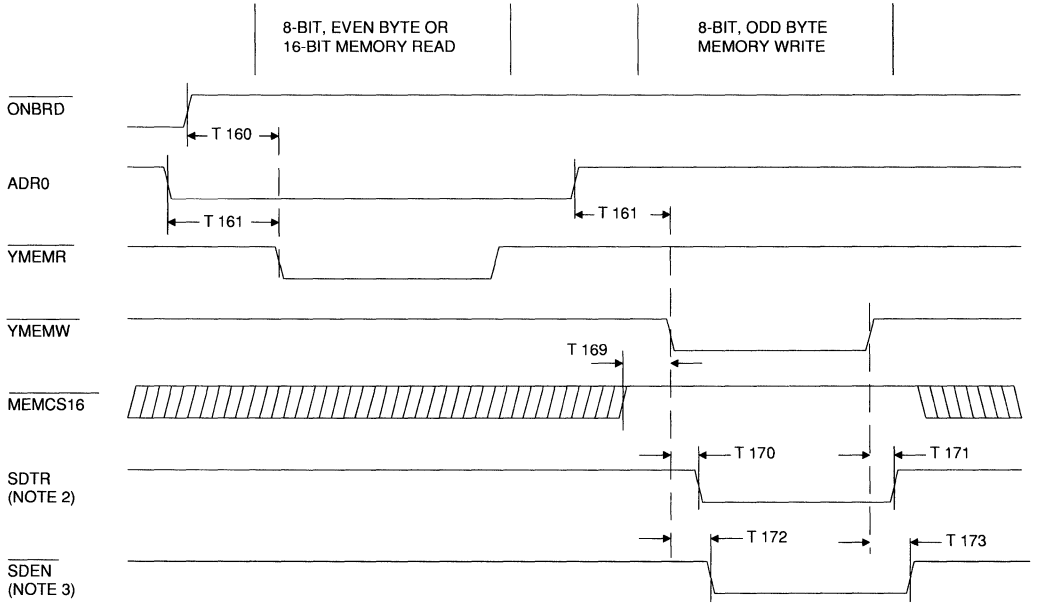
(2) DTR follows $\overline{\text{YMEMW}}$ during Master Mode

(3) $\overline{\text{DEN0}}$ follows $\overline{\text{YMEMR}}$ or $\overline{\text{YMEMW}}$ if both $\overline{\text{ONBRD}}$ and $\overline{\text{ADR0}}$ are low

(4) $\overline{\text{DEN1}}$ follows $\overline{\text{YMEMR}}$ or $\overline{\text{YMEMW}}$ if both $\overline{\text{ONBRD}}$ and $\overline{\text{EBHE}}$ are low

(5) $\overline{\text{SDEN}}$ is high during these cycles

Figure 7-24. Master Mode Transfer Timing: On-board Memory Read/Write



NOTES:

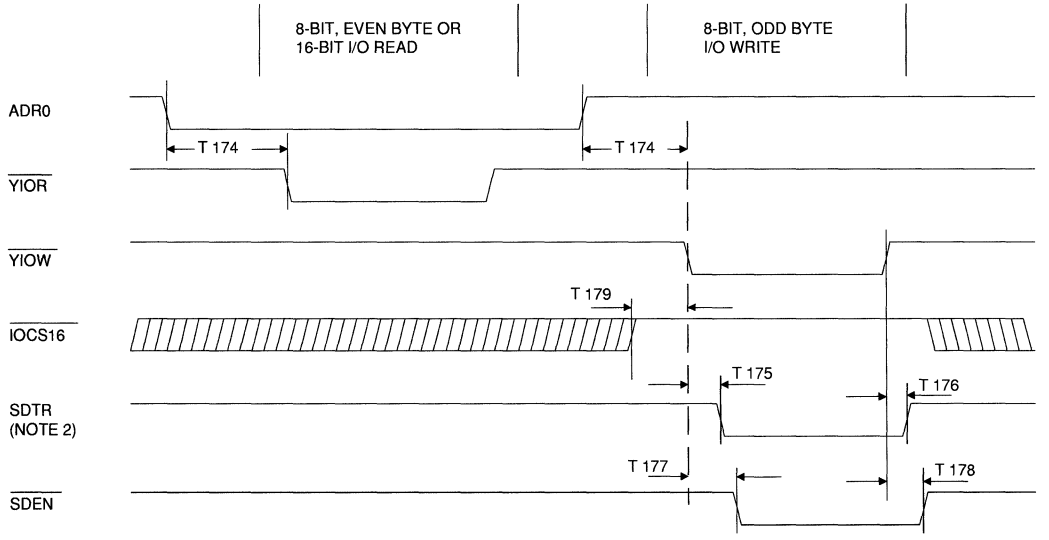
(1) $\overline{\text{MASTER}}$ is low during these cycles

(2) SDTR follows $\overline{\text{YMEMW}}$ when $\overline{\text{MASTER}}$ is low

(3) $\overline{\text{SDEN}}$ follows $\overline{\text{YMEMR}}$ or $\overline{\text{YMEMW}}$ when ADR0, $\overline{\text{MEMCS16}}$, and $\overline{\text{ONBRD}}$ are high

(4) $\overline{\text{DEN0}}$ and $\overline{\text{DEN1}}$ will stay high during these cycles because $\overline{\text{ONBRD}}$ is high

Figure 7-25. Master Mode Timing: Off-Board Memory Read/Write



NOTES:

(1) MASTER is low during these cycles

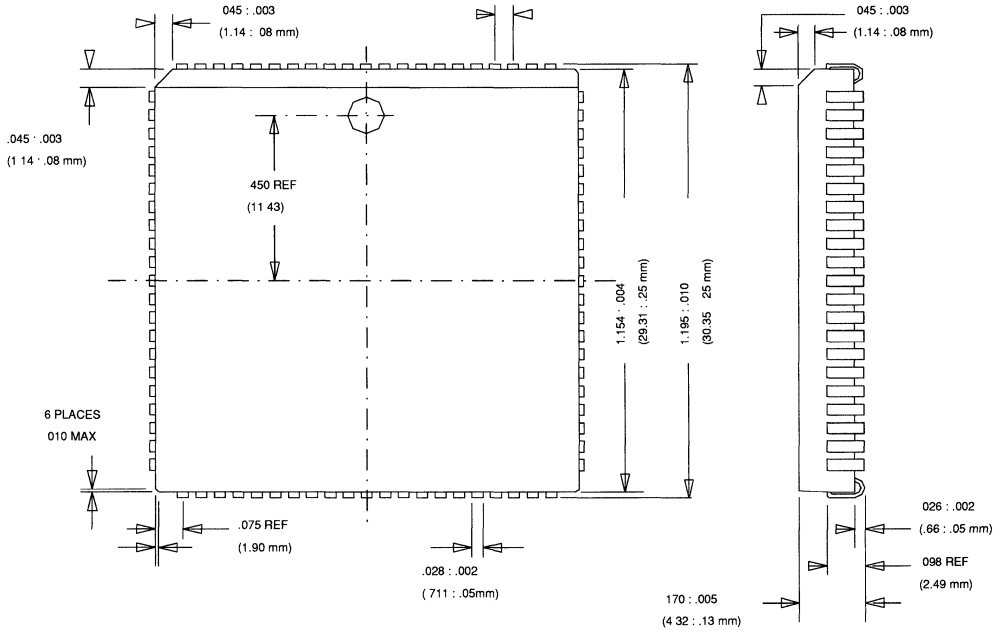
(2) SDTR follows YIOW

(3) SDEN follows YIOR or YIOW when ADR0 and IOCS16 are high. ONBRD does not affect SDEN for I/O cycles

(4) DEN0 and DEN1 will stay high during I/O cycles

Figure 7-26. Master Mode Timing: Off-Board I/O Read/Write

FE3010 84-Pin Plastic Chip Carrier (J-bend Leads)



1. Mating Socket. Burndy part number Q1LE84P10

3010JLED RVA 12/13/86

Figure 7-27. 84-Pin PLCC Packaging Diagram

APPENDIX A

FE3001A RECOMMENDED BUS CYCLE PROGRAMMING

The following tables give recommended values for programming bus timing registers R0-R8 (see Figure 5 and Table 3). These tables address only AT bus timing parameters, as on-board timing is very application specific. Values are provided for 6.25, 8, 12.5 and 16 MHz system clock speeds. The recommended values in these tables are based on emulating an 8 MHz IBM PC/AT Expansion Bus. Two issues that may affect these recommended values are listed below. Consult application notes for additional details.

(1) If the sum of R0 and R1 is 3 or greater, then an internal BALE logic error in first production FE3001A parts may cause BALE to remain high from a previous on-board cycle and fall one PROCLK cycle too early. Widening BALE by one clock accounts for this.

(2) Some adapter boards decode the SA0-SA19 address lines to generate MEMCS16, a dangerous practice. However, widening BALE and delaying the commands relative to an 8 MHz AT provides relaxed MEMCS16 setup time, which is needed for some of these boards to function reliably.

When preparing to select a new CPU clock speed, it is important to setup the FE3001A registers in a particular order so that BALE and commands do not become too short during the programming process. The recommended programming order for selecting high speed or low speed CPU clocks are given below:

Selecting High Speed CPU Clock:

R5, R6, R7, R8, R9, R10, R12, R4, R3, R1, R0

Selecting Low Speed CPU Clock:

R5, R6, R7, R8, R9, R10, R12, R0, R1, R3, R4

A.1 6.25 MHz SYSTEM CLOCK SPEED

REGISTER	FUNCTION	VALUE
R0	BALE delay from ALE leading edge	0
R1	BALE width	3
R3	8-bit memory, 8/16-bit I/O - command delay	3
R4	8-bit memory or I/O cycle - wait states	5
R5	16-bit I/O cycle - wait states	2
R6	16-bit memory cycle - command delay	2
R7	16-bit memory cycle - wait states	2
R8	Minimum number of wait states when ZEROWS is asserted	1

A.2 8 MHz SYSTEM CLOCK SPEED

REGISTER	FUNCTION	VALUE
R0	BALE delay from ALE leading edge	0
R1	BALE width	3
R3	8-bit memory, 8/16-bit I/O - command delay	3
R4	8-bit memory or I/O cycle - wait states	5
R5	16-bit I/O cycle - wait states	2
R6	16-bit memory cycle - command delay	2
R7	16-bit memory cycle - wait states	2
R8	Minimum number of wait states when ZEROWS is asserted	1

A.3 12.5 and 16 MHz SYSTEM CLOCK SPEED

REGISTER	FUNCTION	VALUE
R0	BALE delay from ALE leading edge	1
R1	BALE width	6
R3	8-bit memory, 8/16-bit I/O - command delay	7
R4	8-bit memory or I/O cycle - wait states	12
R5	16-bit I/O cycle - wait states	6
R6	16-bit memory cycle - command delay	6
R7	16-bit memory cycle - wait states	6
R8	Minimum number of wait states when ZEROWS is asserted	4

A.4 20 MHz SYSTEM CLOCK SPEED

REGISTER	FUNCTION	VALUE
R0	BALE delay from ALE leading edge	2
R1	BALE width	5
R3	8-bit memory, 8/16-bit I/O - command delay	9
R4	8-bit memory or I/O cycle - wait states	15
R5	16-bit I/O cycle - wait states	8
R6	16-bit memory cycle - command delay	6
R7	16-bit memory cycle - wait states	8
R8	Minimum number of wait states when ZEROWS is asserted	5

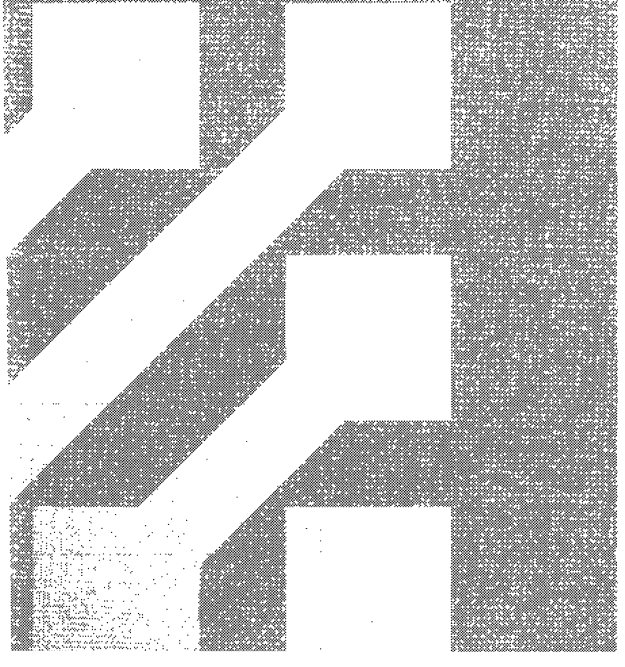
SYSTEMS LOGIC/PERIPHERAL

3

FE3010C

AT Peripheral

Control Device



WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

1.1 DESCRIPTION

As part of the Western Digital® FE3600B and FE3600C chip sets, the FE3010C AT Peripheral Control Device allows designers to build PC/AT Bus compatible single board computers that will operate at speeds from 10 MHz to 20 MHz with an 80286, or 16 or 20 MHz with an 80386SX processor.

The FE3010C is typically used in conjunction with the FE3001 (AT CPU Control Device), the FE3021 (AT Address Buffer and Memory Control Device), and the FE3031 (Data Buffer Device). Doing so allows you to reduce the size of an 80286 or 80386SX-based PC/AT compatible system board by 80%, power by 70%, and component count by 62%.

The FE3010C contains the functional equivalent of two 8237 DMA Controllers in cascade mode. This block improves the performance of a system by allowing external devices to transfer data directly from the system's memory. The FE3010C also contains the functional equivalent of two 8259 interrupt controllers in cascade mode. Additional features include 15 interrupt channels, 3 timer channels, 7 DMA channels, DMA page registers, 8 MHz DMA, and TTL compatibility.

1.2 FEATURES

- Hardware and software compatible with the IBM AT
- 15 interrupt channels
- 3 timer channels
- 7 DMA channels
- TTL compatible
- DMA clock rate up to 8 MHz
- Refresh circuitry for 256 Kbyte or 1 Mbyte DRAMs
- DMA page registers
- 1.25 Micron HCMOS technology
- 84-Pin PLCC

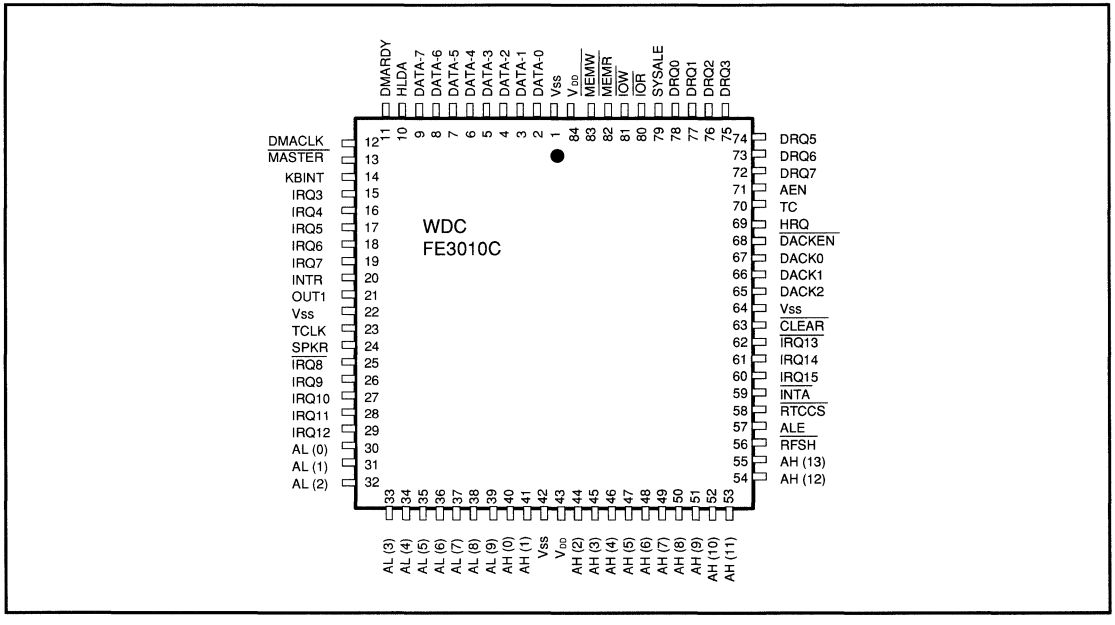


FIGURE 1-1. FE3010C PIN LOCATIONS

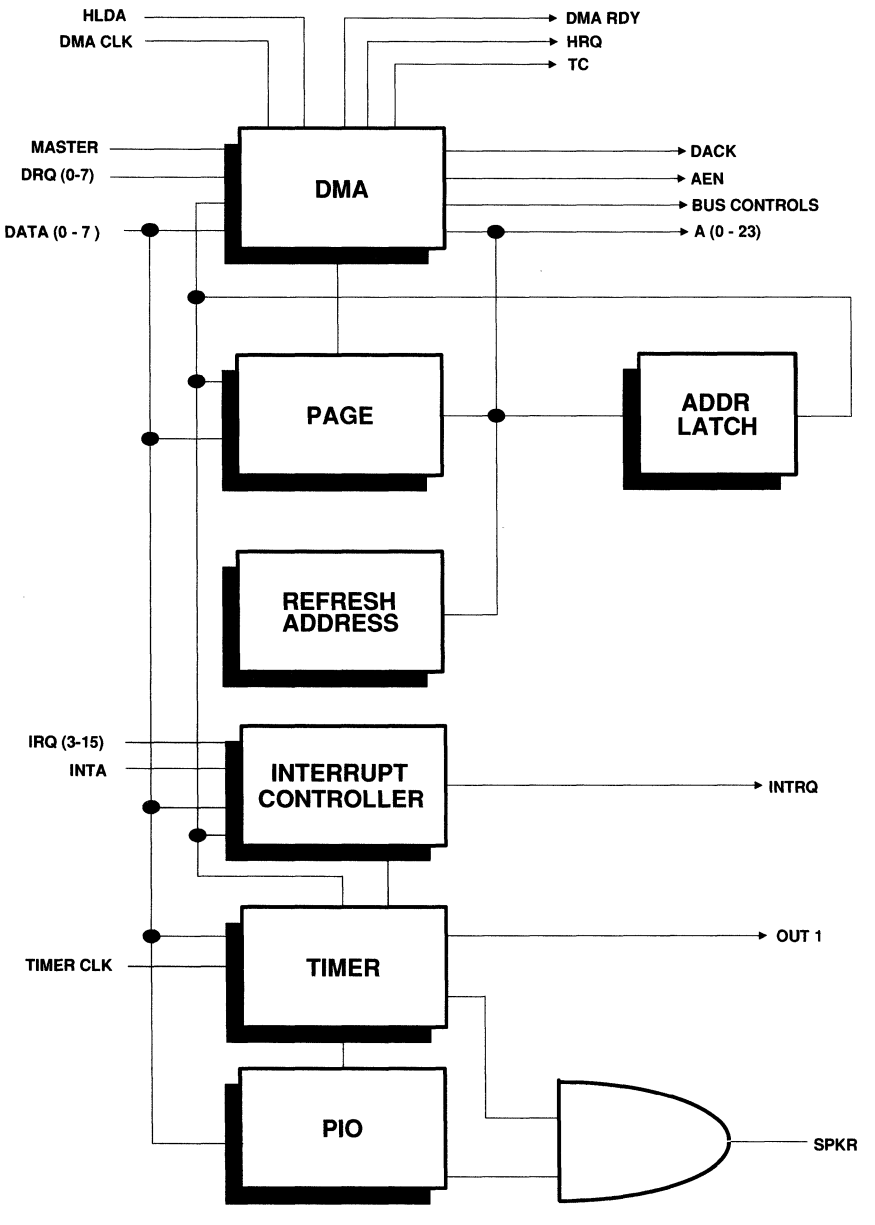


FIGURE 1-2. FE3010C FUNCTIONAL BLOCK DIAGRAM

PIN	TYPE	SYMBOL	FUNCTION
1		VSS	GROUND
2	I/O	DATA(0)	DATA BIT 0
3	I/O	DATA(1)	DATA BIT 1
4	I/O	DATA(2)	DATA BIT 2
5	I/O	DATA(3)	DATA BIT 3
6	I/O	DATA(4)	DATA BIT 4
7	I/O	DATA(5)	DATA BIT 5
8	I/O	DATA(6)	DATA BIT 6
9	I/O	DATA(7)	DATA BIT 7
10	I	HLDA	HOLD ACKNOWLEDGE Active high. Acknowledge from the CPU (80286) for a request for the bus from the DMA controller.
11	I	DMARDY	DMA READY Active high Signal to indicate that the DMA may complete its current cycle.
12	I	DMACLK	DMA CLOCK System clock/ DMACLK 6 MHz / 3 or 6 MHz 8 MHz / 4 or 8 MHz 10 MHz / 5 MHz
13	I	$\overline{\text{MASTER}}$	$\overline{\text{BUS MASTER}}$ Active low Signal indicating a master on the expansion bus has bus control.
14	I	KBINT	KEYBOARD INTERRUPT Active high
15	I	IRQ3	INTERRUPT REQUEST 3 Active high
16	I	IRQ4	INTERRUPT REQUEST 4 Active high
17	I	IRQ5	INTERRUPT REQUEST 5 Active high
18	I	IRQ6	INTERRUPT REQUEST 6 Active high
19	I	IRQ7	INTERRUPT REQUEST 7 Active high
20	O	INTR	INTERRUPT REQUEST TO CPU (80286) Active high
21	O	OUT1	TIMER CHANNEL 1 OUTPUT
22		V_{SS}	GROUND

TABLE 1-1. PIN ASSIGNMENT INFORMATION

PIN	TYPE	SYMBOL	FUNCTION
23	I	TCLK	TIMER CLOCK (1.19 MHz clock for timer)
24	O	SPKR	SPEAKER DATA
25	I	$\overline{\text{IRQ8}}$	$\overline{\text{INTERRUPT REQUEST 8}}$ Active low
26	I	IRQ9	INTERRUPT REQUEST 9 Active high
27	I	IRQ10	INTERRUPT REQUEST 10 Active high
28	I	IRQ11	INTERRUPT REQUEST 11 Active high
29	I	IRQ12	INTERRUPT REQUEST 12 Active high
30-39	I/O	AL(0-9)	ADDRESS BIT 0-9

NOTE

All addresses sent to the FE3010C during CPU cycles are latched with ALE except for A0. This allows compatibility for 16-bit writes to the FE3010C, although 8-bit accesses are preferred. A0 is latched in the FE3001, so no external latch on A0 is necessary if an FE3001 is used with the FE3010C.

40	O	AH(0)	ADDRESS BIT 10
41	O	AH(1)	ADDRESS BIT 11
42		V_{SS}	GROUND
43		V_{DD}	+5 VOLTS SUPPLY
44	O	AH(2)	ADDRESS BIT 12
45	O	AH(3)	ADDRESS BIT 13
46	O	AH(4)	ADDRESS BIT 14
47	O	AH(5)	ADDRESS BIT 15
48	O	AH(6)	ADDRESS BIT 16
49	O	AH(7)	ADDRESS BIT 17
50	O	AH(8)	ADDRESS BIT 18
51	O	AH(9)	ADDRESS BIT 19
52	O	AH(10)	ADDRESS BIT 20
53	O	AH(11)	ADDRESS BIT 21
54	O	AH(12)	ADDRESS BIT 22

TABLE 1-1. PIN ASSIGNMENT INFORMATION, CONTINUED

PIN	TYPE	SYMBOL	FUNCTION
55	O	AH(13)	ADDRESS BIT 23
56	I	$\overline{\text{RFSH}}$	$\overline{\text{REFRESH ADDRESS}}$ Active low Signal to enable the refresh address to the address bus during a RAM refresh cycle.
57	I	ALE	ADDRESS LATCH ENABLE Active high
58	O	$\overline{\text{RTCCS}}$	REAL TIME CLOCK CHIP SELECT
59	I	$\overline{\text{INTA}}$	$\overline{\text{INTERRUPT ACKNOWLEDGE}}$ FROM CPU (80286) Active low Interrupt acknowledge to the interrupt controllers
60	I	IRQ15	INTERRUPT REQUEST 15 Active high
61	I	IRQ14	INTERRUPT REQUEST 14 Active high
62	I	$\overline{\text{IRQ13}}$	$\overline{\text{INTERRUPT REQUEST 13}}$ Active low Error interrupt from (80287)
63	I	$\overline{\text{CLEAR}}$	$\overline{\text{SYSTEM CLEAR}}$ Active low
64		V_{SS}	GROUND
65	O	DACK2	DMA ACKNOWLEDGE BIT 2
DACK2	DACK1	DACK0	DMA Channel Acknowledge
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	illegal
1	0	1	5
1	1	0	6
1	1	1	7
66	O	DACK1	DMA ACKNOWLEDGE BIT 1
67	O	DACK2	DMA ACKNOWLEDGE BIT 0
68	O	DACKEN	$\overline{\text{DMA ACKNOWLEDGE ENABLE}}$ Active low Signal to enable DACK0, DACK1, and DACK2 decode.

TABLE 1-1. PIN ASSIGNMENT INFORMATION, CONTINUED

PIN	TYPE	SYMBOL	FUNCTION
69	O	HRQ	DMA REQUEST TO CPU (80286) Active high
70	O	TC	DMA END OF OPERATION Active high Signal to indicate the DMA controller has finished its cycle.
71	O	AEN	DMA AEN Active high Signal to indicate that the current bus is a DMA cycle.
72	I	DRQ7	CHANNEL 7 DMA REQUEST Active high
73	I	DRQ6	CHANNEL 6 DMA REQUEST Active high
74	I	DRQ5	CHANNEL 5 DMA REQUEST Active high
75	I	DRQ3	CHANNEL 3 DMA REQUEST Active high
76	I	DRQ2	CHANNEL 2 DMA REQUEST Active high
77	I	DRQ1	CHANNEL 1 DMA REQUEST Active high
78	I	DRQ0	CHANNEL 0 DMA REQUEST Active high
79	O	SYSALE	SYSTEM ALE Active high Signal to latch the address in the address latch.
80	I/O	$\overline{IOR}$	$\overline{I/O\ READ\ COMMAND}$ Active low
81	I/O	$\overline{IOW}$	$\overline{I/O\ WRITE\ COMMAND}$ Active low
NOTE Data must be valid before $\overline{IOW}$ to the FE3010C goes low because the leading edge of $\overline{IOW}$ is used to clock some registers in the FE3010C. This setup time (data valid to $\overline{IOW}$ active low) is specified at 30 ns minimum.			
82	O	$\overline{MEMR}$	$\overline{MEMORY\ READ\ COMMAND}$ Active low
83	O	$\overline{MEMW}$	$\overline{MEMORY\ WRITE\ COMMAND}$ Active low
84		V_{DD}	+5 VOLTS SUPPLY

TABLE 1-1. PIN ASSIGNMENT INFORMATION, CONTINUED

2.0 DMA CONTROL

2.1 OVERVIEW

The FE3010C contains two 8237 equivalent DMA controllers. DMA controller #1 is in the I/O address space from 000 to 00F and is used for 8-bit transfers. DMA controller #2 is in the I/O space from 0C0 to 0DE and is used for 16-bit transfers. Channel 0 of DMA controller #2 is used to cascade DMA controller #1.

AT Bus DMA Channel	DMA Controller	Transfer Type
0	#1 Channel 0	8-bit
1	#1 Channel 1	8-bit
2	#1 Channel 2	8-bit
3	#1 Channel 3	8-bit
4	#2 Channel 0	Cascade DMA Cont. #1
5	#2 Channel 1	16-bit
6	#2 Channel 2	16-bit
7	#2 Channel 3	16-bit

TABLE 2-1. DMA TRANSFER TYPES

2.2 TRANSFER MODES

Each DMA channel may be programmed in Single Transfer Mode, Block Transfer Mode, Demand Transfer Mode, or Cascade Mode.

2.2.1 Single Transfer Mode

In single transfer mode the channel will make one transfer for each request. The word count will be decremented, and the address will be incremented or decremented at the end of each transfer. When the word count goes from 0000 to FFFF, a terminal count (TC) will be generated. To start a transfer, the DRQ should be held active high until a DACK is received. If the DRQ is held active through the cycle, only one transfer will take place. The DRQ must go low and then high to start another transfer. The bus will be released between transfers.

2.2.2 Block Mode Transfer

A transfer is started in block mode by a DRQ and continues until a TC is reached. The DRQ should be held active until DACK becomes active. Block mode should be used with caution since refresh will be locked out. The address and word count behave as in single mode.

2.2.3 Demand Mode

In demand mode, a transfer will continue to take place until DRQ is inactive or a TC is reached. If the DRQ is dropped, the bus will be released. If DRQ is activated again, the transfer will resume. The address and word count behave as in single mode.

2.2.4 Cascade Mode

Cascade mode is used to cascade DMA controller #2 to DMA controller #1, and for bus master transfers. A channel in cascade mode will get the bus when a DRQ is active, but the word count and address are ignored. The channel will hold the bus until DRQ is inactive. The IOR, IOW, MEMR, and MEMW signals must be generated by the bus master device. The addresses from the FE3010C are floated when the MASTER signal becomes active.

2.3 TRANSFER TYPES

There are three types of transfers: read, write, and verify.

Read

A read transfers data from memory to an I/O device.

Write

A write transfers data from an I/O device to memory.

Verify

A verify transfer is a pseudo transfer that does not generate IOR, IOW, MEMR, or MEMW signals.

2.4 AUTOINITIALIZE

A channel may be programmed to autoinitialize for any transfer type. In this mode when a TC is reached the channel is loaded with the original word count and address, and is ready to start another transfer.

2.5 PRIORITY

Each DMA controller has two types of priority, fixed and rotating. For fixed priority, channel 0 has the highest priority and channel 3 has the lowest. In rotating priority, the last channel to be serviced has the lowest priority. The DMA controller #2 has priority over the DMA controller #1.

2.6 EXTENDED WRITE

In normal timing the MEMR or IOR pulse is two clock cycles and the MEMW or IOW is one clock cycle. If extended write is selected, the MEMW or IOW will be the same as the MEMR or IOR.

2.7 BASE AND CURRENT ADDRESS REGISTERS

Each channel has a 16-bit base and current address register. The current address register is loaded from the base register when the base register is loaded or when in autoinitilize mode. The current address register is incremented or decremented during a transfer.

Addresses are driven to the bus while $\overline{\text{RFSH}}$ is low, indicating a refresh cycle. Only address bits A23-A16 (from the page register) and bits A10-A0 (from the refresh counter) are meaningful during refresh. The address counter gets incremented on the rising edge of $\overline{\text{RFSH}}$.

2.8 BASE AND CURRENT WORD COUNT

Each channel has a 16-bit base and current word count register. The current word count register is loaded from the base register when the base register is loaded or when in autoinitilize mode. The current word count is decremented during a transfer.

2.9 COMMAND REGISTER WRITE

This register is cleared by a reset or Master Clear command.

0-1	Unused
2	Controller Disable
3	Must be 0 for extended write, otherwise no effect
4	Rotating Priority
5	Extended Write
6-7	Unused

TABLE 2-2. COMMAND REGISTER WRITE FORMAT

2.10 STATUS REGISTER READ

Bits 0-3 are cleared by a reset, a Master Clear command or a status read.

0	Channel 0 has Reached TC
1	Channel 1 has Reached TC
2	Channel 2 has Reached TC
3	Channel 3 has Reached TC
4	Channel 0 DRQ Active
5	Channel 1 DRQ Active
6	Channel 2 DRQ Active
7	Channel 3 DRQ Active

TABLE 2-3. STATUS REGISTER READ FORMAT

2.11 REQUEST REGISTER WRITE

Each channel may be started by a software request. These request are not affected by the mask register. It is cleared by a reset or a Master Clear command.

0-1	Channel Number ⇒	00	Channel 0
2	Request	01	Channel 1
3-7	Unused	10	Channel 2
		11	Channel 3

TABLE 2-4. REQUEST REGISTER WRITE FORMAT

2.12 MASK REGISTER WRITE

Each channel has a mask bit associated with it. If it is set, the channel is disabled. The bits may be set or cleared by software or set by a TC if the channel is not in autoinitilize mode. All the bits are set by a reset or a Master Clear Function.

SINGLE MASK	
0-1	Channel Select
2	Set/Clear Mask (0 = Clear, 1 = Set)
3-7	Unused
CLEAR MASK	
0-7	Unused
MASK ALL	
0	Channel 0 Mask
1	Channel 1 Mask
2	Channel 2 Mask
3	Channel 3 Mask
4-7	Unused

TABLE 2-5. MASK REGISTER WRITE FORMAT

2.13 MODE REGISTER WRITE

0-1	Channel Select ⇒	00 Channel 0
		01 Channel 1
		10 Channel 2
		11 Channel 3
2-3	Transfer Type ⇒	00 Verify
		01 Write
		10 Read
		11 Unused
4	Autoinitialize	
5	Address Decrement	
6-7	Mode ⇒	00 Demand
		01 Single
		10 Block
		11 Cascade

TABLE 2-6. MODE REGISTER WRITE

2.14 CLEAR POINTER WRITE

Each DMA controller has a pointer flip flop that indicates which half of the word count or address is being accessed. Each time a word count or address is written or read, the pointer is toggled. When the flip flop is cleared, bits 0-7 are accessed and when it is set, bits 8-15 are accessed. The pointer may be cleared by writing to the Clear Pointer. Any data is ignored.

2.15 MASTER CLEAR WRITE

A write to the Master Clear will:

1. Clear the Command Register
2. Clear the Status Register
3. Clear the Request Register
4. Set the Mask Register
5. Clear the Pointer Flip Flop

Any data will be ignored.

I/O Address	Read/Write	DMA Controller	Function
000	Read/Write	1	Channel 0 Address
001	Read/Write	1	Channel 0 Word Count
002	Read/Write	1	Channel 1 Address
003	Read/Write	1	Channel 1 Word Count
004	Read/Write	1	Channel 2 Address
005	Read/Write	1	Channel 2 Word Count
006	Read/Write	1	Channel 3 Address
007	Read/Write	1	Channel 3 Word Count
008	Read	1	Status
008	Write	1	Command Register
009	Write	1	Request Register
00A	Write	1	Single Mask
00B	Write	1	Mode Register
00C	Write	1	Clear Pointer
00D	Write	1	Master Clear
00E	Write	1	Clear Mask
00F	Write	1	Mask All
0C0	Read/Write	2	Channel 0 Address
0C2	Read/Write	2	Channel 0 Word Count
0C4	Read/Write	2	Channel 1 Address
0C6	Read/Write	2	Channel 1 Word Count
0C8	Read/Write	2	Channel 2 Address
0CA	Read/Write	2	Channel 2 Word Count
0CC	Read/Write	2	Channel 3 Address
0CE	Read/Write	2	Channel 3 Word Count
0D0	Read	2	Status
0D0	Write	2	Command Register
0D2	Write	2	Request Register
0D4	Write	2	Single Mask
0D6	Write	2	Mode Register
0D8	Write	2	Clear Pointer
0DA	Write	2	Master Clear
0DC	Write	2	Clear Mask
0DE	Write	2	Mask All

TABLE 2-7. DMA CONTROL FUNCTION MAP

3.0 DIFFERENCES BETWEEN THE FE3010C AND 8237

The FE3010C implementation is different from the Intel 8237 in two ways. The DMA address in the 8237 is valid during the entire DMA cycle, while the FE3010C multiplexes the address and transfer count on the address bus. Therefore, addresses A16-A0 from the FE3010C need to be latched with SYSALE coming out from the FE3010C. These latches are in the FE3021.

The second difference is in the cascade mode; the 8237 does not enable the address outputs, while the FE3010C does. Since the only way to use the cascade mode on an AT system is through Bus Master operation, this is not a problem, since the FE3010C disables its address outputs when the MASTER signal becomes active.

4.0 8259 INTERRUPT CONTROLLERS

The FE3010C contains two 8259 equivalent interrupt controllers. Interrupt controller #1 is in the I/O space of 020 to 021, and interrupt controller #2 is in the I/O space of 0A0 to 0A1. Interrupt 2 of interrupt controller #1 is used to cascade interrupt controller #2.

4.1 INTERRUPT SEQUENCE

1. When an interrupt arrives from a peripheral device, the interrupt may be programmed to be level or edge sensitive. In the level mode, the interrupt will keep occuring as long as the interrupt is kept high. In the edge mode, it must go low and high for each interrupt. The interrupt will set the appropriate bit in the Interrupt Request Register (IRR).

System Interrupt	Interrupt Controller	Use
0	#1 Level 0	Timer
1	#1 Level 1	Keyboard
2	#1 Level 2	Cascade
3-7	#1 Level 3 - 7	AT Bus
8	#2 Level 0	R.T.C.
9-12	#2 Level 1-4	AT Bus
13	#2 Level 5	Co-Processor
14-15	#2 Level 6-7	AT Bus

TABLE 4-1. INTERRUPT SEQUENCE FORMAT

2. If the interrupt has not been masked off, it is passed to the priority circuit. There are three types of priority.

Fixed

In fixed priority, interrupt 0 has the highest priority and interrupt 7 has the lowest.

Automatic Rotation

In automatic rotation, the last interrupt serviced has the lowest priority.

Specific Rotation

In this mode, the lowest priority interrupt can be set by software. The next interrupt will have the highest priority. For example if interrupt 4 is set to the lowest level, the priority will be 5, 6, 7, 0, 1, 2, 3, and 4.

3. The interrupt controller sends an IRQ to the CPU.

4. The CPU responds with an INTA cycle that freezes priority.

5. The CPU sends another INTA that causes the interrupt controller to send a vector to the CPU and set the appropriate bit in the Interrupt Service Register (ISR) and clear the corresponding bit in the IRR, if it is in the edge triggered mode. As long as the bit in the ISR is set, all interrupts at the same level or lower will be inhibited unless programmed for special mask mode.

6. An EOI is issued to end the interrupt. This clears the appropriate bit in the Interrupt Service Register. For the slave adapter (interrupt controller #2), two EOI's must be issued. There are three types of EOI's.

Specific

An EOI is issued by software for a specific interrupt.

Non-Specific

A non-specific EOI is issued by software. The hardware will generate a EOI for the highest level active interrupt.

Automatic

An automatic EOI is a non-specific EOI that is caused by the second INTA.

The interrupt controllers may also be operated in a polled mode. In this mode, the CPU is set to disable the interrupt input. In this case, software must issue a poll command. This takes the place of an INTA, and the software can then read the interrupt level to determine the interrupt to be serviced.

When cascading is used and the slave has issued an interrupt, other interrupts from the slave are locked out. If it is desired to preserve priority in the slave (i.e. allow higher interrupts to occur when a lower interrupt is being serviced), Special Fully Nested Mode should be programmed in the master. After a non-specific EOI has been sent to the slave, the ISR should be checked to see if any

other interrupts are active. If there are no interrupts active, a non-specific EOI should be sent to the master.

4.2 SETUP

The interrupt controllers are setup by writing a series of initialization command words (ICW). The sequence is started by writing ICW1 with data bit 4 = 1. ICW2 is then written followed by ICW3 and ICW4 if they are needed.

ICW1 Write	
0	ICW4 Needed
1	Not Cascade Mode
2	Unused
3	Level Triggered
4	1
5-7	Unused
ICW2 Write	
0-2	Unused
3-7	Interrupt Vector
ICW3 Write (Interrupt Controller #1 only)	
0-1	0
2	Interrupt 2 has slave
3-7	0
ICW3 Write (Interrupt Controller # 2 only)	
0-2	Slave I/D
3-7	0
ICW4	
0	1
1	Auto EOI
2-3	0
4	Special Fully Nested Mode
5-7	0

TABLE 4-2. ICW FORMATS

4.3 OPERATION

Once the interrupt controllers are setup, they may be programmed by Operation Control Words (OCW).

OCW1		
0	Interrupt 0 Mask	
1	Interrupt 1 Mask	
2	Interrupt 2 Mask	
3	Interrupt 3 Mask	
4	Interrupt 4 Mask	
5	Interrupt 5 Mask	
6	Interrupt 6 Mask	
7	Interrupt 7 Mask	
OCW2		
0-2	Interrupt Level	
3-4	0	
5-7 ⇒	001	Non-specific EOI
	011	Specific EOI
	111	Rotate on Specific EOI
	101	Rotate on Non-Specific EOI
	100	Select Rotate on Automatic EOI
	000	Clear Rotate On Automatic EOI
	110	Set Priority
	010	Unused

TABLE 4-3. OCW FORMATS

4.3.1 OCW3

Bits 0, 1, and 2 of OCW3 determine what the next read of the interrupt controller will yield.

0-1 ⇒	00	Unused
	01	Unused
	10	Select Read IRR
	11	Select Read ISR
2	Poll Command	
3	1	
4	0	
5-6 ⇒	00	Unused
	01	Unused
	10	Reset Special Mask Mode
	11	Set Special Mask Mode
7	0	

TABLE 4-4. OCW3 FORMATS

Interrupt Controller	Address	Function	Read/Write
1	020	ICW1	Write
1	021	ICW2	Write
1	021	ICW3	Write
1	021	ICW4	Write
1	021	OCW1	Write
1	020	OCW2	Write
1	020	OCW3	Write
1	020	IRR	Read
1	020	ISR	Read
1	021	Mask	Read
1	020, 021	Interrupt Level	Read
2	0A0	ICW1	Write
2	0A1	ICW2	Write
2	0A1	ICW3	Write
2	0A1	ICW4	Write
2	0A1	OCW1	Write
2	0A0	OCW2	Write
2	0A0	OCW3	Write
2	0A0	IRR	Read
2	0A0	ISR	Read
2	0A1	Mask	Read
2	0A0, 0A1	Interrupt Level	Read

TABLE 4-5. INTERRUPT CONTROLLER FUNCTION MAP

5.0 8254 TIMER

The FE3010C contains an 8254 equivalent timer that contains three independent counters. All the timers run off a 1.19 MHz clock. The GATE0 and GATE1 signals are tied high. The GATE2 signal is tied to register 61, bit 0. The counters decrement when counting. The largest possible count is 0.

Each counter may be programmed for different counting modes and the count may be read back. To initilize a counter, the Control Word must be written followed by one or two bytes of count if needed. Each counter may be programmed to count in BCD or binary.

Timer Channel	Use
0	Time of Day (Interrupt)
1	Refresh Request
2	Speaker

I/O Address	Use	Read/Write
040	Timer 0 Count/Status	Read/Write
041	Timer 1 Count/Status	Read/Write
042	Timer 2 Count/Status	Read/Write
043	Control Word	Write

CONTROL WORD (FORMAT 1)			
0	CD		
1-3	Mode ⇒	000	Mode 0
		001	Mode 1
		X10	Mode 2
		X11	Mode 3
		100	Mode 4
		101	Mode 5
4-5	Function ⇒	00	Counter Latch Command
		01	Read/Write Low Byte
		10	Read/Write High Byte
		11	Read/Write Low Byte then High Byte
6-7	Counter ⇒	00	Counter 0
		01	Counter 1
		10	Counter 2
CONTROL WORD (FORMAT 2)			
0		0	
1		Select Counter 0	
2		Select Counter 1	
3		Select Counter 2	
4		Latch Status	
5		Latch Count	
6-7		1	

TABLE 5-1. CONTROL WORD FORMAT

5.1 SETUP

Each counter may be set in one of 5 modes by writing a command word (format 1). The command word must specify the counter and the number of count bytes to be written. A new count may be written at any time.

5.1.1 Mode 0 Interrupt on Terminal Count

The counter starts when the count is loaded. When the count = 0, the counter will continue counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting.

OUT will go low when the counter starts. It will go high when the count = 0, and stay high until a new count or mode is written.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.1.2 Mode 1 Hardware Retriggerable One Shot

The counter starts when GATE goes from low to high. When the count = 0, the counter will continue counting from FFFF in binary mode or 9999 in BCD mode.

Any time GATE goes from low to high, the counter will be reloaded with the original count and the counter started.

OUT will go low when GATE goes from low to high. It will go high when the count = 0. If a new count is written while the counter is counting, it will be loaded the next time GATE goes from low to high.

5.1.3 Mode 2 Rate Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter is started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

OUT will initially be high. When the count = 1, OUT will go low for one clock.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.1.4 Mode 3 Square Wave Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

When the counter starts, OUT will be high. When the count is half done, OUT will go low. If GATE goes low, then OUT will go high.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.1.5 Mode 4 Software Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter will continue counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. OUT will initially be high. When the count = 0, OUT will go low for one clock.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.1.6 Mode 5 Hardware Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter will continue counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded. OUT will be high when the counter starts. When count = 0, OUT will go low for one clock. If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.2 READING THE COUNTER

There are three ways of reading the counters:

1. The count is read directly. This mode can cause false readings due to fact that the counter may be changing while it is read.

2. The count may be read via a Counter Latch Command. (See COMMAND WORD format 1). This command latches the count so it may be read without changing.

3. The count may be read via a Read Back Command. (See COMMAND WORD format 2). This command is the equivalent of multiple Counter Latch Commands.

5.3 READING STATUS

The status of a counter may be read by issuing a Read Back Command with data bit 4 = 0. (See COMMAND WORD format 2). Bits 0-5 are the same as the command word for the counter. Bit 6 tells if the last count that was written has been loaded into the counter. Bit 7 reflects the state of the OUT pin.

STATUS WORD	
0	BCD
1-3	Mode
4-5	Function
6	New Count Written
7	Out Status

5.4 PAGE

The page register is an 8-bit by 16-byte dual-ported RAM. It is used to refresh cycles and to generate address bits 16 to 23 for 8-bit DMA transfers and address bits 17 to 23 for 16-bit DMA transfers. One port of the RAM is a read-only port for DMA or refresh cycles, and the other is a read/write port for the 80286 CPU.

5.5 REFRESH ADDRESS

This block contains an 11-bit counter that is used for the address during a refresh.

6.0 DECODE

Address				Decodes					Hex		
9	8	7	6	5	4	3	2	1	01		
0	0	0	0	0	X	X	X	X	X	DMA Controller 1 (Ch 0-3)0	00-01F
0	0	0	0	1	X	X	X	X	X	Interrupt Controller Master	020-03F
0	0	0	1	0	X	X	X	X	X	Timer	040-05F
0	0	0	1	1	0	X	X	X	1	Port B (PI0)	060-06F(odd)
0	0	0	1	1	1	X	X	X	1	Real Time Clock (RTCCS)	070-07F(odd)
0	0	1	0	0	X	X	X	X	X	Page Register	080-09F
0	0	1	0	1	X	X	X	X	X	Interrupt Controller Slave	0A0-0BF
0	0	1	1	0	X	X	X	X	X	DMA Controller 2 (Ch 4-7)	0C0-0DF

TABLE 6-1. DECODE ADDRESSES

6.1 PAGE REGISTER DECODES

Address	Decode
0087	DMA Channel 0
0083	DMA Channel 1
0081	DMA Channel 2
0082	DMA Channel 3
008B	DMA Channel 5
0089	DMA Channel 6

TABLE 6-2. PAGE REGISTER DECODES

Note: Page register data appears on address bits A23-A16 during refresh and 8-bit DMA cycles. For 16-bit DMA cycles (channels 5-7), the LSB of the page register does not appear; instead the 16-bit DMA address is shifted up one bit and A0 is floated in the FE3010C to be driven by external logic.

6.2 PIO

This block contains the control port to control the speaker and timer channel. It also contains circuitry to detect if refresh is running. This condition may be read back as bit 4. Bits 2 and 3 are read/write, but they do not perform any function. They are used for software compatibility with the IBM PC AT.

Port B (PIO) is an 8-bit control and status register on the AT. Bits 0 through 5 are defined in the FE3010C, while bits 6 and 7 are generated in the FE3001. During a read of Port B (address 0061), the FE3010C drives data bits 0-5 and tri-states bits 6 and 7. The FE3001, if used, will drive bits 6 and 7 indicating the parity error and channel check status. Bits 0 through 5 are described in the table below.

Bits 3 and 2 perform no function on the FE3010C; they are duplicated here to provide the read/write capability, but the actual enable functions are performed in the FE3001.

Bit	Function
5	OUT2 from timer channel 2 (read only)
4	Toggles on each refresh (read only)
3	Enable channel check (active low)
2	Enable parity check (active low)
1	Enable speaker (active high)
0	Gate for timer channel 2

TABLE 6-3. DECODE BIT FUNCTIONS

7.0 ABSOLUTE MAXIMUM RATINGS

T_A=+25 °C	
Power supply voltage, V_{DD} @ V_{SS}=0	7.0 V
Power dissipation, PD_{MAX} @V_{DD}=5.25V	300 mW
Current, I_{DD} @V_{DD}=5.25V	55 mA
Input voltage,V_I	0.0V to V_{DD} + 0.3V
Output voltage,V_O	0.0V to V_{DD} + 0.3V
Operating temperature, T_{OPT}	0° C to 70° C
Storage temperature, T_{STG}	-40° C to 125° C

* Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8.0 CAPACITANCE

(TA=+25° C, V_{DD} = 0V)			
Parameter	**Symbol**	**Max Limits**	**Test Condition**
Input capacitance	C_I	10 pF	fc = 1 MHz unmeasured
			pins returned to 0V
I/O capacitance	C_{IO}	15 pF	

9.0 DC CHARACTERISTICS

TA = 0° C to 70° C, VDD = 5V ± 5%, these inputs have internal 50K Ω(min.) pullups.
[ALE, DMACLK, DMARDY, DRQ0, DRQ1, DRQ2, DRQ3, DRQ5, DRQ6, DRQ7, HLDA, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, IRQ15, KBINT, $\overline{\text{CLEAR}}$, $\overline{\text{INTA}}$, $\overline{\text{IRQ13}}$, $\overline{\text{MASTER}}$, $\overline{\text{RFSH}}$, TLCK, $\overline{\text{IRQ8}}$]

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	V_{IL}	V_{SS}	0.8	V	V_{DD} = 5V ± 5%
Input high voltage	V_{IH}	2.0	V_{DD}	V	V_{DD} = 5V ± 5%
Input low current	I_{IL}	-10.0	-300.0	uA	V_{IN} = 0.0V
Input high current	I_{IH}		40.0	uA	V_{IN} = V_{DD}

[A(0), A(1), A(2), A(3), A(4), A(5), A(6), A(7), A(8), A(9), DATA(0), DATA(1), DATA(2), DATA(3), DATA(4), DATA(5), DATA(6), DATA(7), $\overline{IOR}$, $\overline{IOW}$]

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	V_{IL}	V_{SS}	0.8	V	V_{DD} = 5V ± 5%
Input high voltage	V_{IH}	2.0	V_{DD}	V	V_{DD} = 5V ± 5%
Input low current	I_{IL}		-10.0	uA	V_{IN} = 0.0V
Input high current	I_{IH}		10.0	uA	V_{IN} = V_{DD}
Output low voltage	V_{OL}		0.4	V	I_{OL} = 4.0 mA
Output high voltage	V_{OH}	2.4		V	I_{OH} = - 4.0 mA
Output current	I_{OZ}	-10.0	10.00	uA	0V < V_{OUT} <V_{DD}

[AEN, DACK0, DACK1, DACK2, HRQ, INTR, $\overline{DACKEN}$, $\overline{RTCCS}$, OUT1, SPKR, SYSALE]

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	V_{OL}		0.4	V	I_{OL} = 2.0 mA
Output high voltage	V_{OH}	2.4		V	I_{OH} = - 2.0 mA

[A(10), A(11), A(12), A(13), A(14), A(15), A(16), A(17), A(18), A(19), A(20), A(21), A(22), A(23), $\overline{MEMR}$, $\overline{MEMW}$, TC]

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	V_{OL}		0.4	V	I_{OL} = 4.0 mA
Output high voltage	V_{OH}	2.4		V	I_{OH} = -4.0 mA
Output current	I_{OZ}	-10.0	10.00	uA	0V<V_{OUT}<V_{DD}

10.0 AC CHARACTERISTICS

TA = 0° C to +70° C, V_{DD} = +5V ±5% load capacitance = 85 pF, operating at 8 MHz.

Symbol	Parameter	Min	Max	Unit
t1	DRQ high setup time to DMACLK high	20		ns
t2	HRQ active high delay from DMACLK rising edge	10	49	ns
t3	HLDA high setup time to DMACLK rising edge	15		ns
t4	AEN active high delay from DMACLK falling edge	14	69	ns
t5	AEN inactive low delay from DMACLK rising edge	15	74	ns
t6	SYSALE active high delay from DMACLK rising edge	10	54	ns
t7	SYSALE inactive low delay from DMACLK rising edge	14	69	ns
t8	$\overline{IOR}$ and $\overline{MEMR}$ active low delay from DMACLK rising edge	12	60	ns
t9	$\overline{IOW}$ and $\overline{MEMW}$ active low delay from DMACLK rising edge	12	60	ns
t10	$\overline{IOR}$ and $\overline{MEMR}$ inactive high delay from DMACLK rising edge	11	52	ns
t11	$\overline{IOW}$ and $\overline{MEMW}$ inactive high delay from DMACLK rising edge	11	52	ns
t12	$\overline{DACKEN}$ active low delay from DMACLK falling edge	13	63	ns
t13	$\overline{DACKEN}$ inactive high delay from DMACLK falling edge	10	49	ns
t14	TC active high delay from DMACLK falling edge	11	58	ns
t15	TC inactive low delay from DMACLK falling edge	13	68	ns
t16	DMARDY high setup time delay to DMACLK rising edge	10	2	ns
t17	ADDR active delay from AEN rising edge	2	18	ns
t18a	ADDR valid delay from DMACLK rising edge		178	ns
t19	ADDR float delay from DMACLK falling edge		83	ns
t20	DATA valid delay from $\overline{IOR}$ falling edge	14	68	ns
t21	DATA float delay from $\overline{IOR}$ rising edge	11	51	ns
t22	ADDR valid setup time to SYSALE inactive low	71		ns
t23a	SYSALE inactive low to ADDR valid hold time	121		ns
t24	ADDR valid delay from $\overline{RFSH}$ falling edge	15	78	ns
t25	ADDR float delay from $\overline{RFSH}$ rising edge	10	60	ns
t26	SYSALE active high from delay $\overline{RFSH}$ falling edge	6	29	ns
t27	SYSALE inactive low delay from $\overline{RFSH}$ rising edge	8	40	ns

10.0 AC CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Min	Max	Unit
t28	SYSALE active high delay from ALE rising edge	5	31	ns
t29	SYSALE inactive low delay from ALE falling edge	9	46	ns
t30	INTR (mstr) active high delay from IRQ rising edge	11	105	ns
t31	INTR (slave) active high from ALE rising edge	27	136	ns
t32	DATA valid delay from $\overline{\text{INTA}}$ falling edge	17	84	ns
t33	DATA float delay from $\overline{\text{INTA}}$ rising edge	9	45	ns
t34	RTCCS active low delay from ALE rising edge	13	66	ns
t35	RTCSS inactive high delay from ALE rising edge	9	46	ns
t36	OUT1 active high delay from TCLK falling edge	7	53	ns
t37	OUT1 inactive low delay from TCLK falling edge	10	63	ns
t38	DATA invalid time delay from DATA to $\overline{\text{IOW}}$ inactive high	30		ns
t39	DATA set-up time to $\overline{\text{IOW}}$ active low	30		ns

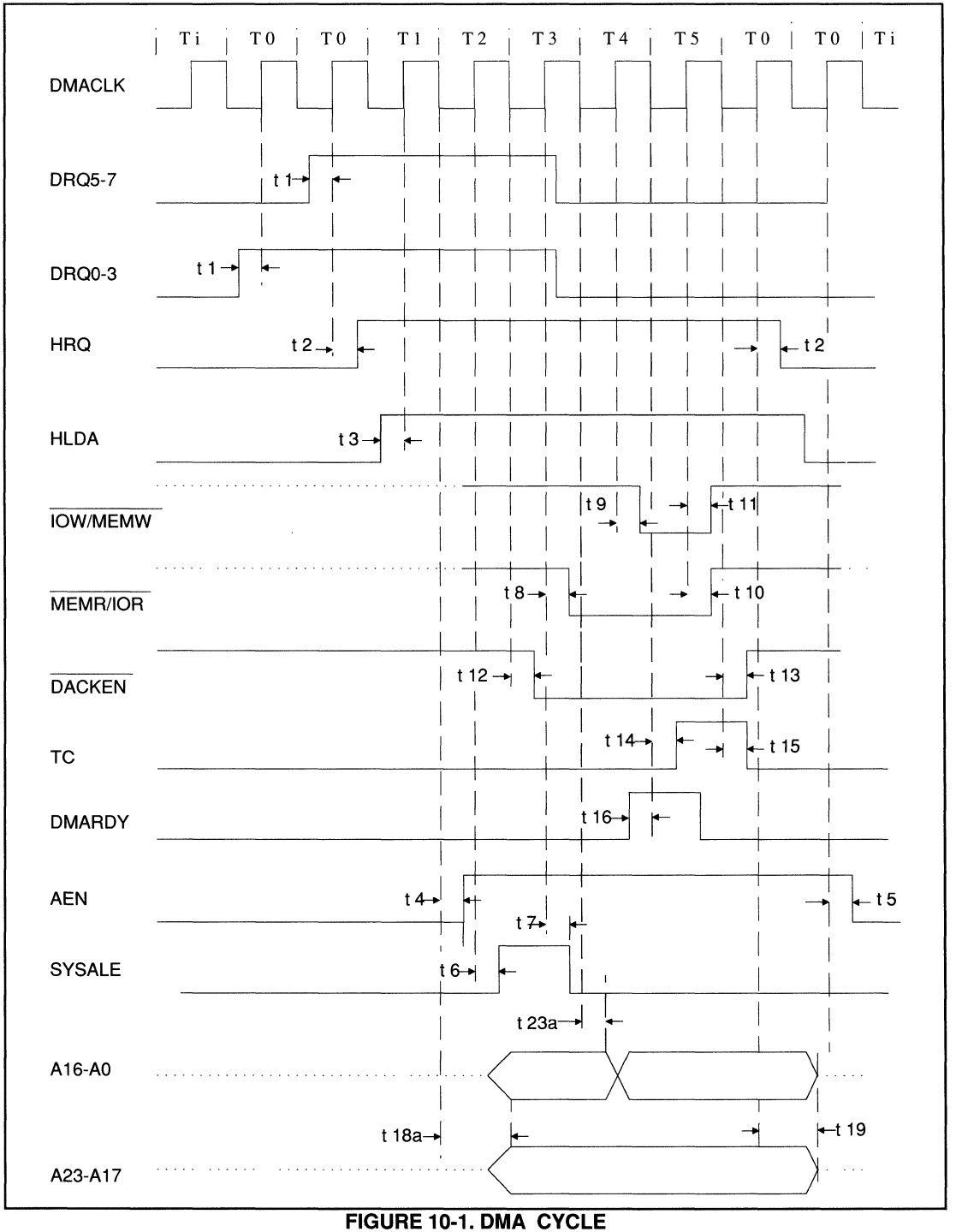


FIGURE 10-1. DMA CYCLE

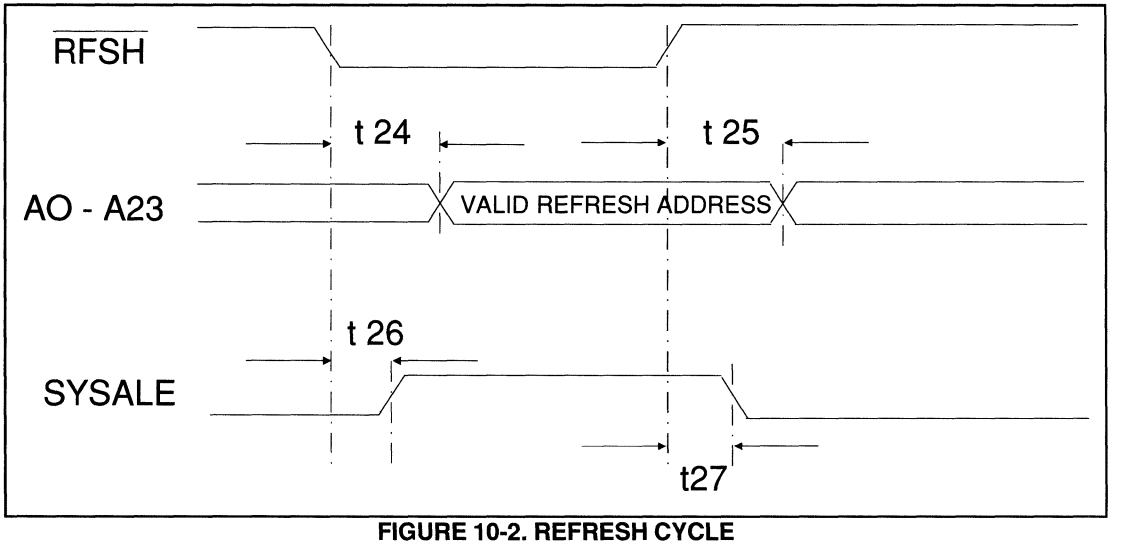


FIGURE 10-2. REFRESH CYCLE

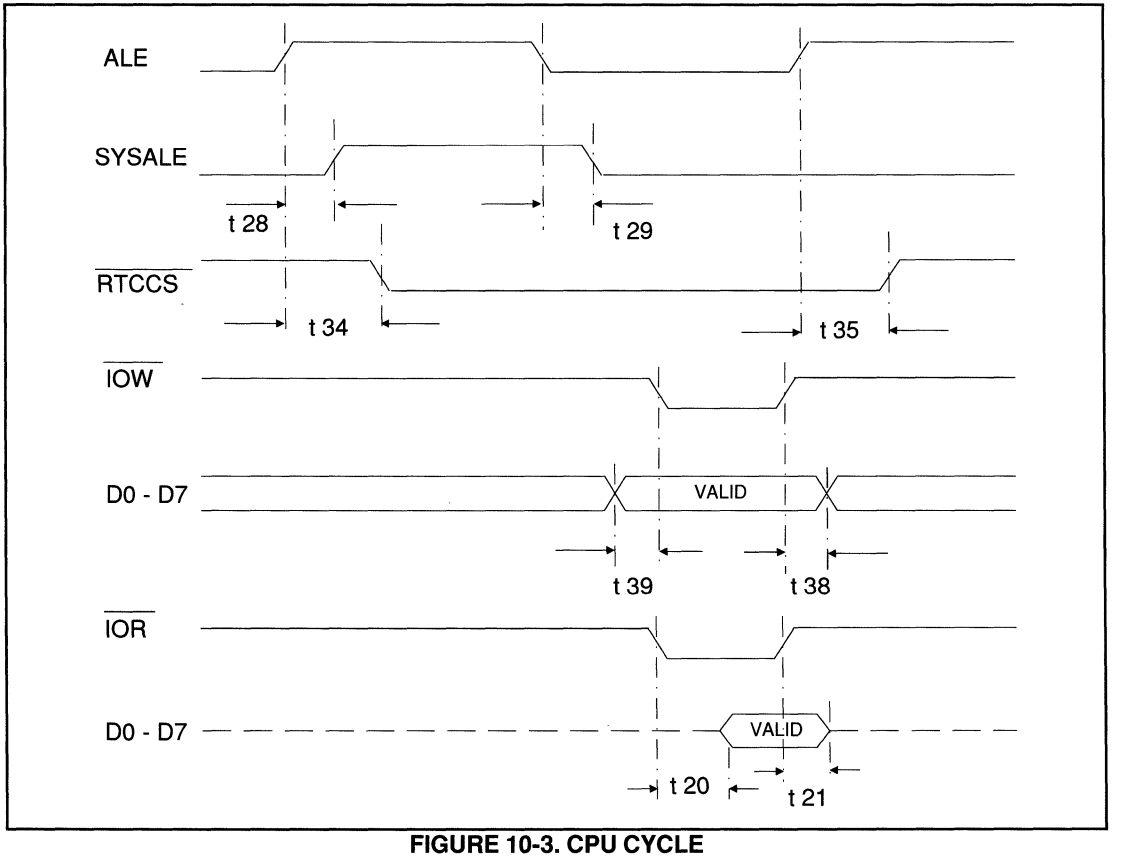


FIGURE 10-3. CPU CYCLE

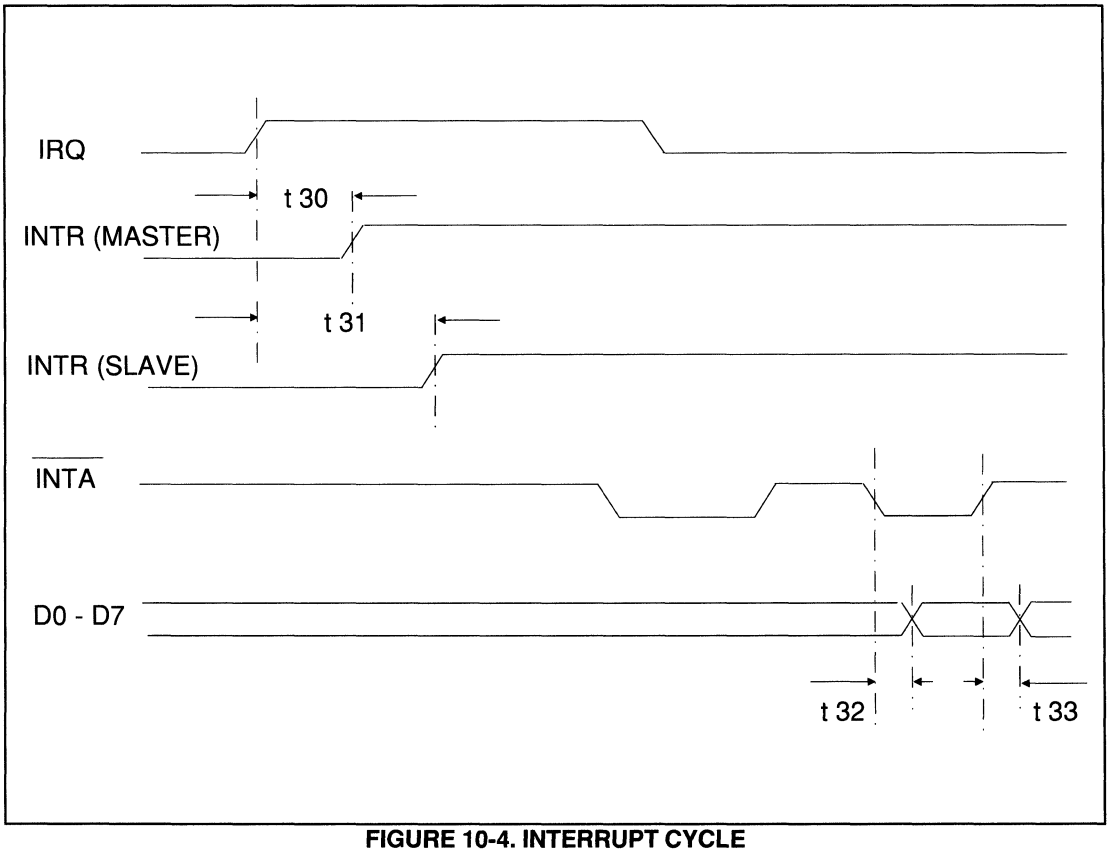


FIGURE 10-4. INTERRUPT CYCLE

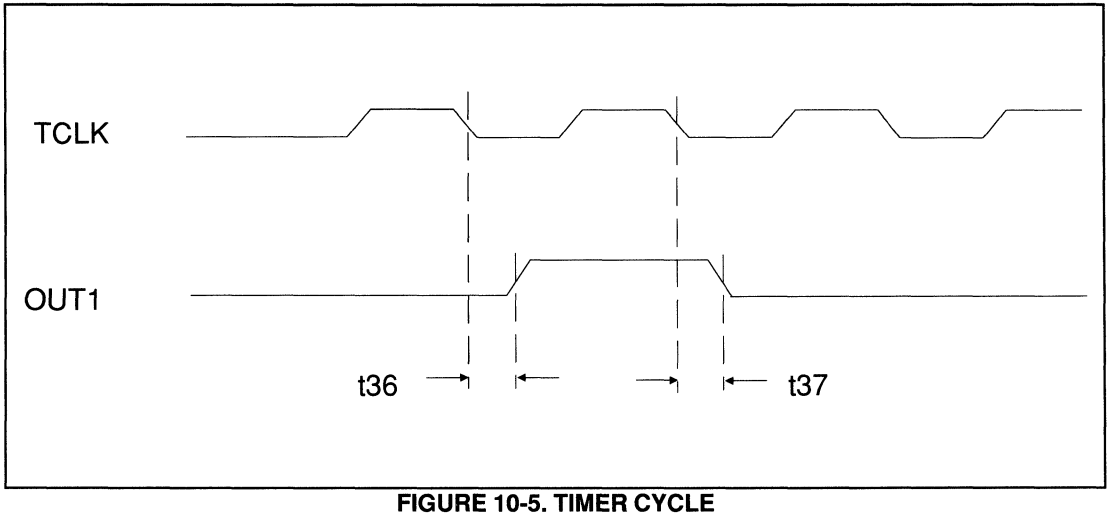


FIGURE 10-5. TIMER CYCLE

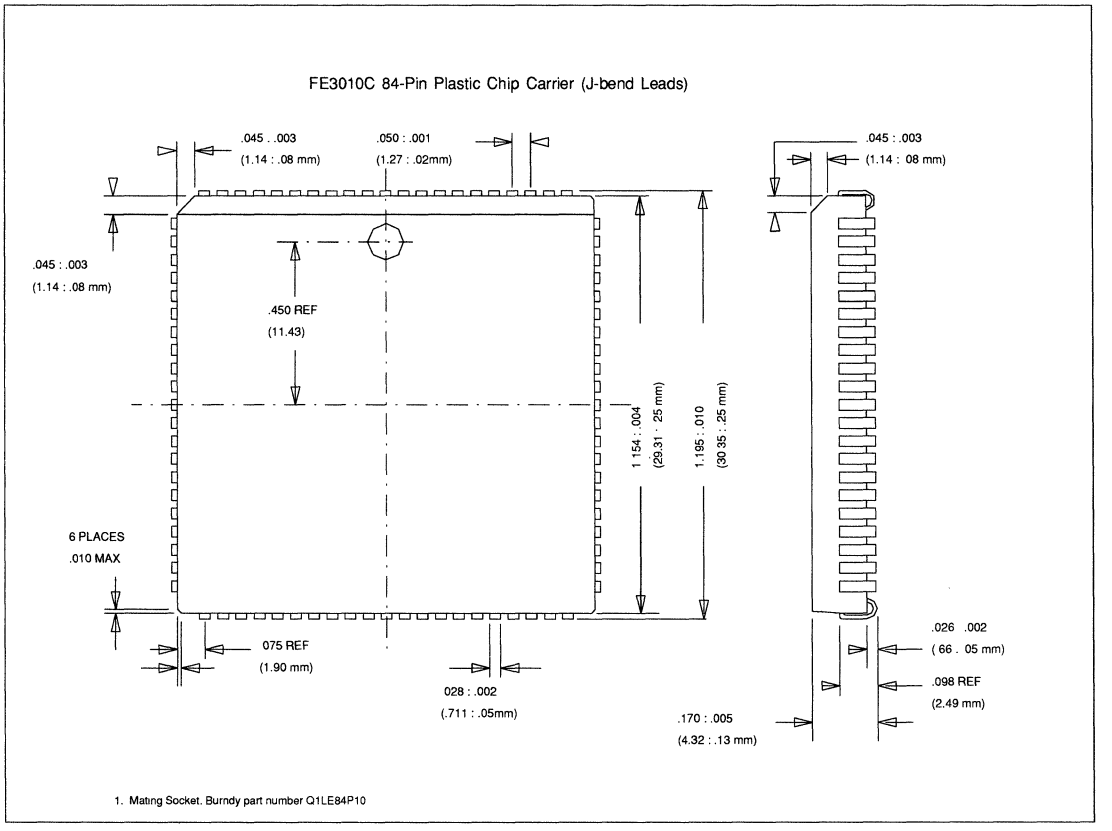


FIGURE 10-6. FE3010C 84-PIN PLCC PACKAGE DIMENSIONS

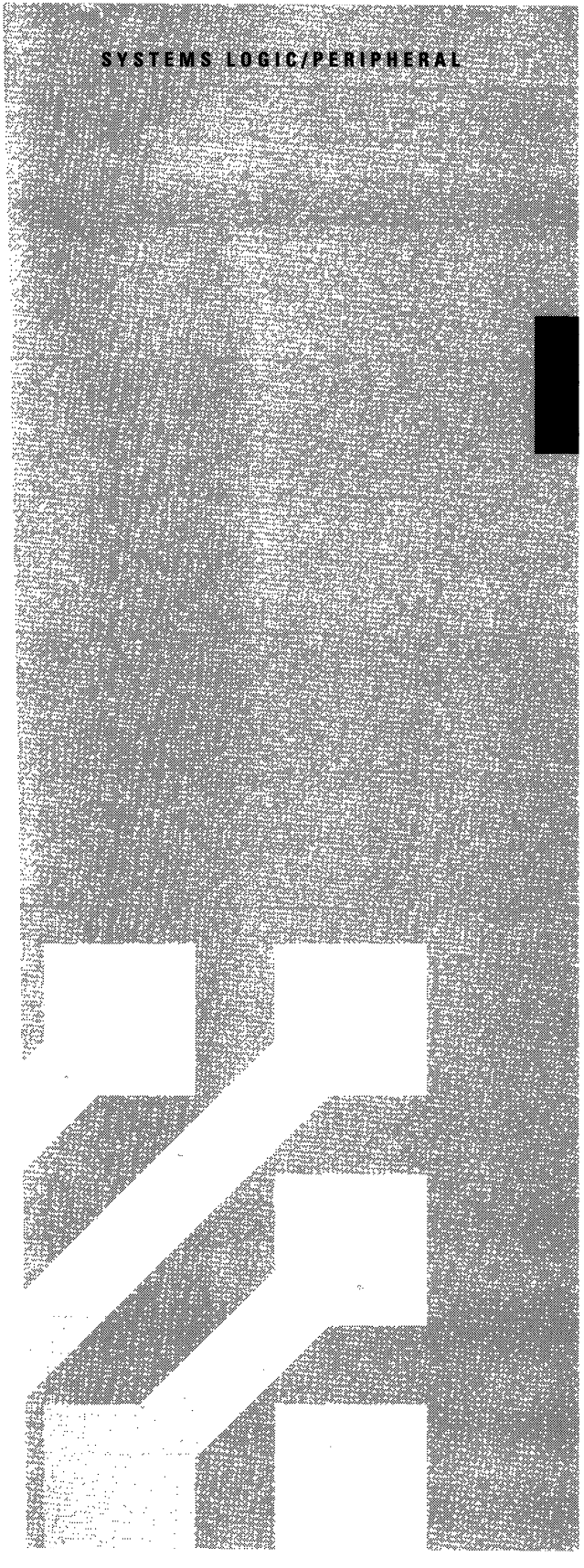
SYSTEMS LOGIC/PERIPHERAL

4

FE3021

Address Buffer and

Memory Controller



WESTERN DIGITAL

TABLE OF CONTENTS

4

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 DESCRIPTION

The FE3021 is a 16 MHz AT address buffer and memory controller in a 132-pin JEDEC package. Chip count is significantly reduced by integrating the memory controller, AT bus address buffers, and I/O into one chip. The memory controller is a high performance design, with programmable modes of operation. It controls page mode DRAM or static column DRAM. A maximum of 4 banks of DRAM can be controlled allowing a maximum of 8 MB of memory to be controlled by the FE3021. The DRAM bank locations are programmable on 128K byte boundries. One memory bank allows split addressing, so that one portion may be placed in conventional memory with the remainder in extended memory.

Additional features of the FE3600B chip set include EMS 4.0 support, on-chip address and control signal buffers for directly driving the AT bus, zero wait state access at 16 MHz using 100 ns DRAM with page mode access, generation of chip selects for floppy controller, 8042, 80287, and NMI, and mapping main and EGA BIOS into one physical PROM.

1.1 FEATURES

- ❑ Page mode DRAM access with interleaved memory banks
- ❑ Controls up to 4 banks (up to 8 MBytes) of memory
- ❑ On- chip RAS and CAS drivers for DRAM chips
- ❑ On- chip DRAM address multiplexer
- ❑ LIM standard EMS expanded memory hardware (supports EMS 4.0 multi-tasking)
- ❑ On- chip address and control signal buffers for directly driving AT bus
- ❑ Zero wait state access at 16 MHz using 100 ns DRAM with page mode access
- ❑ Generates chip selects for floppy controller, 8042, 80287, and NMI
- ❑ Generates programmable chip selects for four additional devices
- ❑ Maps system BIOS and EGA BIOS into one physical PROM
- ❑ "Hot" reset generation for quick 80286 switch from protected to real mode
- ❑ Fast Alternate Gate A20 generation
- ❑ 132 pin JEDEC plastic flat package

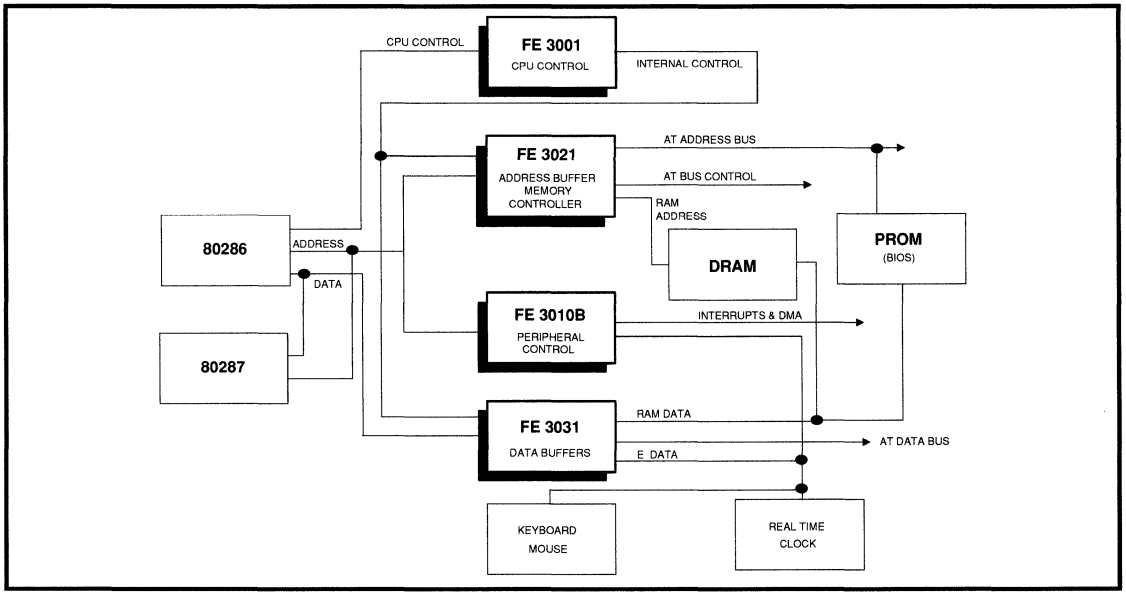


Figure 1. FE3600B Chip Set Functional Block Diagram

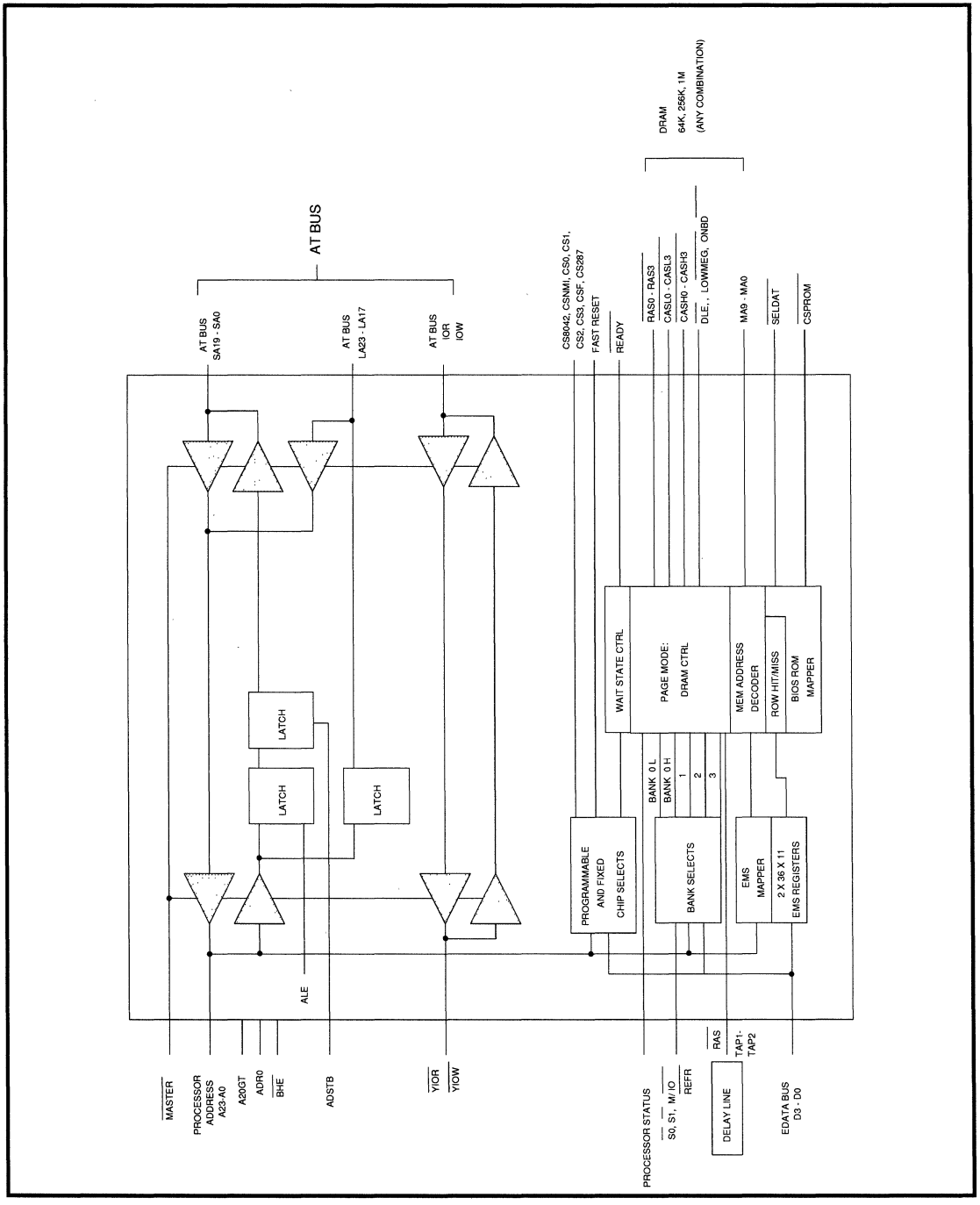


Figure 2. FE3021 Functional Block Diagram

1.2 INTRODUCTION

The FE3021 device is designed to reduce chip count, increase flexibility, and provide improved operating speed and functionality when used with the FE3001, FE3010B, and FE3031 devices to implement a low cost, high performance AT compatible computer.

Chip count is reduced by integrating the memory controller, AT bus address buffers, and I/O Management functions into one chip.

The memory controller is a high performance design, with programmable modes of operation. It controls page mode DRAM or static column DRAM.

Up to 4 banks of DRAM may be controlled. The DRAM bank locations are programmable on 128K byte boundaries. One memory bank allows split addressing, so that one portion may be placed in conventional memory with the remainder in extended memory, with an additional mode to allow copying BIOS code from ROM to RAM for faster execution.

A major function of the FE3021 is to generate chip select decodes for peripheral chips on the system board; for instance, the floppy controller, hard disk controller, serial, and parallel port chips. The floppy and hard disk chip selects may be disabled or may be enabled for either the primary or secondary address decode, as defined by IBM. Four programmable chip selects are available, for supporting serial, parallel, mouse, or other types of ports. Refer to Figure 2 for Pin assignment information and locations.

To reduce chip count and improve performance, particularly when an EGA or VGA graphics controller is placed on the system board, separate blocks of ROM may be mapped into a single physical ROM. For instance, the EGA BIOS and standard BIOS may be placed into the same pair of ROM chips or into a single 8-bit wide ROM. Besides reducing chip count, EGA operating speed will be improved, since EGA BIOS will be accessed 16 bits at a time. To improve BIOS performance, ROM code may be copied into RAM, and the BIOS ROM mapped out and replaced by RAM.

2.0 80286 INTERFACE

This interface port connects with the 80286 address lines and the 80286 bus status lines. By connecting directly to the 80286 and by duplicating a portion of the bus controller logic, early determination of memory or I/O accesses may be made, as well as whether the access will be 8 bits or 16 bits. Pins A23-A0 are normally inputs, receiving addresses from the 80286. When $\overline{\text{MASTER}}$ is asserted, these pins become outputs.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
74	A23	I/O	80286 Address Line
78	A22	I/O	" "
79	A21	I/O	" "
80	A20	I/O	" "
81	A19	I/O	" "
82	A18	I/O	" "
83	A17	I/O	" "
84	A16	I/O	" "
85	A15	I/O	" "
86	A14	I/O	" "
87	A13	I/O	" "
88	A12	I/O	" "
89	A11	I/O	" "
90	A10	I/O	" "
109	A9	I/O	" "
110	A8	I/O	" "
111	A7	I/O	" "
112	A6	I/O	" "
113	A5	I/O	" "
114	A4	I/O	" "
115	A3	I/O	" "
116	A2	I/O	" "
117	A1	I/O	" "
118	A0	I/O	" "
119	$\overline{\text{S0}}$	I	80286 Status Line
120	$\overline{\text{S1}}$	I	80286 Status Line
121	$\overline{\text{M/IO}}$	I	80286 Status Line
122	CPUCLK	I	80286 Clock
123	HLDA	I	80286 Hold Acknowledge Line
21	$\overline{\text{BHE}}$	I	80286 Byte High Enable

Table 1. 80286 Interface Pin Functions

3.0 DATA BUS INTERFACE

The data bus port is 4 bits wide, which should connect to the EDATA local data bus, and is used to access the internal FE3021 control registers. The upper 4 bits should be ignored when reading the control registers. Refer to Table 2 for pin assignments.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
17	EDATA3	I/O	Control Register Data Line
16	EDATA2	I/O	" "
15	EDATA1	I/O	" "
14	EDATA0	I/O	Control Register Data Line

Table 2. Data Bus Interface Pin Assignments

4.0 I/O CHIP SELECTS

This logic section generates chip selects for standard system board functions such as the 8042 keyboard controller, 80287 math coprocessor, floppy controller, and hard disk controller. It also generates chip selects for up to 4 additional I/O ports which may have programmable addresses and wait state characteristics. Refer to Table 3 for pin assignments.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
48	$\overline{CS0}$	O	Programmable Chip Select 0
47	$\overline{CS1}$	O	Programmable Chip Select 1
46	$\overline{CS2}$	O	Programmable Chip Select 2
45	$\overline{CS3}$	O	Programmable Chip Select 3 Or H. D. Control Chipselect
49	CSF	O	Floppy Disk Controller Chip Select Or Operation Or Configuration Register Select
60	$\overline{CS8042}$	O	8042 Keyboard Control Select
56	$\overline{CS287}$	O	80287 Coprocessor Select
20	$\overline{CSNMI}$	O	NMI Logic Chip Select
22	$\overline{CSPTB}$	O	Memory Parityand I/o Check Control Chip Select

Table 3. I/O Chip Selects Pin Assignments

5.0 I/O CONTROL

This logic section contains control logic for the I/O bus.

The IORDY signal will go low when generating wait states. For 12 MHz systems, this signal may be tied directly to the bus signal IOCHRDY. For 16 MHz or 20 MHz systems, this signal should be sent to the FE3001 directly. The IOCHRDY bus signal should be buffered through an open collector driver and wire-OR'ed with the IORDY signal. The IORDY pin will normally be at a high impedance state. When generating wait states, it will go low. When going from a low to a high state, the IORDY pin will be actively driven high for one processor clock time, then the output will tri-state. An external pullup resistor should be used to keep the IORDY signal high when the IORDY pin is at a high impedance state. The state of IORDY is sampled at the rising edge of $\overline{\text{RESET}}$; if IORDY is low at this time, the FE3021 will fetch data and instructions from the BIOS ROM 8 bits at a time over the EDATA bus, otherwise a 16 bit wide ROM on the MDATA bus is assumed.

Table 4 lists the data word size, I/O addresses, and chip selects generated for each variable port type.

The PORT 0, PORT 1, PORT 2, and PORT 3 addresses are fully programmable, with the choice of either using nine I/O addresses for decode, or masking the A8 address bit (for instance, for decoding dual serial ports). The LSB (A0) address is always ignored. The lower 2, 3, or 4 bits of the address may also be ignored so that 2, 4, 8, or 16 bytes may be allocated for the port.

All FE3021 control registers, except those used for EMS page mapping, are accessed by first writing eight times to address FFF00 (in an area allocated for ROM BIOS). Any memory access outside of the ROM BIOS address space, either data access or instruction fetch, will abort the unlocking process. Once unlocked, memory accesses outside of the ROM BIOS area may be made without affecting the unlocked state. When unlocked, the address space from FFF01 to FFFFE becomes register controls for the FE3021 device. The controls are locked again by reading location FFFFF. This access method guarantees that all control register changes will be made through the BIOS.

PIN NUMBER	PIN NAME	I/O	FUNCTION
127	IORDY	I/O	Ready Line, modified Open Drain, Input At Reset Time For 8-Bit ROM Sizing
40	$\overline{\text{SELDAT}}$	O	Direction Of Data Tranceiver Data To EDATA Bus
8	$\overline{\text{IOR}}$	I/O	System I/O Read Command Signal, Drives Expansion Bus. An Input In Master Mode.
9	$\overline{\text{IOW}}$	I/O	System I/o Write Command Signal, Drives Expansion Bus. An Input In Master Mode.
10	$\overline{\text{YMEMR}}$	I	Ungated System Memory Read Command Signal From FE3001
11	$\overline{\text{YMEMW}}$	I	Ungated System Memory Write Command Signal From FE3001

Table 4. I/O Control Pin Functions

PIN NUMBER	MNEMONIC	I/O	FUNCTION
53	ADSTB	I	Address Strobe From FE3001 And FE3010B.
12	$\overline{\text{YIOR}}$	I/O	Ungated I/O Read Strobe From FE3001, An Output In Master Mode.
13	$\overline{\text{YIOW}}$	I/O	Ungated I/O Write Strobe From FE3001, output In Master Mode.
19	$\overline{\text{FRES}}$	I/O	"HOT" Reset Output
25	$\overline{\text{LOMEG}}$	O	To FE3031 Memory Strobe Gating
28	$\overline{\text{RESET}}$	I	Master Reset For FE3021
52	$\overline{\text{MASTER}}$	I	Bus Master Signal From AT Bus
54	A20GT	I	From 8042. When High, A20 Is Ungated
57	$\overline{\text{ONBD}}$	O	To FE3001. Indicates High Speed On-Board Access
59	ADDR19	O	AT Bus SA19
61	ADDR 18	O	AT Bus SA18
62	ADDR 17	O	AT Bus SA17
64	ADDR 16	I/O	AT Bus SA16
65	ADDR 15	I/O	AT Bus SA15
66	ADDR 14	I/O	AT Bus SA14
68	ADDR 13	I/O	AT Bus SA13
69	ADDR 12	I/O	AT Bus SA12
72	ADDR 11	I/O	AT Bus SA11
73	ADDR 10	I/O	AT Bus SA10
75	ADDR 9	I/O	AT Bus SA 9
94	ADDR8	I/O	AT Bus SA8
96	ADDR7	I/O	AT Bus SA7
97	ADDR6	I/O	AT Bus SA6
98	ADDR5	I/O	AT Bus SA5
100	ADDR4	I/O	AT Bus SA4
101	ADDR3	I/O	AT Bus SA3
104	ADDR2	I/O	AT Bus SA2
106	ADDR1	I/O	AT Bus SA1
105	ADDR0	I/O	AT Bus SA0
63	LA23	I/O	AT Bus LA23
70	LA22	I/O	AT Bus LA22
71	LA21	I/O	AT Bus LA21
93	LA20	I/O	AT Bus LA20
95	LA19	I/O	AT Bus LA19
102	LA18	I/O	AT Bus LA18
103	LA17	I/O	AT Bus LA17

Table 4. I/O Control Pin Functions (Continued)

A Version Number register provides information on the version of the FE3021 chip. It also contains a bit which toggles between '0' and '1' when the register is read, which provides indication that the register set has been unlocked.

VERSION NUMBER

FFF01	**X**	**X**	**X**	**X**		**VER**		**T**
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

T : toggles between 0 and 1 with every read access of the Version Number register.

VER : 000 when T=0
101 when T=1 for Early Production Version
100 when T=1 for Production Version

System board devices may be located on the EDATA bus rather than on the I/O expansion slot DATA bus. The $\overline{\text{SELDAT}}$ signal which controls the DATA to EDATA bus direction is affected by the two port location registers. This option is available for peripheral devices which cannot directly drive the high current I/O slot DATA bus. Note, however, that DMA transfers cannot be made to devices on the EDATA bus.

The $\overline{\text{SELDAT}}$ signal is active (low) when $\overline{\text{IOR}}$ is active and address bits A8 and A9 are low, or the PORTS LOCATION register indicates that an addressed port is on the EDATA bus. The $\overline{\text{SELDAT}}$ signal is also low when $\overline{\text{MEMR}}$ is active and the **8-bit** BIOS is being accessed.

PORTS LOCATION REGISTER

FFF06	X	X	X	X	A	B	C	D
	7	6	5	4	3	2	1	0

A = 0	Port 0 On DATA Bus
A = 1	Port 0 On EDATA Bus
B = 0	Port 1 On DATA Bus
B = 1	Port 1 On EDATA Bus
C = 0	Port 2 On DATA Bus
C = 1	Port 2 On EDATA Bus
D = 0	Port 3 On DATA Bus
D = 1	Port 3 On EDATA Bus

THE PORTS LOCATION REGISTER IS CLEARED BY A MASTER RESET.

HOT RESET REGISTER

FFF07	X	X	X	X	0/1	DA	A	H
	7	6	5	4	3	2	1	0

THE HOT RESET REGISTER IS CLEARED BY A MASTER RESET.

Register FFF07 is used to generate a hot reset to the processor or to generate an alternate A20 gate. The state of the A bit is OR'ed with the A20GT pin. If either the A bit is set or the A20GT pin is high, the A20 line is undisturbed. If both are low, then the A20 line is gated low. If the DA bit is set, then a CPU reset generated by the keyboard controller will reset the A bit; the A bit will not be reset by a hot reset generated by the FE3021. A hot reset is generated by changing the H bit from a '0' to a '1'. 131 clocks after the trailing edge of the $\overline{\text{MEMW}}$ strobe, the $\overline{\text{FRES}}$ pin will be pulled low. The reset pulse lasts for 32 clocks, then the $\overline{\text{FRES}}$ pin is actively pulled high for one clock cycle, then is tri-stated. If the $\overline{\text{FRES}}$ pin is pulled low externally (e.g. if wire-OR'ed with the 8042 CPU reset line), then the internal FE3021 registers will relock. If the $\overline{\text{FRES}}$ pin is not used, then it should be pulled up externally or the FE3021 registers will not unlock.

Bit 3 is a writeable bit which is not currently used.

ENABLE PORTS REGISTER

	7	6	5	4	3	2	1	0
FFF10	X	X	X	X	EN3	EN2	EN1	EN0

THE ENABLE PORTS REGISTER IS CLEARED BY A MASTER RESET.

The programmable PORT 0, PORT 1, PORT 2, and PORT 3 chip selects are enabled with the Enable Ports register. If the Enable bit is 0, the port chip select bit will always be at an inactive (high) state. All four ports are disabled after master reset. EN3 enables $\overline{CS3}$ only when $\overline{CS3}$ is a programmed chip select. When $\overline{CS3}$ is a HDC chip select, $\overline{CS3}$ is enabled by register FFF49, bit 1.

For ports 0, 1, and 2, the access will have the default wait states: 1 wait state for 16 bit accesses and 4 wait states for 8 bit accesses, with the wait states set from the FE3001. The selected chip must generate $\overline{IOCS16}$ if it is a 16 bit peripheral.

PORT 3 CONTROL REGISTER

	7	6	5	4	3	2	1	0
FFF08	X	X	X	X	WS		WSE	OB

THE PORT 3 CONTROL REGISTER IS CLEARED BY A MASTER RESET.

WS	HDC DATA PORT HIGH SPEED WAIT STATES
00	1
01	2
10	3
11	4

0B	$\overline{CS3}$ WAIT STATES
0	Default (slow)
1	High Speed Hard Disk Controller

WSE:	HIGH SPEED HDC WAIT STATE ENABLE
0:	High Speed HDC Wait States Set By FE3001
1:	High Speed HDC Wait States Set By WS Field

For port 3, the access will normally have the default wait states but may also be programmed to have high speed wait state timing when $\overline{CS3}$ is programmed as a hard disk chip select and the on-board 16-bit hard disk controller is capable of high speed access. When the high speed disk controller configuration is used, the WSE and OB fields should be set to '1', and the WS field will set the number of high speed wait states, timed from the CPUCLK, rather than from SYSCLK. The other disk controller ports will always be accessed at low speed.

When 0B is set to a 1, the FE3021 will generate the ONBD signal to the FE3001 during HDC accesses through port 3. The FE3001 will provide the same number of wait states it does for on-board memory. If it is desired, the number of wait states for the HDC can be extended using the WS and WSE fields.

When implementing a high speed disk controller port, it is necessary to provide a separate address path for the hard disk controller. The HDC receives ungated I/O read and write strobes at the full CPU speed. The following schematic illustrates the required connections.

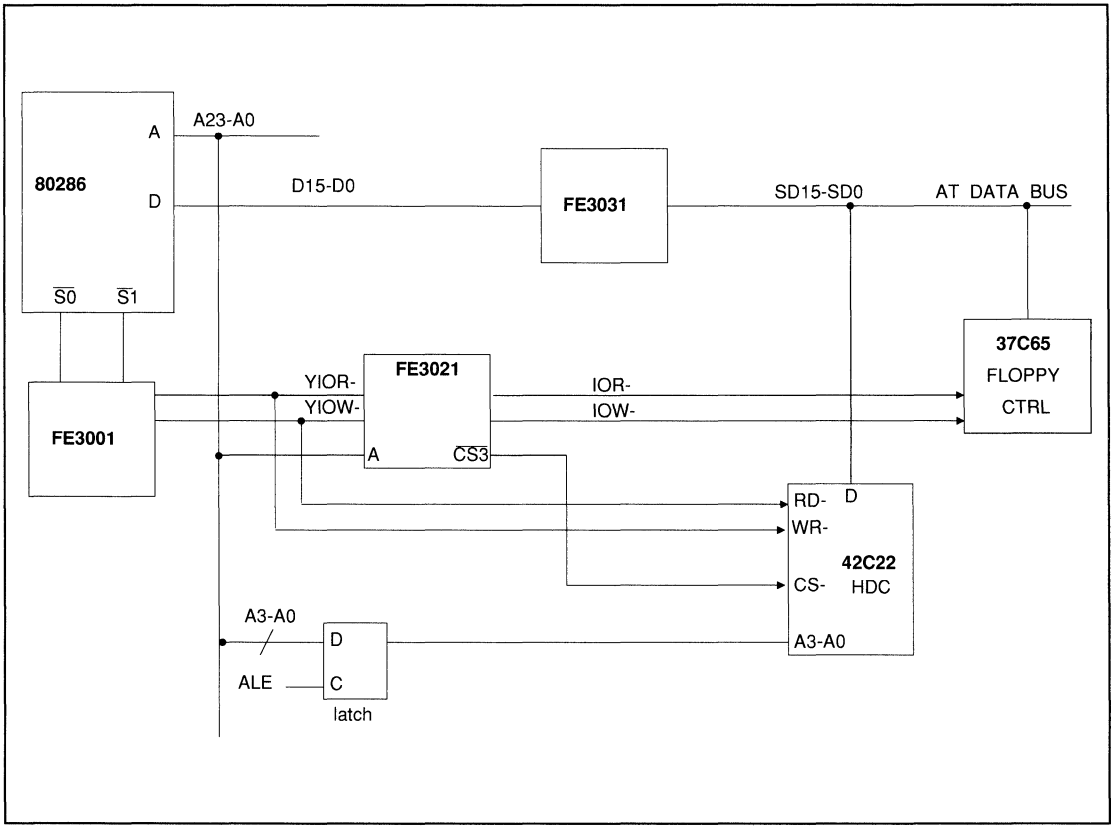


Figure 3. High Speed HDC Configuration

FFF09
FFF11
FFF19
FFF21

X	X	X	X	O	U	LMASK	
7	6	5	4	3	2	1	0

LMASK	ADDRESS BITS COMPARED									
00	A9	A8	A7	A6	A5	A4	A3	A2	A1	X
01	A9	A8	A7	A6	A5	A4	A3	A2	X	X
10	A9	A8	A7	A6	A5	A4	A3	X	X	X
11	A9	A8	A7	A6	A5	A4	X	X	X	X

U = 0 : INCLUDE A8 IN ADDRESS COMPARISON

LMASK	ADDRESS BITS COMPARED									
00	A9	X	A7	A6	A5	A4	A3	A2	A1	X
01	A9	X	A7	A6	A5	A4	A3	A2	X	X
10	A9	X	A7	A6	A5	A4	A3	X	X	X
11	A9	X	A7	A6	A5	A4	X	X	X	X

U = 1 : IGNORE A8 IN ADDRESS COMPARISON

THE PORT ADDRESS MASK REGISTER IS CLEARED BY A MASTER RESET.

PORT	PORT CONTROL REGISTER ADDRESS
0	FFF09
1	FFF11
2	FFF19
3	FFF21

NOTE: Bit 3 is not writeable and is always '0'.

PORT ADDR - LOWER MSB

FFF0A
FFF12
FFF1A
FFF22

X	X	X	X	X	X	A9	A8
7	6	5	4	3	2	1	0

PORT ADDR - UPPER LSB

FFF0B
FFF13
FFF1B
FFF23

X	X	X	X	A7	A6	A5	A4
7	6	5	4	3	2	1	0

PORT ADDR - LOWER LSB

FFF0C
FFF14
FFF1C
FFF24

X	X	X	X	A3	A2	A1	0
7	6	5	4	3	2	1	0

PORT	PORT I/O ADDRESS REGISTERS		
	A9-A8	A7-A4	A3-A0
0	FFF0A	FFF0B	FFF0C
1	FFF12	FFF13	FFF14
2	FFF1A	FFF1B	FFF1C
3	FFF22	FFF23	FFF24

The PORT I/O ADDRESS registers for all four ports are set to all zeros by a master reset.

The following tables list the I/O addresses and chip selects generated for each fixed port type. The chip selects are not gated with IOR or IOW. The CSNMI signal is decoded for both even and odd addresses, so that access may be made to the FE3001 control register at address 073.

The floppy controller operations register select, configuration register select, and floppy disk controller chip select may be generated from the CSF pin and the ADDR2 and ADDR1 lines.

	ADDR2	ADDR1	CSF
OPERATIONS REGISTER ACCESS	0	X	1
CONFIG REGISTER ACCESS	1	1	1
FLOPPY CHIP SELECT ACTIVE	X	0	1

PORT	BIT SIZE	I/O ADDRESS	ACTIVE PIN	FUNCTION
FLOPPY	8	3F2 372	CSF	FDC Operation Select. 3F2 Is Primary Address, 372 Is Secondary
	8	3F4-3F5 374-375	CSF	3F4-3F5 Are Primary Addresses, 374-375 Are Secondary.
	8	3F6 376	$\overline{CS3}$*	Hard Disk Controller Chip Select. 3F6 Is Primary Address, 376 Is Secondary.
	8	3F7 377	CSF $\overline{CS3}$*	$\overline{CS3}$ And CSF Pins Will Be Asserted. 3F7 Is Primary Address, 377 Is Secondary.
80287	8	0E0-0FF	$\overline{CS287}$	80287 Chip Select.
8042	8	060-06E (EVEN)	$\overline{CS8042}$	8042 Chip Select.
NMI LOGIC	8	070-07F	$\overline{CSNMI}$	Real Time Clock And NMI Logic Select
PARITY CHECK	8	061-06F (ODD)	$\overline{CSPTB}$	Parity Check Select And Port B Decode . External Logic Must Separate The Signals.
HARD DISK	16	1F0 170	$\overline{CS3}$ *	HDC Chip Select - Data Port Access. 1F0 Is Primary Address, 170 Is Secondary
	8	1F1-1F7 171-177	$\overline{CS3}$	HDC Chip Select - TASK FILE. 1F1-1F7 Are Primary Addresses, 171-177 Are Secondary.

Table 5. I/O Addresses/Chip Selects for Fixed Ports

* WHEN $\overline{CS3}$ PIN IS PROGRAMMED AS HDC CHIP SELECT .

PRIMARY / SECONDARY PORT FUNCTION SELECT

FFF49	X	X	X	X	DH	PS	H	F
	7	6	5	4	3	2	1	0

DH=0: $\overline{CS3}$ pin will respond to address programmed by FFF22-FFF24
DH=1: $\overline{CS3}$ pin will respond to hard disk addresses
PS=0: Primary hard disk and floppy disk address
PS=1: Secondary hard disk and floppy disk address
H=0: On-board hard disk controller enabled
H=1: Disable on-board hard disk controller
F=0: On-board floppy disk controller enabled
F=1: Disable on-board floppy disk controller

DH, PS, H, AND F ARE CLEARED TO '0' BY MASTER RESET

NOTE: For early production version (ID Register = 0000, 1011) bits 2 - 0 had different definitions:

Bit 2 = 0: Enable CSF Output
Bit 1 = 0: Primary Hard Disk Address
Bit 0 = 0: Primary Floppy Disk Address

4

6.0 MEMORY CONTROL

Four RAS pins are available for controlling up to four 16 bit wide banks of system board RAM. Eight CAS pins control the low and high bytes of each bank. During a refresh cycle, all RAS signals will be active (ignoring the RAM configuration register FFF57) and CAS signals will stay inactive.

The RAS and CAS lines drive the DRAM array directly.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
128	$\overline{\text{RAS0}}$	O	RAS Signal For DRAM Memory Bank 0
129	$\overline{\text{RAS1}}$	O	RAS Signal For DRAM Memory Bank 1
130	$\overline{\text{RAS2}}$	O	RAS Signal For DRAM Memory Bank 2
132	$\overline{\text{RAS3}}$	O	RAS Signal For DRAM Memory Bank 3
125	$\overline{\text{CASL0}}$	O	CAS Signal For DRAM Memory Bank 0, Low Byte
126	$\overline{\text{CASL1}}$	O	CAS Signal For DRAM Memory Bank 1, Low Byte
2	$\overline{\text{CASL2}}$	O	CAS Signal For DRAM Memory Bank 2, Low Byte
3	$\overline{\text{CASL3}}$	O	CAS Signal For DRAM Memory Bank 3, Low Byte
4	$\overline{\text{CASH0}}$	O	CAS Signal For DRAM Memory Bank 0, High Byte
5	$\overline{\text{CASH1}}$	O	CAS Signal For DRAM Memory Bank 1, High Byte
6	$\overline{\text{CASH2}}$	O	CAS Signal For DRAM Memory Bank 2, High Byte
131	$\overline{\text{CASH3}}$	O	CAS Signal For DRAM Memory Bank 3, High Byte
18	$\overline{\text{REFR}}$	I	Memory Refresh Signal
43	$\overline{\text{CSPROM}}$	O	BIOS PROM Select
26	$\overline{\text{TAP2}}$	I	Second Tap Output Of RAS Delay Line
44	$\overline{\text{TAP1}}$	I	First Tap Output Of RAS Delay Line
58	$\overline{\text{RAS}}$	O	To RAS Delay Line Input
23	$\overline{\text{DBLE}}$	O	To FE3031 Memory Data Bus Latch Enable
24	ADR0	I	From FE3001 Byte Conversion

Table 6. Memory Control Pin Information

7.0 MEMORY ADDRESS MULTIPLEXER

The memory address multiplexer generates the row and column addresses for the DRAM. The memory address multiplexer outputs should be buffered by external drivers when driving the memory array.

The memory address multiplexer supports three sizes of DRAM: 64K, 256K, and 1 MB. The three sizes of DRAM's may be intermixed in any order.

The memory address multiplexer is designed so that SIMM mounted DRAM's of the three different sizes may be inserted into SIMM sockets without the need to change board jumpers.

4

PIN NUMBER	MNEMONIC	I/O	FUNCTION
31	RA0	O	Memory Address Multiplexer Output Bit 0 (LSB)
32	RA1	O	Memory Address Multiplexer Output Bit 1
33	RA2	O	Memory Address Multiplexer Output Bit 2
34	RA3	O	Memory Address Multiplexer Output Bit 3
35	RA4	O	Memory Address Multiplexer Output Bit 4
36	RA5	O	Memory Address Multiplexer Output Bit 5
37	RA6	O	Memory Address Multiplexer Output Bit 6
38	RA7	O	Memory Address Multiplexer Output Bit 7
39	RA8	O	Memory Address Multiplexer Output Bit 8
41	RA9	O	Memory Address Multiplexer Output Bit 9 (MSB)

Table 7. Memory Address Multiplexer Outputs

64K DRAM ADDRESS MULTIPLEXER CONFIGURATION											
Memory Mode		MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Independent Non Page Mode	RAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
	CAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A9
Independent Page Mode	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A9
	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
2 Way Intlv Page Mode	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A17
	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
4 Way Intlv Page Mode	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A18	A17
	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
256K DRAM ADDRESS MULTIPLEXER CONFIGURATION											
Independent Non Page Mode	RAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
	CAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A10	A17
Independent Page Mode	RAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A10	A17
	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
2 Way Intlv Page Mode	RAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A19	A17
	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
4 Way Intlv Page Mode	RAS	(A20)	A18	A16	A15	A14	A13	A12	A20	A19	A17
	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1

Table 8. Address Multiplexer Configurations

1 MBIT DRAM ADDRESS MULTIPLEXER CONFIGURATION										
Independent	RAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
Non Page Mode	CAS	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
Independent	RAS	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
Page Mode	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
2 Way Intlv	RAS	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17
Page Mode	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
4 Way Intlv	RAS	A20	A18	A16	A15	A14	A13	A22	A21	A19	A17
Page Mode	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
REFRESH ADDRESS - ALL DRAM SIZES											
		A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Table 8. Address Multiplexer Configurations (Continued)

NOTE: Addresses in parentheses not used by DRAM.

SYSTEM BOARD ROM WAIT STATE CONTROL REGISTER

FFF50

X	X	X	X	RWS		0	RWSE
7	6	5	4	3	2	1	0

RWS	HIGH SPEED WAIT STATE
00 *	1
01	2
10	3
11	4

RWSE=1: Enables RWS, otherwise on-board ROM and RAM Wait States will be set by FE3001.

THIS REGISTER IS CLEARED TO ZERO BY MASTER RESET.

The FE3021 can extend the number of processor wait states for an on-board BIOS access by setting the RWSE bit to a '1'. The number of wait states will then be determined by the value of the RWS field. If the RWSE bit is set to a '0', the number of wait states for an on-board BIOS access is controlled by the FE3001.

The ability to add wait states for BIOS accesses is important for a 16-bit BIOS because the on-board memory read wait states programmed into the FE3001 apply to both on-board BIOS and on-board DRAM. That value will be programmed to optimize DRAM access time (typically zero wait states for page mode operations). This very fast access time will likely be too quick for BIOS ROMs and can therefore be extended for BIOS accesses by setting the RWSE bit.

Bit 1 is used for diagnostic purposes and should remain '0'.

The system BIOS address space may be from F0000 to FFFFF or E0000 to FFFFF. If the EGA BIOS is to be mapped, then the BIOS ROM chip select is also active when the region from C0000 to C3FFF or C0000 to C7FFF is addressed. The address output onto the expansion bus will be automatically translated. The BIOS PROM size and number of wait states will then apply to both the system BIOS region F0000-FFFFF and C0000-C3FFF.

The BIOS EPROM size may either be 8 bits or 16 bits. The EPROM size is determined at reset time, and is signaled by the IORDY line. If the IORDY line is high at the trailing edge of master reset, then the EPROM size is set to 16 bits. If the IORDY line is low at the trailing edge of master reset, then the EPROM size is set to 8 bits. No external logic is required for the 16 bit EPROM size. To select the 8 bit EPROM size, the IORDY line should be pulled low by a master reset. The MDATA bus is used for 16 bit EPROM's while the EDATA bus is used for 8 bit EPROM's.

The $\overline{\text{CSPROM}}$ signal is only active when $\overline{\text{MEMR}}$ is active.

MEMORY ADDRESS RANGE FOR ACTIVE CSPROM	FUNCTION
0F0000-0FFFFF FF0000-FFFFFF	BIOS SIZE = 64K (DEFAULT)
0E0000-0FFFFF FE0000-FFFFFF	BIOS SIZE = 128K
0C0000-0C3FFF	16K EGA BIOS Mapping Enabled Addresses Translated To 0F8000-0FBFFF Or 0F0000 - 0F3FFF
0C0000-0C7FFF	32K EGA BIOS Mapping Enabled Addresses Translated To 0F8000-0FFFFF Or 0F0000 - 0F7FFF * A16 is ignored in early production version (0000, 1011)

EPROM / RAM MAP CONTROL REGISTER

FFF51

X	X	X	X	EGA		MS	PS
7	6	5	4	3	2	1	0

FFF52

X	X	X	X	XLA	'0'	MLA	FAD
7	6	5	4	3	2	1	0

EGA=00 MS=X: No EGA mapping.
EGA=01 MS=0: 16K EGA map. C0000 - C3FFF mapped to F8000 - FBFFF
MS=1: 16K EGA map. C0000 - C3FFF mapped to F0000 - F3FFF
EGA=10 MS=0: 32K VGA map. C0000 - C7FFF mapped to F8000 - FFFFF
MS=1: 32K VGA map. C0000 - C7FFF mapped to F0000 - F7FFF
PS = 0: PROM chip select will be active when address is 0F0000-0FFFFF or FF0000-FFFFFF, for 64K of BIOS. Default case after master reset.
1: PROM chip select will be active when address is 0E0000-0FFFFF or FE0000-FFFFFF, for 128K of BIOS.

THIS REGISTER IS CLEARED TO ZERO BY A MASTER RESET.

ALL BITS ARE CLEARED BY MASTER RESET

XLA=0: LA23 - LA17 low speed timing
XLA=1: LA23 - LA17 high speed timing

MLA=0: LA23 - LA17 latches are transparent during refresh cycles
MLA=1: LA23 - LA17 gated to '0' during refresh cycles

FAD=0: 3 wait state EMS misses
FAD=1: 2 wait state EMS misses

Register FFF52 controls logic for various speed enhancement and diagnostic modes. The XLA bit controls the timing of the LA23 - LA17 signals. Use of this bit can affect compatibility of plug-in bus cards.

When XLA=0, LA23 - LA17 signals are generated by latching the processor addresses by active $\overline{S0}$ or $\overline{S1}$. The LA23 - LA17 latches become transparent when a $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, or $\overline{IOW}$ strobe occurs. This bit should be 0 when running at 8 MHz, when the FE3001 is using the low speed clock.

When XLA=1, LA23 - LA17 signals are latched by active $\overline{S0}$ or $\overline{S1}$, but do not become transparent again until two CPU clocks after $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, or $\overline{IOW}$. This delay provides proper 8 MHz bus emulation of the LA23 - LA17 signals when the processor is running at 16 MHz.

The MLA bit is provided for diagnostic purposes. Bit 2 of register FFF52 is reserved and must be '0'.

The FAD bit can be used to enhance EMS performance for lower speed systems. EMS misses are normally three wait states, which are necessary for 16/20 MHz operation. At 12 MHz and below, EMS misses only need to be two wait states. This bit can be used for the non-page or page mode 2 operation at 12 MHz or below. This bit should remain 0 for page mode 3 or 16/20 MHz operation.

A single contiguous block of memory may be write protected, so that when BIOS ROM is copied into RAM, the RAM copy will not be inadvertently altered. Write protection is accomplished by not asserting CAS when MEMW is active.

Master reset clears the upper address boundary registers and presets the lower address boundary registers, which disables write protection. Write protection is enabled on the address range where the RAM address is less than or equal to the upper address boundary as well as greater than or equal to the lower address boundary.

RAM WRITE PROTECT
UPPER ADDRESS BOUNDARY

	7	6	5	4	3	2	1	0
FFF53	X	X	X	X	'1'	A18	A17	A16

THIS REGISTER IS CLEARED BY MASTER RESET

RAM WRITE PROTECT
LOWER ADDRESS BOUNDARY

	7	6	5	4	3	2	1	0
FFF55	X	X	X	X	'1'	A18	A17	A16

THIS REGISTER IS PRESET TO ALL '1' BY MASTER RESET

Write protection is programmable on 64K boundaries, and the write protection boundaries must be equal to or above 80000H and equal to or below FFFFFH. Write protection will not affect EMS writing even if the EMS window address range is covered by write protection boundaries. This allows protection of BIOS code copied into RAM without affecting operation of EMS.

The memory banks may be programmed to various sizes on 128K boundaries, except the upper split of bank 0, which is programmable on 64K boundaries.

A pair of window registers determines the address range for each memory bank. This allows the banks to be positioned at varying points and in different order than the bank number. If one bank of memory is defective, it can be disabled and the other banks can be programmed to replace it.

NOTE: For the early production version of the FE3021 (version reg=0000, 1011), bank 0 has three pairs of window registers to allow split addressing. The bottom split could be used for conventional memory from 8000 to 9FFFF. The top split could be used for extended memory or could be used to copy main BIOS from ROM to RAM in the address range E0000 or F0000 to FFFFF. A middle split was available for copying user and video BIOS from ROM to RAM. This middle split had boundaries programmable between C0000 to DFFFF in 16K address increments. One limitation was that if the middle split were used, unused memory between the splits could not be translated and used for extended memory.

For the production version of the FE3021 (version reg=0000, 1001), the middle split of Bank 0 was removed. Video BIOS is shadowed instead by mapping the EGA/VGA BIOS to F0000 or F8000 and then shadowing the F0000 - FFFFF BIOS area. This method also allows a ROM resident setup program to reside at F0000 in ROM, which can be replaced with EGA/VGA BIOS by shadowing. This method allows a 512K bank to be allocated as 128K of conventional memory, 64K of shadowed VGA and system BIOS, and 320K of extended or EMS memory.

4

BANK 0 - LOWER SPLIT

UPPER ADDRESS BOUNDARY

FFF57	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

UPPER BOUNDARY MUST BE 0FXXXX OR BELOW

LOWER ADDRESS BOUNDARY

FFF59	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

LOWER BOUNDARY MUST BE 0FXXXX OR BELOW

UPPER ADDRESS BOUNDARY = 09XXXX (HEX) BY MASTER RESET

LOWER ADDRESS BOUNDARY = 08XXXX (HEX) BY MASTER RESET

BANK 0 - UPPER SPLIT

UPPER ADDRESS BOUNDARY - MSD

FFF5A	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

BANK 0 - UPPER SPLIT

UPPER ADDRESS BOUNDARY - LSD

FFF5B	X	X	X	X	A19	A18	A17	A16**
	7	6	5	4	3	2	1	0

LOWER ADDRESS BOUNDARY - MSD

FFF5C	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

UPPER ADDRESS BOUNDARY = 00XXXX (HEX) BY MASTER RESET

LOWER ADDRESS BOUNDARY = FFXXXX (HEX) BY MASTER RESET
(UPPER SPLIT DISABLED)

LOWER ADDRESS BOUNDARY - LSD

FFF5D	X	X	X	X	A19	A18	A17	A16**
	7	6	5	4	3	2	1	0

* Don't care

** A16 is ignored in early production version (0000, 1011)

BANK 0 - MIDDLE SPLIT

UPPER ADDRESS BOUNDARY - MSD

FFF5E	X	X	X	X	'1'	'1'	'0'	A16
	7	6	5	4	3	2	1	0

(ONLY IN EARLY PRODUCTION VERSION)

UPPER ADDRESS BOUNDARY - LSD

FFF5F	X	X	X	X	A15	A14	'0'	'0'
	7	6	5	4	3	2	1	0

LOWER ADDRESS BOUNDARY - MSD

FFF60	X	X	X	X	'1'	'1'	'0'	A16
	7	6	5	4	3	2	1	0

UPPER ADDRESS BOUNDARY = 00XXXX (HEX) BY MASTER RESET
LOWER ADDRESS BOUNDARY = FFXXXX (HEX) BY MASTER RESET
(MIDDLE SPLIT DISABLED)

LOWER ADDRESS BOUNDARY - LSD

FFF61	X	X	X	X	A15	A14	'0'	'0'
	7	6	5	4	3	2	1	0

BANK 1

UPPER ADDRESS BOUNDARY - MSD

FFF62	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

BANK 1

UPPER ADDRESS BOUNDARY - LSD

FFF63	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

LOWER ADDRESS BOUNDARY - MSD

FFF64	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

UPPER ADDRESS BOUNDARY = 07XXXX (HEX) BY MASTER RESET
LOWER ADDRESS BOUNDARY = 00XXXX (HEX) BY MASTER RESET

LOWER ADDRESS BOUNDARY - LSD

FFF65	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

* Don't care

BANK 2

UPPER ADDRESS BOUNDARY - MSD

	7	6	5	4	3	2	1	0
FFF66	X	X	X	X	A23	A22	A21	A20

THESE REGISTERS ARE CLEARED BY MASTER RESET

BANK 2

UPPER ADDRESS BOUNDARY - LSD

	7	6	5	4	3	2	1	0
FFF67	X	X	X	X	A19	A18	A17	0/1*

LOWER ADDRESS BOUNDARY - MSD

	7	6	5	4	3	2	1	0
FFF68	X	X	X	X	A23	A22	A21	A20

THESE REGISTERS ARE PRESET TO ALL '1' BY MASTER RESET

(BANK 2 DISABLED BY MASTER RESET)

LOWER ADDRESS BOUNDARY - LSD

	7	6	5	4	3	2	1	0
FFF69	X	X	X	X	A19	A18	A17	0/1*

BANK 3

UPPER ADDRESS BOUNDARY - MSD

	7	6	5	4	3	2	1	0
FFF6A	X	X	X	X	A23	A22	A21	A20

THESE REGISTERS ARE CLEARED BY MASTER RESET

BANK 3

UPPER ADDRESS BOUNDARY - LSD

	7	6	5	4	3	2	1	0
FFF6B	X	X	X	X	A19	A18	A17	0/1*

LOWER ADDRESS BOUNDARY - MSD

	7	6	5	4	3	2	1	0
FFF6C	X	X	X	X	A23	A22	A21	A20

THESE REGISTERS ARE PRESET TO ALL '1' BY MASTER RESET

(BANK 3 DISABLED BY MASTER RESET)

LOWER ADDRESS BOUNDARY - LSD

	7	6	5	4	3	2	1	0
FFF6D	X	X	X	X	A19	A18	A17	0/1*

* Don't care

The RAM banks may be either independent or two-way or four-way page interleaved. DRAM banks which are interleaved must be the same DRAM size.

This register is not used in non-page mode.

When the memory system operates in page mode, the banks of memory may operate independently or may be interleaved. Interleaving may decrease the average number of wait states, thus increasing performance, but interleaving may only be done if the memory banks to be interleaved are the same size.

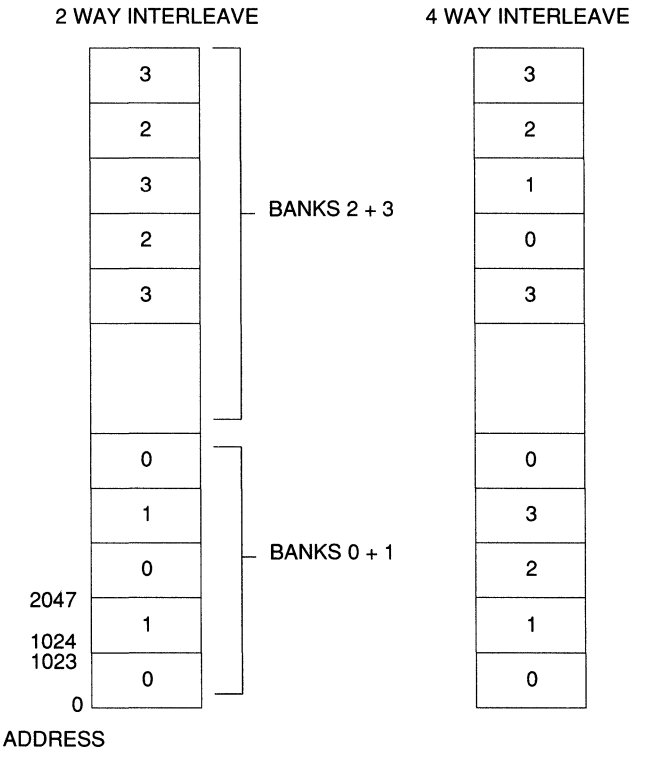
FFF6F

X	X	X	X	0/1*		CFG	
7	6	5	4	3	2	1	0

* Don't care

CFG	FUNCTION
000*	All banks are independent
011	Bank 2 paired with Bank 3, Banks 0 and 1 are independent
101	Bank 0 paired with Bank 1, Banks 2 and 3 are independent
111	Bank 0 paired with Bank 1, Bank 2 paired with Bank 3
110	All four banks are interleaved

* : Default after Master Reset

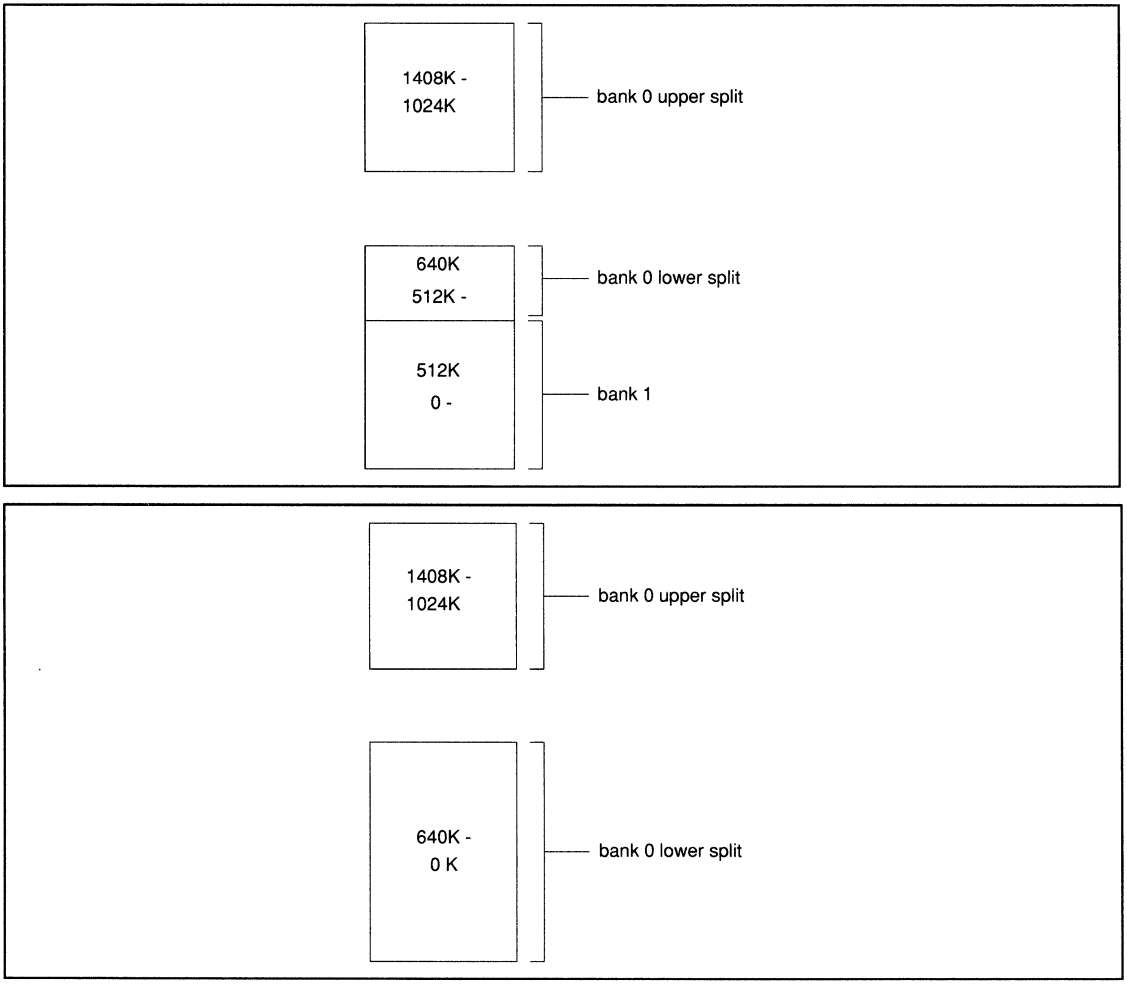


When the memory system operates in page mode, accesses to DRAM in the same page are made with zero wait states. An access to a different page, or the first access to a page after a refresh, DMA, or master cycle will be made either with two wait states for memory mode 2, or three wait states for memory mode 3. The actual page size is variable, depending on the DRAM size.

DRAM SIZE	PAGE SIZE
64K	512 bytes
256K	1024 bytes
1M	2048 bytes

Multiple banks of memory operating in page mode may operate independently or may be interleaved. Interleaving may decrease the average number of wait states, thus increasing performance, but interleaving may only be done if the memory banks to be interleaved are the same size. Only banks 0 and 1 or banks 2 and 3 may be interleaved together when implementing 2-way interleave. When banks 0 and 1 are interleaved, bank 1 boundary registers should be programmed so that the bank is disabled and the bank 0 boundaries should be programmed as if bank 0 were twice the normal size. As an example, for a system with 2 banks of 256K DRAM operating independently, the banks could be programmed as shown in the upper diagram below.

When the banks are interleaved, the banks would be programmed as shown in the lower diagram below.



The following tables illustrate memory system characteristics with various configurations of memory and processor speed, both for page mode and non-page mode DRAM access.

For a page mode hit, the read and write accesses may have different performance. For a page mode miss or the first access to a page, the read and write accesses have the same performance. In a page mode miss, $\overline{RAS}$ starts out low and must be brought high for a RAS precharge time before the memory can be accessed.

NON-PAGE MODE	CPU FREQUENCY	WAIT STATES			DRAM SPEED
		READ	WRITE	EMS MISS	
MODE 4	8 MHz	0	0	2	120 ns
MODE 0	16 MHz	1	1	3	80 ns
MODE 4	12.5 MHz	1	1	2	120 ns

PAGE MODE	CPU FREQUENCY	WAIT STATES				DRAM SPEED
		READ	WRITE	NON-EMS MISS	EMS MISS	
MODE 2	12.5 MHz	0	1	2	3	120 ns
MODE 3	20 MHz	0	1	3	3	80 ns
MODE 3	16 MHz	0	1	3	3	100 ns
MODE 3	12.5 MHz	0	1	3	3	120 ns

RAM SIZE CONFIGURATION REGISTER - BANK 1 AND 0

FFF70

BNK 1 SZ		BNK 0 SZ	
3	2	1	0

SZ = 00 *: 256K
01 : 1M
10 : RESERVED
11 : 64K

RAM SIZE CONFIGURATION REGISTER - BANK 3 AND 2

FFF71

BNK 3 SZ		BNK 2 SZ	
3	2	1	0

SZ = 00 *: 256K
01 : 1M
10 : RESERVED
11 : 64K

The DRAM timing is set by an external delay line for DMA or master mode transfers. The RAS leading edge becomes active from the active level of the MEMR or MEMW signals.

The DRAM timing modes are programmed by writing into register FFF72. The DRAM timing mode is actually switched during a processor hold state caused by a refresh, DMA, or bus master cycle. The Present DRAM Timing Mode register contains the current timing mode. Registers FFF72 and FFF73 will thus disagree until after a processor hold state occurs; typically, a refresh cycle will occur in 10 to 15 microseconds.

DRAM TIMING MODE

FFF72

X	X	X	X	D	DTYP		
7	6	5	4	3	2	1	0

DRAM TIMING MODE WILL GO INTO EFFECT AFTER REFRESH, DMA, OR OTHER HOLD CYCLE

PRESENT DRAM TIMING MODE

FFF73

X	X	X	X	D	DTYP			READ-ONLY
7	6	5	4	3	2	1	0	

DTYP	DRAM MODE	
000*	Non-Page	(MODE 0)
001	Zero Wait State Read, One Wait State Write	(MODE 1)
010	Page Mode DRAM At 12.5 MHz CPU rate	(MODE 2)
011	Standard Page Mode for 8-20 MHz CPU rate	(MODE 3)
100	Identical to Mode 0, but RAS delayed one-half CPU clock	(MODE 4)
101	Non-Page for 8-12 MHz CPU rate,with 0 Wait States, RAS pulse width is 2 CPU clocks	(MODE 5)

* : Default after Master Reset
D = 0: Normal operation (default)
1 : Reversed for diagnostics;
disables DRAM Page Mode Hit/Miss logic

8.0 EMS MEMORY

RAM memory above 1024K may be used both for expanded or extended memory. EMS memory may be as small as 128K bytes or as large as 7168K bytes. The EMS memory is accessed by two sets of EMS Page Registers, which reside in user I/O space. Each set of EMS Page Registers points to 36 blocks of memory, each block 16K bytes in size, which make up the EMS Page Frame. Four of the blocks are located above 640K, with the other 32 blocks located between 128K and 640K.

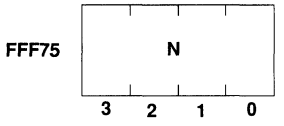
Each EMS Page Register is associated with one page of the EMS Page Frame, and consists of an enable bit and a 10 bit page number. When enabled, a 24 bit real address is formed by taking the 10 bit page number and appending the 14 bit address referencing the byte or word in the EMS page. The 24 bit address is then used to access the DRAM memory controlled by the FE3021.

In either page mode or non-page mode, if the DRAM row address does not change, then no additional wait states are required for EMS translation. This will allow EMS access without additional wait states if accesses are made to the same 512, 1024, or 2048 byte page, depending on DRAM size.

The EMS hardware must first be configured by programming the EMS control registers located in the FFF00-FFFFF register space, which is unlocked by writing to memory location FFF00 eight times. The I/O port locations of the EMS Page Registers are in user I/O space and their locations are selected with EMS Configuration Registers FFF75 and FFF78.

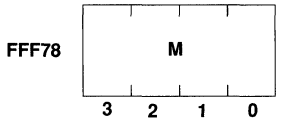
EMS Configuration Register FFF79 is used to completely enable or disable EMS, as well as to switch between the two sets of EMS Page registers. When the 'E' bit is '0', EMS operation is disabled and the EMS registers in user I/O space are inaccessible. When this is '0', it is as if the EMS hardware had been "unplugged" from the bus. When the 'E' bit is a '1', the EMS registers in the user I/O space become accessible. Registers FFF75 and FFF78 (which determine the I/O port addresses for the EMS logic), should be programmed prior to setting the 'E' bit to '1'.

EMS CONFIGURATION REGISTER N



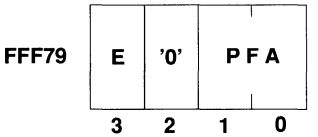
THIS REGISTER IS LOADED WITH '0110' BY MASTER RESET

EMS CONFIGURATION REGISTER M



THIS REGISTER IS LOADED WITH '1000' BY MASTER RESET

EMS CONFIGURATION REGISTER



E=1: MASTER ENABLE FOR EMS
BIT 2 RESERVED, '0'

PFA = 00 : EMS PAGE FRAME C4000-D3FFF
PFA = 01 : EMS PAGE FRAME C8000-D7FFF
PFA = 10 : EMS PAGE FRAME CC000-DBFFF
PFA = 11 : EMS PAGE FRAME D0000-DFFFF

THIS REGISTER IS CLEARED BY MASTER RESET

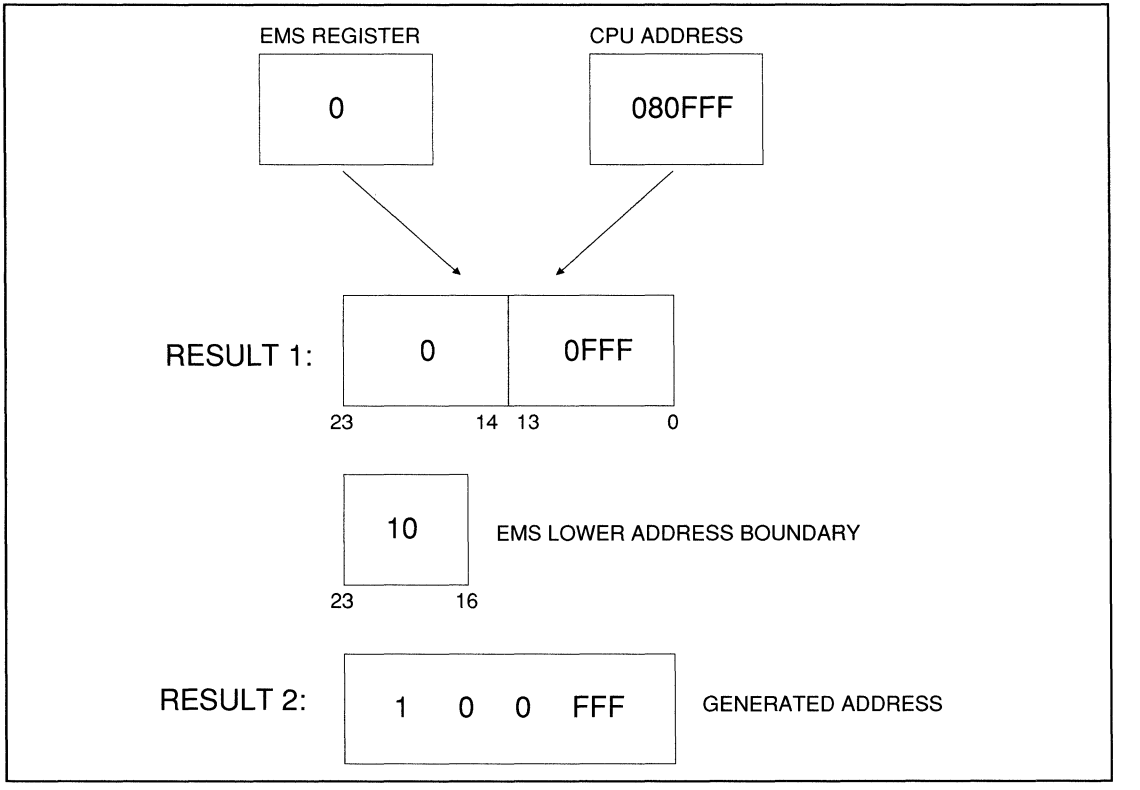
LOWER EMS BOUNDARY

THESE REGISTERS ARE SET TO '1111' BY MASTER RESET

* Don't care

Registers FFF76 and FFF77 are used to allocate memory for EMS, on 128K byte boundaries. Memory with addresses below the EMS boundary is accessed normally, as conventioanl or extended memory.

On-board memory with addresses above the EMS boundary is reserved for use only as EMS memory. DRAM memory accesses to addresses above the EMS boundary are made to the expansion bus. This allows EMS, off-board, and on-board extended memory to be used simultaneously.



Any CPU address above 1 MB (the EMS lower address boundary), is assumed to reference memory on the expansion bus, rather than on-board memory, which prevents extended memory references from affecting on-board EMS memory.

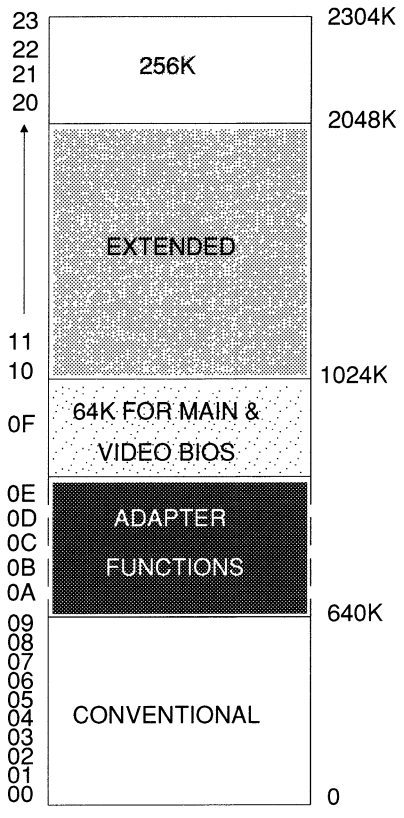
EMS DMA Control Register FFF7A is used to control the selected EMS map register set during DMA or master transfers. This allows DMA transfers to be made to a particular EMS task, whether or not it is the currently selected task.

On-board memory may be allocated either to extended or to EMS memory in 128K byte blocks. EMS memory is allocated from the top of on-board memory down to the desired limit.

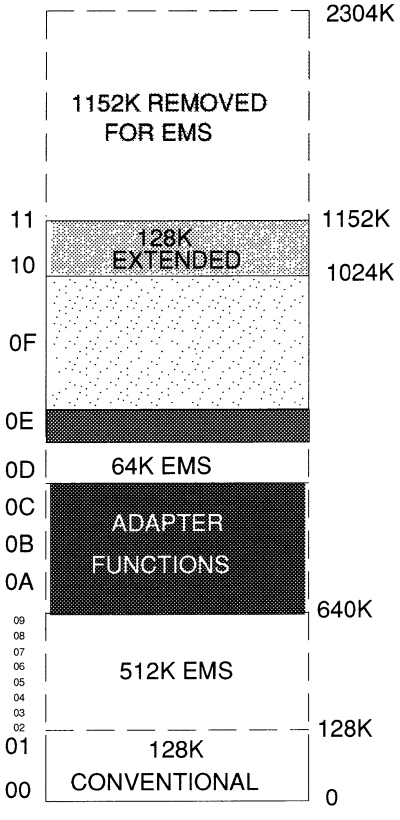
As an example, if the system contained 2 MB of DRAM, the memory map (without EMS) might look similar to figure 5a on the following page. The system would contain 640K of conventional memory and 1,280K of extended memory. The 1,280K of extended memory is composed of two parts: the original 1,024K and 256K of memory relocated from 0A0000 - 0E0000. The 128K area from 0E0000 - 0F0000 could also be relocated but in this example, it is not.

Figure 5b illustrates the memory map after EMS has been installed. The EMS boundary registers have been programmed so that on-board memory above 1,152K is reserved for EMS. 128K of on-board extended memory remains between 100000 - 120000. Additional extended memory could be added on the expansion bus, starting at 120000. Two EMS areas are shown, one 64K area at 0D0000 - 0E0000, and the other at 020000 - 0A0000.

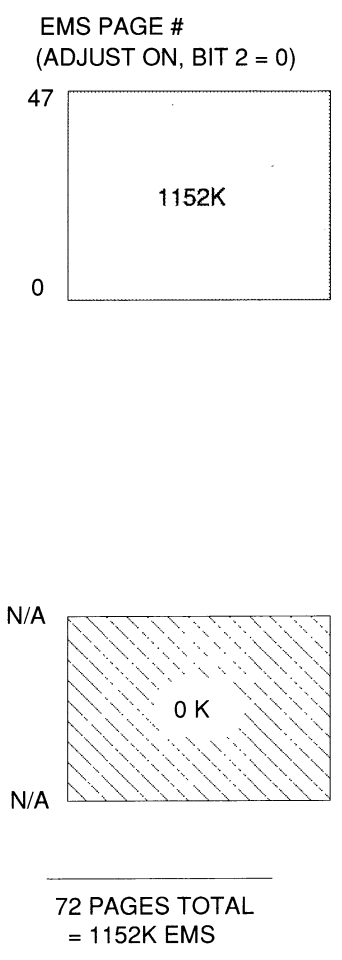
Figure 5c shows the possible EMS page numbers ranging from 0 - 4F for the 1,280K of memory available for EMS paging.



a) 2 MB Memory Map
before EMS installed



b) EMS Installed



c) Available EMS
Memory

Figure 4. EMS/Memory Map Configurations

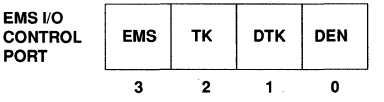
The EMS Control Register and EMS Page Registers are addressed in the user I/O port address space, I/O ports 100 (hex) through 3FF (hex). The EMS Control Registers and EMS Page Registers are selected when the I/O port address bits 9 - 6 match the value 'M' programmed by register FFF78 and the I/O port address bits 5 - 2 match the value 'N' programmed by register FFF75.

The EMS I/O Control Port is used to enable or disable EMS translation. When EMS translation is disabled, the EMS I/O control port and EMS page registers may still be accessed, but EMS page swapping will not occur.

The EMS I/O Control Port is also used to select the active page register set. When the processor accesses EMS memory, it always uses the register set specified by the TK bit. Normally, when DMA accesses EMS memory, it also uses the register set specified by the TK bit. Alternatively, the DMA transfer may be made using a particular register set, independently of the register set currently being used by the processor. This allows a DMA operation to start, continue, and finish while the processor is time-slicing and swapping back and forth between two programs.

The P and W fields for each page register are specified in the following table. Each EMS Page register is composed of a one bit enable bit (E) and a 10-bit page number (Q9-Q0). EMS translation for the EMS page is enabled when the E bit is a '1'.

EMS CONTROL REGISTER

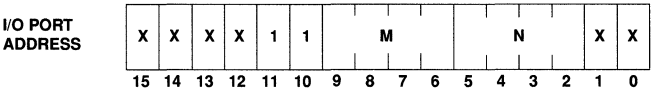


EMS = 1: EMS TRANSLATION ENABLED

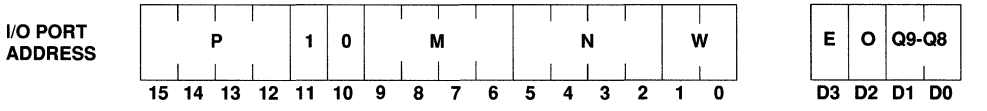
DEN = 0 : DMA TRANSFERS MADE TO MAP REGISTER SET SPECIFIED BY "TK" BIT

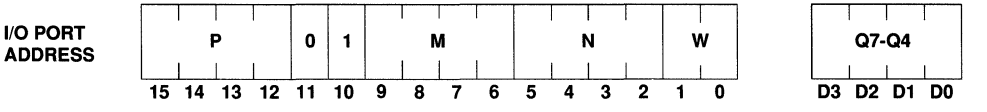
DEN = 1 : DMA TRANSFERS MADE TO MAP REGISTER SET SPECIFIED BY "DTK" BIT

EMS CONTROL REGISTER ADDRESS LOCATION

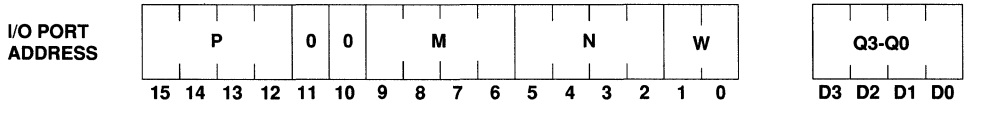


EMS PAGE REGISTER - MSD





EMS PAGE REGISTER - LSD



9.0 TEST MODE

All output pins will become tristated if $\overline{YMEMR}$ and $\overline{YMEMW}$ are active simultaneously while $\overline{MR}$ is active. The outputs will remain tristated if $\overline{MR}$ is brought inactive while $\overline{YMEMR}$ and $\overline{YMEMW}$ are both active. The outputs will become active drivers again when $\overline{MR}$ is brought low without both $\overline{YMEMR}$ and $\overline{YMEMW}$ active. This "all output tristate" mode allows an in-circuit board tester to drive the FE3021 output pins.

4

P	W	EMS PAGE			
		PFA=00	PFA=01	PFA=10	PFA=11
0000	11	D0000-D3FFF	D4000-D7FFF	D8000-DBFFF	DC000-DFFFF
0000	10	CC000-CFFFF	D0000-D3FFF	D4000-D7FFF	D8000-DBFFF
0000	01	C8000-CBFFF	CC000-CFFFF	D0000-D3FFF	D4000-D7FFF
0000	00	C4000-C7FFF	C8000-CBFFF	CC000-CFFFF	D0000-D3FFF
1001	11	9C000-9FFFF	624K TO 640K		
1001	10	98000-9BFFF	608K TO 624K		
1001	01	94000-97FFF	592K TO 608K		
1001	00	90000-93FFF	576K TO 592K		
1000	11	8C000-8FFFF	560K TO 576K		
1000	10	88000-8BFFF	544K TO 560K		
1000	01	84000-87FFF	528K TO 544K		
1000	00	80000-83FFF	512K TO 528K		
0111	11	7C000-7FFFF	496K TO 512K		
0111	10	78000-7BFFF	480K TO 496K		
0111	01	74000-77FFF	464K TO 480K		
0111	00	70000-73FFF	448K TO 464K		
0110	11	6C000-6FFFF	432K TO 448K		
0110	10	68000-6BFFF	416K TO 432K		
0110	01	64000-67FFF	400K TO 416K		
0110	00	60000-63FFF	384K TO 400K		
0101	11	5C000-5FFFF	368K TO 384K		
0101	10	58000-5BFFF	352K TO 368K		
0101	01	54000-57FFF	336K TO 352K		
0101	00	50000-53FFF	320K TO 336K		
0100	11	4C000-4FFFF	304K TO 320K		
0100	10	48000-4BFFF	288K TO 304K		
0100	01	44000-47FFF	272K TO 288K		
0100	00	40000-43FFF	256K TO 272K		
0011	11	3C000-3FFFF	240K TO 256K		
0011	10	38000-3BFFF	224K TO 240K		
0011	01	34000-37FFF	208K TO 224K		
0011	00	30000-33FFF	192K TO 208K		
0010	11	2C000-2FFFF	176K TO 192K		
0010	10	28000-2BFFF	160K TO 176K		
0010	01	24000-27FFF	144K TO 160K		
0010	00	20000-23FFF	128K TO 144K		

Table 9. EMS Page Register Information

10.0 FE3021 PINOUT

As illustrated in Figure 5, the FE3021 is packaged in a 132-pin plastic flat pack. Table 10 groups the pins by function.

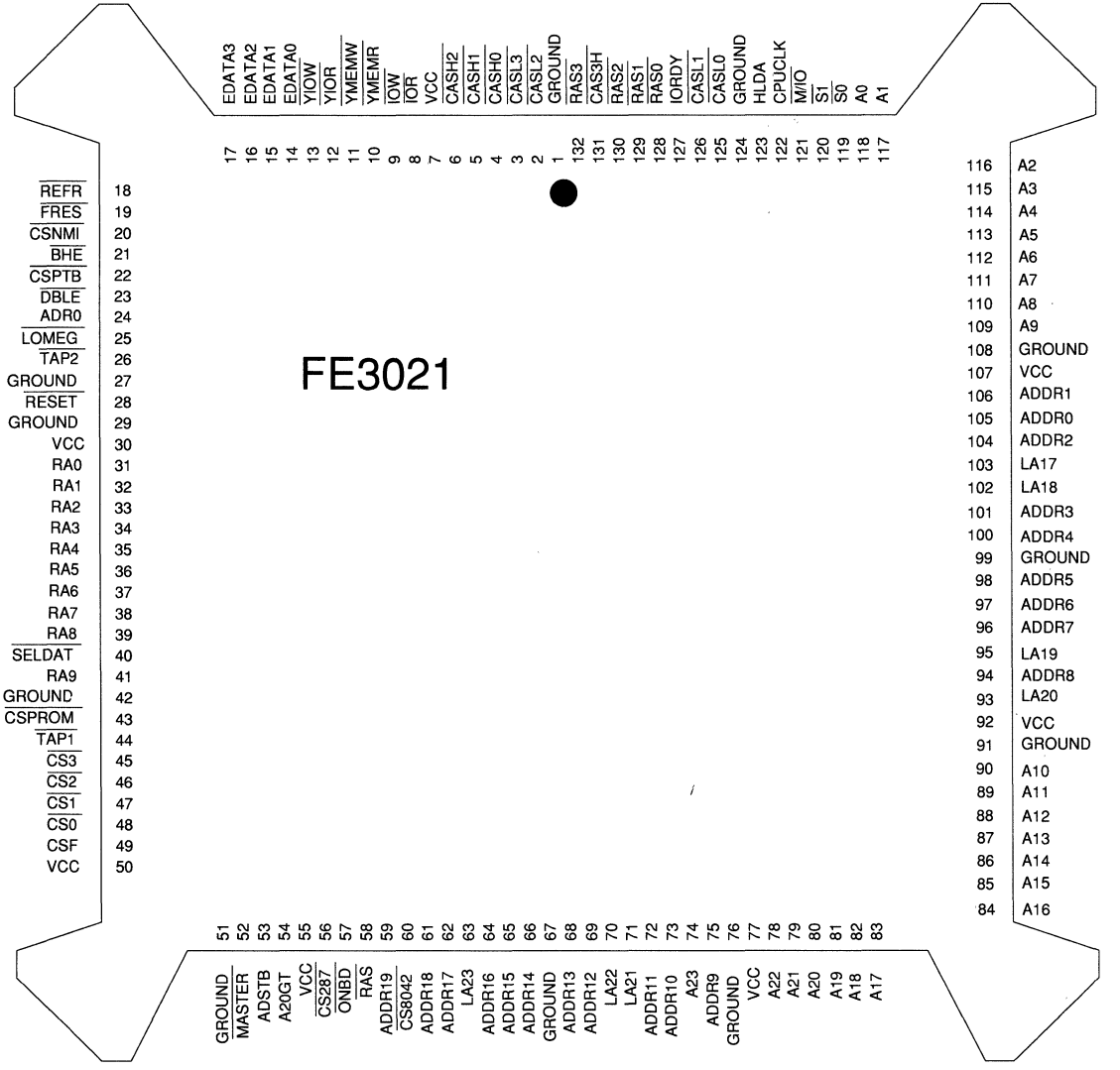


Figure 5. FE3021 Pin Assignment

AT BUS	
LA23	63
LA22	70
LA21	71
LA20	93
LA19	95
LA18	102
LA17	103
ADDR19	59
ADDR18	61
ADDR17	62
ADDR16	64
ADDR15	65
ADDR14	66
ADDR13	68
ADDR12	69
ADDR11	72
ADDR10	73
ADDR9	75
ADDR8	94
ADDR7	96
ADDR6	97
ADDR5	98
ADDR4	100
ADDR3	101
ADDR2	104
ADDR1	106
ADDR0	105
MASTER	52
GROUND	**POWER**
1	7
27	30
29	50
42	55
51	77
67	92
76	107
91	
99	
108	
124	

DATA BUS	
EDATA3	17
EDATA2	16
EDATA1	15
EDATA0	14
CHIP SELECTS AND CONTROL	
CS0	48
CS1	47
CS2	46
CS3	45
CSF	49
CS8042	60
CS287	56
CSNMI	20
CSPTB	22
ADSTB	53
SELDAT	40
YMEMR	10
YMEMW	11
YIOR	12
YIOW	13
IOR	8
IOW	9
MEMORY ADDRESS MUX	
RA9	41
RA8	39
RA7	38
RA6	37
RA5	36
RA4	35
RA3	34
RA2	33
RA1	32
RA0	31
RAS	58

80286 INTERFACE	
A23	74
A22	78
A21	79
A20	80
A19	81
A18	82
A17	83
A16	84
A15	85
A14	86
A13	87
A12	88
A11	89
A10	90
A9	109
A8	110
A7	111
A6	112
A5	113
A4	114
A3	115
A2	116
A1	117
A0	118
S0	119
S1	120
M/IO	121
CPUCLK	122
HLDA	123
IORDY	127

MEMORY CONTROL	
RAS0	128
RAS1	129
RAS2	130
RAS3	132
CASL0	125
CASL1	126
CASL2	2
CASL3	3
CASH0	4
CASH1	5
CASH2	6
CASH3	131
REFR	18
CSPROM	43
ONBD	57
BHE	21
DBLE	23
ADR0	24
LOMEG	25
A20GT	54

RESET	
RESET	28
FRES	19

Table 10. FE3021 Pins Grouped By Function

11.0 DC OPERATING CHARACTERISTICS

T_a = 0° to 70° C, Vcc = 5 V ± .25 V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
IIL	Input Leakage		±10	UA	VIN=.4 TO VCC
IOZ	Tri-State And Open Drain Output Leakage		±10	UA	VOUT=.4 TO VCC
VIH	Input High Voltage	2.0		V	
VIL	Input Lowvoltage		.8	V	
VILC	CPU Clock Input High Voltage	.6		V	
VILC	CPU Clock Input Low Voltage		.6	V	
ICC	Supply Current		50	mA	All Outputs Open, Inputs At 2.0V, CPUCLK = 16 MHz

For outputs: $\overline{\text{YIOR}}$, $\overline{\text{YIOW}}$, RA9-RA0, $\overline{\text{ONBD}}$, $\overline{\text{LOMEG}}$, A23-A0, CSF, $\overline{\text{CS0}}$, $\overline{\text{CS1}}$, $\overline{\text{CS2}}$, $\overline{\text{CS3}}$, $\overline{\text{CS8042}}$, $\overline{\text{CS287}}$, $\overline{\text{CSNMI}}$, $\overline{\text{CSPTB}}$, $\overline{\text{RAS}}$, $\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{RAS2}}$, $\overline{\text{RAS3}}$, $\overline{\text{CASL0}}$, $\overline{\text{CASL1}}$, $\overline{\text{CASL2}}$, $\overline{\text{CASL3}}$, $\overline{\text{CASH0}}$, $\overline{\text{CASH1}}$, $\overline{\text{CASH2}}$, $\overline{\text{CASH3}}$, $\overline{\text{CSPROM}}$, $\overline{\text{DBLE}}$, $\overline{\text{FRES}}$, $\overline{\text{SELDAT}}$, AND EDATA3-EDATA0

For outputs: ADDR19-ADDR0, LA23-LA17, $\overline{\text{IOR}}$, $\overline{\text{IOW}}$, IORDY

* 10 mA for $\overline{\text{IOR}}$, $\overline{\text{IOW}}$.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT=-1 mA
VOL	Output Low Voltage		.4	V	IOUT=1 mA

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT=-3 mA
VOL	Output Low Voltage		.4	V	IOUT=12 mA*

12.0 AC TIMING CHARACTERISTICS

load capacitance = 50 pF for outputs: CSF, $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{CS8042}$, $\overline{CS287}$, $\overline{CSNMI}$, $\overline{CSPTB}$, $\overline{SELDAT}$, RA0-RA9, $\overline{ONBD}$, $\overline{LOMEG}$, $\overline{DBLE}$, $\overline{RAS}$, $\overline{CSPROM}$, $\overline{YIOR}$, $\overline{YIOW}$, $\overline{FRES}$

load capacitance = 100 pF for output: IORDY, A19-A0, EDATA3-EDATA0

load capacitance = 200 pF for outputs: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$, $\overline{CASL0}$, $\overline{CASL1}$, $\overline{CASL2}$, $\overline{CASL3}$, $\overline{CASH0}$, $\overline{CASH1}$, $\overline{CASH2}$, $\overline{CASH3}$, LA23-LA17, ADDR19-ADDR0, $\overline{IOR}$, $\overline{IOW}$

13.0 SYSTEM TIMING

		PRELIMINARY		PRELIMINARY		PRELIMINARY	
		12 MHz		16 MHz		20 MHz	
SYMBOL	CHARACTERISTIC	MIN	MAX	MIN	MAX	MIN	MAX
T1	CPUCLK Cycle	40		31		25	
T2	CPUCLK High Pulse	13		12			
T3	CPUCLK Low Pulse	11		10			
T4	A23-A0, MIO Setup To $\overline{S0}$ OR $\overline{S1}$ Falling	22		22			
T5	A23-A0, MIO To $\overline{ONBD}$		38		34		
T6	$\overline{S0}$, $\overline{S1}$ Setup To CPUCLK Falling	20		11		9	
T7	$\overline{S0}$, $\overline{S1}$ Hold From CPUCLK Falling	3		2		1	
T10	MIO, A23..A0 To LA23..LA17		50		45		45
T13	$\overline{YMEMR}$ To $\overline{CSPROM}$		45		38		30
T14	ADSTB To $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{CSPTB}$, $\overline{CSF}$, $\overline{CS287}$, $\overline{CSNMI}$, $\overline{CS8042}$		45		35		35
T17a	$\overline{YIOR}$ To $\overline{IOR}$		40		35		35
T17	$\overline{YIOW}$ To $\overline{IOW}$		40		35		35
T18	ADSTB To ADDR19..ADDR1		50		45		45
T19	ADR0 To ADDR0		45		40		40
T20	Data Valid From $\overline{YMEMR}$ Or $\overline{YIOR}$ Active		180		150		150
T22	LA23..LA17 From CPUCLK Falling		50		45		45
T24	DATA Setup To $\overline{YMEMW}$ Or $\overline{YIOW}$ Inactive		180	150		150	
T25	Data Hold From $\overline{YMEMW}$ Or $\overline{YIOW}$ Inactive	10		10		10	
T26	$\overline{YIOR}$ Or $\overline{YMEMR}$ To $\overline{SELDAT}$		50		45		45
T27	$\overline{IOR}$ To $\overline{SELDAT}$, Master Mode Cycle		50		45		45
T28	ADSTB To Row Address; DMA Cycle, Non-EMS		50		42		35
T28a	ADSTB To Row Address; DMA Cycle, EMS		180		145		145

		PRELIMINARY		PRELIMINARY		PRELIMINARY	
		12 MHz		16 MHz		20 MHz	
SYMBOL	CHARACTERISTIC	MIN	MAX	MIN	MAX	MIN	MAX
T29	$\overline{YMEMR}$ To $\overline{RAS}$, $\overline{RAS3}$: $\overline{RAS0}$; Refresh Cycle		35		30		30
T30	$\overline{YMEMR}$ Or $\overline{YMEMW}$ To $\overline{RAS}$; DMA Cycle		35		30		30
T31	$\overline{TAP1}$ Falling To Column Address		45		37		30
T32	$\overline{YMEMR}$ Or YMEMW To $\overline{RAS3}$..$\overline{RAS0}$; DMA Cycle		35		30		30
T33	$\overline{TAP2}$ Falling To $\overline{CASL3}$.. $\overline{CASL0}$, $\overline{CASH0}$; DMA Cycle		30		26		25
T34	$\overline{YMEMR}$ Or $\overline{YMEMW}$ Rising To $\overline{CASL3}$...$\overline{CASL0}$ Or $\overline{CASH3}$..$\overline{CASH0}$ Inactive		35		28		27
T35	$\overline{YMEMR}$ Active To $\overline{DLE}$ Active; DMA Or Master Mode		40		32		30
T36	$\overline{YMEMR}$ inactive To $\overline{DLE}$ inactive: DMA Or Master Mode		40		32		30
T37	$\overline{BHE}$ Or ADR0 Setup To CPUCLK Falling		25	20		20	
T38a	ADR0 Setup To CPUCLK Falling		25	20		20	
T38b	$\overline{BHE}$ Setup To CPUCLK Falling		25	20		20	
T39	A23..A1 To RA9..RA0 Row Address; Mode 0, 1, 4, 5		45		37		30
T40	$\overline{TAP1}$ Falling To RA9. . RA0 Column Address; Mode 0, 1, 4, 5		45		37		30
T41	RA9..RA0 Row Address Valid From CPUCLK At End Of CAS		50		39		
T43	CPUCLK Falling To $\overline{RAS}$; Mode 0, 1, & 5		35		30		30
T44	CPUCLK Falling To $\overline{RAS3}$; $\overline{RAS0}$; Mode 0 & 1 & 5		35		30		30
T45	CPUCLK Rising To $\overline{RAS}$; Mode 4		35		30		30
T46	CPUCLK Rising To $\overline{RAS3}$..$\overline{RAS0}$; Mode 4		35		30		30

		PRELIMINARY		PRELIMINARY		PRELIMINARY	
		12 MHz		16 MHz		20 MHz	
SYMBOL	CHARACTERISTIC	MIN	MAX	MIN	MAX	MIN	MAX
T47	$\overline{TAP2}$ Falling To $\overline{CASL3}$.. $\overline{CASL0}$; Or $\overline{CASH3}$..$\overline{CASH0}$ Active; Mode 0, 1, &4 & 5		35		25		25
T48	CPUCLK Falling To $\overline{CASL3}$.. $\overline{CASL0}$ Or $\overline{CASH3}$.. $\overline{CASH0}$ Inactive; Mode 0, 1, & 4 & 5		35		27		27
T49	Row ADDR From $\overline{S0}$ Or $\overline{S1}$ Inactive; Mode 2		50		44		
T50	$\overline{TAP2}$ Falling To $\overline{DLE}$ Active; Mode 0, 1, 4, & 5		35		30		30
T51	CPUCLK Falling To $\overline{DLE}$ Inactive; Mode 0, 1, 4, & 5		35		30		30
T52	Ready Low From $\overline{S0}$ OR $\overline{S1}$ low		35		30		30
T53	Ready High From CPUCLK Falling		35		30		
T54	Column ADDR From CPUCLK Falling; Mode 2		40		34		
T56	$\overline{RAS3}$ ..$\overline{RAS0}$ Active From CPUCLK Falling; Mode 2		35		30		
T57	$\overline{CASL3}$..$\overline{CASL0}$ Or $\overline{CASH3}$.. $\overline{CASH0}$ Active From CPUCLK Rising; Mode 2		30		23		
T58	$\overline{CASL3}$ ..$\overline{CASL0}$ Or $\overline{CASH3}$ .. $\overline{CASH0}$ Inactive From CPUCLK Rising		30		23		
T5857	Difference Of CAS Inactive And Active Time (T58-T57)		4		4		
T59	$\overline{DLE}$ From CPUCLK		35		26		
T60	Row Address Valid From CPUCLK Falling; Mode 3		40		34		
T61	$\overline{RAS3}$ ..$\overline{RAS0}$ Inactive From $\overline{S0}$ Or $\overline{S1}$ Active		35		30		
T62	$\overline{RAS3}$ ..$\overline{RAS0}$ Inactive From HLDA Active		40		35		
T63	Column Address Hold From End Of CAS	1		1		1	
T64	Column Address From CPUCLK; MODE 2 & 3		50		44		

		PRELIMINARY		PRELIMINARY		PRELIMINARY	
		12 MHz		16 MHz		20 MHz	
SYMBOL	CHARACTERISTIC	MIN	MAX	MIN	MAX	MIN	MAX
T65	Column Address From A23-A1		45		37		
T66	$\overline{RAS3}$ ..$\overline{RAS0}$ Active From CPUCLK Rising; Mode 3		35		30		
T67	$\overline{CASL3}$ ..$\overline{CASL0}$ Or $\overline{CASH3}$ .. $\overline{CASH0}$ Active From CPUCLK;Mode 3		28		23		
T68	$\overline{CASL3}$ ..$\overline{CASL0}$ Or $\overline{CASH3}$ .. $\overline{CASH0}$ Inactive From CPUCLK Rising; Mode 3		28		23		
T6867	Difference Of CAS Inactive And Active Time (T68-T67)		4		4		
T69	$\overline{REFR}$ To $\overline{ONBD}$		40		35		35
T70	Refresh Address Valid From $\overline{REFR}$		50		39		35
T72	$\overline{MASTER}$ Active To LA[23:17], ADDR[16:0] High Impedance		45		45		45
T73	$\overline{MASTER}$ Inactive To LA[23:17], ADDR [16:0] Low Impedance		45		45		45
T74	ADDR[9:0] To Chip Selects				65		65
T75	$\overline{MASTER}$ Active To A[23:0], ADR0 Low Impedance		45		45		45
T76	$\overline{MASTER}$ Inactive To A[23:0], ADR0 High Impedance		45		45		45
T77	LA[23:17], ADDR[16:1] To RA[9:0]		45		40		40
T78	$\overline{MASTER}$ Active To $\overline{YIOR}$, $\overline{YIOW}$ Low Impedance		45		45		45
T79	$\overline{MASTER}$ Inactive To $\overline{YIOR}$, YIOW High Impedance		45		45		45
T80	$\overline{MASTER}$ Active To $\overline{IOR}$, $\overline{IOW}$ High Impedance		45		45		45
T81	$\overline{MASTER}$ Inactive To $\overline{IOR}$, $\overline{IOW}$ Low impedance		45		45		45
T82a	$\overline{IOR}$ To $\overline{YIOR}$		30		25		25
T82b	$\overline{IOW}$ To $\overline{YIOW}$		30		25		25
T83	LA[23:17], ADDR[16:0] To A[23:0], ADRO		40		35		35

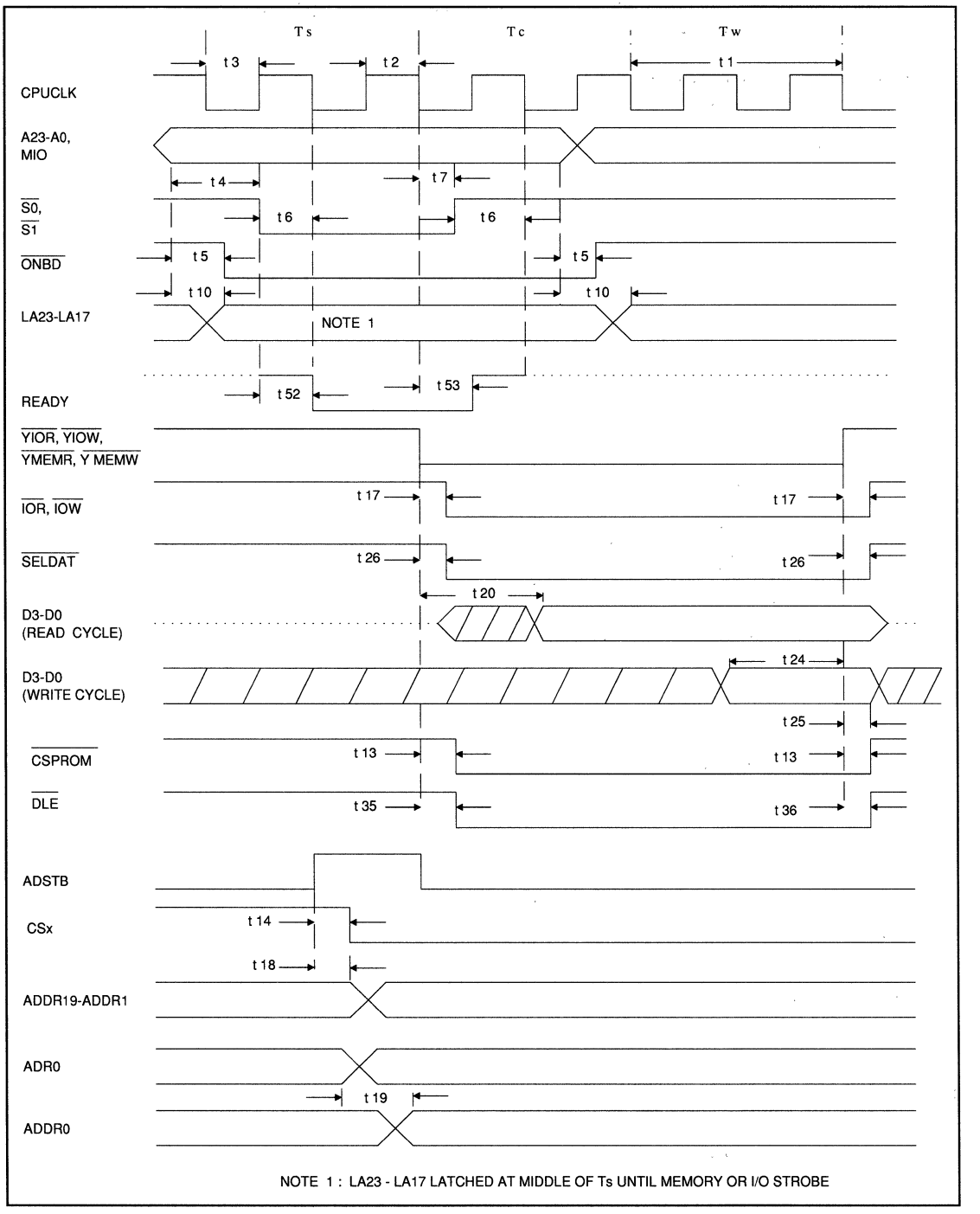
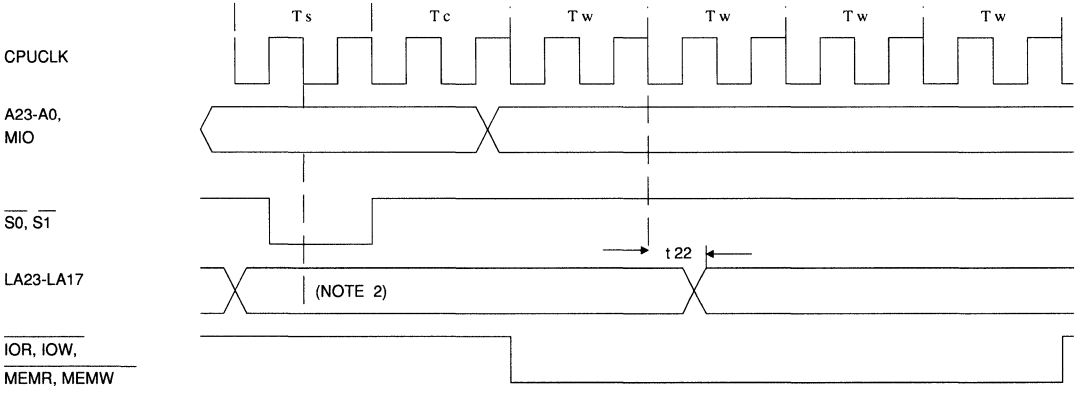


Figure 6. Basic Timing



NOTE 2: FOR OFF-BOARD CYCLES, LA23 - LA17 LATCHED AT MIDDLE OF Ts UNTIL 2 CPUCLK's AFTER MEMORY OR I/O STROBE

Figure 7. High Speed Mode LA23-LA17 Timing

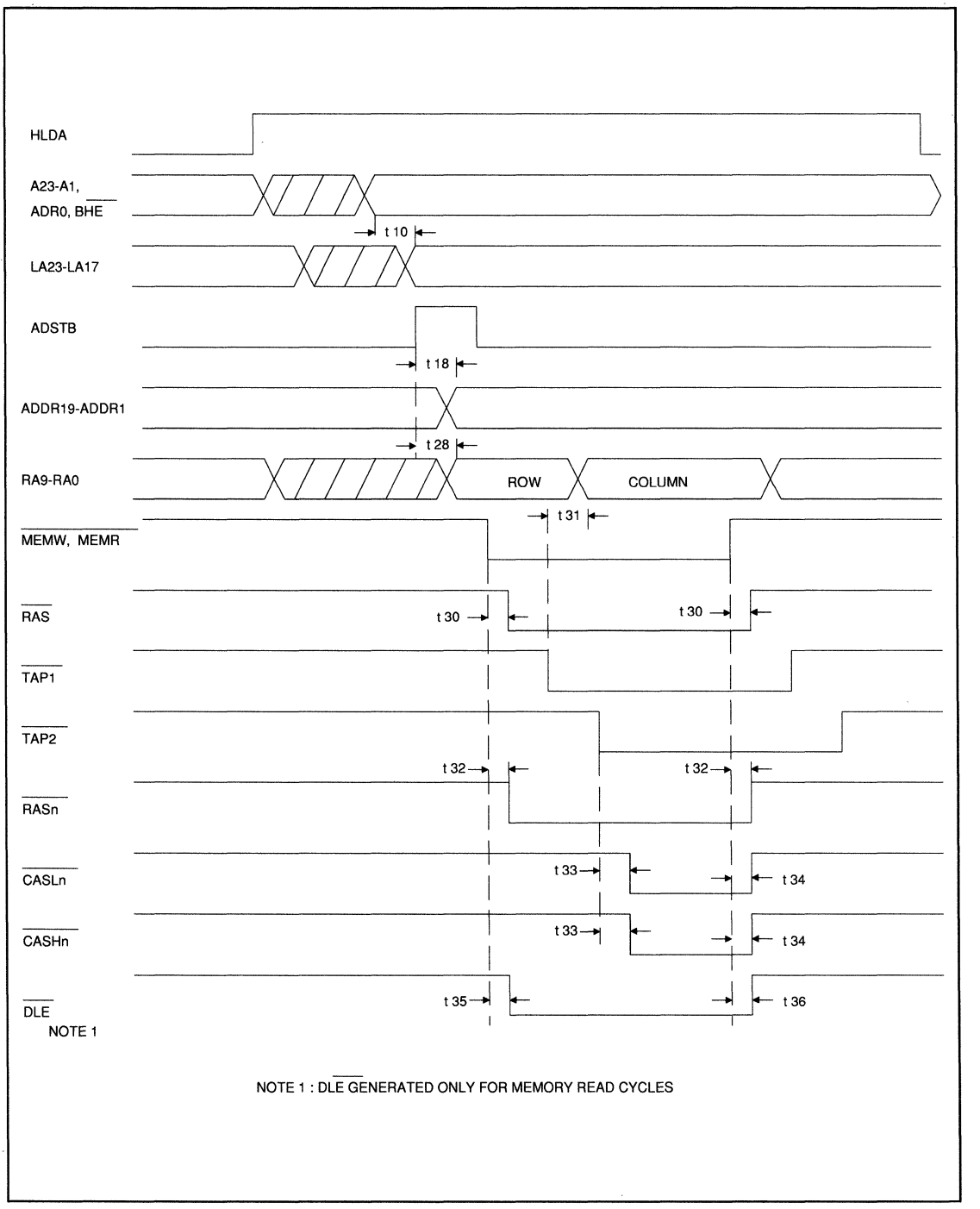
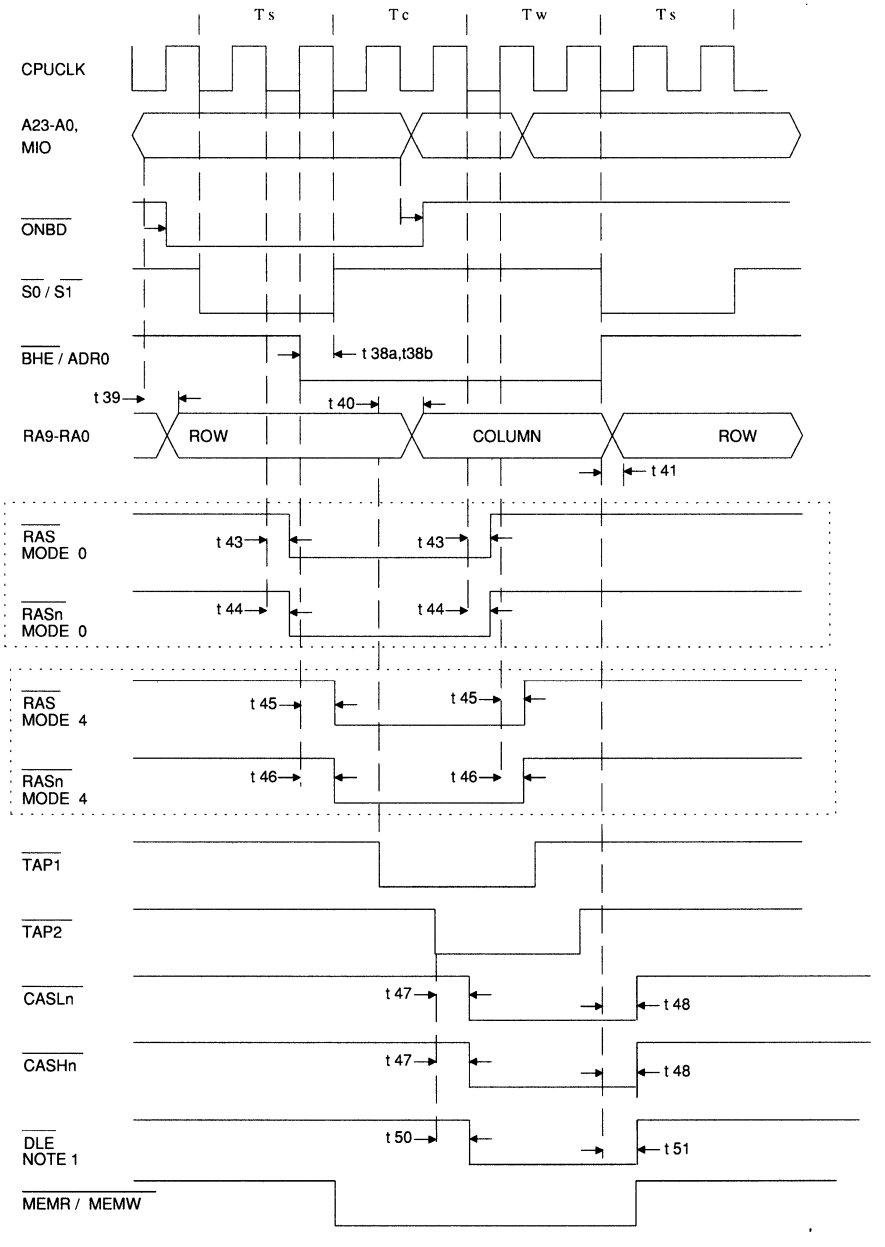


Figure 8. DMA Memory Cycle



NOTE 1: DLE GENERATED ONLY FOR MEMORY READ CYCLES

Figure 9. Memory Modes 0 & 4 (Non-page Mode)

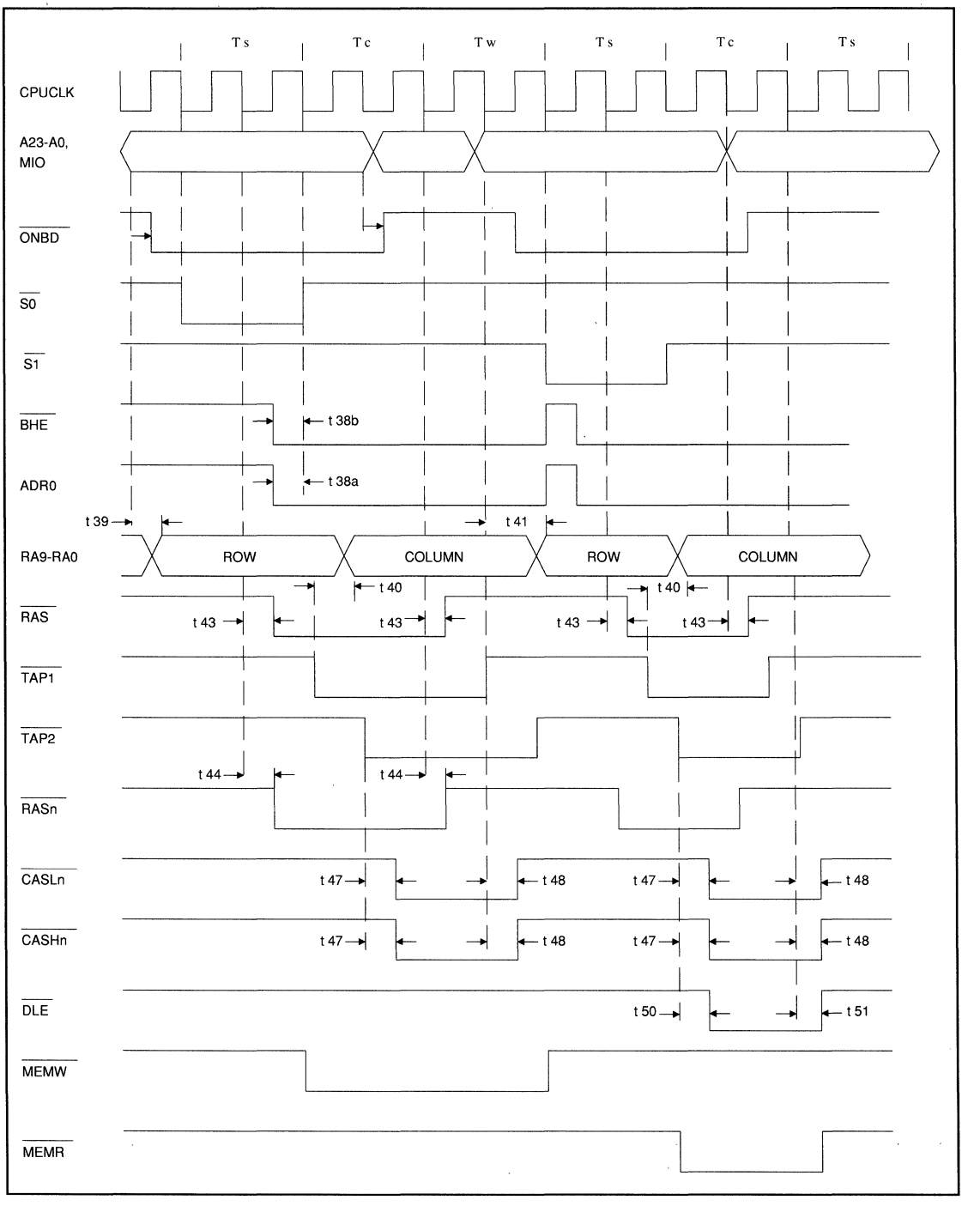


Figure 10. Memory Mode 1 (Non-Page 0 WS Read/1 WS Write)

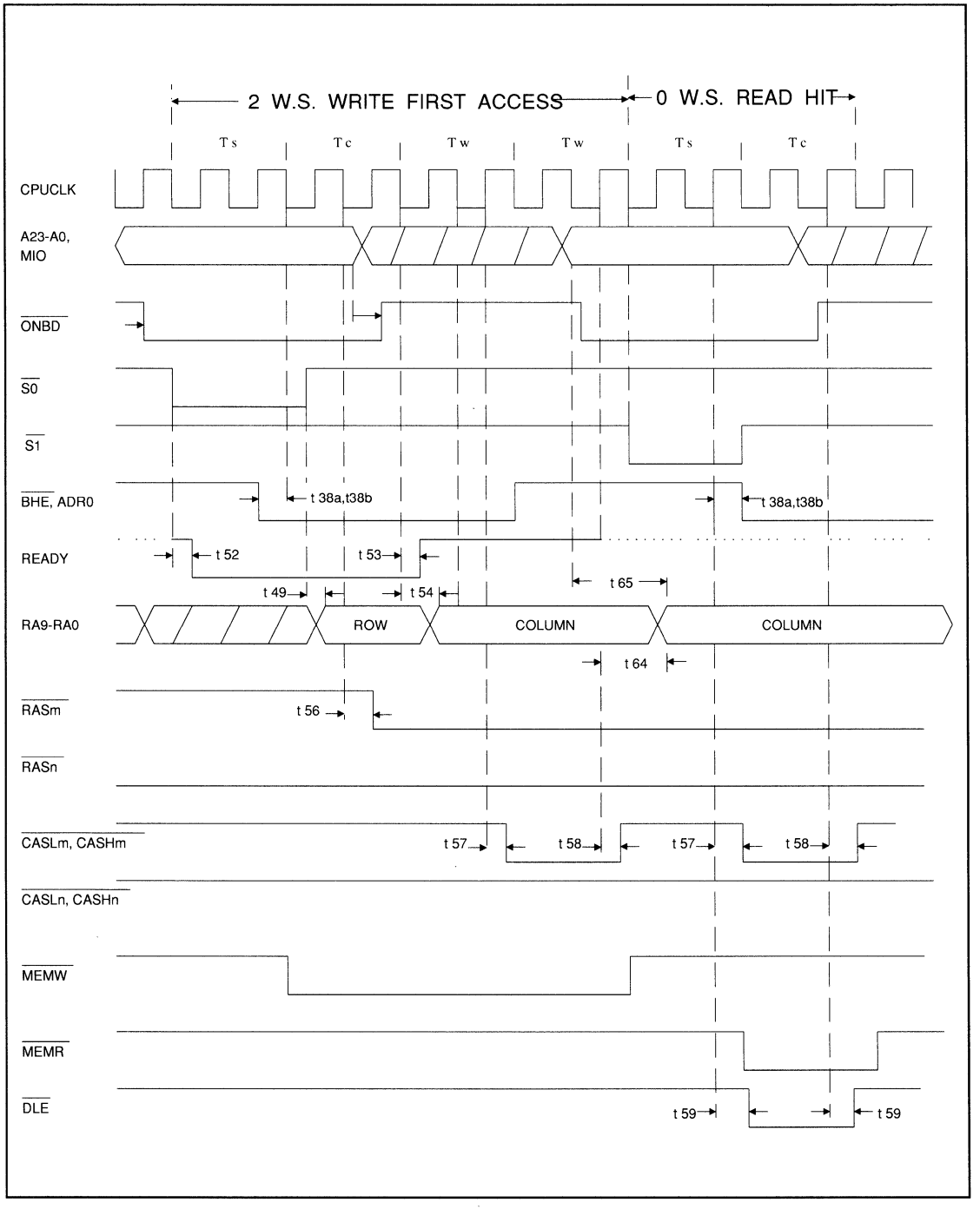


Figure 11. Memory Mode 2 (PAGE) 1 0F 2

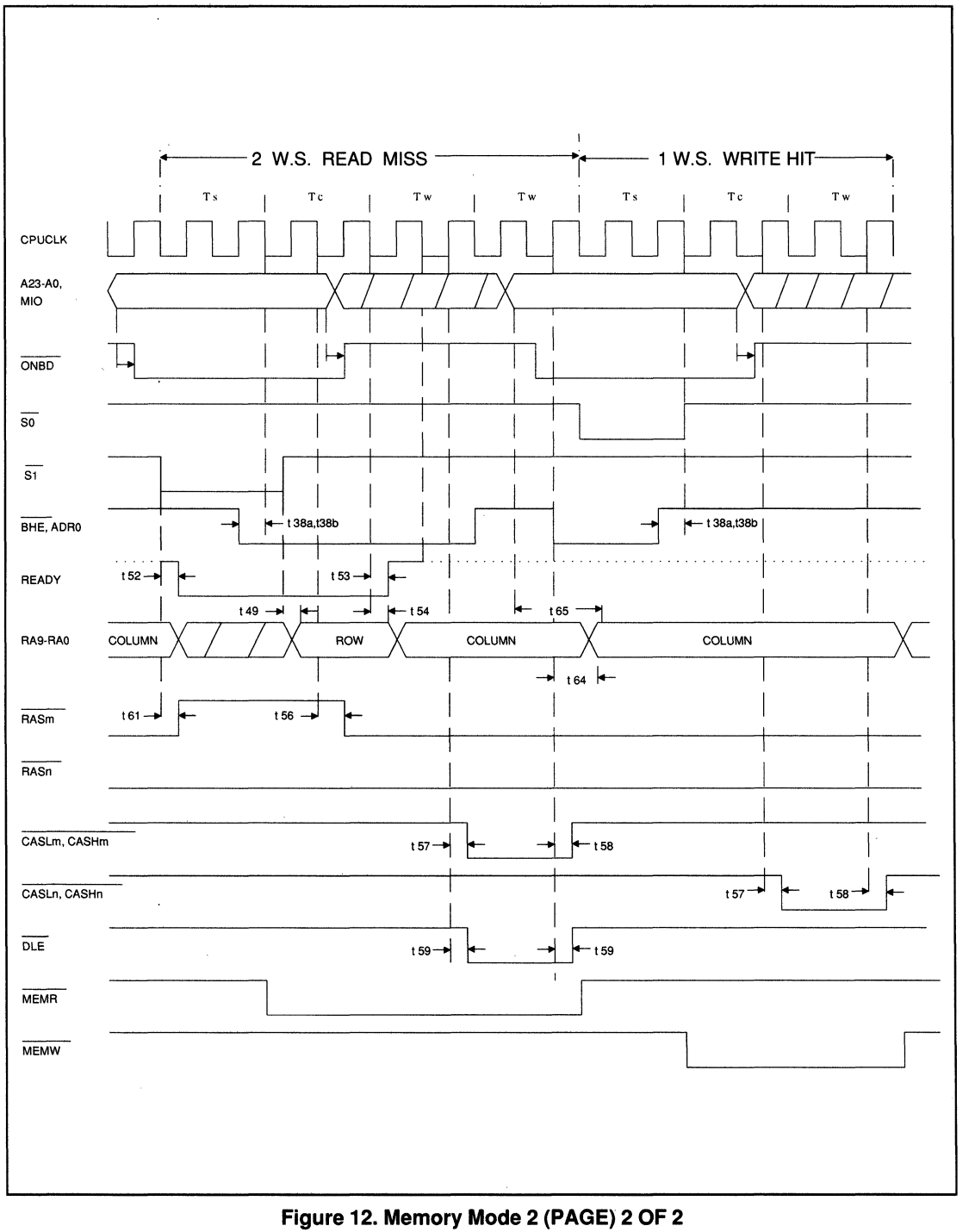


Figure 12. Memory Mode 2 (PAGE) 2 OF 2

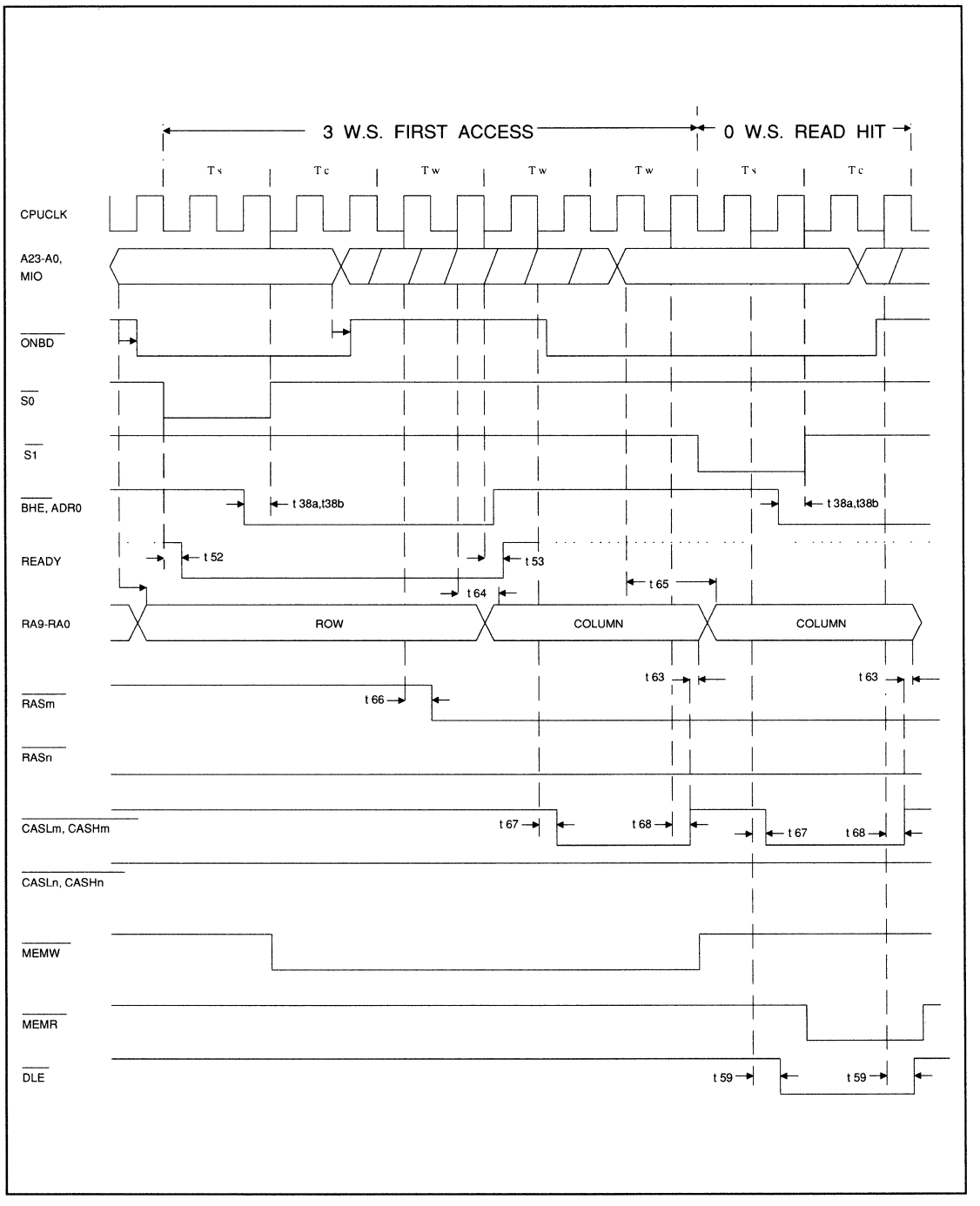


Figure 13. Memory Mode 3 (PAGE) 1 OF 2

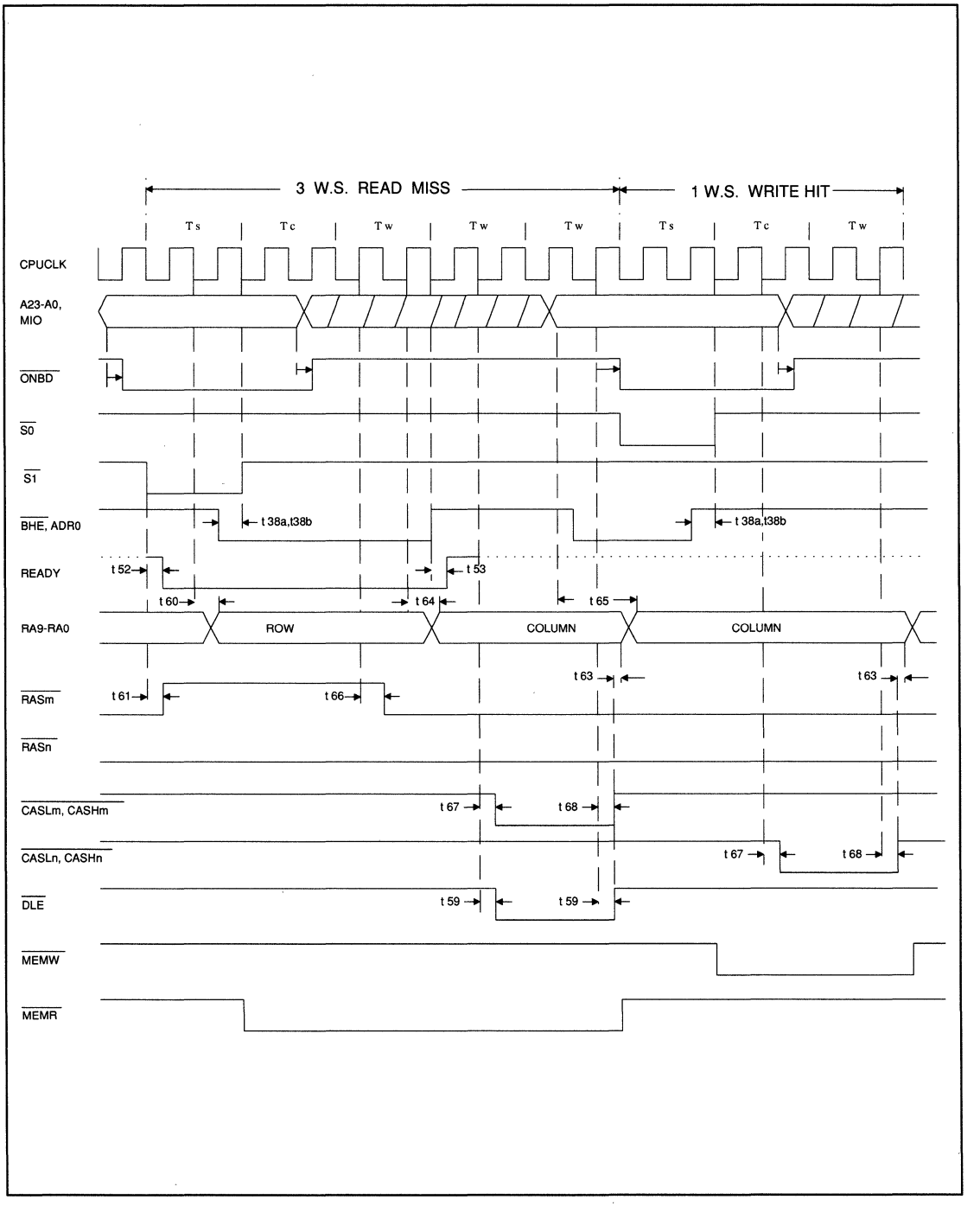


Figure 14. Memory Mode 3 (PAGE) 2 OF 2

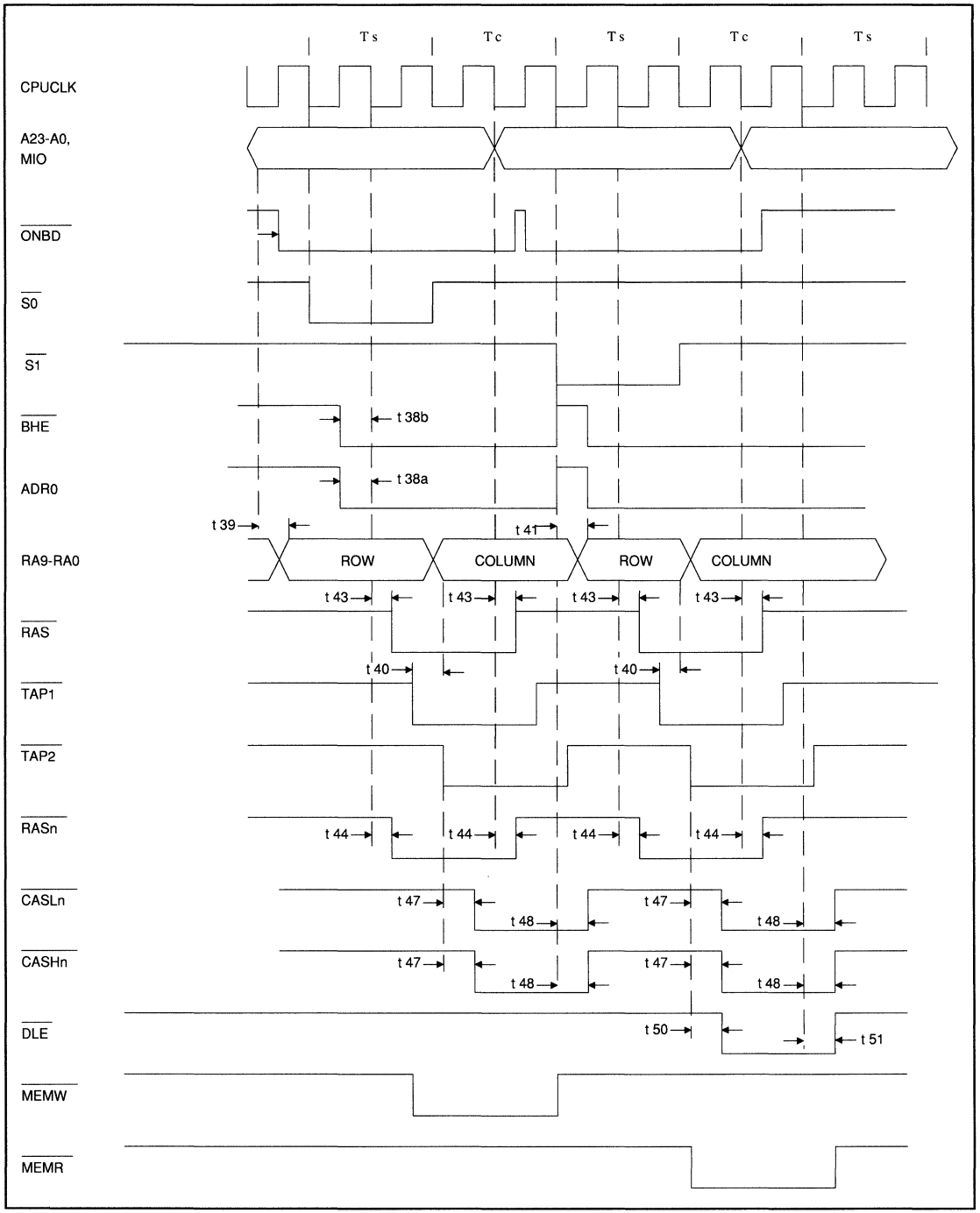


Figure 15. Memory Mode 5 (Non-Page) 0 WS Read & Write

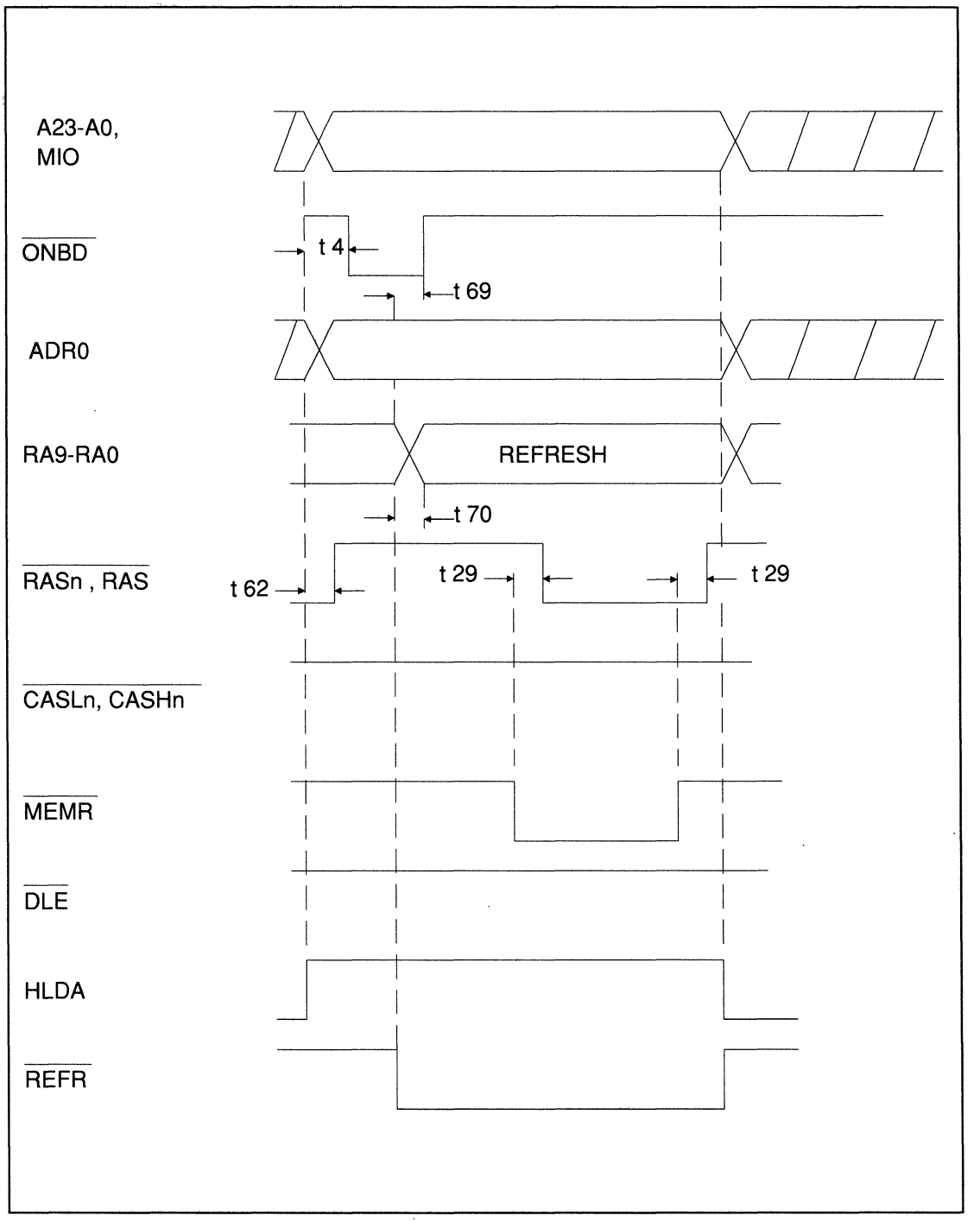
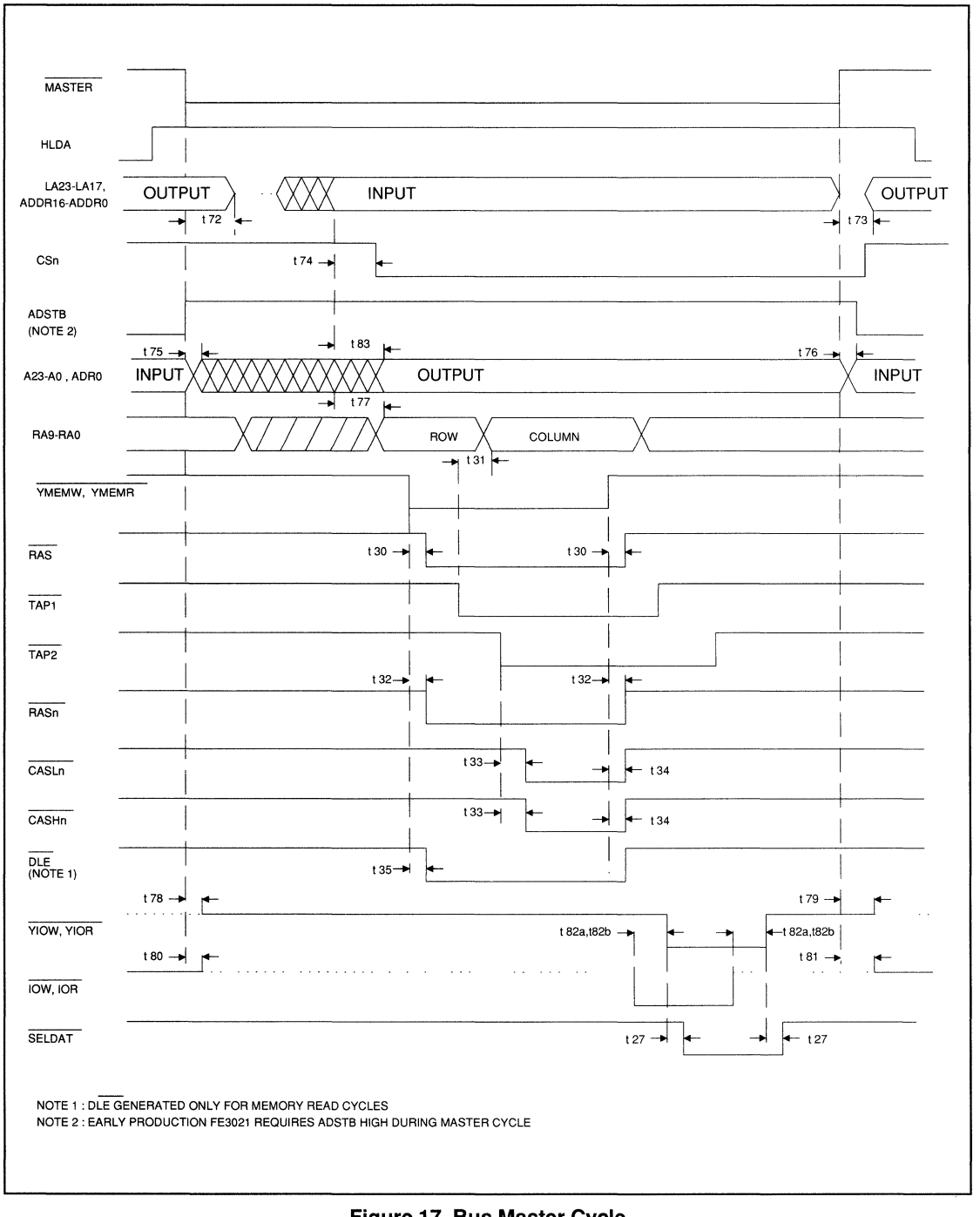


Figure 16. Refresh Cycle



NOTE 1 : DLE GENERATED ONLY FOR MEMORY READ CYCLES
NOTE 2 : EARLY PRODUCTION FE3021 REQUIRES ADSTB HIGH DURING MASTER CYCLE

Figure 17. Bus Master Cycle

14.0 PACKAGE DIAGRAMS

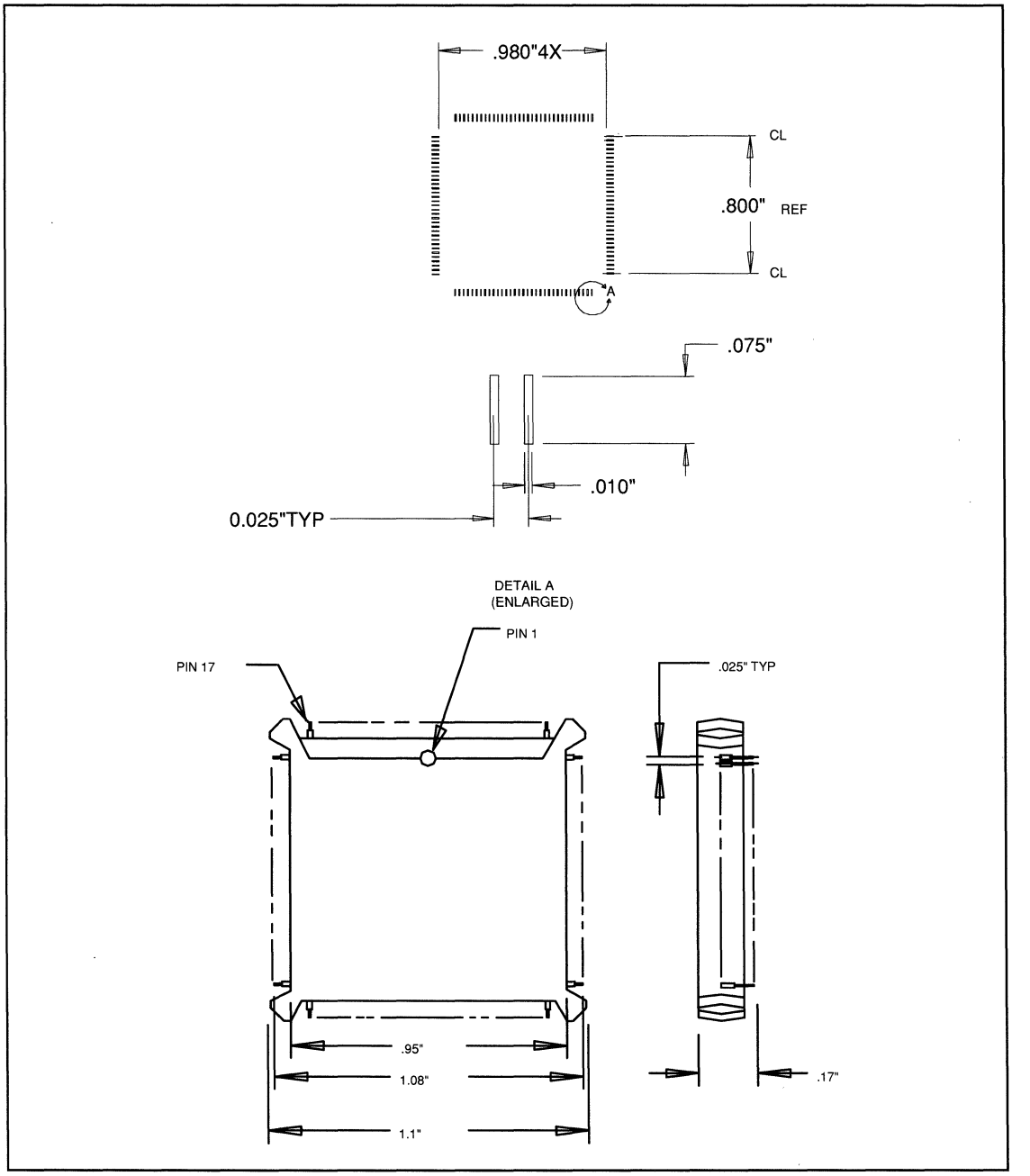
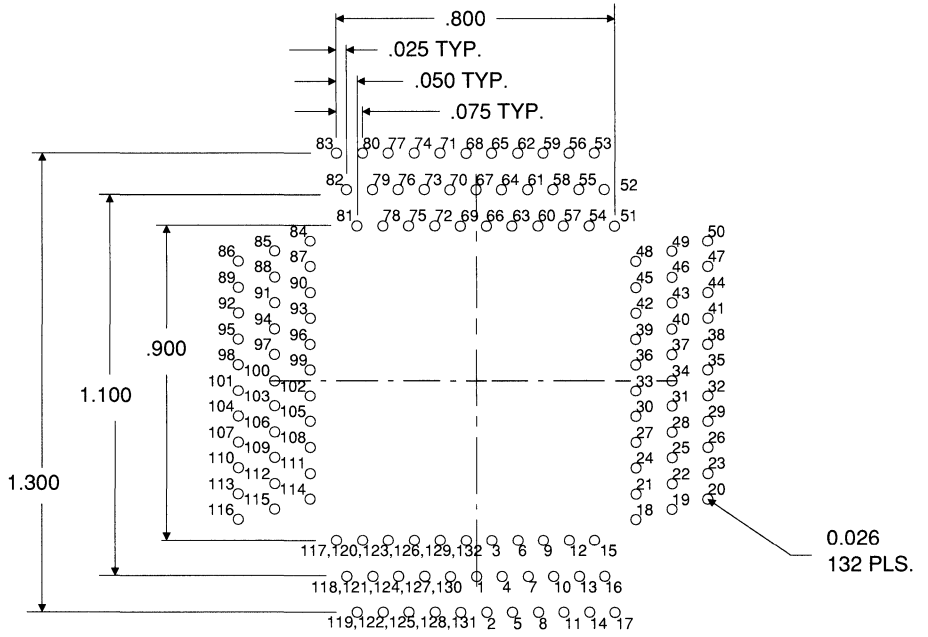


Figure 18. 132-Pin JEDEC Flat Pack Packaging Diagram



RECOMMENDED P.C. BOARD HOLE PATTERN
SOCKET SIDE
132 POSN

Amp Incorporated
Harrisburg PA
Part No. 821932-5

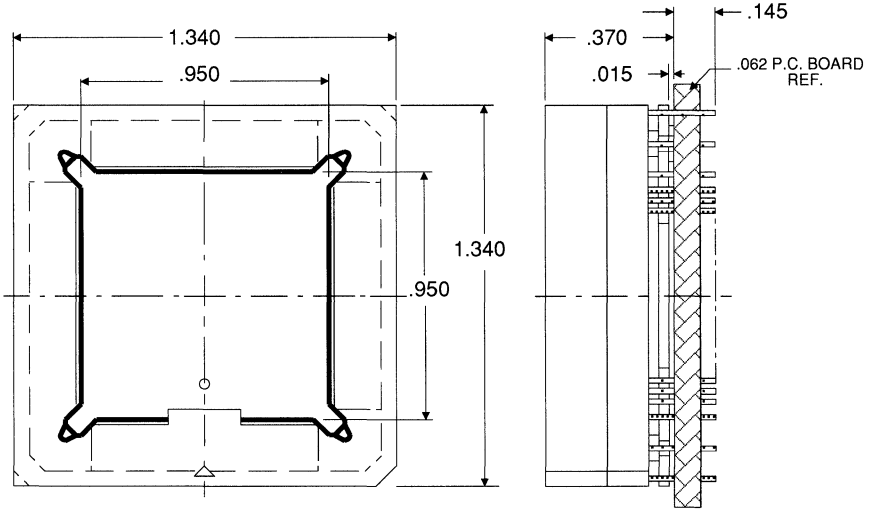


Figure 19. Socket Diagram

SYSTEMS LOGIC/PERIPHERAL

5

FE3021A

Address Buffer and Memory Controller

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

P R E F A C E

The FE3021A Address Buffer And Memory Controller device is an enhancement of the FE3021. Although the two devices are very similar in design, it is important to use the appropriate document when designing around the use of this device. The FE3021 literature order number is I0505. The FE3021A literature order number is I0503.

Some of the areas affected by the enhancement of the device are:

The FE3021A operates as a 20 MHz address buffer and memory controller using 80 ns DRAMs, as well as a 16 MHz using 100 ns DRAMs as does the FE3021.

The version numbers read from the Version Number Register (FFF01) are 010 = FE3021A and 100 = FE3021.

Bits 3 and 2 of the Hot Reset Register (FFF07) have been redefined. Bit 3 = 1 to tri-state ADDR0 (pin 105), bit 2 no longer has a function and bits 1 and 0 remain unchanged.

Page Mode 2 now operates at 16 MHz with 80 ns DRAMs as well as 12.5 MHz with 120 ns DRAMs.

The efficiency of all timing parameters have been increased considerably.

1.0 DESCRIPTION

The FE3021A is a 20 MHz AT address buffer and memory controller in a 132-pin PQFP package. Chip count is significantly reduced by integrating the memory controller, AT bus address buffers, and I/O into one chip. The memory controller is a high performance design, with programmable modes of operation. It controls page mode DRAM or static column DRAM. Up to 4 banks of DRAM, allowing a maximum of 8 Mbytes of memory can be controlled by the FE3021A. The DRAM bank locations are programmable on 128 Kbyte boundaries. One memory bank allows split addressing, so that one portion may be placed in conventional memory with the remainder in extended memory.

Additional features of the FE3021A include EMS 4.0 support, on-chip address and control signal buffers for directly driving the AT bus, zero wait state access at 16 MHz using 100 ns DRAM with page mode access, generation of chip selects for floppy controller, 8042 keyboard controller, 80287 numeric processor, and NMI, and mapping main and EGA/VGA BIOS into one physical PROM.

1.1 FEATURES

- Page mode DRAM access with interleaved memory banks
- Controls up to 4 banks (up to 8 Mbytes) of memory
- On-chip RAS and CAS drivers for DRAM chips
- On-chip DRAM address multiplexer
- LIM (Lotus, Intel, Microsoft) standard EMS expanded memory hardware (supports EMS 4.0 multi-tasking)
- On-chip address and control signal buffers for directly driving AT bus
- Zero wait state access at 16 MHz using 100 ns DRAM with page mode access and up to 20 MHz with 80 ns DRAM
- Generates chip selects for floppy controller, 8042 keyboard controller, 80287 numeric processor, and NMI (Non-maskable Interrupt)
- Generates programmable chip selects for four additional devices
- Address buffer and memory controller for the four chip core logic set
- Maps system BIOS and EGA BIOS into one physical PROM
- "Hot" reset generation for quick 80286 switch from protected to real mode
- Fast Alternate Gate A20 generation
- Interfaces with the FE3600/B/C chip set devices FE3001/A, FE3010/B/C, and FE3031/A
- 132-pin JEDEC PQFP (plastic quad flat package)

1.2 INTRODUCTION

The FE3021A device is designed to reduce chip count, increase flexibility, and provide improved operating speed and functionality when used with the FE3001/A, FE3010B/C, and FE3031/A devices to implement a low cost, high performance AT compatible computer at speeds up to 20 MHz. Together these four chips make up the FE3600B/C chip set.

Chip count is reduced by integrating the memory controller, AT bus address buffers, and I/O Management functions into one chip.

The memory controller is a high performance design, with programmable modes of operation. It controls page mode DRAM or static column DRAM.

Up to 4 banks of DRAM may be controlled. The DRAM bank locations are programmable on 128 Kbyte boundaries. One memory bank allows split addressing, so that one portion may be placed in conventional memory with the remainder in extended memory, with an additional mode to allow copying BIOS code from ROM to RAM for faster execution.

A major function of the FE3021A is to generate chip select decodes for peripheral chips on the system board; for instance, the floppy controller, hard disk controller, serial, and parallel port chips. The floppy and hard disk chip selects may be disabled or may be enabled for either the primary or secondary address decode, as defined by IBM. Four programmable chip selects are available, for supporting serial, parallel, mouse, or other types of ports. Refer to Figure 7 for Pin assignment and locations.

To reduce chip count and improve performance, particularly when an EGA or VGA graphics controller is placed on the system board, separate blocks of ROM may be mapped into a single physical ROM. For instance, the EGA BIOS and standard BIOS may be placed into the same pair of ROM chips or into a single 8-bit wide ROM. Besides reducing chip count, EGA operating speed will be improved, since EGA BIOS will be accessed 16 bits at a time. To improve BIOS performance, ROM code may be copied into RAM, and the BIOS ROM mapped out and replaced by RAM.

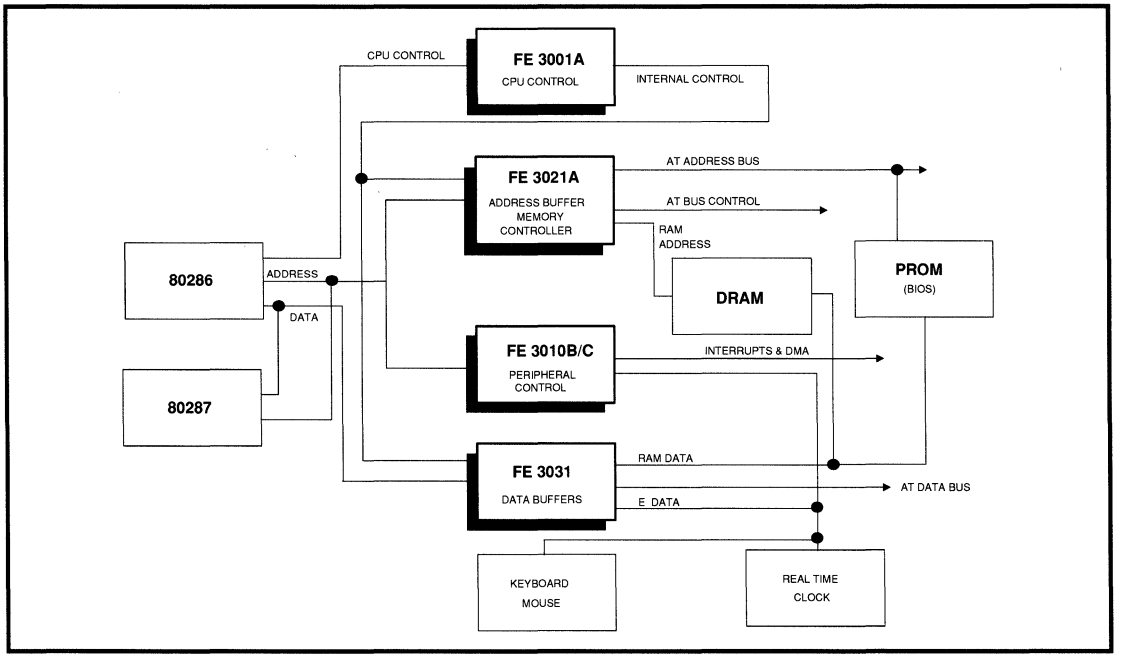


FIGURE 1. FE3600B/C CHIP SET FUNCTIONAL BLOCK DIAGRAM

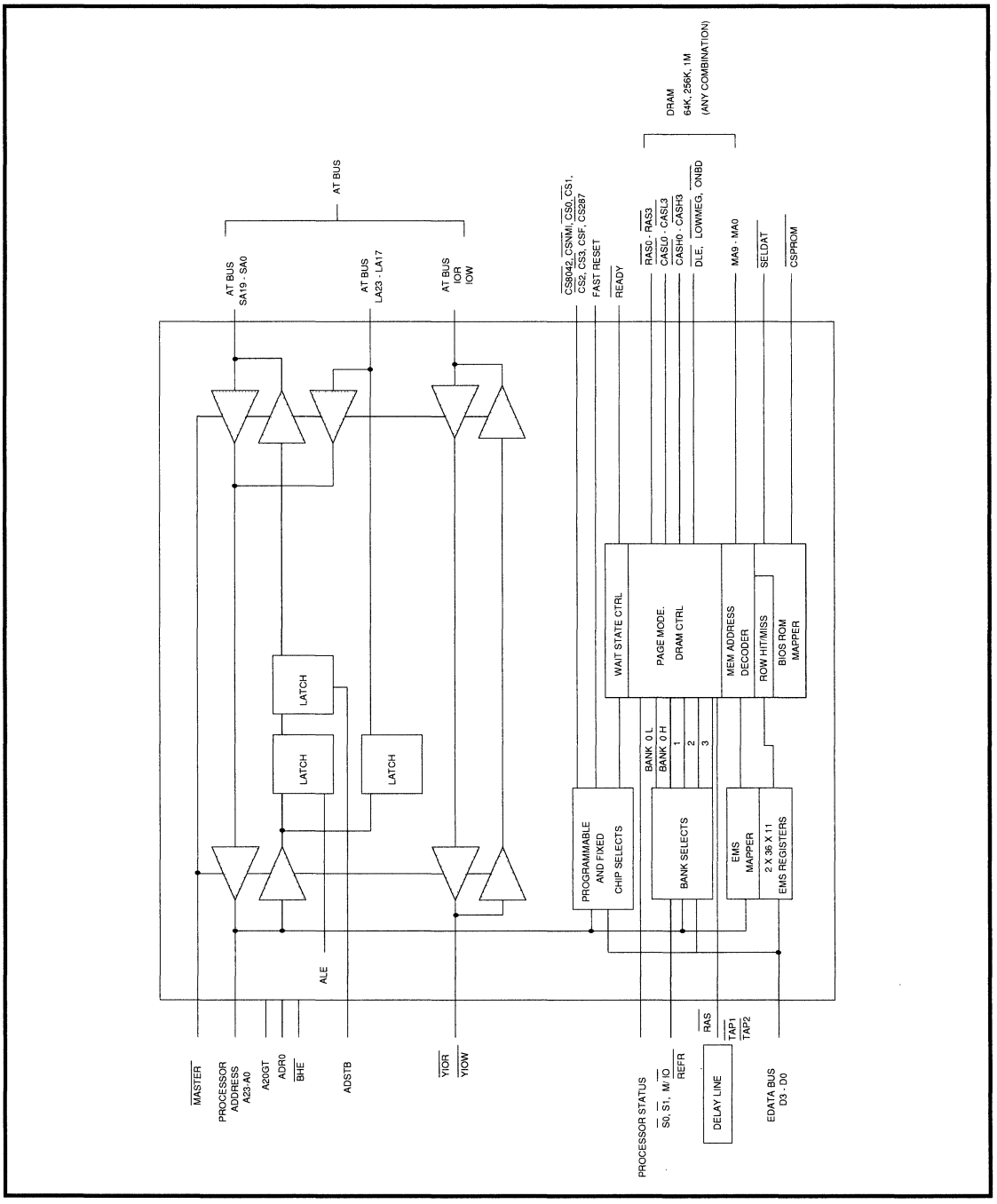


FIGURE 2. FE3021A FUNCTIONAL BLOCK DIAGRAM

2.0 80286 INTERFACE

This interface port connects with the 80286 address lines and the 80286 bus status lines. By connecting directly to the 80286 and by duplicating a portion of the bus controller logic, early determination of memory or I/O accesses may be made, as well as whether the access will be 8 bits or 16 bits. Pins A23-A0 are normally inputs, receiving addresses from the 80286. When $\overline{\text{MASTER}}$ is asserted, these pins become outputs.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
74	A23	I/O	80286 ADDRESS LINE
78	A22	I/O	" "
79	A21	I/O	" "
80	A20	I/O	" "
81	A19	I/O	" "
82	A18	I/O	" "
83	A17	I/O	" "
84	A16	I/O	" "
85	A15	I/O	" "
86	A14	I/O	" "
87	A13	I/O	" "
88	A12	I/O	" "
89	A11	I/O	" "
90	A10	I/O	" "
109	A9	I/O	" "
110	A8	I/O	" "
111	A7	I/O	" "
112	A6	I/O	" "
113	A5	I/O	" "
114	A4	I/O	" "
115	A3	I/O	" "
116	A2	I/O	" "
117	A1	I/O	" "
118	A0	I/O	" "
119	$\overline{\text{S0}}$	I	80286 STATUS LINE
120	$\overline{\text{S1}}$	I	80286 STATUS LINE
121	M/$\overline{\text{IO}}$	I	80286 STATUS LINE
122	CPUCLK	I	80286 CLOCK
123	HLDA	I	80286 HOLD ACKNOWLEDGE LINE
21	$\overline{\text{BHE}}$	I	80286 BYTE HIGH ENABLE

TABLE 1. 80286 INTERFACE PIN ASSIGNMENTS

3.0 DATA BUS INTERFACE

The data bus port is 4 bits wide, which should connect to the EDATA local data bus, and is used to access the internal FE3021A control registers. The upper 4 bits should be ignored when reading the control registers. Refer to Table 2 for pin assignments.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
17	EDATA3	I/O	Control Register Data Line
16	EDATA2	I/O	" "
15	EDATA1	I/O	" "
14	EDATA0	I/O	Control Register Data Line

TABLE 2. DATA BUS INTERRFACE PIN ASSIGNMENTS

4.0 I/O CHIP SELECTS

This logic section generates chip selects for standard system board functions such as the 8042 keyboard controller, 80287 math coprocessor, floppy controller, and hard disk controller. It also generates chip selects for up to 4 additional I/O ports which may have programmable addresses and wait state characteristics. Refer to Table 3 for pin assignments.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
48	$\overline{CS0}$	O	Programmable Chip Select 0
47	$\overline{CS1}$	O	Programmable Chip Select 1
46	$\overline{CS2}$	O	Programmable Chip Select 2
45	$\overline{CS3}$	O	Programmable Chip Select 3 or H. D. Controller Chip Select
49	CSF	O	Floppy Disk Controller Chip Select or Operation or Config. Register Select
60	$\overline{CS8042}$	O	8042 Keyboard Controller Select
56	$\overline{CS287}$	O	80287 Coprocessor Select/ROM Chip Select
20	$\overline{CSNMI}$	O	NMI Logic Chip Select
22	$\overline{CSPTB}$	O	Memory Parity and I/O Check

TABLE 3. I/O CHIP SELECT PIN ASSIGNMENTS

5.0 I/O CONTROL

This logic section contains control logic for the I/O bus.

The IORDY signal will go low when generating wait states. For 12 MHz systems, this signal may be tied directly to the bus signal IOCHRDY. For 16 MHz or 20 MHz systems, this signal should be sent to the FE3001A directly. The IOCHRDY bus signal should be buffered through an open collector driver and wire-ORed with the IORDY signal. The IORDY pin will normally be at a high impedance state. When generating wait states, it will go low. When going from a low to a high state, the IORDY pin will be actively driven high for one processor clock time, then the output will tri-state. An external pullup resistor should be used to keep the IORDY signal high when the IORDY pin is at a high impedance state. The state of IORDY is sampled at the rising edge of $\overline{\text{RESET}}$; if IORDY is low at this time, the FE3021A will fetch data and instructions from the BIOS ROM 8 bits at a time over the EDATA bus, otherwise a 16-bit wide ROM on the MDATA bus is assumed.

The PORT 0, PORT 1, PORT 2, and PORT 3 addresses are fully programmable, with the choice of either using nine I/O addresses for decode, or masking the A8 address bit (for instance, for decoding dual serial ports). The LSB (A0) address is always ignored. The lower 2, 3, or 4 bits of the address may also be ignored so that 2, 4, 8, or 16 bytes may be allocated for the port.

All FE3021A control registers, except those used for EMS page mapping, are accessed by first writing eight times to address FFF00 (in an area allocated for ROM BIOS). Any memory access outside of the ROM BIOS address space, either data access or instruction fetch, will abort the unlocking process. Once unlocked, memory accesses outside of the ROM BIOS area may be made without affecting the unlocked state. When unlocked, the address space from FFF01 to FFFFE becomes register controls for the FE3021A device. The controls are locked again by reading location FFFFF. This access method guarantees that all control register changes will be made through the BIOS.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
127	IORDY	I/O	Ready line, modified open drain, input at reset time for 8-bit ROM sizing.
40	$\overline{\text{SELDAT}}$	O	Direction of data transceiver data to EDATA bus.
8	$\overline{\text{IOR}}$	I/O	System I/O Read Command signal, drives expansion bus. An input in master mode.
9	$\overline{\text{IOW}}$	I/O	System I/O Write Command signal, drives expansion bus. An input in master mode.
10	$\overline{\text{YMEMR}}$	I	Ungated system memory Read Command signal from FE3001A.
11	$\overline{\text{YMEMW}}$	I	Ungated system memory Write Command signal from FE3001A.
53	ADSTB	I	Address strobe from FE3001A and FE3010B/C.
12	$\overline{\text{YIOR}}$	I/O	Ungated I/O read strobe from FE3001A. An output in master mode.
13	$\overline{\text{YIOW}}$	I/O	Ungated I/O write strobe from FE3001A. An output in master mode.
19	$\overline{\text{FRES}}$	I/O	"HOT" reset output
25	$\overline{\text{LOMEG}}$	O	To FE3031 memory strobe gating.
28	$\overline{\text{RESET}}$	I	Master Reset for FE3021A.
52	$\overline{\text{MASTER}}$	I	Bus master signal from the AT bus.
54	A20GT	I	From 8042. When high, A20 is ungated.
57	$\overline{\text{ONBD}}$	O	To FE3001A. Indicates high speed on-board access.

TABLE 4. I/O CONTROL PIN ASSIGNMENTS

PIN NUMBER	MNEMONIC	I/O	FUNCTION
59	ADDR19	O	AT BUS SA19
61	ADDR18	O	AT BUS SA18
62	ADDR17	O	AT BUS SA17
64	ADDR16	I/O	AT BUS SA16
65	ADDR15	I/O	AT BUS SA15
66	ADDR14	I/O	AT BUS SA14
68	ADDR13	I/O	AT BUS SA13
69	ADDR12	I/O	AT BUS SA12
72	ADDR11	I/O	AT BUS SA11
73	ADDR10	I/O	AT BUS SA10
75	ADDR9	I/O	AT BUS SA 9
94	ADDR8	I/O	AT BUS SA8
96	ADDR7	I/O	AT BUS SA7
97	ADDR6	I/O	AT BUS SA6
98	ADDR5	I/O	AT BUS SA5
100	ADDR4	I/O	AT BUS SA4
101	ADDR3	I/O	AT BUS SA3
104	ADDR2	I/O	AT BUS SA2
106	ADDR1	I/O	AT BUS SA1
105	ADDR0	I/O	AT BUS SA0
63	LA23	I/O	AT BUS LA23
70	LA22	I/O	AT BUS LA22
71	LA21	I/O	AT BUS LA21
93	LA20	I/O	AT BUS LA20
95	LA19	I/O	AT BUS LA19
102	LA18	I/O	AT BUS LA18
103	LA17	I/O	AT BUS LA17

TABLE 4. I/O CONTROL PIN ASSIGNMENTS (Cont.)

A Version Number register provides information on the version of the FE3021A chip. It also contains a bit which toggles between '0' and '1' when the register is read, which provides indication that the register set has been unlocked.

VERSION NUMBER

	7	6	5	4	3	2	1	0
FFF01	X	X	X	X	VER			T

T : toggles between 0 and 1 with every read access of the Version Number register.

VER : 000 when T=0
010 when T=1 for version FE3021A
100 when T=1 for version FE3021

System board devices may be located on the EDATA bus rather than on the I/O expansion slot DATA bus. The $\overline{\text{SELDAT}}$ signal which controls the DATA to EDATA bus direction is affected by the two port location registers. This option is available for peripheral devices which cannot directly drive the high current I/O slot DATA bus. Note, however, that DMA transfers cannot be made to devices on the EDATA bus.

The $\overline{\text{SELDAT}}$ signal is active (low) when $\overline{\text{IOR}}$ is active and address bits A8 and A9 are low, or the PORTS LOCATION register indicates that an addressed port is on the EDATA bus. The $\overline{\text{SELDAT}}$ signal is also low when $\overline{\text{MEMR}}$ is active and the **8-bit** BIOS is being accessed.

PORTS LOCATION REGISTER

	7	6	5	4	3	2	1	0
FFF06	X	X	X	X	A	B	C	D

The Ports Location Register is cleared by a master reset.

A = 0 Port 0 On Data Bus
A = 1 Port 0 On Edata Bus

B = 0 Port 1 On Data Bus
B = 1 Port 1 On Edata Bus

C = 0 Port 2 On Data Bus
C = 1 Port 2 On Edata Bus

D = 0 Port 3 On Data Bus
D = 1 Port 3 On Edata Bus

HOT RESET REGISTER

	7	6	5	4	3	2	1	0
FFF07	X	X	X	X	T	X	A	H

The Hot Reset Register is cleared by a master reset.

Register FFF07 is used to generate a hot reset to the processor or to generate an alternate A20 gate. The state of the A bit is ORed with the A20GT pin. If either the A bit is set or the A20GT pin is high, the A20 line is undisturbed. If both are low, then the A20 line is gated low. A hot reset is generated by changing the H bit from a '0' to a '1'. 131 clocks after the trailing edge of the $\overline{\text{MEMW}}$ strobe, the $\overline{\text{FRES}}$ pin is pulled low. The reset pulse lasts for 32 clocks, then the $\overline{\text{FRES}}$ pin is actively pulled high for one clock cycle, then is tri-stated. If the $\overline{\text{FRES}}$ pin is pulled low externally (e.g. if wire-OR'ed with the 8042 CPU reset line), then the internal FE3021A registers will relock. If the $\overline{\text{FRES}}$ pin is not used, then it should be pulled up externally.

When the T bit is set, ADDR0 is tri-stated (pin 105).

ENABLE PORTS REGISTER

	7	6	5	4	3	2	1	0
FFF10	X	X	X	X	EN3	EN2	EN1	EN0

The Enable Ports Register is cleared by a master reset.

The programmable PORT 0, PORT 1, PORT 2, and PORT 3 chip selects are enabled with the Enable Ports register. If the Enable bit is 0, the port chip select bit will always be at an inactive (high) state. All four ports are disabled after master reset. EN3 enables $\overline{CS3}$ only when $\overline{CS3}$ is a programmed chip select. When $\overline{CS3}$ is a HDC chip select, CS3 is enabled by register FFF49, bit 1.

For ports 0, 1, and 2, the access will have the default wait states: 1 wait state for 16 bit accesses and 4 wait states for 8 bit accesses, with the wait states set from the FE3001A. The selected chip must generate $\overline{IOCS16}$ if it is a 16-bit peripheral.

PORT 3 CONTROL REGISTER

	7	6	5	4	3	2	1	0
FFF08	X	X	X	X	WS		WSE	OB

The Port 3 Control Register is cleared by a master reset.

WS	HDC DATA PORT HIGH SPEED WAIT STATES
00	1
01	2
10	3
11	4

0B	$\overline{CS3}$ WAIT STATES
0	Default (slow)
1	High speed hard disk controller

WSE	HIGH SPEED HDC WAIT STATE ENABLE
0	High speed HDC wait states set by FE3001A
1	High speed HDC Wait States set by WS field

For port 3, the access will normally have the default wait states but may also be programmed to have high speed wait state timing when $\overline{CS3}$ is programmed as a hard disk chip select and the on-board 16-bit hard disk controller is capable of high speed access. When the high speed disk controller configuration is used, the WSE and OB fields should be set to '1', and the WS field will set the number of high speed wait states, timed from the CPUCLK, rather than from SYSCLK. The other disk controller ports will always be accessed at low speed.

When 0B is set to a 1, the FE3021A will generate the $\overline{ONBD}$ signal to the FE3001A during HDC accesses through port 3. The FE3001A will provide the same number of wait states it does for on-board memory. If it is desired, the number of wait states for the HDC can be extended using the WS and WSE fields.

When implementing a high speed disk controller port, it is necessary to provide a separate address path for the hard disk controller. The HDC receives ungated I/O read and write strobes at the full CPU speed. The following schematic illustrates the required connections.

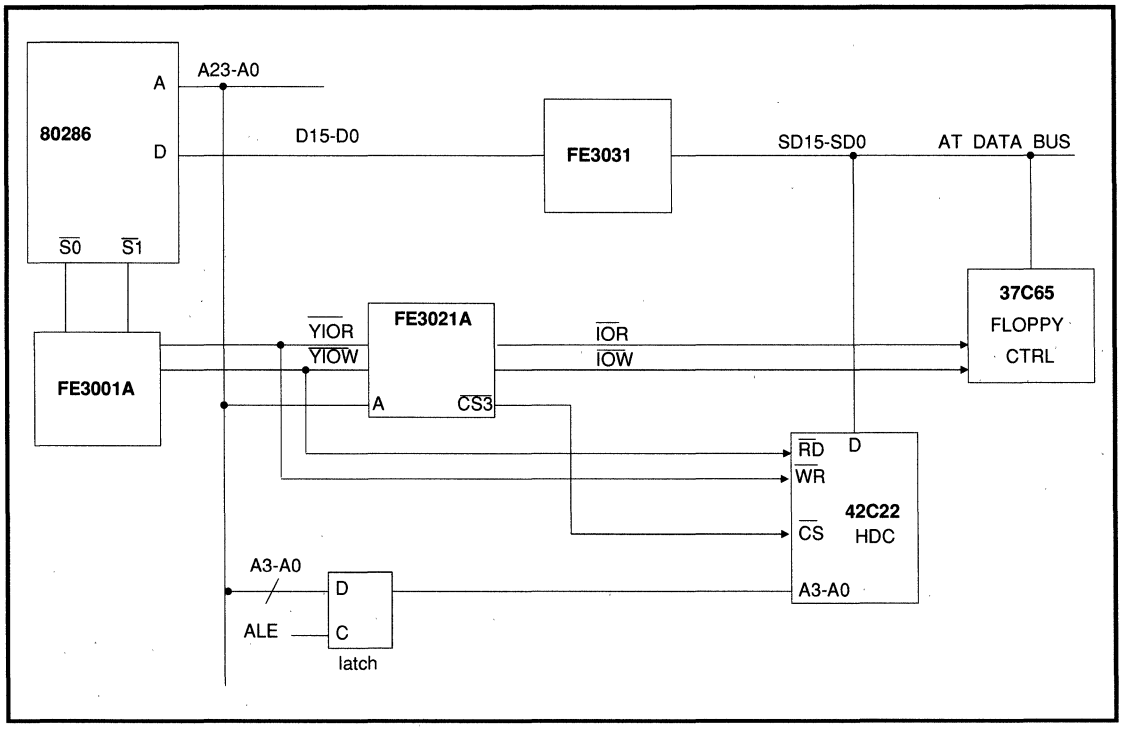


FIGURE 3. HIGH SPEED HDC CONFIGURATION

PORT ADDRESS MASK REGISTER

FFF09
FFF11
FFF19
FFF21

X	X	X	X	O	U	LMASK	
7	6	5	4	3	2	1	0

The Port Address Mask Register is cleared by a master reset.

5

LMASK	ADDRESS BITS COMPARED									
00	A9	A8	A7	A6	A5	A4	A3	A2	A1	X
01	A9	A8	A7	A6	A5	A4	A3	A2	X	X
10	A9	A8	A7	A6	A5	A4	A3	X	X	X
11	A9	A8	A7	A6	A5	A4	X	X	X	X

U = 0 : Include A8 In Address Comparison

LMASK	ADDRESS BITS COMPARED									
00	A9	X	A7	A6	A5	A4	A3	A2	A1	X
01	A9	X	A7	A6	A5	A4	A3	A2	X	X
10	A9	X	A7	A6	A5	A4	A3	X	X	X
11	A9	X	A7	A6	A5	A4	X	X	X	X

U = 1 : Ignore A8 In Address Comparison

PORT	PORT CONTROL REGISTER ADDRESS
0	FFF09
1	FFF11
2	FFF19
3	FFF21

NOTE: Bit 3 is not writable and is always '0'.

PORT ADDR - LOWER MSB

FFF0A
FFF12
FFF1A
FFF22

X	X	X	X	X	X	A9	A8
7	6	5	4	3	2	1	0

PORT ADDR - UPPER LSB

FFF0B
FFF13
FFF1B
FFF23

X	X	X	X	A7	A6	A5	A4
7	6	5	4	3	2	1	0

PORT ADDR - LOWER LSB

FFF0C
FFF14
FFF1C
FFF24

X	X	X	X	A3	A2	A1	0
7	6	5	4	3	2	1	0

The Port I/O Address registers for all four ports are set to all zeros by a master reset.

PORT	PORT I/O ADDRESS REGISTERS		
	A9-A8	A7-A4	A3-A0
0	FFF0A	FFF0B	FFF0C
1	FFF12	FFF13	FFF14
2	FFF1A	FFF1B	FFF1C
3	FFF22	FFF23	FFF24

	ADDR2	ADDR1	CSF
OPERATIONS REGISTER ACCESS	0	X	1
CONFIG REGISTER ACCESS	1	1	1
FLOPPY CHIP SELECT ACTIVE	X	0	1

Table 5 lists the I/O addresses and chip selects generated for each fixed port type. The chip selects are not gated with $\overline{IOR}$ or $\overline{IOW}$. The $\overline{CSNMI}$ signal is decoded for both even and odd addresses, so that access may be made to the FE3001A control register at address 073.

The floppy controller operations register select, configuration register select, and floppy disk controller chip select may be generated from the CSF pin and the ADDR2 and ADDR1 lines.

PORT	BIT SIZE	I/O ADDRESS	ACTIVE SIGNAL	FUNCTION
FLOPPY	8	3F2 372	CSF	FDC operation select. 3F2 is primary address, 372 is secondary.
	8	3F4-3F5 374-375	CSF	3F4-3F5 are primary addresses, 374-375 are secondary.
	8	3F6 376	$\overline{CS3}$*	Hard disk controller chip select. 3F6 is primary address, 376 is secondary.
	8	3F7 377	CSF $\overline{CS3}$*	$\overline{CS3}$ and CSF pins will be asserted. 3F7 is primary address, 377 is secondary.
80287	8	0E0-0FF	$\overline{CS287}$	80287 Chip Select.
8042	8	060-06E (EVEN)	$\overline{CS8042}$	8042 Chip Select.
NMI LOGIC	8	070-07F	$\overline{CSNMI}$	Real Time Clock and NMI logic select.
PARITY CHECK	8	061-06F (ODD)	$\overline{CSPTB}$	Parity check select and Port B decode. External logic must separate the signals.
HARD DISK	16	1F0 170	$\overline{CS3}$ *	HDC Chip Select - Data Port access. 1F0 IS primary address, 170 is secondary.
	8	1F1-1F7 171-177	$\overline{CS3}$	HDC Chip Select - Task File. 1F1-1F7 are primary addresses, 171-177 are secondary.

TABLE 5. I/O ADDRESS/CHIP SELECTS FOR FIXED PORTS

*When $\overline{CS3}$ pin is programmed as HDC Chip Select .

PRIMARY / SECONDARY PORT FUNCTION SELECT

	X	X	X	X	DH	PS	H	F
FFF49	7	6	5	4	3	2	1	0

DH, PS, H, and F are cleared to '0' by master reset

DH=0: $\overline{CS3}$ pin will respond to address programmed by FFF22-FFF24
DH=1: $\overline{CS3}$ pin will respond to hard disk addresses

PS=0: Primary hard disk and floppy disk address
PS=1: Secondary hard disk and floppy disk address

H=0: On-board hard disk controller enabled
H=1: Disable on-board hard disk controller

F=0: On-board floppy disk controller enabled
F=1: Disable on-board floppy disk controller

NOTE: For early production version (ID Register= 0000, 1011) bits 2 - 0 had different definitions:

Bit 2 = 0 : Enable CSF Output
Bit 1 = 0 : Primary Hard Disk Address
Bit 0 = 0 : Primary Floppy Disk Address

6.0 MEMORY CONTROL

Four RAS pins are available for controlling up to four 16-bit wide banks of system board RAM. Eight CAS pins control the low and high bytes of each bank. During a refresh cycle, all RAS signals will be active (ignoring the RAM configuration register FFF57) and CAS signals will stay inactive.

The RAS and CAS lines drive the DRAM array directly.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
128	$\overline{RAS0}$	O	RAS signal for DRAM Memory Bank 0
129	$\overline{RAS1}$	O	RAS signal for DRAM Memory Bank 1
130	$\overline{RAS2}$	O	RAS signal for DRAM Memory Bank 2
132	$\overline{RAS3}$	O	RAS signal for DRAM Memory Bank 3
125	$\overline{CASL0}$	O	CAS signal for DRAM Memory Bank 0, low byte
126	$\overline{CASL1}$	O	CAS signal for DRAM Memory Bank 1, low byte
2	$\overline{CASL2}$	O	CAS signal for DRAM Memory Bank 2, low byte
3	$\overline{CASL3}$	O	CAS signal for DRAM Memory Bank 3, low byte
4	$\overline{CASH0}$	O	CAS signal for DRAM Memory Bank 0, high byte
5	$\overline{CASH1}$	O	CAS signal for DRAM Memory Bank 1, high byte
6	$\overline{CASH2}$	O	CAS signal for DRAM Memory Bank 2, high byte
131	$\overline{CASH3}$	O	CAS signal for DRAM Memory Bank 3, high byte
18	$\overline{REFR}$	I	Memory Refresh signal
43	$\overline{CSPROM}$	O	BIOS PROM select
26	$\overline{TAP2}$	I	Second tap output of RAS delay line
44	$\overline{TAP1}$	I	First tap output of RAS delay line
58	$\overline{RAS}$	O	To RAS delay line input
23	$\overline{DLE}$	O	To FE3031 memory data bus latch enable
24	ADR0	I	From FE3001A byte conversion

TABLE 6. MEMORY CONTROL PIN ASSIGNMENTS

7.0 MEMORY ADDRESS MULTIPLEXER

The memory address multiplexer generates the row and column addresses for the DRAM. The memory address multiplexer outputs should be buffered by external drivers when driving the memory array.

The memory address multiplexer supports three sizes of DRAM: 64K, 256K, and 1 MB. The three sizes of DRAM's may be intermixed in any order.

The memory address multiplexer is designed so that SIMM mounted DRAM's of the three different sizes may be inserted into SIMM sockets without the need to change board jumpers.

5

PIN NUMBER	MNEMONIC	I/O	FUNCTION
31	RA0	O	Memory address multiplexer output bit 0 (LSB)
32	RA1	O	Memory address multiplexer output bit 1
33	RA2	O	Memory address multiplexer output bit 2
34	RA3	O	Memory address multiplexer output bit 3
35	RA4	O	Memory address multiplexer output bit 4
36	RA5	O	Memory address multiplexer output bit 5
37	RA6	O	Memory address multiplexer output bit 6
38	RA7	O	Memory address multiplexer output bit 7
39	RA8	O	Memory address multiplexer output bit 8
41	RA9	O	Memory address multiplexer output bit 9 (MSB)

TABLE 7. MEMORY ADDRESS MULTPLEXER OUTPUT PIN ASSIGNMENTS

MEMORY MODE		MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
64K DRAM ADDRESS MULTIPLEXER CONFIGURATION											
INDEPENDENT	RAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
NON PAGE MODE	CAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A9
INDEPENDENT	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A9
PAGE MODE	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
2 WAY INTLV	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A17
PAGE MODE	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
4 WAY INTLV	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A18	A17
PAGE MODE	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
256K DRAM ADDRESS MULTIPLEXER CONFIGURATION											
INDEPENDENT	RAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
NON PAGE MODE	CAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A10	A17
INDEPENDENT	RAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A10	A17
PAGE MODE	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
2 WAY INTLV	RAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A19	A17
PAGE MODE	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
4 WAY INTLV	RAS	(A20)	A18	A16	A15	A14	A13	A12	A20	A19	A17
PAGE MODE	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
1 MBIT DRAM ADDRESS MULTIPLEXER CONFIGURATION											
INDEPENDENT	RAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
NON PAGE MODE	CAS	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
INDEPENDENT	RAS	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
PAGE MODE	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
2 WAY INTLV	RAS	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17
PAGE MODE	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
4 WAY INTLV	RAS	A20	A18	A16	A15	A14	A13	A22	A21	A19	A17
PAGE MODE	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
REFRESH ADDRESS - ALL DRAM SIZES											
		A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

TABLE 8. ADDRESS MULTIPLEXER CONFIGURATIONS

Note: Addresses in parentheses are not used by DRAM

SYSTEM BOARD ROM WAIT STATE CONTROL REGISTER

	7	6	5	4	3	2	1	0
FFF50	X	X	X	X	RWS		0	RWSE

This register is cleared to zero by master reset.

RWS	HIGH SPEED WAIT STATE
00 *	1
01	2
10	3
11	4

RWSE=1: Enables RWS, otherwise on-board ROM and RAM Wait States will be set by FE3001A.

The FE3021A can extend the number of processor wait states for an on-board BIOS access by setting the RWSE bit to a '1'. The number of wait states will then be determined by the value of the RWS field. If the RWSE bit is set to a '0', the number of wait states for an on-board BIOS access is controlled by the FE3001A.

The ability to add wait states for BIOS accesses is important for a 16-bit BIOS because the on-board memory read wait states programmed into the FE3001A apply to both on-board BIOS and on-board DRAM. That value will be programmed to optimize DRAM access time (typically zero wait states for page mode operations). This very fast access time will likely be too quick for BIOS ROMs and can therefore be extended for BIOS accesses by setting the RWSE bit.

Bit 1 is used for diagnostic purposes and should remain '0'.

The system BIOS address space may be from F0000 to FFFFF or E0000 to FFFFF. If the EGA BIOS is to be mapped, then the BIOS ROM chip select is also active when the region from C0000 to C3FFF or C0000 to C7FFF is addressed. The address output onto the expansion bus will be automatically translated. The BIOS PROM size and number of wait states will then apply to both the system BIOS region F0000-FFFFF and C0000-C3FFF.

The BIOS EPROM size may either be 8 bits or 16 bits. The EPROM size is determined at reset time, and is signaled by the IORDY line. If the IORDY line is high at the trailing edge of master reset, then the EPROM size is set to 16 bits. If the IORDY line is low at the trailing edge of master reset, then the EPROM size is set to 8 bits. No external logic is required for the 16 bit EPROM size. To select the 8 bit EPROM size, the IORDY line should be pulled low by a master reset. The MDATA bus is used for 16 bit EPROM's while the EDATA bus is used for 8 bit EPROM's.

The $\overline{\text{CSPROM}}$ signal is only active when $\overline{\text{MEMR}}$ is active.

MEMORY ADDRESS RANGE FOR ACTIVE $\overline{\text{CSPROM}}$	FUNCTION
0F0000-0FFFFF FF0000-FFFFFF	BIOS Size = 64K (Default)
0E0000-0FFFFF FE0000-FFFFFF	BIOS Size = 128K
0C0000-0C3FFF	16K EGA BIOS mapping enabled addresses translated to 0F8000-0FBFFF or 0F0000 - 0F3FFF
0C0000-0C7FFF	32K EGA BIOS mapping enabled addresses translated to 0F8000-0FFFFF or 0F0000 - 0F7FFF

EPROM / RAM MAP CONTROL REGISTER

	7	6	5	4	3	2	1	0
FFF51	X	X	X	X	EGA		MS	PS
FFF52	X	X	X	X	XLA	'0'	MLA	FAD

The EPROM/RAM Map Control Register is cleared to zero by a master reset.

EGA=00 MS=X: No EGA mapping.

EGA=01 MS=0: 16K EGA map. C0000 - C3FFF mapped to F8000 - FBFFF

MS=1: 16K EGA map. C0000 - C3FFF mapped to F0000 - F3FFF

EGA=10 MS=0: 32K VGA map. C0000 - C7FFF mapped to F8000 - FFFFF

MS=1: 32K VGA map. C0000 - C7FFF mapped to F0000 - F7FFF

PS = 0: PROM chip select will be active when address is 0F0000-0FFFFF or FF0000-FFFFFF, for 64K of BIOS. Default case after master reset.

PS = 1: PROM chip select will be active when address is 0E0000-0FFFFF or FE0000-FFFFFF, for 128K of BIOS.

XLA=0: LA23 - LA17 low speed timing

XLA=1: LA23 - LA17 high speed timing

MLA=0: LA23 - LA17 latches are transparent during refresh cycles

MLA=1: LA23 - LA17 gated to '0' during refresh cycles

FAD=0: 3 wait state EMS misses

FAD=1: 2 wait state EMS misses

Register FFF52 controls logic for various speed enhancement and diagnostic modes. The XLA bit controls the timing of the LA23 - LA17 signals. Use of this bit can affect compatibility of plug-in bus cards.

When XLA=0, LA23 - LA17 signals are generated by latching the processor addresses by active $\overline{S0}$ or $\overline{S1}$. The LA23 - LA17 latches become transparent when a $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, or $\overline{IOW}$ strobe occurs. This bit should be 0 when running at 8 MHz, when the FE3001A is using the low speed clock.

When XLA=1, LA23 - LA17 signals are latched by active $\overline{S0}$ or $\overline{S1}$, but do not become transparent again until two CPU clocks after $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, or $\overline{IOW}$. This delay provides proper 8 MHz bus emulation of the LA23 - LA17 signals when the processor is running at 16 MHz or 20 MHz.

The MLA bit is provided for diagnostic purposes. Bit 2 of register FFF52 is reserved and must be '0'.

The FAD bit can be used to enhance EMS performance for lower speed systems. EMS misses are normally three wait states, which are necessary for 16/20 MHz operation. At 12 MHz and below, EMS misses only need to be two wait states. This bit can be used for the non-page or page mode 2 operation at 12 MHz or below. This bit should remain 0 for page mode 3 or 16/20 MHz operation.

A single contiguous block of memory may be write protected, so that when BIOS ROM is copied into RAM, the RAM copy will not be inadvertently altered. Write protection is accomplished by not asserting CAS when MEMW is active.

RAM Write Protect - Upper Address Boundary

FFF53	X	X	X	X	'1'	A18	A17	A16
	7	6	5	4	3	2	1	0

The Upper Address Boundary Register is cleared by master reset

RAM Write Protect - Lower Address Boundary

FFF55	X	X	X	X	'1'	A18	A17	A16
	7	6	5	4	3	2	1	0

The Lower Address Boundary Register is preset to all 1's by master reset

Master reset clears the upper address boundary registers and presets the lower address boundary registers, which disables write protection. Write protection is enabled on the address range where the RAM address is less than or equal to the upper address boundary as well as greater than or equal to the lower address boundary. Write protection is programmable on 64K boundaries, and the write protection boundaries must be equal to or above 80000H and equal to or below FFFFFH. Write protection will not affect EMS writing even if the EMS window address range is covered by write protection boundaries. This allows protection of BIOS code copied into RAM without affecting operation of EMS.

The memory banks may be programmed to various sizes on 128K boundaries, except the upper split of bank 0, which is programmable on 64K boundaries.

A pair of window registers determines the address range for each memory bank. This allows the banks to be positioned at varying points and in different order than the bank number. If one bank of memory is defective, it can be disabled and the other banks can be programmed to replace it.

Video BIOS is shadowed instead by mapping the EGA/VGA BIOS to F0000 or F8000 and then shadowing the F0000 - FFFFF BIOS area. This method also allows a ROM resident setup program to reside at F0000 in ROM, which can be replaced with EGA/VGA BIOS by shadowing. This method allows a 512K bank to be allocated as 128K of conventional memory, 64K of shadowed VGA and system BIOS, and 320K of extended or EMS memory.

BANK 0 - LOWER SPLIT

Upper Address Boundary

FFF57	**X**	**X**	**X**	**X**	**A19**	**A18**	**A17**	**0/1***
	7	6	5	4	3	2	1	0

Upper boundary must be 0FXXXX or below

BANK 0 - LOWER SPLIT

Lower Address Boundary

FFF59	**X**	**X**	**X**	**X**	**A19**	**A18**	**A17**	**0/1***
	7	6	5	4	3	2	1	0

Lower boundary must be 0FXXXX or below

Upper Address Boundary = 09XXXX (Hex) by master reset

Lower Address Boundary = 09XXXX (Hex) by master reset

BANK 0 - UPPER SPLIT

Upper Address Boundary - MSD

FFF5A	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Lower Address Boundary - MSD

FFF5C	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Upper Address Boundary = 00XXXX (Hex) by master reset
Lower Address Boundary = FFXXXX (Hex) by master reset
(upper split disabled)

BANK 0 - UPPER SPLIT

Upper Address Boundary - LSD

FFF5B	X	X	X	X	A19	A18	A17	A16**
	7	6	5	4	3	2	1	0

Lower Address Boundary - LSD

FFF5D	X	X	X	X	A19	A18	A17	A16**
	7	6	5	4	3	2	1	0

* Don't care

** A16 is ignored in early production version (0000, 1011)

BANK 1

Upper Address Boundary - MSD

FFF62	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Lower Address Boundary - MSD

FFF64	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Upper Address Boundary = 07XXXX (Hex) by master reset
Lower Address Boundary = 00XXXX (Hex) by master reset

BANK 1

Upper Address Boundary - LSD

FFF63	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

Lower Address Boundary - LSD

FFF65	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

* Don't care

BANK 2

Upper Address Boundary - MSD

FFF66	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Registers FFF66 and FFF67 are cleared by master reset

BANK 2

Upper Address Boundary - LSD

FFF67	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

Lower Address Boundary - MSD

FFF68	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Registers FFF68 and FFF69 are preset to all '1s' by master reset

(Bank 2 disabled by master reset)

Lower Address Boundary - LSD

FFF69	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

* Don't care

BANK 3

Upper Address Boundary - MSD

FFF6A	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Registers FFF6A and FFF6B are cleared by master reset

BANK 3

Upper Address Boundar - LSD

FFF6B	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

Lower Address Boundary - MSD

FFF6C	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

Registers FFF6C and FFF6D are preset to all '1s' by master reset

(Bank 3 is disabled by master reset)

Lower Address Boundary - LSD

FFF6D	X	X	X	X	A19	A18	A17	0/1*
	7	6	5	4	3	2	1	0

* Don't care

The RAM banks may be either independent or two-way or four-way page interleaved. DRAM banks which are interleaved must be the same DRAM size.

DRAM SIZE	PAGE SIZE
64K	512 bytes
256K	1024 bytes
1M	2048 bytes

FFF6F	X	X	X	X	0/1*		CFG	
	7	6	5	4	3	2	1	0

* Don't care

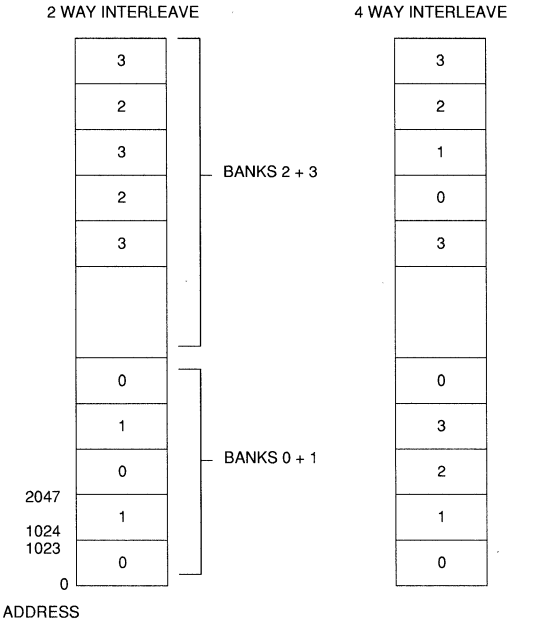
Register FFF6F is not used in non-page mode.

When the memory system operates in page mode, the banks of memory may operate independently or may be interleaved. Interleaving may decrease the average number of wait states, thus increasing performance, but interleaving may only be done if the memory banks to be interleaved are the same size.

CFG	FUNCTION
000*	All banks are independent
011	Bank 2 paired with Bank 3, Banks 0 and 1 are independent
101	Bank 0 paired with Bank 1, Banks 2 and 3 are independent
111	Bank 0 paired with Bank 1, Bank 2 paired with Bank 3
110	All four Banks are interleaved

* Default after master reset

When the memory system operates in page mode, accesses to DRAM in the same page are made with zero wait states. An access to a different page, or the first access to a page after a refresh, DMA, or master cycle will be made either with two wait states for memory mode 2, or three wait states for memory mode 3. The actual page size is variable, depending on the DRAM size.



Multiple banks of memory operating in page mode may operate independently or may be interleaved. Interleaving may decrease the average number of wait states, thus increasing performance, but interleaving may only be done if the memory banks to be interleaved are the same size. Only banks 0 and 1 or banks 2 and 3 may be interleaved together when implementing 2-way interleave. When banks 0 and 1 are interleaved, bank 1 boundary registers should be programmed so that the bank is disabled and the bank 0 boundaries should be programmed as if bank 0 were twice the normal size. As an example, for a system with 2 banks of 256K DRAM operating independently, the banks could be programmed as shown in Figure 4.

When the banks are interleaved, the banks would be programmed as shown Figure 5.

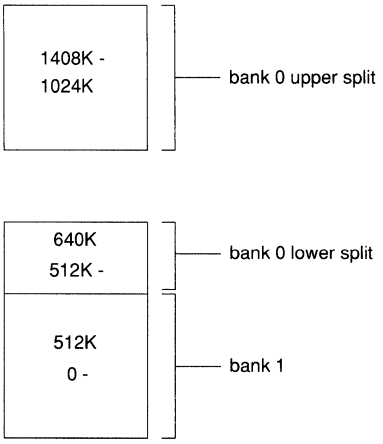


FIGURE 4. BANKS OPERATING INDEPENDENTLY

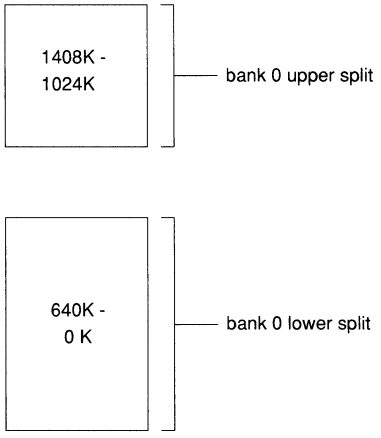


FIGURE 5. BANKS INTERLEAVED

The following tables illustrate memory system characteristics with various configurations of memory and processor speed, both for page mode and non-page mode DRAM access.

For a page mode hit, the read and write accesses may have different performance. For a page mode miss or the first access to a page, the read and write accesses have the same performance. In a page mode miss, $\overline{RAS}$ starts out low and must be brought high for a RAS precharge time before the memory can be accessed.

NON-PAGE MODE	CPU FREQUENCY	WAIT STATES READ	WRITE	EMS MISS	DRAM SPEED
MODE 4	8 MHz	0	0	2	120 ns
MODE 0	16 MHz	1	1	3	80 ns
MODE 4	12.5 MHz	1	1	2	120 ns

PAGE MODE	CPU FREQUENCY	WAIT STATES READ	WRITE	NON-EMS MISS	EMS MISS	DRAM SPEED
MODE 2	16 MHz	0	1	2	3	80 ns
MODE 3	20 MHz	0	1	3	3	80 ns
MODE 3	16 MHz	0	1	3	3	100 ns
MODE 3	12.5 MHz	0	1	3	3	120 ns

The DRAM timing is set by an external delay line for DMA or master mode transfers. The RAS leading edge becomes active from the active level of the $\overline{MEMR}$ or $\overline{MEMW}$ signals.

The DRAM timing modes are programmed by writing into register FFF72. The DRAM timing mode is actually switched during a processor hold state caused by a refresh, DMA, or bus master cycle. The Present DRAM Timing Mode register contains the current timing mode. Registers FFF72 and FFF73 will thus disagree until after a processor hold state occurs; typically, a refresh cycle will occur in 10 to 15 microseconds.

RAM SIZE CONFIGURATION REGISTER - BANK 1 AND 0

FFF70

BNK 1 SZ		BNK 0 SZ	
3	2	1	0

SZ = 00 *: 256K
01 : 1M
10 : RESERVED
11 : 64K

DRAM TIMING MODE

FFF72

X	X	X	X	D	DTYP		
7	6	5	4	3	2	1	0

DRAM TIMING MODE WILL GO INTO EFFECT AFTER REFRESH, DMA, OR OTHER HOLD CYCLE

RAM SIZE CONFIGURATION REGISTER - BANK 3 AND 2

FFF71

BNK 3 SZ		BNK 2 SZ	
3	2	1	0

SZ = 00 *: 256K
01 : 1M
10 : RESERVED
11 : 64K

PRESENT DRAM TIMING MODE

FFF73

X	X	X	X	D	DTYP			READ-ONLY
7	6	5	4	3	2	1	0	

DTYP	DRAM MODE	
000*	Non-page	(MODE 0)
001	Zero wait state read, one wait state write	(MODE 1)
010	Page mode DRAM at 12.5 MHz CPU rate	(MODE 2)
011	Standard page mode for 8-20 MHz CPU rate	(MODE 3)
100	Identical to mode 0, but RAS delayed one-half CPU clock	(MODE 4)
101	Non-page for 8-12 MHz CPU rate,with 0 wait states, RAS pulse width is 2 CPU clocks	(MODE 5)

* Default after master reset
D = 0: Normal operation (default)
D = 1: Reserved for diagnostics; disables DRAM page mode hit/miss logic

8.0 EMS MEMORY

RAM memory above 1024K may be used both for expanded or extended memory. EMS memory may be as small as 128 Kbytes or as large as 7168 Kbytes. The EMS memory is accessed by two sets of EMS Page Registers, which reside in user I/O space. Each set of EMS Page Registers points to 36 blocks of memory, each block 16 Kbytes in size, which make up the EMS Page Frame. Four of the blocks are located above 640K, with the other 32 blocks located between 128K and 640K.

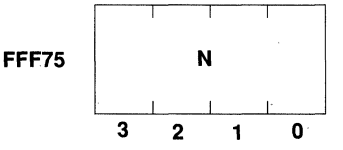
Each EMS Page Register is associated with one page of the EMS Page Frame, and consists of an enable bit and a 10-bit page number. When enabled, a 24-bit real address is formed by taking the 10-bit page number and appending the 14 bit address referencing the byte or word in the EMS page. The 24-bit address is then used to access the DRAM memory controlled by the FE3021A.

In either page mode or non-page mode, if the DRAM row address does not change, then no additional wait states are required for EMS translation. This will allow EMS access without additional wait states if accesses are made to the same 512, 1024, or 2048 byte page, depending on DRAM size.

The EMS hardware must first be configured by programming the EMS control registers located in the FFF00-FFFFF register space, which is unlocked by writing to memory location FFF00 eight times. The I/O port locations of the EMS Page Registers are in user I/O space and their locations are selected with EMS Configuration Registers FFF75 and FFF78.

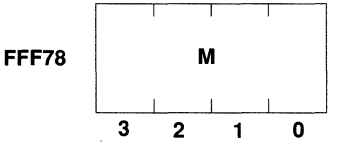
EMS Configuration Register FFF79 is used to completely enable or disable EMS, as well as to switch between the two sets of EMS Page registers. When the 'E' bit is '0', EMS operation is disabled and the EMS registers in user I/O space are inaccessible. When this is '0', it is as if the EMS hardware had been "unplugged" from the bus. When the 'E' bit is a '1', the EMS registers in the user I/O space become accessible. Registers FFF75 and FFF78 (which determine the I/O port addresses for the EMS logic), should be programmed prior to setting the 'E' bit to '1'.

EMS CONFIGURATION REGISTER N



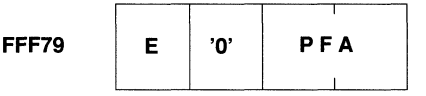
This register is set to '0110' by master reset

EMS CONFIGURATION REGISTER M



This register is set to '1000' by master reset

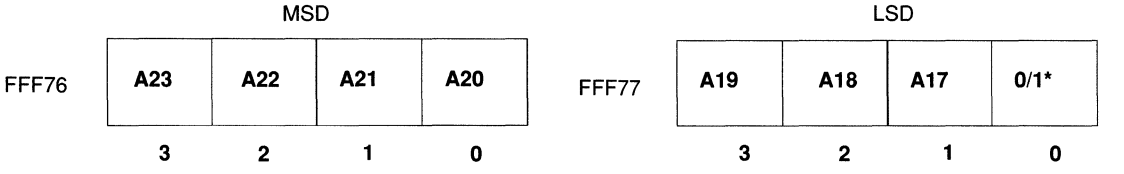
EMS CONFIGURATION REGISTER



E=1: MASTER ENABLE FOR EMS
BIT 2 RESERVED, '0'

PFA = 00 : EMS PAGE FRAME C4000-D3FFF
PFA = 01 : EMS PAGE FRAME C8000-D7FFF
PFA = 10 : EMS PAGE FRAME CC000-DBFFF
PFA = 11 : EMS PAGE FRAME D0000-DFFFF

This register is cleared by master reset



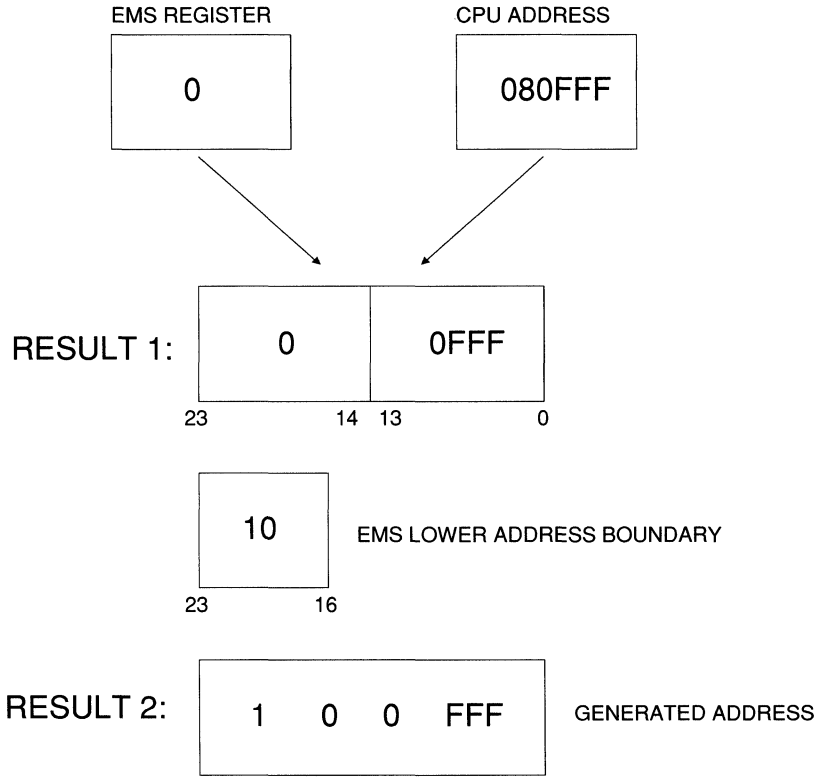
LOWER EMS BOUNDARY

These registers are set to '1111' by master reset

* Don't care

Registers FFF76 and FFF77 are used to allocate memory for EMS, on 128 Kbyte boundaries. Memory with addresses below the EMS boundary is accessed normally, as conventional or extended memory.

On-board memory with addresses above the EMS boundary is reserved for use only as EMS memory. DRAM memory accesses to addresses above the EMS boundary are made to the expansion bus. This allows EMS, off-board, and on-board extended memory to be used simultaneously.



Any CPU address above 1 MB (the EMS lower address boundary), is assumed to reference memory on the expansion bus, rather than on-board memory, which prevents extended memory references from affecting on-board EMS memory.

EMS DMA Control Register FFF7A is used to control the selected EMS map register set during DMA or master transfers. This allows DMA transfers to be made to a particular EMS task, whether or not it is the currently selected task.

On-board memory may be allocated either to extended or to EMS memory in 128 Kbyte blocks. EMS memory is allocated from the top of on-board memory down to the desired limit.

As an example, if the system contained 2 MB of DRAM, the memory map (without EMS) might look similar to Figure 6 (a) on the following page. The system would contain 640K of conventional memory and 1,280K of extended memory. The 1,280K of extended memory is composed of two parts: the original 1,024K and 256K of memory relocated from 0A0000 - 0E0000. The 128K area from 0E0000 - 0F0000 could also be relocated but in this example, it is not.

Figure 6 (b) illustrates the memory map after EMS has been installed. The EMS boundary registers have been programmed so that on-board memory above 1,152K is reserved for EMS. 128K of on-board extended memory remains between 100000 - 120000. Additional extended memory could be added on the expansion bus, starting at 120000. Two EMS areas are shown, one 64K area at 0D0000 - 0E0000, and the other at 020000 - 0A0000.

Figure 6 (c) shows the possible EMS page numbers ranging from 0 - 4F for the 1,280K of memory available for EMS paging.

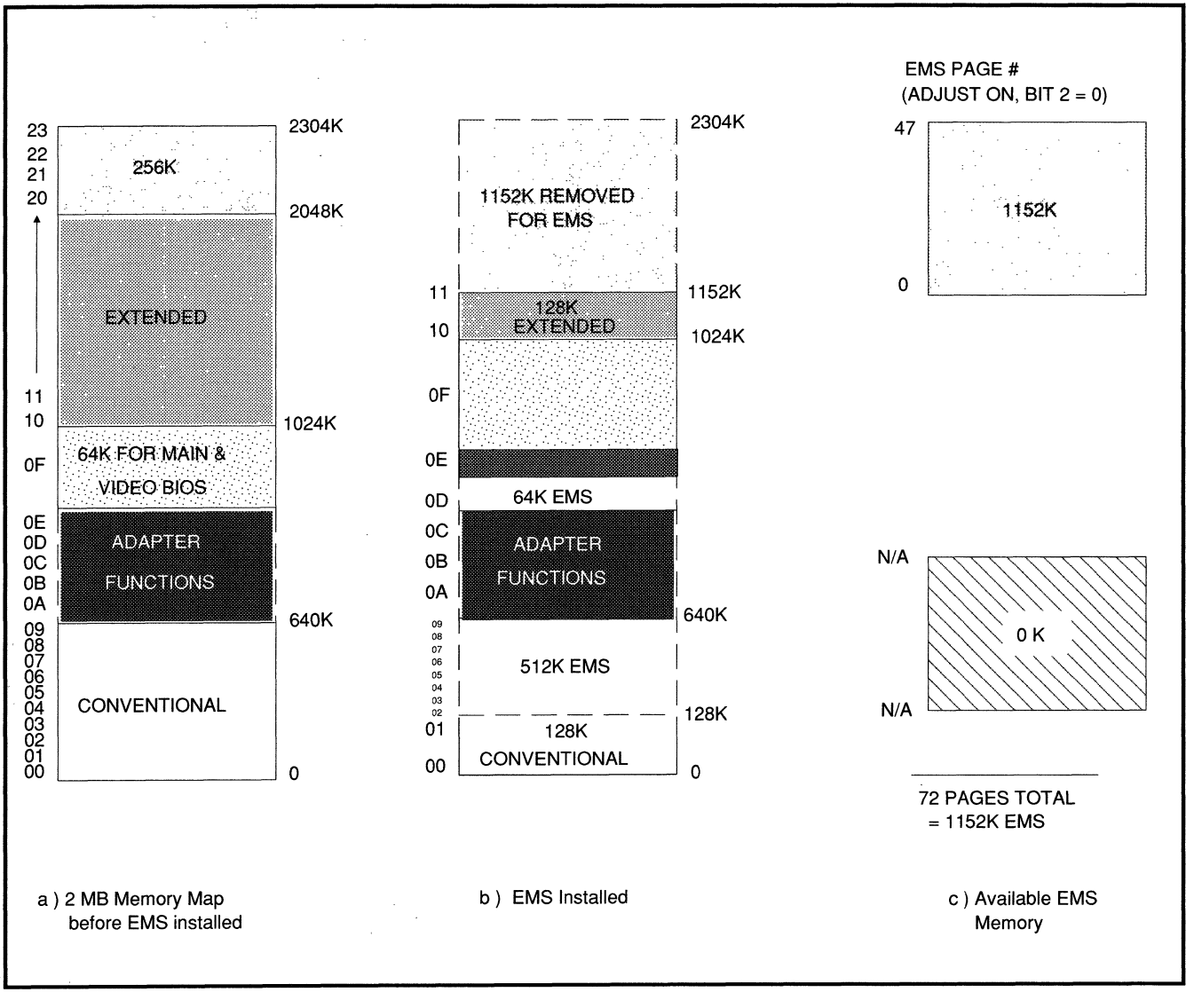


FIGURE 6. EMS/MEMORY MAP CONFIGURATIONS

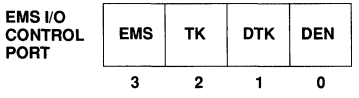
The EMS Control Register and EMS Page Registers are addressed in the user I/O port address space, I/O ports 100 (hex) through 3FF (hex). The EMS Control Registers and EMS Page Registers are selected when the I/O port address bits 9 - 6 match the value 'M' programmed by register FFF78 and the I/O port address bits 5 - 2 match the value 'N' programmed by register FFF75.

The EMS I/O Control Port is used to enable or disable EMS translation. When EMS translation is disabled, the EMS I/O control port and EMS page registers may still be accessed, but EMS page swapping will not occur.

The EMS I/O Control Port is also used to select the active page register set. When the processor accesses EMS memory, it always uses the register set specified by the TK bit. Normally, when DMA accesses EMS memory, it also uses the register set specified by the TK bit. Alternatively, the DMA transfer may be made using a particular register set, independently of the register set currently being used by the processor. This allows a DMA operation to start, continue, and finish while the processor is time-slicing and swapping back and forth between two programs.

The P and W fields for each page register are specified in the following table. Each EMS Page register is composed of a one bit enable bit (E) and a 10-bit page number (Q9-Q0). EMS translation for the EMS page is enabled when the E bit is a '1'.

EMS CONTROL REGISTER

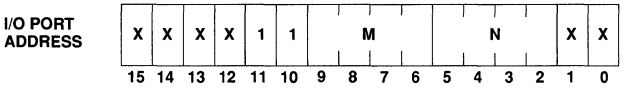


EMS = 1: EMS TRANSLATION ENABLED

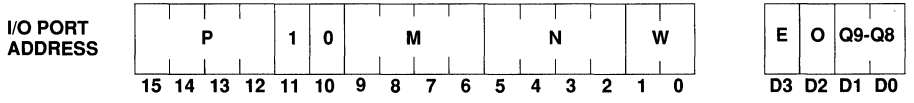
DEN = 0 : DMA TRANSFERS MADE TO MAP REGISTER SET SPECIFIED BY "TK" BIT

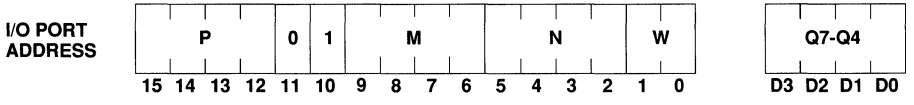
DEN = 1 : DMA TRANSFERS MADE TO MAP REGISTER SET SPECIFIED BY "DTK" BIT

EMS CONTROL REGISTER ADDRESS LOCATION

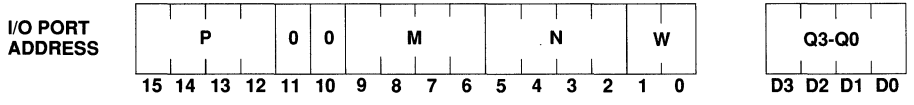


EMS PAGE REGISTER - MSD





EMS PAGE REGISTER - LSD



P	W	EMS PAGE			
		PFA=00	PFA=01	PFA=10	PFA=11
0000	11	D0000-D3FFF	D4000-D7FFF	D8000-DBFFF	DC000-DFFFF
0000	10	CC000-CFFFF	D0000-D3FFF	D4000-D7FFF	D8000-DBFFF
0000	01	C8000-CBFFF	CC000-CFFFF	D0000-D3FFF	D4000-D7FFF
0000	00	C4000-C7FFF	C8000-CBFFF	CC000-CFFFF	D0000-D3FFF
1001	11	9C000-9FFFF	624K TO 640K		
1001	10	98000-9BFFF	608K TO 624K		
1001	01	94000-97FFF	592K TO 608K		
1001	00	90000-93FFF	576K TO 592K		
1000	11	8C000-8FFFF	560K TO 576K		
1000	10	88000-8BFFF	544K TO 560K		
1000	01	84000-87FFF	528K TO 544K		
1000	00	80000-83FFF	512K TO 528K		
0111	11	7C000-7FFFF	496K TO 512K		
0111	10	78000-7BFFF	480K TO 496K		
0111	01	74000-77FFF	464K TO 480K		
0111	00	70000-73FFF	448K TO 464K		
0110	11	6C000-6FFFF	432K TO 448K		
0110	10	68000-6BFFF	416K TO 432K		
0110	01	64000-67FFF	400K TO 416K		
0110	00	60000-63FFF	384K TO 400K		
0101	11	5C000-5FFFF	368K TO 384K		
0101	10	58000-5BFFF	352K TO 368K		
0101	01	54000-57FFF	336K TO 352K		
0101	00	50000-53FFF	320K TO 336K		
0100	11	4C000-4FFFF	304K TO 320K		
0100	10	48000-4BFFF	288K TO 304K		
0100	01	44000-47FFF	272K TO 288K		
0100	00	40000-43FFF	256K TO 272K		
0011	11	3C000-3FFFF	240K TO 256K		
0011	10	38000-3BFFF	224K TO 240K		
0011	01	34000-37FFF	208K TO 224K		
0011	00	30000-33FFF	192K TO 208K		
0010	11	2C000-2FFFF	176K TO 192K		
0010	10	28000-2BFFF	160K TO 176K		
0010	01	24000-27FFF	144K TO 160K		
0010	00	20000-23FFF	128K TO 144K		

TABLE 9. EMS PAGE REGISTER INFORMATION

9.0 TEST MODE

All output pins will become tri-stated if $\overline{\text{YMEMR}}$ and $\overline{\text{YMEMW}}$ are active simultaneously while $\overline{\text{MR}}$ is active. The outputs will remain tri-stated if $\overline{\text{MR}}$ is brought inactive while $\overline{\text{YMEMR}}$ and $\overline{\text{YMEMW}}$ are both active. The outputs will become active drivers again when $\overline{\text{MR}}$ is brought low without both $\overline{\text{YMEMR}}$ and $\overline{\text{YMEMW}}$ active. This "all output tri-state" mode allows an in-circuit board tester to drive the FE3021A output pins.

10.0 FE3021A PINOUT

The FE3021A is packaged in a 132-pin plastic quad flat pack. Table 10 lists the pins according to their function.

AT BUS	
LA23	63
LA22	70
LA21	71
LA20	93
LA19	95
LA18	102
LA17	103
ADDR19	59
ADDR18	61
ADDR17	62
ADDR16	64
ADDR15	65
ADDR14	66
ADDR13	68
ADDR12	69
ADDR11	72
ADDR10	73
ADDR9	75
ADDR8	94
ADDR7	96
ADDR6	97
ADDR5	98
ADDR4	100
ADDR3	101
ADDR2	104
ADDR1	106
ADDR0	105
$\overline{\text{MASTER}}$	52

DATA BUS	
EDATA3	17
EDATA2	16
EDATA1	15
EDATA0	14

CHIP SELECTS & CONTROL	
$\overline{\text{CS0}}$	48
$\overline{\text{CS1}}$	47
$\overline{\text{CS2}}$	46
$\overline{\text{CS3}}$	45
CSF	49
$\overline{\text{CS8042}}$	60
$\overline{\text{CS287}}$	56
$\overline{\text{CSNMI}}$	20
$\overline{\text{CSPTB}}$	22
ADSTB	53
$\overline{\text{SELDAT}}$	40
$\overline{\text{YMEMR}}$	10
$\overline{\text{YMEMW}}$	11
$\overline{\text{YIOR}}$	12
$\overline{\text{YIOW}}$	13
$\overline{\text{IOR}}$	8
$\overline{\text{IOW}}$	9

MEMORY ADDRESS MUX	
RA9	41
RA8	39
RA7	38
RA6	37
RA5	36
RA4	35
RA3	34
RA2	33
RA1	32
RA0	31
$\overline{\text{RAS}}$	58
$\overline{\text{TAP1}}$	44
$\overline{\text{TAP2}}$	26

80286 INTERFACE	
A23	74
A22	78
A21	79
A20	80
A19	81
A18	82
A17	83
A16	84
A15	85
A14	86
A13	87
A12	88
A11	89
A10	90
A9	109
A8	110
A7	111
A6	112
A5	113
A4	114
A3	115
A2	116
A1	117
A0	118
$\overline{\text{S0}}$	119
$\overline{\text{S1}}$	120
M/$\overline{\text{IO}}$	121
CPUCLK	122
HLDA	123
IORDY	127

RESET	
$\overline{\text{RESET}}$	28
$\overline{\text{FRES}}$	19

MEMORY CONTROL	
$\overline{\text{RAS0}}$	128
$\overline{\text{RAS1}}$	129
$\overline{\text{RAS2}}$	130
$\overline{\text{RAS3}}$	132
$\overline{\text{CASL0}}$	125
$\overline{\text{CASL1}}$	126
$\overline{\text{CASL2}}$	2
$\overline{\text{CASL3}}$	3
$\overline{\text{CASH0}}$	4
$\overline{\text{CASH1}}$	5
$\overline{\text{CASH2}}$	6
$\overline{\text{CASH3}}$	131
$\overline{\text{REFR}}$	18
$\overline{\text{CSPROM}}$	43
$\overline{\text{ONBD}}$	57
$\overline{\text{BHE}}$	21
$\overline{\text{DLE}}$	23
ADR0	24
$\overline{\text{LOMEG}}$	25
A20GT	54

GROUND	POWER
1	7
27	30
29	50
42	55
51	77
67	92
76	107
91	
99	
108	
124	

TABLE 10. PIN LISTING

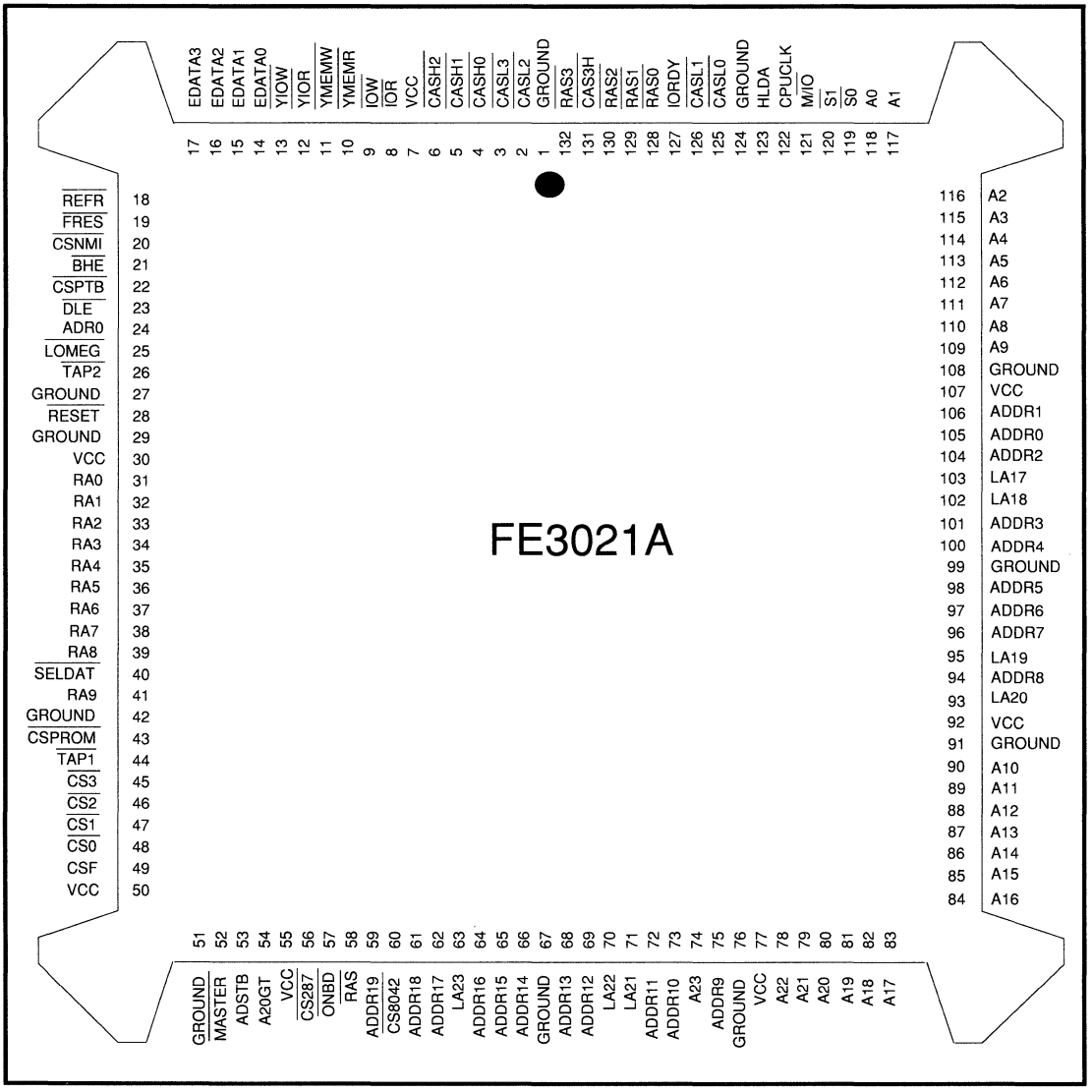


FIGURE 7. (PQFP) PLASTIC QUAD FLAT PACK PIN ASSIGNMENTS

11.0 ELECTRICAL SPECIFICATIONS

11.1 MAXIMUM RATINGS

Supply Voltage (VCC) with respect to VSS (ground) . . . . . -0.5V to +7V
Operating temperature . . . . . 0°C (32°F) to 70°C (158°F)
Storage temperature . . . . . -40°C (-40°F) to 125°C (257°F)
Power dissipation . . . . . 500 mW

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Operating Characteristics.

11.2 DC OPERATING CHARACTERISTICS

T_a = 0°C (32°F) to 70°C (158°F), Vcc = 5 V ± .25 V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
IIL	Input Leakage		±10	µA	VIN = .4 TO VCC
IOZ	Tri-state And Open Drain Output Leakage		±10	µA	VOUT = .4 TO VCC
VIH	Input High Voltage	2.0		V	
VIL	Input Low voltage		.8	V	
VIHC	CPU Clock Input High Voltage	.6		V	
VILC	CPU Clock Input Low Voltage		.6	V	
ICC	Supply Current		50	mA	All outputs open, inputs at 2.0V, CPUCLK = 16 MHz

TABLE 11. DC OPERATING CHARACTERISTICS

For outputs $\overline{YIOR}$, $\overline{YIOW}$, RA[9:0], $\overline{ONBD}$, $\overline{LOMEG}$, A[23:0], CSF, $\overline{CS[3:0]}$, $\overline{CS8042}$, $\overline{CS287}$, $\overline{CSNMI}$, $\overline{CSPTB}$, $\overline{RAS}$, $\overline{RAS[3:0]}$, $\overline{CASL[3:0]}$, $\overline{CASH[3:0]}$, $\overline{CSPROM}$, $\overline{DLE}$, $\overline{FRES}$, $\overline{SELDAT}$, and EDATA[3:0]

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT = -1 mA
VOL	Output Low Voltage		.4	V	IOUT = 1 mA

TABLE 11. DC OPERATING CHARACTERISTICS cont.

For outputs ADDR[19:0], LA[23:17], $\overline{IOR}$, $\overline{IOW}$, IORDY

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT = -3 mA
VOL	Output Low Voltage		.4	V	IOUT = 12 mA*

TABLE 11. DC OPERATING CHARACTERISTICS cont.

* 10 mA for $\overline{IOR}$, $\overline{IOW}$.

11.3 AC TIMING CHARACTERISTICS

Load Capacitance = 20 pF for output: $\overline{DLE}$

Load Capacitance = 50 pF for outputs: CSF, $\overline{CS[3:0]}$, $\overline{CS8042}$, $\overline{CS287}$, $\overline{CSNMI}$ $\overline{CSPTB}$, $\overline{SELDAT}$, $\overline{RA[9:0]}$, $\overline{ONBD}$, $\overline{LOMEG}$, $\overline{RAS}$, $\overline{CSPROM}$, $\overline{YIOR}$, $\overline{YIOW}$, $\overline{FRES}$

Load Capacitance = 100 pF for output: IORDY, A[19:0], EDATA[3:0], $\overline{CASL[3:0]}$, $\overline{CASH[3:0]}$

Load Capacitance = 200 pF for outputs: $\overline{RAS[3:0]}$, LA[23:17], ADDR[19:0], $\overline{IOR}$, $\overline{IOW}$

SYMBOL	CHARACTERISTIC	PRELIMINARY 12 MHz		PRELIMINARY 16 MHz		PRELIMINARY 20 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX
T1	CPUCLK Cycle	40		31		25	
T2	CPUCLK High Pulse	13		12			
T3	CPUCLK Low Pulse	11		10			
T4	A[23:0], M/$\overline{IO}$ Setup To $\overline{S0}$ Or $\overline{S1}$ Falling	22		16		12	
T5	A[23:0], M/$\overline{IO}$ To $\overline{ONBD}$, Memory Cycle		56		33		27
T5a	A[23:6], M/$\overline{IO}$ to $\overline{ONBD}$, I/O cycle		56		33		22
T6	$\overline{S0}$, $\overline{S1}$ Setup To CPUCLK Falling	20		11		8	
T7	$\overline{S0}$, $\overline{S1}$ Hold From CPUCLK Falling	3		2		1	
T10	M/$\overline{IO}$, A[23:0] To LA[23:17]		50		45		45
T13	$\overline{YMEMR}$ To $\overline{CSPROM}$		45		46		46

TABLE 12. SYSTEM TIMING

SYMBOL	CHARACTERISTIC	PRELIMINARY 12 MHz		PRELIMINARY 16 MHz		PRELIMINARY 20 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX
T14	ADSTB To $\overline{CS[3:0]}$, $\overline{CSPTB}$, CSF, $\overline{CSNMI}$, $\overline{CS8042}$		45		37		37
T14a	ADSTB To $\overline{CS287}$		45		37		30
T14b	CPUCLK Falling To CS287 ROM Cycle		44		44		44
T15	CPUCLK Falling To $\overline{LOMEG}$		43		43		43
T17a	$\overline{YIOR}$ To $\overline{IOR}$		40		35		35
T17	$\overline{YIOW}$ To $\overline{IOW}$		40		35		35
T18	ADSTB To ADDR[19:1]		78		59		45
T19	ADR0 To ADDR0		45		40		40
T20	Data Valid From $\overline{YMEMR}$ Or $\overline{YIOR}$ Active		180		150		140
T22	LA[23:17] From CPUCLK Falling		50		45		45
T24	Data Setup To $\overline{YMEMW}$ Or $\overline{YIOW}$ Inactive		180	150		150	
T25	Data Hold From $\overline{YMEMW}$ Or $\overline{YIOW}$ Inactive	10		10		10	
T26	$\overline{YIOR}$ Or $\overline{YMEMR}$ To $\overline{SELDAT}$		55		55		55
T27	$\overline{IOR}$ To $\overline{SELDAT}$, Master Mode Cycle		50		45		45
T28	ADSTB To Row Address; DMA Cycle, NON-EMS		50		47		47
T28a	ADSTB To Row Address; DMA Cycle, EMS		180		147		147
T29	$\overline{YMEMR}$ To $\overline{RAS}$, $\overline{RAS[3:0]}$, Refresh Cycle		36		36		36
T30	$\overline{YMEMR}$ Or $\overline{YMEMW}$ To $\overline{RAS}$; DMA Cycle		35		30		30
T31a	TAP1 Falling To ROW Address Invalid	5		5		5	
T31b	$\overline{TAP1}$ Falling To Column Address Valid		45		T33+18		T33+12
T32	$\overline{YMEMR}$ Or YMEMW To $\overline{RAS[3:0]}$, DMA Cycle		35		30		30

TABLE 12. SYSTEM TIMING cont.

SYMBOL	CHARACTERISTIC	PRELIMINARY 12 MHz		PRELIMINARY 16 MHz		PRELIMINARY 20 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX
T33	$\overline{TAP2}$ Falling To $\overline{CASL[3:0]}$, $\overline{CASH0}$, DMA Cycle		30		29		29
T34	$\overline{YMEMR}$ Or $\overline{YMEMW}$ Rising To $\overline{CASL[3:0]}$ Or $\overline{CASH[3:0]}$ Inactive		35		29		29
T35	$\overline{YMEMR}$ Active To $\overline{DLE}$ Active; DMA Or Master Mode		40		32		32
T36	$\overline{YMEMR}$ inactive To $\overline{DLE}$ Inactive: DMA Or Master Mode		40		32		32
T37	$\overline{BHE}$ Or ADR0 Setup To CPUCLK Falling	25		20		20	
T38a	ADR0 Setup To CPUCLK Falling	25		20		20	
T38b	$\overline{BHE}$ Setup To CPUCLK Falling	25		20		20	
T39	A[23:1] To RA[9:0] Row Address; Mode 0, 1, 4, 5		45		27		27
T40	$\overline{TAP1}$ Falling To RA[9:0] Column Address; Mode 0, 1, 4, 5		45		29		29
T41	RA[9:0] Row Address Valid From CPUCLK At End Of $\overline{CAS[3:0]}$		50		47		47
T43	CPUCLK Falling To $\overline{RAS}$; Mode 0, 1, 5		35		30		30
T44	CPUCLK Falling To $\overline{RAS[3:0]}$, Mode 0, 1, 5		35		30		30
T47	$\overline{TAP2}$ Falling To $\overline{CASL[3:0]}$, Or $\overline{CASH[3:0]}$, Active; Mode 0, 1, 4, 5		35		29		29
T48	CPUCLK Falling To $\overline{CASL[3:0]}$, Or $\overline{CASH[3:0]}$ Inactive; Mode 0, 1, 4, 5		35		27		27
T49	ROW Address From Middle Of TS		52		52		
T50	$\overline{TAP2}$ Falling To $\overline{DLE}$ Active; Mode 0, 1, 4, 5		35		32		32

TABLE 12. SYSTEM TIMING cont.

SYMBOL	CHARACTERISTIC	PRELIMINARY 12 MHz		PRELIMINARY 16 MHz		PRELIMINARY 20 MHz	
		MIN	MAX	MIN	MAX	MIN	MAX
T51	CPUCLK Falling To $\overline{DLE}$ Inactive; Mode 0, 1, 4, 5		35		35		35
T52a	Ready Low From $\overline{S0}$ Or $\overline{S1}$ Low		35		30		25
T52b	Ready Low From CPUCLK Rising		35		30		25
T53	Ready High From CPUCLK Falling		35		30		30
T54	Column Address From CPUCLK Falling				T57+30		N/A
T56	$\overline{RAS[3:0]}$ Active From CPUCLK Falling				30		N/A
T57	$\overline{CAS[3:0]}$ Active From CPUCLK Rising				23		N/A
T58	$\overline{CAS[3:0]}$ Inactive From CPUCLK Rising				23		N/A
T59a	$\overline{DLE}$ Active From CPUCLK Falling		35		30		30
T59b	$\overline{DLE}$ Inactive From CPUCLK Rising		T68+5		T68+5		T68+5
T60	Row Address Valid From CPUCLK Falling; Mode 3		52		52		52
T61a	$\overline{RAS[3:0]}$ Inactive From CPUCLK Falling		30		30		30
T62	$\overline{RAS[3:0]}$ Inactive From HLDA Active		40		35		35
T63	Column Address Hold From End Of $\overline{CAS[3:0]}$	1		1		1	
T64	Column Address From CPUCLK; Mode 2 & 3		50		T67+30		T67+21
T65	Column Address From A[23:1]		45		T67+19		T67+13
T66	$\overline{RAS[3:0]}$ Active From CPUCLK Rising; Mode 3		35		30		26
T67	$\overline{CASL[3:0]}$ Or $\overline{CASH[3:0]}$ Active From CPUCLK; Mode 3		28		19		19

TABLE 12. SYSTEM TIMING cont.

SYMBOL	CHARACTERISTIC	PRELIMINARY 12 MHz MIN	PRELIMINARY 12 MHz MAX	PRELIMINARY 16 MHz MIN	PRELIMINARY 16 MHz MAX	PRELIMINARY 20 MHz MIN	PRELIMINARY 20 MHz MAX
T68	$\overline{CASL}$[3:0] Or $\overline{CASH}$[3:0], Inactive From CPUCLK Rising; Mode 3		28		23		23
T6867	Difference Of $\overline{CAS}$[3:0] Inactive And Active Time (T[68:67])		4		4		N/A
T69	$\overline{REFR}$ To $\overline{ONBD}$		50		50		50
T70	Refresh Address Valid From $\overline{REFR}$		50		50		50
T72	$\overline{MASTER}$ Active To LA[23:17], ADDR[16:0] High Impedance		45		45		45
T73	$\overline{MASTER}$ Inactive To LA [23:17], ADDR [16:0] Low Impedance		45		45		45
T74	ADDR[9:0] To Chip Selects		65		65		65
T75	$\overline{MASTER}$ Active to A[23:0], ADR0 Low Impedance		45		45		45
T76	$\overline{MASTER}$ Inactive To A[23:0], ADR0 High Impedance		45		45		45
T77	LA[23:17], ADDR[16:1] To RA[9:0]		45		42		42
T77a	LA[23:17], ADDR [16:1] To RA [9:0] - EMS Cycle		198		198		198
T78	$\overline{MASTER}$ Active To $\overline{YIOR}$, $\overline{YIOW}$ Low Impedance		45		45		45
T79	$\overline{MASTER}$ Inactive To $\overline{YIOR}$, $\overline{YIOW}$ High Impedance		45		45		45
T80	$\overline{MASTER}$ Active To $\overline{IOR}$, $\overline{IOW}$ High Impedance		45		45		45
T81	$\overline{MASTER}$ Inactive To $\overline{IOR}$, $\overline{IOW}$ Low Impedance		45		45		45
T82a	$\overline{IOR}$ To $\overline{YIOR}$		30		25		25
T82b	$\overline{IOW}$ To $\overline{YIOW}$		30		25		25
T83	LA[23:17], ADDR[16:0] To A[23:0], ADR0		40		35		35

TABLE 12. SYSTEM TIMING cont.

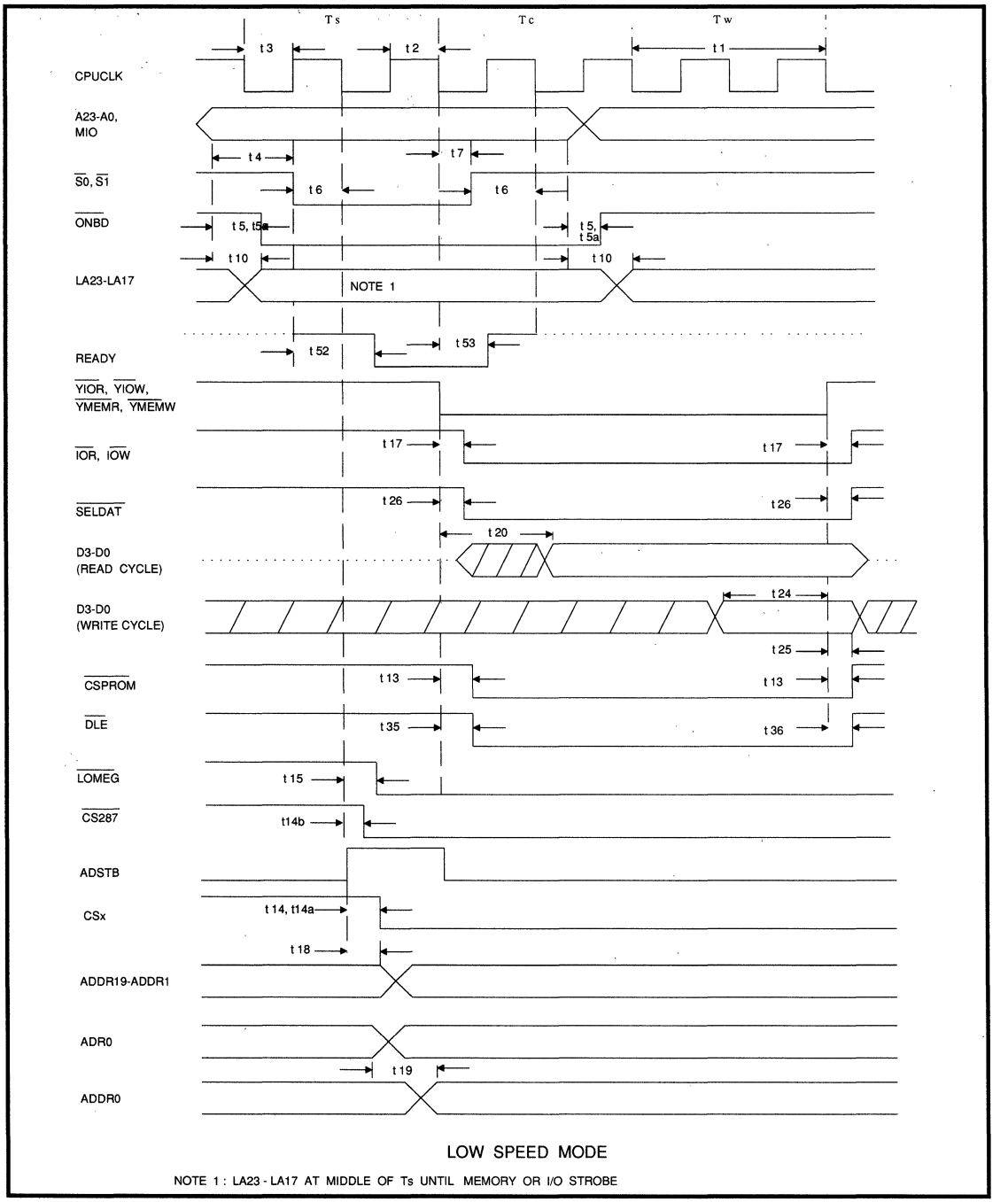


FIGURE 8. BASIC TIMING

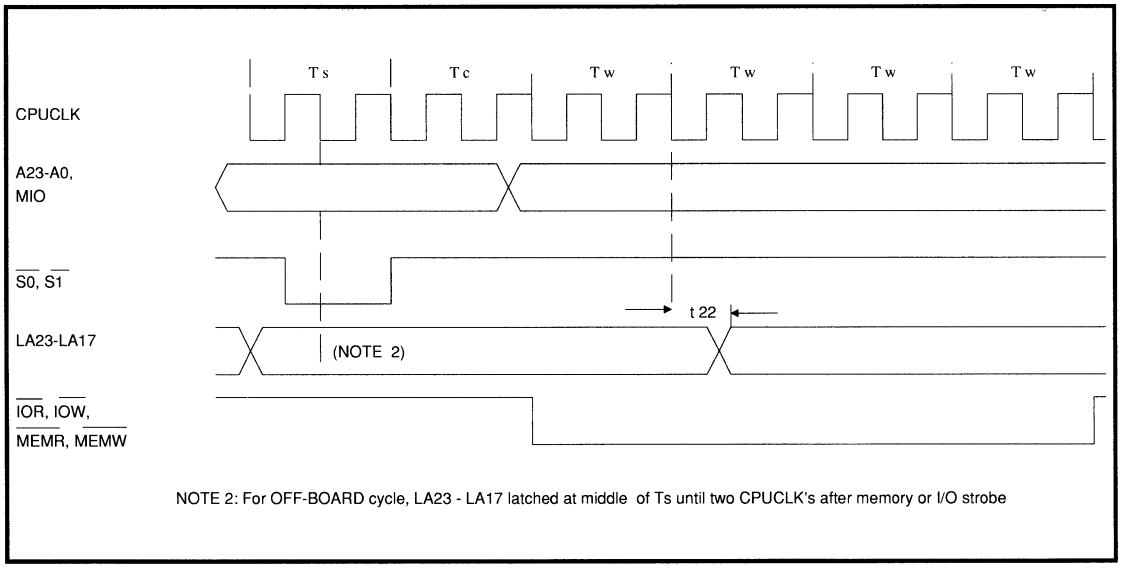


FIGURE 9. HIGH SPEED MODE LA23-LA17 TIMING

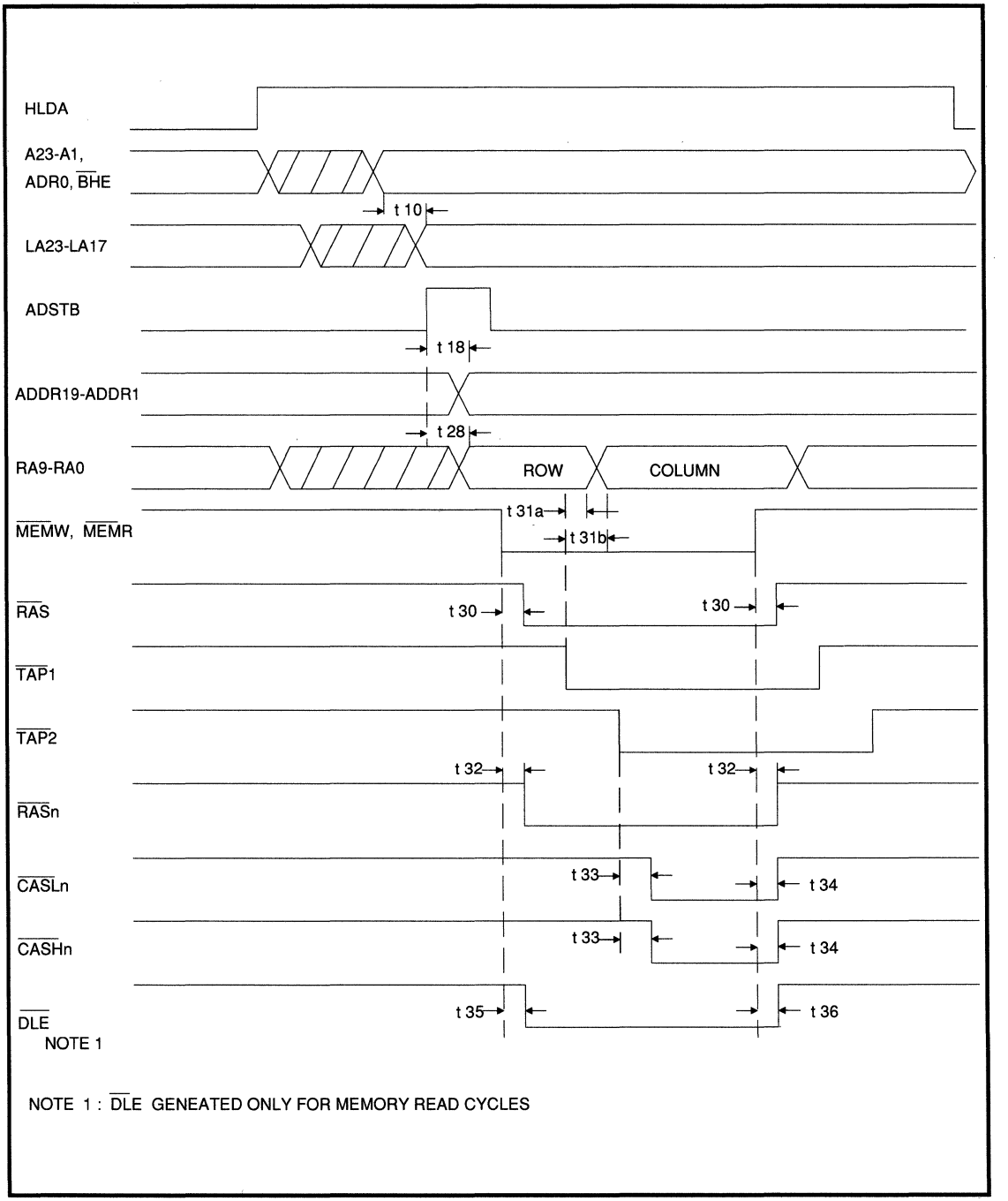


FIGURE 10. DMA MEMORY CYCLE

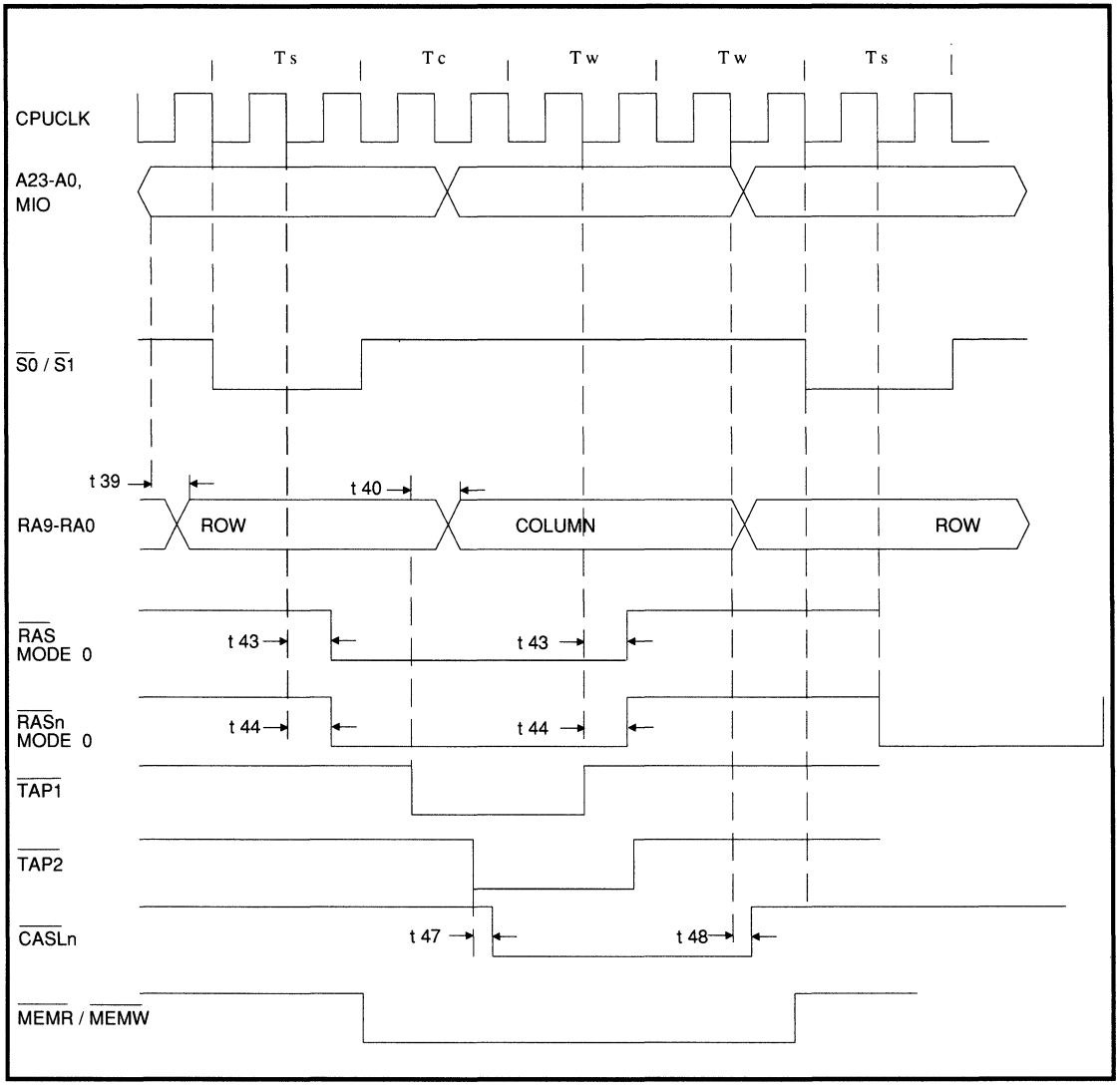


FIGURE 11. MEMORY MODE 0 (NON-PAGE MODE)

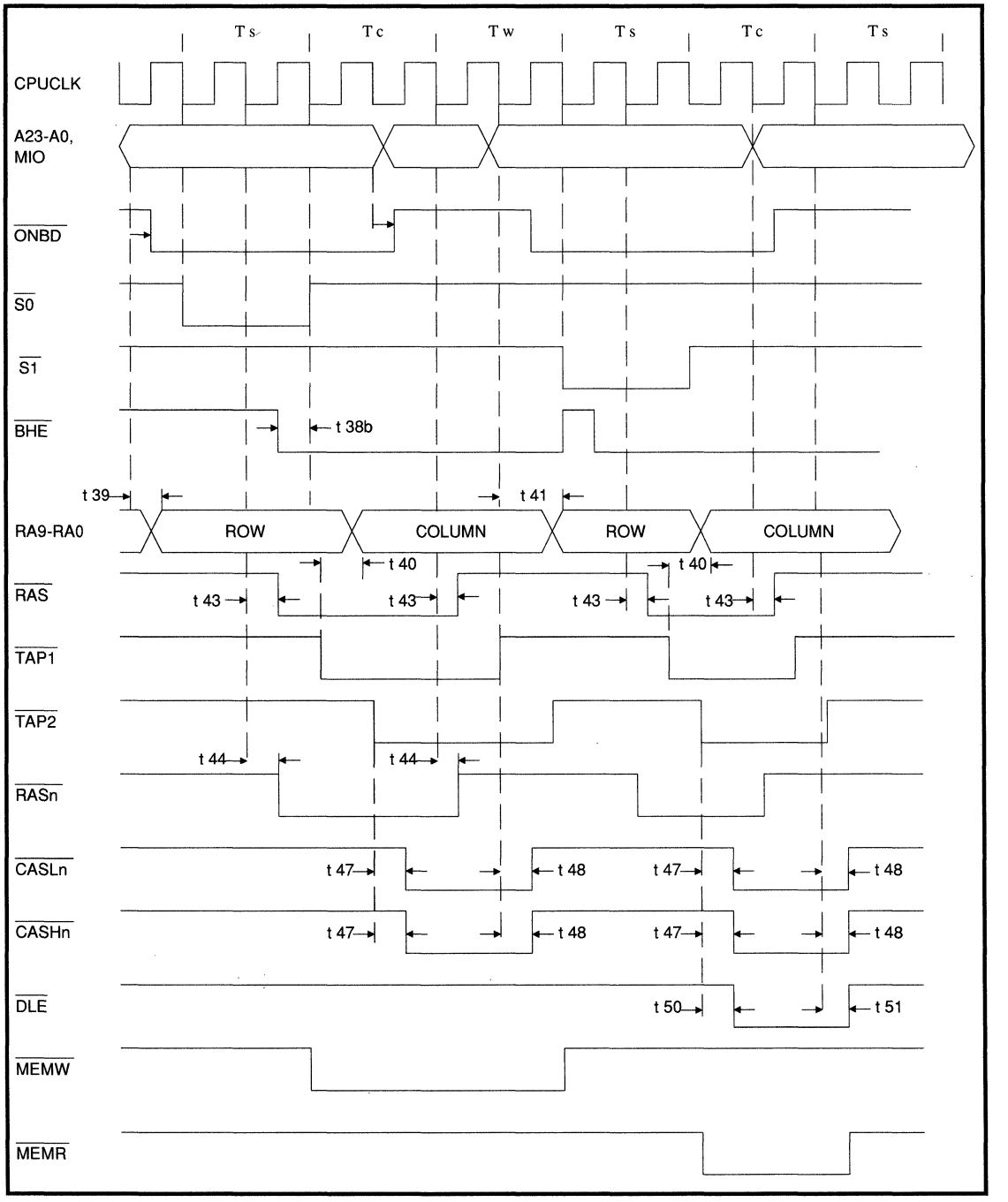


FIGURE 12. MEMORY MODE 1 (NON-PAGE 0 WS READ - 1 WS WRITE)

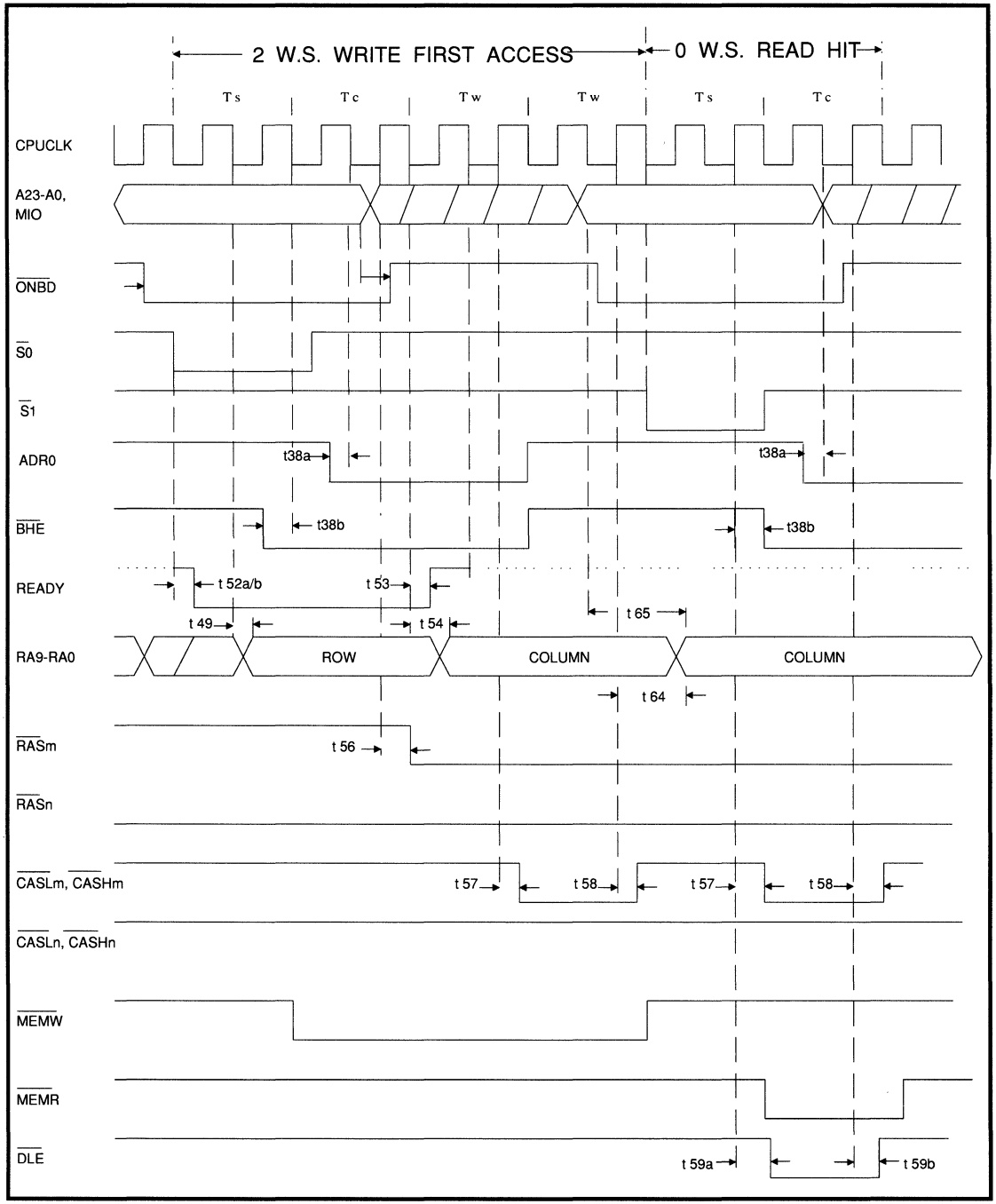


FIGURE 13. MEMORY MODE 2 (PAGE) 1 OF 2

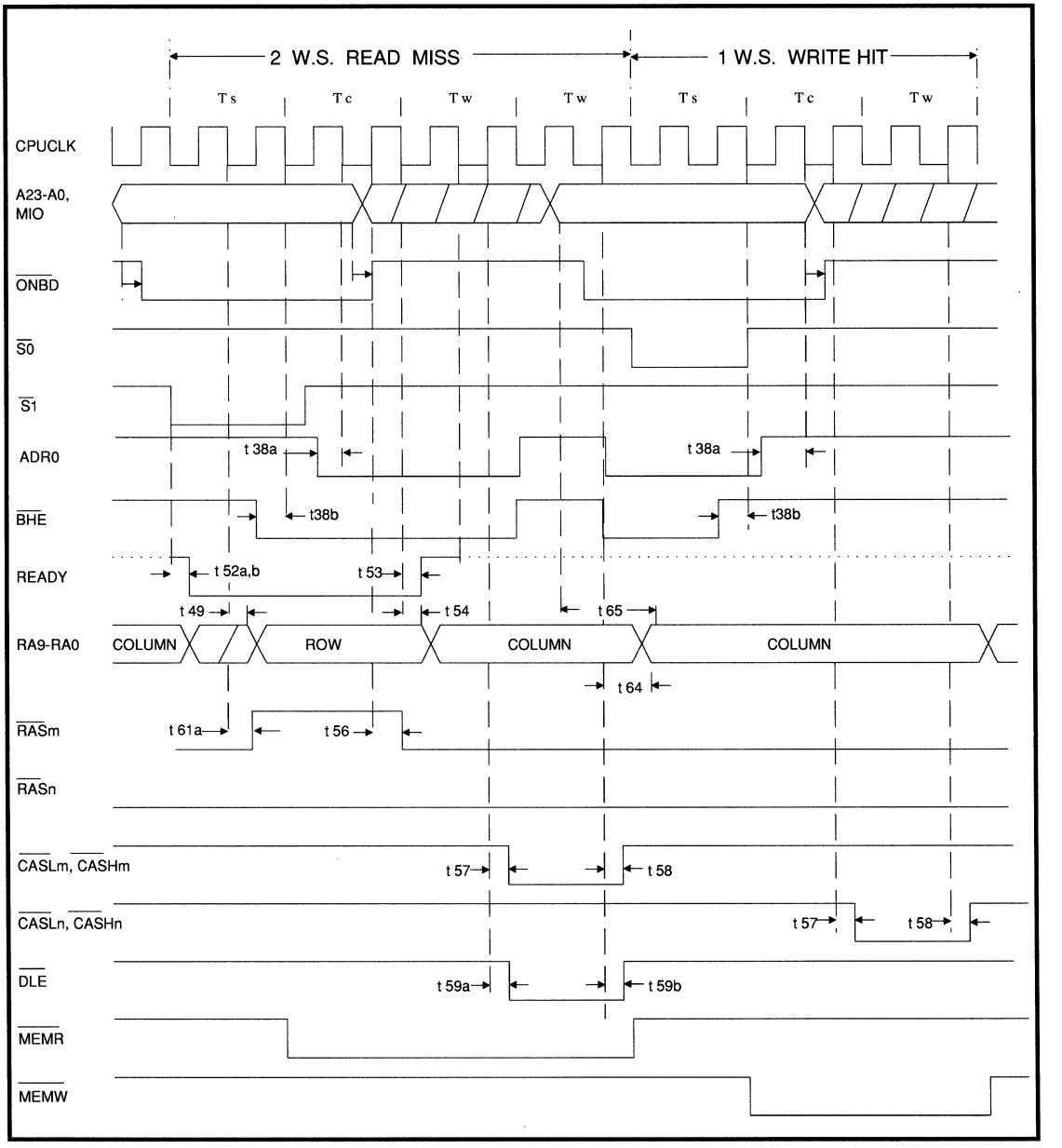


FIGURE 14. MEMORY MODE 2 (PAGE) 2 OF 2

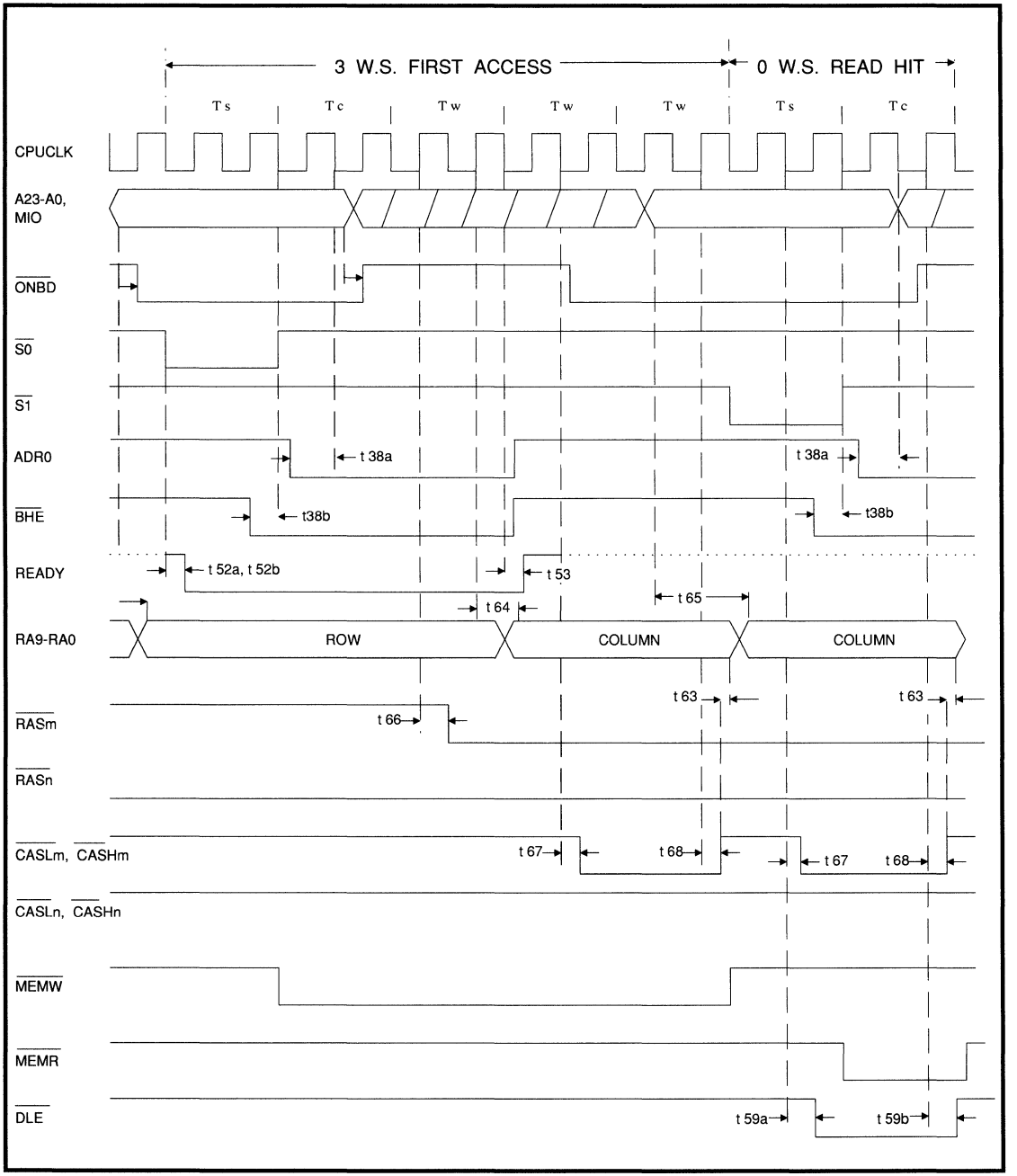


FIGURE 15. MEMORY MODE 3 (PAGE) 1 OF 2

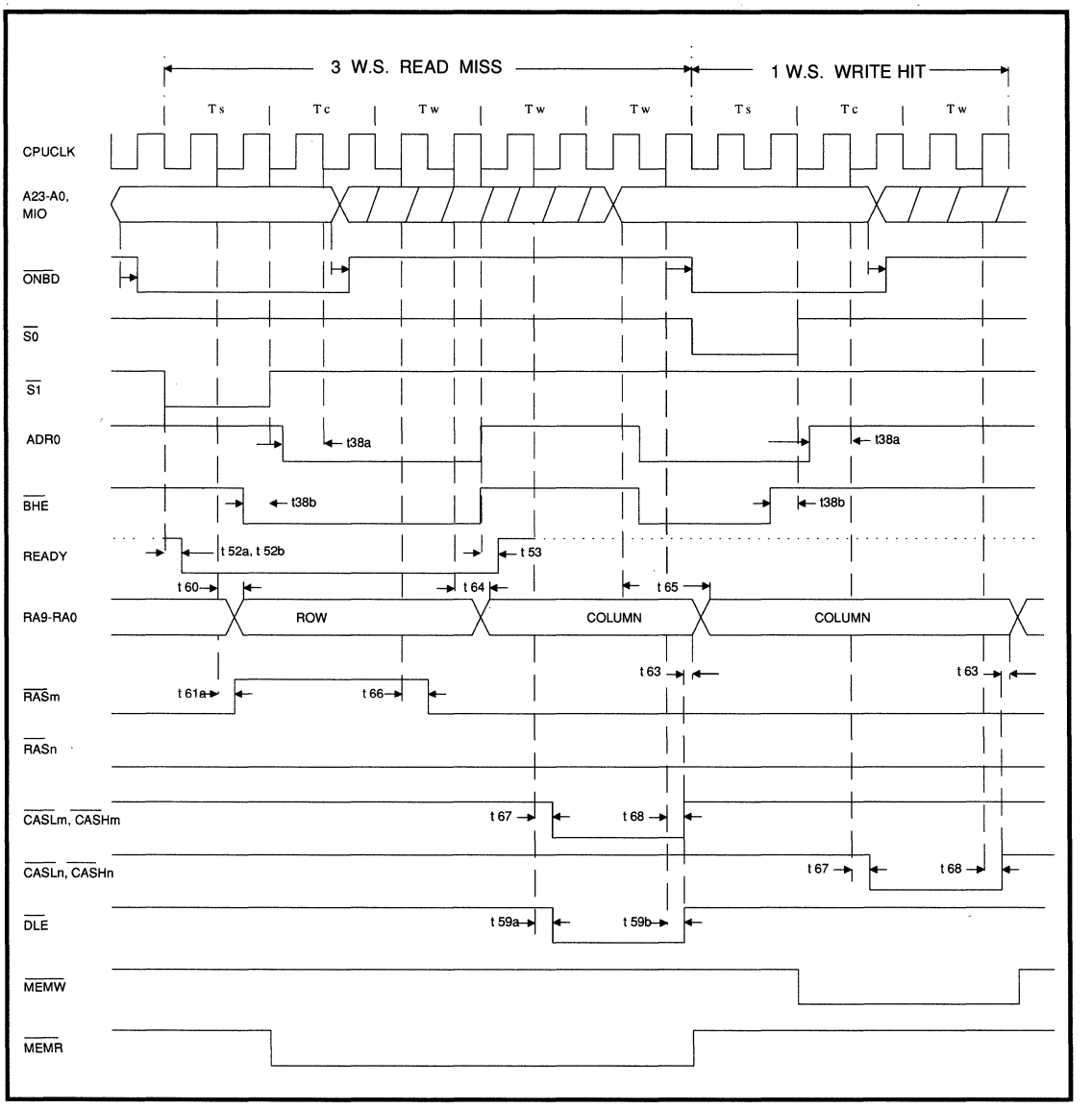


FIGURE 16. MEMORY MODE 3 (PAGE) 2 OF 2

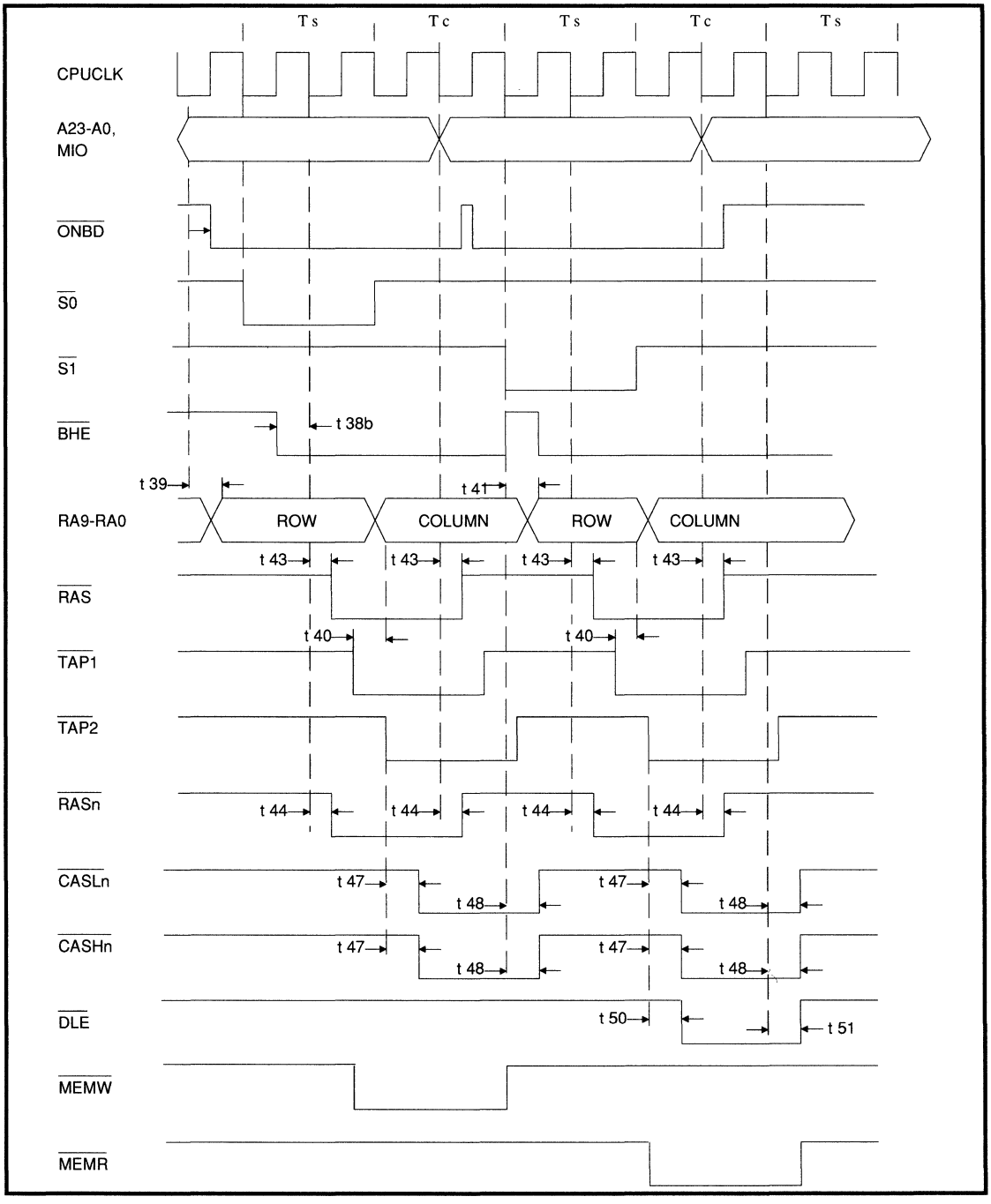


FIGURE 17. MEMORY MODE 5 (NON-PAGE) 0 WS READ AND WRITE

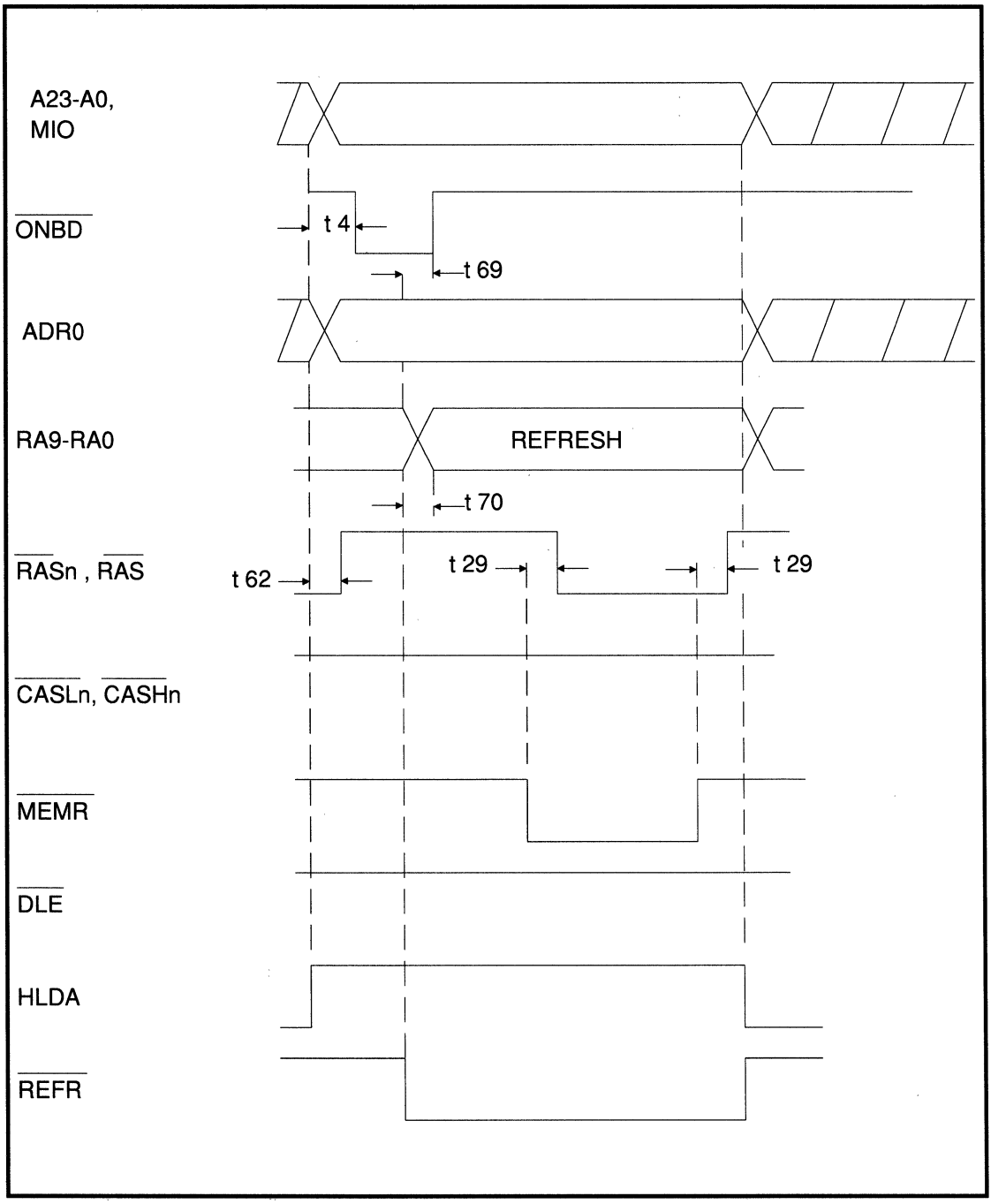
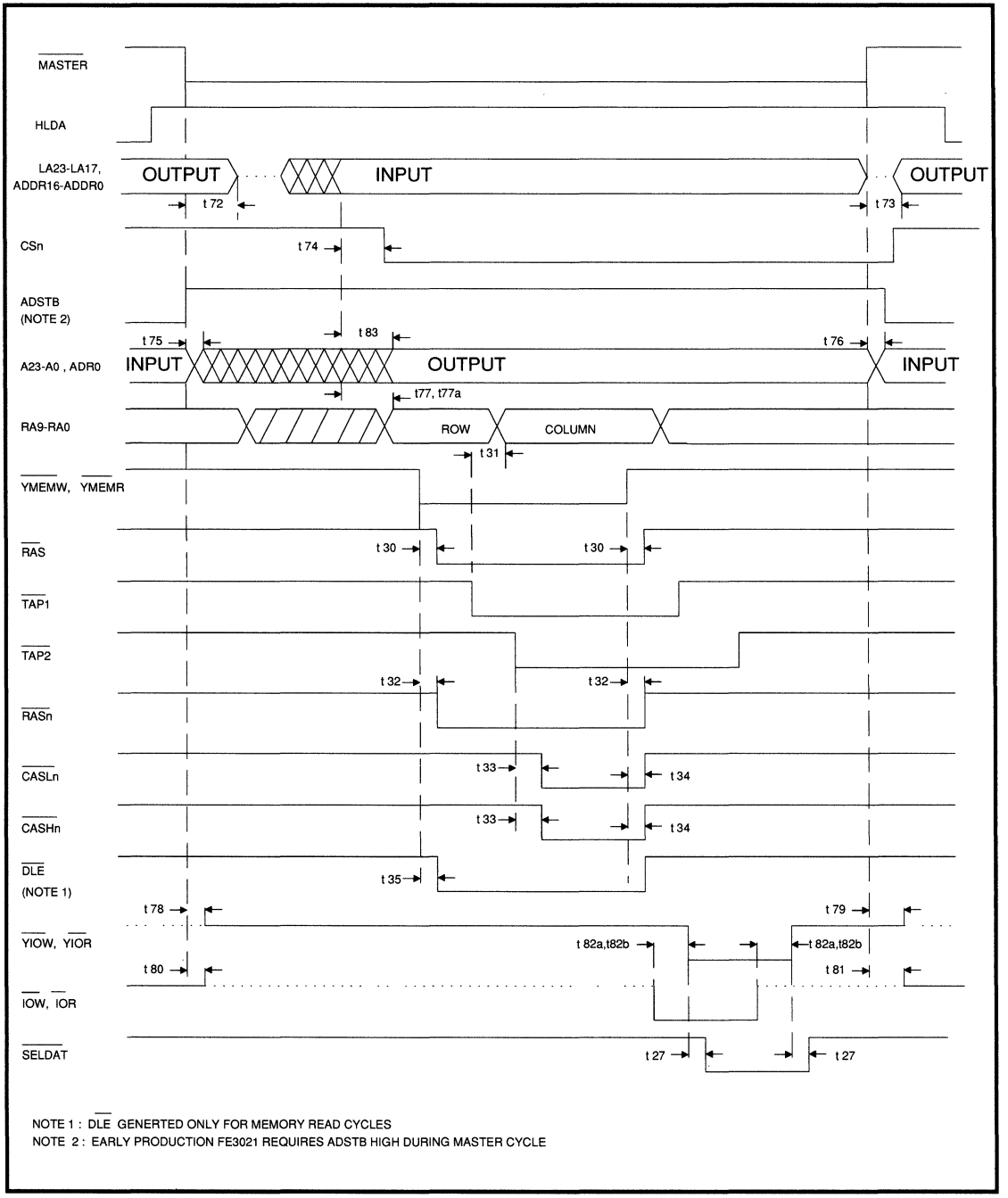


FIGURE 18. REFRESH CYCLE



NOTE 1 : DLE GENERTED ONLY FOR MEMORY READ CYCLES
NOTE 2 : EARLY PRODUCTION FE3021 REQUIRES ADSTB HIGH DURING MASTER CYCLE

FIGURE 19. BUS MASTER CYCLE

12.0 PACKAGE DIAGRAM

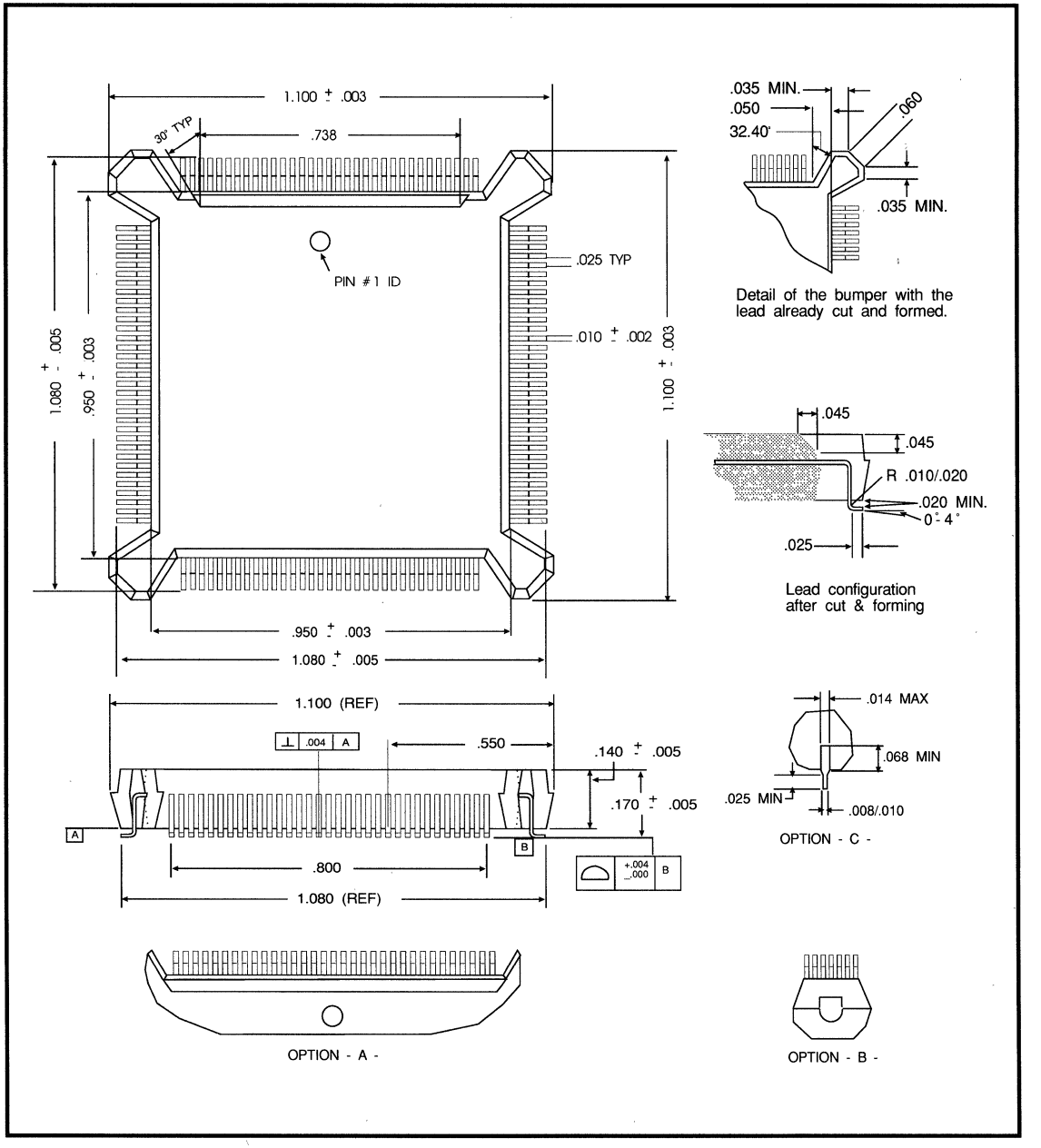


FIGURE 20. 132-PIN PQFP PACKAGE

SYSTEMS LOGIC/PERIPHERAL

FE3031

AT Data Buffer

6

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

ADDITIONAL REFERENCES

IBM AT Technical Reference Manual
Intel Microprocessor and Peripheral Handbook

1.0 INTRODUCTION

1.1 DESCRIPTION

The FE3031 is an IBM* AT data buffer and parity generator/checker in a 100-pin PLCC package that contains all of the data buffers necessary to implement an AT compatible computer. The FE3031 functions as a peripheral data bus buffer, memory data bus buffer, a parity/generator/checker, and PC/AT data bus buffer.

This document describes the pinouts, signals, timing and electrical specifications of the FE3031 AT Data Buffer IC. The FE3031 is part of the FE3600B AT Core Logic chip set for 16 MHz 80286 based AT computers.

1.2 FEATURES

- ❑ 100 Pin PLCC
- ❑ PC AT* Data Bus Buffers
- ❑ Peripheral Data Bus Buffer
- ❑ Memory Data Bus Buffers
- ❑ Parity Generator/Checker
- ❑ 1.25 Micron CMOS Technology

6

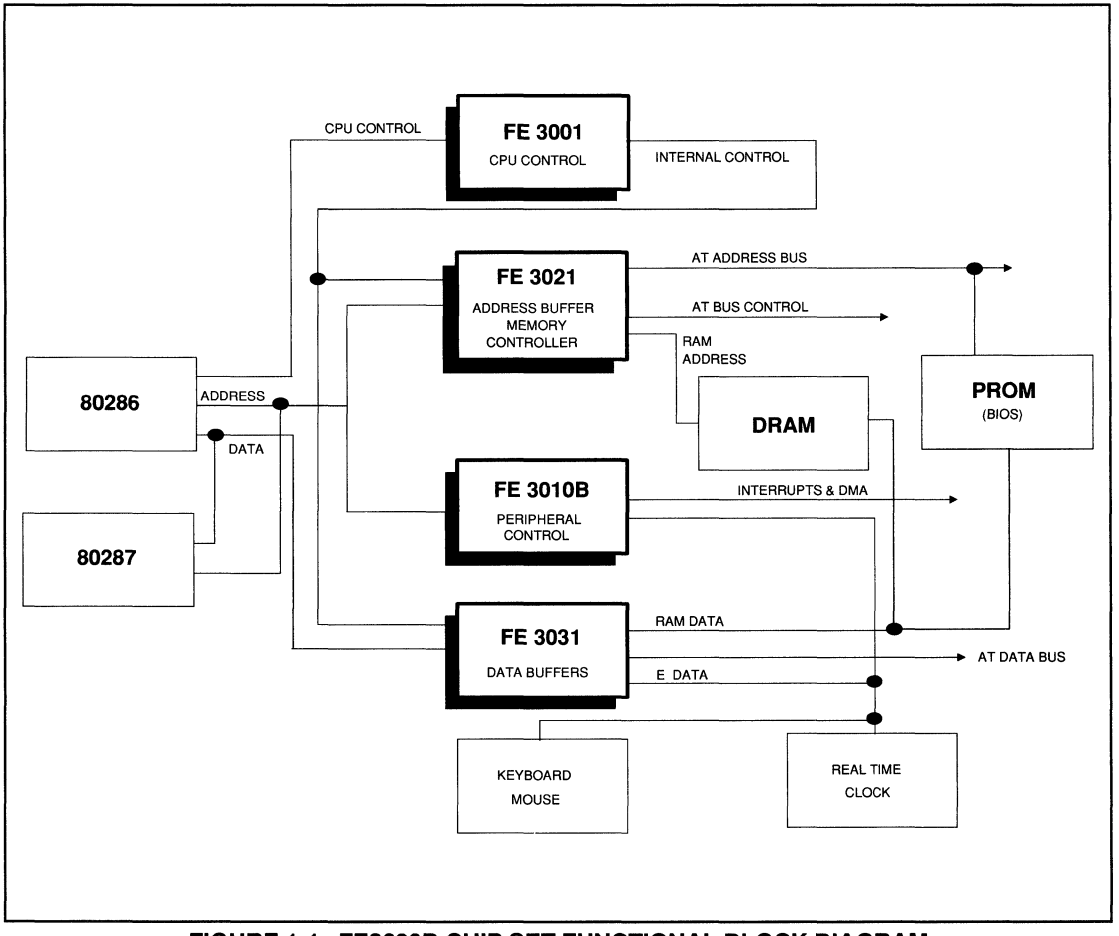


FIGURE 1-1. FE3600B CHIP SET FUNCTIONAL BLOCK DIAGRAM

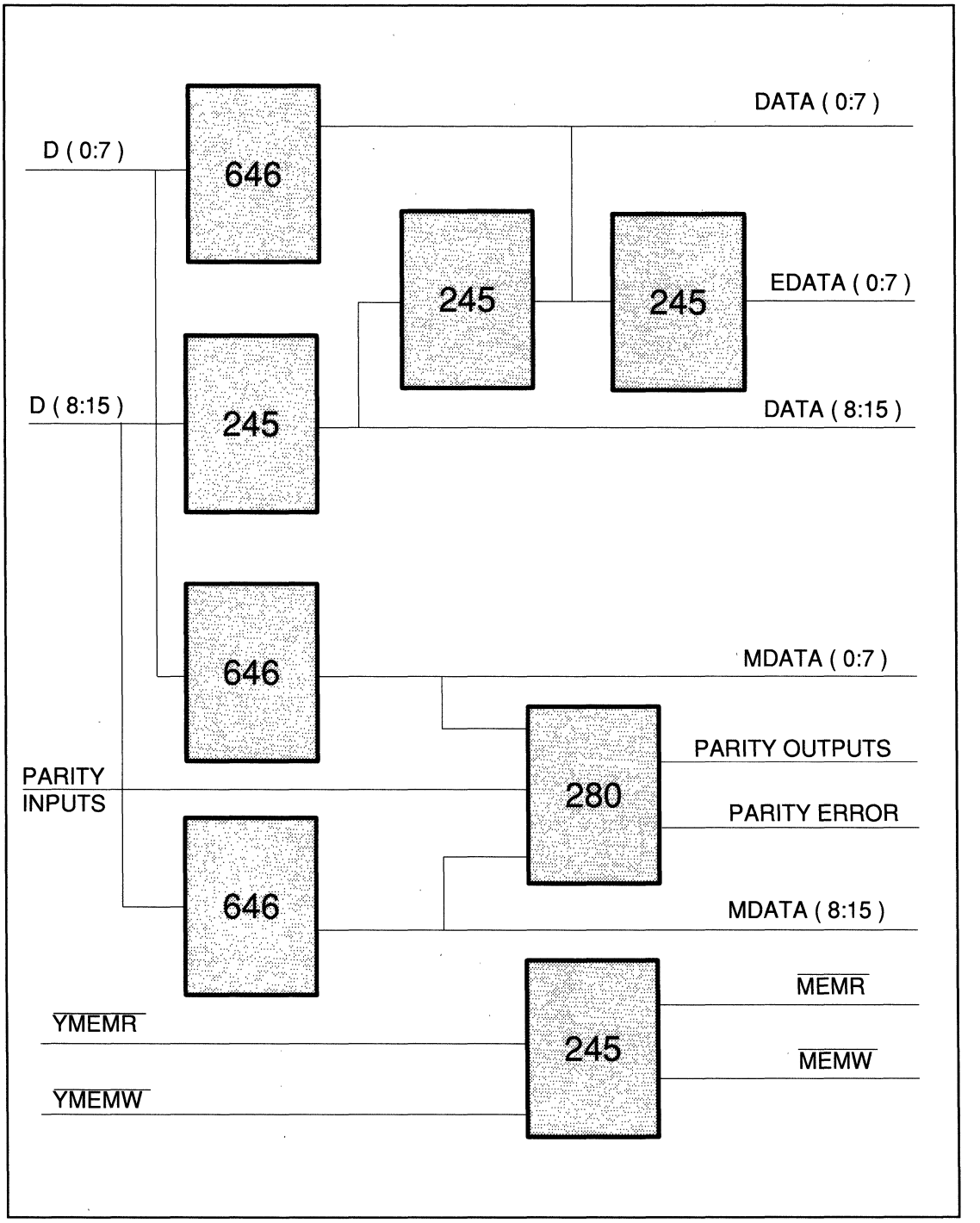


FIGURE 1-2. FE3031 FUNCTIONAL BLOCK DIAGRAM

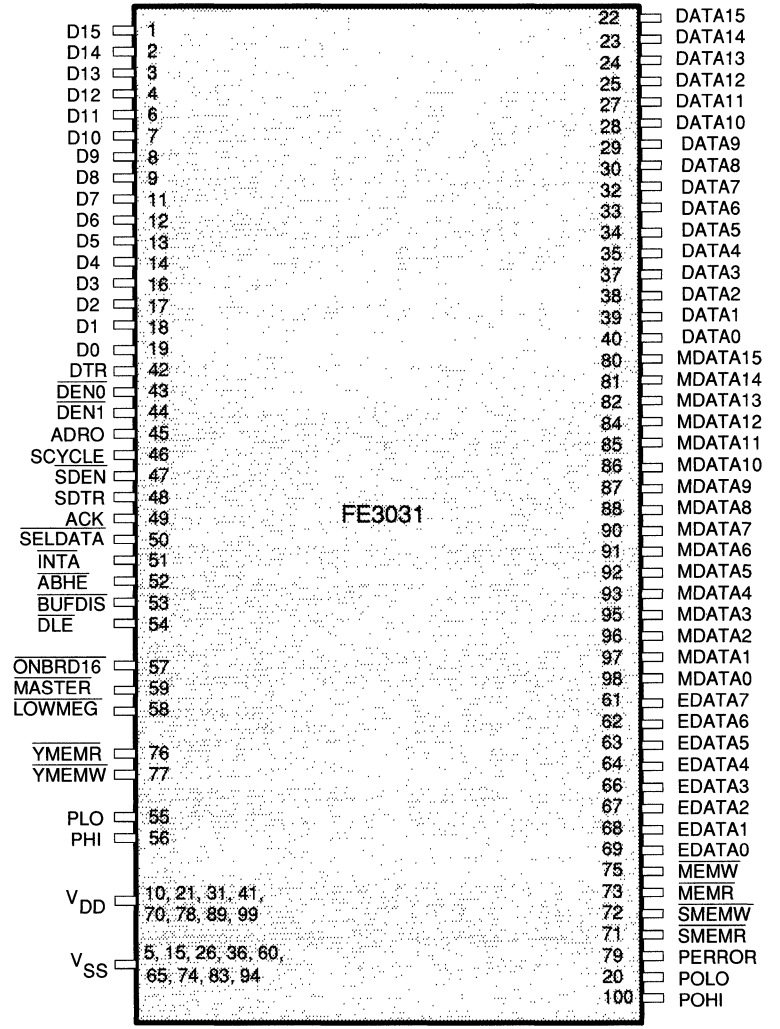


FIGURE 1-3. FE3031 PIN ASSIGNMENTS & LOCATIONS

2.0 SIGNAL DESCRIPTIONS

PIN#	SIGNAL	TYPE	DESCRIPTION
1-4 6-9 11-14 16-19	D(0:15)	I/O	80286 Local Data Bus
5,15 26,36 60,65 74,83 94	V_{SS}		Ground
10,21 31,41 70,78 89,99	V_{DD}		+5V V_{DD}
20	POLO	O	Low byte parity bit to the DRAMs
22-25 27-30 32-35 37-40	DATA (0:15)	I/O	PC/AT Data Bus
42	DTR	I	Data direction for DATA buffers
43	$\overline{\text{DEN0}}$	I	Low byte data enable to DATA buffers
44	$\overline{\text{DEN1}}$	I	High byte data enable to DATA buffers
45	ADR0	I	Address bit 0 for MDATA buffers and byte swap
46	SCYCLE	I	Latch low byte during byte swap read
47	$\overline{\text{SDEN}}$	I	Byte swap data buffer enable
48	SDTR	I	Byte swap data direction to swap buffer
49	ACK	I	DMA Acknowledge signal to the PC/AT bus
50	$\overline{\text{SELDATA}}$	I	EDATA bus enable
51	$\overline{\text{INTA}}$	I	Interrupt acknowledge
52	$\overline{\text{ABHE}}$	I	High byte enable for MDATA bus
53	$\overline{\text{BUFDIS}}$	I	Disable Buffers when low
54	$\overline{\text{DLE}}$	I	Latch MDATA bus during a read
55	PLO	I	Low byte parity bit from DRAMs
56	PHI	I	High byte parity bit from DRAMs
57	$\overline{\text{ONBRD16}}$	I	$\overline{\text{ONBRD}}$ indicates a local

TABLE 2-1. FE3031 SIGNAL DESCRIPTIONS

PIN	SIGNAL	TYPE	DESCRIPTION
58	$\overline{\text{LOWMEG}}$	I	$\overline{\text{LOWMEG}}$ indicates access of low MB of memory
59	$\overline{\text{MASTER}}$	I	Master on PC bus has control of the bus
61-64 66-69	EDATA (0:7)	I/O	Peripheral Data Bus for FE3001, FE3010B, RTC and Keyboard controller
71	$\overline{\text{SMEMR}}$	O	Low 1 MB Memory Read to PC bus
72	$\overline{\text{SMEMW}}$	O	Low 1 MB Memory Write to PC bus
73	$\overline{\text{MEMR}}$	I/O	Memory read to/from AT bus
75	$\overline{\text{MEMW}}$	I/O	Memory read to/from AT bus
76	$\overline{\text{YMEMR}}$	I/O	Memory read to/from FE3001
77	$\overline{\text{YMEMW}}$	I/O	Memory write to/from FE3001
79	PERROR	O	RAM parity error
80-82 84-88 90-93 95-98	MDATA (0:15)	I/O	Memory Data bus
100	POHI	O	High byte parity bit to the DRAMs

TABLE 2-1. FE3031 SIGNAL DESCRIPTIONS, Continued

3.0 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature (operating) = 0° to + 70°C
Storage Temperature = - 40° to +125°C
Voltage on any pin to ground = +7 V
Power Dissipation = 400 mW

4.0 DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{IL}	Input LOW Voltage		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V	
I_{OL}	LOW V Output Current[1]		4	mA	V_{OL} = 0.4 V
I_{OH}	HIGH V Output Current[1]		-4	mA	V_{OH} = 2.4 V
I_{OL}	LOW V Output Current[2]		6.4	mA	V_{OL} = 0.4 V
I_{OH}	HIGH V Output Current[2]		-6.4	mA	V_{OH} = 2.4 V
V_{DD}	Supply Voltage	4.75	5.25	V	

FIGURE 4-1. DC CHARACTERISTICS

Notes:

1. Output currents are for D(0:15), EDATA(0:7), YMEMR, YMEMW, PERROR
2. Output currents are for DATA(0:15), MDATA(0:15), MEMR, MEMW, SMEMR, SMEMW, POLO, PHI

5.0 AC CHARACTERISTICS

SIGNAL PATH		PROP DLY (MAX)[1]	UNIT	NOTES
D(0:7) from	DATA (0:7)	22	ns	
	MDATA (0:7)	20	ns	
	ADR0	30	ns	
	$\overline{\text{BUFDIS}}$	30	ns	
	$\overline{\text{ONBRD16}}$	30	ns	1
	$\overline{\text{YMEMR}}$	30	ns	
	$\overline{\text{DEN0}}$	30	ns	
	DATA (8:15)	40	ns	
	EDATA (0:7)	40	ns	
D(8:15) from	DATA (8:15)	22	ns	
	MDATA (8:15)	20	ns	
	$\overline{\text{ABHE}}$	30	ns	
	$\overline{\text{BUFDIS}}$	30	ns	
	$\overline{\text{ONBRD16}}$	30	ns	1
	$\overline{\text{YMEMR}}$	30	ns	
	$\overline{\text{DEN1}}$	30	ns	
	DATA (0:7)	40	ns	
	EDATA (0:7)	40	ns	
DATA (0:7) from	D(0:7)	22	ns	
	D(8:15)	40	ns	
	DATA(8:15)	22	ns	
	EDATA(0:7)	22	ns	1, 2
	$\overline{\text{SDEN}}$	30	ns	
	$\overline{\text{DEN0}}$	30	ns	
	$\overline{\text{INTA}}$	30	ns	
	$\overline{\text{SELDATA}}$	30	ns	
DATA (8:15) from	D (8:15)	22	ns	
	DATA (0:7)	22	ns	1, 2
	$\overline{\text{DEN1}}$	30	ns	
EDATA (0:7) from	DATA(0:7)	36	ns	
	D(0:7)	36	ns	
	D (8:15)	36	ns	1
	$\overline{\text{INTA}}$	40	ns	
	$\overline{\text{SELDATA}}$	40	ns	
$\overline{\text{YMEMW}}$ from	$\overline{\text{MEMW}}$	33	ns	1
	$\overline{\text{MASTER}}$	40	ns	
$\overline{\text{YMEMR}}$ from	$\overline{\text{MEMR}}$	33	ns	1
	$\overline{\text{MASTER}}$	40	ns	

TABLE 5-1. AC CHARACTERISTICS

Notes: 1. Prop delays are for 75pf load.
2. Add 8 ns for 200pf load.

SIGNAL PATH	PROP DLY (MAX) 1	UNIT	NOTES
$\overline{\text{MEMW}}$ from $\overline{\text{YMEMW}}$	20	ns	
$\overline{\text{MASTER}}$	30	ns	1
$\overline{\text{ONBRD16}}$	30	ns	
$\overline{\text{MEMR}}$ from $\overline{\text{YMEMW}}$	20	ns	
$\overline{\text{MASTER}}$	30	ns	1
$\overline{\text{ONBRD16}}$	30	ns	
$\overline{\text{SMEMW}}$ from $\overline{\text{YMEMW}}$	20	ns	
$\overline{\text{MASTER}}$	30	ns	1
$\overline{\text{ONBRD16}}$	30	ns	
$\overline{\text{SMEMR}}$ from $\overline{\text{YMEMW}}$	20	ns	
$\overline{\text{MASTER}}$	30	ns	1
$\overline{\text{ONBRD16}}$	30	ns	
PERROR from MDATA(0:15)	40	ns	
PLO	40	ns	
PHI	40	ns	1
ADR0	40	ns	
$\overline{\text{ABHE}}$	40	ns	
POLO from D(0:7)	35	ns	1
POHI from D(8:15)	35	ns	1
MDATA (0:7) from D (0:7)	18	ns	
ADR0	30	ns	
$\overline{\text{ONBRD16}}$	30	ns	1
$\overline{\text{YMEMR}}$	30	ns	
$\overline{\text{DLE}}$	30	ns	
MDATA (8:15) from D (8:15)	18	ns	
$\overline{\text{ABHE}}$	30	ns	
$\overline{\text{ONBRD16}}$	30	ns	1
$\overline{\text{YMEMR}}$	30	ns	
$\overline{\text{DLE}}$	30	ns	

TABLE 5-1. AC CHARACTERISTICS, Continued

Notes: 1. Prop delays are for 75pf load.
2. Add 8 ns for 200pf load.

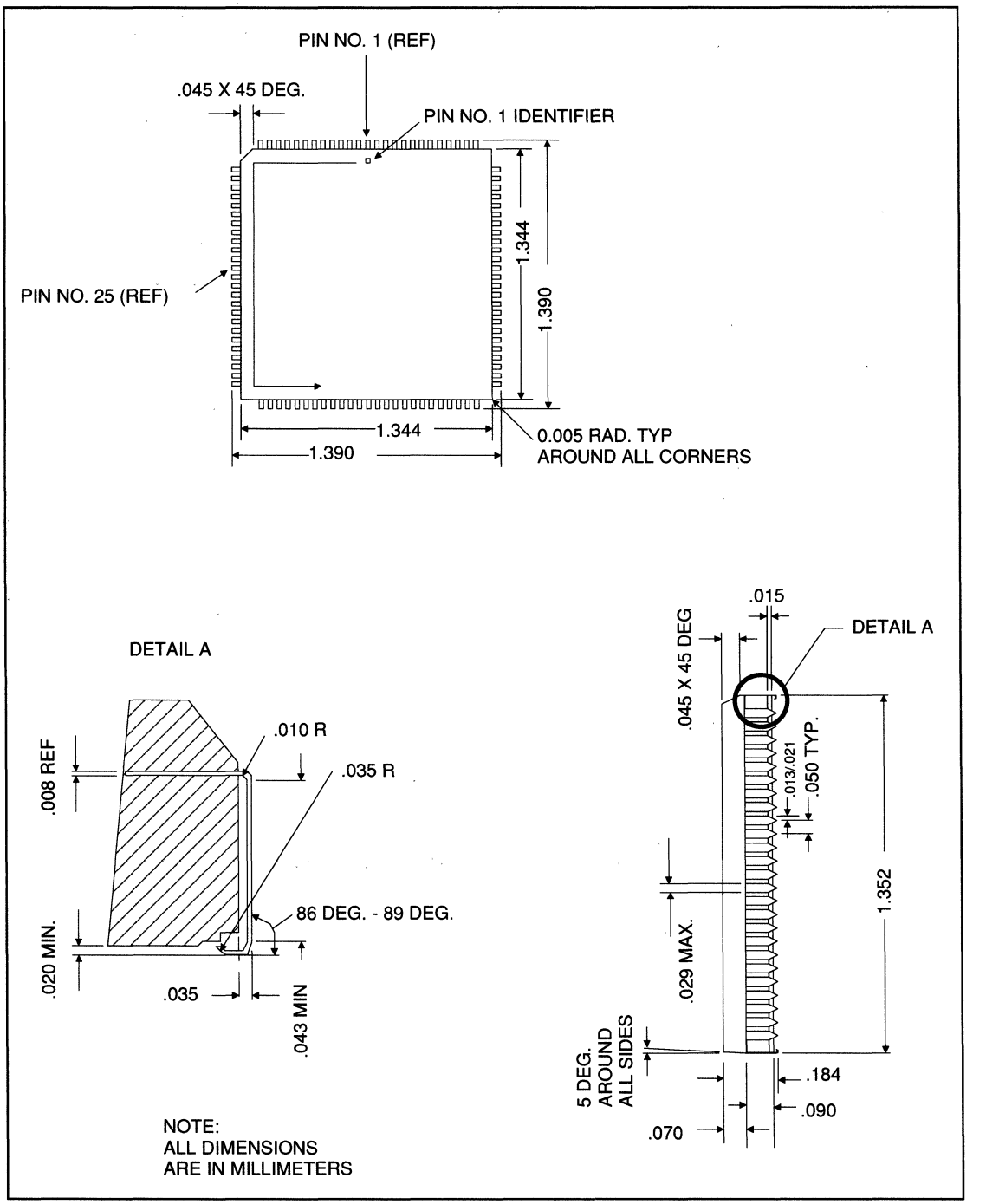


FIGURE 5-1. 100-PIN PLCC PACKAGING DIAGRAM

6.0 PC/AT DATA BUS CYCLES

This description of the data bus cycles of the FE3600B PC AT expansion bus includes CPU, DMA, and MASTER cycles. The data portion of the PC AT expansion bus is a 16-bit wide bus divided into two bytes. In general, the low byte (DATA[0:7]) is accessed during cycles in which the address is even. The high byte (DATA[8:15]) is accessed when the address is odd. During 16-bit operations, both low and high bytes are accessed. There are several combinations of byte wide, word wide, even and odd addressing. Each of these combinations present a unique pattern of bus buffer enables and directions. These data buffer control states are described in this document.

NOTES:

* Eight bit devices on the PC AT bus are always on the low byte (DATA[0:7]) of the expansion bus regardless of address. Sixteen bit devices use ADR0 and *EBHE* to distinguish between high and low byte transfers.

* In previous designs, the data buffers on the PC AT were inactive during DMA. This was due to the on-board DRAM being on the system bus. Now that the DRAM is on the 286 local bus the data buffers must be enabled and directed during DMA operations.

* A block diagram of the data bus hardware on the PC AT board is shown in Figure 5-1. It represents the equivalent 74LSXXX circuitry for the data buffers contained on the board. Signals used in this document are discussed in Table 6-1.

6

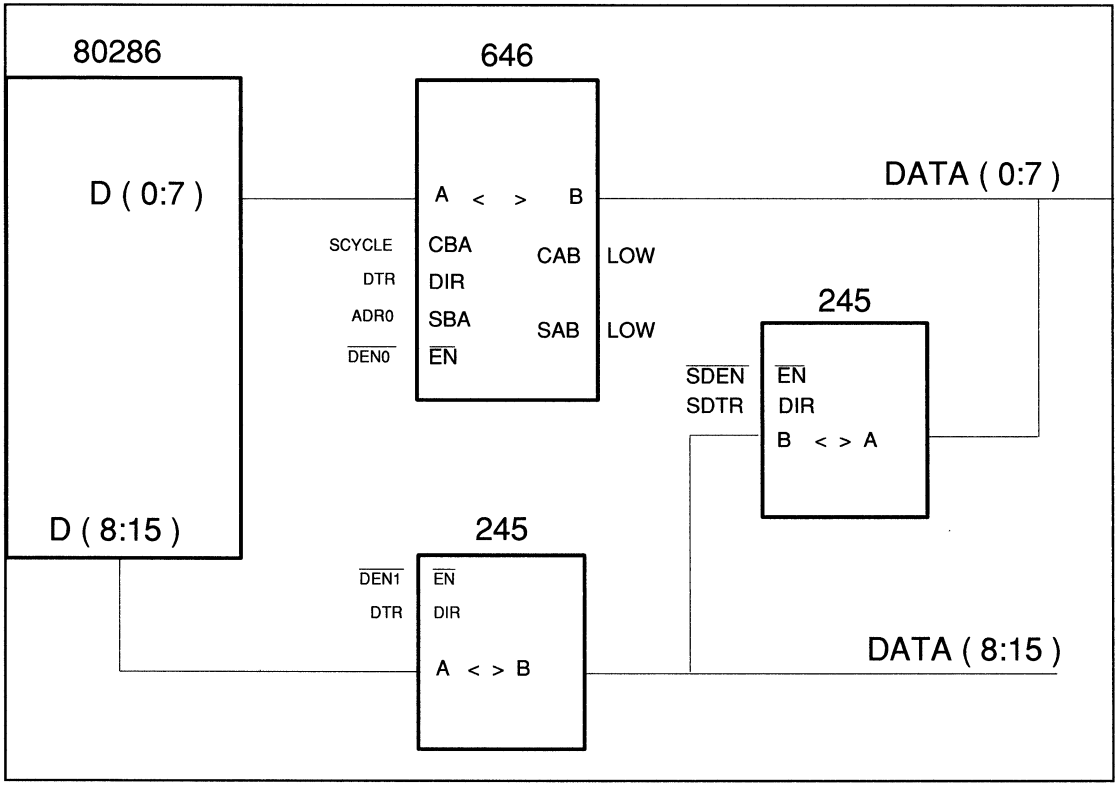


FIGURE 6-1. PC/AT DATA BUS ARCHITECTURE

'646				
$\overline{EN}$ $\overline{DEN0}$	DIR DTR	CBA SCYCLE	SBA ADR0	OPERATION
X	X	^	X	LATCH B DATA
0	0	X	0	A <------B (REAL TIME)
0	0	X	1	A <------B (LATCHED DATA)
0	1	X	X	A ------>B (REAL TIME)
1	X	X	X	BUFFERS DISABLED

'245	
DIR	OPERATION
0	A <---------- B
1	A ----------> B

COMMAND SIGNALS	DEFINITIONS
S0, S1	BUS CYCLE STATUS FROM 286
$\overline{MEMR}$	SYSTEM MEMORY READ
$\overline{MEMW}$	SYSTEM MEMORY WRITE
$\overline{IOR}$	SYSTEM I/O READ
$\overline{IOW}$	SYSTEM I/O WRITE
$\overline{NPCS}$	NUMERIC PROCESSOR CHIP SELECT
A0	ADDRESS BIT 0 FROM 286
$\overline{BHE}$	BUS HIGH ENABLE FROM 286
HLDA	HOLD ACKNOWLEDGE FROM 286
HLDA1	DMA HOLD ACKNOWLEDGE FROM DMA CONTROLLER
$\overline{PROMSL}$	BIOS DECODE FROM MEMORY/IO DECODER
$\overline{ONBRD}$	ON BOARD DRAM OR I/O DECODE
$\overline{IOCS16}$	16-BIT I/O DEVICE DECODE FROM EXPANSION BUS
$\overline{MEMCS16}$	16-BIT MEMORY DEVICE DECODE FROM EXPANSION BUS
$\overline{MASTER}$	BUS CONTROL SIGNAL FROM BUS MASTER
CONTROL SIGNALS	**DEFINITIONS**
DTR	DATA TRANSMIT/RECEIVE
$\overline{DEN0}$	LOW BYTE DATA ENABLE
$\overline{DEN1}$	HIGH BYTE DATA ENABLE
$\overline{SDEN}$	BYTE SWAP BUFFER ENABLE
SCYCLE	LOW BYTE DATA LATCH
SDTR	BYTE SWAP BUFFER TRANSMIT/RECEIVE

TABLE 6-1. SIGNAL DEFINITIONS

7.0 CPU CYCLES

The following cycles represent data cycles under CPU control for all devices excluding the on board DRAM and the 80287 Math Coprocessor. Since the 80287 and on-board DRAM are on the local bus, the data bus drivers for the expansion bus will be disabled. This is accomplished by setting DEN0, DEN1 and SDEN = 1 when ONBRD + /MNIO = 0 or NPCS = 0. Note that on-board I/O is indicated by ONBRD + MNIO = 0. On-board I/O devices are on the system bus.

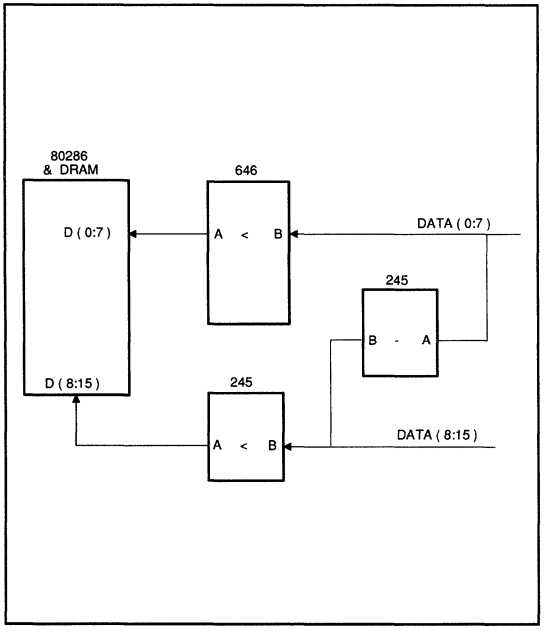
For all CPU cycles HLDA=0 and INTA- =1. In the following tables, CS16 indicates that there is a 16-bit device on the expansion bus. The boolean equation for CS16 is:

CS16 = PROMCS * (IOCS16 + MNIO) * (MEMCS16 + /MNIO)

The following cycles are described in this section.

6

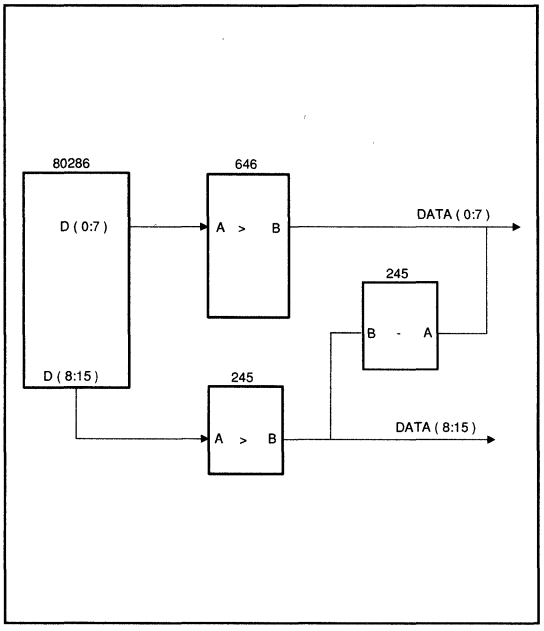
7.1 16-BIT READ FROM 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	0

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADRO	0

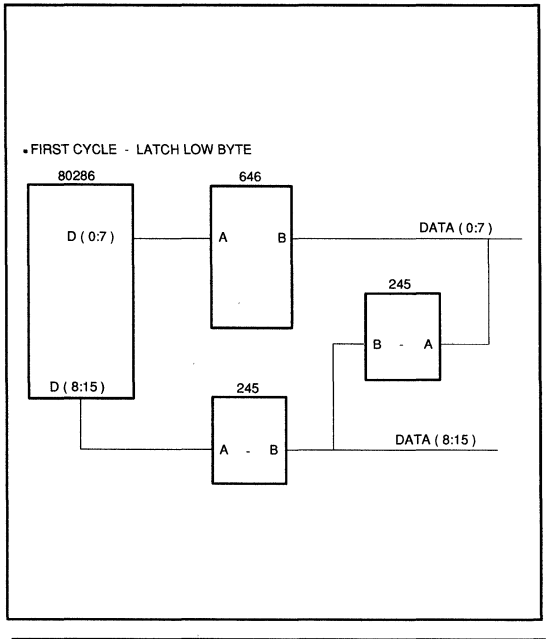
7.2 16-BIT WRITE TO 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	1
S0	0
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	0

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADRO	0

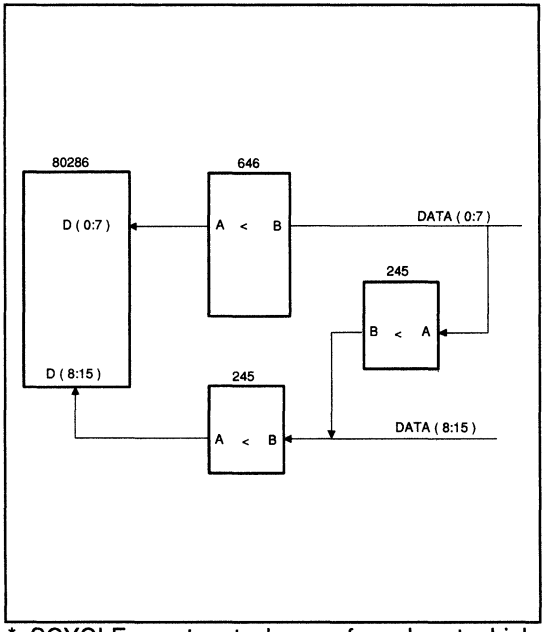
7.3 16-BIT READ FROM 8-BIT DEVICE



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	X
$\overline{DEN0}$	X
$\overline{DEN1}$	X
$\overline{SDEN}$	1
SCYCLE	^
SDTR	X
ADR0	0

* Second cycle - Enable latched low byte to 286 low byte and enable bus low byte to 286 high byte.



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	0
SCYCLE	X*
SDTR	1
ADRO	1

* SCYCLE must not change from low to high during the cycle.

7.4 16-BIT WRITE TO 8-BIT DEVICE

INPUT SIGNALS	STATE
S1	1
S0	0
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	1

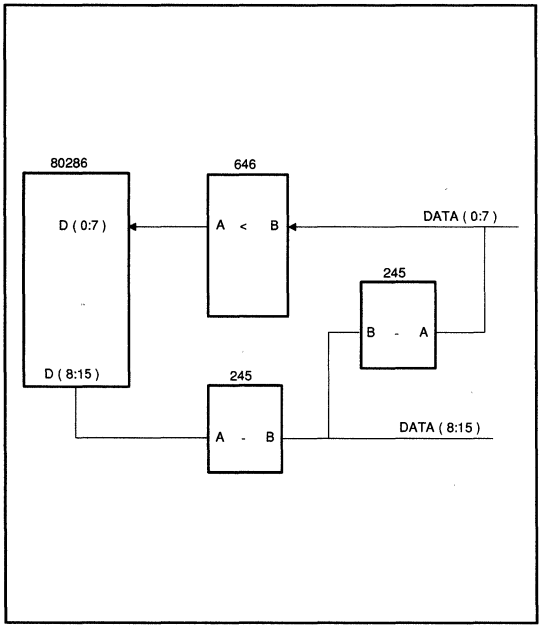
❑ FIRST CYCLE

- 8-bit, low byte write to 8-bit device or 16-bit device
- ADR0 is driven low during this cycle
- EBHE is driven high during this cycle

❑ SECOND CYCLE

- 8-bit, high byte write to 8-bit device
- ADR0 is driven high during this cycle
- EBHE is driven low during this cycle

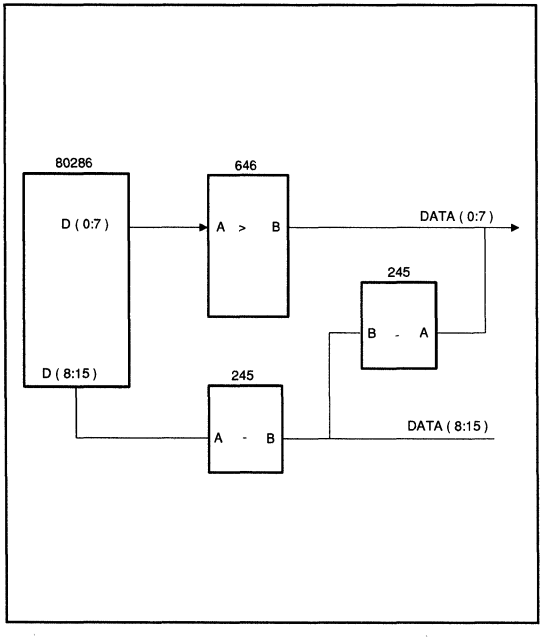
7.5 8-BIT, LOW BYTE READ FROM 8-BIT OR 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
$\overline{BHE}$	1
$\overline{CS16}$	X

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN1}$	1
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADR0	0

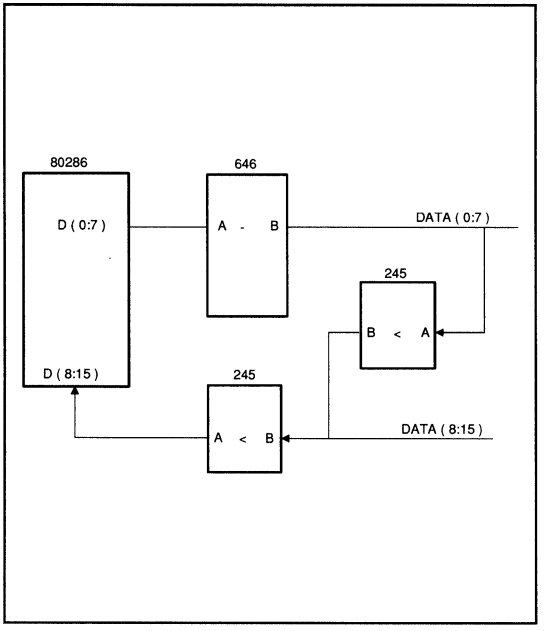
7.6 8-BIT, LOW BYTE WRITE TO 8-BIT OR 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	1
A0	0
$\overline{BHE}$	1
$\overline{CS16}$	X

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN1}$	1
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADR0	0

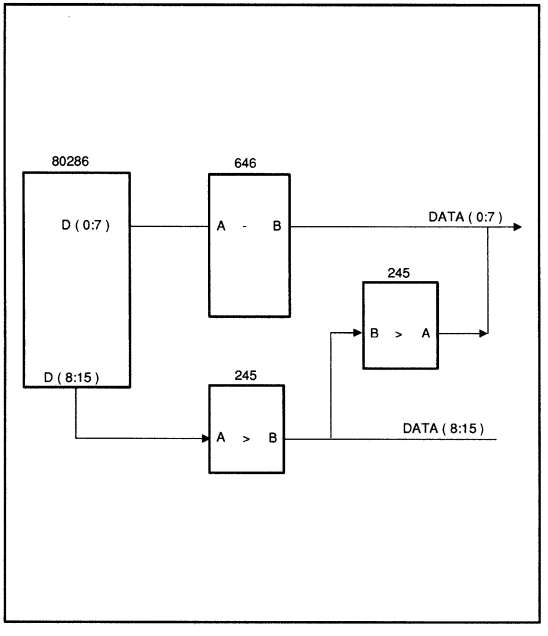
7.7 8-BIT, HIGH BYTE READ FROM 8-BIT DEVICE



INPUT SIGNALS	STATE
S1	0
S0	1
A0	1
$\overline{BHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	0
SCYCLE	X
SDTR	1
ADR0	1

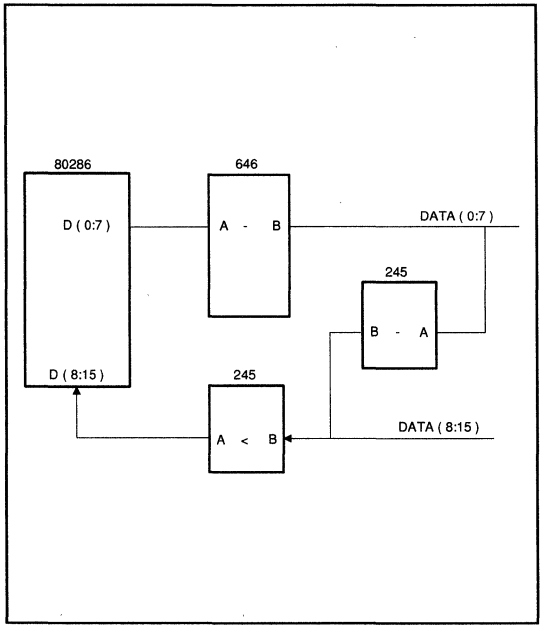
7.8 8-BIT, HIGH BYTE WRITE TO 8-BIT DEVICE



INPUT SIGNALS	STATE
S1	1
S0	0
A0	1
$\overline{BHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	0
SCYCLE	X
SDTR	0
ADR0	1

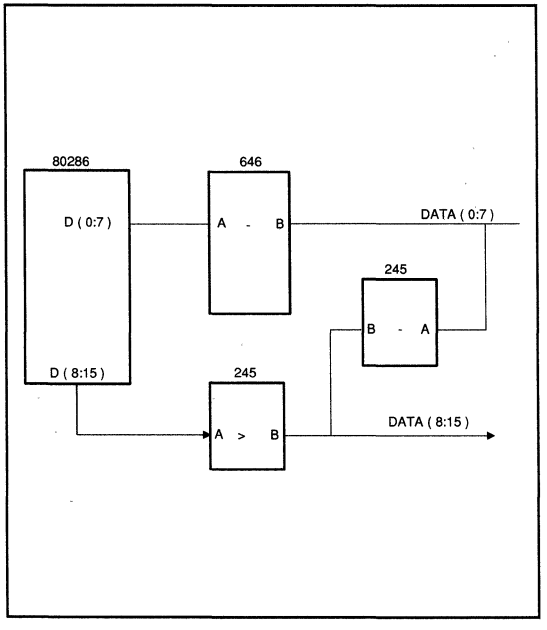
7.9 8-BIT, HIGH BYTE READ FROM 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	0
S0	1
A0	1
$\overline{BHE}$	0
$\overline{CS16}$	0

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADR0	1

7.10 8-BIT, HIGH BYTE WRITE TO 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	1
S0	0
A0	1
$\overline{BHE}$	0
$\overline{CS16}$	0

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADR0	1

8.0 DMA CYCLES

The following cycles represent data cycles under DMA control for all devices. DMA may be for on board DRAM (ONBRD =0) or system memory (ONBRD =1). Note that ONBRD decode for on-board I/O will be disabled during DMA.

The following DMA cycles are described in this section.

- ❑ For on board DRAM ($\overline{ONBRD}$ = 0)

8.1 8-bit DMA from even memory address to 8-bit I/O device.
8.2 8-bit DMA to even memory address from 8-bit I/O device.
8.3 8-bit DMA from odd memory address to 8-bit I/O device.
8.4 8-bit DMA to odd memory address from 8-bit I/O device.
8.5 16-bit DMA from memory to 16-bit I/O.
8.6 16-bit DMA to memory from 16-bit I/O.

- ❑ For system memory (ONBRD = 1)

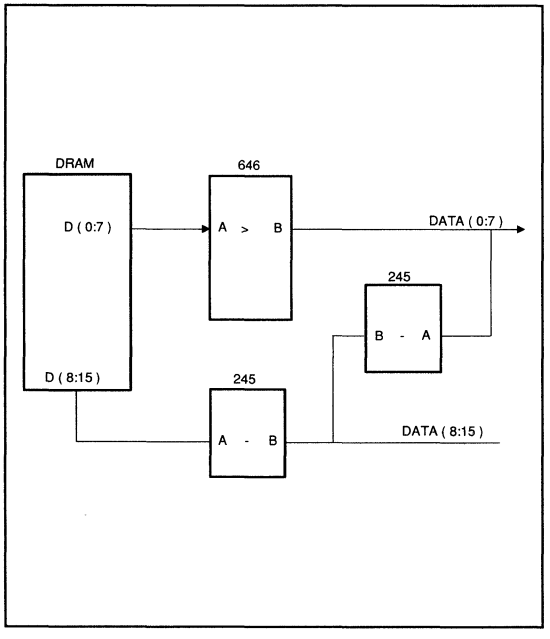
8.7 8-bit DMA from 16-bit memory, odd address to 8-bit I/O device.
8.8 8-bit DMA to 16-bit memory, odd address from 8-bit I/O device.

- ❑ For all other DMA cycles the data buffers are disabled.

8.9 All other DMA cycles.

For all DMA cycles HLDA=1, HLDA1=1 and MASTER =1.

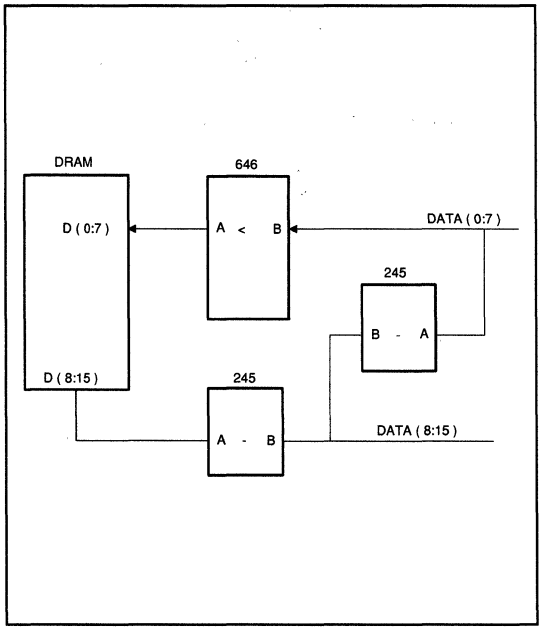
8.1 8-BIT DMA TRANSFER FROM EVEN MEMORY ADDRESS TO 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{DMAMR}$	0
$\overline{MEMW}$	1
$\overline{IOR}$	1
$\overline{IOW}$	0
ADR0	0
$\overline{EBHE}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	0
$\overline{DEN1}$	1
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

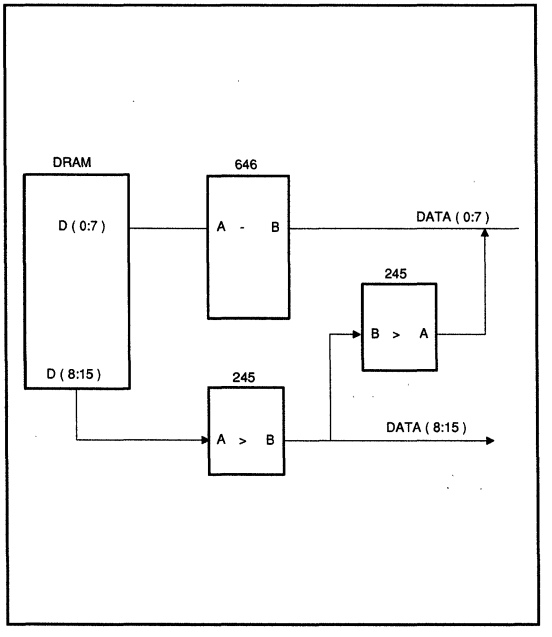
8.2 8-BIT DMA TRANSFER TO EVEN MEMORY ADDRESS FROM 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{DMAMR}$	1
$\overline{MEMW}$	0
$\overline{IOR}$	0
$\overline{IOW}$	1
ADR0	0
$\overline{EBHE}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN1}$	1
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

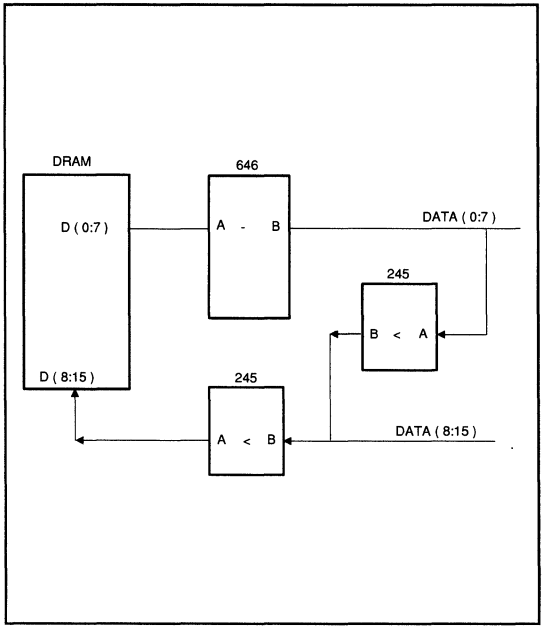
8.3 8-BIT DMA TRANSFER FROM ODD MEMORY ADDRESS TO 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{DMAMR}$	0
$\overline{MEMW}$	1
$\overline{IOR}$	1
$\overline{IOW}$	0
ADR0	1
$\overline{EBHE}$	0

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	0
SCYCLE	X
SDTR	0

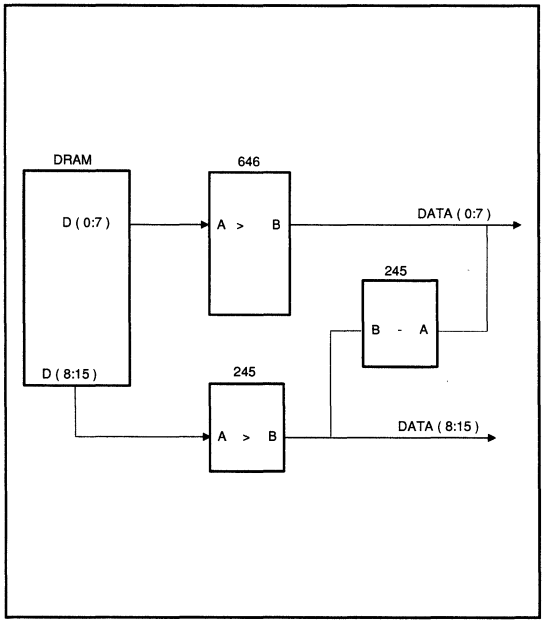
8.4 8-BIT DMA TRANSFER TO ODD MEMORY ADDRESS FROM 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{DMAMR}$	1
$\overline{MEMW}$	0
$\overline{IOR}$	0
$\overline{IOW}$	1
ADR0	1
$\overline{EBHE}$	0

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	0
SCYCLE	X
SDTR	1

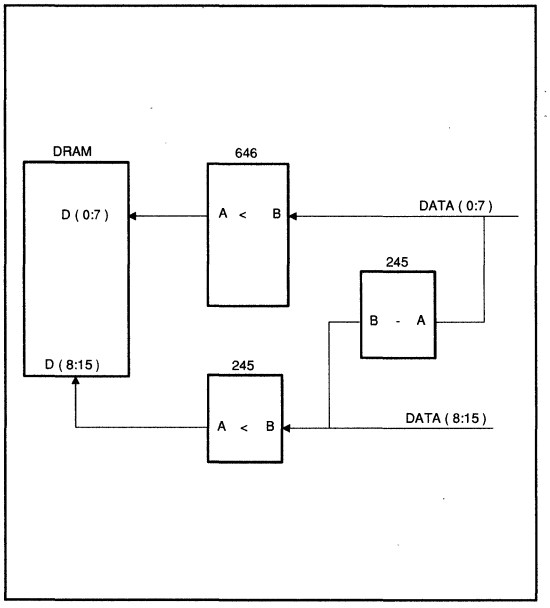
8.5 16-BIT DMA TRANSFER FROM MEMORY TO 16-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{DMAMR}$	0
$\overline{MEMW}$	1
$\overline{IOR}$	1
$\overline{IOW}$	0
ADR0	0
$\overline{EBHE}$	0

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

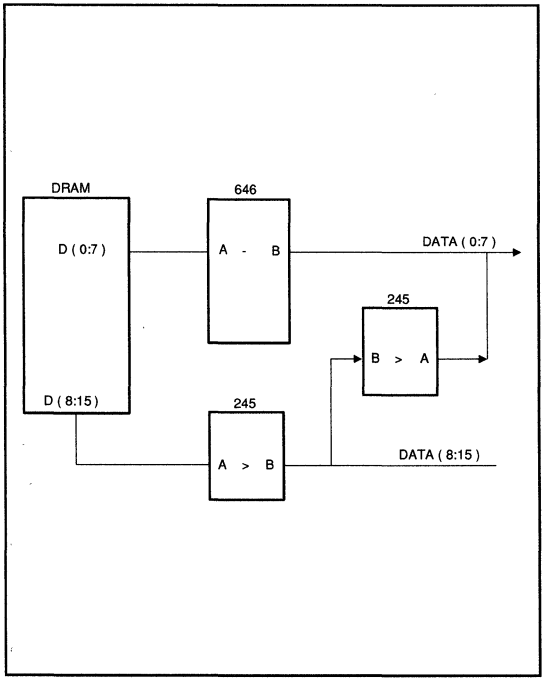
8.6 16-BIT DMA TRANSFER TO MEMORY FROM 16-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{DMAMR}$	1
$\overline{MEMW}$	0
$\overline{IOR}$	0
$\overline{IOW}$	1
ADR0	0
$\overline{EBHE}$	0

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

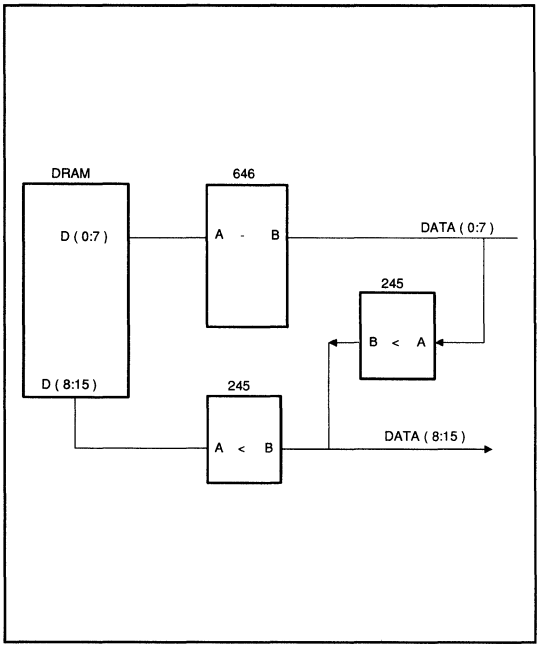
8.7 8-BIT DMA FROM 16-BIT MEMORY, ODD ADDRESS TO 8-BIT I/O DEVICE.



INPUT SIGNALS	STATE
$\overline{DMAMR}$	0
$\overline{MEMW}$	1
$\overline{IOR}$	1
$\overline{IOW}$	0
ADR0	1
$\overline{EBHE}$	0
$\overline{MEMCS16}$ * $\overline{PROMSL}$	0

CONTROL SIGNALS	STATE
DTR	X
$\overline{DEN0}$	1
$\overline{DEN1}$	1
$\overline{SDEN}$	0
SCYCLE	X
SDTR	0

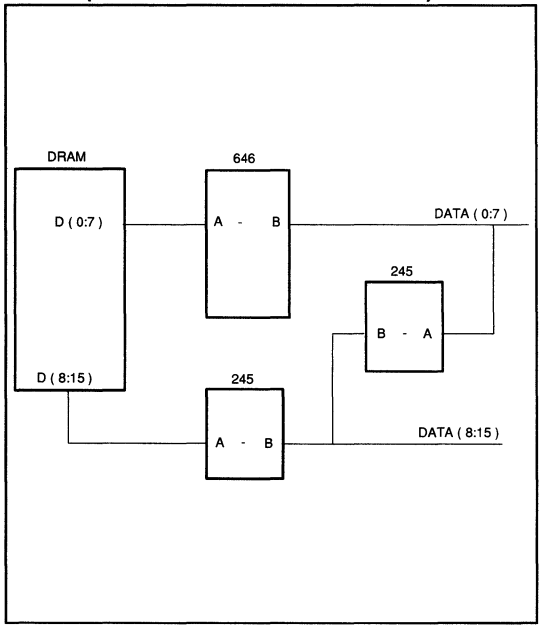
8.8 8-BIT DMA TO 16-BIT MEMORY, ODD ADDRESS FROM 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	1
$\overline{\text{MEMW}}$	0
$\overline{\text{IOR}}$	0
$\overline{\text{IOW}}$	1
ADR0	1
$\overline{\text{EBHE}}$	0
$\overline{\text{MEMCS16}}$ * $\overline{\text{PROMSL}}$	0

CONTROL SIGNALS	STATE
DTR	X
$\overline{\text{DEN0}}$	1
$\overline{\text{DEN1}}$	1
$\overline{\text{SDEN}}$	0
SCYCLE	X
SDTR	1

8.9 ALL OTHER DMA CYCLES (DATA BUFFERS DISABLED)



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	
$\overline{\text{MEMW}}$	
$\overline{\text{IOR}}$	
$\overline{\text{IOW}}$	
ADR0	
$\overline{\text{EBHE}}$	0

CONTROL SIGNALS	STATE
DTR	X
$\overline{\text{DEN0}}$	1
$\overline{\text{DEN1}}$	1
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

9.0 BUS MASTER CYCLES

The following cycles represent data cycles under the control of a bus master other than the 80286 or DMA controller. This condition is indicated by hold acknowledge active (HLDA=1) and bus master asserted (MASTER = 0). It is assumed that the bus master is always a 16-bit device. On-board DRAM and on-board I/O are distinguished by the memory or I/O read/write commands.

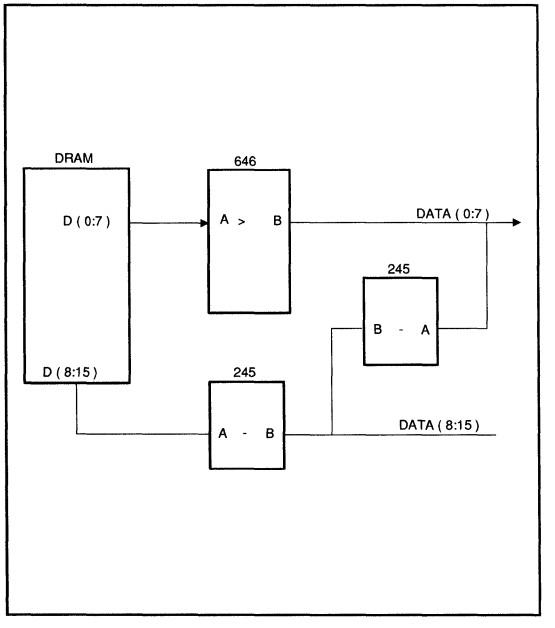
- ❑ For on-board DRAM

9.1 8-bit transfer low byte read from memory
9.2 8-bit transfer low byte write to memory
9.3 8-bit transfer high byte read from memory
9.4 8-bit transfer high byte write to memory
9.5 16-bit transfer read from memory
9.6 16-bit transfer write to memory

- ❑ For system memory and I/O

9.7 8-bit transfer high byte read from 8-bit system memory or I/O
9.8 8-bit transfer high byte write to 8-bit system memory or I/O

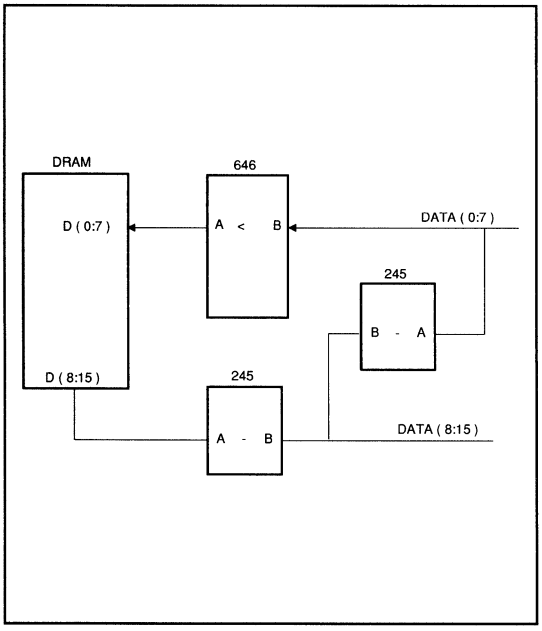
9.1 8-BIT LOW BYTE READ FROM MEMORY



INPUT SIGNALS	STATE
$\overline{\text{MEMR}}$	0
$\overline{\text{MEMW}}$	1
ADR0	0
$\overline{\text{EBHE}}$	1
$\overline{\text{CS16}}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{\text{DEN0}}$	0
$\overline{\text{DEN1}}$	1
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

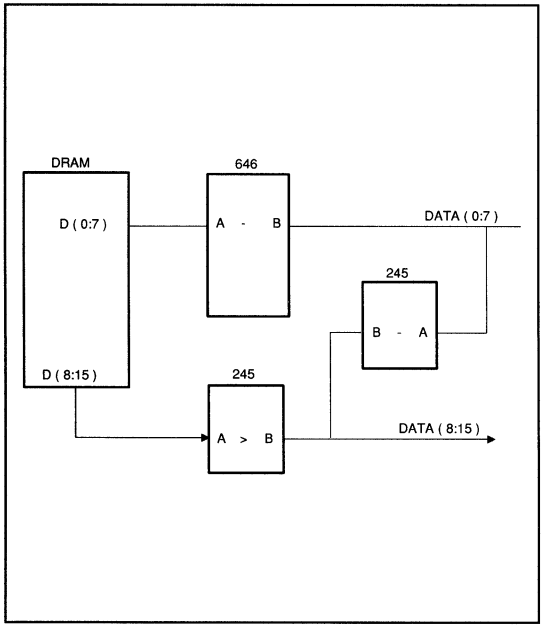
9.2 8-BIT LOW BYTE WRITE TO MEMORY



INPUT SIGNALS	STATE
$\overline{MEMR}$	1
$\overline{MEMW}$	0
ADR0	0
$\overline{EBHE}$	1
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN1}$	1
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

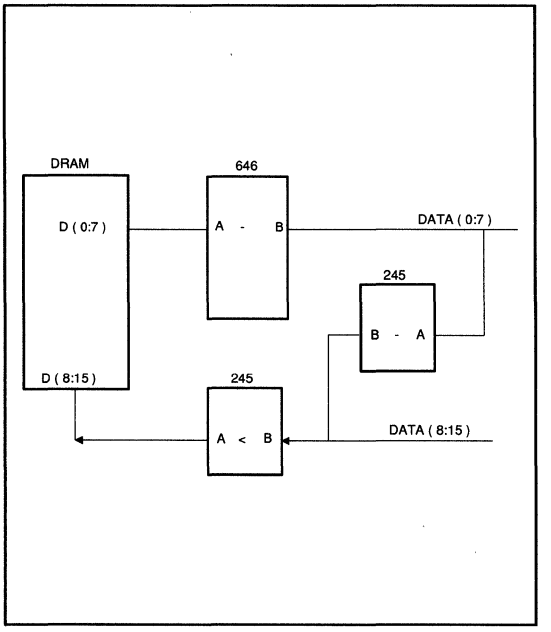
9.3 8-BIT HIGH BYTE READ FROM MEMORY



INPUT SIGNALS	STATE
$\overline{MEMR}$	0
$\overline{MEMW}$	1
ADR0	1
$\overline{EBHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

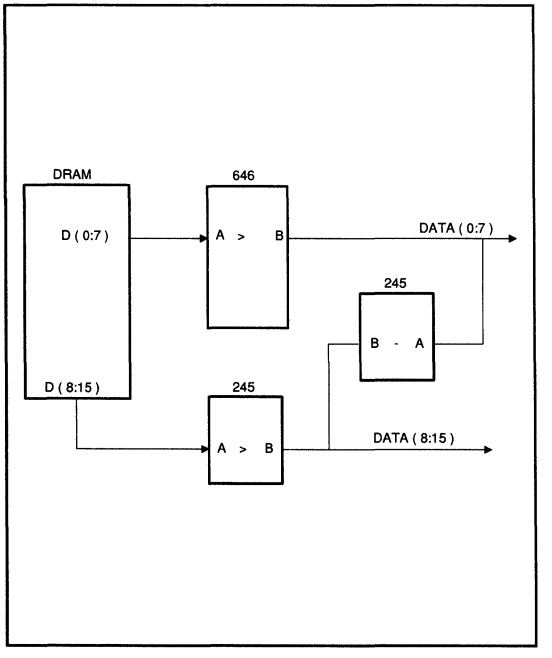
9.4 8-BIT HIGH BYTE WRITE TO MEMORY



INPUT SIGNALS	STATE
$\overline{MEMR}$	1
$\overline{MEMW}$	0
ADR0	1
$\overline{EBHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

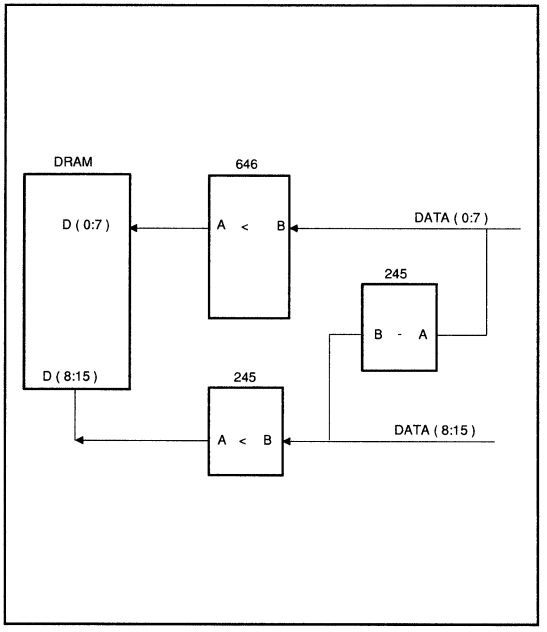
9.5 16-BIT READ FROM MEMORY



INPUT SIGNALS	STATE
$\overline{MEMR}$	0
$\overline{MEMW}$	1
ADR0	0
$\overline{EBHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

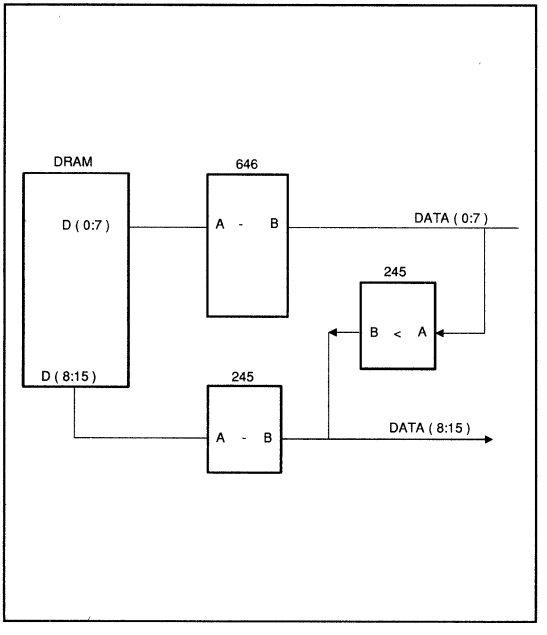
9.6 16-BIT WRITE TO MEMORY



INPUT SIGNALS	STATE
$\overline{MEMR}$	1
$\overline{MEMW}$	0
ADR0	0
$\overline{EBHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

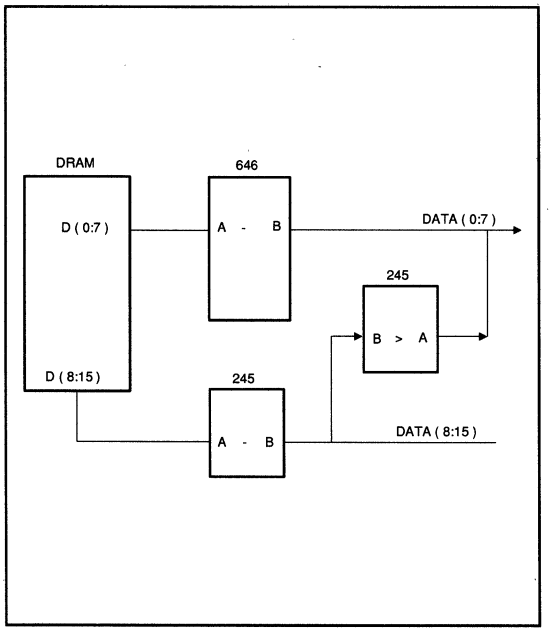
9.7 8-BIT HIGH BYTE READ FROM 8-BIT DEVICE



INPUT SIGNALS	STATE
$\overline{MEMR}$ * $\overline{IOR}$	0
$\overline{MEMW}$ * $\overline{IOW}$	1
ADR0	1
$\overline{EBHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	X
$\overline{DEN0}$	1
$\overline{DEN1}$	1
$\overline{SDEN}$	0
SCYCLE	X
SDTR	1

9.8 8-BIT HIGH BYTE WRITE TO 8-BIT DEVICE



INPUT SIGNALS	STATE
$\overline{MEMR}$ * $\overline{IOR}$	1
$\overline{MEMW}$ * $\overline{IOW}$	0
ADR0	1
$\overline{EBHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	X
$\overline{DEN0}$	1
$\overline{DEN1}$	1
$\overline{SDEN}$	0
SCYCLE	X
SDTR	0

FE3031A

AT Data Buffer

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

ADDITIONAL REFERENCES

IBM AT Technical Reference Manual
Intel Microprocessor and Peripheral Handbook

1.0 INTRODUCTION

1.1 DESCRIPTION

The FE3031A is an IBM AT data buffer and parity generator/checker in a 100-pin PLCC package that contains all of the data buffers necessary to implement an AT compatible computer. The FE3031A functions as a peripheral data bus buffer, memory data bus buffer, a parity/generator/checker, and PC/AT data bus buffer.

This document describes the pinouts, signals, timing and electrical specifications of the FE3031A AT Data Buffer IC, which is part of the FE3600 B/C AT Core Logic chip set for 16 MHz 80286 and 80386SX based AT computers at speeds up to 20 MHz.

1.2 FEATURES

- Data Buffer for the FE3600 BC AT 4-chip Core Logic Set
- For 80286 and 80386SX systems, up to 20 MHz.
- Peripheral Data Bus Buffer
- Memory Data Bus Buffers
- Parity Generator/Checker
- 1.25 Micron CMOS Technology
- 100 Pin PLCC

7

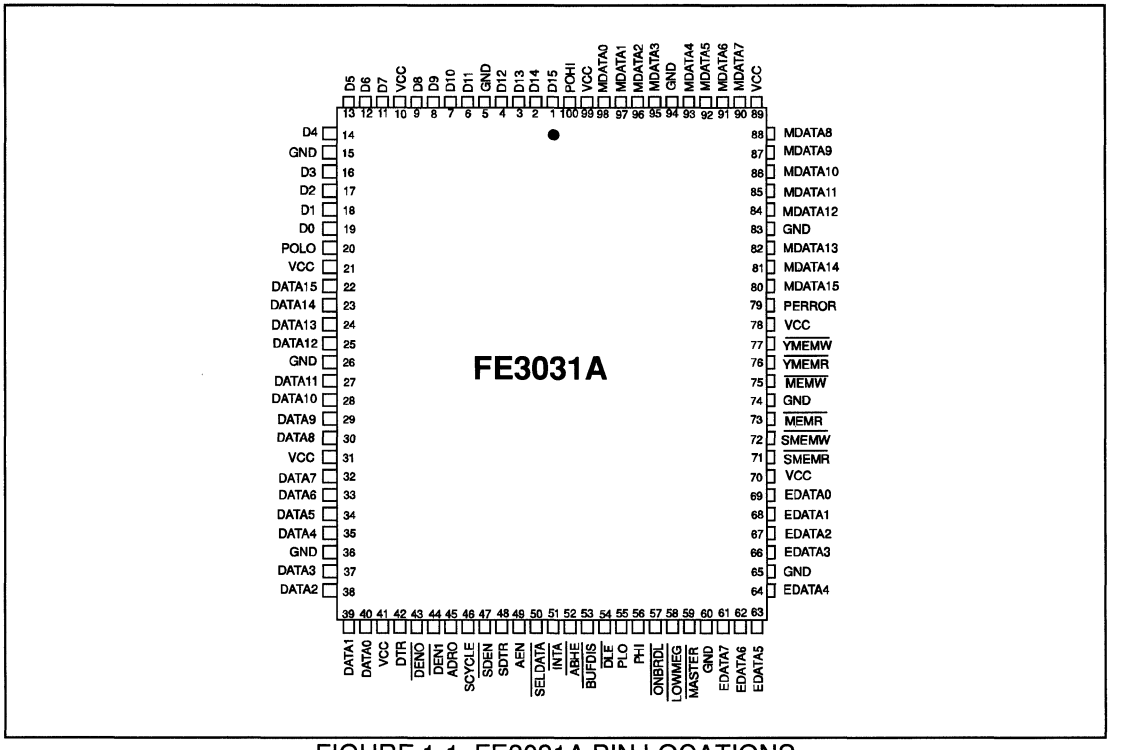


FIGURE 1-1. FE3031A PIN LOCATIONS

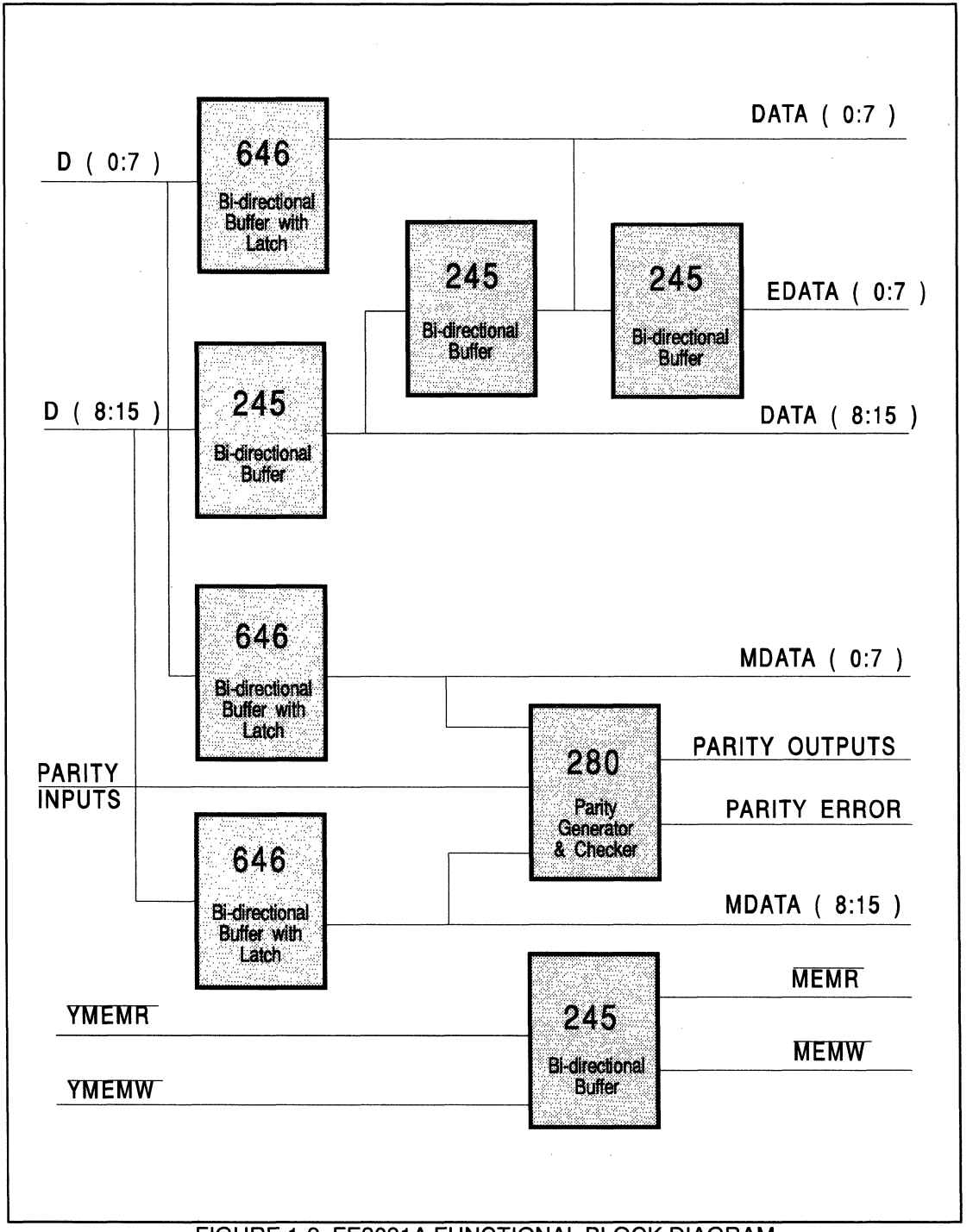


FIGURE 1-2. FE3031A FUNCTIONAL BLOCK DIAGRAM

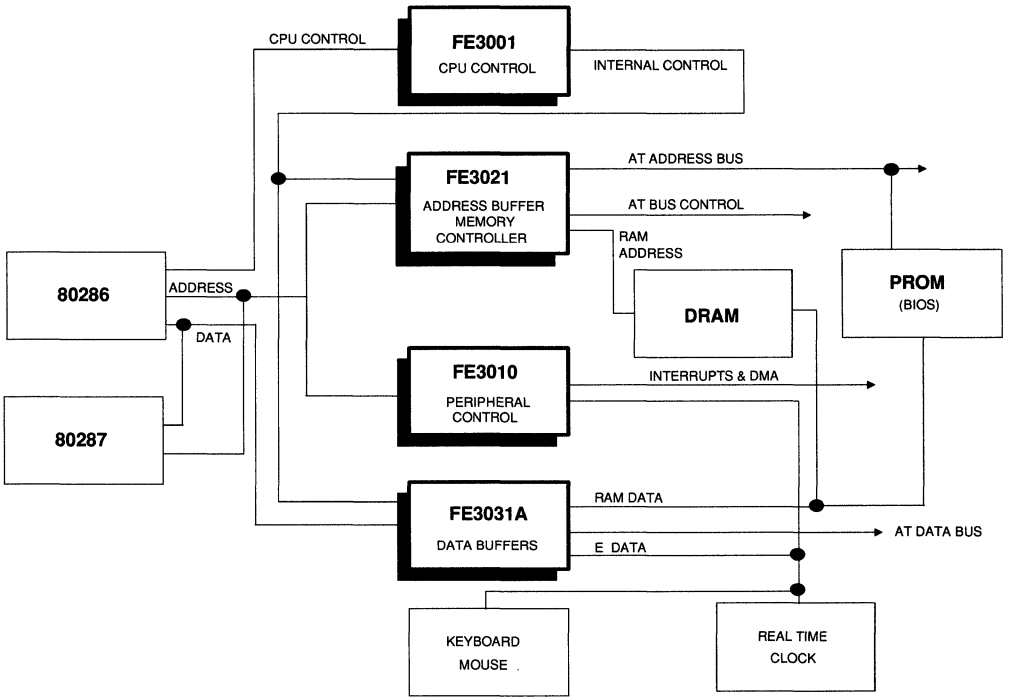


FIGURE 1-3. FE3600 B/C CHIP SET FUNCTIONAL BLOCK DIAGRAM

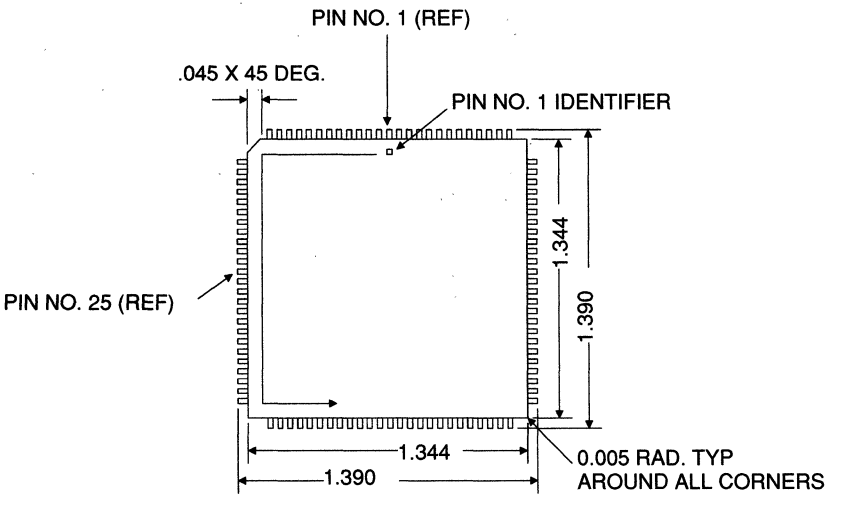
2.0 SIGNAL DESCRIPTIONS

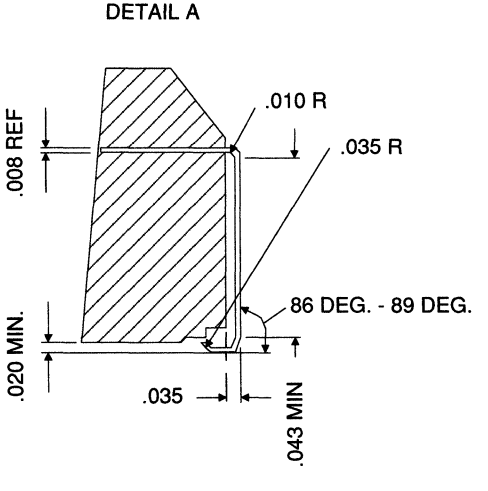
PIN#	SYMBOL	TYPE	FUNCTION
1-4 6-9 11-14 16-19	D(0:15)	I/O	80286 Local Data Bus
5,15 26,36 60,65 74,83 94	V_{SS}		Ground
10,21 31,41 70,78 89,99	V_{DD}		+5V V_{DD}
20	POLO	O	Low byte parity bit to the DRAMs
22-25 27-30 32-35 37-40	DATA (0:15)	I/O	PC/AT Data Bus
42	DTR	I	Data direction for DATA buffers
43	$\overline{\text{DEN0}}$	I	Low byte data enable to DATA buffers
44	$\overline{\text{DEN1}}$	I	High byte data enable to DATA buffers
45	ADR0	I	Address bit 0 for MDATA buffers and byte swap
46	SCYCLE	I	Latch low byte during byte swap read
47	$\overline{\text{SDEN}}$	I	Byte swap data buffer enable
48	SDTR	I	Byte swap data direction to swap buffer
49	ACK	I	DMA Acknowledge signal to the PC/AT bus
50	$\overline{\text{SELDATA}}$	I	EDATA bus enable
51	$\overline{\text{INTA}}$	I	Interrupt acknowledge
52	$\overline{\text{ABHE}}$	I	High byte enable for MDATA bus
53	$\overline{\text{BUFDIS}}$	I	Disable Buffers when low
54	$\overline{\text{DLE}}$	I	Latch MDATA bus during a read
55	PLO	I	Low byte parity bit from DRAMs
56	PHI	I	High byte parity bit from DRAMs
57	$\overline{\text{ONBRD16}}$	I	$\overline{\text{ONBRD}}$ indicates a local DRAM operation
58	$\overline{\text{LOWMEG}}$	I	$\overline{\text{LOWMEG}}$ indicates access of low Mbyte of memory
59	$\overline{\text{MASTER}}$	I	Master on PC bus has control of the bus

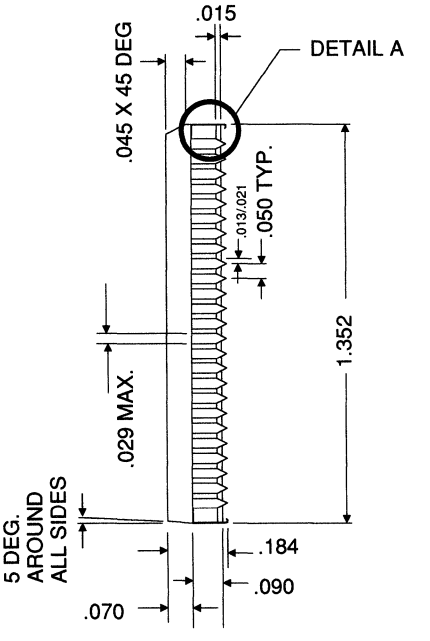
TABLE 2-1. FE3031A PIN ASSIGNMENT INFORMATION

PIN#	SYMBOL	TYPE	FUNCTION
61-64 66-69	EDATA (0:7)	I/O	Peripheral Data Bus for FE3001, FE3010B, RTC and Keyboard controller
71	$\overline{\text{SMEMR}}$	O	Low 1 MB Memory Read to PC bus
72	$\overline{\text{SMEMW}}$	O	Low 1 MB Memory Write to PC bus
73	$\overline{\text{MEMR}}$	I/O	Memory read to/from AT bus
75	$\overline{\text{MEMW}}$	I/O	Memory read to/from AT bus
76	$\overline{\text{YMEMR}}$	I/O	Memory read to/from FE3001
77	$\overline{\text{YMEMW}}$	I/O	Memory write to/from FE3001
79	PERROR	O	RAM parity error
80-82 84-88 90-93 95-98	MDATA (0:15)	I/O	Memory Data bus
100	POHI	O	High byte parity bit to the DRAMs

TABLE 2-1. FE3031A PIN ASSIGNMENT INFORMATION, Continued







NOTE:
ALL DIMENSIONS
ARE IN MILLIMETERS

FIGURE 2-1. 100-PIN PLCC PACKAGING DIAGRAM

3.0 PC/AT DATA BUS CYCLES

This description of the data bus cycles of the FE3600B/C PC AT expansion bus includes CPU, DMA, and MASTER cycles. The data portion of the PC AT expansion bus is a 16-bit wide bus divided into two bytes. In general, the low byte (DATA[0:7]) is accessed during cycles in which the address is even. The high byte (DATA[8:15]) is accessed when the address is odd. During 16-bit operations, both low and high bytes are accessed. There are several combinations of byte wide, word wide, even and odd addressing. Each of these combinations present a unique pattern of bus buffer enables and directions. These data buffer control states are described in this document.

NOTES:

Eight bit devices on the PC AT bus are always on the low byte (DATA[0:7]) of the expansion bus regardless of address. Sixteen bit devices use ADR0 and $\overline{EBHE}$ to distinguish between high and low byte transfers.

In previous ATdesigns, the data buffers on the PC AT were inactive during DMA. This was due to the on-board DRAM being on the system bus. Now that the DRAM is on the CPU local bus the data buffers must be enabled and directed during DMA operations.

A block diagram of the data bus hardware on the PC AT board is shown in Figure 3-1. It represents the equivalent 74LSXXX circuitry for the data buffers contained on the board. Signals used in this document are discussed in Table 9-1.

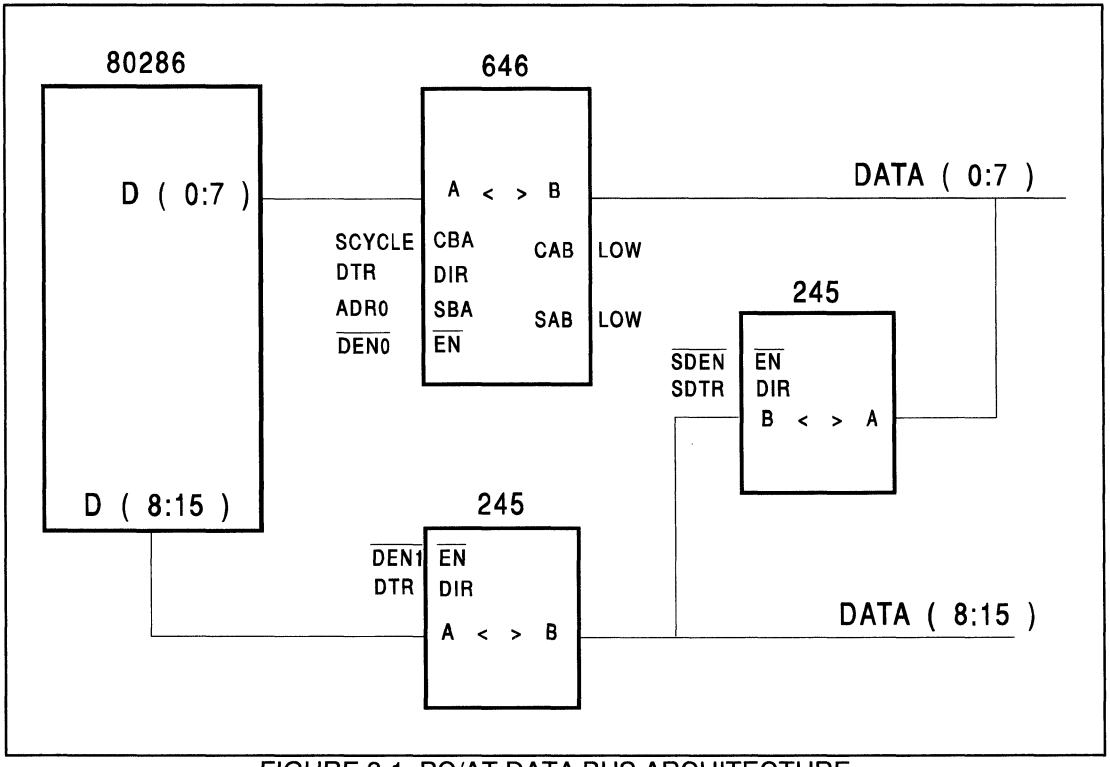


FIGURE 3-1. PC/AT DATA BUS ARCHITECTURE

'646				
EN DEN0	**DIR DTR**	**CBA SCYCLE**	**SBA ADR0**	**OPERATION**
X	X	X	X	LATCH B DATA
0	0	X	0	A <------B (REAL TIME)
0	0	X	1	A <------B (LATCHED DATA)
0	1	X	X	A ------>B (REAL TIME)
1	X	X	X	BUFFERS DISABLED

'245	
DIR	**OPERATION**
0	A <---------- B
1	A ----------> B

COMMAND SIGNALS	DEFINITIONS
S0, S1	BUS CYCLE STATUS FROM 286
$\overline{\text{MEMR}}$	SYSTEM MEMORY READ
$\overline{\text{MEMW}}$	SYSTEM MEMORY WRITE
$\overline{\text{IOR}}$	SYSTEM I/O READ
$\overline{\text{IOW}}$	SYSTEM I/O WRITE
$\overline{\text{NPCS}}$	NUMERIC PROCESSOR CHIP SELECT
A0	ADDRESS BIT 0 FROM 286
$\overline{\text{BHE}}$	BUS HIGH ENABLE FROM 286
HLDA	HOLD ACKNOWLEDGE FROM 286
HLDA1	DMA HOLD ACKNOWLEDGE FROM DMA CONTROLLER
$\overline{\text{PROMSL}}$	BIOS DECODE FROM MEMORY/IO DECODER
$\overline{\text{ONBRD}}$	ON BOARD DRAM OR I/O DECODE
$\overline{\text{IOCS16}}$	16-BIT I/O DEVICE DECODE FROM EXPANSION BUS
$\overline{\text{MEMCS16}}$	16-BIT MEMORY DEVICE DECODE FROM EXPANSION BUS
$\overline{\text{MASTER}}$	BUS CONTROL SIGNAL FROM BUS MASTER
DTR	DATA TRANSMIT/RECEIVE
$\overline{\text{DEN0}}$	LOW BYTE DATA ENABLE
$\overline{\text{DEN1}}$	HIGH BYTE DATA ENABLE
$\overline{\text{SDEN}}$	BYTE SWAP BUFFER ENABLE
SCYCLE	LOW BYTE DATA LATCH
SDTR	BYTE SWAP BUFFER TRANSMIT/RECEIVE
ADR0	SYSTEM ADDRESS BIT 0

TABLE 3-1. SIGNAL DEFINITIONS

4.0 CPU CYCLES

The following cycles represent data cycles under CPU control for all devices excluding the on board DRAM and the 80287 Math Coprocessor. Since the 80287 and on-board DRAM are on the local bus, the data bus drivers for the expansion bus will be disabled. This is accomplished by setting DEN0, DEN1 and SDEN = 1 when ONBRD + /MNIO = 0 or NPCS = 0. Note that on-board I/O is indicated by ONBRD + MNIO = 0. On-board I/O devices are on the system bus.

The following cycles are described in this section:

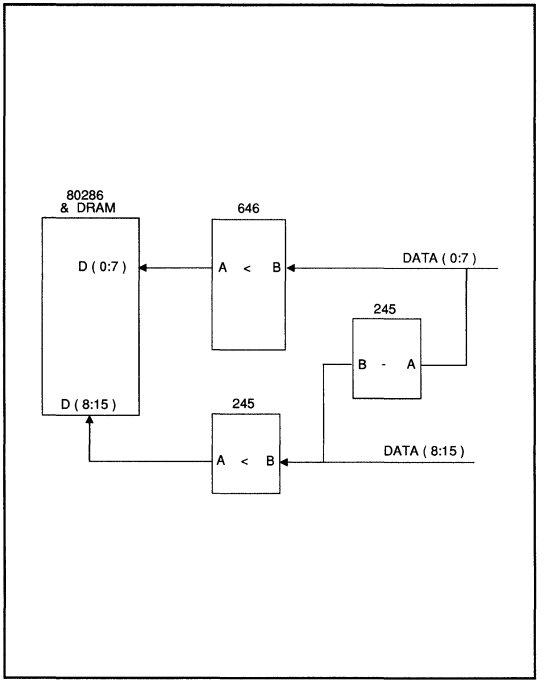
4.1 16-bit transfer, read from 16-bit device
4.2 16-bit transfer, write to 16-bit device
4.3 16-bit transfer, read from 8-bit device
4.4 16-bit transfer, write to 8-bit device
4.5 8-bit transfer, low byte read from 8 or 16-bit device
4.6 8-bit transfer, low byte write to 8 or 16-bit device
4.7 8-bit transfer, high byte read from 8-bit device
4.8 8-bit transfer, high byte write to 8-bit device
4.9 8-bit transfer, high byte read from 16-bit device
4.10 8-bit transfer, high byte write to 16-bit device

For all CPU cycles HLDA=0 and INTA- =1. In the following tables, CS16 indicates that there is a 16-bit device on the expansion bus. The boolean equation for CS16 is:

$$\overline{CS16} = (MNIO * \overline{NMEMCS16}) + (MNIO * \overline{NIOCS16}) + NPROMCS$$

7

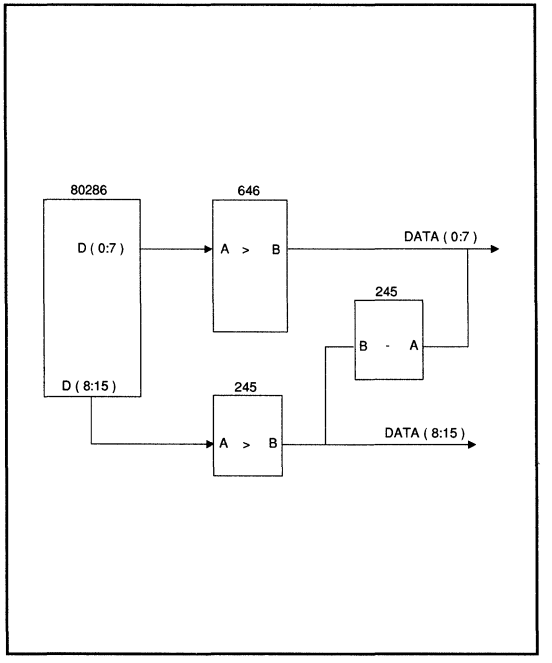
4.1 16-BIT READ FROM 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	0

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADRO	0

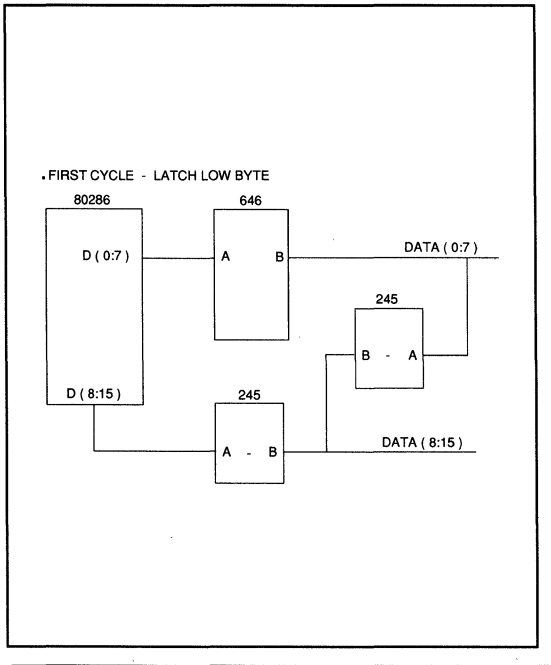
4.2 16-BIT WRITE TO 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	1
S0	0
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	0

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADRO	0

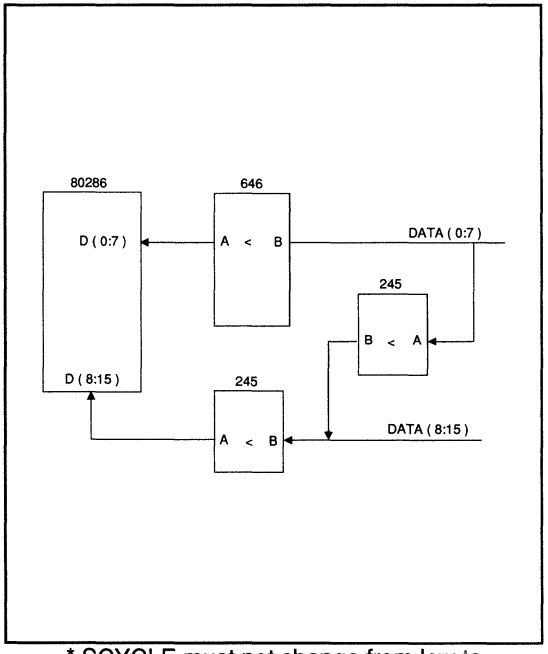
4.3 16-BIT READ FROM 8-BIT DEVICE



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	X
$\overline{DEN0}$	X
$\overline{DEN1}$	X
$\overline{SDEN}$	1
SCYCLE	^
SDTR	X
ADR0	0

* Second cycle - Enable latched low byte to 286 low byte and enable bus low byte to 286 or 386/SX high byte.



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	0
SCYCLE	X*
SDTR	1
ADRO	1

* SCYCLE must not change from low to high during the cycle.

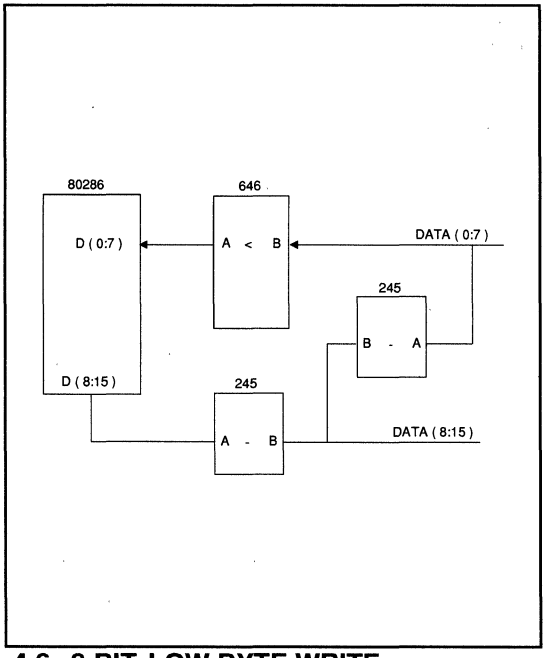
4.4 16-BIT WRITE TO 8-BIT DEVICE

INPUT SIGNALS	STATE
S1	1
S0	0
A0	0
$\overline{BHE}$	0
$\overline{CS16}$	1

- FIRST CYCLE
  - 8-bit, low byte write to 8-bit or 16-bit device
  - ADR0 is driven low during this cycle
  - $\overline{EBHE}$ is driven high during this cycle

- SECOND CYCLE
  - 8-bit, high byte write to 8-bit device
  - ADR0 is driven high during this cycle
  - $\overline{EBHE}$ is driven low during this cycle

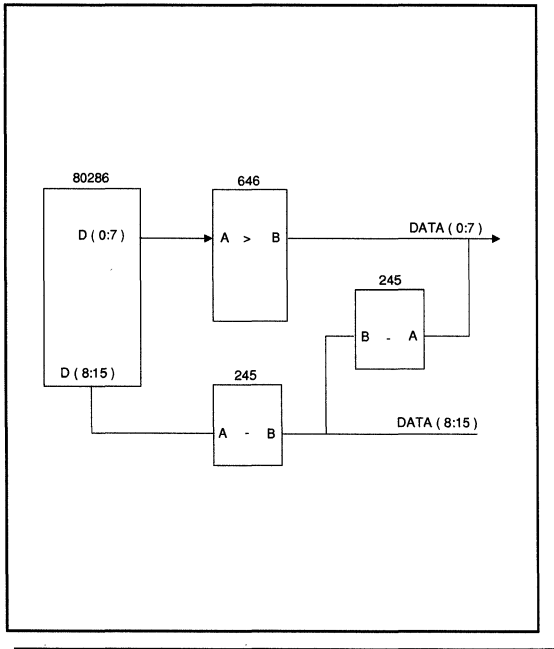
4.5 8-BIT, LOW BYTE READ FROM 8-BIT OR 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
$\overline{BHE}$	1
$\overline{CS16}$	X

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN1}$	1
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADR0	0

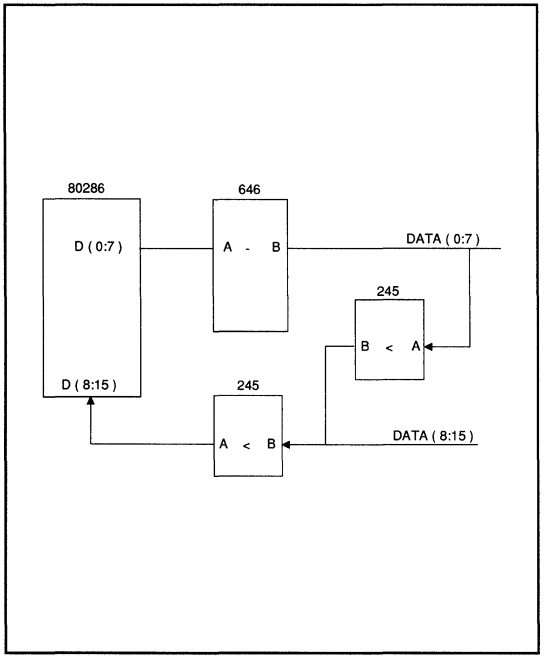
4.6 8-BIT, LOW BYTE WRITE TO 8-BIT OR 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	1
A0	0
$\overline{BHE}$	1
$\overline{CS16}$	X

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN1}$	1
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADR0	0

4.7 8-BIT, HIGH BYTE READ FROM 8-BIT DEVICE

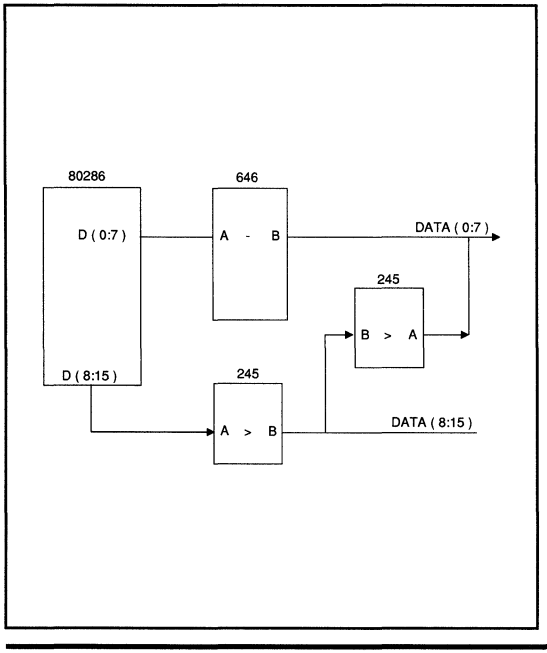


INPUT SIGNALS	STATE
S1	0
S0	1
A0	1
$\overline{BHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	0
SCYCLE	X
SDTR	1
ADR0	1

7

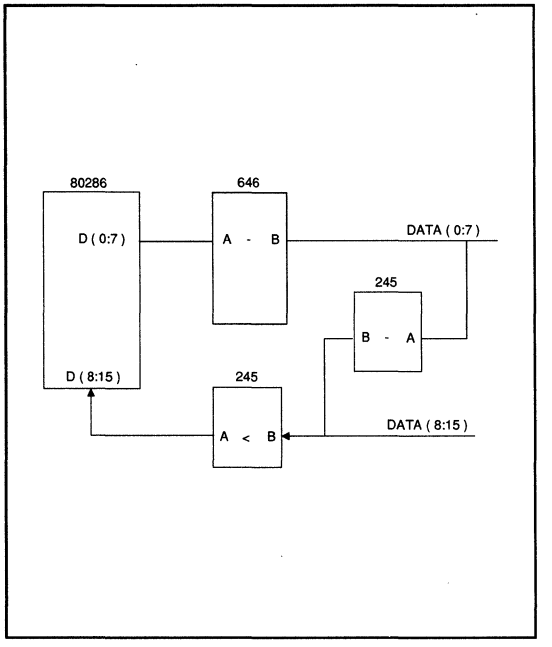
4.8 8-BIT, HIGH BYTE WRITE TO 8-BIT DEVICE



INPUT SIGNALS	STATE
S1	1
S0	0
A0	1
$\overline{BHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	0
SCYCLE	X
SDTR	0
ADR0	1

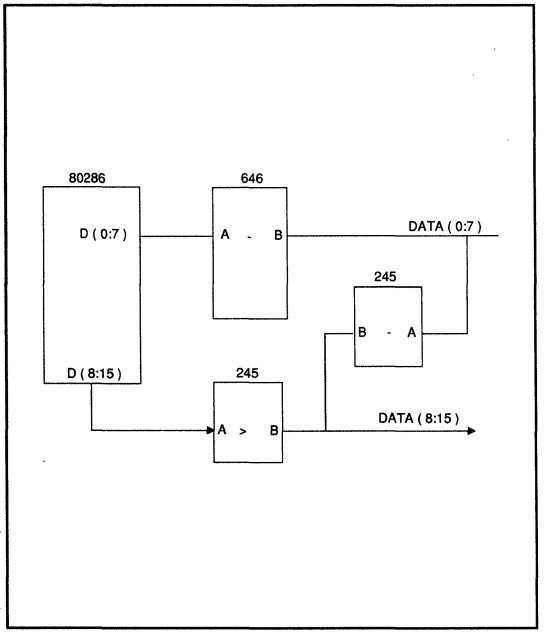
4.9 8-BIT, HIGH BYTE READ FROM 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	0
S0	1
A0	1
$\overline{BHE}$	0
$\overline{CS16}$	0

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADR0	1

4.10 8-BIT, HIGH BYTE WRITE TO 16-BIT DEVICE



INPUT SIGNALS	STATE
S1	1
S0	0
A0	1
$\overline{BHE}$	0
$\overline{CS16}$	0

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X
ADR0	1

5.0 DMA CYCLES

The following cycles represent data cycles under DMA control for all devices. DMA may be for on board DRAM ($\overline{ONBRD}$ =0) or system memory ($\overline{ONBRD}$ =1). Note that $\overline{ONBRD}$ decode for on-board I/O will be disabled during DMA.

The following DMA cycles are described in this section.

- For on board DRAM ($\overline{ONBRD}$ = 0)

5.1 8-bit DMA from even memory address to 8-bit I/O device.
5.2 8-bit DMA to even memory address from 8-bit I/O device.
5.3 8-bit DMA from odd memory address to 8-bit I/O device.
5.4 8-bit DMA to odd memory address from 8-bit I/O device.
5.5 16-bit DMA from memory to 16-bit I/O.
5.6 16-bit DMA to memory from 16-bit I/O.

- For system memory ($\overline{ONBRD}$ = 1)

5.7 8-bit DMA from 16-bit memory, odd address to 8-bit I/O device.
5.8 8-bit DMA to 16-bit memory, odd address from 8-bit I/O device.

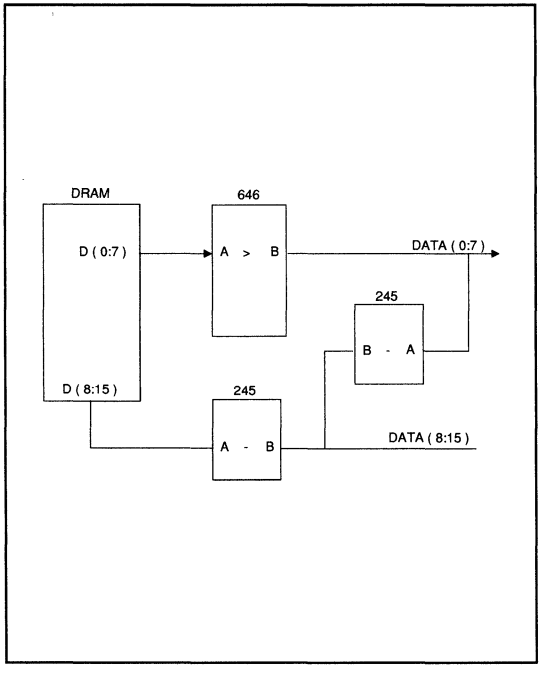
- For all other DMA cycles the data buffers are disabled.

5.9 All other DMA cycles.

For all DMA cycles HLDA=1, HLDA1=1 and $\overline{MASTER}$ =1.

7

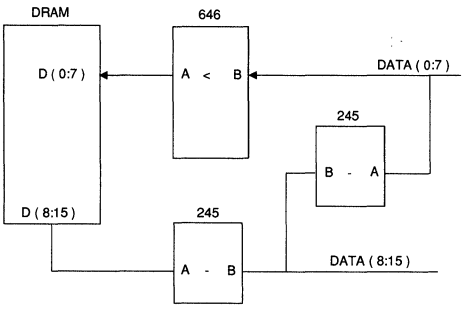
5.1 8-BIT DMA TRANSFER FROM EVEN MEMORY ADDRESS TOI 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{DMAMR}$	0
$\overline{MEMW}$	1
$\overline{IOR}$	1
$\overline{IOW}$	0
ADR0	0
$\overline{EBHE}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	0
$\overline{DEN1}$	1
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

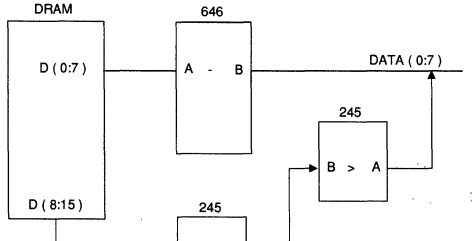
5.2 8-BIT DMA TRANSFER TO EVEN MEMORY ADDRESS FROM 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	1
$\overline{\text{MEMW}}$	0
$\overline{\text{IOR}}$	0
$\overline{\text{IOW}}$	1
ADR0	0
$\overline{\text{EBHE}}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{\text{DEN0}}$	0
$\overline{\text{DEN1}}$	1
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

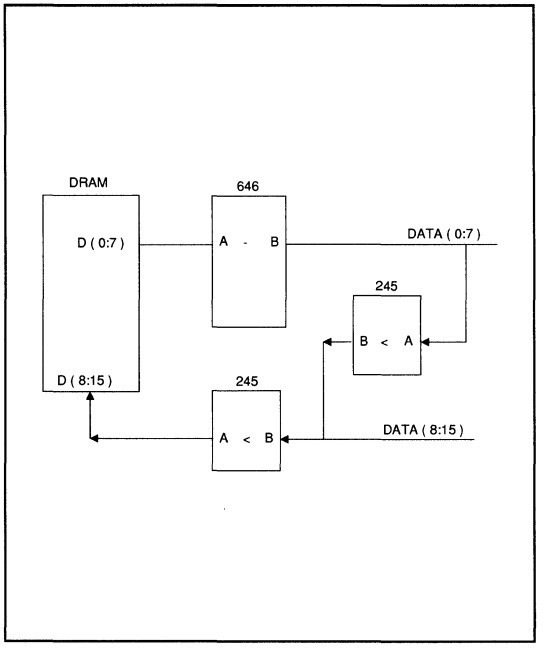
5.3 8-BIT DMA TRANSFER FROM ODD MEMORY ADDRESS TO 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	0
$\overline{\text{MEMW}}$	1
$\overline{\text{IOR}}$	1
$\overline{\text{IOW}}$	0
ADR0	1
$\overline{\text{EBHE}}$	0

CONTROL SIGNALS	STATE
DTR	1
$\overline{\text{DEN0}}$	1
$\overline{\text{DEN1}}$	0
$\overline{\text{SDEN}}$	0
SCYCLE	X
SDTR	0

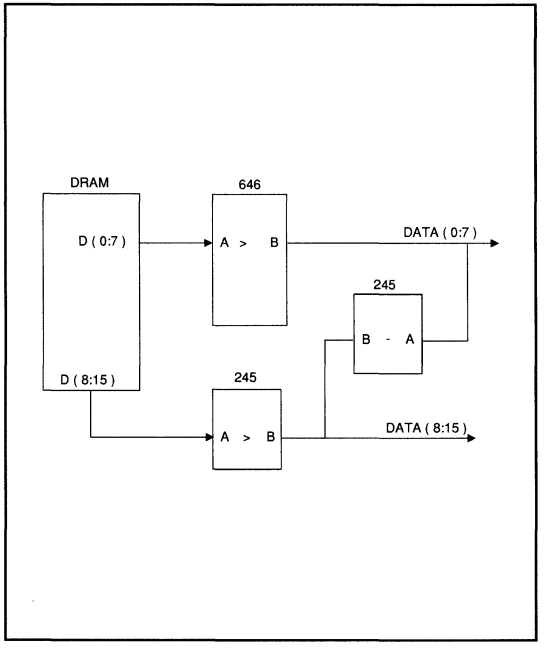
5.4 8-BIT DMA TRANSFER TO ODD MEMORY ADDRESS FROM 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	1
$\overline{\text{MEMW}}$	0
$\overline{\text{IOR}}$	0
$\overline{\text{IOW}}$	1
ADR0	1
$\overline{\text{EBHE}}$	0

CONTROL SIGNALS	STATE
DTR	0
$\overline{\text{DEN0}}$	1
$\overline{\text{DEN1}}$	0
$\overline{\text{SDEN}}$	0
SCYCLE	X
SDTR	1

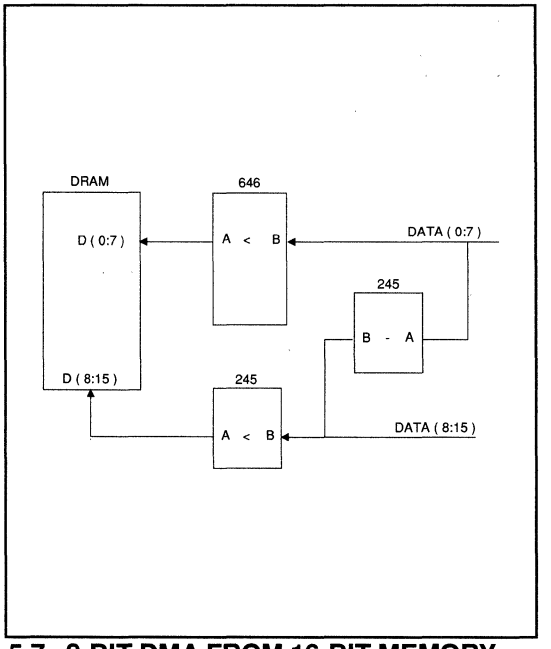
5.5 16-BIT DMA TRANSFER FROM MEMORY TO 16-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	0
$\overline{\text{MEMW}}$	1
$\overline{\text{IOR}}$	1
$\overline{\text{IOW}}$	0
ADR0	0
$\overline{\text{EBHE}}$	0

CONTROL SIGNALS	STATE
DTR	1
$\overline{\text{DEN0}}$	0
$\overline{\text{DEN1}}$	0
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

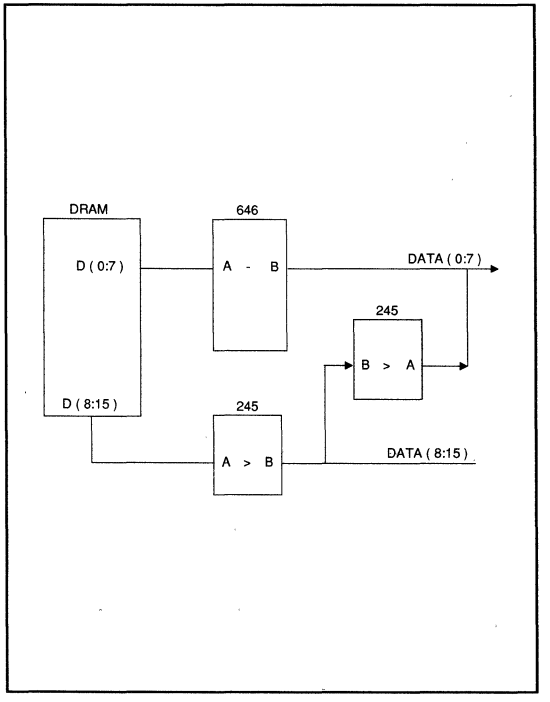
5.6 16-BIT DMA TRANSFER TO MEMORY FROM 16-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{DMAMR}$	1
$\overline{MEMW}$	0
$\overline{IOR}$	0
$\overline{IOW}$	1
ADR0	0
$\overline{EBHE}$	0

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

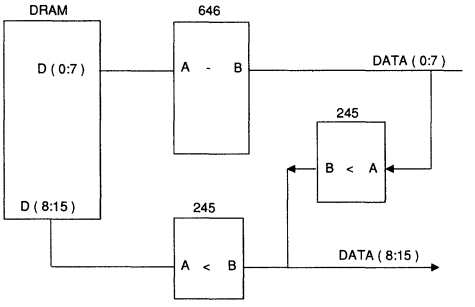
5.7 8-BIT DMA FROM 16-BIT MEMORY, ODD ADDRESS TO 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{DMAMR}$	0
$\overline{MEMW}$	1
$\overline{IOR}$	1
$\overline{IOW}$	0
ADR0	1
$\overline{EBHE}$	0
$\overline{MEMCS16}$ * $\overline{PROMSL}$	0

CONTROL SIGNALS	STATE
DTR	X
$\overline{DEN0}$	1
$\overline{DEN1}$	1
$\overline{SDEN}$	0
SCYCLE	X
SDTR	0

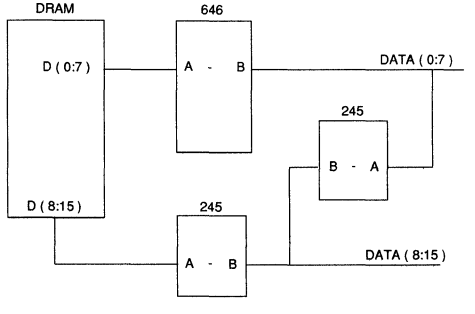
5.8 8-BIT DMA TO 16-BIT MEMORY, ODD ADDRESS FROM 8-BIT I/O DEVICE



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	1
$\overline{\text{MEMW}}$	0
$\overline{\text{IOR}}$	0
$\overline{\text{IOW}}$	1
ADR0	1
$\overline{\text{EBHE}}$	0
$\overline{\text{MEMCS16}}$ * $\overline{\text{PROMSL}}$	0

CONTROL SIGNALS	STATE
DTR	X
$\overline{\text{DEN0}}$	1
$\overline{\text{DEN1}}$	1
$\overline{\text{SDEN}}$	0
SCYCLE	X
SDTR	1

5.9 ALL OTHER DMA CYCLES (DATA BUFFERS DISABLED)



INPUT SIGNALS	STATE
$\overline{\text{DMAMR}}$	
$\overline{\text{MEMW}}$	
$\overline{\text{IOR}}$	
$\overline{\text{IOW}}$	
ADR0	
$\overline{\text{EBHE}}$	0

CONTROL SIGNALS	STATE
DTR	X
$\overline{\text{DEN0}}$	1
$\overline{\text{DEN1}}$	1
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

6.0 BUS MASTER CYCLES

The following cycles represent data cycles under the control of a bus master other than the 80286 or DMA controller. This condition is indicated by hold acknowledge active (HLDA=1) and bus master asserted ($\overline{\text{MASTER}}$ = 0). It is assumed that the bus master is always a 16-bit device. On-board DRAM and on-board I/O are distinguished by the memory or I/O read/write commands.

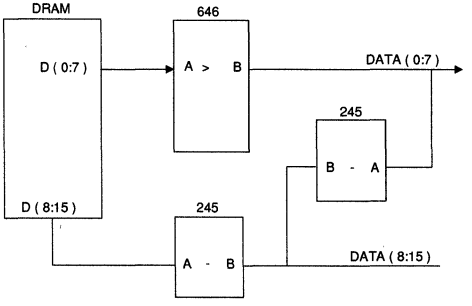
- ❑ For on-board DRAM

6.1 8-bit transfer low byte read from memory
6.2 8-bit transfer low byte write to memory
6.3 8-bit transfer high byte read from memory
6.4 8-bit transfer high byte write to memory
6.5 16-bit transfer read from memory
6.6 16-bit transfer write to memory

- ❑ For system memory and I/O

6.7 8-bit transfer high byte read from 8-bit system memory or I/O
6.8 8-bit transfer high byte write to 8-bit system memory or I/O

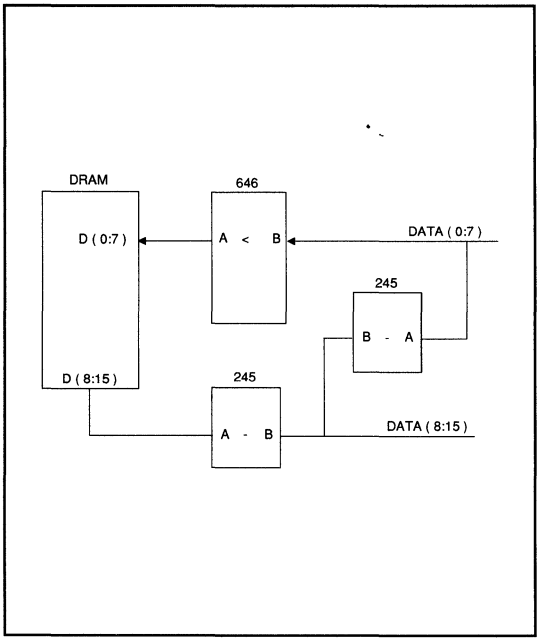
6.1 8-BIT BYTE READ FROM MEMORY



INPUT SIGNALS	STATE
$\overline{\text{MEMR}}$	0
$\overline{\text{MEMW}}$	1
ADR0	0
$\overline{\text{EBHE}}$	1
$\overline{\text{CS16}}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{\text{DEN0}}$	0
$\overline{\text{DEN1}}$	1
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

6.2 8-BIT LOW BYTE WRITE TO MEMORY

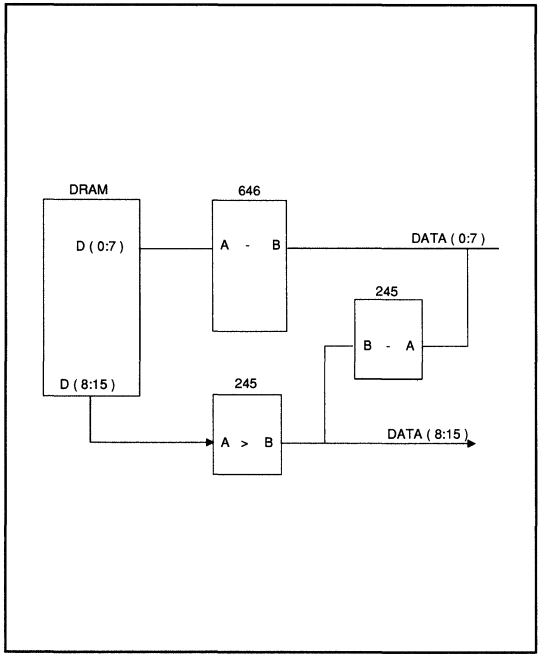


INPUT SIGNALS	STATE
$\overline{\text{MEMR}}$	1
$\overline{\text{MEMW}}$	0
ADR0	0
$\overline{\text{EBHE}}$	1
$\overline{\text{CS16}}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{\text{DEN0}}$	0
$\overline{\text{DEN1}}$	1
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

7

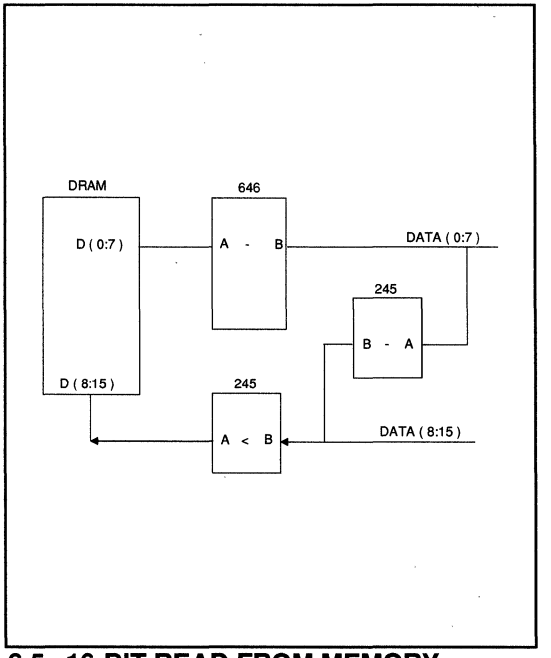
6.3 8-BIT HIGH BYTE READ FROM MEMORY



INPUT SIGNALS	STATE
$\overline{\text{MEMR}}$	0
$\overline{\text{MEMW}}$	1
ADR0	1
$\overline{\text{EBHE}}$	0
$\overline{\text{CS16}}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{\text{DEN0}}$	1
$\overline{\text{DEN1}}$	0
$\overline{\text{SDEN}}$	1
SCYCLE	X
SDTR	X

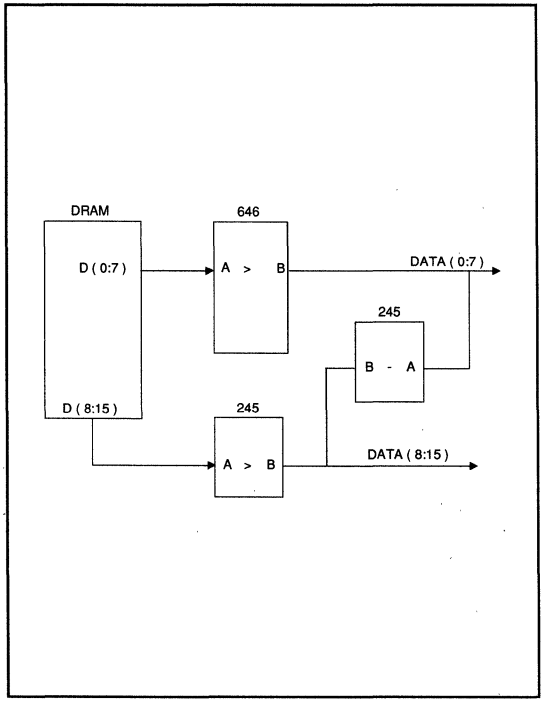
6.4 8-BIT HIGH BYTE WRITE TO MEMORY



INPUT SIGNALS	STATE
$\overline{MEMR}$	1
$\overline{MEMW}$	0
ADR0	1
$\overline{EBHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	1
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

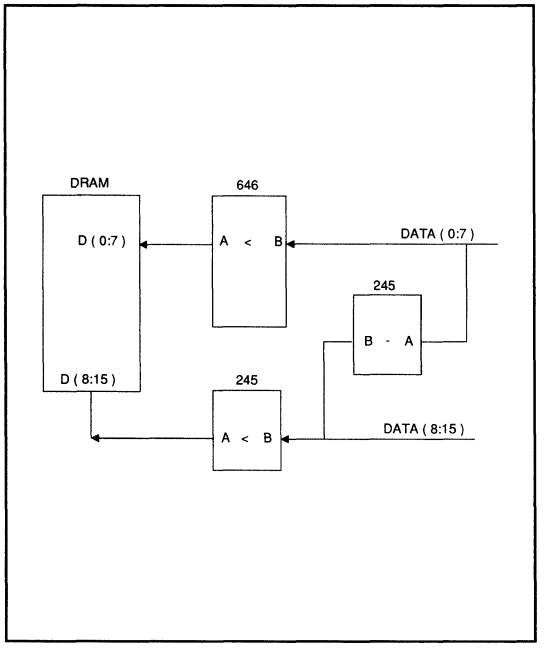
6.5 16-BIT READ FROM MEMORY



INPUT SIGNALS	STATE
$\overline{MEMR}$	0
$\overline{MEMW}$	1
ADR0	0
$\overline{EBHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	1
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

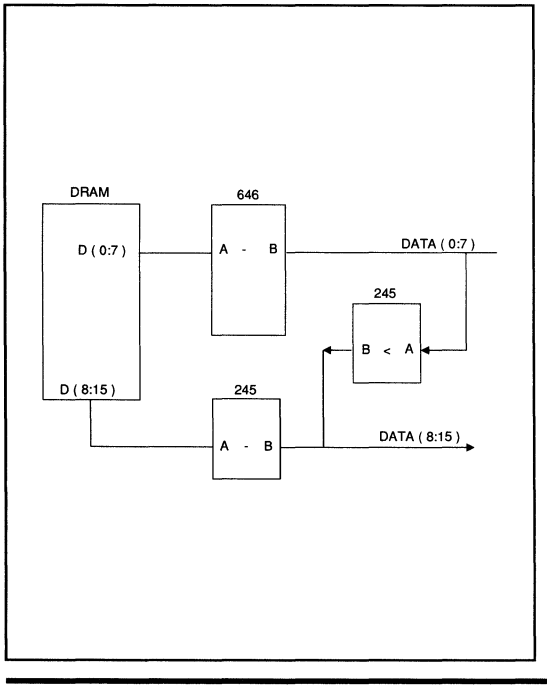
6.6 16-BIT WRITE TO MEMORY



INPUT SIGNALS	STATE
$\overline{MEMR}$	1
$\overline{MEMW}$	0
ADR0	0
$\overline{EBHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	0
$\overline{DEN0}$	0
$\overline{DEN0}$	0
$\overline{DEN1}$	0
$\overline{SDEN}$	1
SCYCLE	X
SDTR	X

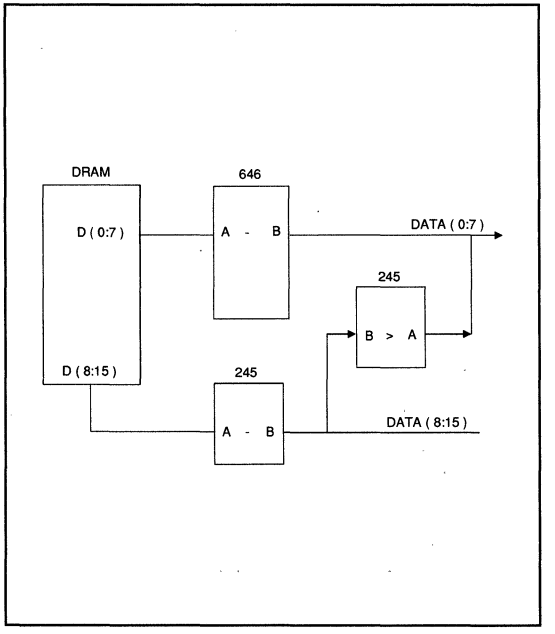
6.7 8-BIT HIGH BYTE READ FROM 8-BIT DEVICE



INPUT SIGNALS	STATE
$\overline{MEMR}$ * $\overline{IOR}$	0
$\overline{MEMW}$ * $\overline{IOW}$	1
ADR0	1
$\overline{EBHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	X
$\overline{DEN0}$	1
$\overline{DEN1}$	1
$\overline{SDEN}$	0
SCYCLE	X
SDTR	1

6.8 8-BIT HIGH BYTE WRITE TO 8-BIT DEVICE



INPUT SIGNALS	STATE
$\overline{MEMR}$ * $\overline{IOR}$	1
$\overline{MEMW}$ * $\overline{IOW}$	0
ADR0	1
$\overline{EBHE}$	0
$\overline{CS16}$	1

CONTROL SIGNALS	STATE
DTR	X
$\overline{DEN0}$	1
$\overline{DEN1}$	1
$\overline{SDEN}$	0
SCYCLE	X
SDTR	0

7.0 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature (operating) . . . . . .0° to +70°C
Storage Temperature . . . . . .40° to +125°C
Voltage on any pin to ground . . . . . .+7V
Power Dissipation . . . . . .400 mW

8.0 DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{IL}	Input LOW Voltage		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V	
I_{OL}	LOW V Output Current[1]		4	m	V_{OL} = 0.4V
I_{OH}	HIGH V Output Current[1]		-4	mA	V_{OH} = 2.4V
I_{OL}	LOW V Output Current[2]		6.4	mA	V_{OL} = 0.4V
I_{OH}	HIGH V Output Current[2]		-6.4	mA	V_{OH} = 2.4V
.V_{DD}	Supply Voltage	4.75	5.25	V	

TABLE 8-1. DC CHARACTERISTICS

7

Notes:
1. Output currents are for D(0:15), EDATA(0:7), $\overline{\text{MEMR}}$, $\overline{\text{YMEMW}}$, PERROR
2. Output currents are for DATA(0:15), MDATA(0:15), $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$, POLO, PHI

9.0 AC CHARACTERISTICS

SIGNAL PATH		PROP DLY (MAX)[1] 16 MHz	20 MHz	UNIT	NOTES
D(0:7) from	DATA (0:7)	22	22	ns	
	MDATA (0:7)	20	20	ns	
	ADR0	30	30	ns	
	BUFDIS	30	30	ns	
	ONBRD16	30	30	ns	1
	YMEMR	30	30	ns	
	DEN0	30	30	ns	
	DATA (8:15)	40	40	ns	
	EDATA (0:7)	40	40	ns	
	NSDEN	50	50	ns	
	SDTR	50	50	ns	
D(8:15) from	DATA (8:15)	22	22	ns	
	MDATA (8:15)	20	20	ns	
	ABHE	30	30	ns	
	BUFDIS	30	30	ns	
	ONBRD16	30	30	ns	
	YMEMR	30	30	ns	1
	DEN1	30	30	ns	
	DATA (0:7)	40	40	ns	
	EDATA (0:7)	40	40	ns	
	NSOEN	50	50	ns	
	NSDEN	50	50	ns	
DATA (0:7) from	D(0:7)	22	22	ns	
	D(8:15)	40	40	ns	
	DATA(8:15)	22	22	ns	
	EDATA(0:7)	22	22	ns	
	SDEN	30	30	ns	
	DEN0	30	30	ns	
	INTA	30	30	ns	1,2
	SELDATA	30	30	ns	
	MDATA(0:7)	40	40	ns	
	MDATA(8:15)	60	60	ns	
	SDTR	30	30	ns	
	NSDEN	30	30	ns	
Setup Time from	SCYCLE	07	07	ns	
Hold Time from	SCYCLE	05	05	ns	
DATA (8:15) from	D (8:15)	22	22	ns	
	DATA (0:7)	22	22	ns	
	DEN1	30	30	ns	1,2
	MDATA(8:15)	40	40	ns	

TABLE 9-1. AC CHARACTERISTICS

SIGNAL PATH		PROP DLY (MAX)1 16 MHz	20 MHz	UNIT	NOTES
DATA(8:15) continued					
	NSDEN	30	30	ns	1,2
	SDTR	30	30	ns	
EDATA (0:7) from	DATA(0:7)	36	36	ns	
	D(0:7)	36	36	ns	
	D (8:15)	36	36	ns	
	INTA	40	40	ns	1
	SELDATA	40	40	ns	
	NSDEN	40	40	ns	
	SDTR	40	40	ns	
YMEMW from	MEMW	33	33	ns	
	MASTER	40	40	ns	
YMEMR from	MEMR	33	33	ns	1
	MASTER	40	40	ns	
MEMW from	YMEMW	20	20	ns	
	MASTER	30	30	ns	1
	ONBRD16	30	30	ns	
MEMR from	YMEMW	20	20	ns	
	MASTER	30	30	ns	1
	ONBRD16	30	30	ns	
SMEMW from	YMEMW	20	20	ns	
	MASTER	30	30	ns	1
	ONBRD16	30	30	ns	
SMEMR from	YMEMW	20	20	ns	
	MASTER	30	30	ns	1
	ONBRD16	30	30	ns	
PERROR from	MDATA(0:15)	30	30	ns	
	PLO	40	40	ns	
	PHI	40	40	ns	1
	ADR0	40	40	ns	
	ABHE	40	40	ns	
POLO	from D(0:7)	19	19	ns	1
POHI	from D(8:15)	19	19	ns	1
MDATA (0:7) from	D (0:7)	18	18	ns	
	ADR0	27	27	ns	
	ONBRD16	30	25	ns	1
	YMEMR	30	30	ns	
	DLE	30	30	ns	
	DATA(0:7)	40	40	ns	
	DEN0	50	50	ns	

TABLE 9-1. AC CHARACTERISTICS, Continued

SIGNAL PATH	PROP DLY (MAX)1 16 MHz	20 MHz	UNIT	NOTES
MDATA(0:15)				
PL0, PH1 Setup Time from NDLE	05	05	ns	
PL0, PH1 Hold Time from NDLE	05	05	ns	
MDATA(8:15) from D(8:15)	18	18	ns	
ABHE	27	27	ns	
ONBRD16	30	25	ns	
YMEMR	30	30	ns	1
DATA(0:7)	40	40	ns	
DATA (8:15)	40	40	ns	
DLE	30	30	ns	

TABLE 9-1. AC CHARACTERISTICS, Continued

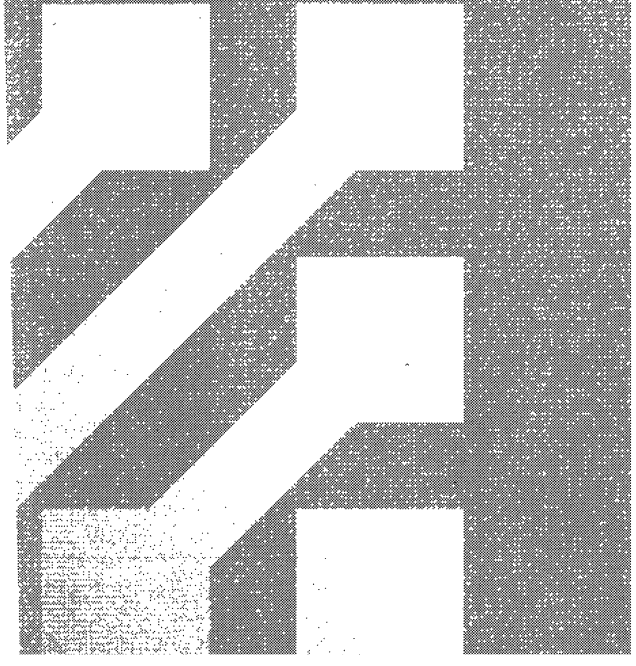
Notes:
1. Prop delays are for 75 pf load.
2. Add 8 ns for 200 pf load.

SYSTEMS LOGIC/PERIPHERAL

WD16C451, WD16C551

Enhanced Asynchronous Communications Element (ACE) with Parallel Port

8



WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

1.0 INTRODUCTION

1.1 DESCRIPTION

The low-power CMOS WD16C451/WD16C551 is a single-device solution for serving one serial I/O port and one bidirectional parallel port on the IBM PC, PC XT, PC AT, PS/2, and compatible systems. The WD16C451/WD16C551 is an enhanced ACE with a bidirectional parallel port. The ACE performs parallel-to-serial conversion on output and serial-to-parallel conversion on input. It is programmable, independent, and has a maximum recommended data rate of 512K baud.

The WD16C451 family (WD16C451, WD16C451A, WD16C451B) is a WD16C450 ACE plus a bidirectional parallel data port.

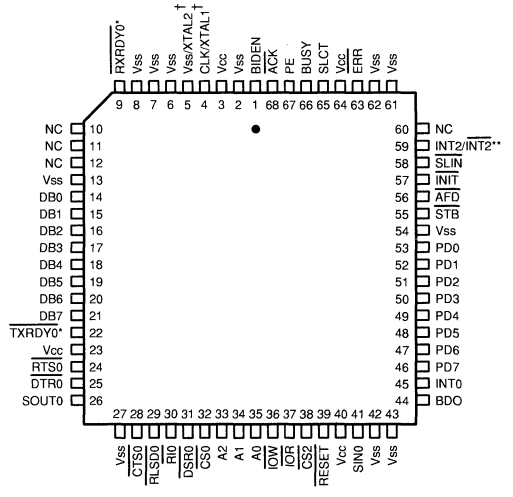
The WD16C451 and WD16C451A parallel port supports a Centronics-compatible printer interface. The parallel port, together with the serial port, provides IBM PC XT, PC AT and compatibles with a single-device solution for serving both ports. The WD16C451A is further enhanced by its crystal input capability.

The WD16C451B, also enhanced by its crystal input capability, supports a PS/2-compatible printer port interface. The parallel port, together with the serial port, provides IBM PS/2 and compatibles with a single-device solution for serving both ports.

The WD16C551 is a WD16C550 Enhanced ACE plus a compatible PS/2 bidirectional parallel port. After power-up and hardware reset, the ACE is functionally compatible with WD16C450 (Character Mode). The ACE in the WD16C551 has been enhanced with 16-byte FIFO buffers on both the receive and transmit lines, allowing an additional mode of operation called FIFO Mode. The FIFO Mode, only available in WD16C551, can be activated through software, relieving CPU of interrupt overhead. Buffering of data also allows greater latency time in interrupt servicing, which is vital in multitasking environments. The WD16C551 also has DMA signaling between the FIFO buffers and host CPU allowing single-character or multicharacter transfers. The recommended maximum data rate is 512 Kbaud with an 8.0 MHz clock rate. The PS/2 parallel port, together with the serial port, provides IBM PS/2 and compatibles with a single-device solution for servicing both ports.

1.2 FEATURES

- Fully programmable serial interface characteristics including:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no parity bit generation/detectio
  - 1, 1-1/2, or 2 stop-bit generation
  - DC to 512 Kbaud rate generation
- Tri-state TTL drive capabilities for bidirectional data bus and control bus
- Loopback controls for communications link fault isolation
- Line break generation and detection
- False start-bit detection



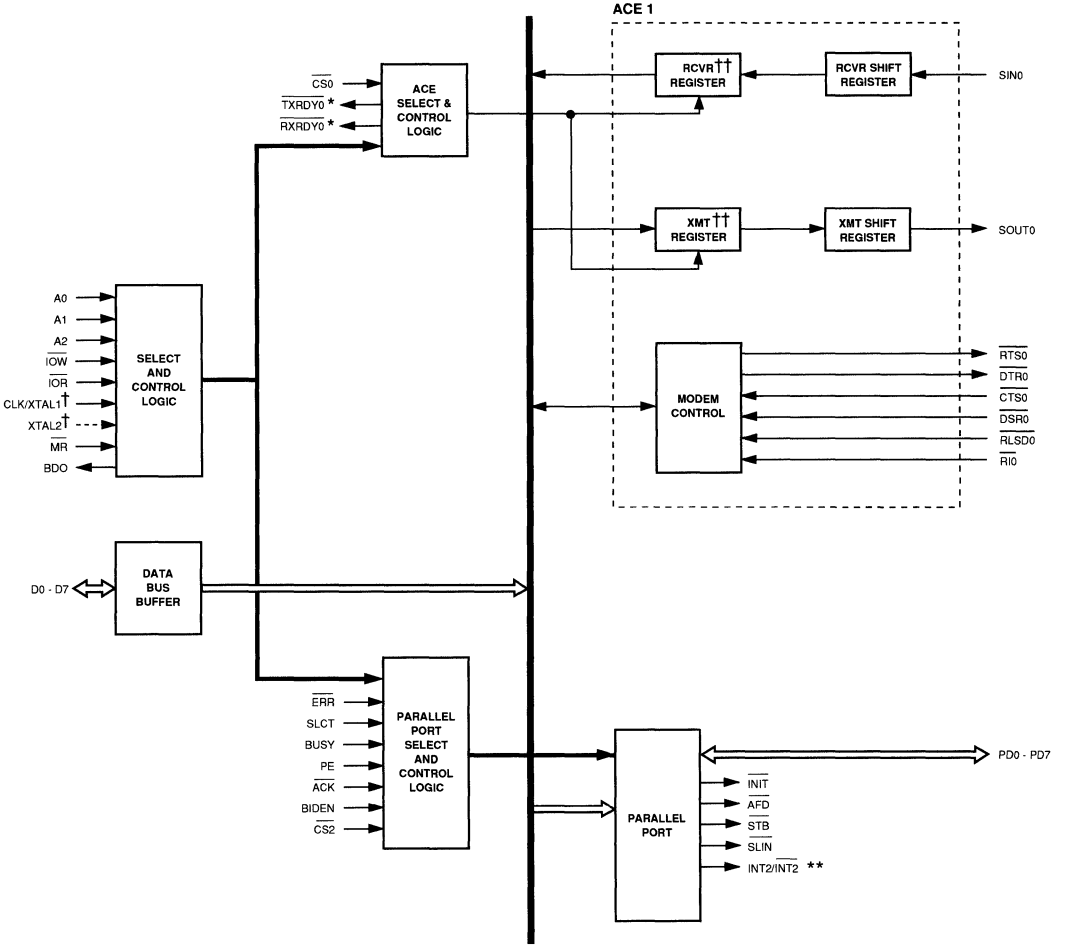
* INTERNAL NO CONNECTS FOR WD16C451/16C451A/16C451B, RXRDY0 (PIN 9) AND TXRDY0 (PIN 22) FOR WD16C551.
** INT2 FOR WD16C451/16C451A AND INT2 FOR WD16C551/16C451B.

Figure 1. 68-Pin Quad

- Complete status reporting capabilities
- Generation and stripping of serial asynchronous data control bits (start, stop, parity)
- Programmable baud rate generator and MODEM control signals
- Fully prioritized independent interrupt system controls
- CMOS implementation for high-speed, low-power requirements
- 68-pin QUAD package

AVAILABLE VERSIONS

- **WD16C451** with:
  - Centronics (PC/AT) compatible bidirectional parallel port for direct printer interface
- **WD16C451A** with:
  - Centronics (PC/AT) compatible bidirectional parallel port for direct printer interface
  - Crystal-controlled external clock input
- **WD16C451B** with:
  - PS/2-compatible bidirectional parallel port
  - Crystal-controlled external clock input
- **WD16C551** with:
  - PS/2-compatible bidirectional parallel port
  - 16-byte transmit and receive FIFO buffers for CPU relief during high-speed data transfer
  - Programmable 1-, 4-, 8-, or 14-byte FIFO threshold levels on each receive channel
  - Two modes of DMA signaling for transfer of data characters to and from FIFO buffers



(*) TXRDY0 and RXRDY0 for WD16C551 only.
(**) INT2 for WD16C451/16C451A, INT2 for WD16C551/16C451B.
(†) CLK for WD16C451/16C551, XTAL1 and XTAL2 for WD16C451A/16C451B.
(††) 16-byte FIFO buffers for WD16C551.

Figure 2. WD16C451/WD16C55A Block Diagram

2.0 SERIAL CHANNEL REGISTERS

2.1 SERIAL PORT REGISTER ADDRESSING

Chip Select ($\overline{CSO}$): When $\overline{CSO}$ is low, registers for the serial channel can be accessed.

Master Reset:
A low level input on this pin causes the ACE to reset to the condition listed in Table 3-1.

Software Reset:
A software reset is performed by writing to the Divisor Latches, forcing the transmitter and receiver to an Idle Mode. (Registers are not reset by this operation.) Prior to enabling interrupts, the LSR and RBR registers should be read to clear out any data. This is used to return to a known state without resetting the system.

Chip Select ($\overline{CSO}$) and register select (A0, A1, A2) signals must be stable for the duration of a read or write operation.

Register Select (A0, A1, A2): To select a register for read or write operation, see table 2-1

NOTE:
Divisor Latch Access Bit (DLAB) is the MSB of the Line Control Register. DLAB must be programmed high (logic 1) by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer Register (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable Register
X	0	1	0	Interrupt Identification Register (read only)
X	0	1	0	FIFO Control Register (write only)
X	0	1	1	Line Control Register
X	1	0	0	MODEM Control Register
X	1	0	1	Line Status Register (read only)
X	1	1	0	MODEM Status Register
X	1	1	1	Scratch Pad Register
1	0	0	0	Divisor Latch Register (least significant byte)
1	0	0	1	Divisor Latch Register (most significant byte)

Table 2-1. Register Addressing

3.0 ACE OPERATIONAL DESCRIPTION

3.1 MASTER RESET

A low-level input on this pin causes the ACE to reset to the condition listed in Table 3-1.

3.2 ACE ACCESSIBLE REGISTERS

The system programmer has access to any of the registers as summarized in Table 3-2. For individual register descriptions, refer to the following pages under register heading.

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-3; 6 and 7 are forced Low. Bits 4 and 5 are permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, except Bits 5 and 6 are High
MODEM Status Register	Master Reset	Bits 0-3 Low, Bits 4-7 at Input Signal
Divisor Latch (low order byte)	Writing into the Latch	Data
Divisor Latch (high order byte)	Writing into the Latch	Data
SOUT	Master Reset	High
BDO	BDO = $\overline{RCLK}$ • IOR (At Master Reset, the CPU sets RCLK and $\overline{IOR}$ = Low when device is selected.)	High
INT0 (RCVR ERRS)	Master Reset/Read LSR	Low
INT0 (RCVR DATA READY)	Master Reset/Read RBR	Low
INT2 (WD16C451/WD16C451A)	Master Reset/$\overline{ACK}$ (High)	Low
$\overline{INT2}$ (WD16C551/WD16C451B)	Master Reset/Read PPSR	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
RCVR FIFO Counter (WD16C551 Only)	MR or FCR1 • FCR0 or ΔFCR0	All Bits Low
$\overline{XMIT\ FIFO\ Counter}$ (WD16C551 only)	MR or FCR1 • FCR0 or $\overline{\Delta FCR0}$	All Bits Low
FIFO CONTROL (WD16C551 only)	Master Reset	All Bits Low
D7 - D0 Data Bus Lines	In Tri-state Mode, Unless $\overline{IOR}$ = Low or $\overline{IOW}$ = Low when Device is Selected	Tri-state Data (ACE to CPU) Data (CPU to ACE)

Table 3-1. Reset Control of Registers and Pinout Signals

Register Address						
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending (IP)	FIFO Enable (Write Only) (FEWO)	Word Length Select Bit 0 (WLS0)
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 0 (IIDB0)	Rcvr FIFO Reset (RFR)	Word Length Select Bit 1 (WLS1)
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ERLSI)	Interrupt ID Bit 2 (IIDB2)	Transmitter FIFO Reset (TFR)	Number of Stop Bits (STB)
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit 3 (IIDB3) ♦	DMA Mode Select (DMS)	Parity Enable (PEN)
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity (STP)
6	Data Bit 6	Data Bit 6	0	FIFO Enabled♦ (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (LSB)(RTLSB)	Set Break Control (SBR)
7	Data Bit 7	Data Bit 7	0	FIFO Enabled ♦ (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (MSB) (RTMSB)	Divisor Latch Access Bit (DLAB)
(♦) These bits are 0 in Character Mode.						

Table 3-2. Accessible WD16C451/WD16C551 Registers

	Register Address					
	4	5	6	7	0 DLAB=1	1 DLAB=1
Bit No.	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Pad Register	Divisor Latch (LSB)	Divisor Latch (MSB)
0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Not Connected (NC)	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Interrupt (Int)	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO (EIRF)	Received Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15
(♦) These bits are 0 in Character Mode.						

Table 3-2. Accessible WD16C451/WD16C551 Registers (Contd)

3.3 LINE CONTROL REGISTER

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 are as follows:

Bit 1	Bit 0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1-1/2 Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (Transmit data) or checked (Receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1's when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

3.4 ACE PROGRAMMABLE BAUD RATE GENERATOR

The ACE contains a programmable Baud Rate Generator capable of taking any clock input (dc to 8.0 MHz) and dividing it by any divisor from 1 to (2^{16} - 1). The output frequency of the Baud Generator is 16X the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3-3, 3-4, and 3-5 illustrate the use of the Baud Generator with three different driving frequencies. One is referenced to a 1.8432 MHz clock. Another is a 3.072 MHz clock. The third is an 8.0 MHz clock.

NOTE:
The maximum operating frequency of the Baud Generator is 8.0 MHz.

In no case should the data rate be greater than 512K baud.

Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	2304	--
75	1536	--
110	1047	0.026
134.5	857	0.058
150	768	--
300	384	--
600	192	--
1200	96	--
1800	64	--
2000	58	0.690
2400	48	--
3600	32	--
4800	24	--
7200	16	--
9600	12	--
19200	6	--
38400	3	--
56000	2	2.860

Table 3-3. Baud Rates Using 1.8432 MHz Clock

Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	3840	--
75	2560	--
110	1745	0.026
134.5	1428	0.034
150	1280	--
300	640	--
600	320	--
1200	160	--
1800	107	--
2000	96	--
2400	80	--
3600	53	0.628
4800	40	--
7200	27	1.230
9600	20	--
19200	10	--
38400	5	--
56000	3	14.285

Table 3-4. Baud Rates Using 3.072 MHz Clock

Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	10000	--
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	--
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.344

Table 3-5. Baud Rates Using 80.0 MHz Clock

3.5 LINE STATUS REGISTER

This 8-bit read only register provides status information to the CPU concerning the data transfer. Its contents are indicated in Table 3-2 and are described below.

Bit 0: This bit is the Receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register, or to the RCVR FIFO (when in FIFO Mode). Bit 0 will be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register (for Character Mode) or by writing a logic 0 into it from the CPU.

In FIFO Mode Receiver Data Ready is set when the receiver shift register is loaded into the FIFO and reset when the receiver FIFO is empty.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode an OE occurs after the RCVR FIFO is full and the receiver shift register has completely received the next character. An OE is indicated to the CPU as soon as it happens. The character in the shift register will be written over, but nothing will be transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to logic 0 whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode a parity error is associated with a particular character in the FIFO buffer, and revealed to the CPU when the associated character is in the top of the FIFO buffer.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop Bit. Bit 3 is set to a logic 1 whenever the Stop Bit following the last data bit or parity bit is detected as a zero bit (Spacing Level).

When in FIFO Mode, an FE is associated with a particular character in the FIFO buffer, and revealed to the CPU when the associated character is in the top of the FIFO buffer.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + data bits + Parity + Stop Bits). Bit 4 is reset to logic 0 whenever the CPU reads the contents of the Line Status Register. Restarting after a break is received requires the SIN pin be high for at lease one-half bit time.

When in FIFO Mode BI is associated to the particular character in the FIFO buffer, and this bit is set when the associated character is in the top of the FIFO buffer.

8

NOTE:
Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and Receiver Line Status interrupt is enabled. All bits except bit 7 of the Status Register can be set or reset by writing to the register.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. This bit also causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

When in the FIFO Mode this bit will be set when the XMIT FIFO is empty, and cleared after at least one character is written into the XMIT FIFO buffer. The Transmitter FIFO Empty indications will be delayed one character time minus the last Stop bit time whenever the following occurs: the Transmitter FIFO buffer is empty and there have not been at least two chaacters in the Transmitter FIFO buffer at the same time since the last time that Transmitter FIFO buffer was empty. The first transmitter interrupt after changing the first bit of the FIFO Control Register will be immediate if it is enabled.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 when both transmitter registers (Transmitter Holding Register and Transmitter Shift Register) are idle (empty). It is reset to a logic 0 upon loading of data into the Transmitter Holding Register.

In FIFO Mode this bit is set when the XMIT FIFO buffer and SMIT Shift Register are both empty. It is cleared when at least one byte is written into the XMIT FIFO.

Bit 7: This bit (LSR7) is 0 when in Character Mode. When in FIFO Mode, this bit is a one if there is at least one parity error, framing error or break indication in the FIFO buffer. LSR7 is cleared when this register is read as long as there are no addition errors in the FIFO buffer.

3.6 INTERRUPT IDENTIFICATION REGISTER

The ACE has an interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the Interrupt Identification Register (refer to Table 3-2)

This register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Its contents are indicated in Table 3-6 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 through 3: These three bits are used to identify the highest prioritiy interrupt pending (see Table 3-6).

Bits 4 and 5: These bits are always logic 0.

Bits 6 and 7: These bits, when set, indicate that the device is in FIFO Mode (FCR0 = 1).

Interrupt Identification Register				Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	0	1	--	None	None	--
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
1	1	0	0	Second	Character Timeout Identification	No Characters have been input or removed from RCVR FIFO buffer during the last four character times, and at least one character occupies it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Table 3-6. Interrupt Control Functions

3.7 INTERRUPT ENABLE REGISTER

This 8-bit register enables the four interrupt sources of the ACE to separately activate the device Interrupt (INT) output signal, when bit 3 of MCR is a logic 1. Its contents are indicated in Table 3-2 and are described below. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INT output from the device. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

3.8 SCRATCH PAD REGISTER

This 8-bit register does not control or report status on any part of the ACE. It is a read/write register that can be used by the programmer to as a general purpose register.

3.9 FIFO CONTROL REGISTER

This write only register is located at the same address as the IIR (read only). This register is used to enable FIFO Mode, clear FIFO buffers, set the RCVR FIFO trigger levels, and select the mode of DMA signaling.

Bit 0: Writing a one to this bit enables the XMIT and RCVR FIFO buffers. When changing from Character Mode to FIFO Mode and vice versa, data in the FIFO buffers does not automatically clear. Resetting FCR0 will clear all characters from RCVR Error FIFO. The FIFOs should be cleared immediately after changing to FIFO mode. This bit must be a 1 before writing to other FCR bits or they will not be programmed.

Bit 1: Writing a 1 to FCR1 will clear all bytes from RCVR Error FIFO and reset its counters to 0, and then self clear this bit to 0. The shift register and RCVR FIFO are not cleared.

Bit 2: Functions the same as bit 1, but for XMIT FIFO.

Bit 3: If FCR0 = 1, setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from Mode 0 to Mode 1 (See pin description of RXRDY and TXRDY).

Bits 4 and 5: Reserved for future use.

Bits 6 and 7: These bits control the trigger level of the RCVR FIFO interrupt.

7	6	RCVR FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

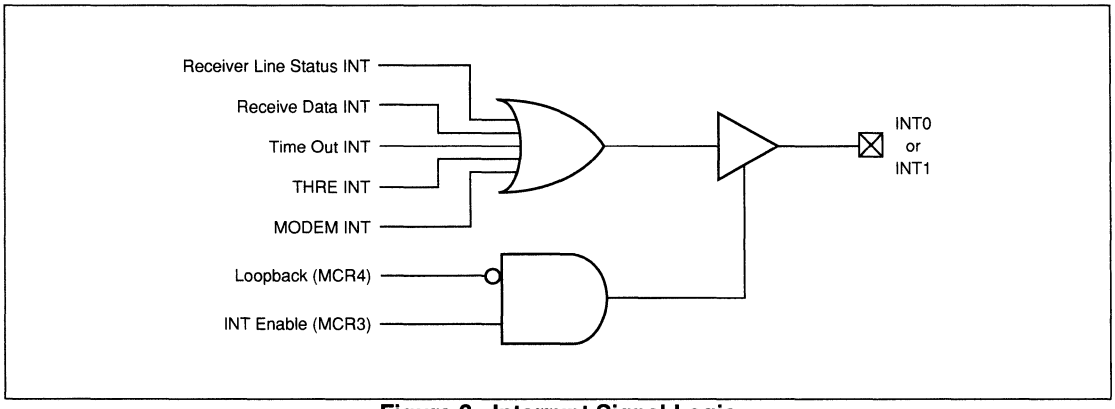


Figure 3. Interrupt Signal Logic

4.0 MODEM CONTROL REGISTER

This 8-bit register controls the interface either with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 3.2

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE:
The $\overline{DTR}$ output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: No connect. In loopback mode this bit is connected to the MODEM Status Register bit 6.

Bit 3: This bit enables the INT output pin. When this bit is a logic 0 the INT output pin is tri-stated. In loopback mode this bit is connected to bit 7 of the MODEM Status Register.

Bit 4: This bit provides a loopback feature for diagnostic testing of the ACE. When bit 4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to a logic 1 (high) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control Inputs (CTS, DSR, RLSD, and RI) are disconnected; and the four MODEM Control outputs (0-3) are internally connected to the four MODEM Control inputs. The INT output pin is tri-stated when in loopback mode. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The ACE MODEM interrupt system can be tested by writing into the lower four bits of the MODEM Status Register. The resetting of these interrupts is the same as in normal ACE operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to a logic 0.

Bits 5 through 7: These bits are permanently set to a logic 0

5.0 MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. Besides this information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 3.2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input to the device has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSR input to the device has changed since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the device has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the RLSD input to the chip has changed state.

NOTE: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send (CTS) input. This bit becomes equivalent to RTS of the MODEM control register, if Bit 4 of the MODEM control register is set to 1.

Bit 5: This bit is the complement of the Data Set Ready (DSR) input. This bit becomes equivalent to DTR of the MODEM control register, if Bit 4 of the MODEM control register is set to 1.

Bit 6: This bit is the complement of the Ring Indicator (RI) input. This bit becomes equivalent to Bit 2 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 7: This bit is the complement of the Received Line Signal Detect (RLSD) input. This bit becomes equivalent to Bit 3 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

5.1 FIFO INTERRUPT MODE OPERATION NOTES

When FCR0=1 and IER0=1 the following RCVR interrupts will occur:

1. A FIFO timeout interrupt occurs when:
   a. There is at least one byte in the RCVR FIFO buffer
   b. No character has been received in 4 continuous character times (if 2 stop bits are being used the second one is included in this time delay).
   c. The most recent CPU read from the FIFO buffer has exceeded 4 continuous character times.

The timeout counter is proportional to the baud rate. After a time out interrupt, the interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

2. When the RCVR FIFO buffer reaches its programmed trigger level the receive data interrupt is set. This interrupt is cleared as soon as the FIFO buffer level falls below the trigger level.

5.2 FIFO POINTER NOTES

The RCVR FIFO has an internal pointer that automataically points to the RCVR Data byte to be read and the associated Status byte. Reading the RCVR Data byte will increment the internal counter, whereas reading the Status byte will not. The Status byte should always be read prior to the Data byte associated with it.

5.3 FIFO POLLING MODE OPERATION NOTES

This mode is initialized when FCR0=1 and IER0, IER1, IER2, and IER3 are all 0. In polling mode the user must poll the LSR to check the transmitter and receiver status. Since the receiver and transmitter are controlled separately either one or both can be in polling mode.

There is no trigger level reached or timeout condition indicated in the FIFO Polling Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

6.0 PARALLEL PORT DESCRIPTION

The parallel port supports Centronics-type printers. When CS2 is low, the parallel port is selected allowing access to all parallel port control and status registers. (Refer to Tables 6-1 and 6-2.)

Register Descriptons:

Read Port Register

Bits 0 through 7: These bits correspond to the data on the parallel bus. This register is used to read the data from the parallel bus.

Read Status Register

Bits 0 through 1: These bits are set to a logic one.

Bits 2: This bit represents the status of the $\overline{INT}$ pin. This bit is only available in the WD16C551/ WD16C451B.

Bits 3 through 7: These bits represent the status of the corresponding pins. Refer to Table 6-2.

Read Control Register

Bits 0 through 3: These bits show the status of the corresponding pins. Refer to Table 6-2.

Note: These values reflect the signal on the open drain outputs, not necessarily the value in the write control register.

A1	A0	$\overline{IOR}$	$\overline{IOW}$	REGISTER
0	0	0	1	Read Data
0	1	0	1	Read Status
1	0	0	1	Read Control
1	1	0	1	Invalid
0	0	1	0	Write Data
0	1	1	0	Invalid
1	0	1	0	Write Data
1	1	1	0	Invalid

Table 6-1. Parallel Port (CS2=0) Register Addresses

BIT NO.	READ PORT 0	READ STATUS 1	READ CONTROL 2	WRITE CONTROL 2	WRITE DATA 0
0	Data Bit 0	1	Strobe	Strobe	Data Bit 0
1	Data Bit 1	1	Autofd	Autofd	Data Bit 1
2	Data Bit 2	$\overline{INT}$ ♦	Init	Init	Data Bit 2
3	Data Bit 3	Error	Slin	Slin	Data Bit 3
4	Data Bit 4	Slct	Irq Enb	Irq Enb	Data Bit 4
5	Data Bit 5	PE	1	DIR ♦	Data Bit 5
6	Data Bit 6	Ack	1	1	Data Bit 6
7	Data Bit 7	Busy	1	1	Data Bit 7
(♦) These bits are 0 in Character Mode.					

Table 6-2. Accessible Parallel Port Registers

Bit 4: This bit represents the status of INT2 being enabled. INT2 is enabled when this bit is set to one.

Bits 5 through 7: These bits always return to a logic one.

Write Port Register

Bits 0 through 7: These bits correspond to the data to be placed on the parallel bus. This register is used to write data to the parallel bus based on Table 6-3.

Write Control Register

Bits 0 through 4: Writing to these bits will set the output of the corresponding pins.

Bit 5: The Direction bit works in conjunction with the BIDEN pin to determine the direction of the parallel port data bus in extended mode, as described in the table below. This bit is only availabe in the WD16C551/WD16C451B, and is a write-only bit.

Port Mode	Port Direction	Pin 1 Biden	Direction Bit
Extended	Write	1	O
Extended	Write	0	X
Extended	Read	1	1
Compatible	Write	0	N/A
Compatible	Read	1	N/A

Table 6-3. Parallel Port Operation Modes

Register/Signal	Reset Control	Reset State
Control	Master Reset	All bits low.
Data (Write)	Master Reset	All bits low.
Data (Read)	Master Reset	Data
Status	Master Reset	Bits 0-2 are high, Bits 3-7 are ERR, SLCT, PE, ACK and Busy inputs.
INT2	Master Reset	High Impedance
$\overline{\text{SLIN}}$	Master Reset	High
$\overline{\text{INIT}}$	Master Reset	Low
$\overline{\text{AFD}}$	Master Reset	High
$\overline{\text{STB}}$	Master Reset	High

Table 6-4. Registers/Signals Parallel Port Reset Control

7.0 TYPICAL APPLICATIONS

Figures 7-1 and 7-2 show how to use the ACE devices in a 80286 system and in a microcomputer system with a high-capacity data bus.

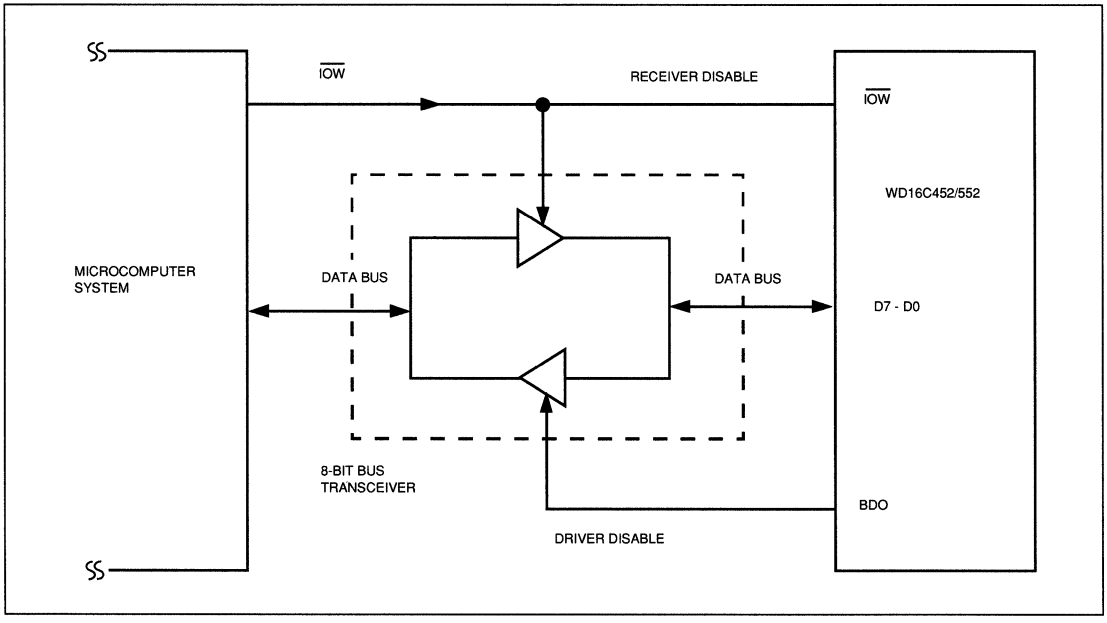


Figure 4. Typical Interface for a High-Capacity Data Bus

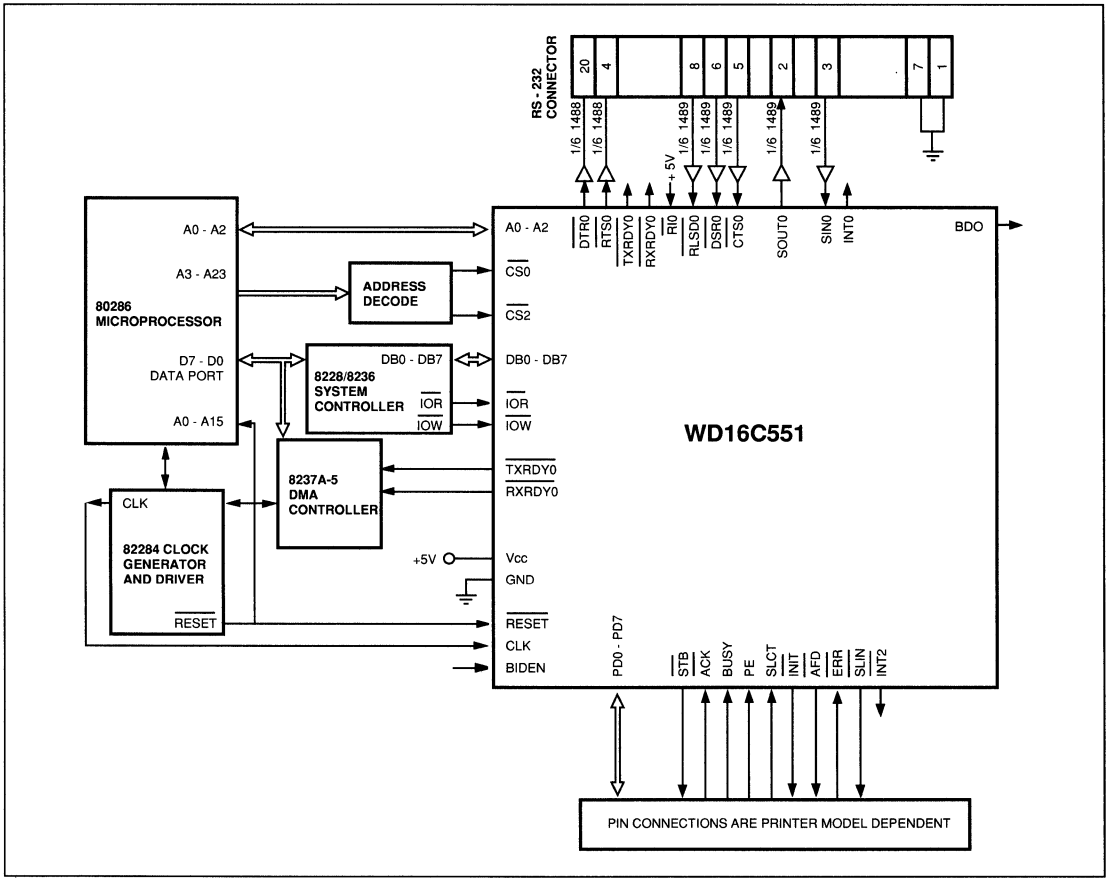


Figure 5. Typical 16-Bit Microprocessor/RS-232 Terminal Interface Using The WD16C551

8.0 CRYSTAL MANUFACTURERS (Partial List)

American Time Products Division
Frequency Control Products Inc
Woodside, NY 11337

Bliley Electric Company
Erie, PA 16508

Cryster Crystals
Whitby, Ontario

Erie Frequency Control
Carlisle, PA 17013

Q-Matic Corporation
Costa Mesa, CA 92626

CRYSTAL SPECIFICATIONS

Frequency: 1.8432 MHz, 3.072 MHz, and 8.0 MHz

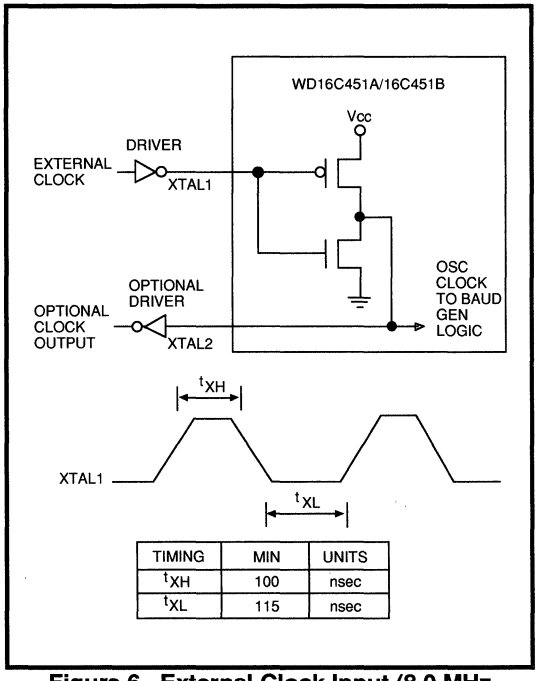
Type: Microprocessor Crystal

Temp. Range: 0°C (32°F) to +70°C (158°F)

Series Resistance:

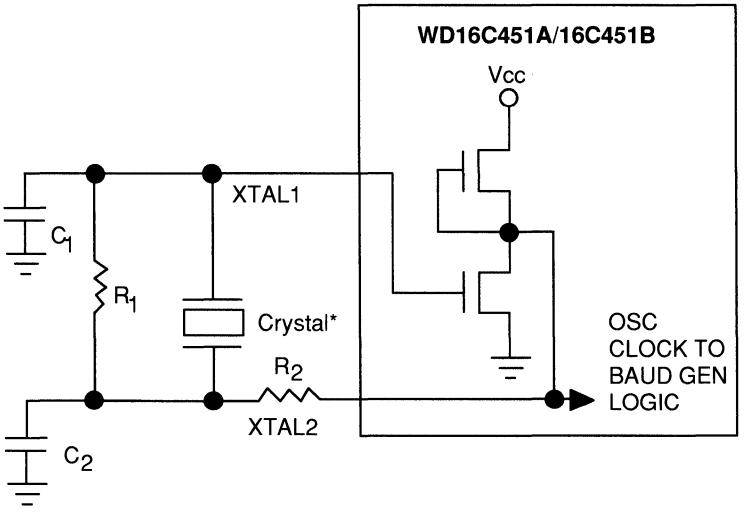
200-500 Ohms at 1.8432 MHz
100-200 Ohms at 3.072 MHz
20-40 Ohms at 8.0 MHz

Series Resonant
Overall Tolerance: ±0.01%



TIMING	MIN	UNITS
t_{XH}	100	nsec
t_{XL}	115	nsec

Figure 6. External Clock Input (8.0 MHz Maximum)



Crystal	R_1	R_2	C_1	C_2
8.0 MHz	1M Ohm	0-100 Ohm	5-10 pF	20-40 pF
3.1 MHz	1M Ohm	0-100 Ohm	10-20 pF	100-200 pF
1.8 MHz	1M Ohm	0-100 Ohm	10-20 pF	100-200 pF

EXAMPLE

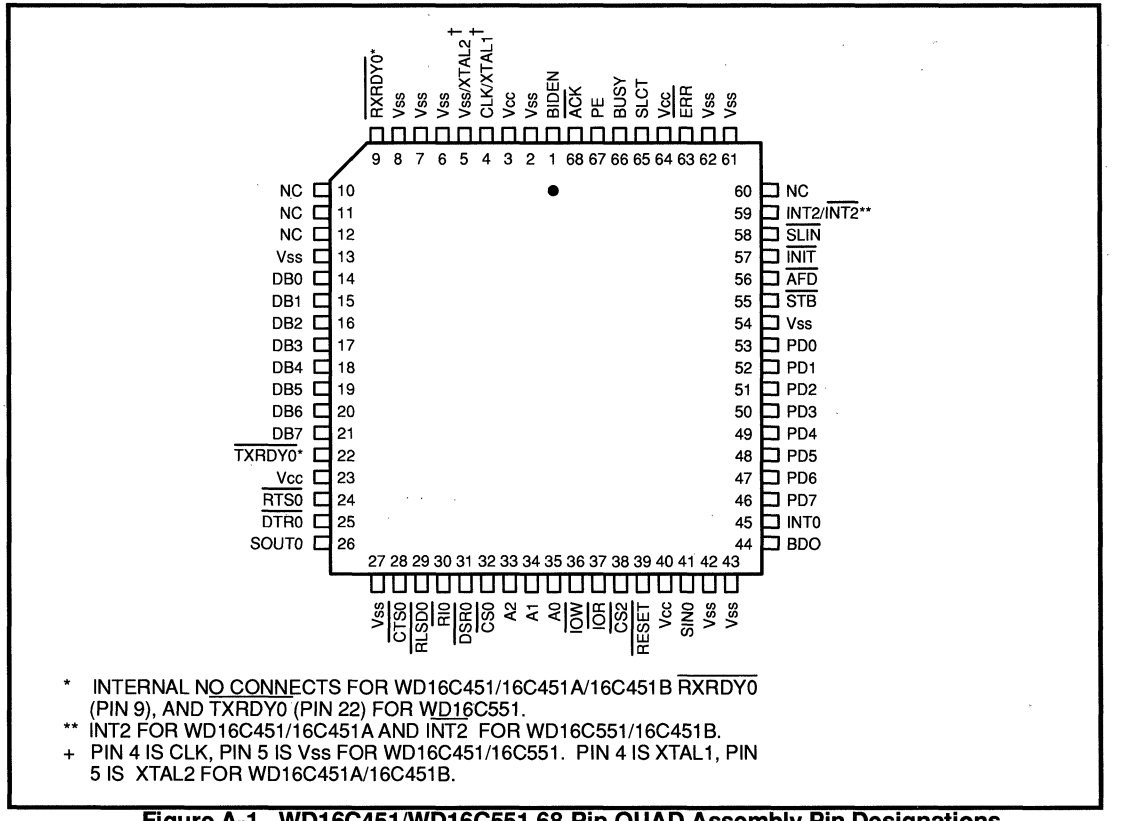
Figure 7. Typical Crystal Oscillator Network

8

APPENDIX A

A.0 PIN DESCRIPTIONS

Figure A-1 illustrates the 68-Pin QUAD assembly. Table A-1 lists all pin designations.



* INTERNAL NO CONNECTS FOR WD16C451/16C451A/16C451B RXRDY0 (PIN 9), AND TXRDY0 (PIN 22) FOR WD16C551.
** INT2 FOR WD16C451/16C451A AND INT2 FOR WD16C551/16C451B.
\+ PIN 4 IS CLK, PIN 5 IS Vss FOR WD16C451/16C551. PIN 4 IS XTAL1, PIN 5 IS XTAL2 FOR WD16C451A/16C451B.

Figure A-1. WD16C451/WD16C551 68-Pin QUAD Assembly Pin Designations

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
1	BIDEN	Bidirectional enable	Input signal in WD16C451/16C451A when low enables the parallel port data lines as outputs. When high, the WD16C451 /16C451A will hold the parallel port data pins in a high-impedance state, allowing these pins to be driven with data. The BIDEN input signal on the WD16C551/16C451B works in conjunction with the DIR bit (see Table 6-3) to control the direction of the parallel port data bit.
2, 6-8, 13, 42, 27, 43, 54, 61, 62	Vss	Ground	System signal ground.
3, 23, 40, 64	Vcc	Power Supply	+5V power supply.
WD16C451/16C551:			
4	CLK (Times 1)	Clock Input	External clock input.
5	Vss	Ground	System signal ground.
WD16C451A/16C551B:			
4	XTAL1	External Clock In	Connects the crystal to the ACE baud rate divisor circuit.
5	XTAL2	External Clock Out	Connects the crystal to the ACE baud rate divisor circuit.
9	$\overline{\text{RXRDY0}}$ ♦	$\overline{\text{Receiver Ready}}$	Receiver ready output is used to signal DMA transfer to the CPU from the ACE. Two modes of operation are available in FIFO Mode, and one (Mode 0) in Chararacter Mode. Mode 0: When in Character Mode (FCR0=0), or in the FIFO Mode (FCR0=1) with FCR3=0, RXRDY will be active (low) if there is at least one character in the RCVR holding register or RCVR FIFO register. RXRDY will go inactive when the RCVR FIFO buffer (FIFO Mode), or holding register (Character Mode) is empty. Mode 1: In FIFO Mode (FCR0=1) with FCR3=1, $\overline{\text{RXRDY}}$ will go active (low) when the trigger level or time out has been reached. $\overline{\text{RXRDY}}$ goes inactive (high) when the FIFO buffer is empty.
(♦) These pins are internal no-connects on the WD16C451.			

Table A-1. Pin Descriptions

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
10-12	NC	No connection	Internally not connected.
14-21	DB0-DB7	Data Bits	Tri-state, bidirectional communication lines between the internal registers and Data Bus. D0 is the LSB and the first serial transmitted or received bit.
22	$\overline{\text{TXRDY0}}$♦	$\overline{\text{Transmitter Ready}}$ FIFO Contro	Transmit ready output is used to signal. DMA transfer to the CPU from the ACE. Two modes of operation are available when using FIFO Mode, and one (Mode 0) when using Character Mode. Mode 0: In Character Mode (FCR0=0) or in FIFO Mode (FCR0=1) with FCR3=0, TXRDY will be active (low) if there are no characters in the Xmit FIFO buffer (FIFO Mode) or Xmit holding register (Character Mode). TXRDY will go inactive after the first character is loaded. Mode 1: In FIFO Mode (FCR0=1) with FCR3=1, if there is one or more unfilled position in the Xmit FIFO $\overline{\text{TXRDY0}}$ will be active (low). $\overline{\text{TXRDY0}}$ goes inactive when the FIFO buffer is completely full.
24	RTS0	$\overline{\text{Request to Send}}$	Output when low informs the MODEM or data set that the ACE is ready to transmit data. This value is reflected in bit 1 of the MODEM Control Register.
25	$\overline{\text{DTR0}}$	$\overline{\text{Data Terminal Ready}}$	Output when low informs the MODEM or data set that the ACE is ready to receive. This value is reflected in bit 0 of the MODEM Control Register.
26	SOUT0	Serial Data Output	Transmitted Serial Data Out to the communication link from the ACE.SOUT is set to a marking condition (logical 1) on a Master Reset.
28	$\overline{\text{CTS0}}$	$\overline{\text{Clear to Send}}$	Input from DCE to the ACE indicating remote device is ready to transmit. This value is reflected in bit 4 of the MODEM Status Register.
(♦) These pins are internal no-connects on the WD16C451.			

Table A-1. Pin Designations (Contd)

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
29	RLSD0	Received Line Signal Detect	IInput from the DCE indicating that the ACE is receiving a signal that meets its signal quality conditions. Bit 3 of the MODEM Status Register reflects this value.
30	$\overline{RI0}$	Ring Indicator	Input when low indicates a ringing signal being received by the MODEM or data set. This logical value is reflected in bit 6 of the MODEM status Register.
31	$\overline{DSR0}$	Data Set Ready	When low, this input signal from the communication link indicates that it is ready to exchange data with the ACE. Bit 5 of the associated MODEM Status Register reflects the $\overline{DSR}$ logical state.
32	$\overline{CS0}$	Chip Select 0	Chip Select input when active (low) selects serial channel 0.
33 thru 35	A2, A1, A0	Address lines A2-A0	These three inputs are used to select an internal register of the ACE, or parallel port.
36	$\overline{IOW}$	$\overline{Input/Output}$ Write Strobe	Input when active (low), causes data from the data bus (DB0-DB7) to be input to the selected port's addressed register. The data will be written to the register chosen by A0-A2 and the port is chosen by CS0 or CS2 to be ACE parallel port, respectively.
37	$\overline{IOR}$	Input/Output Read Strobe	Input active (low) will display data from the selected internal register on the data bus DB0-DB7. The chip select line determines within which port the register being accessed resides, and A0-A2 choose the internal register to be read.
$\overline{38}$	CS2	$\overline{Chip\ Select\ 2}$	Chip Select input when active (low), enables the line printer port.
39	$\overline{Reset}$	$\overline{Reset}$	Input when active (low), will force the device into an idle mode where all serial data activity is suspended. The device will remain in an idle state until programmed to begin data activities.
41	SIN0	Serial Data Inputs	Received Serial Data Input from the communication link to the ACE. Data on the serial data inputs are disabled when exercising loopback mode, and internally connected to their respective SIN lines.

Table A-1. Pin Descriptions (Contd)

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
44	BDO	Bus Buffer Output	Output goes active when either the serial channel or the parallel port is serial channel or the parallel port is selected as an output. BDO is used to control the system bus driver device (74LS245).
45	INT0	Serial Channel Interrupt	Tri-state output (enabled by bit 3 of MCR) goes high whenever an enabled interrupt is pending. INT is reset when the pending interrupt(s) are serviced, or a Master Reset is performed.
46-53	PD7-PD0	Parallel Data Bits	Bidirectional data port which provides parallel input and output to the system. The 8 lines are held in a high impedance state when BIDEN is high.
55	$\overline{STB}$†	$\overline{Line\ Printer\ Strobe}$	Output line, when active, provides the line printer with a signal to latch the data currently on the parallel port.
56	$\overline{AFD}$†	$\overline{Line\ Printer\ Autofeed}$	Output line, when active, provides a signal for the line printer to autofeed continuous form paper.
57	INIT†	$\overline{Line\ Printer\ Initialize}$	Output line to printer, when active (low), signals the line printer to begin an initialization routine.
58	$\overline{SLIN}$†	$\overline{Line\ Printer\ Select}$	Output line, when active (low), selects the printer.
59	INT2/$\overline{INT2}$††	Interrupt Printer Port	Tri-state output enabled by bit 4 of WCR. For the WD16C451/16C451A, INT2 goes active high on the rising transition of $\overline{ACK}$ and reset (low) on the falling transition of $\overline{ACK}$. For the WD16C551/16C451B, INT2 goes active low on the rising edge of $\overline{ACK}$. INT 2 is reset (high) on the rising edge of $\overline{IOR}$, when reading the parallel port status register.
60	NC	No connection	Internally not connected.
63	$\overline{ERR}$	Line Printer Error	Input line from the line printer, informs the parallel port of an error by inputting an active low signal. Set low by the printer upon a deselect condition, PE, or other error condition.

(†) These outputs are open drain with internal pull-ups.
(††) This pin is INT2 fro WD16C451/16C451A and $\overline{INT2}$ for WD16C551/16C451B.

Table A-1. Pin Descriptions (Contd)

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
65	SLCT	Line Printer Select	Input from the line printer that goes high when the line printer has been selected.
66	BUSY	Line Printer Busy	Input from the line printer that goes high when the line printer has an operation in progress.
67	PE	Line Printer Paper Empty	Input from the line printer goes high when the printer is out of paper.
68	$\overline{ACK}$	Line Printer Acknowledge	Input from the line printer that goes low to confirm the data transfer from the WD16C451/16C551 to the printer was successful.

Table A-1. Pin Descriptions (Contd)

8

APPENDIX B

B.0 DC OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Temperature
Under Bias ..... 0°C (32°F) to 70°C (158°F)

Storage Temperature ..... -65°C (-85°F) to +150°C (302°F)

All Input or Output Voltages
With respect to Vss ..... -0.5V to +7.0V

Power Dissipation WD16C451/WD16C551 ..... 300 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Operating Characteristics

WD16C451/WD16C551					
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
Vilx	Clock Input Low Voltage	-0.5	0.8	V	
Vihx	Clock Input High Voltage	2.0	Vcc	V	
Vil	Input Low Voltage	-0.5	0.8	V	
Vih	Input High Voltage	2.0	Vcc	V	
Vol	Output Low Voltage		0.4	V	Iol = 4.0 mA on DB0-DB7. Iol = 24 mA on PD0-PD7. Iol = 20 mA on INIT, STB, SLIN, AFD (NOTE). Iol = 2.0 mA on other outputs.
Voh	Output High Voltage	2.4		V	Ioh = 4.0 mA on DB0-DB7. Ioh = 15.0 mA on PD0-PD7. Ioh = 0.55 mA on INIT, AFD, STB, SLIN. Ioh = 0.2 mA on other outputs.
Icc	Power Supply Current		60	mA	Vcc = 5.25V, no loads on outputs: SIN0, SIN1, DSR0, DSR1, RLSD0, RLSD1, CTS0, CTS1, RI0, RI1 = 2.0V. Other inputs = 0.8V. Baud Rate = 512K. BRG = 8 MHz.
Iil	Input Leakage		æ10	uA	Vcc = 5.25V, Vss = 0.0V. All other pins float.
Icl	Clock Leakage		±10	uA	Vin = 0.0V, 5.25V.
Idl	Data Bus Leakage		±10	uA	Vout = 0.4V, Vout = 4.6V Data Bus in High Impedance State.
Ioz	Tri-state Leakage		±20	uA	Vcc = 5.25V, GND = 0V, Vout = 0.0V, 5.25V.
Vil (RES)	Reset Schmitt Vil		0.8	V	
Vih (RES)	Reset Schmitt Vih	2.0		V	

NOTE: The $\overline{SLIN}$, $\overline{AFD}$, $\overline{STB}$ and $\overline{INIT}$ outputs are all open collector with 2.5K to 3.5K Ohms internal pull-up resistors. When in Vol state, each input will sink a minimum of 20 mA. The internal pull-ups generate 2.0 mA of internal Iol.

Ta = 0°C (32°F) to = 70°C (158°F), Vcc = +5V±5%, Vss = 0V, unless otherwise specified.

Table B-1. DC Operating Characteristics

WD16C451/WD16C551					
SYMBOL	CHARACTERISTIC	TYP	MAX	UNITS	TEST CONDITIONS
Cxin	Clock Input Capacitance	15	20	pF	fc = 1 MHz
Cxout	Clock Output Capacitance	20	30	pF	
Cin	Input Capacitance	6	10	pF	Unmeasured Pins Returned to Vss
Cout	Output Capacitance	10	20	pF	Unmeasured Pins Returned to Vss

Ta = 25°C (77°F), f = 1.0 MHz, Vcc = Vss = 0V

Table B-2. Capacitance

APPENDIX C

C.0 AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

Ta = 0°C (32°F) to + 70°C (158°F), Vss = +5V ±5%

TIMING DIAGRAMS

FIGURE NUMBER	TITLE
C-1	Receiver Timing
C-2	Transmitter Timing
C-3	MODEM Control Timing
C-4	Read Cycle Timing
C-5	Write Cycle Timing
C-6	RCVR FIFO Signaling Timing for First Byte
C-7	RCVR FIFO Signaling Timing after First Byte (RBR already set)
C-8	Receiver DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
C-9	Receiver DMA Mode 1 Timing (FCR0 = 1 and FCR3 = 1)
C-10	Transmitter DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
C-11	Transmitter DMA Mode 1 (FCR3 = 1)
C-12	Parallel Port Timing
C-13	WD16C451/WD16C451A Parallel Port Input Timing
C-14	WD16C551/WD16C451B Parallel Port Input Timing

Table C-1. WD16C451/WD16C551 Timing Diagrams

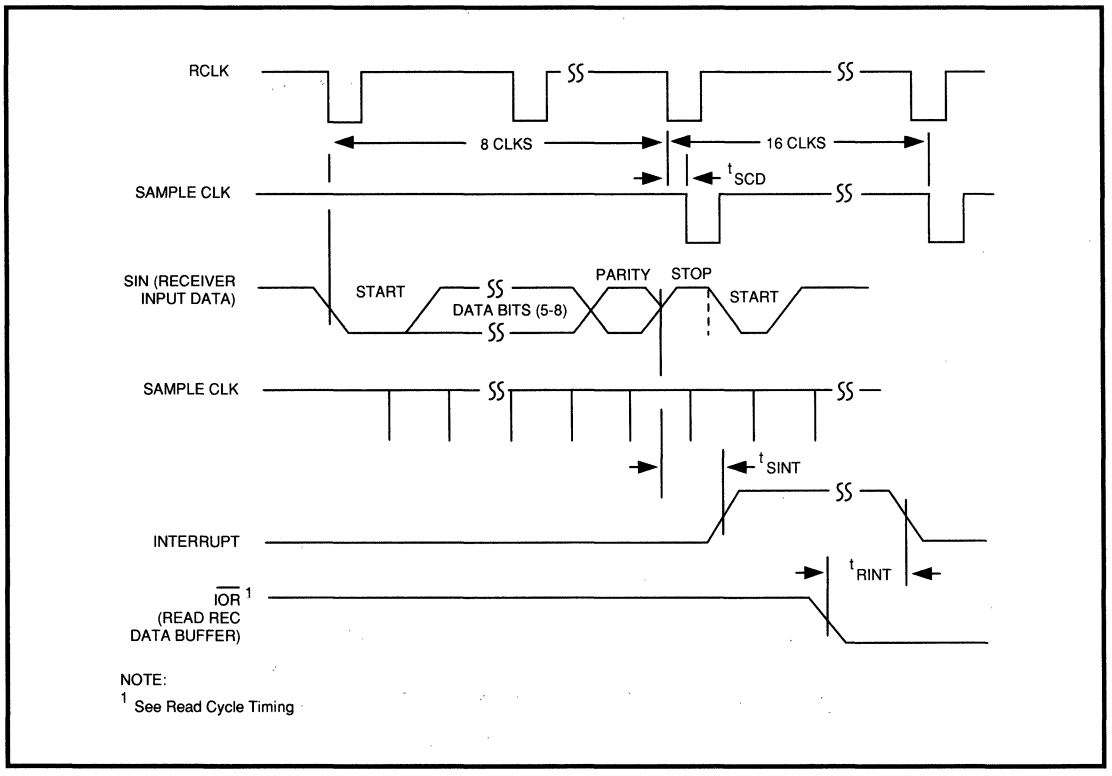


Figure C-1. Receiver Timing

WD16C451/WD16C551					
SYMBOL	**CHARACTERISTIC**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
tSCD	Delay from RCLK† to Sample Time		2	µs	
tSINT	Delay from Stop to Set Interrup		17♦	RCLK† Cycles	100 pF Load
tRINT	Delay from $\overline{IOR}$ (RD RBR) Reset Interrupt		1	µs	100 pF Load

(♦) When receiving the first byte in FIFO Mode, tSINT (only for timeout or trigger level interrupt) will be delayed 19 RCLK cycles, except for a timeout interrupt where tSINT will be delayed 24 RCLK cycles.

(†) RCLK is an internal clock used for sampling serial in data. RCLK is equivalent to 16 times the baud rate clock.

Table C-2. Receiver Timing

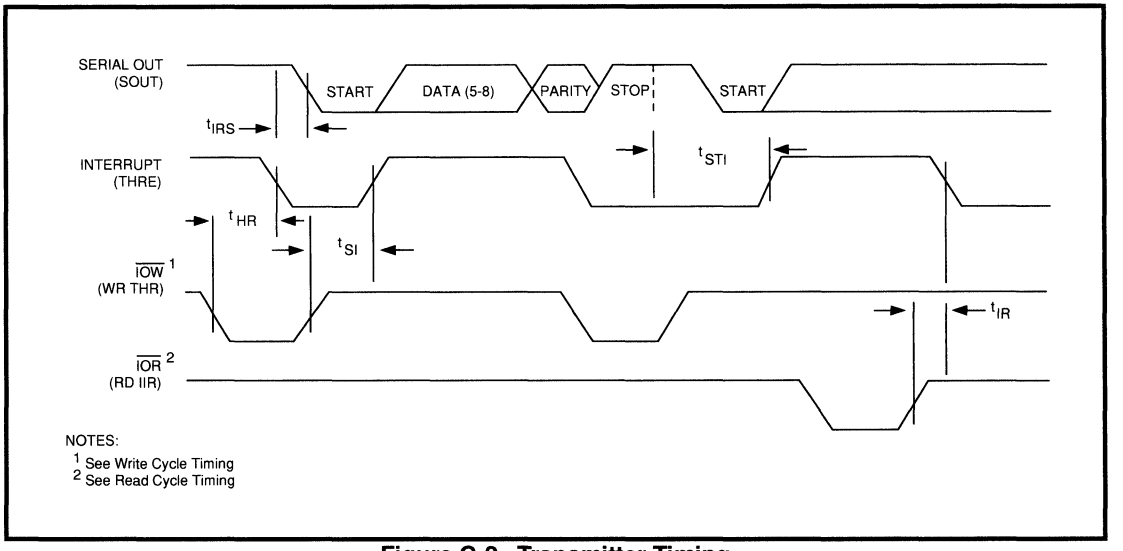


Figure C-2. Transmitter Timing

WD16C451/WD16C551					
SYMBOL	**CHARACTERISTIC**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
tHR	Delay from IOW (WR THR) to Reset Interrupt		175	ns	100 pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start	8	24	TCLK† Clock Cycles	
tSI*	Delay from Initial Write to Interrupt	16	24	TCLK† Clock Cycles	
tSTI	Delay from Stop to Interrupt (THRE)	8	8	TCLK† Clock Cycles	
tIR	Delay from IOR (RD IIR to Reset Interrupt (THRE)		250	ns	100 pF Load
tSXA	Delay from Start to TXRDY Active	0	8	TCLK† Clock Cycles	
tWXI	Delay from Write to TXRDY Inactive	0	300	ns	

(†) TCLK is an internal clock used for sending serial out data. TCLK is equivalent to 16 times the baud rate clock.
(*) In FIFO Mode, tSI might extend to beginning of Stop bit. See Line Status Register for details.

Table C-3. Transmitter Timing

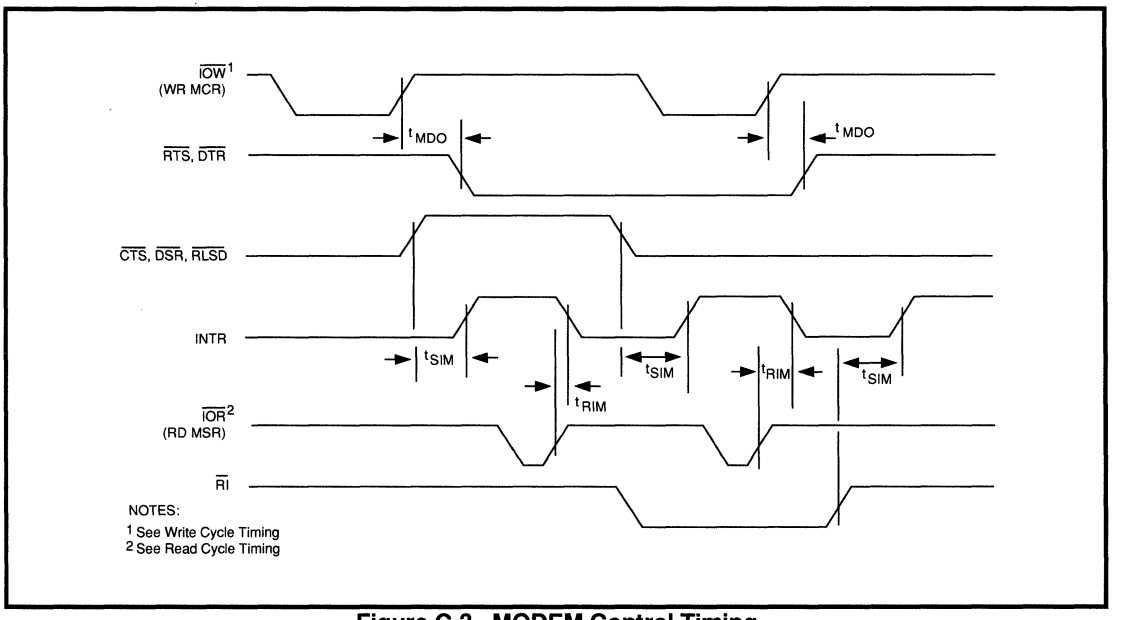


Figure C-3. MODEM Control Timing

WD16C451/WD16C551					
SYMBOL	**CHARACTERISTIC**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
t_{MDO}	Delay from $\overline{IOW}$ (WR MCR) to Output		200	ns	100 pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		250	ns	100 pF Load
t_{RIM}	Delay to Reset Interrupt from IOR (RD MSR)		250	ns	100 pF Load

Table C-4. MODEM Control Timing

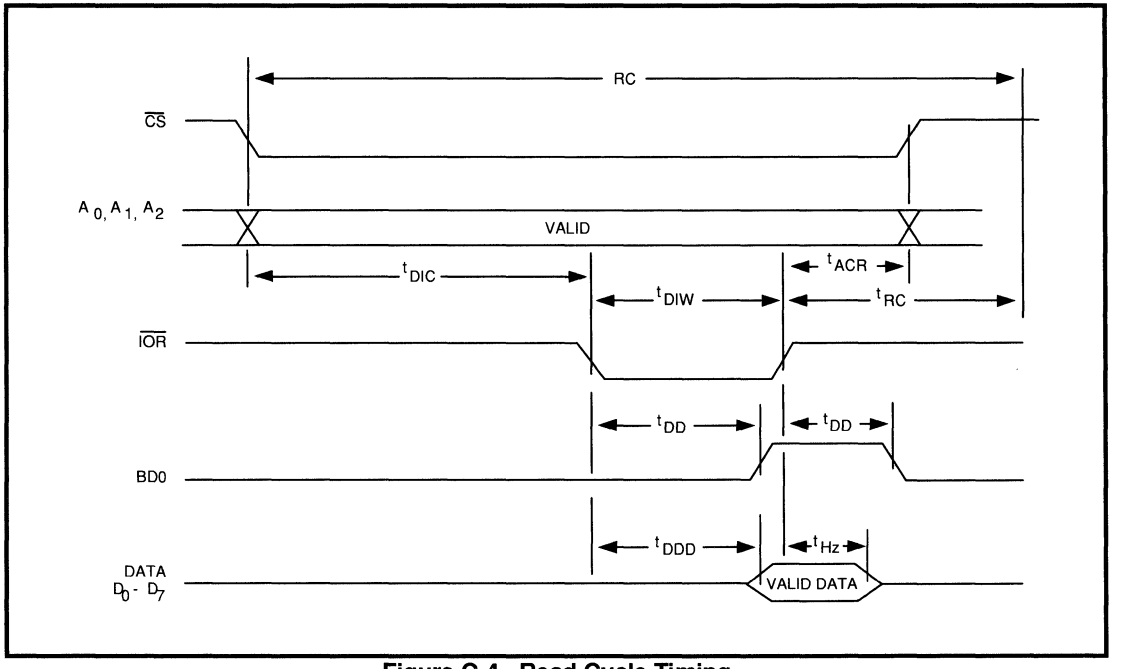


Figure C-4. Read Cycle Timing

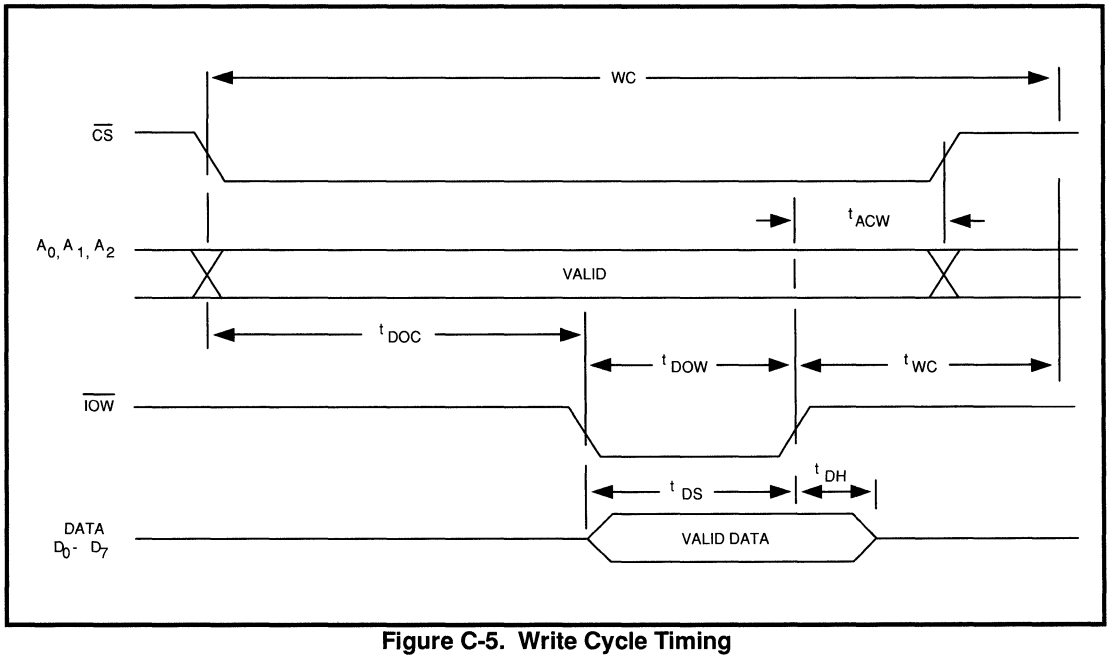


Figure C-5. Write Cycle Timing

WD16C451/WD16C551					
SYMBOL	**CHARACTERISTIC**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
t_{DIW}	$\overline{IOR}$ Strobe Width	125		ns	1TTL Load
tRC	Read Cycle Delay	125		ns	1TTL Load
RC	Read Cycle = tDIC + tDIW + tRC + 20 nsec	280		ns	1TTL Load
t_{DD}	$\overline{IOR}$ to Driver Enable (BDO) Delay		60	ns	1TTL Load
t_{DDD}	Delay from $\overline{IOR}$ to Data		100	ns	1TTL Load
t_{HZ}	$\overline{IOR}$ to Floating Data Delay	0	100	ns	1TTL Load
t_{DOW}	$\overline{IOW}$ Strobe Width	100		ns	1TTL Load
t_{WC}	Write Cycle Delay	150		ns	1TTL Load
WC	Write Cycle = + t_{DOC} + t_{DOW} + t_{WC} + 20 nsec	280		ns	1TTL Load
t_{DS}	Data Setup Time	30		ns	1TTL Load
t_{DH}	Data Hold Time	30		ns	1TTL Load
t_{DIC}	$\overline{IOR}$ DELAY from Select or Address	30		ns	1TTL Load
t_{DOC}	$\overline{IOW}$ Delay from Select or Address	30		ns	1TTL Load
t_{ACR}	Address and Chip Select Hold Time from $\overline{IOR}$	20		ns	1TTL Load
t_{ACW}	Address and Chip Select Hold Time from $\overline{IOR}$	20		ns	1TTL Load
t_{MR}	Master Reset Pulse Width	5.0		µs	1TTL Load
t_{XH}	Duration of Clock HIGH Pulse	55		ns	1TTL Load
t_{XL}	Duration of Clock LOW Pulse	55		ns	External Clock (8.0 MHz Max.)

Table C-5. Read/Write Cycle Timing

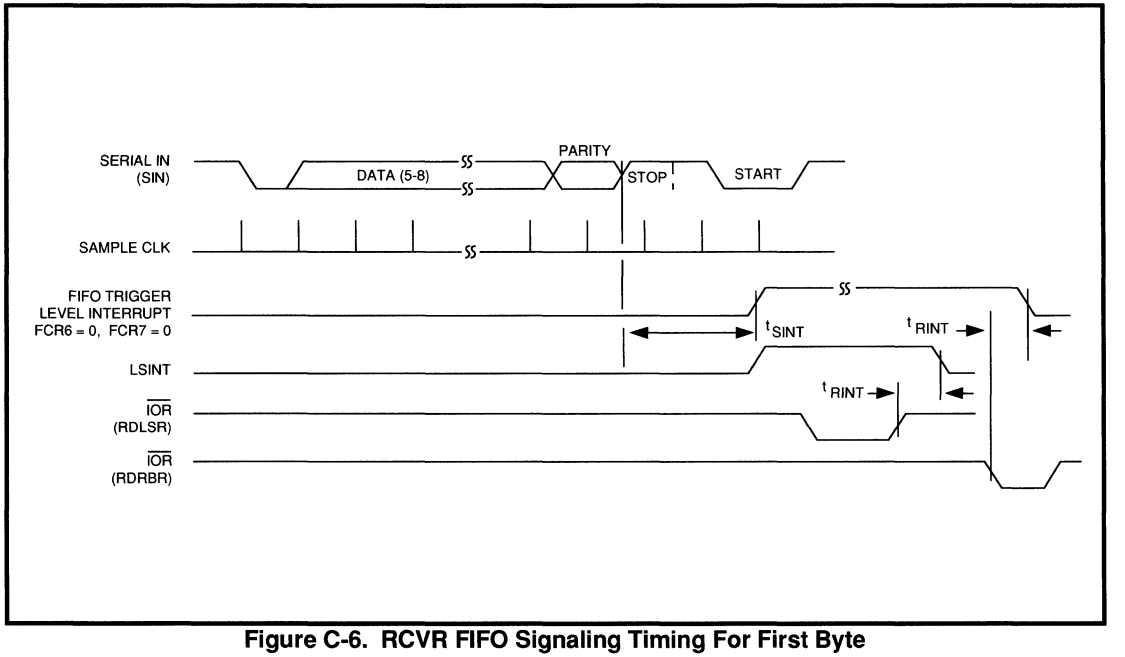


Figure C-6. RCVR FIFO Signaling Timing For First Byte

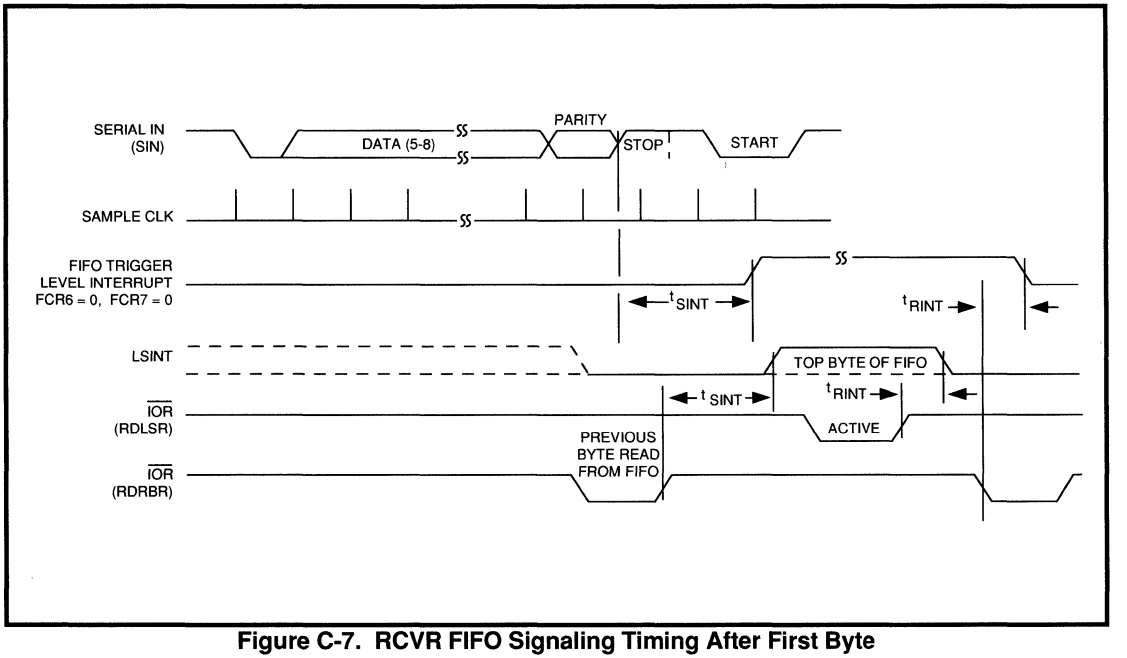


Figure C-7. RCVR FIFO Signaling Timing After First Byte (RBR Already Set)

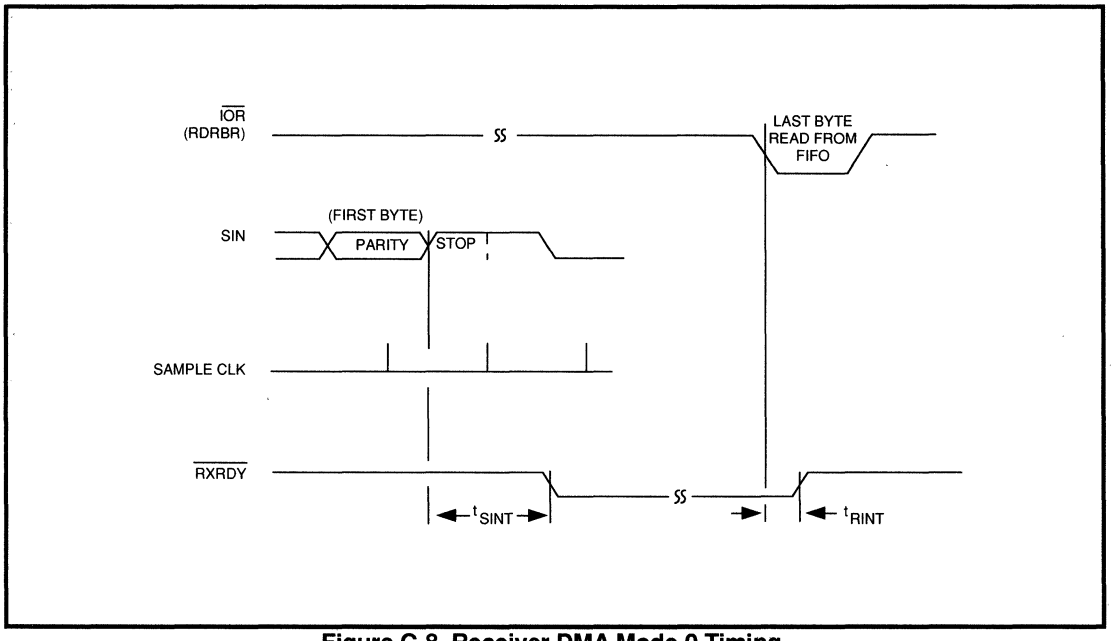


Figure C-8. Receiver DMA Mode 0 Timing
(FCR0 = 0 or FCR0 = 1 and FCR3 = 0)

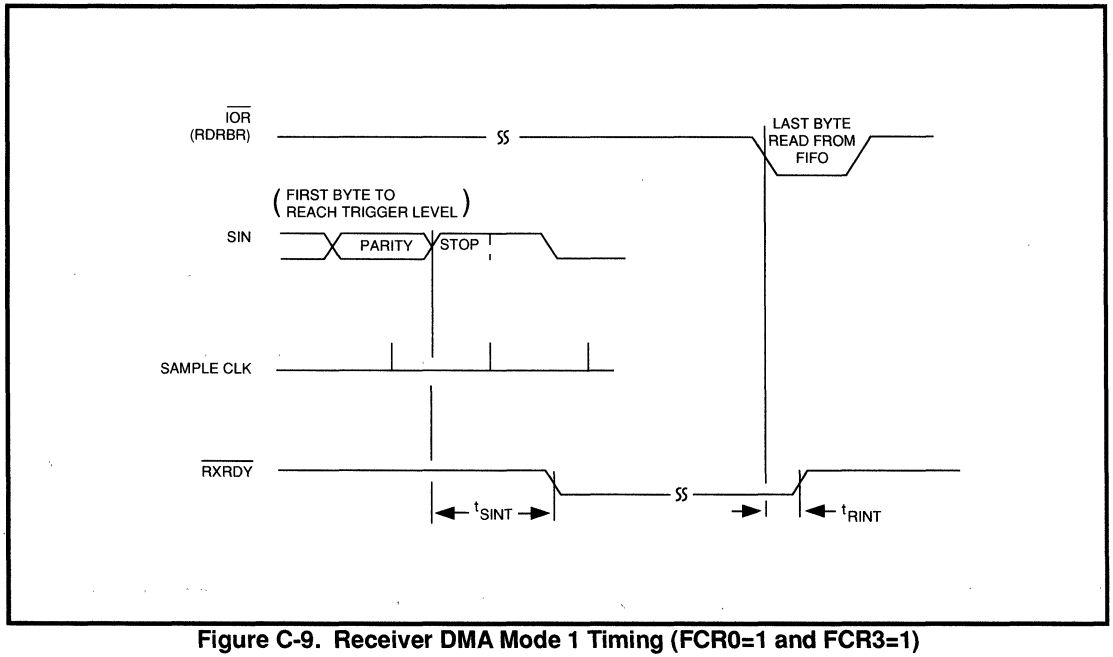


Figure C-9. Receiver DMA Mode 1 Timing (FCR0=1 and FCR3=1)

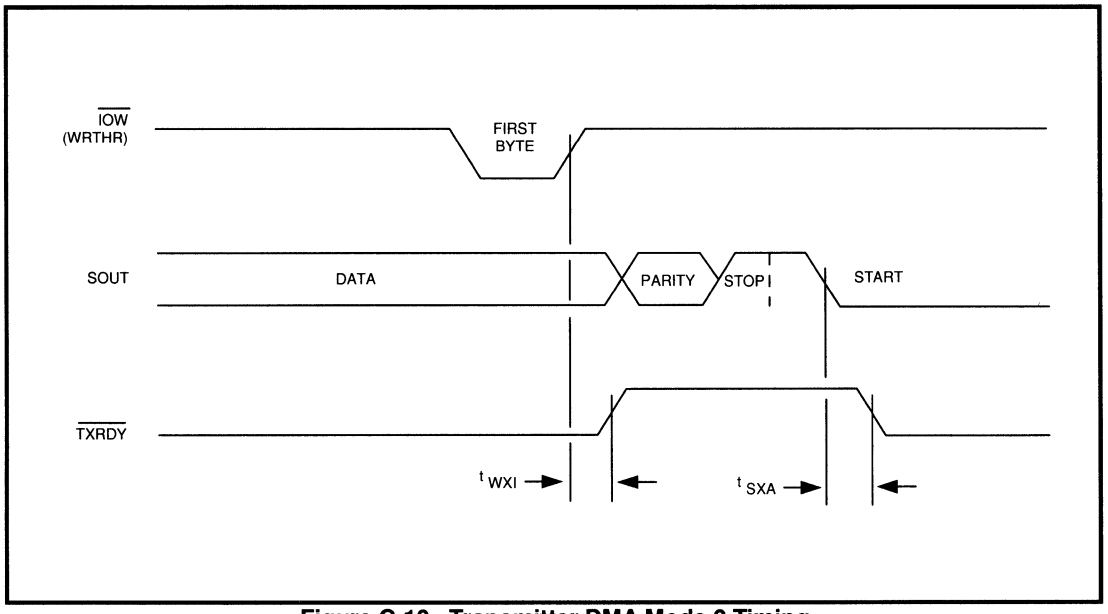


Figure C-10. Transmitter DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)

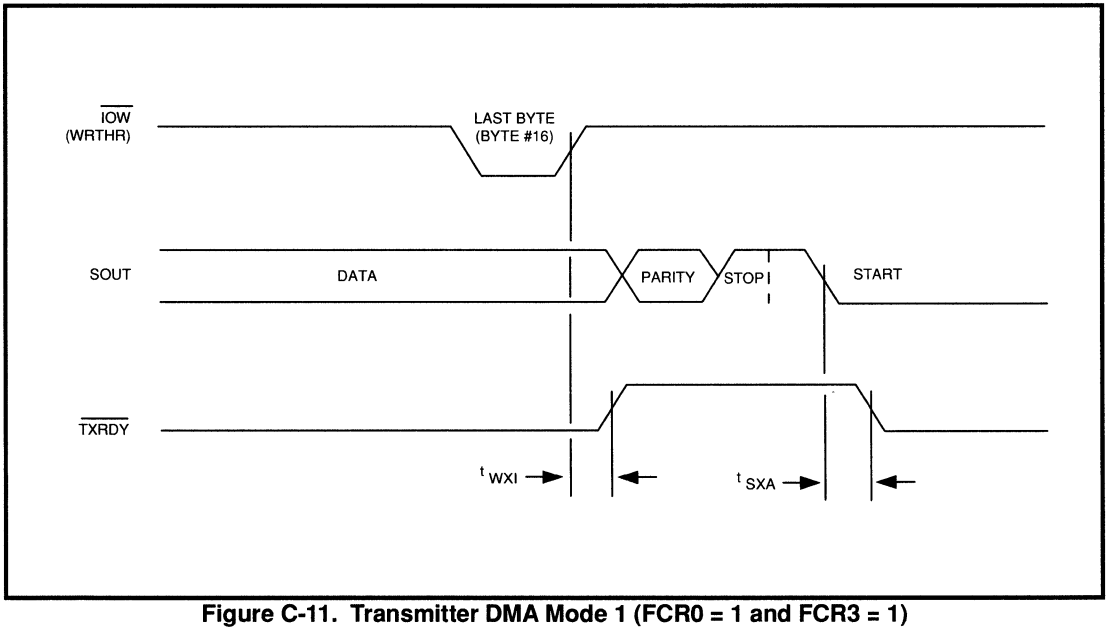
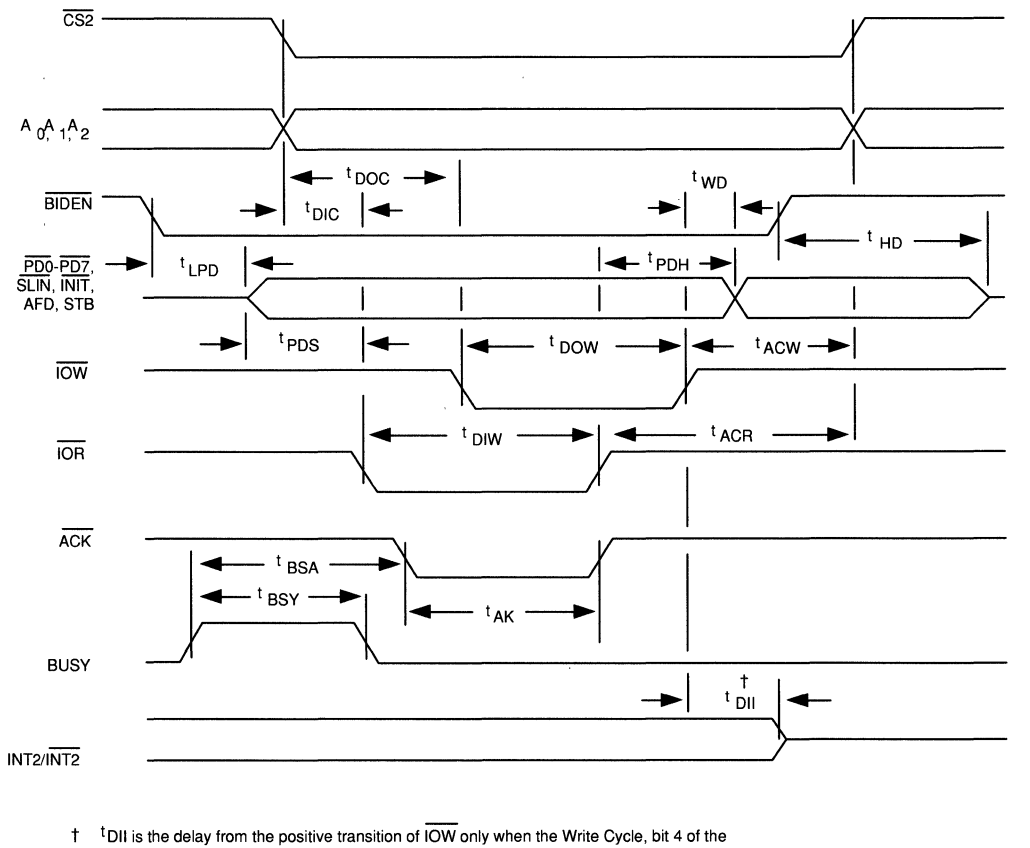


Figure C-11. Transmitter DMA Mode 1 (FCR0 = 1 and FCR3 = 1)



† t_{DII} is the delay from the positive transition of $\overline{IOW}$ only when the Write Cycle, bit 4 of the Write Control Register (IRQ Enable Bit) is low.

Figure C-12. Parallel Port Timing

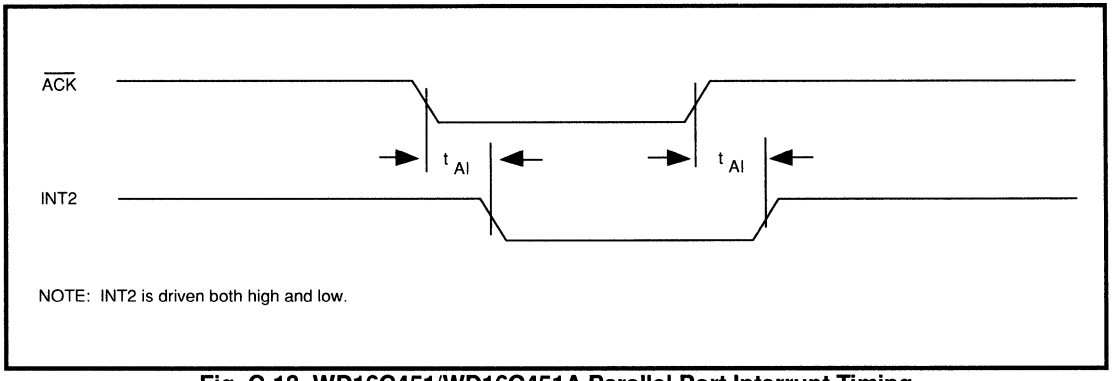


Fig. C-13. WD16C451/WD16C451A Parallel Port Interrupt Timing

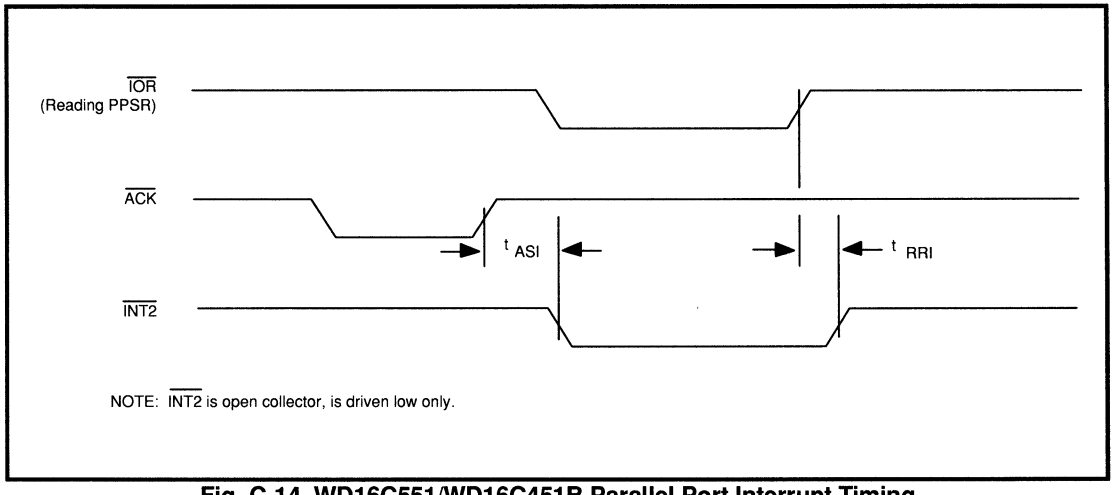


Fig. C-14. WD16C551/WD16C451B Parallel Port Interrupt Timing

WD16C451/WD16C551					
SYMBOL	**CHARACTERISTIC**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
t_{DOC}	$\overline{IOW}$ Delay from Chip Select and Address	30		ns	
t_{DIC}	$\overline{IOR}$ Delay from Chip Select and Address	30		ns	
t_{WD}	$\overline{IOW}$ High to PD0-PD7, SLIN, $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$		1	µs	No External Pull-up Resistor and 50 pF load
t_{HD}	BIDEN High to PD0-PD7 Tri-State		120	ns	
t_{LPD}	BIDEN Low to PD0-PD7 Delay		100	ns	
t_{PDH}	PD0-PD7 Hold Time from $\overline{IOR}$	100		ns	
t_{PDS}	PD0-PD7 Set-up Time from $\overline{IOR}$	100		ns	
t_{DOW}	$\overline{IOW}$ Strobe Width	100		ns	
t_{DIW}	$\overline{IOR}$ Strobe Width	125		ns	
t_{ACW}	Chip Select and Address Hold Time from $\overline{IOW}$	20		ns	
t_{ACR}	Chip Select and Address Hold Time from $\overline{IOR}$	20		ns	
t_{BSA}	BUSY Start to $\overline{ACK}$			ms	Printer Dependent
t_{BSY}	BUSY Width			µs	Printer Dependent
t_{AK}	$\overline{ACK}$ Width			µs	Printer Dependent
t_{AI}	INT2 Delay from $\overline{ACK}$ (WD16C451)		60	ns	1 TTL Load
t_{ASI}	$\overline{ACK}$ to set interrupt (WD16C551)		60	ns	1 TTL Load
t_{RRI}	Read Parallel Port Status Register (PPSR) to reset INT2		60	ns	1 TTL Load
tDII	$\overline{IOW}$ high to INT2/$\overline{INT2}$ Tri-state	0	100	ns	1 TTL Load

Table C-6. Parallel Port Timing

APPENDIX D

D.O PACKAGE DIAGRAM

Figure D-1 illustrates the 68-Pin QUAD plastic package showing dimensions in inches.

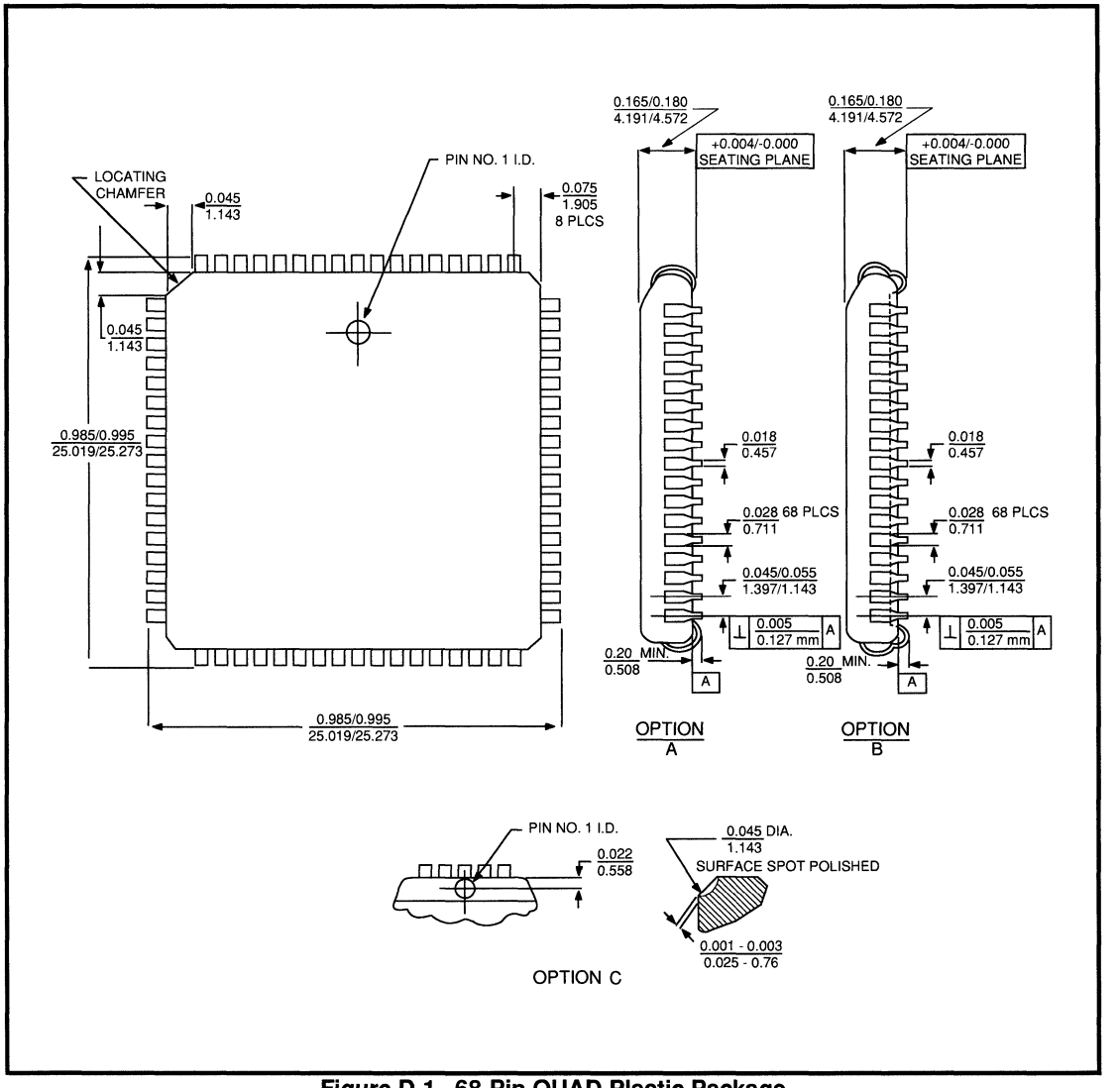


Figure D-1. 68-Pin QUAD Plastic Package

SYSTEMS LOGIC/PERIPHERAL

WD16C452, WD16C552

Dual Enhanced Asynchronous Communications Elements (ACE) with Parallel Port

9

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS
(Continued)

LIST OF TABLES

1.0 INTRODUCTION

1.1 DESCRIPTION

The low power CMOS WD16C452/552 is a single device solution for serving two serial input/output ports simultaneously and one bi-directional parallel port for the IBM PC XT, PC AT, PS/2, and compatible systems. The WD16C452 parallel port is compatible with the Centronics printer port and IBM Serial/Parallel Adapter, and each ACE is programmable and compatible with a WD16C450. The WD16C552 parallel port is compatible with the IBM PS/2 bidirectional parallel port and each ACE is compatible with the WD16C550. Each ACE in the WD16C552 is programmable, and it is capable of buffering up to 16 bytes of data for transmission and up to 16 bytes of data upon reception, relieving the CPU of interrupt overhead. Buffering of data also allows greater latency time in interrupt servicing, which is vital in a multitasking environment. DMA signaling, between the internal FIFO buffers and host CPU, allows single or multiple character transfers. Each ACE has a maximum recommended data rate of 512K with a clock frequency of 8.0 MHz.

(†) The FIFO mode of operation and PS/2 compatible parallel port are not available in the WD16C452.

(*)All trademarks mentioned herein belong to their respective companies.

1.2 FEATURES

- Two fully programmable serial I/O channels (DC to 512K baud)
- Tri-state TTL drive capabilities for bi-directional data bus and control bus on each channel
- Loopback controls for communications link fault isolation for each ACE
- Line break generation and detection for each ACE
- Complete status reporting capabilities
- Generation and stripping of serial asynchronous data control bits (start, stop, parity)
- Programmable baud rate generator and MODEM control signals for each channel
- Fully prioritized independent interrupt system controls for each channel
- 16 byte FIFO buffers on both transmit and receive of each channel for CPU relief during high speed data transfer †
- Programmable FIFO threshold levels of 1, 4, 8, or 14 bytes on each receive channel †
- Two modes of DMA signaling available for transfer of data characters to and from FIFO buffers †
- Bidirectional Centronics compatible parallel port for direct printer interface
- PS/2 compatible bidirectional parallel port †
- CMOS implementation for high speed and low power requirements

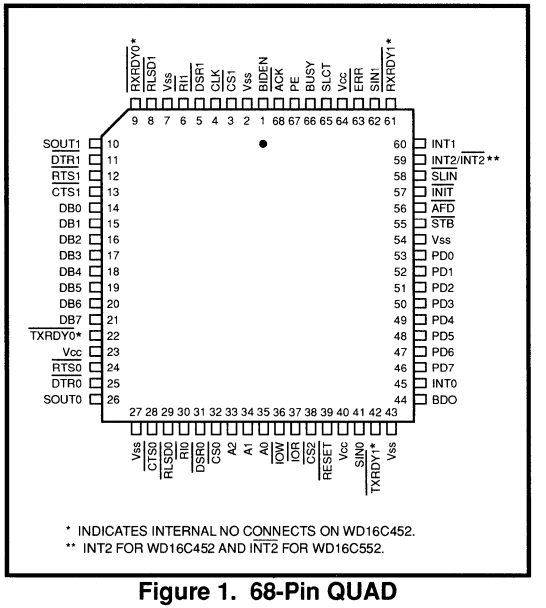


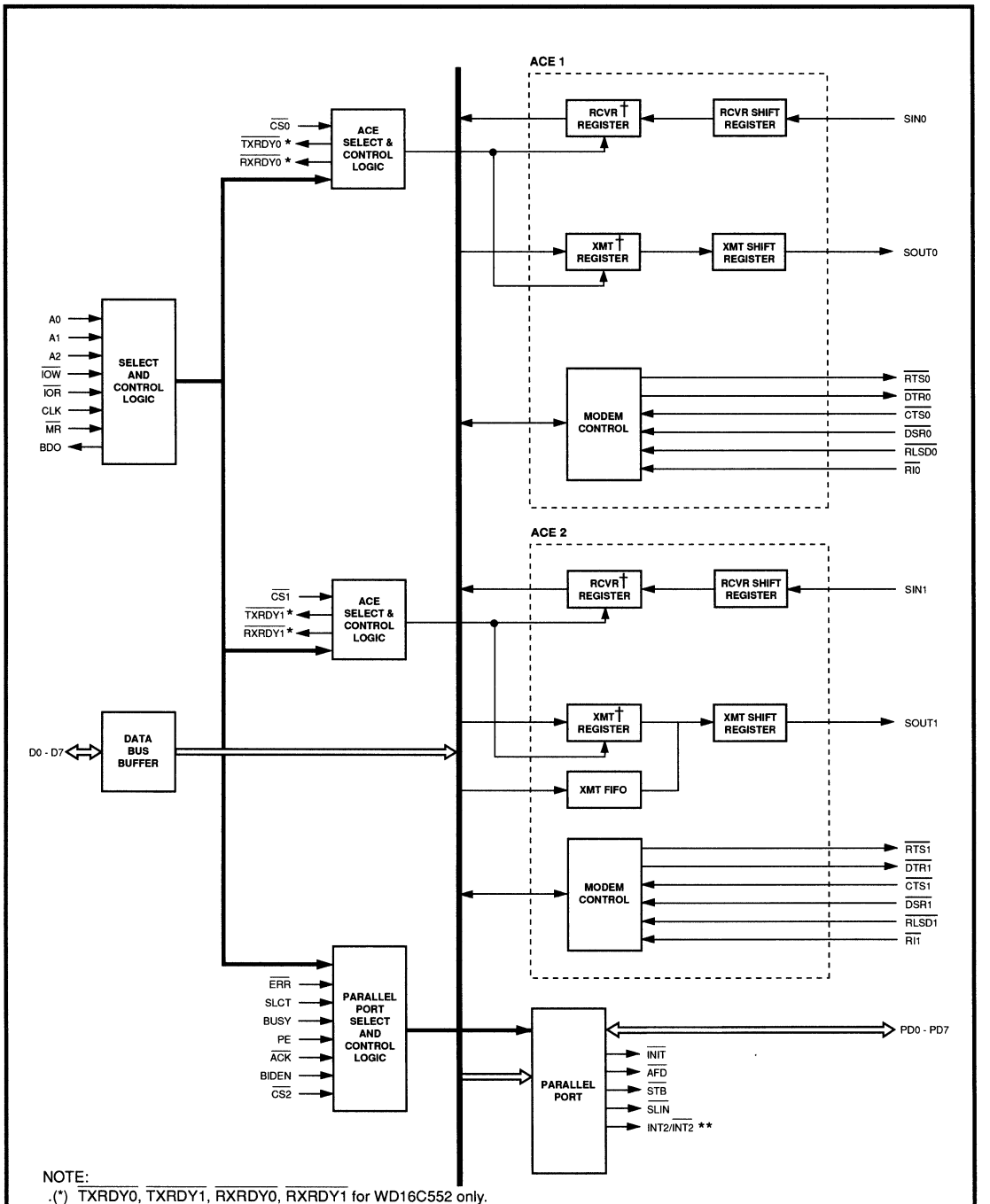
Figure 1. 68-Pin QUAD

1.3 GENERAL

The WD16C452/WD16C552 is a dual ACE, plus a bidirectional parallel port. The two ACE's perform parallel-to-serial conversion on the output and serial-to-parallel conversion on the input. Each ACE is programmable, independent, and has a maximum recommended data rate of 512K baud.

The WD16C452 is a dual channel version of the WD16C450 ACE, plus a bidirectional parallel data port which supports a Centronics compatible printer interface. The parallel port, together with the two serial ports, provides IBM PC XT, PC AT, and compatibles with a single device solution for serving three ports.

The WD16C552 is a dual channel version of the WD16C550 Enhanced ACE, plus a compatible PS/2 bidirectional parallel port. After power-up and hardware reset, each ACE is functionally compatible to the WD16C450 (Character Mode). Each ACE in the WD16C552 has been enhanced with 16 byte FIFO buffers on both the receive and transmit lines, allowing an additional mode of operation called FIFO mode. FIFO mode (only available in WD16C552), can be activated through software, relieving the CPU of excessive overhead due to interrupts. The PS/2 parallel port, together with the two serial ports, provides IBM PS/2 and compatibles with a single device solution for serving three ports.



NOTE:
.(*) TXRDY0, TXRDY1, RXRDY0, RXRDY1 for WD16C552 only.
.(**) INT2 for WD16C452, INT2 for WD16C552.
.(†) 16-byte FIFOs for WD16C552.

Figure 2. WD16C452/WD16C552 Block Diagram

2.0 SERIAL CHANNEL REGISTERS

The WD16C552 contains two serial ports. Therefore, the following registers exist in duplicate, one per channel.

2.1 SERIAL PORT REGISTER ADDRESSING

Chip Select ($\overline{CS0}$, $\overline{CS1}$): When $\overline{CS0}$ is low, registers for serial channel 0 can be accessed, and when $\overline{CS1}$ is low, registers for serial channel 1 can be accessed. No more than one $\overline{CS}$ ($\overline{CS0}$, $\overline{CS1}$) should ever be low at any time (an invalid condition).

Master Reset:
A low level input on this pin causes the ACE to reset to the condition listed in Table 3-1.

Software Reset:
A software reset is performed by writing to the Divisor Latches, forcing the transmitter and receiver to an Idle Mode. (Registers are not reset by this operation.) Prior to enabling interrupts, the LSR and RBR registers should be read to clear out any data. This is used to return to a known state without resetting the system.

Chip Select ($\overline{CS0}$, $\overline{CS1}$) and register select (A0, A1, A2) signals must be stable for the duration of a read or write operation.

Register Select (A0, A1, A2): To select a register for read or write operation, see Table 2-1.

NOTE:
Divisor Latch Access Bit (DLAB) is the MSB of the Line Control Register. DLAB must be programmed high (logic 1) by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer Register (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable Register
X	0	1	0	Interrupt Identification Register (read only)
X	0	1	0	FIFO Control Register (write only)
X	0	1	1	Line Control Register
X	1	0	0	MODEM Control Register
X	1	0	1	Line Status Register (read only)
X	1	1	0	MODEM Status Register
X	1	1	1	Scratch Pad Register
1	0	0	0	Divisor Latch Register (least significant byte)
1	0	0	1	Divisor Latch Register (most significant byte)

Table 2-1. Register Addressing

3.0 ACE OPERATIONAL DESCRIPTION

3.1 MASTER RESET

A low-level input on this pin causes the ACE to reset to the condition listed in Table 3-1.

3.2 ACE ACCESSIBLE REGISTERS

The system programmer has access to any of the registers as summarized in Table 3-2. For individual register descriptions, refer to the following pages under register heading.

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-3; 6 and 7 are forced Low. Bits 4 and 5 are permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, except Bits 5 and 6 are High
MODEM Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low, Bits 4-7 at Input Signal
Divisor Latch (low order byte)	Writing into the Latch	Data
Divisor Latch (high order byte)	Writing into the Latch	Data
SOUT	Master Reset	High
BDO	BDO = $\overline{RCLK \cdot IOR}$ (At Master Reset, the CPU sets RCLK and $\overline{IOR}$ = Low when device is selected.)	High
INT0,1 (RCVR ERRS)	Master Reset/Read LSR	Low
INT0,1 (RCVR DATA READY)	Master Reset/Read RBR	Low
INT2 (WD16C452)	Master Reset/$\overline{ACK}$ (High)	Low
$\overline{INT2}$ (WD16C552)	Master Reset/Read PPSR	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
RCVR FIFO Counter (WD16C552 only)	MR or FCR1• FCR0 or ΔFCR0	All Bits Low
XMIT FIFO Counter (WD16C552 only)	MR or FCR2 • FCR0 or ΔFCR0	All Bits Low
FIFO CONTROL (WD16C552 only)	Master Reset	All Bits Low
D7 - D0 Data Bus Lines	InTri-state Mode, Unless IOR = Low or IOW = Low when Device is Selected	Tri-state Data (ACE to CPU) Data (CPU to ACE)

Table 3-1. Reset Control of Registers and Pinout Signals

	Register Address					
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending (IP)	FIFO Enable (Write Only) (FEWO)	Word Length Select Bit 0 (WLS0)
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 0 (IIDB0)	Rcvr FIFO Reset (RFR)	Word Length Select Bit 1 (WLS1)
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ERLSI)	Interrupt ID Bit 2 (IIDB2)	Transmitter FIFO Reset (TFR)	Number of Stop Bits (STB)
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit 3 (IIDB3)♦	DMA Mode Select (DMS)	Parity Enable (PEN)
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity (STP)
6	Data Bit 6	Data Bit 6	0	FIFO Enabled♦ (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (LSB)(RTLSB)	Set Break Control (SBR)
7	Data Bit 7	Data Bit 7	0	FIFO Enabled♦ (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (MSB) (RTMSB)	Divisor Latch Access Bit (DLAB)

(♦) These bits are 0 in Character Mode.

Table 3-2. Accessible WD16C452/WD16C552 Registers

	Register Address					
	4	5	6	7	0 DLAB=1	1 DLAB=1
Bit No.	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Pad Register	Divisor Latch (LSB)	Divisor Latch (MSB)
0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Not Connected (NC)	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Interrupt (Int)	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO♦ (EIRF)	Received Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

(♦) These bits are 0 in Character Mode.

Table 3-2. Accessible WD16C452/WD16C552 Registers (Contd)

3.3 LINE CONTROL REGISTER

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 are as follows:

Bit 1	Bit 0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1-1/2 Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (Transmit data) or checked (Receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1's when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

3.4 ACE PROGRAMMABLE BAUD RATE GENERATOR

The ACE contains a programmable Baud Rate Generator capable of taking any clock input (dc to 8.0 MHz) and dividing it by any divisor from 1 to (2^{16} - 1). The output frequency of the Baud Generator is 16 times the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3-3, 3-4, and 3-5 illustrate the use of the Baud Generator with three different driving frequencies. One is referenced to a 1.8432 MHz clock. Another is a 3.072 MHz clock. The third is an 8.0 MHz clock.

NOTE:
The maximum operating frequency of the Baud Generator is 8.0 MHz.

In no case should the data rate be greater than 512K baud.

Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	2304	--
75	1536	--
110	1047	0.026
134.5	857	0.058
150	768	--
300	384	--
600	192	--
1200	96	--
1800	64	--
2000	58	0.690
2400	48	--
3600	32	--
4800	24	--
7200	16	--
9600	12	--
19200	6	--
38400	3	--
56000	2	2.860

Table 3-3. BAUD Rates Using 1.8432 MHz Clock

Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	3840	--
75	2560	--
110	1745	0.026
134.5	1428	0.034
150	1280	--
300	640	--
600	320	--
1200	160	--
1800	107	--
2000	96	--
2400	80	--
3600	53	0.628
4800	40	--
7200	27	1.230
9600	20	--
19200	10	--
38400	5	--
56000	3	14.285

Table 3-4. BAUD Rates Using 3.072 MHz Clock

Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	10000	--
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	--
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.344

Table 3-5. BAUD Rates Using 8.0 MHz Clock

3.5 LINE STATUS REGISTER

This 8-bit read and write register provides status information to the CPU concerning the data transfer. Its contents are indicated in Table 3-2 and are described below.

Bit 0: This bit is the Receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register, or to the RCVR FIFO (when in FIFO Mode). Bit 0 will be reset to a logic 0 by the CPU reading the data in the Receiver Buffer Register (for Character Mode).

In FIFO Mode, Receiver Data Ready is set when the receiver shift register is loaded into the FIFO and reset when the receiver FIFO is empty.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode, an OE occurs after the RCVR FIFO is full and the receiver shift register has completely received the next character. An OE is indicated to the CPU as soon as it occurs. The character in the shift register will be written over, but nothing will be transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to logic 0 whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode a parity error is associated with a particular character in the FIFO, and revealed to the CPU when the associated character is in the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop Bit. Bit 3 is set to a logic 1 whenever the Stop Bit following the last data bit or parity bit is detected as a zero bit (Spacing Level). Bit 3 is reset to logic 0 whenever the CPU reads the contents of the Line Status Register. When in FIFO Mode, an FE is associated with a particular character in the FIFO, and revealed to the CPU when the associated character is in the top of the FIFO.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + data bits + Parity + Stop Bits). Bit 4 is reset to logic 0 whenever the CPU reads the contents of the Line Status Register. Restarting after a break is received requires the SIN pin be high for at least one-half (1/2) bit time.

When in FIFO Mode, BI is associated to the particular character in the FIFO, and this bit is set when the associated character is in the top of the FIFO.

NOTE:
Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and Receiver Line Status interrupt is enabled. All bits except bit 7 of the Status Register can be set or reset by writing to the register.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. This bit also causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

When in the FIFO Mode, this bit will be set when the XMIT FIFO is empty, and cleared after at least one character is written into the XMIT FIFO. The Transmitter FIFO Empty indications will be delayed one character time minus the last Stop bit time whenever the following occurs: the Transmitter FIFO is empty and there have not been at least two characters in Transmitter FIFO at the same time since the last time that Transmitter FIFO was empty. The first transmitter interrupt after changing the first bit of FIFO Control Register will be immediate if it is enabled.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 when both transmitter registers (Transmitter Holding Register and Transmitter Shift Register) are idle (empty). It is reset to a logic 0 upon loading of data into the Transmitter Holding Register.

In FIFO Mode this bit is set when the XMIT FIFO and XMIT Shift Register are both empty. It is cleared when at least one byte is written into the XMIT FIFO.

Bit 7: This bit (LSR7) is 0 when in Character Mode. When in FIFO Mode, this bit is a one if there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when this register is read as long as there are no additional errors in the FIFO.

3.6 INTERRUPT IDENTIFICATION REGISTER

The ACE has an interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the Interrupt Identification Register (refer to Table 3-2).

This register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Its contents are indicated in Table 3-6 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 through 3: These three bits are used to identify the highest prioritiy interrupt pending (see Table 3-6).

Bits 4 and 5: These bits are always logic 0.

Bits 6 and 7: These bits, when set, indicate that the device is in FIFO Mode (FCR0 = 1).

Interrupt Identification Register				Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	0	1	--	None	None	--
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
1	1	0	0	Second	Character Timeout Identification	No Characters have been input or removed from RCVR FIFO during the last 4 character times, and at least one character occupies it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Table 3-6. Interrupt Control Functions

3.7 INTERRRUPT ENABLE REGISTER

This 8-bit register enables the four interrupt sources of the ACE to separately activate the device Interrupt (INT) output signal, when bit 3 of MCR is a logic 1. Its contents are indicated in Table 3-2 and are described below. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INT output from the device. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

3.8 SCRATCH PAD REGISTER

This 8-bit register does not control or report status on any part of the ACE. It is a read/write register that can be used by the programmer as a general purpose register.

3.9 FIFO CONTROL REGISTER

This write only register is located at the same address as the IIR (read only). This register is used to enable FIFO Mode, clear FIFOs, set the RCVR FIFO trigger levels, and select the mode of DMA signaling.

Bit 0: Writing a one to this bit enables the XMIT and RCVR FIFOs. When changing from Character Mode to FIFO Mode, data in the FIFOs does not automatically clear. Resetting FCR0 will clear all characters from RCVR Error FIFO. The FIFOs should be cleared immediately after changing to FIFO mode. This bit must be a 1 before writing to other FCR bits or they will not be programmed.

Bit 1: Writing a 1 to FCR1 will clear all bytes from RCVR Error FIFO and reset its counters to 0, and then self clear this bit to 0. The shift register and RCVR FIFO are not cleared.

Bit 2: Functions the same as bit 1, but for XMIT FIFO.

Bit 3: If FCR0 = 1, setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from Mode 0 to Mode 1 (see pin description of RXRDY and TXRDY).

Bits 4 and 5: Reserved for future use.

Bits 6 and 7: These bits control the trigger level of the RCVR FIFO interrupt.

7	6	RCVR FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

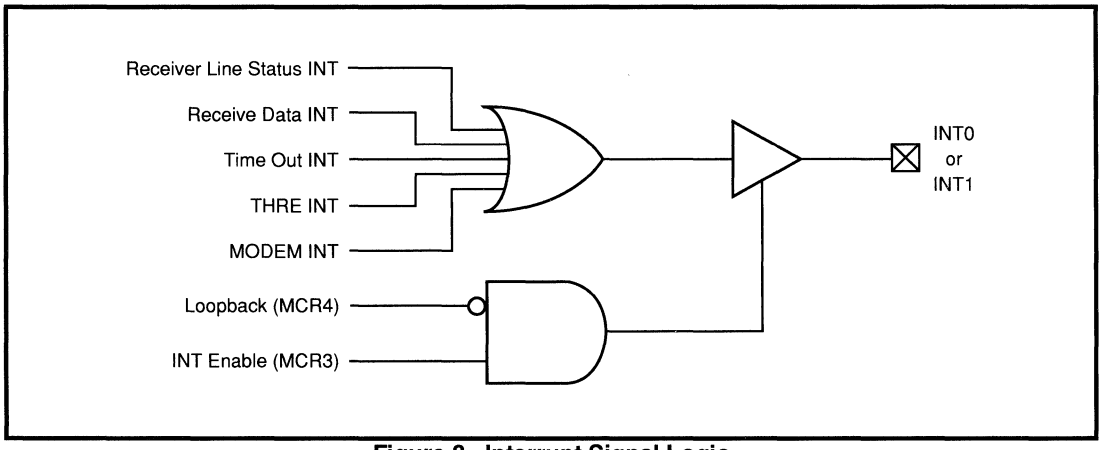


Figure 3. Interrupt Signal Logic

4.0 MODEM CONTROL REGISTER

This 8-bit register controls the interface either with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 3-2.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

> NOTE:
> The $\overline{DTR}$ output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: No connect. In loopback mode this bit is connected to the MODEM Status Register bit 6.

Bit 3: This bit enables the INT output pin. When this bit is a logic 0 the INT output pin is tri-stated. In loopback mode this bit is connected to bit 7 of the MODEM Status Register.

Bit 4: This bit provides a loopback feature for diagnostic testing of the ACE. When bit 4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to a logic 1 (high) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control Inputs (CTS, DSR, RLSD, and RI) are disconnected; and the four MODEM Control bits (0-3) are internally connected to the four MODEM Control inputs. The INT output pin is tri-stated when in loopback mode. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The ACE MODEM interrupt system can be tested by writing into the lower four bits of the MODEM Status Register. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to a logic 0.

Bits 5 through 7: These bits are permanently set to a logic 0.

5.0 MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 3-2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input to the device has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSR input to the device has changed since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the device has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the RLSD input to the device has changed state.

NOTE: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send (CTS) input. This bit becomes equivalent to RTS of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 5: This bit is the complement of the Data Set Ready (DSR) input. This bit becomes equivalent to DTR of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 6: This bit is the complement of the Ring Indicator (RI) input. This bit becomes equivalent to Bit 2 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 7: This bit is the complement of the Received Line Signal Detect (RLSD) input. This bit becomes equivalent to Bit 3 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

FIFO Interrupt Mode Operation Notes:

When FCR0=1 and IER0=1 the following RCVR interrupts will occur:

1. A FIFO timed interrupt occurs when:

   a. There is at least one byte in the RCVR FIFO.

   b. No character has been received in 4 continuous character times (if 2 stop bits are being used the second one is included in this time delay).

   c. The most recent CPU read from the FIFO has exceeded 4 continuous character times.

The timeout counter is proportional to the baud rate. After a timeout interrupt, the interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

2. When the RCVR FIFO reaches its programmed trigger level, the receive data interrupt is set. This interrupt is cleared as soon as the FIFO level falls below the trigger level.

FIFO Pointer Notes:

The RCVR FIFO has an internal pointer that automatically points to the RCVR Data byte to be read and the associated Status byte. Reading the RCVR Data byte will increment the internal counter, whereas reading the Status byte will not. The Status byte should always be read prior to the Data byte associated with it.

FIFO Polling Mode Operation Notes:

This mode is initialized when FCR0=1 and IER0, IER1, IER2, and IER3 are all 0. In polling mode, the user can poll the LSR directly to check the transmitter and receiver status. Since the receiver and transmitter are controlled separately, either one or both can be in polling mode.

There is no trigger level reached or timeout condition indicated on the Interrupt pin in the FIFO Polling Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

6.0 PARALLEL PORT DESCRIPTION

The parallel port supports Centronics-type printers. When CS2 is low, the parallel port is selected allowing access to all parallel port control and status registers. (Refer to Tables 6-1 and 6-2.)

Register Descriptions:

Read Port Register

Bits 0 through 7: These bits correspond to the data on the parallel bus. This register is used to read the data from the parallel bus.

Read Status Register

Bits 0 through 1: These bits are set to a logic one.

Bit 2: This bit represents the status of the INT pin. This bit is only available in the WD16C552.

Bits 3 through 7: These bits represent the status of the corresponding pins. Refer to Table 6-2.

Read Control Register

Bits 0 through 3: These bits show the status of the corresponding pins. Refer to Table 6-2. NOTE: These values reflect the signal on the open drain outputs, not necessarily the value in the write control register.

A1	A0	IOR	IOW	REGISTER
0	0	0	1	Read Data
0	1	0	1	Read Status
1	0	0	1	Read Control
1	1	0	1	Invalid
0	0	1	0	Write Data
0	1	1	0	Invalid
1	0	1	0	Write Control
1	1	1	0	Invalid

Table 6-1. Parallel Port (CS2=0) Register Addresses

BIT NO.	READ PORT 0	READ STATUS 1	READ CONTROL 2	WRITE CONTROL 2	WRITE DATA 0
0	Data Bit 0	1	Strobe	Strobe	Data Bit 0
1	Data Bit 1	1	Autofd	Autofd	Data Bit 1
2	Data Bit 2	INT♦	Init	Init	Data Bit 2
3	Data Bit 3	Error	Slin	Slin	Data Bit 3
4	Data Bit 4	Slct	Irq Enb	Irq Enb	Data Bit 4
5	Data Bit 5	PE	1	DIR♦	Data Bit 5
6	Data Bit 6	Ack	1	1	Data Bit 6
7	Data Bit 7	Busy	1	1	Data Bit 7

(♦) These bits are only available in the WD16C552.

Table 6-2. Accessible Parallel Port Registers

Bit 4: This bit represents the status of INT2 being enabled. INT2 is enabled when this bit is set to one.

Bits 5 through 7: These bits always return to a logic one.

Write Port Register

Bits 0 through 7: These bits correspond to the data to be placed on the parallel bus. This register is used to write data to the parallel bus based on Table 6-3.

Write Control Register

Bits 0 through 4: Writing to these bits will set the output of the corresponding pins.

Bit 5: The Direction bit works in conjunction with the BIDEN pin to determine the direction of the parallel port data bus in extended mode, as described in the table below. This bit is only available in the WD16C552, and is a write only bit.

Port Mode	Port Direction	Pin 1 Biden	Direction Bit
Extended	Write	1	0
Extended	Write	0	X
Extended	Read	1	1
Compatible	Write	0	N/A
Compatible	Read	1	N/A

Table 6-3. Parallel Port Operation Modes

Register/ Signal	Reset Control	Reset State
Control	Master Reset	All bits low.
Data (Write)	Master Reset	All bits low.
Data (Read)	Master Reset	Data
Status	Master Reset	Bits 0-2 are high, Bits 3-7 are ERR, SLCT, PE, ACK and Busy inputs.
INT2	Master Reset	High Impedence.
$\overline{\text{SLIN}}$	Master Reset	High.
$\overline{\text{INIT}}$	Master Reset	Low.
$\overline{\text{AFD}}$	Master Reset	High.
$\overline{\text{STB}}$	Master Reset	High.

Table 6-4.Parallel Port Reset Control of Registers & Signals

7.0 TYPICAL APPLICATIONS

Figures 4 and 5 show how to use the ACE devices in a 80286 system and in a microcomputer system with a high-capacity data bus.

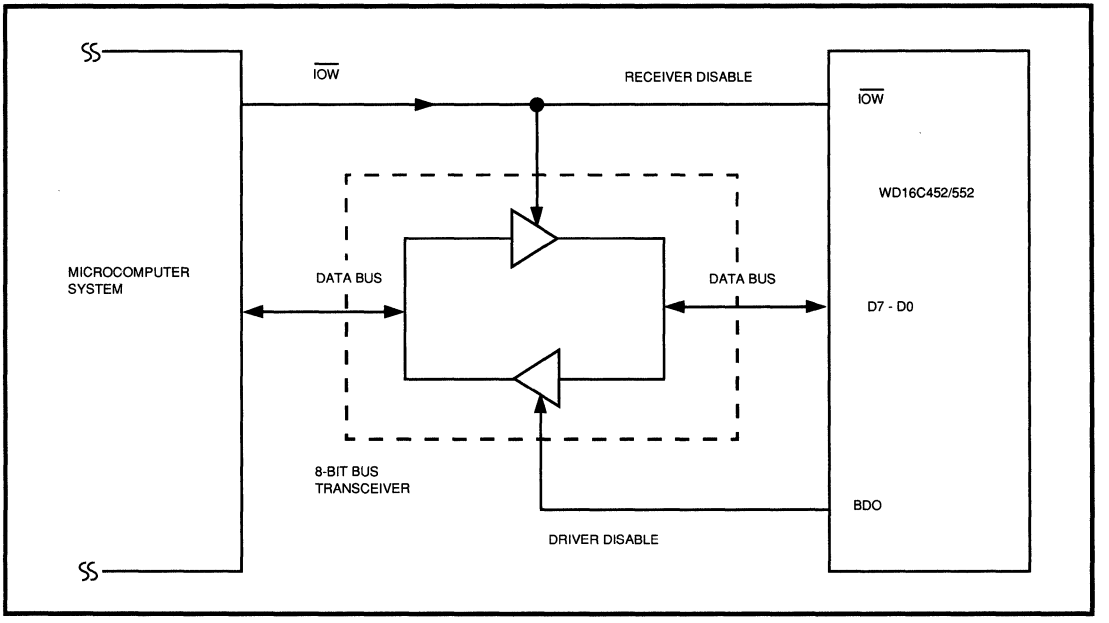


Figure 4. Typical Interface for a High-Capacity Data Bus

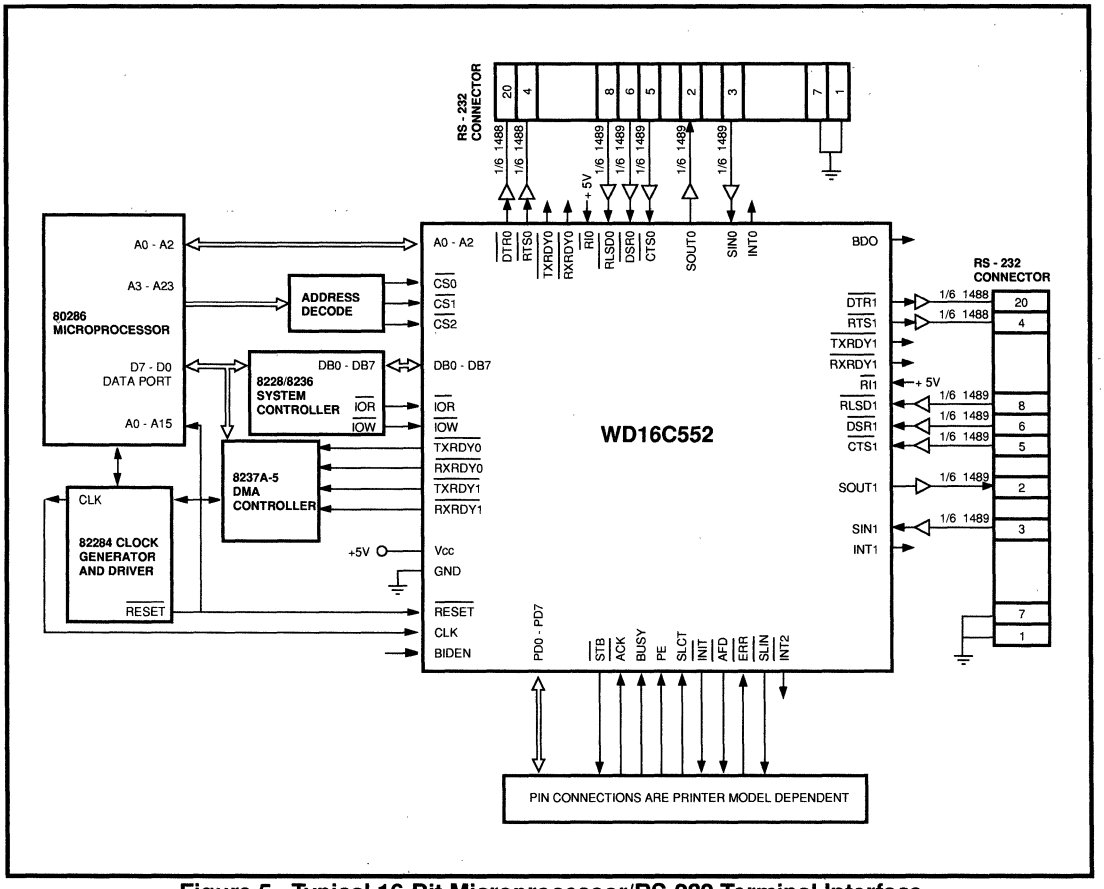


Figure 5. Typical 16-Bit Microprocessor/RS-232 Terminal Interface Using the WD16C552

APPENDIX A

A.O PIN DESIGNATIONS

Figure A-1 illustrates the 68-Pin QUAD assembly. Table A-1 lists all pin designations.

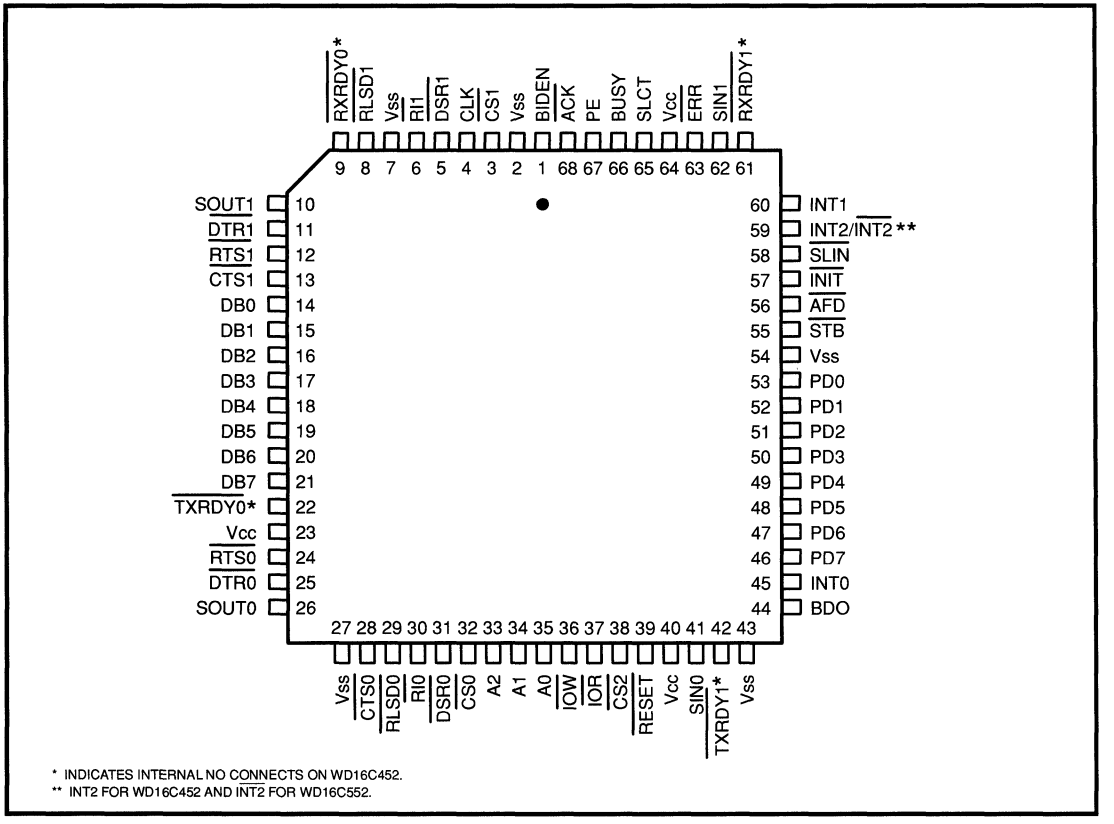


Figure A-1. WD16C452/WD16C552 68-Pin QUAD Assembly Pin Designations

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
1	BIDEN	Bidirectional enable	Input signal in the WD16C452, when low enables the parallel port data lines as outputs. When high the WD16C452 will hold the parallel port data pins in a high impedance state, allowing these pins to be driven with data. The BIDEN input signal on the WD16C552 works in conjunction with the DIR bit (see Table 6-3) to control the direction of the parallel port data bit.
2, 7, 27, 43, 54	Vss	Ground	System signal ground.
3	$\overline{CS1}$	Chip Select 1	Chip Select input when active (low), selects serial channel 1.
4	CLK (1 time)	Clock Input	External clock input.
5, 31	$\overline{DSR1}$, $\overline{DSR0}$	Data Set Ready	When low, this input signal from the communication link indicates that it is ready to exchange data with the associated ACE. Bit 5 of the associated MODEM Status Register reflects the logical state of DSR.
6, 30	$\overline{RI1}$, $\overline{RI0}$	Ring Indicator	Input when low indicates, for the associated ACE, a ringing signal is being received by the MODEM or data set. This logical value is reflected in bit 6 of the associated MODEM Status Register.
8, 29	$\overline{RLSD1}$, $\overline{RLSD0}$	Received Line Signal Detect	Input from the DCE indicating that the associated ACE is receiving a signal which meets its signal quality conditions. Bit 3 of the associated MODEM Status Register reflects this value.
9, 61	$\overline{RXRDY0}$♦, RXRDY1♦	Receiver Ready	Receiver ready output is used to signal DMA transfer to the CPU from the associated ACE. Two modes of operation are available when using FIFO Mode, and one (Mode 0) when using Character Mode.

(♦) These pins are internal no connects on the WD16C452.

Table A-1. Pin Designations

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
			Mode 0: When in Character Mode (FCR0=0), or in the FIFO Mode (FCR0=1) with FCR3=0, RXRDY will be active (low) if there is at least one character in the RCVR holding register or RCVR FIFO register. RXRDY will go inactive when the RCVR FIFO (FIFO Mode), or holding register (Character Mode) is empty. Mode 1: In FIFO Mode (FCR0=1) with FCR3=1, RXRDY will go active (low) when the trigger level or time out has been reached. RXRDY goes inactive (high) when the FIFO is empty.
10, 26	SOUT1, SOUT0	Serial Data Output	Transmitted Serial Data Out to the communication link from the associated ACE. The SOUT signal is set to a marking condition (logical 1) upon a Master Reset.
11, 25	$\overline{DTR1}$, $\overline{DTR0}$	Data Terminal Ready	Output when low informs the MODEM or data set that the associated ACE is ready to receive. This value is reflected in bit 0 of the MODEM Control Register.
12, 24	$\overline{RTS1}$, $\overline{RTS0}$	Request to Send	Output when low informs the MODEM or data set that the associated ACE is ready to transmit data. This value is reflected in bit 1 of the MODEM Control Register.
13, 28	$\overline{CTS1}$, $\overline{CTS0}$	Clear to Send	Input from DCE to the associated ACE indicating remote device is ready to transmit. This value is reflected in bit 4 of the MODEM Status Register.
14 thru 21	DB0-DB7	Data Bits	Tri-state, bidirectional communication lines between the ACE and Data Bus. D0 is the least significant bit (LSB) and the first serial transmitted or received bit.
22, 42	$\overline{TXRDY0}$♦, $\overline{TXRDY1}$♦	Transmitter Ready FIFO Control	Transmit ready output is used to signal DMA transfer to the CPU from the associated ACE. Two modes of operation are available when using FIFO Mode, and one (Mode 0) when using Character Mode.

(♦) These pins are internal no connects on the WD16C452.

Table A-1. Pin Designations (Contd)

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
			Mode 0: In Character Mode (FCR0=0) or in FIFO Mode (FCR0=1) with FCR3=0, TXRDY will be active (low) if there are no characters in the Xmit FIFO (FIFO Mode) or Xmit holding register (Character Mode). TXRDY will go inactive after the first character is loaded. Mode 1: In FIFO Mode (FCR0=1) with FCR3=1, if there is one, or more, unfilled position in the Xmit FIFO TXRDY will be active (low). TXRDY will go inactive when the FIFO is completely full.
23, 40, 64	Vcc	Power Supply	+5V power supply.
32	CS0	Chip Select 0	Chip Select input when active (low) selects serial channel 0.
33 thru 35	A2, A1, A0	Address lines A2-A0	These three inputs are used to select an internal register of the ACE, or parallel port.
36	IOW	Input/Output Write Strobe	Input when active (low), causes data from the data bus (DB0-DB7) to be input to the selected port's addressed register. The data will be written to the register chosen by A0-A2 and the port is chosen by CS0, CS1, or CS2 to be ACE#1, ACE#2, or parallel port (respectively).
37	IOR	Input/Output Read Strobe	Input active (low) will display data from the selected internal register on the data bus DB0-DB7. The chip select line determines within which port the register being accessed resides, and A0-A2 choose the internal register to be read.
38	CS2	Chip Select 2	Chip Select input when active (low), enables the line printer port.
39	Reset	Reset	Input when active (low), will force the device into an idle mode in which all serial data activities are suspended. The device will remain in an idle state until programmed to begin data activities.

Table A-1. Pin Designations (Contd)

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
41, 62	SIN0, SIN1	Serial Data Inputs	Received Serial Data Input from the communication link to the associated ACE. Data on the serial data inputs are disabled when exercising loop back mode, and internally connected to their respective SIN lines.
44	BDO	Bus Buffer Output	Output goes active when either serial channel, or the parallel port is selected as an output. BDO is used to control the system bus driver device (74LS245).
45, 60	INT0, INT1	Serial Channel Interrupts	Tri-state output (enabled by bit 3 of MCR) goes high whenever an enabled interrupt is pending for the associated ACE. INT is reset when the pending interrupt(s) are serviced, or a Master Reset is performed.
46 thru 53	PD7-PD0	Parallel Data Bits	Bidirectional data port which provides parallel input and output to the system. The eight lines are held in a high impedance state when BIDEN is high.
55	$\overline{STB}$†	Line Printer Strobe	Output line, when active, provides the the line printer with a signal to latch the data currently on the parallel port.
56	$\overline{AFD}$†	Line Printer Autofeed	Output line, when active, provides a signal for the line printer to autofeed continuous form paper.
57	$\overline{INIT}$†	Line Printer Initialize	Output line to printer, when active (low), signals the line printer to begin an initialization routine.
58	$\overline{SLIN}$†	Line Printer Select	Output line, when active (low), selects the printer.
59	INT2/$\overline{INT2}$††	Interrupt Printer Port	Tri-state output enabled by bit 4 of WCR. For the WD16C452, INT2 goes active (high) on the rising transition of $\overline{ACK}$ and reset (low) on the falling transition of $\overline{ACK}$. For the WD16C552 INT2 goes active (low) on the rising edge of $\overline{ACK}$. $\overline{INT2}$ is reset (high) on the rising edge of $\overline{IOR}$, when reading the parallel port status register.

(†) These outputs are open drain with internal pull-ups.

(††) This pin is INT2 for WD16C452 and $\overline{INT2}$ for WD16C552.

Table A-1. Pin Designations (Contd)

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
63	$\overline{ERR}$	Line Printer Error	Input line from the line printer, informs the parallel port of an error by inputting an active low signal. Set low by the printer upon a deselect condition, PE, or other error condition.
65	SLCT	Line Printer Select	Input from the line printer that goes high when the line printer has been selected.
66	BUSY	Line Printer Busy	Input from the line printer that goes high when the line printer has an operation in progress.
67	PE	Line Printer Paper Empty	Input from the line printer goes high when the printer is out of paper.
68	$\overline{ACK}$	Line Printer Acknowledge	Input from line printer that goes low to confirm the data transfer from the WD16C552 to the printer was successful.

Table A-1. Pin Designations (Contd)

APPENDIX B

B.0 DC OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Temperature
Under Bias . . . . . .0°C (32°F) to 70°C (158°F)

Storage Temperature . . . . . .-65°C (-85°F) to +150°C (302°F)

All Input or Output Voltages
with respect to Vss . . . . . .-0.5V to +7.0V

Power Dissipation WD16C452/WD16C552 . . . . . .300 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Operating Characteristics.

9

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 MIN	MAX	UNITS	TEST CONDITIONS
Vilx	Clock Input Low Voltage	-0.5	0.8	V	
Vihx	Clock Input High Voltage	2.0	Vcc	V	
Vil	Input Low Voltage	-0.5	0.8	V	
Vih	Input High Voltage	2.0	Vcc	V	
Vol	Output Low Voltage		0.4	V	Iol = 4.0 mA on DB0-DB7. Iol = 24 mA on PD0-PD7. Iol = 20 mA on INIT, STB , SLIN, AFD (NOTE). Iol = 2.0 mA on other outputs.
Voh	Output High Voltage	2.4		V	Ioh = -0.4 mA on DB0-DB7. Ioh = -15.0 mA on PD0-PD7. Ioh = -0.55 mA on INIT, AFD, STB, SLIN. Ioh= -0.2 mA on other outputs.
Icc	Power Supply Current		60	mA	Vcc = 5.25V, no loads on outputs: SIN0, SIN1, DSR0, DSR1, RLSD0, RLSD1, CTS0, CTS1, RI0, RI1 = 2.0V. Other inputs = 0.8V. Baud Rate = 512K. BRG = 8 MHz.
Iil	Input Leakage		±10	µA	Vcc = 5.25V, Vss = 0.0V. All other pins float.
Icl	Clock Leakage		±10	µA	Vin = 0.0V, 5.25V.
Idl	Data Bus Leakage		±10	µA	Vout = 0.4V, Vout = 4.6V Data Bus in High Impedance State.
Ioz	3 State Leakage		± 20	µA	Vcc = 5.25V, GND = 0V, Vout = 0.0V, 5.25V.
Vil (RES)	Reset Schmitt Vil		0.8	V	
Vih (RES)	Reset Schmitt Vih	2.0		V	

NOTE:
The SLIN, AFD, STB and INIT outputs are all open collector with 2.5K to 3.5K Ohms internal pull-up resistors. When in Vol state, each input will sink a minimum of 20 mA. The internal pull-ups generate 2.0 mA of internal Iol.

Table B-1. DC Operating Characteristics
Ta = 0°C (32°F) to =70°C (158°F), Vcc = +5V ± 5%, Vss = 0V, unless otherwise specified.

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 TYP	MAX	UNITS	TEST CONDITIONS
Cin	Input Capacitance	6	10	pF	Unmeasured Pins Returned to Vss
Cout	Output Capacitance	10	20	pF	Unmeasured Pins Returned to Vss

Table B-2. Capacitance
Ta = 25°C (77°F), f = 1.0 MHz, Vcc = Vss = 0V

APPENDIX C

C.0 AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

Ta = 0°C (32°F) to +70°C (158°F), Vss = +5V ± 5%

C.1 TIMING DIAGRAMS

FIGURE NUMBER	TITLE
C-1	Receiver Timing
C-2	Transmitter Timing
C-3	MODEM Control Timing
C-4	Read Cycle Timing
C-5	Write Cycle Timing
C-6	RCVR FIFO Signaling Timing for First Byte
C-7	RCVR FIFO Signaling Timing after First Byte (RBR already set)
C-8	Receiver DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
C-9	Receiver DMA Mode 1 Timing (FCR0 = 1 and FCR3 = 1)
C-10	Transmitter DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
C-11	Transmitter DMA Mode 1 (FCR3 = 1)
C-12	Parallel Port Timing
C-13	WD16C452 Parallel Port Interrupt Timing
C-14	WD16C552 Parallel Port Interrupt Timing

Table C-1. WD16C452/WD16C552 Timing Diagrams

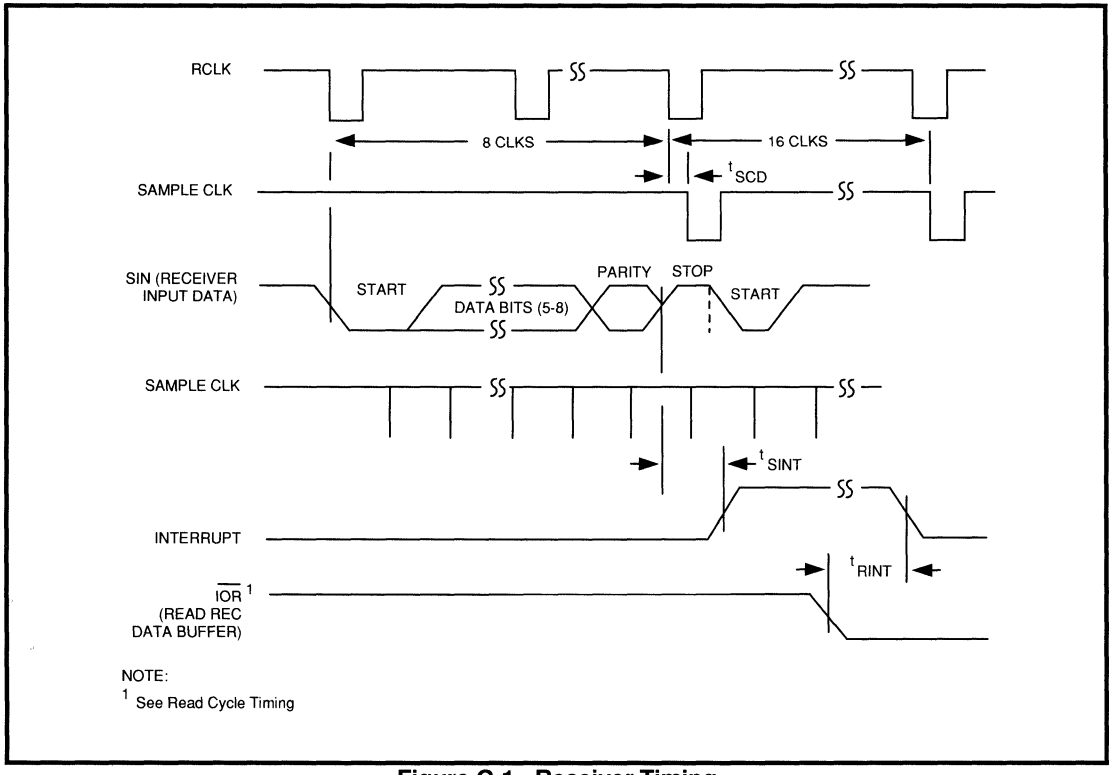


Figure C-1. Receiver Timing

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 MIN	MAX	UNITS	TEST CONDITIONS
tSCD	Delay from RCLK† to Sample Time		2	µs	
tSINT	Delay from Stop to Set Interrupt		17♦	RCLK† Cycles	100 pF Load
tRINT	Delay from IOR (RD RBR) Reset Interrupt		1	µs	100 pF Load

(♦) When receiving the first byte in FIFO Mode, tSINT (only for timeout or trigger level interrupt) will be delayed 19 RCLK cycles, except for a timeout interrupt where tSINT will be delayed 24 RCLK cycles.

(†) RCLK is an internal clock used for sampling serial in data.
RCLK is equivalent to 16 times the baud rate clock.

Table C-2. Receiver Timing

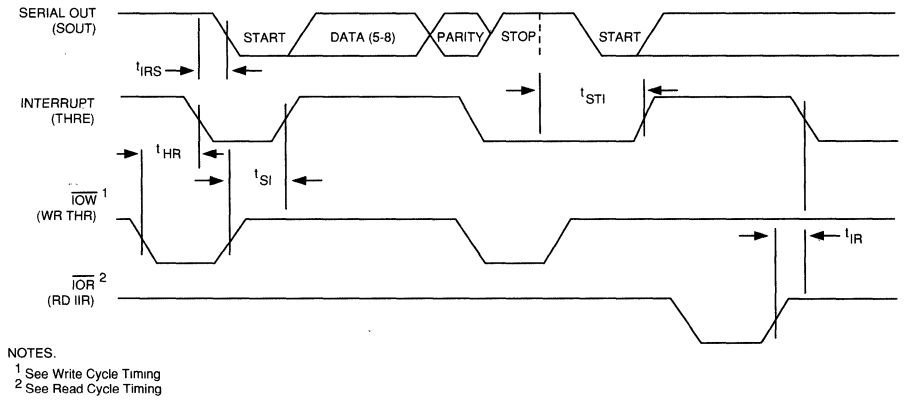


Figure C-2. Transmitter Timing

WD16C452/WD16C552

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
^{t}HR	Delay from IOW (WR THR) to Reset Interrupt		175	ns	100 pF Load
^{t}IRS	Delay from Initial INTR Reset to Transmit Start	8	24	TCLK† Clock Cycles	
^{t}SI*	Delay from Initial Write to Interrupt	16	24	TCLK† Clock Cycles	
^{t}STI	Delay from Stop to Interrupt (THRE)	8	8	TCLK† Clock Cycles	
^{t}IR	Delay from IOR (RD IIR to Reset Interrupt (THRE)		250	ns	100 pF Load
^{t}SXA	Delay from Start to TXRDY Active	0	8	TCLK† Clock Cycles	
^{t}WXI	Delay from Write to TXRDY Inactive	0	300	ns	

(†) TCLK is an internal clock used for sending serial out data. TCLK is equivalent to 16 times the baud rate clock.

(*) In FIFO mode, ^{t}SI might extend to beginning of the Stop bit. See Line Status Register for details.

Table C-3. Transmitter Timing

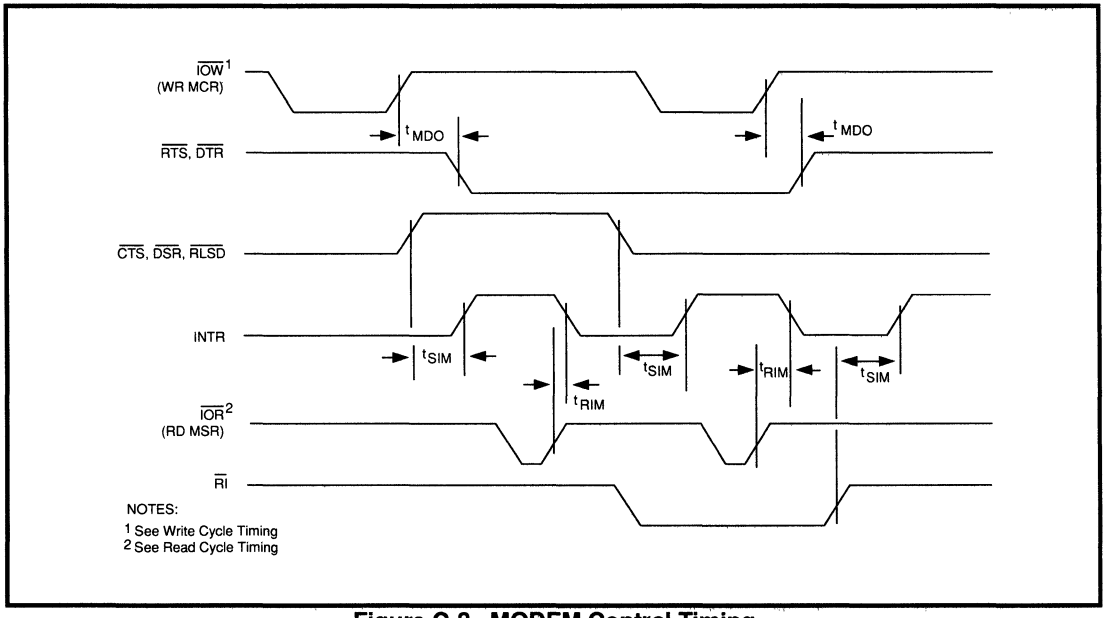


Figure C-3. MODEM Control Timing

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 MIN	MAX	UNITS	TEST CONDITIONS
^tMDO	Delay from $\overline{IOW}$ (WR MCR) to Output		200	ns	100 pF Load
^tSIM	Delay to Set Interrupt from MODEM Input		250	ns	100 pF Load
^tRIM	Delay to Reset Interrupt from $\overline{IOR}$ (RD MSR)		250	ns	100 pF Load

Table C-4. MODEM Control Timing

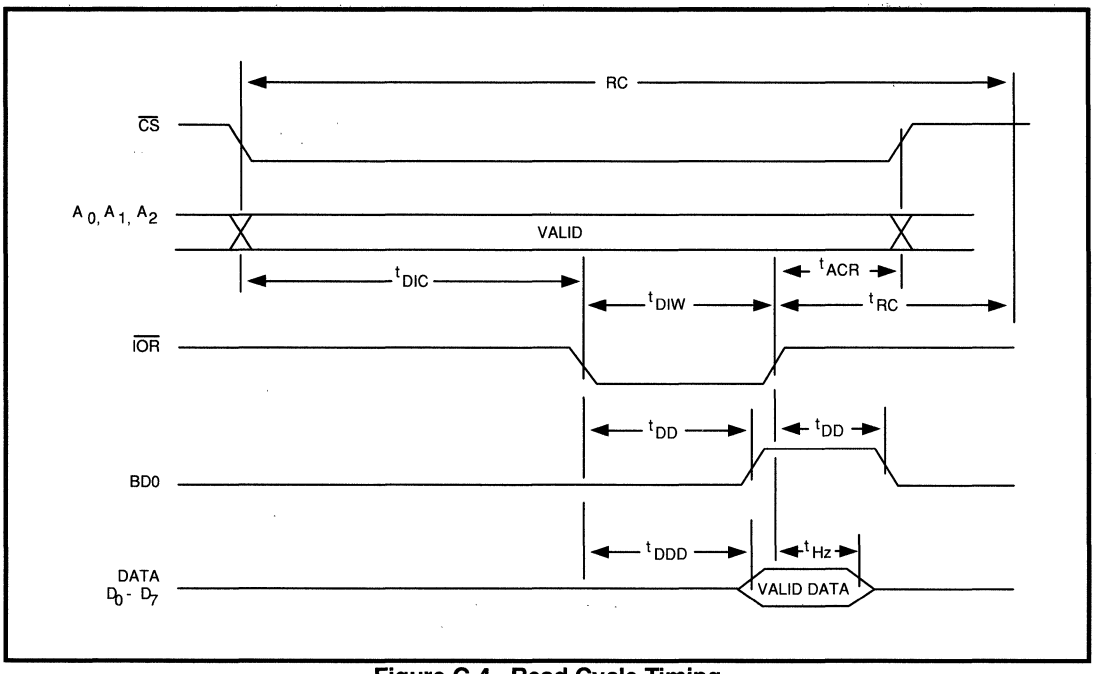


Figure C-4. Read Cycle Timing

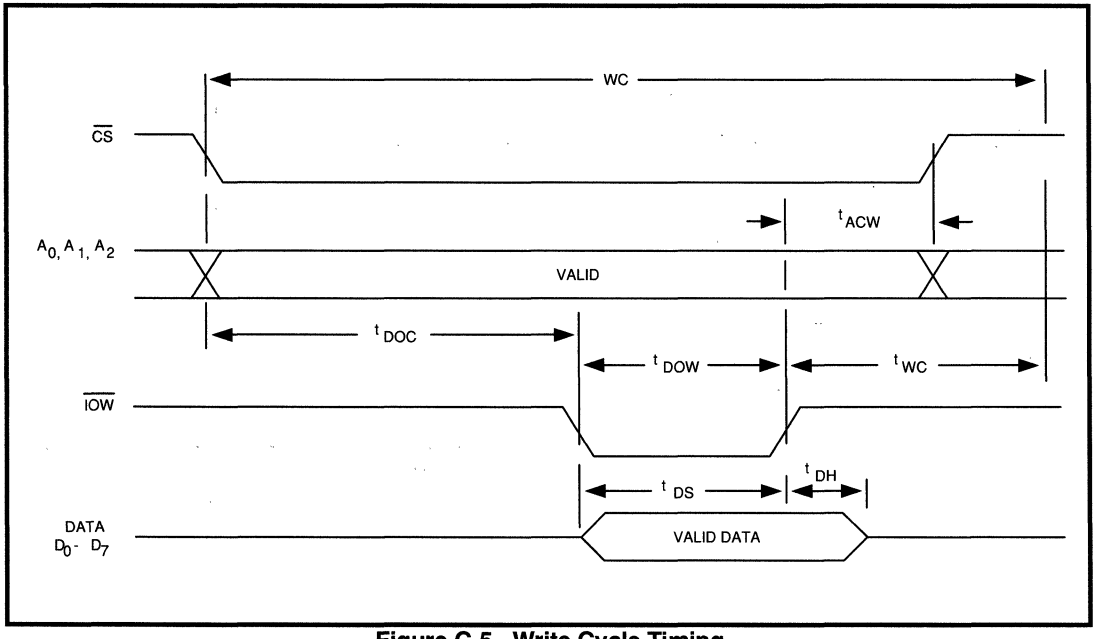


Figure C-5. Write Cycle Timing

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 MIN	MAX	UNITS	TEST CONDITIONS
t_{DIW}	$\overline{IOR}$ Strobe Width	125		ns	1TTL Load
t_{RC}	Read Cycle Delay	125		ns	1TTL Load
RC	Read Cycle = t_{DIC} + t_{DIW} + t_{RC} + 20 nsec	280		ns	1TTL Load
t_{DD}	$\overline{IOR}$ to Driver Enable (BDO) Delay		60	ns	1TTL Load
t_{DDD}	Delay from $\overline{IOR}$ to Data		100	ns	1TTL Load
t_{HZ}	$\overline{IOR}$ to Floating Data Delay	0	100	ns	1TTL Load
t_{DOW}	$\overline{IOW}$ Strobe Width	100		ns	1TTL Load
t_{WC}	Write Cycle Delay	150		ns	1TTL Load
WC	Write Cycle = + t_{DOC} + t_{DOW} + t_{WC} + 20 nsec	280		ns	1TTL Load
t_{DS}	Data Setup Time	30		ns	1TTL Load
t_{DH}	Data Hold Time	30		ns	1TTL Load
t_{DIC}	$\overline{IOR}$ DELAY from Select or Address	30		ns	1TTL Load
t_{DOC}	$\overline{IOW}$ Delay from Select or Address	30		ns	1TTL Load
t_{ACR}	Address and Chip Select Hold Time from $\overline{IOR}$	20		ns	1TTL Load
t_{ACW}	Address and Chip Select Hold Time from $\overline{IOR}$	20		ns	1TTL Load
t_{MR}	Master Reset Pulse Width	5.0		µs	1TTL Load
t_{XH}	Duration of Clock HIGH Pulse	55		ns	
t_{XL}	Duration of Clock LOW Pulse	55		ns	External Clock (8.0 MHz Max.)

Table C-5. Read/Write Cycle Timing

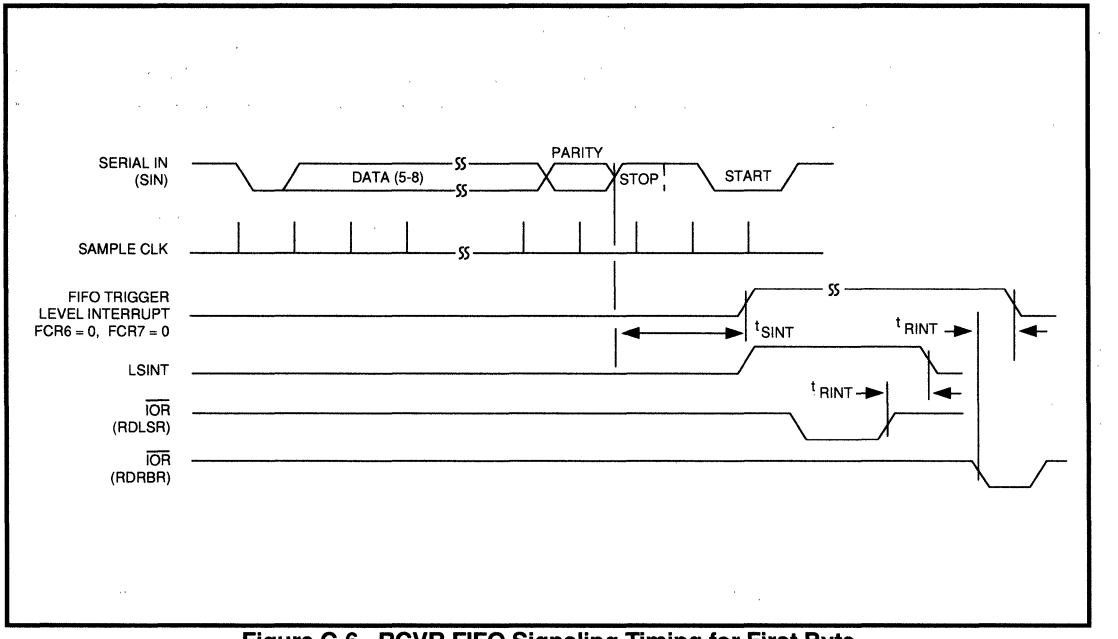


Figure C-6. RCVR FIFO Signaling Timing for First Byte

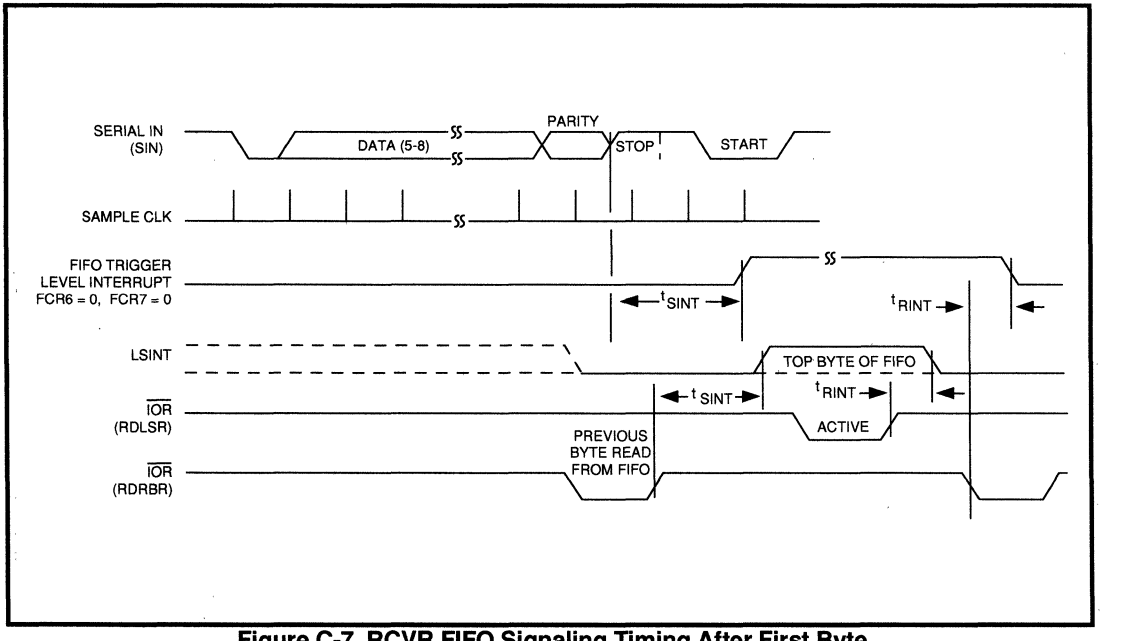


Figure C-7. RCVR FIFO Signaling Timing After First Byte (RBR Already Set)

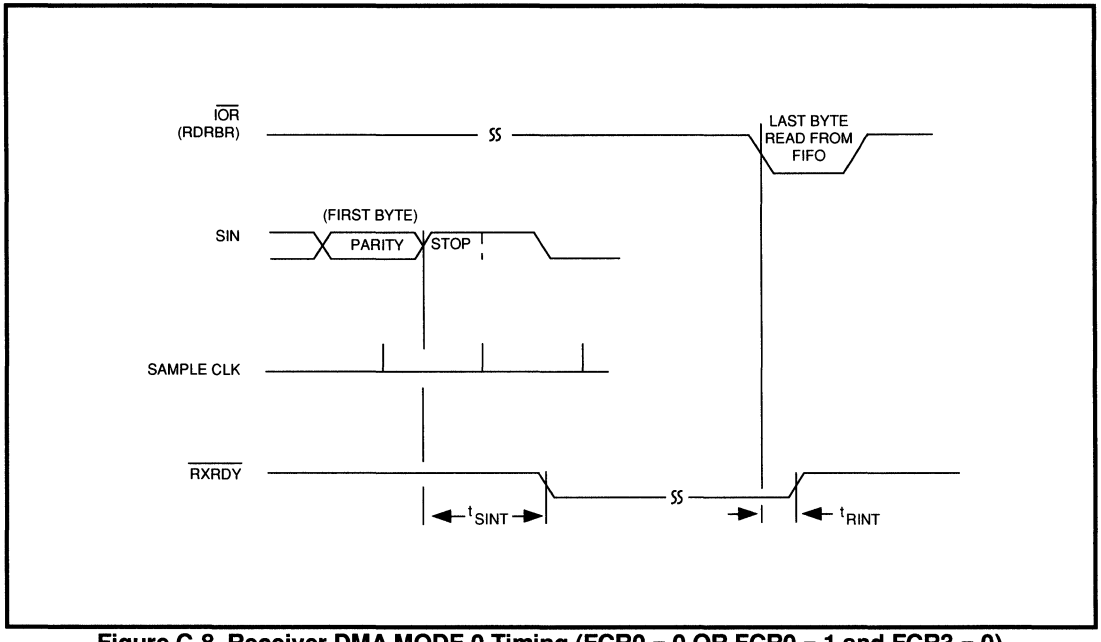


Figure C-8. Receiver DMA MODE 0 Timing (FCR0 = 0 OR FCR0 = 1 and FCR3 = 0)

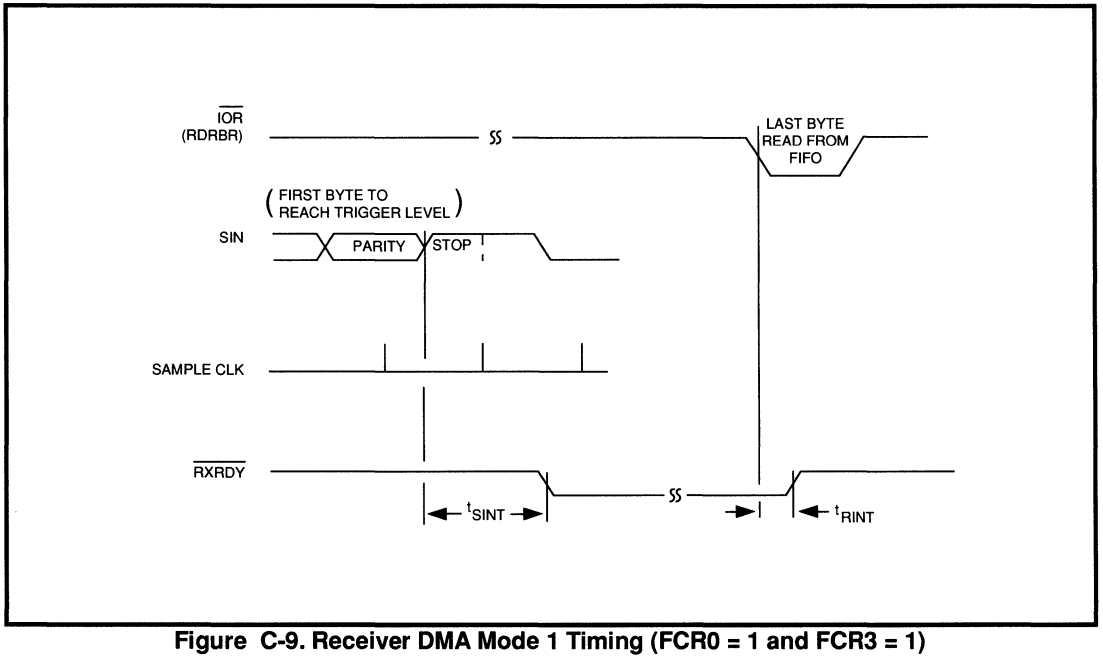


Figure C-9. Receiver DMA Mode 1 Timing (FCR0 = 1 and FCR3 = 1)

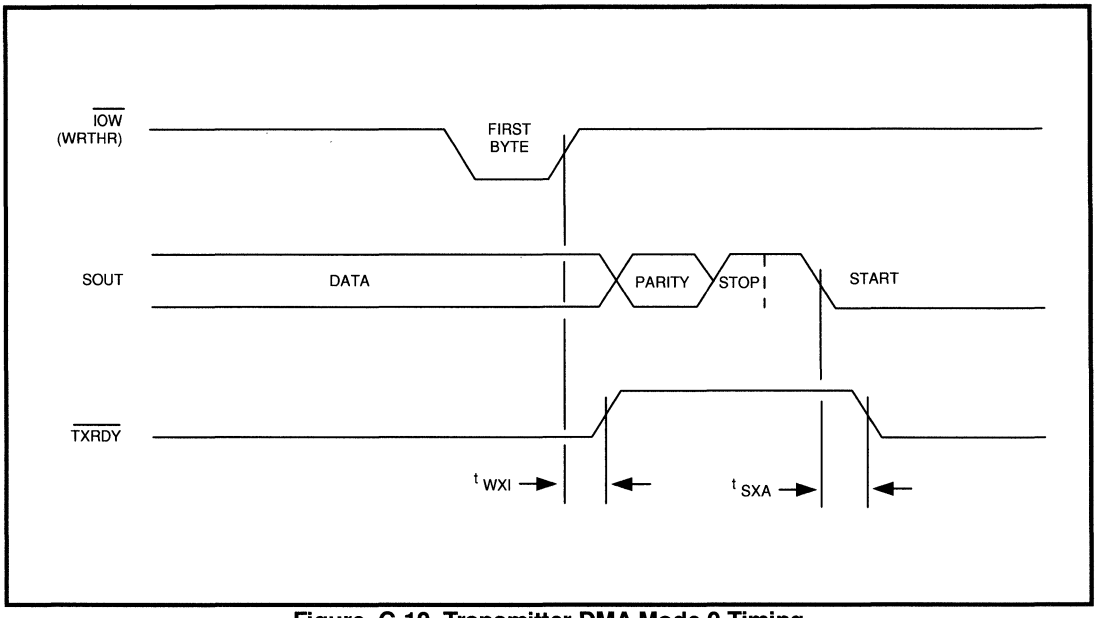


Figure C-10. Transmitter DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)

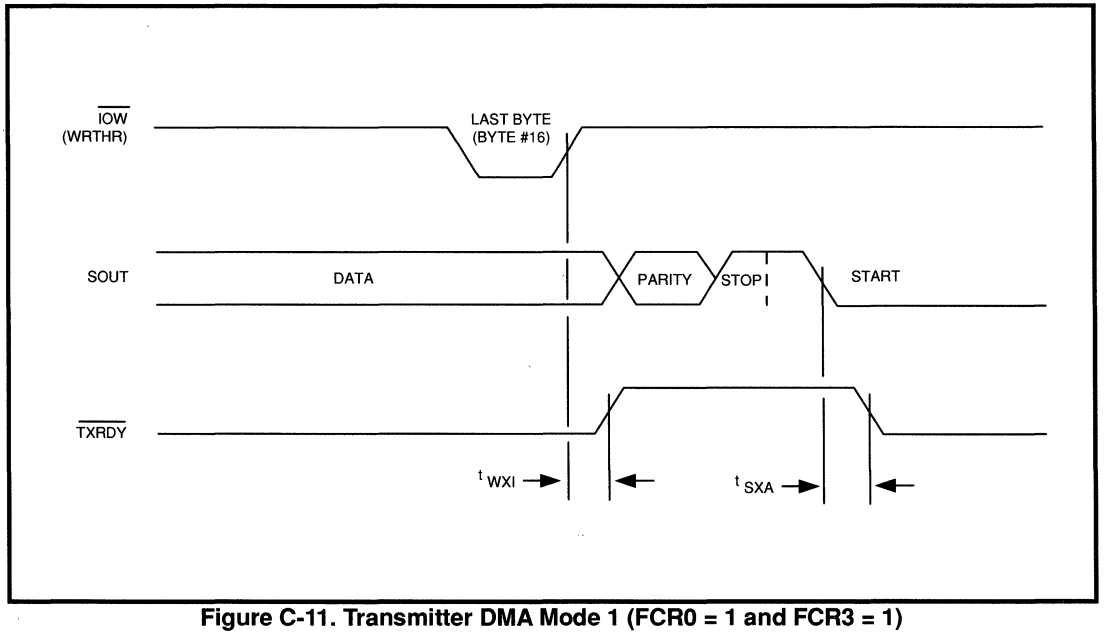
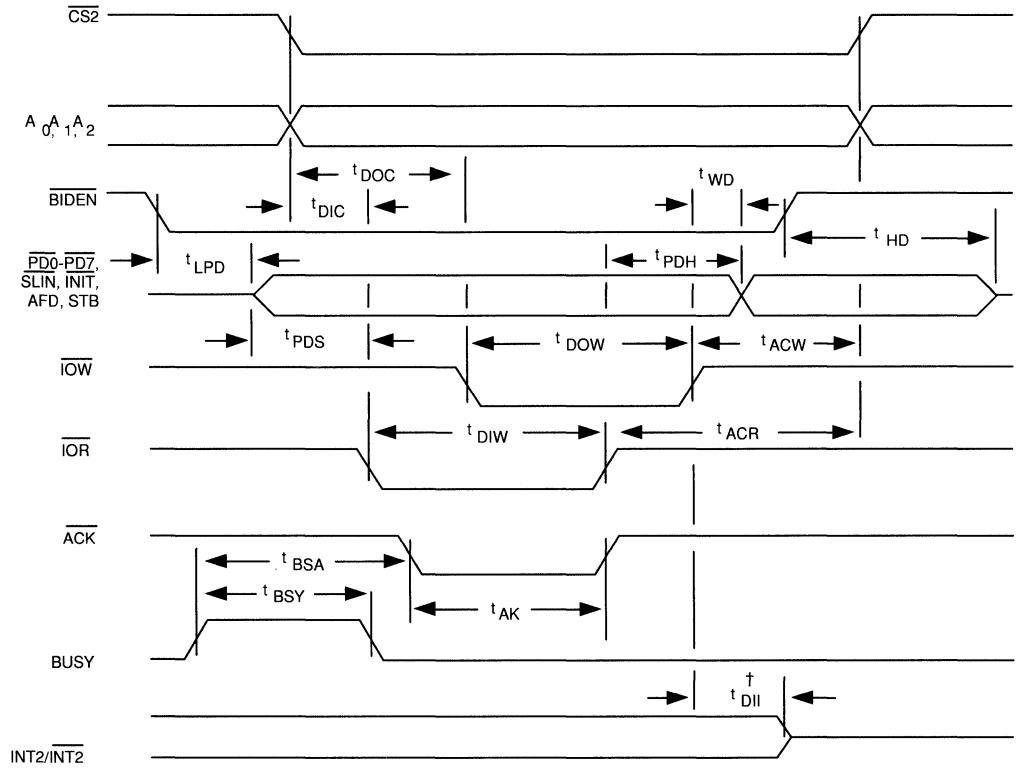


Figure C-11. Transmitter DMA Mode 1 (FCR0 = 1 and FCR3 = 1)



† t_{DII} is the delay from the positive transition of $\overline{IOW}$ only when the Write Cycle, bit 4 of the Write Control Register (IRQ Enable Bit) is low.

Figure C-12. Parallel Port Timing

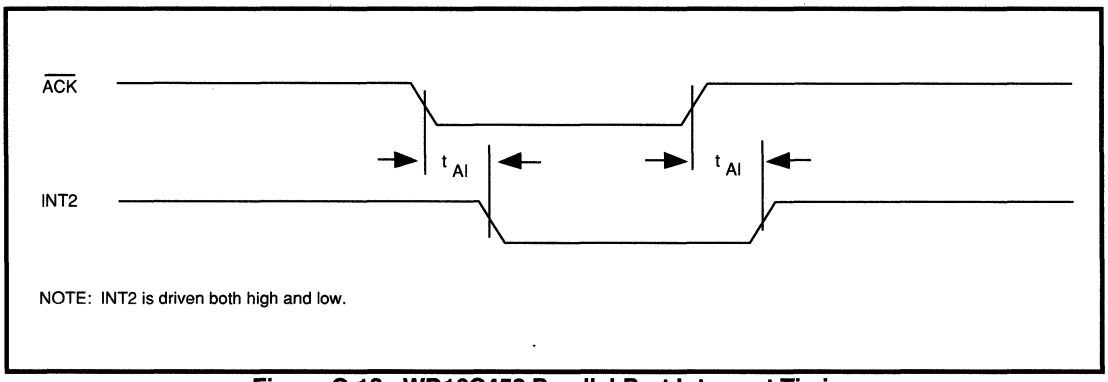


Figure C-13. WD16C452 Parallel Port Interrupt Timing

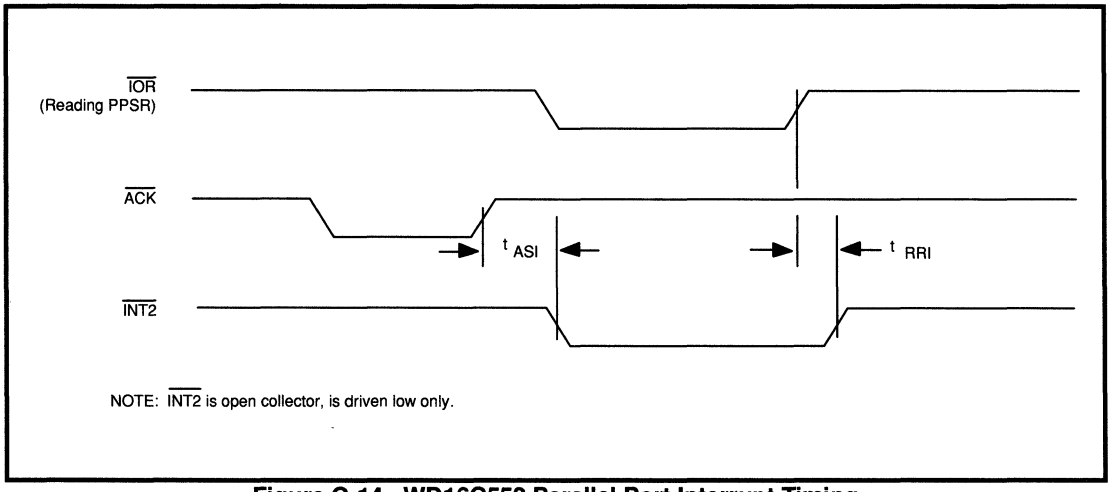


Figure C-14. WD16C552 Parallel Port Interrupt Timing

SYMBOL	CHARACTERISTIC	WD16C452/WD16C552 MIN	MAX	UNITS	TEST CONDITIONS
t_{DOC}	$\overline{IOW}$ Delay from Chip Select and Address	30		ns	
t_{DIC}	$\overline{IOR}$ Delay from Chip Select and Address	30		ns	
t_{WD}	$\overline{IOW}$ High to PD0-PD7, SLIN, $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$		1	µs	No External Pull-up Resistor and 50 pF Load
t_{HD}	$\overline{BIDEN}$ High to PD0-PD7 tri-state		120	ns	
t_{LPD}	$\overline{BIDEN}$ Low to PD0-PD7 Delay		100	ns	
t_{PDH}	PD0-PD7 Hold Time from $\overline{IOR}$	100		ns	
t_{PDS}	PD0-PD7 Set-up Time from $\overline{IOR}$	100		ns	
t_{DOW}	$\overline{IOW}$ Strobe Width	100		ns	
t_{DIW}	$\overline{IOR}$ Strobe Width	125		ns	
t_{ACW}	Chip Select and Address Hold Time from $\overline{IOW}$	20		ns	
t_{ACR}	Chip Select and Address Hold Time from $\overline{IOR}$	20		ns	
t_{BSA}	BUSY Start to $\overline{ACK}$			ms	Printer Dependent
t_{BSY}	BUSY Width			µs	Printer Dependent
t_{AK}	$\overline{ACK}$ Width			µs	Printer Dependent
t_{AI}	INT2 Delay from $\overline{ACK}$ (WD16C452)		60	ns	1 TTL Load
t_{ASI}	$\overline{ACK}$ to set interrupt (WD16C552)		60	ns	1 TTL Load
t_{RRI}	Read Parallel Port Status Register (PPSR) to reset INT2.		60	ns	1 TTL Load
tDII	$\overline{IOW}$ High to INT2/$\overline{INT2}$ tri-state	0	100	ns	1 TTL Load

Table C-6. Parallel Port Timing

APPENDIX D

D.0 PACKAGE DIAGRAM

Figure D-1 illustrates the 68-Pin QUAD plastic package showing dimensions in inches.

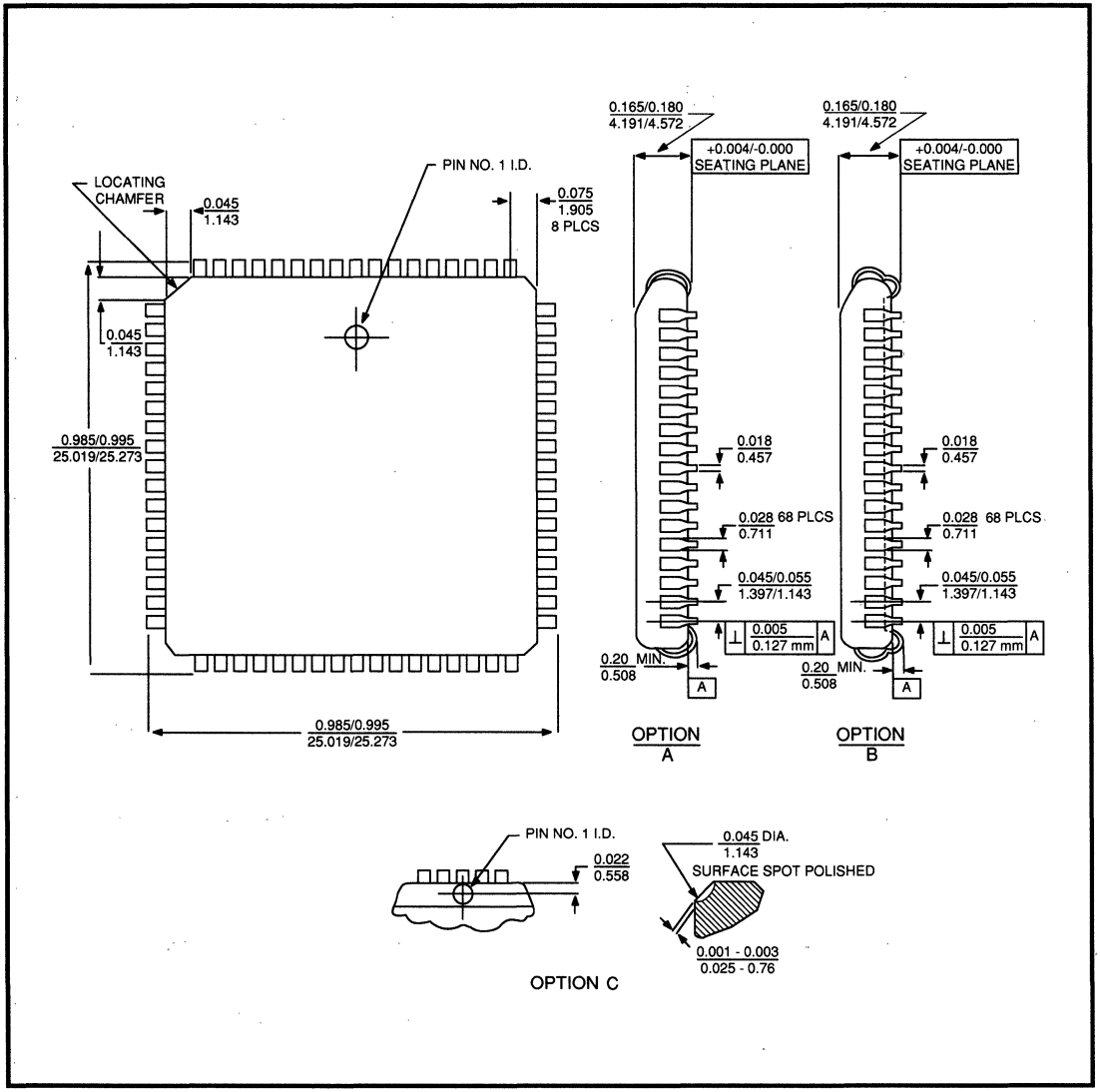


Figure D-1. 68-Pin QUAD Plastic Package

SYSTEMS LOGIC/PERIPHERAL

WD16C550

Enhanced Asynchronous Communications Element (ACE) with FIFOs

10

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

1.0 INTRODUCTION

1.1 DESCRIPTION

The WD16C550 is an enhanced programmable Asynchronous Communications Element (ACE) fabricated in CMOS silicon gate technology. The WD16C550 is fully compatible to the National NS16550A. Upon powerup the WD16C550 is functionally identical to the WD16C450 (Character Mode), and an alternate mode (FIFO Mode) can be activated through software to relieve the CPU of excessive overhead during high data rates due to interrupts.

1.2 FEATURES

- Designed to be easily interfaced to most 8-, 16-, and 32-bit microprocessors
- Generating and stripping of serial asynchronous data control bits (start, stop, parity)
- Provides 16-byte FIFO buffers on the transmitter and receiver for CPU relief during high speed data transfer
- FIFO or Character Modes are user selectable
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud rate generator allows division of any input clock by 1 to (2^{16} -1) and generates the internal clock
- Independent receiver 16X clock input
- MODEM interface capabilities
- Fully programmable serial-interface characteristics
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1 1/2-, or 2-stop bit generation
  - baud rate generation (dc to 512K baud)
- False start bit detector
- Complete status reporting capabilities
- Three-state TTL drive capabilities for bi-directional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities
  - Loopback controls for communication link fault isolation
- Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls
- Single +5 Volt power supply
- CMOS implementation for high speed and low power requirements
- Available in 40-Pin DIP and 44-Pin QUAD packages

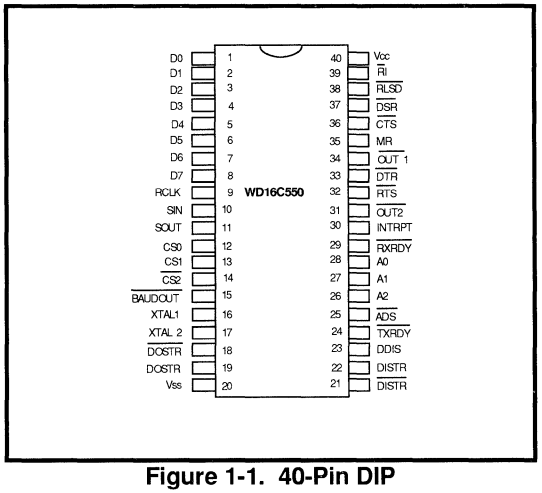


Figure 1-1. 40-Pin DIP

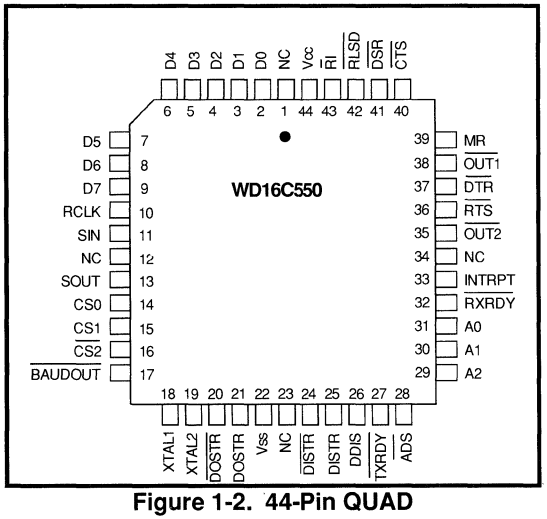


Figure 1-2. 44-Pin QUAD

1.3 GENERAL

The WD16C550 is an enhanced programmable Asynchronous Communications Element (ACE) with FIFOs (hereafter referred to as ACE) fabricated in CMOS silicon gate technology. The WD16C550 is fully compatible to the NS16550A. Upon powerup the WD16C550 is functionally identical to the WD16C450 (Character Mode), and an alternate mode (FIFO Mode) can be activated through software to relieve the CPU of excessive interrupt overhead during high data rates.
(Refer to figure 1-1.)

In FIFO Mode, internal 16-byte FIFOs (with an additional 3 error data bits per byte in the receiver FIFO) are located on the transmitter and receiver lines. Two FIFO control pins have been added for signaling of DMA transfers.

The ACE is a software-oriented device using a three-state, 8-bit, bi-directional data bus.

The ACE is used to convert parallel data to a serial format on the transmit side, and convert serial data to parallel on the receiver side. The serial format,in order of transmission and reception, is a start bit, followed by 5 to 8 data bits, a parity bit (if programmed) and 1-, 1 1/2- (5-bit format only), or 2-stop bits (all but the 5-bit format). The maximum recommended data rate is 512K baud.

Internal registers enable the user to program various types of interrupts, MODEM controls, and character formats. The user can read the status of the ACE at any time, monitoring word conditions, interrupts and MODEM status.

An additional feature of the ACE is a programmable baud rate generator capable of dividing a TTL signal clock by a divisor of 1 to (2^{16} - 1).

The ACE is designed to work in either a polling or interrupt driven system, which is programmable by user's software.

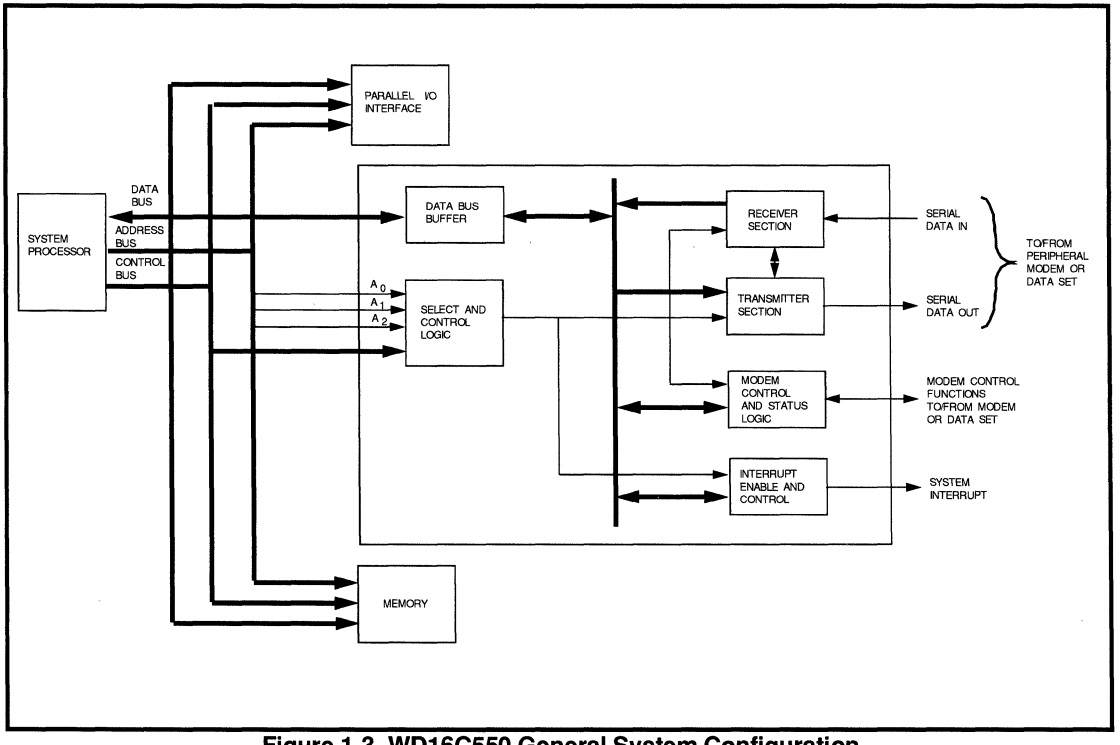


Figure 1-3. WD16C550 General System Configuration

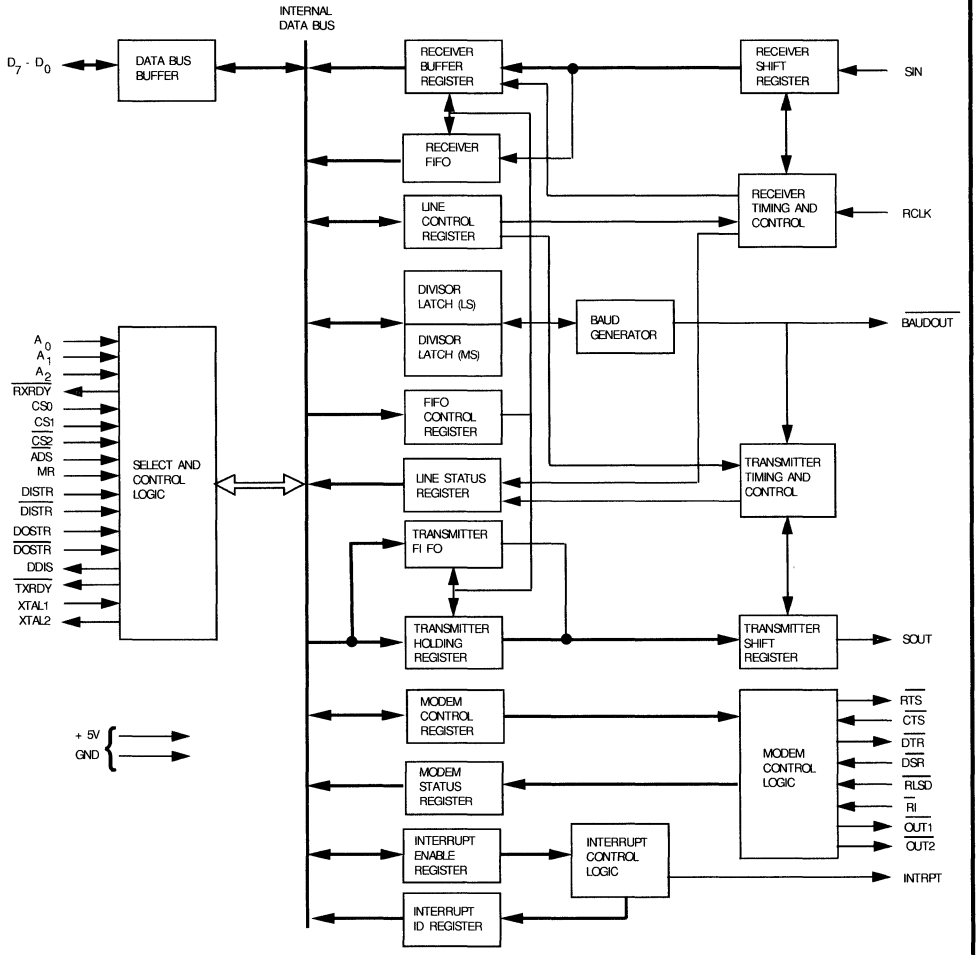


Figure 1-4. WD16C550 Block Diagram

2.0 CHIP SELECTION AND REGISTER ADDRESSING

2.1 ADDRESS STROBE ($\overline{ADS}$)

When low, provides latching for register select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$). (Refer to figure 1-2.)

NOTE:
The rising edge (↑) of the $\overline{ADS}$ input is required when Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals are not stable for the duration of a read or write operation. If $\overline{ADS}$ is required for latching, this input can be tied permanently low.

2.2 CHIP SELECT (CS0, CS1, $\overline{CS2}$)

The definition of a chip selected is CS0, CS1 both high and $\overline{CS2}$ low. Chip selection is complete when latched by ADS or $\overline{ADS}$ is tied low.

2.3 REGISTER SELECT (A0, A1, A2)

To select a register for read or write operation, see table 2-1.

NOTE:
Divisor Latch Access Bit (DLAB) is the MSB of the Line Control Register. DLAB must be programmed high (logic 1) by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	0	FIFO Control (write only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status (read only)
X	1	1	0	MODEM Status
X	1	1	1	Scratch Pad
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Table 2-1. Register Addressing

3.0 ACE OPERATIONAL DESCRIPTION

3.1 MASTER RESET

A high-level input on this pin causes the ACE to reset to the condition listed in table 3-1.

3.2 ACE ACCESSIBLE REGISTERS

The system programmer has access to any of the registers as summarized in table 3-2. For individual register descriptions, refer to the following pages under register heading.

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 Permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, and Bits 1-3, 6 and 7 are forced Low. Bits 4 and 5 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low (0-3 forced and and 4-7 Premanent)
Line Status Register	Master Reset	Bits 0-4 and 7 forced Low, Bits 5 and 6 forced High
MODEM Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low, Bits 4-7 - Input Signal
Divisor Latch (low order byte)	Writing into the Latch	Data
Divisor Latch (high order byte)	Writing into the Latch	Data
SOUT	Master Reset	High
$\overline{\text{BAUDOUT}}$	Writing into either Divisor Latch	Low
DDIS	DDIS = $\overline{\text{RCLK} \bullet \text{DISTR}}$ (At Master Reset, the CPU sets RCLK and DISTR low when device is selected.)	High
INTRPT (RCVR ERRS)	Master Reset/LSR	Low
INTRPT (RCVR DATA READY)	Master Reset/Read RBR	Low
$\overline{\text{OUT 2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT 1}}$	Master Reset	High
RCVR FIFO	MR or FCR1 • FCR0 or ΔFCR0	All Bits Low
XMIT FIFO	MR or FCR2 • FCR0 or ΔFCR0	All Bits Low
FIFO CONTROL	Master Reset	All Bits Low (Bits 0-3, 7 forced Low; Bits 4 and 5 Permanently Low)
D7 - D0 Data Bus Lines	In THREE-STATE Mode, Unless DISTR = HIGH or DOSTR = HIGH when device is selected	THREE-STATE Data (ACE to CPU) Data (CPU to ACE)

Table 3-1. Reset Control of Registers and Pinout Signals

10

	Register Address					
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending ID Bit 0 (IP)	FIFO Enable (Write Only) (FEWO)	Word Length Select Bit 0 (WLS0)
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 1 (IIDB0)	Rcvr FIFO Reset (RFR)	Word Length Select Bit 1 (WLS1)
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ERLSI)	Interrupt ID Bit 2 (IIDB2)	Transmitter FIFO Reset (TFR)	Number of Stop Bits (STB)
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit 3 (IIDB3)*	DMA Mode Select (DMS)	Parity Enable (PEN)
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)
5	Data Bit 5	Data Bit 5	0	0	Reserved	StickParity (STP)
6	Data Bit 6	Data Bit 6	0	FIFO Enabled* (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (LSB)(RTLSB)	Set Break Control (SBR)
7	Data Bit 7	Data Bit 7	0	FIFO Enabled* (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (MSB) (RTMSB)	Divisor Latch Access Bit (DLAB)

* These bits are 0 in Character Mode.

Table 3-2. Accessible WD16C550 Registers

	Register Address					
	4	5	6	7	0 DLAB=1	1 DLAB=1
Bit No.	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Pad Register	Divisor Latch (LSB)	Divisor Latch (MSB)
0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO* (EIRF)	Received Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

* These bits are 0 in Character Mode.

Table 3-2. Accessible WD16C550 Registers (Contd)

10

3.3 LINE CONTROL REGISTER

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 are as follows:

Bit 1	Bit 0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1-1/2 Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (Transmit data) or checked (Receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1's when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

3.4 ACE PROGRAMMABLE BAUD RATE GENERATOR

The ACE contains a programmable Baud Rate Generator capable of taking any clock input (dc to 8.0 MHz) and dividing it by any divisor from 1 to (2^{16} - 1). The output frequency of the Baud Generator is 16X the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3-3, 3-4, and 3-5 illustrate the use of the Baud Generator with three different driving frequencies. One is referenced to a 1.8432 MHz clock. Another is a 3.072 MHz clock. The third is an 8.0 MHz clock.

NOTE:
The maximum operating frequency of the Baud Generator is 8.0 MHz.

In no case should the data rate be greater than 512K baud.

See Crystal Specifications.

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Difference Between Desired and Actual
50	2304	--
75	1536	--
110	1047	0.026
134.5	857	0.058
150	768	--
300	384	--
600	192	--
1200	96	--
1800	64	--
2000	58	0.690
2400	48	--
3600	32	--
4800	24	--
7200	16	--
9600	12	--
19200	6	--
38400	3	--
56000	2*	2.860

Table 3-3. BAUD Rates Using 1.8432 MHz Clock

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Difference Between Desired and Actual
50	3840	--
75	2560	--
110	1745	0.026
134.5	1428	0.034
150	1280	--
300	640	--
600	320	--
1200	160	--
1800	107	--
2000	96	--
2400	80	--
3600	53	0.628
4800	40	--
7200	27	1.230
9600	20	--
19200	10	--
38400	5	--
5600	3*	14.285

Table 3-4. BAUD Rate Using 3.072 MHz Clock

* Smallest allowable divisor when using corresponding clock.

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Difference Between Desired and Actual
50	10000	--
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	--
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1*	2.344

Table 3-5. BAUD Rate Using 8.0 MHz Clock

* Smallest allowable divisor when using corresponding clock.

3.5 LINE STATUS REGISTER

This 8-bit read only register provides status information to the CPU concerning the data transfer. Its contents are indicated in table 3-2 and are described below.

Bit 0: This bit is the Receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register, or to the RCVR FIFO (when in FIFO Mode). Bit 0 will be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register (for Character Mode) or by writing a logic 0 into it from the CPU.

In FIFO Mode, Receiver Data Ready is set when the receiver shift register is loaded into the FIFO and reset when the receiver FIFO is empty.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode, an OE occurs after the RCVR FIFO is full and the receiver shift register has completely received the next character. An OE is indicated to the CPU as soon as it happens. The character in the shift register will be written over, but nothing will be transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to logic 0 whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode a parity error is associated with a particular character in the FIFO, and revealed to the CPU when the associated character is in the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop Bit. Bit 3 is set to a logic 1 whenever the Stop Bit following the last data bit or parity bit is detected as a zero bit (Spacing Level).

When in FIFO Mode, an FE is associated with a particular character in the FIFO, and revealed to the CPU when the associated character is in the top of the FIFO.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + data bits + Parity + Stop Bits).

When in FIFO Mode, BI is associated to the particular character in the FIFO, and this bit is set when the associated character is in the top of the FIFO.

NOTE:
Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and Receiver Line Status interrupt is enabled.

10

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

When in the FIFO Mode, this bit will be set when the XMIT FIFO is empty, and cleared after at least one character is written into the XMIT FIFO.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator and is a read-only bit. Bit 6 is set to a logic 1 when both transmitter registers (Transmitter Holding Register and Transmitter Shift Register) are idle (empty). It is reset to a logic 0 upon loading of data into the Transmitter Holding Register.

In FIFO Mode, this bit is set when the XMIT FIFO is empty. It is cleared when at least one byte is written into the XMIT FIFO.

Bit 7: This bit (LSR7) is 0 when in Character Mode. When in FIFO Mode, this bit is a one if there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when this register is read as long as there are no addition errors in the FIFO.

3.6 INTERRUPT IDENTIFICATION REGISTER

The ACE has an interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the Interrupt Identification Register (refer to table 3-2)

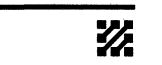
This register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Its contents are indicated in table 3-6 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 through 3: These three bits are used to identify the highest prioritiy interrupt pending (see table 3-6).

Bits 4 and 5: These bits are always logic 0.

Bits 6 and 7: These bits, when set, indicate that the device is in FIFO Mode (FCR0 = 1).



Interrupt Identification Register				Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	0	1	--	None	None	--
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
1	1	0	0	Second	Character Timeout Identification	No Characters have been input or removed from RCVR FIFO during the last 4 character times, and at least one character occupies it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Table 3-6. Interrupt Control Functions

3.7 INTERRUPT ENABLE REGISTER

This 8-bit register enables the four interrupt sources of the ACE to separately activate the chip Interrupt (INTRPT) output signal. Its contents are indicated in table 3-2 and are described below. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the device. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

3.8 SCRATCH PAD REGISTER

This 8-bit register does not control or report status on any part of the WD16C550. It is a read/write register that can be used by the programmer as a general purpose register.

3.9 FIFO CONTROL REGISTER

This write only register is located at the same address as the IIR (read only). This register is used to enable FIFO Mode, clear FIFOs, set the RCVR FIFO trigger levels, and select the mode of DMA signaling.

Bit 0: Writing a one to this bit enables the XMIT and RCVR FIFOs. When changing from Character Mode to FIFO Mode and vice versa, data in the FIFOs does not automatically clear. Resetting FCR0 will clear all characters from both FIFOs. The FIFOs should be cleared before changing modes. This bit must be a 1 before writing to other FCR bits or they will not be programmed.

Bit 1: Writing a 1 to FCR1 will clear all bytes from RCVR FIFO and reset its counters to 0, and then self clear this bit to 0. The shift register is not cleared.

Bit 2: Functions the same as bit 1, but for XMIT FIFO.

Bit 3: If FCR0 = 1, setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from Mode 0 to Mode 1 (see pin description of RXRDY and TXRDY).

Bits 4 and 5: Reserved for future use.

Bits 6 and 7: These bits control the trigger level of the RCVR FIFO interrupt.

7	6	RCVR FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

4.0 MODEM CONTROL REGISTER

This 8-bit register controls the interface either with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 3-2.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

> NOTE:
> The $\overline{DTR}$ output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxilliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the ACE. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to a logic 1 (high) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control Inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{RTS}$, $\overline{DTR}$, $\overline{OUT2}$, $\overline{OUT1}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The ACE MODEM interrupt system can be tested by writing into the lower four bits of the MODEM Status Register. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to a logic 0.

Bits 5 through 7: These bits are permanently set to a logic 0.

5.0 MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 3-2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input to the device has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSR input to the device has changed since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the device has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the RLSD input to the device has changed state.

NOTE:
Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send (CTS) input. This bit becomes equivalent to RTS of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 5: This bit is the complement of the Data Set Ready (DSR) input. This bit becomes equivalent to DTR of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 6: This bit is the complement of the Ring Indicator (RI) input. This bit becomes equivalent to OUT1 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

Bit 7: This bit is the complement of the Received Line Signal Detect (RLSD) input. This bit becomes equivalent to OUT2 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

5.1 FIFO OPERATION NOTES

FIFO Interrupt Mode Operation Notes:

When FCR0=1 and IER0=1 the following RCVR interrupts will occur:

1. A FIFO timeout interrupt will occur if the following is true:
   a. There is at least one byte in the RCVR FIFO.
   b. No character has been received in 4 continuous character times (if 2 stop bits are being used the second one is included in this time delay).
   c. The most recent CPU read from the FIFO has exceeded 4 continuous character times.

The timeout counter uses RCLK for an input to calculate character times; therefore, this delay is proportional to the baud rate. After a timeout interrupt, the interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

2. When the RCVR FIFO reaches its programmed trigger level the receive data interrupt is set. This interrupt is cleared as soon as the FIFO level falls below the trigger level.

FIFO Polling Mode Operation Notes:

This mode is initialized when FCR0=1 and IER0, IER1, IER2, and IER3 are all 0. In polling mode the user must poll the LSR to check the transmitter and receiver status. Since the receiver and transmitter are controlled separately either one or both can be in polling mode.

There is no trigger level reached or timeout condition indicated in the FIFO Polling Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

6.0 TYPICAL APPLICATIONS

Figures 6-1 and 6-2 show how to use the ACE device in an 80286 system and in a microcomputer system with a high-capacity data bus.

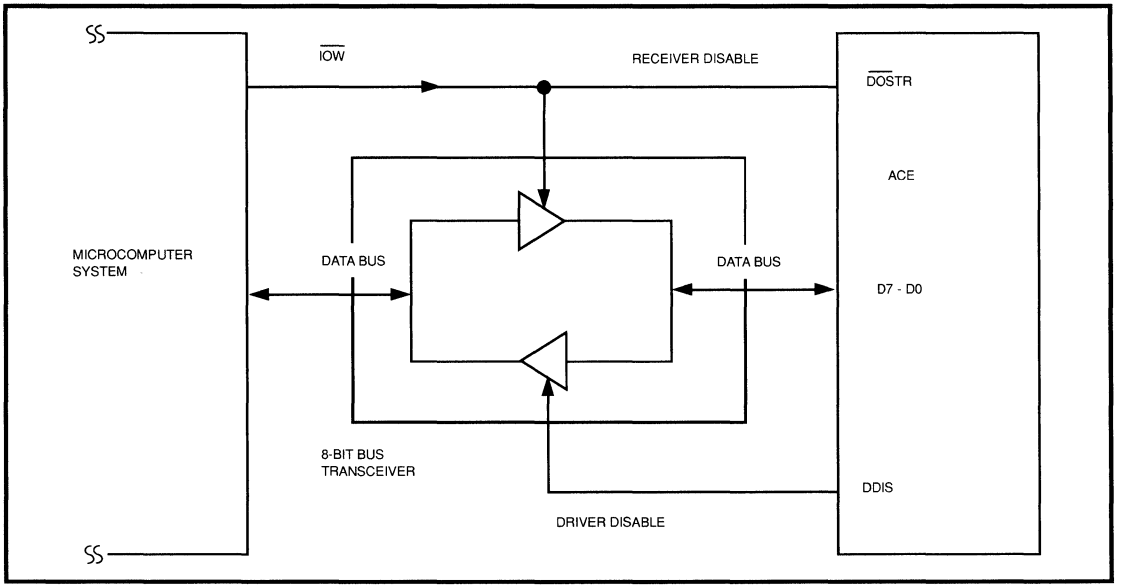


Figure 6-1. Typical Interface for a High-Capacity Data Bus

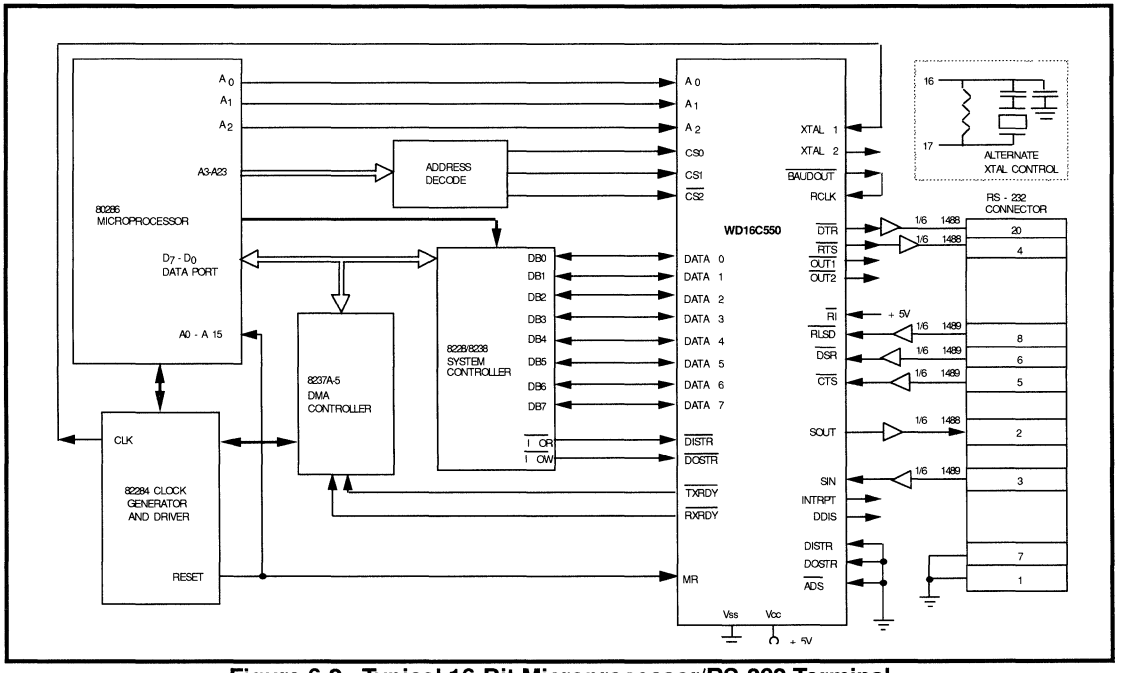


Figure 6-2. Typical 16-Bit Microprocessor/RS-232 Terminal Interface Using the ACE

7.0 CRYSTAL MANUFACTURERS (Partial List)

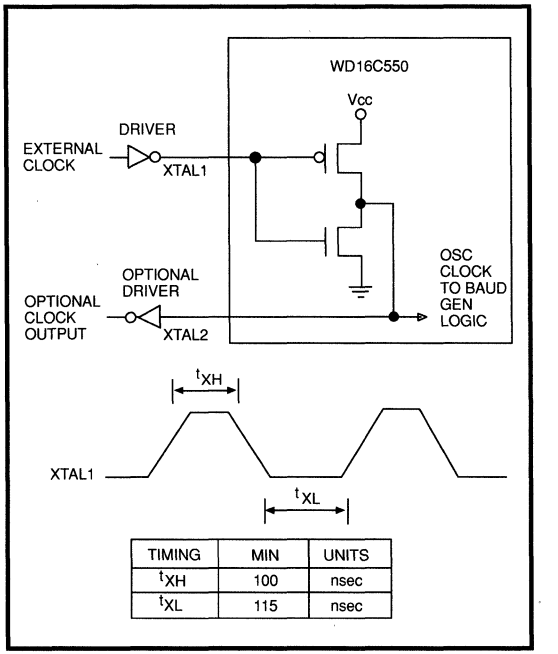
American Time Products Division
Frequency Control Products, Inc.
Woodside, New York 11377

Bliley Electric Company
Erie, Pennsylvania 16508

Cryster Crystals
Whitby, Ontario

Erie Frequency Control
Carlisle, Pennsylvania 17013

Q-Matic Corporation
Costa Mesa, California 92626



TIMING	MIN	UNITS
t_{XH}	100	nsec
t_{XL}	115	nsec

Figure 7-1. External Clock Input (8.0 MHz Max.)

CRYSTAL SPECIFICATIONS

Frequency: 1.8432 MHz, 3.072 MHz, and 8.0 MHz.
Type: Microprocessor Crystal

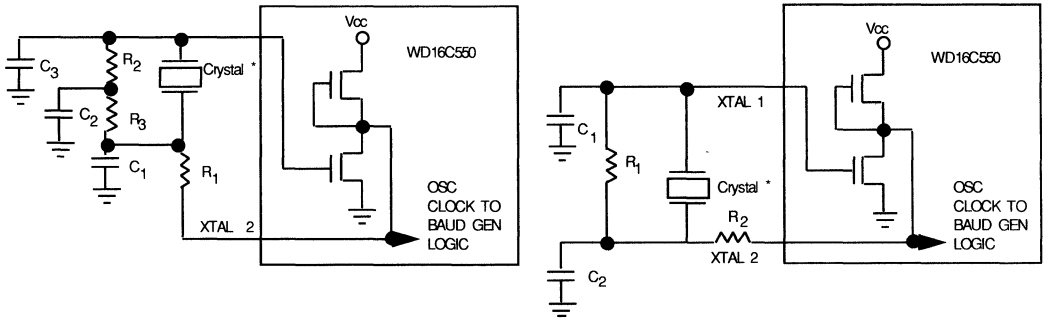
Temperature Range: 0°C(32°F) to + 70°C(158°F)

Series Resistance: 200 Ohms to 500 Ohms
(1.8432 MHz)

100 Ohms to 200 Ohms
(3.072 MHz)

20 Ohms to 40 Ohms
(8.0 MHz)

Series Resonant
Overall Tolerance: ±0.01%



Crystal	R_1	R_2	R_3	C_1	C_2	C_3
3.1 MHz	2K	0.5M	0.5M	40-60pF	0.01pF	10-30pF
1.8 MHz	2K	0.5M	0.5M	65-100pF	0.01pF	10-15pF

Crystal	R_1	R_2	C_1	C_2
8.0 MHZ	1 M?	1.68K	22pF	40pF
3.1 MHz	1 M?	1.5K	10-30pF	40-60pF
1.8 MHz	1 M?	1.0K	5-15pF	50-100pF

Figure 7-2. Typical Crystal Oscillator Networks

* See Crystal Specifications

APPENDIX A

A.0 PIN DESIGNATIONS

Figures A-1 and A-2 illustrate the 40 - Pin DIP and 44 - Pin QUAD assemblies. Table A - 1 lists all pin designations.

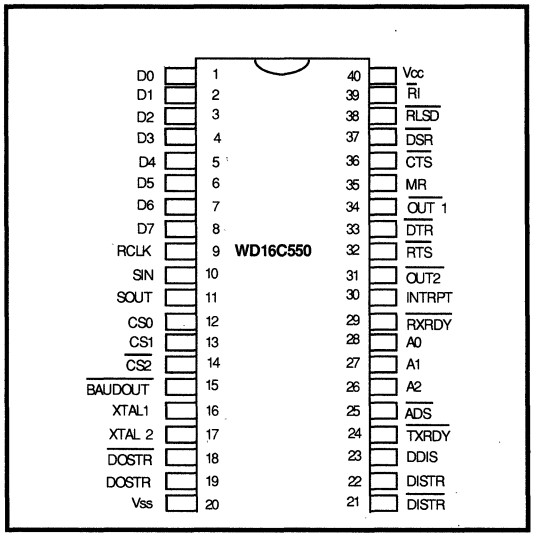


Figure A-1. WD16C550 40-Pin DIP Assembly Pin Designations

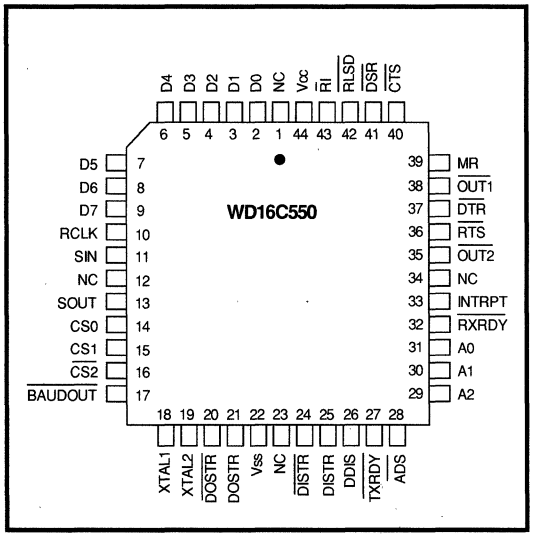


Figure A-2. WD16C550 44-Pin QUAD Assembly Pin Designations

PIN NUMBERS DIP	PIN NUMBERS QUAD	MNEMONIC	SIGNAL NAME	FUNCTION
1 thru 8	2 thru 9	D0 thru D7	DATA BUS	3-state, bi-directional communication lines between the ACE and Data bus. All prepared TX and assembled REC data, Control characters, and Status information are transferred via the data (D0-D7).
--	1	NC	NO CONNECTION	No Connection.
9	10	RCLK	RECEIVE CLK	This input is the 16X baud rate clock for the receiver section of the chip, may be tied to BAUDOUT (pin 15 for DIP package and/or pin 17 for QUAD package).
10	11	SIN	SERIAL INPUT	Received Serial Data In from the communications link (peripheral device, modem or data set).
--	12	NC	NO CONNECTION	No Connection
11	13	SOUT	SERIAL OUTPUT	Transmitted Serial Data Out to the communication link. The SOUT signal is set to a (logic 1) marking condition upon a MASTER RESET.
12	14	CS0	CHIP SELECT	When CS0 and CS1 are high, and CS2 is low, chip is selected. Selection is complete when the address strobe ADS latches the chip select signals.
13	15	CS1	CHIP SELECT 1	Same as CS0.
14	16	$\overline{CS2}$	$\overline{CHIP\ SELECT\ 2}$	Same as CS0.
15	17	$\overline{BAUDOUT}$	$\overline{BAUDOUT}$	16X clock signal for the transmitter section of the ACE. The clock rate is equal to the oscillator frequency divided by the divisor loaded into the divisor latches. The BAUDOUT signal may be used to clock the receiver by tying to RCLK (pin 9 for DIP package and/or pin 10 for QUAD package).

Table A-1. Pin Designations

10

PIN NUMBERS DIP	PIN NUMBERS QUAD	MNEMONIC	SIGNAL NAME	FUNCTION
16	18	XTAL 1	EXTERNAL CLOCK IN	These pins connect the crystal or signal clock to the ACE baud rate divisor circuit. See Fig.7-1 and 7-2 for circuit connection diagrams.
17	19	XTAL 2	EXTERNAL CLOCK OUT	
18	20	$\overline{\text{DOSTR}}$	$\overline{\text{DATA OUT}}$ STROBE	When the chip has been selected, a low DOSTR or high DOSTR will latch into the selected WD16C550 register (a CPU write). Only one of these lines Need be used. Tie unused line to its inactive state, DOSTR - high or DOSTR - low.
19	21	DOSTR	DATA OUT	
20	22	Vss	GROUND	System signal ground.
--	23	NC	NO CONNECTION	No Connection.
21	24	$\overline{\text{DISTR}}$	$\overline{\text{DATA IN}}$ STROBE	When chip has been selected, a low DISTR or high DISTR will allow a read of the selected WD16C550 register (a CPU read). Only one of these lines need be used. Tie unused line to its inactive state, DISTR - high or DISTR - low.
22	25	DISTR	DATA IN STROBE	
23	26	DDIS	DRIVER DISABLE	Output goes low whenever data is being read from the ACE. Can be used to reverse data direction of external transceiver.
24	27	$\overline{\text{TXRDY}}$	$\overline{\text{TRANSMIT}}$ READY	$\overline{\text{TXRDY}}$ output is used to DMA transfers. Two modes of operatoin are available when using FIFO Mo;de, and one (Mode 0) is available when using Character Mode. Mode 0 (FCR0=0 OR FCR0=1 AND FCR3=0): DMA transfers are interleaved between bus cycles. In character mode with FCR3=0, $\overline{\text{TXRDY}}$ will be active (low) if there are no characters in the XMIT FIFO (FIFO Mode) or Xmit Holding Register (CHAR Mode). $\overline{\text{TXRDY}}$ will go inactive after the first character is loaded.

Table A-1. Pin Designations (Contd)

PIN NUMBERS DIP	PIN NUMBERS QUAD	MNEMONIC	SIGNAL NAME	FUNCTION
				Mode 1: Multiple DMA bursts are made until TXMT **is empty or XMIT is full. In FIFO Mode (FCR=1) with FCR3=1, if there is at least one unfilled position in the Xmit FIFO,** TXRDY will be active (low). TXRDY will go inactive after the first character is loaded into the Xmit FIFO.
25	**28**	$\overline{\text{ADS}}$	$\overline{\text{ADDRESS}}$ STROBE	When low, provides latching for Register Select (A0,A1,A2) and Chip Select (CS0,CS1,CS2). NOTE: The rising edge (↑) of the ADS signal is required when the Register Select (A0,A1,A2) and the Chip Select (CS0, CS1, CS2) signals are not stable for the duration of a read or write operation. If not required, the ADS input can be tied perman -ently low.
26	29	A2	REGISTER SELECT A2	These three inputs are used to select an internal register of the ACE during a read or a write. See Table 2-1.
27	30	A1	REGISTER SELECT A1	
28	31	A0	REGISTER SELECT A0	
29	32	$\overline{\text{RXRDY}}$	$\overline{\text{RECEIVER}}$ READY	Receiver Ready output is used to signal DMA transfes. Two modes of operation are available when using FIFO Mode, and one mode (Mode 0) is available when using Character Mode. Mode 0: DMA transfers are interleaved between bus cycles When in Character Mode (FCR0=0) or in the FIFO Mode (FCR0=1), with FCR3=0, and there is at least 1 character in the Rcvr FIFO Register or Rcvr Holding Register, the RXRDY will be active (low). It will go inactive when the Rcvr FIFO (FIFO Mode) or Holding Register (Character Mode) is empty.

Table A-1. Pin Designations (Contd)

PIN NUMBERS DIP	PIN NUMBERS QUAD	MNEMONIC	SIGNAL NAME	FUNCTION
				Mode 1: Multiple DMA bursts are made until RCVR FIFO is empty or XMIT FIFO is full. In FIFO Mode (FCR0=1) and FCR3=1, will go active (low) when the trigger level or time out has been reached. RXRDY becomes inactive (high) when the FIFO is empty.
30	33	INTRPT	INTERRUPT	Output goes high whenever an enabled interrupt is pending.
--	34	NC	NO CONNECTION	No Connection.
31	**35**	$\overline{OUT2}$	$\overline{OUTPUT\ 2}$	User-designated output that can be programmed by Bit 3 of the Modem Control Register (OUT2 goes low when Bit 3 = 1).
32	36	$\overline{RTS}$	$\overline{REQUEST\ TO\ SEND}$	Output when low informs the modem or data set that the ACE is ready to transmit data. See Modem Control Register.
33	37	$\overline{DTR}$	$\overline{DATA\ TERMINAL\ READY}$	Output when low informs the modem or data set that the ACE is ready to receive data.
34	38	$\overline{OUT\ 1}$	$\overline{OUTPUT\ 1}$	User-designated output that can be programmed by Bit 2 of Modem Control Register (OUT1 goes low when Bit 2 = 1).
35	39	MR	MASTER RESET	When high clears the registers to the states as indicated in Table 3-1.
36	40	$\overline{CTS}$	$\overline{CLEAR\ TO\ SEND}$	Input from DCE indicating remote device is ready to Transmit data. See Modem Status Register.
37	41	$\overline{DSR}$	$\overline{DATA\ SET\ READY}$	Input from DCE used to indicate the status of the local data set. See Modem Status Register.

Table A-1. Pin Designations (Contd)

PIN NUMBERS DIP	PIN NUMBERS QUAD	MNEMONIC	SIGNAL NAME	FUNCTION
38	42	$\overline{RLSD}$	$\overline{RECEIVER\ LINE\ SIGNAL\ DETECT}$	Input from DCE indicating that it is receiving a signal which meets its signal quality conditions. See Modem Status Register.
39	43	$\overline{RI}$	$\overline{RING\ INDICATOR}$	Input when low indicates that a ringing signal is being received by the modem or data set. See Modem Status Register.
40	44	Vcc	+5V	+5 Volt Supply.

Table A-1. Pin Designations (Contd)

APPENDIX B

B.0 DC OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Temperature
Under Bias ..... 0°C (32°F) to 70°C (158°F)

Storage Temperature
Ceramic ..... -65°C (-85°F) to +150°C (302°F)
Plastic ..... -50°C (-58°F) to +125°C (257°F)

All Input or Output Voltages
with respect to Vss ..... -0.5V to +7.0V

Power Dissipation WD16C550 ..... 40mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Operating Characteristics

SYMBOL	CHARACTERISTIC	WD16C550 MIN	MAX	UNITS	TEST CONDITIONS
Vil x	Clock Input Low Voltage	-0.5	0.8	V	
Vih x	Clock Input High Voltage	0.2	Vcc	V	
Vil	Input Low Voltage	-0.5	0.8	V	
Vih	Input High Voltage	2.0	Vcc	V	
Vol	Output Low Voltage		0.4	V	Iol = 1.6mA on all outputs
Voh	Output High Voltage	2.4		V	Ioh = -100µA
Icc	(AV) Average Power Supply Current (Vcc)		8	mA	Vcc = 5.25V Ta = 25°C. No (Vcc) loads on SIN, DSR,RLSD, CTS. RI = 2.0V. All other inputs = 0.8V. Baud rate generator at 8 MHz. Baud rate at 512K.
Iil	Input Leakage		±15	uA	Vcc = 5.25V. Vss = 0V. All other pins floating.
Icl	Clock Leakage		±10	uA	Vin = 0V, 5.25V
Idl	Data Bus Leakage		±10	uA	Vout = 0.0V Vout = 5.25V Data Bus is at High-Impedance State
Vilmr	MR Schmitt Vil		0.8	V	
Vihmr	MR Schmitt Vih	2.0		V	

Table B-1. DC Operating Characteristics
Ta = 0°C (32°F) to +70°C (158°F), Vcc = +5V ± 5%, Vss = 0V, Unless Otherwise Specified.

SYMBOL	CHARACTERISTIC	WD16C550 TYP	MAX	UNITS	TEST CONDITIONS
Cxin	Clock Input Capacitance	15	20	pF	fc = 1 MHz
Cxout	Clock Output Capacitance	20	30	pF	
Cin	Input Capacitance	6	10	pF	Unmeasured Pins Returned to Vss
Cout	Output Capacitance	10	20	pF	Unmeasured Pins Returned to Vss

Table B-2. Capacitance
Ta = 25°C (77°F), f = 1.0 MHz, Vcc = Vss = 0V

APPENDIX C

C.O AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

Ta = 0°C (32°F) to +70°C (158°F), Vss = +5V ± 5%,

C.1 TIMING DIAGRAMS

FIGURE NUMBER	TITLE
C-1	Baud Rate Generator Timing
C-2	Receiver Timing
C-3	Transmitter Timing
C-4	MODEM Control Timing
C-5	Read Cycle Timing
C-6	Write Cycle Timing
C-7	RCVR FIFO Signaling Timing for First Byte
C-8	RCVR FIFO Signaling Timing after First Byte (RBR already set)
C-9	Receiver DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
C-10	Receiver DMA Mode 1 Timing (FCR0 = 1 and FCR3 = 1)
C-11	Transmitter DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
C-12	Transmitter DMA Mode 1 (FCR0 = 1 and FCR3 = 1)

Table C-1. WD16C550 Timing Diagrams

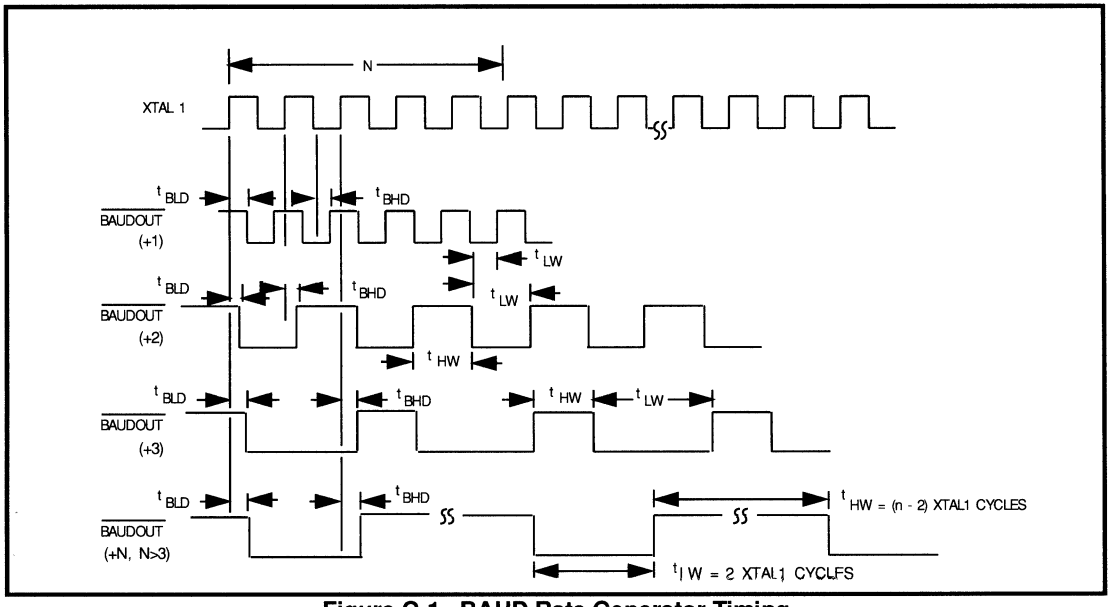


Figure C-1. BAUD Rate Generator Timing

10

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
N	Baud Rate Divisor	1	$(2^{16} - 1)$		
t_{BLD}	Baud Output Negative Edge Delay		100	nsec	100pF Load
t_{BHD}	Baud Output Positive Edge Delay		100	nsec	100pF Load
t_{LW}	Baud Output Low Time	32		nsec	100pF Load (fx = 8. 0 MHz÷1)
t_{HW}	Baud Output High Time	30		nsec	100pF Load (fx = 8. 0 MHz÷1)

Table C-2. BAUD Rate Generator Timing

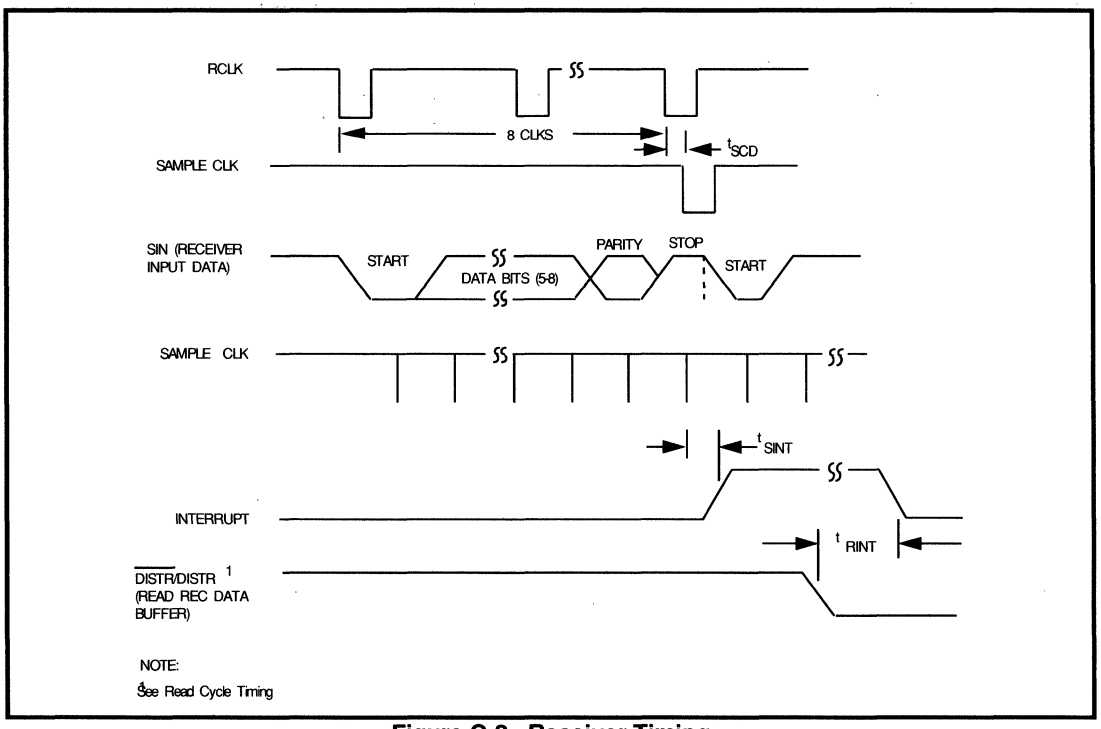


Figure C-2. Receiver Timing

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
tSCD	Delay from RCLK to Sample Time		2	µsec	
tSINT	Delay from Stop to Set Interrupt		1*	RCLK Cycles	100pF Load
tRINT	Delay from DIST/DISTR (RD RBR) Reset Interrupt	0.250	1	µsec	100pF Load

Table C-3. Receiver Timing

* When receiving the first byte in FIFO mode tSINT (only for timeout or trigger level interrupt) will be delayed 3 RCLK cycles, except for a timeout interrupt where tSINT will be delayed 8 RCLK cycles.

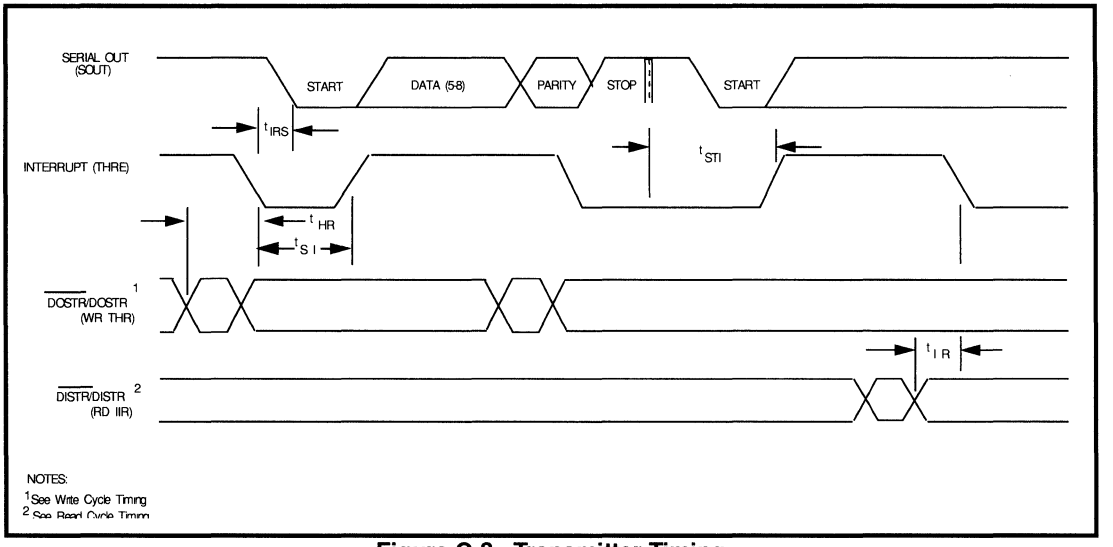


Figure C-3. Transmitter Timing

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
tHR	Delay from $\overline{\text{DOSTR}}$/ DOSTR (WR THR) to Reset Interrupt		0.175	µsec	100pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start	8	24	$\overline{\text{BAUDOUT}}$ Cycles	
tSI	Delay from Initial Write to Interrupt	16	24	$\overline{\text{BAUDOUT}}$ Cycles	
tSTI	Delay from Stop to Interrupt ($\overline{\text{THRE}}$)	8	8	$\overline{\text{BAUDOUT}}$ Cycles	
tIR	Delay from $\overline{\text{DISTR}}$/ DISTR (RD IIR to Reset Interrupt (THRE)		0.250	µsec	100pF Load
tSXA	Delay from Start to TXRDY Active	0	8	$\overline{\text{BAUDOUT}}$ Cycles	
tWXI	Delay from Write to TXRDY Inactive	0	0.195	µsec	

Table C-4. Transmitter Timing

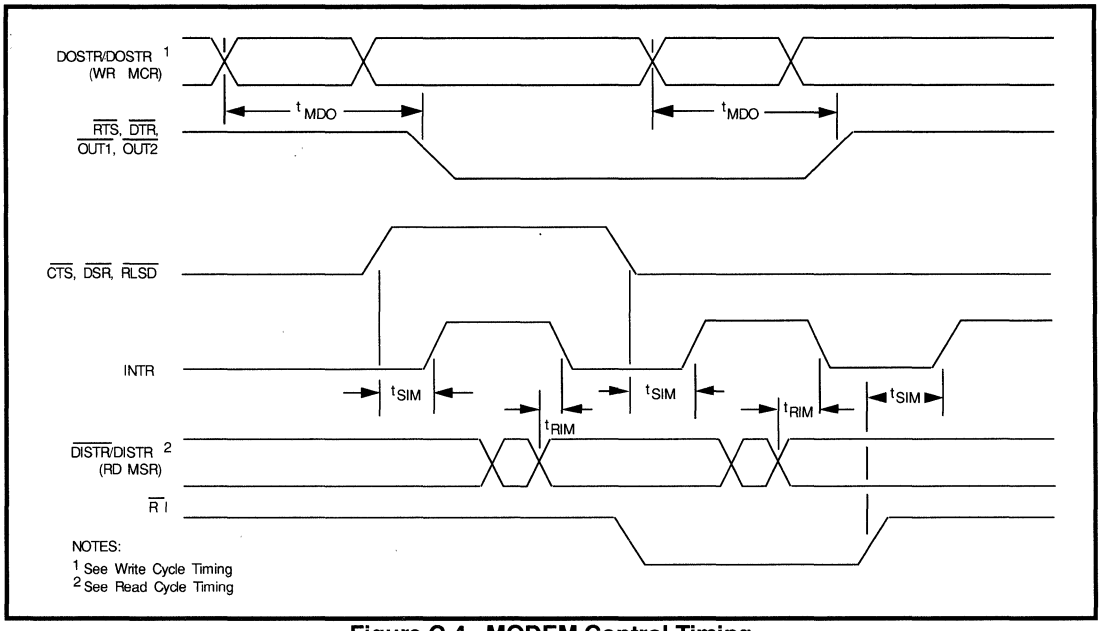


Figure C-4. MODEM Control Timing

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
t_{MDO}	Delay from $\overline{DOSTR}$/ DOSTR (WR MCR) to Output		0.200	µsec	100pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		0.250	µsec	100pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/ DISTR (RD MSR)		0.250	µsec	100pF Load

Table C-5. MODEM Control Timing

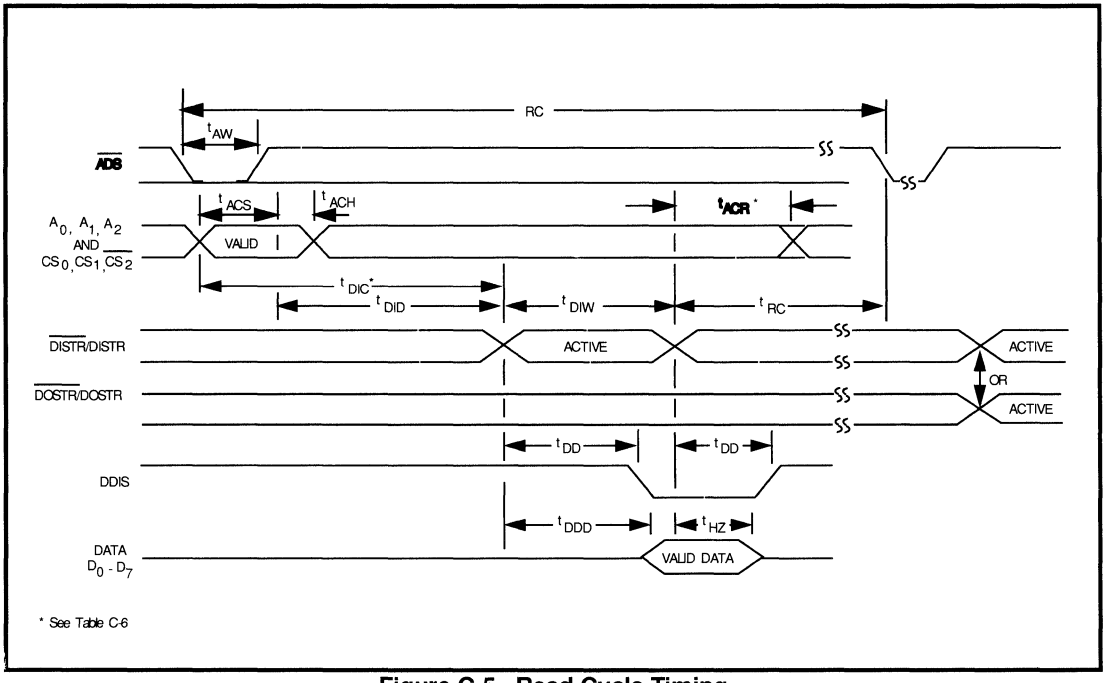


Figure C-5. Read Cycle Timing

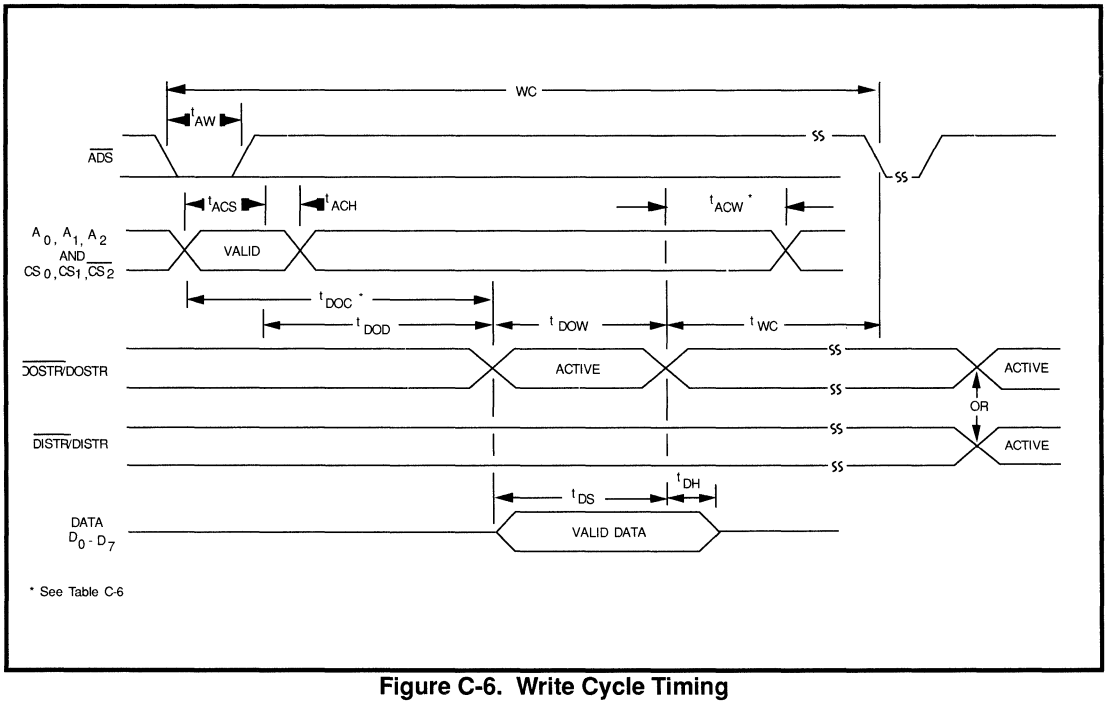


Figure C-6. Write Cycle Timing

SYMBOL	CHARACTERISTIC	WD16C550 MIN	WD16C550 MAX	UNITS	TEST CONDITIONS
tAW	Address Strobe Width	60		nsec	1TTL Load
tACS	Address and Chip Select Setup Time	60		nsec	1TTL Load
tACH	Address and Chip Select Hold Time	0		nsec	1TTL Load
tDID	$\overline{\text{DISTR}}$/DISTR Delay from latch			nsec	1TTL Load
tDIW	$\overline{\text{DISTR}}$/DISTR Strobe Width	125		nsec	1TTL Load
tRC	Read Cycle Delay	125		nsec	1TTL Load
RC	Read Cycle = tACS + tDID + tDIW + tRC + 20 nsec	280		nsec	1TTL Load
tDD	$\overline{\text{DISTR}}$/DISTR to Driver Disable Delay		60	nsec	1TTL Load
tDDD	Delay from $\overline{\text{DISTR}}$/DISTR to Data		100	nsec	1TTL Load
tHZ	$\overline{\text{DISTR}}$/DISTR to Floating Data Delay	0	100	nsec	1TTL Load
tDOD	DOSTR/DOSTR Delay from Latch			nsec	1TTL Load
tDOW	DOSTR/DOSTR Strobe Width	100		nsec	1TTL Load
tWC	Write Cycle Delay	150		nsec	1TTL Load
WC	Write Cycle =tACS + tDOD + tDOW + tWC + 20 nsec	280		nsec	1TTL Load
tDS	Data Setup Time	30		nsec	1TTL Load
tDH	Data Hold Time	30		nsec	1TTL Load
tDIC*	DISTR/DISTR DELAY from Select or Address	30		nsec	1TTL Load
tDOC*	$\overline{\text{DOSTR}}$/DOSTR Delay from Select or Address	30		nsec	1TTL Load
tACR*	Address and Chip Select Hold Time from DISTR/DISTR	20		nsec	1TTL Load
tACW*	Address and Chip Select Hold Time from DOSTR/DOSTR	20		nsec	1TTL Load
tMR	Master Reset Pulse Width	5.0		µsec	1TTL Load
tXH	Duration of Clock HIGH Pulse	55		nsec	
tXL	Duration of Clock LOW Pulse	55		nsec	External Clock (8.0 MHz Max.)

* Only applicable when $\overline{\text{ADS}}$ is permanently low.

Table C-6. Read/Write Cycle Timing

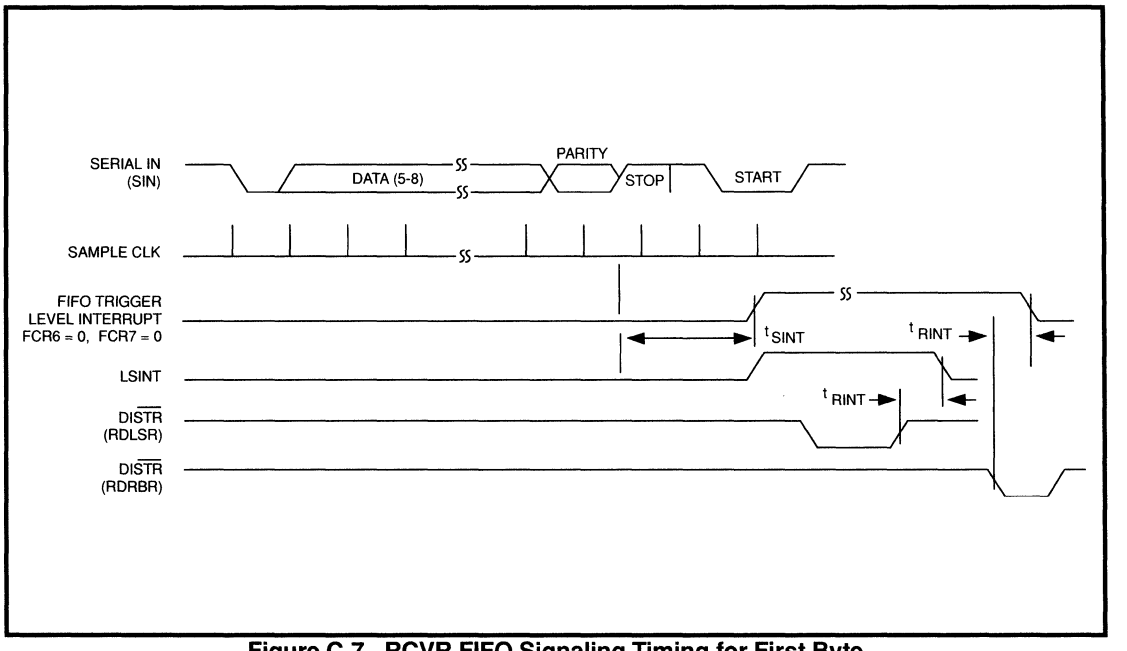


Figure C-7. RCVR FIFO Signaling Timing for First Byte

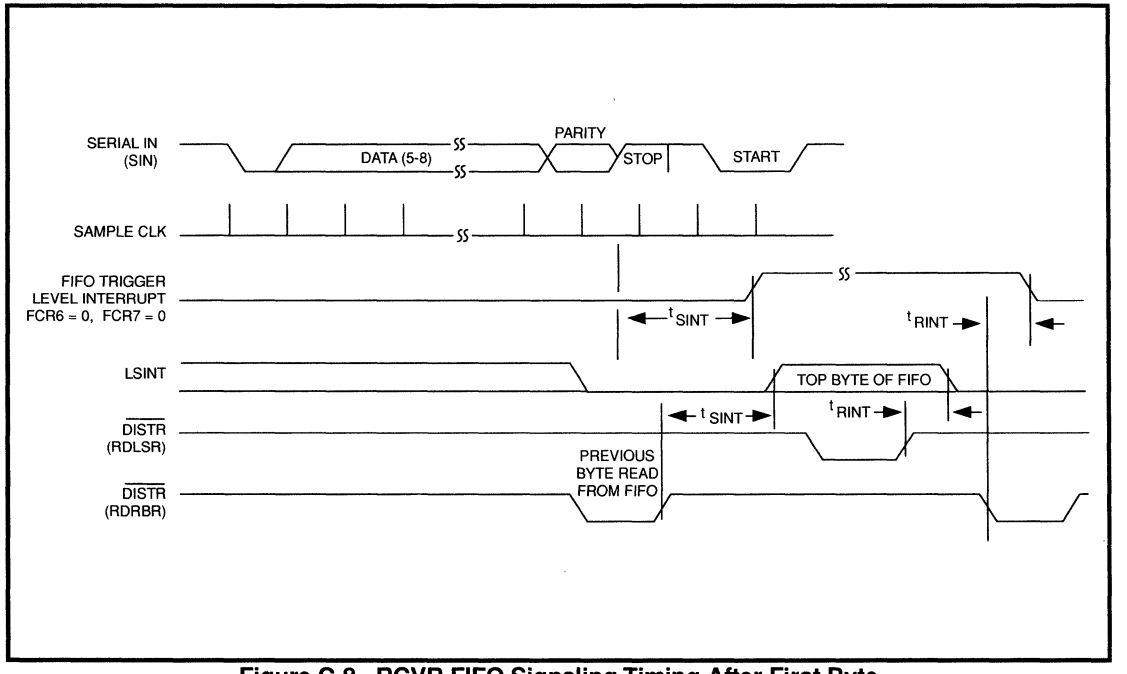


Figure C-8. RCVR FIFO Signaling Timing After First Byte (RBR Already Set)

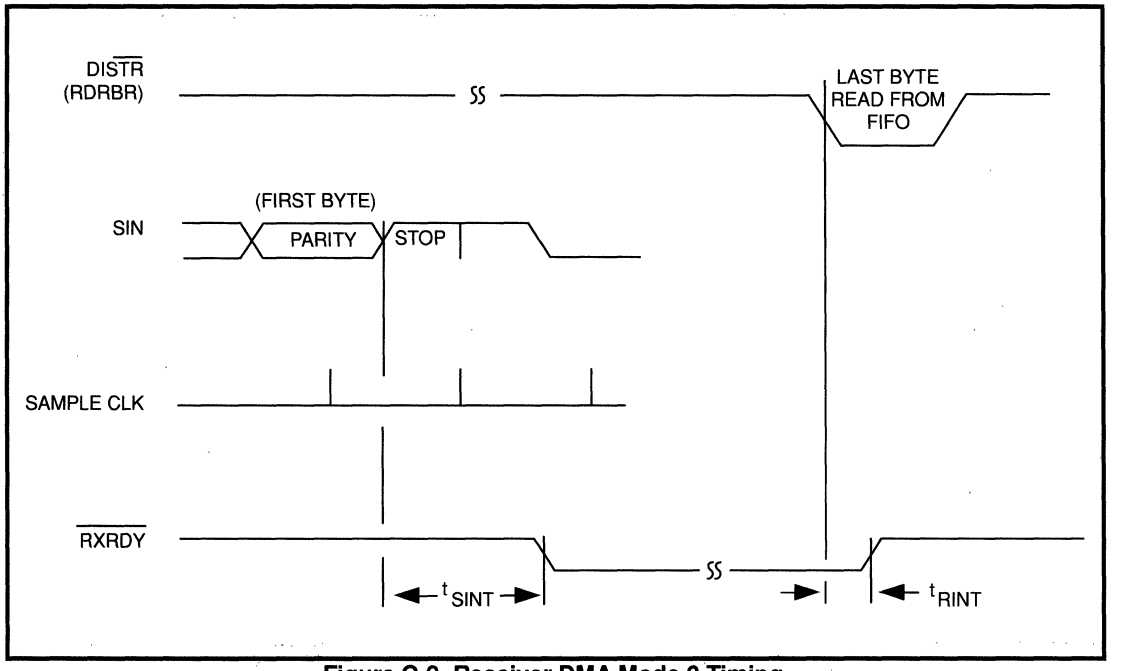


Figure C-9. Receiver DMA Mode 0 Timing
(FCR0=0 or FCR0=1, FCR3=0)

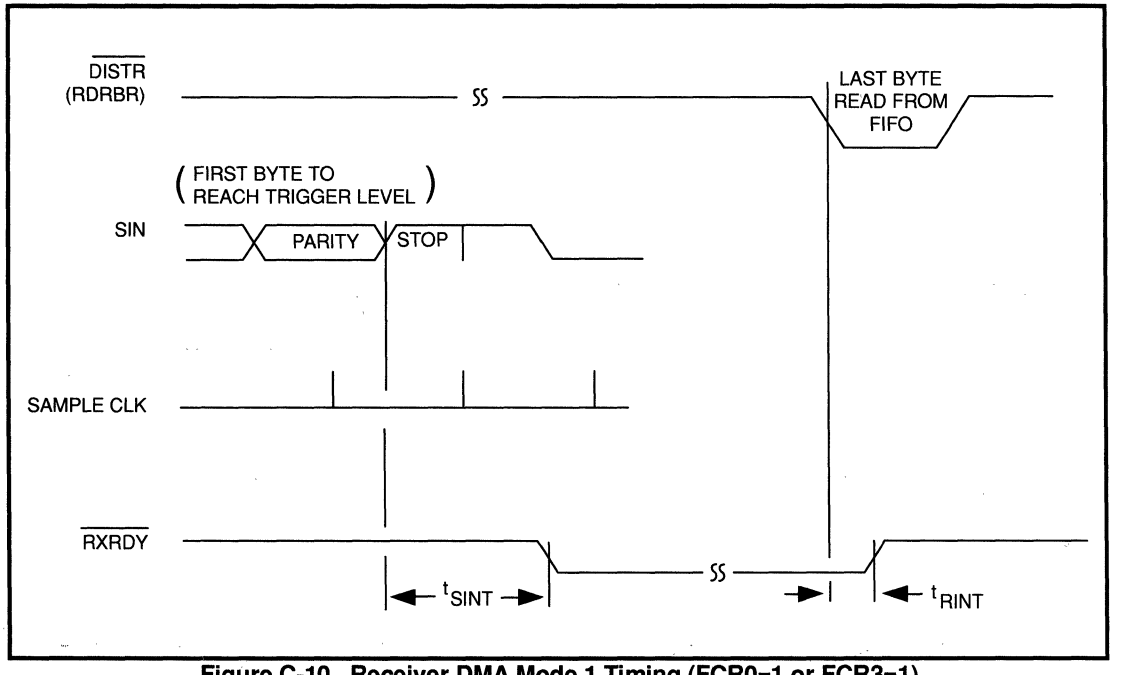


Figure C-10. Receiver DMA Mode 1 Timing (FCR0=1 or FCR3=1)

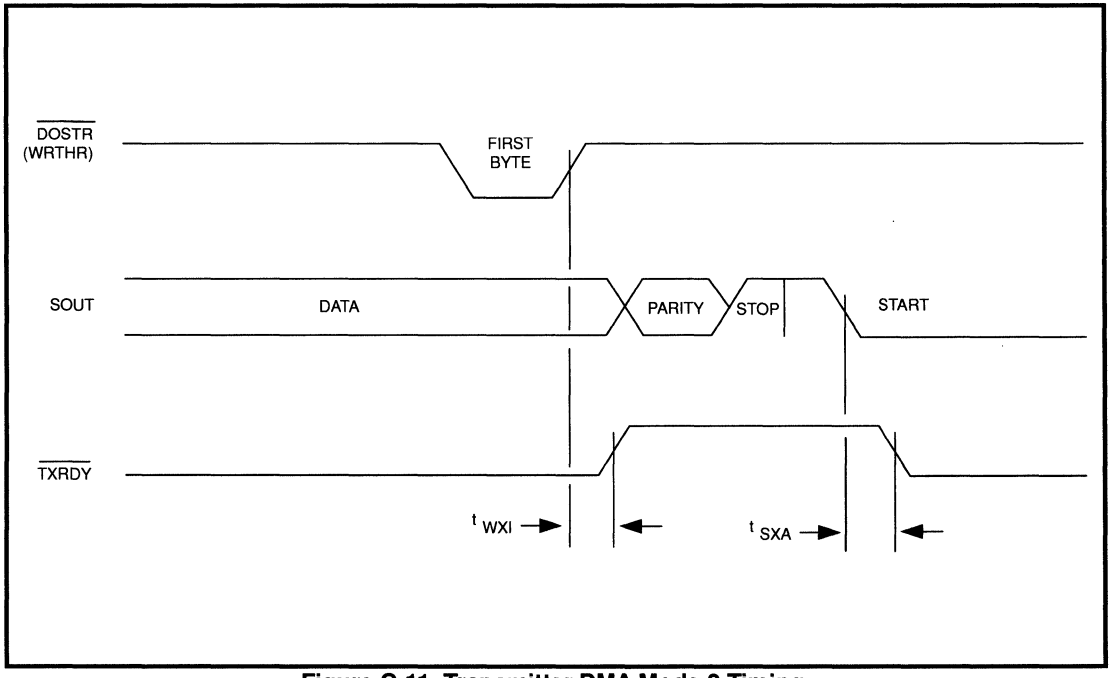


Figure C-11. Transmitter DMA Mode 0 Timing (FCR0=0 or FCR0=1 and FCR3=0)

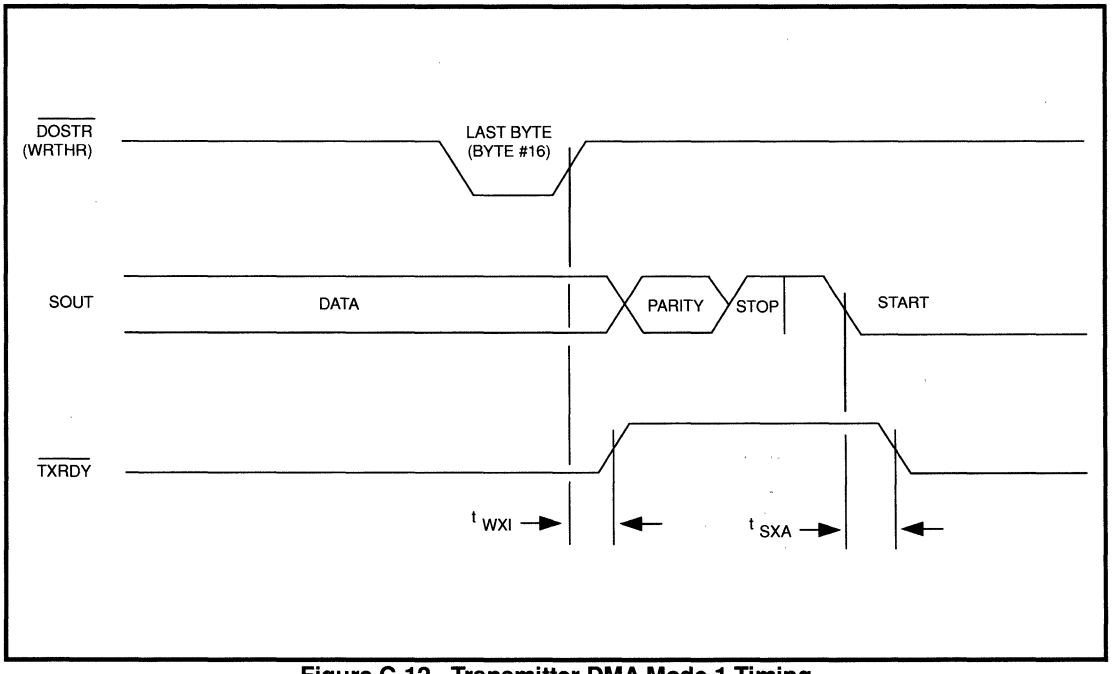


Figure C-12. Transmitter DMA Mode 1 Timing (FCR0=0 or FCR0=1 and FCR3=0)

APPENDIX D

D.O PACKAGE DIAGRAMS

Figures D-1, D-2, and D-3 illustrate the 40-Pin DIP packages and 44-Pin QUAD package showing dimensions in inches.

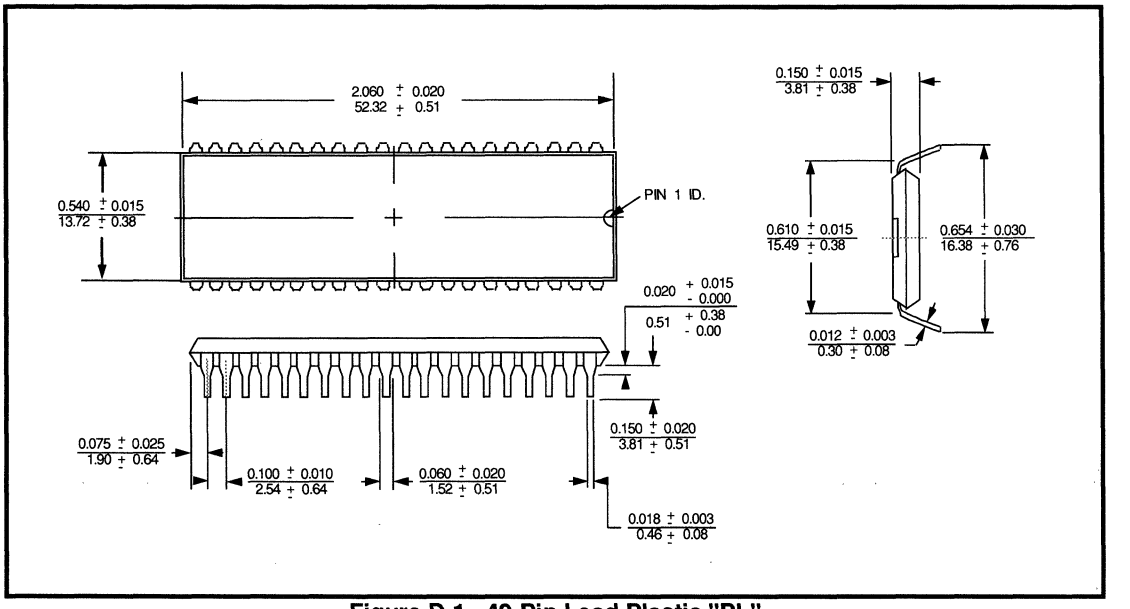


Figure D-1. 40-Pin Lead Plastic "PL"

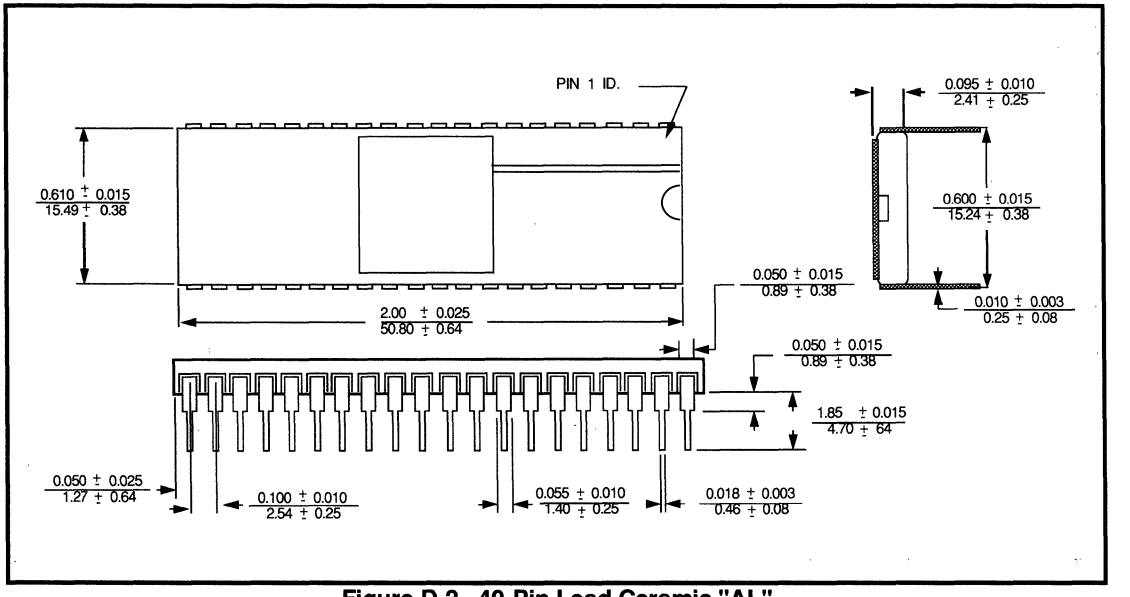


Figure D-2. 40-Pin Lead Ceramic "AL"

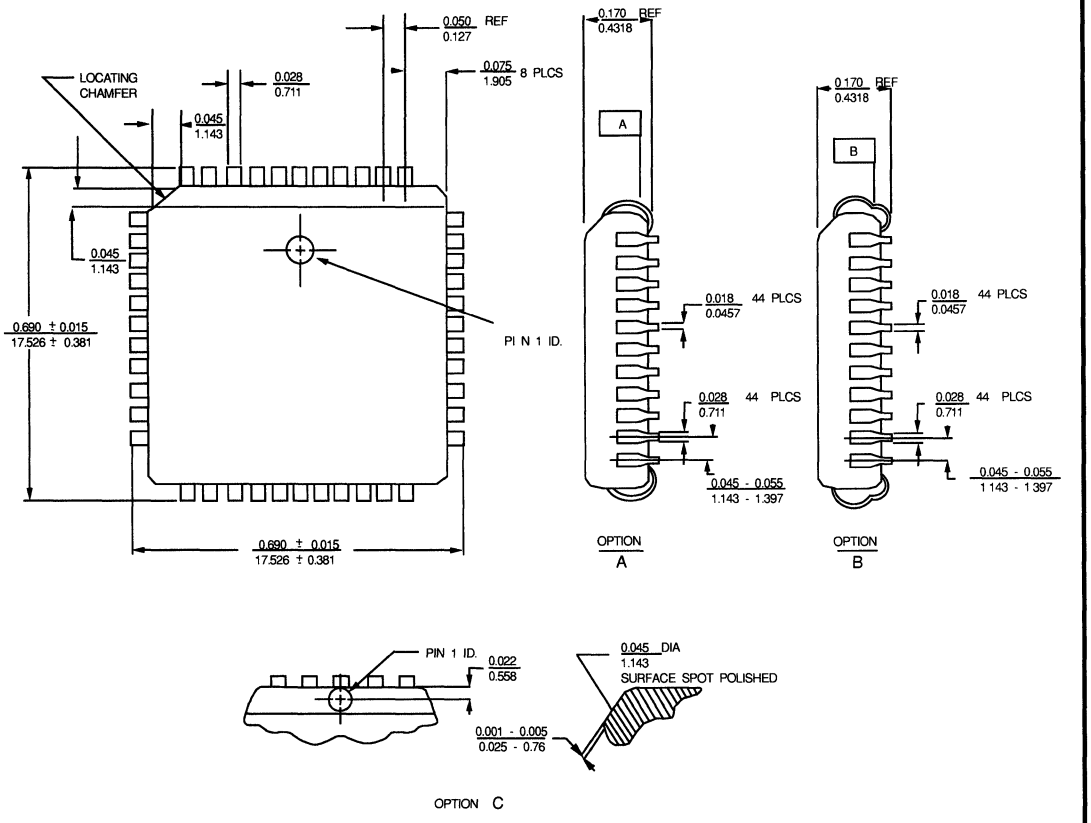


Figure D-3. 44-Pin QUAD Lead Plastic "JM"

WD6000

Enhanced CPU and Peripheral Control Device

WESTERN DIGITAL

TABLE OF CONTENTS

TABLE OF CONTENTS, Continued

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS, Continued

LIST OF TABLES

ADDITIONAL REFERENCES

IBM PS/2 Model 50/60 Technical Reference Manual

Intel Microprocessor and Peripheral Handbook

IBM PS/2 Model 70/80 Technical Reference Manual

1.0 INTRODUCTION

1.1 DESCRIPTION

As part of the Western Digital® Micro Channel compatible chip sets (WD6500, WD6400SX, WD6400SX/LP), the WD6000 CPU and Peripheral Control Logic integrated circuit significantly facilitates the design and implementation of system boards compatible with IBM's Micro Channel architecture. It decreases the design complexity and saves space by combining the functions of many discrete arrays and components, while reducing system cost and increasing system reliability.

The Extended Setup Facility (ESF) is a fully compatible enhancement that allows designers to easily configure additional functionality such as a Winchester controller, LAN adapter, or an additional serial port on the system board. This facility can help reduce costs and provide system level product differentiation. Figure 1 shows a typical system diagram using Western Digital's Micro Channel compatible chip sets.

1.2 FEATURES

- Hardware (Register Level) and Software Compatible to the IBM Personal System/2 Micro Channel implementations
- Functionality equivalent to the following:
  - Two 8259 Interrupt Controllers
  - 8254 Timer
  - Watchdog Timer Logic
  - System Board I/O Decode Logic
  - Peripheral Bus Control Generator
  - NMI Generator
  - Error Control Logic
- Interfaces Directly to the Micro Channel
- Operates in an 80486, 80386DX or 80386SX System
- Math Coprocessor Support (80387/80387SX, Weitek 4167/3167 or compatible)
- Programmable Option Select (POS) Logic
- Clock Generation Logic for Math Coprocessor and Keyboard Controller
- Support for External CMOS RAM for storage of Configuration Data
- Extended Setup Facility™ (ESF™)
- Low Power 1.25 Micron CMOS Technology
- 132-Lead JEDEC Plastic Quad Flat Pack

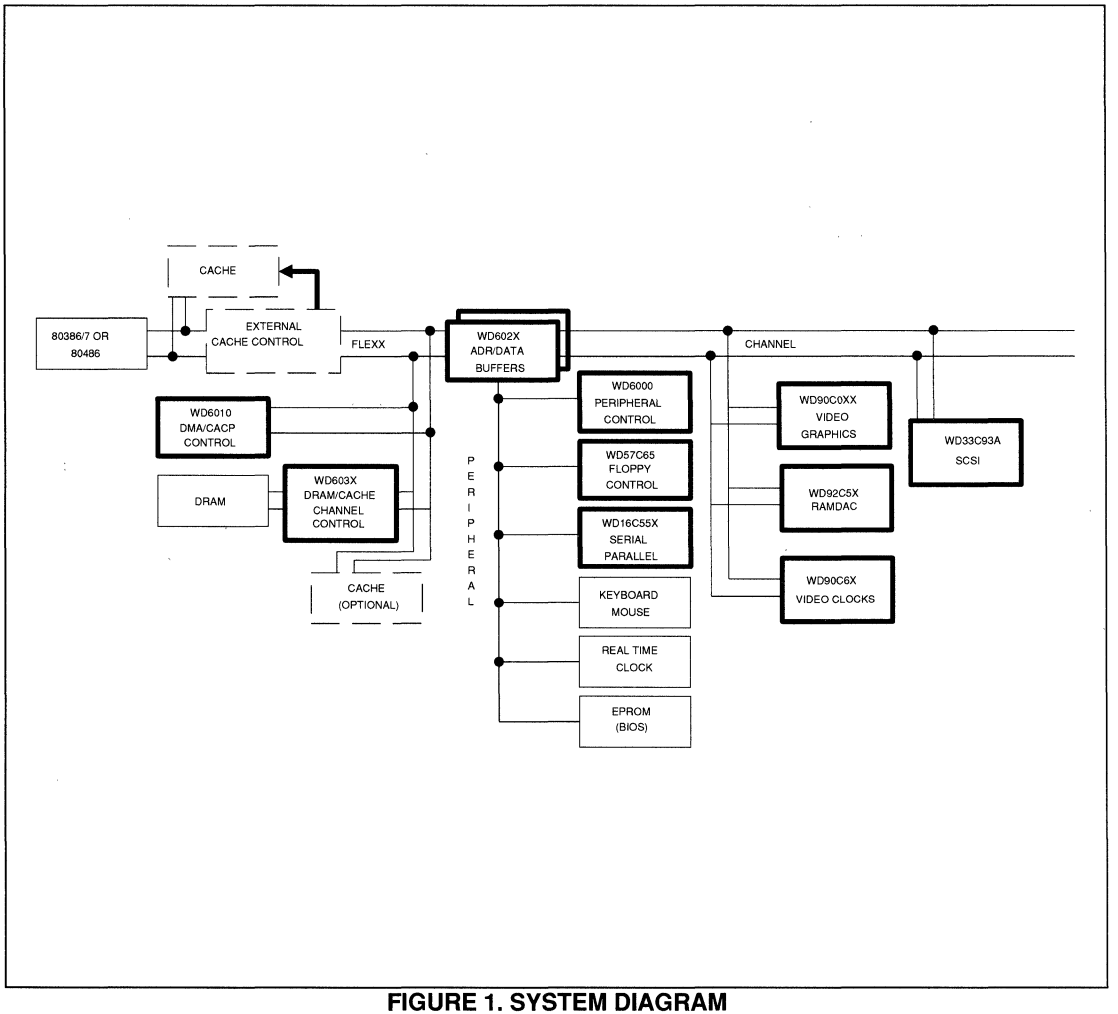


FIGURE 1. SYSTEM DIAGRAM

(DEVICES WITH BOLD OUTLINES AVAILABLE FROM WESTERN DIGITAL CORPORATION)

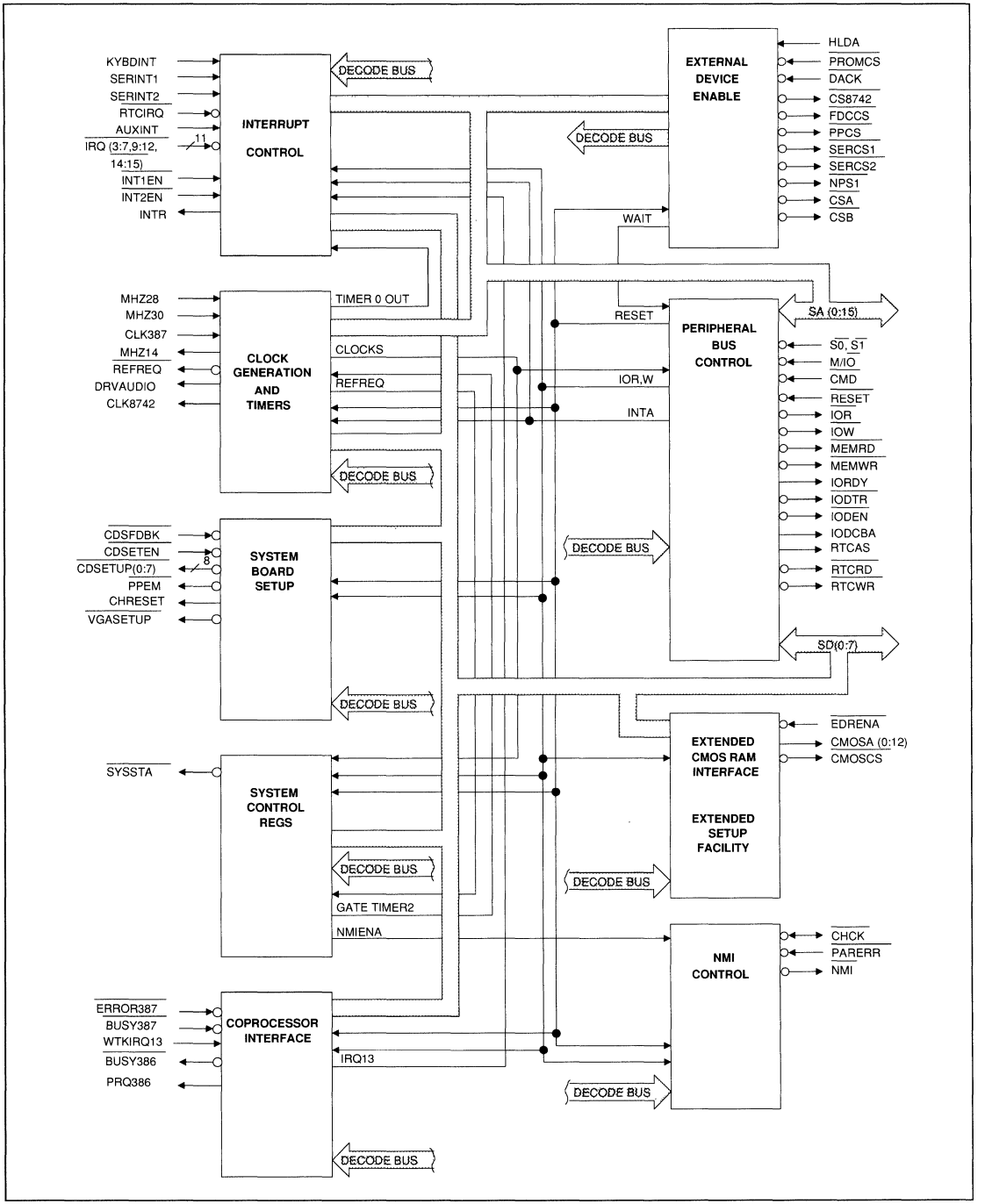


FIGURE 2. WD6000 BLOCK DIAGRAM

2.0 PIN DESCRIPTION

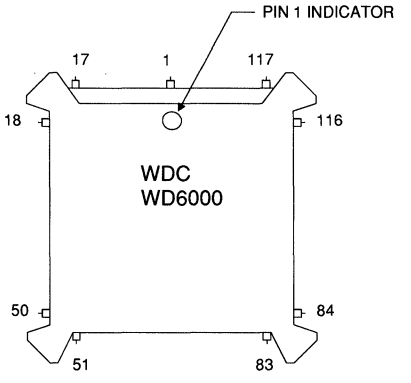


FIGURE 1. 132-PIN JEDEC FLAT PACK

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	SD6	34	SA14	67	TEST	100	RTCWR
2	V_{DD}	35	V_{DD}	68	V_{DD}	101	V_{SS}
3	SD5	36	SA13	69	CMOSA10	102	RTCRD
4	CLK387	37	SA12	70	CMOSA9	103	RTCAS
5	SD4	38	SA11	71	CMOSA8	104	IOW
6	SD3	39	SA10	72	CMOSA7	105	IOR
7	SD2	40	SA9	73	CMOSA6	106	MEMWR
8	WTKIRQ13	41	SA8	74	CMOSA5	107	MEMRD
9	SD1	42	SA7	75	CMOSA4	108	N/C
10	SD0	43	SA6	76	V_{SS}	109	CLK8742
11	V_{SS}	44	SA5	77	CMOSA3	110	IODCBA
12	CHCK	45	SA4	78	CMOSA2	111	IODEN
13	V_{SS}	46	SA3	79	CMOSA1	112	IODTR
14	BUSY387	47	SA2	80	CMOSA0	113	PRQ386
15	ERROR387	48	SA1	81	MHZ14	114	CMOSA12
16	RESET	49	SA0	82	NMI	115	V_{SS}
17	MHZ28	50	V_{SS}	83	DRVAUDIO	116	CMOSA11
18	PARERR	51	IRQ11	84	SYSSTA	117	BUSY386
19	CDSETEN	52	IRQ10	85	CMOSCS	118	CSA
20	MHZ30	53	IRQ9	86	V_{DD}	119	CSB
21	SERINT2	54	RTCIRQ	87	INTR	120	N/C
22	SERINT1	55	IRQ7	88	V_{SS}	121	CDSETUP0
23	INT2EN	56	IRQ6	89	NPS1	122	CDSETUP1
24	INT1EN	57	IRQ5	90	PPCS	123	V_{DD}
25	AUXINT	58	IRQ4	91	SERCS2	124	CDSETUP2
26	DACK	59	IRQ3	92	SERCS1	125	V_{SS}
27	PROMCS	60	KYBDINT	93	FDCCS	126	CDSETUP3
28	HLDA	61	M/IO	94	CS8742	127	CDSETUP4
29	IRQ15	62	CMD	95	PPEM	128	CDSETUP5
30	IRQ14	63	N/C	96	VGASETUP	129	CDSETUP6
31	EDRENA	64	S1	97	IORDY	130	CDSETUP7
32	IRQ12	65	S0	98	REFREQ	131	CHRESET
33	SA15	66	CDSFDBK	99	V_{DD}	132	SD7

PIN NO.	NAME	TYPE	FUNCTION
		INTERRUPT CONTROL	
60	KYBDINT	I	KEYBOARD INTERRUPT - Driven by the system keyboard controller.
22	SERINT1	I	SERIAL INTERRUPT 1 - Internally switched with SERINT2 to share IRQ3 and IRQ4 under software control. The Program Control Register (PCR) and Setup Register 0102H are used to assign the serial interrupt signals.
21	SERINT2	I	SERIAL INTERRUPT 2 - Internally switched with SERINT1 to share IRQ3 and IRQ4 under software control. The Program Control Register (PCR) and Setup Register 0102H are used to assign the serial interrupt signals.
54	$\overline{\text{RTCIRQ}}$	I	$\overline{\text{REAL-TIME CLOCK INTERRUPT}}$ - Generated by the system Real-Time Clock module.
25	AUXINT	I	AUXILIARY INTERRUPT - Driven by the system keyboard controller.
59 58 57 56 55 53 52 51 32 30 29	$\overline{\text{IRQ3}}$ $\overline{\text{IRQ4}}$ $\overline{\text{IRQ5}}$ $\overline{\text{IRQ6}}$ $\overline{\text{IRQ7}}$ $\overline{\text{IRQ9}}$ $\overline{\text{IRQ10}}$ $\overline{\text{IRQ11}}$ $\overline{\text{IRQ12}}$ $\overline{\text{IRQ14}}$ $\overline{\text{IRQ15}}$	I	$\overline{\text{INTERRUPT REQUESTS}}$ - Asynchronous inputs that may be shared by other interrupting devices.
24	$\overline{\text{INT1EN}}$	I	$\overline{\text{SERIAL INTERRUPT 1 ENABLE}}$ - System generated programmable output that gates the interrupt signal SERINT1 from the associated serial device. This line must be grounded to enable the interrupt.
23	INT2EN	I	SERIAL INTERRUPT 2 ENABLE - System generated programmable output that gates the interrupt signal SERINT2 from the associated serial device. Line must be grounded to enable the interrupt.
87	INTR	O	INTERRUPT - Drives the system CPU interrupt pin.
		CLOCK GENERATION & TIMERS	
17	MHZ28	I	28.636 MHz - Basic clock used for all WD6000 internal functions (timers, wait generator, bus interface logic.

O = Output, I = Inputy, I/O = Bi-directional

PIN NO.	NAME	TYPE	FUNCTION
CLOCK GENERATION & TIMERS, Continued			
20	MHZ30 (optional)	I	30.0 MHz - Drives the coprocessor and keyboard clock outputs appropriately. See Pin 109 below.
81	MHZ14	O	14.318 MHz - This clock output drives the Channel OSC line.
98	$\overline{\text{REFREQ}}$	O	$\overline{\text{REFRESH REQUEST}}$ - Timer output used to request a refresh cycle by the CACP and DMA controller.
83	DRVAUDIO	O	DRIVE AUDIO - Drives the audio summing network shared by the Channel audio line and Timer 2 OUT gated by Control Port B (0061H) bit 0.
109	CLK8742	O	8742 CLOCK - Drives the keyboard controller. It is derived from the 30 MHz clock input divided by 3 if the MHZ30 clock input is present. If the MHZ30 clock input is connected to the MHZ28 clock, then the keyboard clock (CLK8742), is derived from the MHZ28 clock input divided by 3, and a math coprocessor will not be supported.
4	CLK387	I	For systems using an 80387 or 80387SX, this pin should be connected to the CLK phase of the coprocessor. It is used to synchronize the coprocessor logic to the coprocessor clock. For systems with non-Intel coprocessors, this pin should be left unconnected.
SYSTEM BOARD SETUP			
66	$\overline{\text{CDSFDBK}}$	I	$\overline{\text{CARD SELECTED FEEDBACK}}$ - This Channel signal indicates the addressed slave is present.
19	$\overline{\text{CDSETEN}}$	I	$\overline{\text{CARD SETUP ENABLE}}$ - Timing decode for the 0100H-0107H from the WD6010.
121 122 124 126 127 128 129 130	$\overline{\text{CDSETUP0}}$ $\overline{\text{CDSETUP1}}$ $\overline{\text{CDSETUP2}}$ $\overline{\text{CDSETUP3}}$ $\overline{\text{CDSETUP4}}$ $\overline{\text{CDSETUP5}}$ $\overline{\text{CDSETUP6}}$ $\overline{\text{CDSETUP7}}$	O	$\overline{\text{CARD SETUP}}$ - Each signal drives a Channel slot.
95	$\overline{\text{PPEM}}$	O	$\overline{\text{PARALLEL PORT EXTENDED MODE}}$ - When asserted, this signal puts the parallel port into Extended (bidirectional) Mode.
131	CHRESET	O	CHANNEL RESET - This software-generated signal resets all Channel resident adapters and system board I/O devices only. Located in register 0096H Bit 7.
96	$\overline{\text{VGASETUP}}$	O	$\overline{\text{VGA SETUP}}$ - Tells the VGA device to enter Setup Mode.

O = Output, I = Input, I/O = Bi-directional

PIN NO.	NAME	TYPE	FUNCTION
			SYSTEM CONTROL REGISTERS
84	SYSSTA	O	SYSTEM STATUS - This signal is used to drive a hard disk active LED.
			COPROCESSOR INTERFACE
15	ERROR387	I	ERROR 387 - Driven by the coprocessor, this signal indicates the coprocessor has encountered an error condition which causes an interrupt (13H) to be issued and holds the BUSY386 signal in the busy state. The busy and interrupt are cleared by issuing an 8-bit I/O write command to location 00F0H with data equal to 00H. For 80387/80387SX-based systems, this pin should be connected to the ERROR pin.
14	BUSY387	I	BUSY 387 - Driven by the coprocessor, this signal indicates the coprocessor is currently executing a command. This can also be used on 80386SX/80387SX-based systems.
117	BUSY386	O	BUSY 386 - Indicates the coprocessor is currently executing a command.
8	WTKIRQ13	I	For systems implementing a Weitek 4167/3167 (or compatible) math coprocessor, this pin should be connected to the IRQ13 pin of the EMC (Extended Math Coprocessor) socket. It is used to generate an interrupt 13 to the system when the Weitek coprocessor requires service.
			This pin has dual functions. At power up (trailing edge of RESET), the state of this pin is latched to determine whether the WD6000 will implement an 80386 or 80386SX-compatible math interface.
			For an 80386/80386SX/80486 system, this pin should be pulled down with a 100 ohm resistor.
			For an 80386/80386SX/80486 system which includes a Weitek (or compatible) coprocessor, this pin should be connected to the IRQ13 pin of the Weitek device.
113	PRQ386	O	The PRQ386 signal is OR'ed with the coprocessor request (PEREQ) to drive the PRQ386 signal to the CPU high to allow the coprocessor to complete any pending data transfers.
			EXTERNAL DEVICE ENABLE
28	HLDA	I	BUS HOLD ACKNOWLEDGE - This line indicates when the CPU has given the system local bus to another master (Channel bus master or DMA controller). It is used to prevent non-system CPU access to locations 0000-00FFH in the WD6000 during master cycles.

O = Output, I = Input, I/O = Bi-directional

11

PIN NO.	NAME	TYPE	FUNCTION
EXTERNAL DEVICE ENABLE, Continued			
27	$\overline{\text{PROMCS}}$	I	$\overline{\text{PROM CHIP SELECT}}$ - This signal indicates an access to a PROM location and is activated on read accesses to the PROM address spaces E0000 - FFFFFH, FE0000 - FFFFFFH (80386SX systems), or FFFE0000 - FFFFFFFFH (80386 systems). This line is used by the Wait/Ready in the WD6030 logic to control the length of the channel cycle for PROM accesses.
26	$\overline{\text{DACK}}$	I	$\overline{\text{FLOPPY DMA ACKNOWLDGE}}$ - This pin is activated on a DMA Transfer to the floppy disk. It is used by the Wait/Ready logic in the WD6030 to control the length of the channel cycle for the floppy DMA.
94	$\overline{\text{CS8742}}$	O	$\overline{\text{CHIP SELECT 8742}}$ - This signal is the chip select to the keyboard/auxiliary device controller.
93	$\overline{\text{FDCCS}}$	O	$\overline{\text{FLOPPY DISK CONTROLLER CHIP SELECT}}$ - This signal is the chip select to the floppy disk controller.
90	$\overline{\text{PPCS}}$	O	$\overline{\text{PARALLEL PORT CHIP SELECT}}$ - This signal is the chip select to the parallel port controller.
92	$\overline{\text{SERCS1}}$	O	$\overline{\text{SERIAL CHIP SELECT 1}}$ - This signal is the chip select for the first serial port controller.
91	$\overline{\text{SERCS2}}$	O	$\overline{\text{SERIAL CHIP SELECT 2}}$ - This signal is the chip select for the second serial port controller.
89	$\overline{\text{NPS1}}$	O	$\overline{\text{NUMERIC PROCESSOR SELECT}}$ - This signal is the chip select for the math coprocessor.
118	$\overline{\text{CSA}}$	O	$\overline{\text{CHIP SELECT A}}$ - This signal is a software-programmable chip select.
119	$\overline{\text{CSB}}$	O	$\overline{\text{CHIP SELECT B}}$ - This signal is a software-programmable chip select.
PERIPHERAL BUS CONTROL			
10 9 7 6 5 3 1 132	SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7	I/O	SYSTEM DATA - Theses bi-directional lines are the low byte of data from the Channel data bus (buffered).

IO = Output, I = Input, I/O = Bi-directional

PIN NO.	NAME	TYPE	FUNCTION
			PERIPHERAL BUS CONTROL, Continued
49 48 47 46 45 44 43 42 41 40 39 38 37 36 34 33	SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11 SA12 SA13 SA14 SA15	I	SYSTEM ADDRESS - These 16 address lines are used to decode the appropriate locations of the system CPU 64K I/O space. These lines should be connected to the channel address bus (0...15).
65 64 61	$\overline{S0}$ $\overline{S1}$ M/$\overline{IO}$	I	$\overline{CHANNEL\ STATUS}$ and MEMORY $\overline{I/O}$ - These three lines encode information on the type of Channel bus cycle.
62	$\overline{CMD}$	I	$\overline{COMMAND}$ - This signal defines when data to or from the Channel is valid.
16	$\overline{RESET}$	I	$\overline{RESET}$ - This signal initializes all the internal logic to a power-on state.
105 104 107 106	$\overline{IOR}$ $\overline{IOW}$ $\overline{MEMRD}$ $\overline{MEMWR}$	O	$\overline{I/O\ READ}$, $\overline{I/O\ WRITE}$, $\overline{MEMORY\ READ}$ and $\overline{MEMORY\ WRITE}$ - These signals comprise the command information for peripheral bus cycles and track the Channel cycle.
97	IORDY	O	I/O READY - This signal indicates the WD6000 is finished with the current bus cycle. It is deactivated to extend the current Channel cycle.
112 111 110	$\overline{IODTR}$ $\overline{IODEN}$ IODCBA	O O O	$\overline{I/O\ DATA\ TRANSMIT/RECEIVE}$, $\overline{I/O\ DATA\ ENABLE}$, I/O DATA CLOCK (latches when clock is low) - These three lines control the address and data buffer latches for the peripheral bus. The I/O data transmit/receive signal controls the direction of the I/O data buffers inside the WD6022. If $\overline{IODTR}$ is low, the WD6022 drives data from IOD (0:15) to D (0:15), and if $\overline{IODTR}$ is high, the WD6022 drives data from D (0:15) to IOD (0:15). $\overline{IODEN}$ enables the I/O data buffers. When active, the WD6022 drives either the D (0:15) to IOD (0:15), depending on the direction set by $\overline{IODTR}$. The I/O data clock (IODCBA) is used to latch the data during reads from the Channel peripherals on the I/O bus.

IO = Output, I = Input, I/O = Bi-directional

11

PIN NO.	NAME	TYPE	FUNCTION
			PERIPHERAL BUS CONTROL, Continued
103	RTCAS	O	REAL-TIME CLOCK ADDRESS SELECT - This signal latches the address into the Real-Time Clock module.
102 100	$\overline{\text{RTCRD}}$ $\overline{\text{RTCWR}}$	O	REAL-TIME CLOCK READ/WRITE - These two lines are the command lines to the Real-Time Clock module.
			EXTENDED CMOS RAM INTERFACE
31	$\overline{\text{EDRENA}}$	I	ESF DATA REGISTER PORT ENABLE - This signal from the WD6010 indicates that the ESF Data Register is being read or written to.
80 79 78 77 75 74 73 72 71 70 69 116 114	CMOSA0 CMOSA1 CMOSA2 CMOSA3 CMOSA4 CMOSA5 CMOSA6 CMOSA7 CMOSA8 CMOSA9 CMOSA10 CMOSA11 CMOSA12	O	CMOS ADDRESS - These 13 lines are used to address the Extended CMOS RAM.
85	$\overline{\text{CMOSCS}}$	O	CMOS CHIP SELECT - This line is used to select the Extended CMOS RAM.
			NMI CONTROL
12	$\overline{\text{CHCK}}$	I/O	CHANNEL CHECK - This signal is the channel error indication. It is driven by bus resident adapters. During a bus master DRAM cycle, the system board drives this line if a parity error occurs. When this signal is an output, it is an open collector output.
18	$\overline{\text{PARERR}}$	I	PARITY ERROR - This signal is the output of the DRAM controller parity generator.
82	$\overline{\text{NMI}}$	O	NON-MASKABLE INTERRUPT - When driven by the WD6010 to the CPU, $\overline{\text{NMI}}$ indicates the CACP has reached a bus timeout condition while monitoring the bus. When the signal is received by the WD6010 fromn the WD6000, it instructs the CACP in the WD6010 to initiate an arbitration cycle to remove any bus masters so the the CPU can service the interrupt.

IO = Output, I = Input, I/O = Bi-directional

PIN NO.	NAME	TYPE	FUNCTION
		MISCELLANEOUS	
2,35,68, 86,99,123	V_{DD}	I	+5 Power Supply
11,13,50, 76,88,101 115,125	V_{SS}	I	0 V Ground
63,108, 120	N/C	-	Not Connected
67	$\overline{\text{TEST}}$	I	$\overline{\text{TEST PIN}}$ - This is an active low pin that facilitates board-level testing. When low, this signal tri-states all outputs and bi-directional signal lines, allowing an ATE tester to drive these signals. When high, the outputs and bi-directional lines are enabled by the chip.

IO = Output, I = Input, I/O = Bi-directional

The WD6500 and WD6400SX I/O map is shown in Table 1.

ADDRESS RANGE	LOCATION	FUNCTION
0000 to 000FH	WD6010	DMA Controller, Channels 0-3 [1]
0018H	WD6010	Extended Function Register [1]
001AH	WD6010	Extended Function Execute [1]
0020 to 0021H	WD6000I	Interrupt Controller 1 (Master)
0040, 0042-0044, 0047H	WD6000	System Timers
0060H	WD6000	Keyboard Data Port
0061H	WD6000	System Control Port B
0064H	WD6000	RD=Kybd status, WR=Kybd command
0070H	WD6000	RTC/CMOS Addr. Register, NMI Mask
0071H	WD6000	RTC/CMOS Data Port
0074H	WD6000	EAR0 Extended CMOS RAM, ESF
0075H	WD6000	EAR1 Extended CMOS RAM
0076H	WD6000	Extended CMOS RAM data port
0081 to 0083, 0087H	WD6010	DMA Page Registers (0-3)[1]
0089 to 008B, 008FH	WD6010	DMA Page Registers (4-7)[1]
0090H	WD6010	Central Arbitration Control Point [1]
0091H	WD6000	Card Selected Feedback
0092H	WD6000	System Control Port A
0094H	WD6000	System Board Setup
0096, 0097H	WD6000	POS, Channel Connector Select
00A0 to 00A1H	WD6000	Interrupt Controller 2 (Slave)
00C0 to 00DFH	WD6010	DMA Controller (4 to 7)[1]
00F0H	WD6000	Coprocessor Clear Busy
00F1H	WD6000	Coprocessor Reset
00F8 to 00FFH	WD6000	Coprocessor
0100, 0101H	WD6000	System ID
0102 to 0107H	WD6000	System Board Configuration (POS)
0278 to 027BH	WD6000	Parallel Port 3
02F8 to 02FFH	WD6000	Alternate Serial Port
0378 to 037BH	WD6000	Parallel Port 2
03BC to 03BFH	WD6000	Parallel Port 1
03B4, 03B5, 03BA, 03C0-03C5H	VIDEO	Video Subsystem [2]
03CE, 03CF, 03D4, 03D5, 03DAH	VIDEO	Video Subsystem [2]
03C6 to 03C9H	VIDEO	Video DAC [2]
03F0 to 03F7H	WD6000	Diskette Drive Controller
03F8 to 03FFH	WD6000	Primary Serial Port
0700H	WD6010	ESF Data Register (Default)

[1] No Channel cycle is generated on these I/O addresses
[2] I/O location 03C3H (VGA Enable Register) is in WD6010.

TABLE 1. SYSTEM LEVEL I/O MAP

3.0 INTERRUPT CONTROLLER

The Interrupt Controller is functionally equivalent to two Intel 8259 controllers cascaded together. It operates in level-sensitive mode and controls sixteen levels of interrupts, five interna,l and eleven system interrupts. Interrupt Controller 1 is the master controller, located at I/O space 0020H and 0021H. Interrupt Controller 2 is the slave and is located at I/O space 00a0H and 00A1H. Interrupt Request 2 (IRQ2) from Interrupt Controller 1 is used to cascade the two controllers, as illustrated in Figure 4.

The edge trigger mode is not available. Any or all of the interrupts may be masked. The non-maskable interrupt may be masked by setting Register (0070H) Bit 7.

Interrupts may be shared by more than one hardware interrupt. Table 2 shows the interrupt assignments in a typical system environment.

The auxiliary and serial port interrupt signals are discussed below:

- AUXINT is the interrupt from the auxiliary device. It is an active high input that is ORed with IRQ12 from the Channel. It is treated exactly like an IRQ12 interrupt.
- SERINT1 is an active high interrupt from Serial Port 1 (SP1). SERINT1 is masked by $\overline{\text{INT1EN}}$, which must be low in order to detect SERINT1. SERINT1 is ORed with IRQ3 or IRQ4, depending on the programming. If SP1 is enabled (See Section 4.0), and it is programmed to Alternate Addresses 02F8 - 02FFH, SERINT 1 is treated as IRQ3. It is treated as IRQ4 when SP1 is programmed to Primary Addresses 03F8 - 03FFH.
- SERINT2 is an active high interrupt from Serial Port 2 (SP2). SERINT2 is masked by $\overline{\text{INT2EN}}$, which must be low in order to detect SERINT2. SERINT2 is ORed with IRQ3 or IRQ4, depending on the programming. If SP2 is enabled (See Section 9.2.3), and it is programmed to Primary Addresses 03F8 - 03FFH, SERINT2 is treated as IRQ4. It is treated as IRQ3 when SP2 is programmed to Alternate Addresses 02F8 - 02FFH.

3.1 INTERRUPT CONTROLLER OPERATION

Figure 5 contains a functional diagram of an interrupt controller in the WD6000, providing an operational representation of how each controller works. The various interrupt controller functions are described below.

3.1.1 Interrupt Request Register (IRR) and In-Service Register (ISR)

Interrupts are handled by the IRR and the ISR. The IRR stores all the interrupt levels that are being serviced.

3.1.2 Priority Resolver

This function decodes the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during the INTA cycle.

3.1.3 Interrupt Mask Register

The IMR stores the bits that mask selected interrupt lines. Masking a higher priority input does not affect lower priority interrupt request lines.

3.1.4 Read/Write Control Logic

This function accepts commands from the CPU and allows the status of the Interrupt Controller to be read on the Data Bus. It contains the Initialization Command Word (ICW) and Operation Command Word (OCW) registers, that store the various control formats for device operation.

3.1.5 Cascade Buffer/Comparator

This function stores and compares the ID of the slave controller. In the WD6000 Interrupt Controller configuration, the CAS bus is an output from the master and an input to the slave. When a slave request line is activated and acknowledged, the master sends the ID of the slave, fixed at 2, to the CAS bus. This enables the slave to send its pre-programmed subroutine address to the data bus during the second INTA cycle. All handshaking is handled internally.

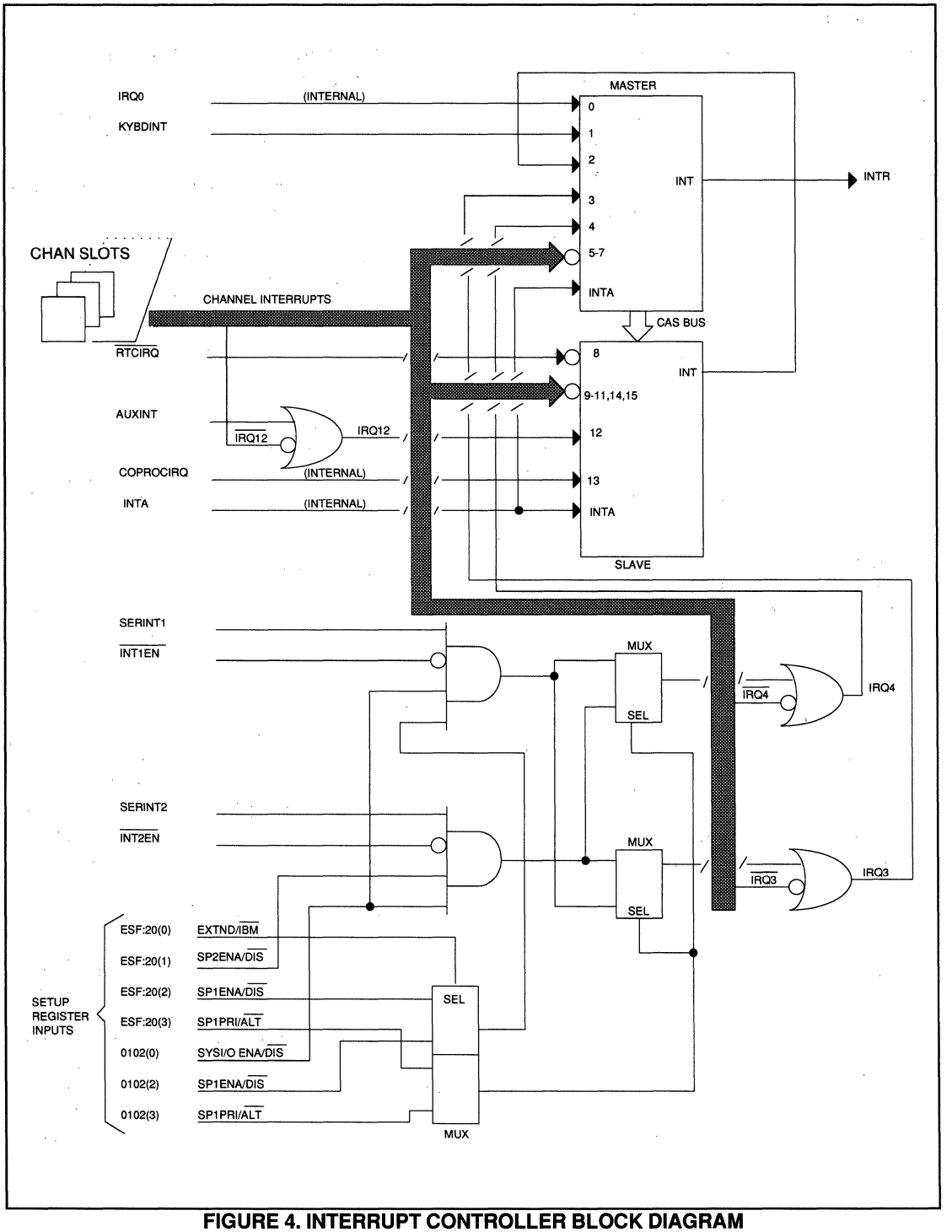


FIGURE 4. INTERRUPT CONTROLLER BLOCK DIAGRAM

SYSTEM SOURCE	CHANNEL	LEVEL
Timer	-	0 [1]
Keyboard Port	-	1
Cascade	-	2 [1]
Alternate Srial Port	IRQ3	3
Primary Serial Port	IRQ4	4
Reserved	IRQ5	5
Floppy Disk	IRQ6	6
Parallel Port	IRQ7	7
RTC	-	8
Cascade Redirectd	IRQ9	9
Reserved	IRQ10	10
Reserved	IRQ11	11
Mouse/Auxiliary	IRQ12	12
Coprocessor	-	13 [1]
Hard Disk	IRQ14	14
Reserved	IRQ15	15

[1] This interrupt is internally generated in the WD6000.

TABLE 2. INTERRUPT SHARING

3.2 INTERRUPT SEQUENCE

The sequence of events that make up an interrupt system environment are described below:

1. One or more interrupts arrive from a peripheral device which sets the corresponding bit(s) in the IRR.

2. The request is evaluated and if the interrupt has not been masked, it is passed to the priority circuit and the Interrupt Controller sends an interrupt (INTR) to the CPU.

3. The CPU responds to the interrupt with an INTA cycle.

4. When the INTA is received, the priority is frozen and the highest priority ISR bit is set. The Interrupt Controller does not drive the data bus during this cycle.

5. The CPU initiates another INTA cycle that causes the Interrupt Controller to send an 8-bit vector to the CPU. Either the master or slave may be programmed to send the byte of data. As long as the ISR bit is set, all interrupts at the same level or lower are inhibited. In Special Mask Mode (SMM), only interrupts at the same level are inhibited. If a higher priority interrupt occurs during an interrupt service routine, it is only acknowledged if the CPU internal interrupt enable has been re-enabled.

When the slave issues an interrupt, other interrupts from the slave are locked out. To preserve priority in the slave, that is, to allow higher interrupts to occur when a power interrupt is being serviced, Special Fully Nested Mode (SFNM) should be programmed in the master. See Section 2.9.4 for more details.

6. At the end of the second INTA cycle, one or two End-of-Interrupt (EOI) commands must be issued to complete the interrupt; one for the master and the other for the slave. This clears the appropriate bit in the ISR.

3.3 END OF INTERRUPT

There are three EOI commands: Specific, Non-Specific, and Automatic. When the Interrupt Controller is programmed to operate in modes that preserve fully nested interrupts, the CPU can determine which ISR bit to reset on EOI, since the

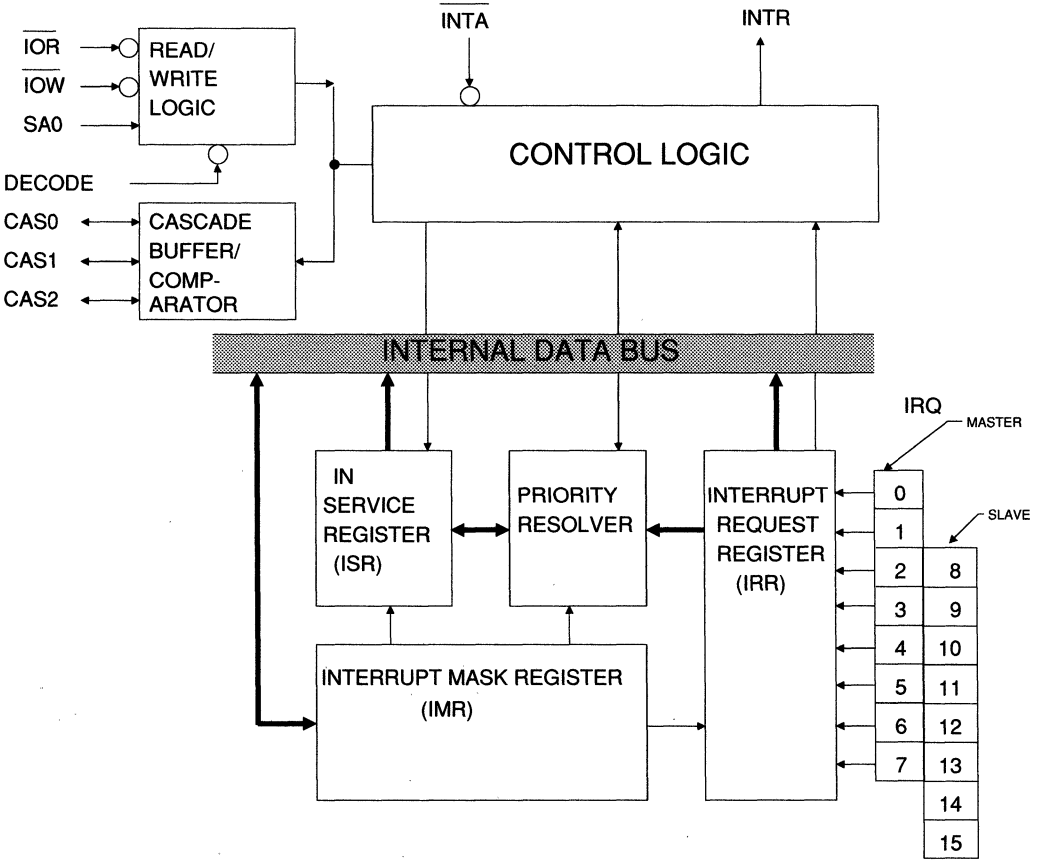


FIGURE 5. INTERRUPT CONTROLLER FUNCTIONAL DIAGRAM

(TYPICAL MASTER OR SLAVE)

current highest priority ISR bit is necessarily the last level acknowledged and serviced. In this case, a non-specific EOI can be issued. In Special Mask Mode, an ISR bit that is masked in the IMR is not cleared by a non-specific EOI.

When the fully nested structure is not preserved, a Specific EOI must be issued at the end of the interrupt service routine, which includes the ISR bit to reset. Both Specific and Non-Specific EOIs are issued with OCW2.

Automatic EOI (AEOI) automatically occurs on the trailing edge of the second INTA cycle. AEOI can only be used for the master, not the slave. AEOI is set with ICW4.

3.4 POLLED MODE

The Interrupt Controller may also be operated in Polled Mode. In this mode, interrupts should be masked by the CPU. An interrupt is detected when the software issues a poll command, setting P = 1 in OCW3. This results in an equivalent INTA cycle during the next read operation to the Interrupt Controller (i.e., IOR = 0, DECODE = 0) which sets the IS bit, if a request was made, and allows the priority level to be read. See Figure 6. The IRR remains frozen until the read cycle is complete. At the end of the process, Polled Mode is reset to zero.

D7	D6	D5	D4	D3	D2	D1	D0
I	-	-	-	-	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

I: Equal to "1" if there is an interrupt.

FIGURE 6. INTERRUPT PRIORITY LEVEL USING THE POLL COMMAND

3.5 INTERRUPT PRIORITY

There are three types of interrupt priority:

- Fixed Priority
- Automatic Rotation
- Specific Rotation

3.5.1 Fixed Priority

In this mode, the interrupts are fully nested; IRQ0 is assigned the highest priority, and IRQ7 the lowest priority. Fixed priority is the default condition, unless Automatic or Specific Rotation is programmed with OCW3.

3.5.2 Automatic Rotation

Automatic Rotation is useful for applications where a number of interrupting devices have equal priority, as the priority is rotated between them. In this mode, the last interrupt serviced has the lowest priority. Figures 7 and 8 show the status of the ISR before and after Automatic Rotation. Once the interrupt with the highest priority (IRQ4 in Figure 7) has been serviced, its status changes from the highest to the lowest priority, as illustrated in Figure 7.

IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
0	1	0	1	0	0	0	0

IRQ STATUS

Lowest Priority ... Highest Priority

3	2	1	0	7	6	5	4

PRIORITY STATUS

FIGURE 7. INTERRUPT PRIORITY BEFORE AUTOMATIC ROTATION

IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
0	1	0	0	0	0	0	0

IRQ STATUS

Lowest Priority ... Highest Priority

4	3	2	1	0	7	6	5

PRIORITY STATUS

FIGURE 8. INTERRUPT PRIORITY AFTER AUTOMATIC ROTATION

3.5.3 Specific Rotation

Specific Rotation fixes the priorities by assigning one interrupt the lowest priority, and thus changing the priorities of the rest. For example, if IRQ4 is programmed to have the lowest priority, then the new order of priority is 5, 6, 7, 0, 1, 2, 3, and 4, with IRQ5 having the highest priority and IRQ4 the lowest priority.

Specific Rotation is programmed with OCW2 in two ways, Rotate on Specific EOI, and Set Priority. Note that priority changes can only be made during an EOI command by using Rotate on Specific EOI.

3.6 SPECIAL MASK MODE

Special Mask Mode (SMM) allows the interrupt priority structure to be dynamically changed. In SMM, when a bit is masked in OCW1, interrupts are inhibited at that level; all other levels, lower or higher, that are not masked are enabled. This selectively enables interrupts by changing the IMR. SMM is programmed with OCW3.

3.7 READING REGISTER STATUS

The status of the IRR and ISR can be read at Address 020H (master) and 0A0H (slave). Prior to the read status operation, indicate the register to be read with OCW3. The contents of the selected register can be read again, unless Polled Mode is selected, that is, there is no need to write another OCW3 to read the same register.

The IMR can be read at Addresses 021H and 0A1H.

3.8 INTERRUPT TRIGGERING

An interrupt request is recognized by a low level on the $\overline{IRQ}$ input. The interrupt request must be removed before the EOI is issued or before the CPU internal interrupt enable has been re-enabled. Otherwise, a second interrupt is detected.

The $\overline{IRQ}$ inputs must remain low until after the falling edge of the first $\overline{INTA}$ as generated from interrupt acknowledge cycles from the CPU. See Figure 9. If the $\overline{IRQ}$ goes high before this time, the Interrupt Controller issues an Interrupt Level 7 vector during the second INTA cycle, thus ignoring the false interrupt. This allows false interrupts caused by spurious noise glitches on the interrupt inputs to be detected.

If IRQ7 is needed for another purpose, a false IRQ7 can still be detected by reading the ISR. A normal IRQ7 sets the corresponding ISR bit; a false IRQ7 does not, except when a false IRQ7 occurs during a normal IRQ7. In this case, it is necessary to keep track of IRQ7 occurrences to determine default occurrences that may follow.

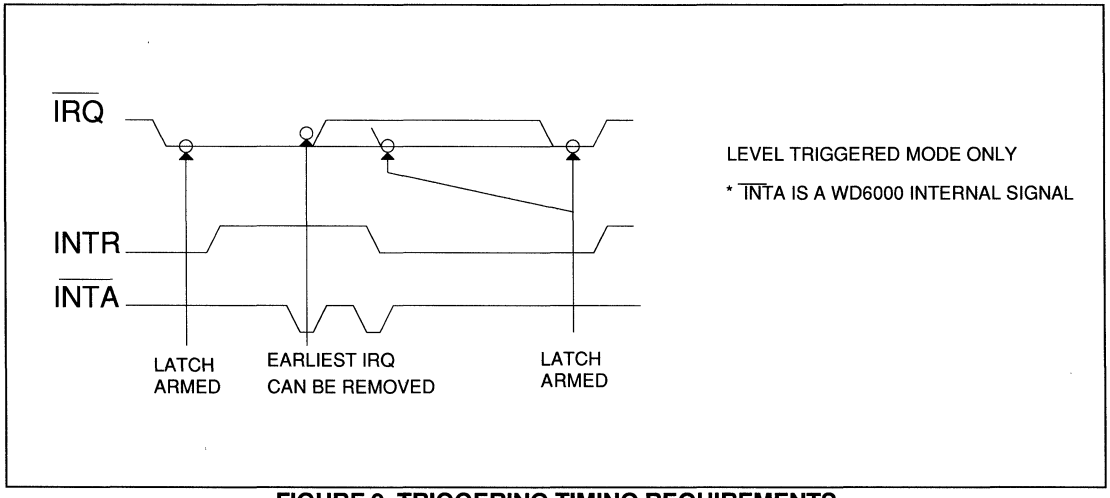


FIGURE 9. TRIGGERING TIMING REQUIREMENTS

(NOTE: I/O ADDRESS 20/21H APPLIES TO MASTER, A0/A1H APPLIES TO SLAVE)

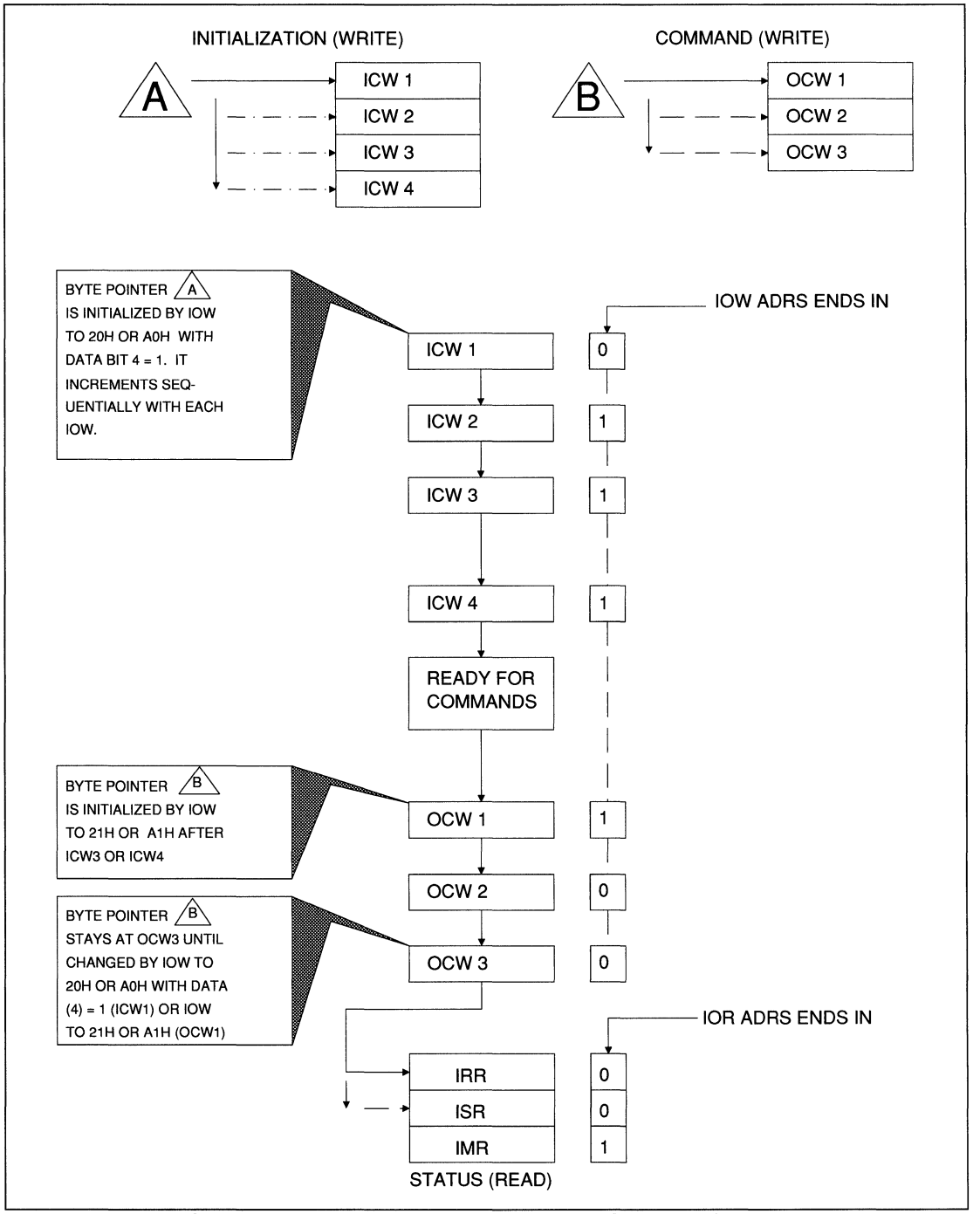


FIGURE 10. INTERRUPT CONTROLLER PROGRAMMING MODEL

(NOTE: I/O ADDRESS 20/21H APPLIES TO MASTER, A0/A1H APPLIES TO SLAVE)

3.9 PROGRAMMING

The Interrupt Controller is initialized by writing a series of Initialization Command Words (ICWs) to each controller, whether master or slave. See Figure 10 for more information. After initialization, the controllers are ready to accept interrupt requests. Operation Control Words (OCWs) can then be used to change operating modes and command the controllers for various functions. The master and slave can be programmed to work in different modes.

Table 3 indicates each read/write function and its corresponding address for Interrupt Controllers 1 and 2, master and slave respectively.

INTERRUPT CONTROLLER	ADDRESS	FUNCTION	READ/WRITE
1	020	ICW1	Fixed
1	021	ICW2	Write
1	021	ICW3	Write
1	021	ICW4	Write
1	021	OCW1	Write
1	020	OCW2	Write
1	020	OCW3	Write
1	020	IRR	Read
1	020	ISR	Read
1	021	IMR	Read
2	0A0	ICW1	Write
2	0A1	ICW2	Write
2	0A1	ICW3	Write
2	0A1	ICW4	Write
2	0A1	OCW1	Write
2	0A0	OCW2	Write
2	0A0	OCW3	Write
2	0A0	IRR	Read
2	0A0	ISR	Read
2	0A1	IMR	Read

TABLE 3. INTERRUPT CONTROLLER FUNCTION MAP

3.9.1 Initialization Command Word 1 (ICW1)

The initialization sequence is started by writing ICW1 to Address 020H or 0A0H. ICW1 has a fixed format, illustrated in Figure 11. Initialization accomplishes the following:

1. The Interrupt Mask Register is cleared.
2. Fixed Priority Mode is selected.
3. The Slave Mode address is set to 2.
4. Special Mask Mode is cleared.
5. IRR is set for Status Read.

The next three commands to Addresses 021H or 0A1H load ICW2 through ICW4.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
-		-		-		-		LVL TRIG MODE		-		CASCADE MODE		ICW4 NEEDED	
0		0		0		1		1		0		0		1	

FIGURE 11. ICW1

▒ = Nonprogrammable

3.9.2 Initializaation Command Word 2 (ICW2)

Bits 3-7 are the five most significant bits of the interrupt vector (T3-T7); they are programmable by the CPU. Bits 0-2 are generated by the Priority Resolver during the INTA cycle, according to the interrupt level. Refer to Table 2. Figure 12 shows the format for ICW2.

11

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
INTERRUPT LEVEL HAS SLAVE															
YES	NO	YES	NO	YES	No	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO
0		0		0		0		0		0		1		0	

			LEVEL	
D2	D1	D0	MASTER	SLAVE
0	0	0	0	8
0	0	1	1	9
0	1	0	2	10
0	1	1	3	11
1	0	0	4	12
1	0	1	5	13
1	1	0	6	14
1	1	1	7	15

FIGURE 12. ICW2 FORMATS

3.9.3 Initialization Command Word 3 (ICW3)

ICW3 initializes the master and slave. For the master, ICW3 sets a 1 for each IRQ input used to cascade a slave. For the slave, bits 0-2 of ICW3 provide the Slave Mode address. Figure 13 shows the format for ICW3 for master and slave. The formats are fixed and must be written as shown in order to function.

7	6	5	4	3	2	1	0
1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0
INTERRUPT LEVEL HAS SLAVE							
YES NO	YES NO	YES No	YES NO	YES NO	YES NO	YES NO	YES NO
0	0	0	0	0	0	1	0

D2	D1	D0	SLAVE ID = 2
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

FIGURE 13. ICW3 FORMATS

3.9.4 Initialization Command Word 4 (ICW4)

ICW4 is used to program Special Fully Nested Mode (SFNM) and Automatic End of Interrupt (AEOI). See Figure 14 for details.

7	6	5	4	3	2	1	0
1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0
-	-	-	SPECFULLY NESTMODE	-	-	AUTO EOI	-
0	0	0	YES NO	0	0	AUTO NOR	

FIGURE 14. ICW4

= Non-programmable

3.9.5 Operation Control Word 1 (OCW1)

OCW1 sets and clears the mask bits in the IMR. See Figure 15. M0-M7 represent the eight mask bits, where M0 controls IRQ0, M1 controls IRQ1, and so on. Programming a 1 indicates that the interrupt is masked.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
M7/S15		M6/S14		M5/S13		M4/S12		M3/S11		M2/S10		M1/S9		M0/S8	
YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO

Mn = Master Mask Bit
Sn = Slave Mask Bit

FIGURE 15. OCW1 (MAS REG)

3.9.6 Operation Control Word 2 (OCW2)

Bits 5-7 (EOI, SL and R) of COW2 control the EOI and Rotate modes and combinations of the two. See Figure 16. Bits 0-2 (L0-L2) of OCW2 determine which interrupt is affected when Bit 6 is active.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
R		SL		EOI		-		-		IRQ LEVEL					
-		-		-		0		0		L2		L1		L0	

D2	D1	D0	FUNCTION
0	0	0	Non-specific EOI Command
0	1	1	Specific EOI Command
1	0	1	Rotate Non-specific EOI command
1	0	0	Rotate In Automatic EOI Mode (set)
0	0	0	Rorate in Automatic EOI Mode (Clr)
1	1	1	*Rotate on Specific EOI Command
1	1	0	*Set Priority Command
0	1	0	No Operation

*L0-L2 ARE USED

L2	L1	L0	IRQ LEVEL MASTER	IRQ LEVEL SLAVE
0	0	0	0	8
0	0	1	1	9
0	1	0	2	10
0	1	1	3	11
1	0	0	4	12
1	0	1	5	13
1	1	0	6	14
1	1	1	7	15

= Non-programmable

FIGURE 16. OCW2

3.9.7 Operation Control Word 3 (OCW3)

Bits 5 and 6 program Speciao Mask Mode (SMM). Sets Bits 5 (SMM) and 6 (ESMM) to 1 to program SMM. Refer to Figure 17. If SMM is set to zero, it resets the controller to Normal Mask Mode. Polled Mode is enabled when Bit 2 is set to 1.

Set Bit 1 (RR) and Bit 0 (RIS) to 0 to read the status of the ISR on SD0-SD7 at Address 020H or 0A0H. Set Bit 1 to 1 and Bit 0 to 0 to read the status of the IRR on SD0-SD7 at Address 020H or 0A0H.

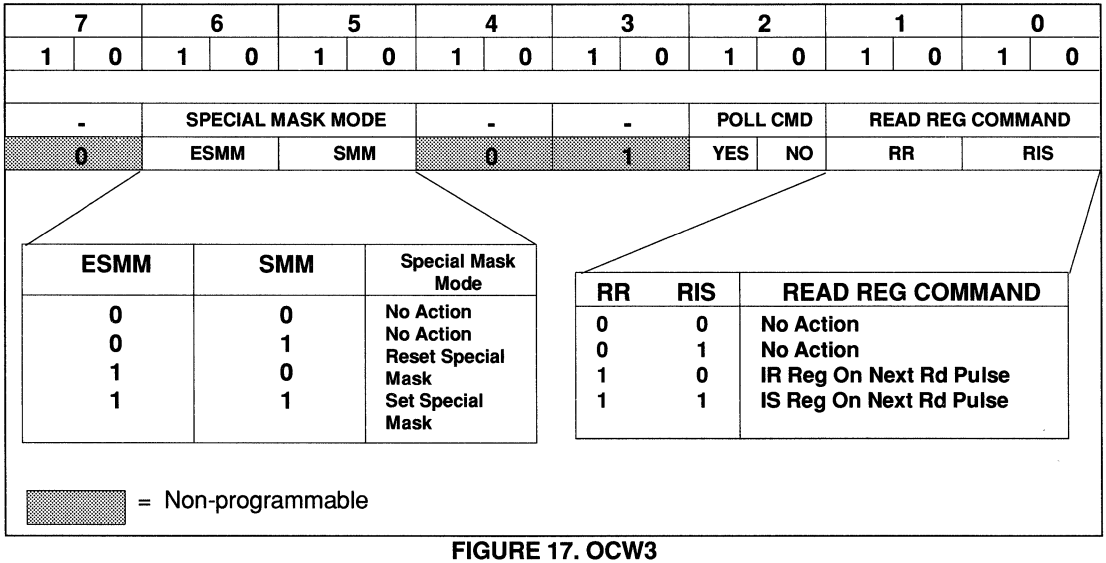


FIGURE 17. OCW3

4.0 TIMERS AND CLOCK GENERATION

The WD6000 has four counters of timers designated Timers 0, 1, 2 and 3. See Figure 18.

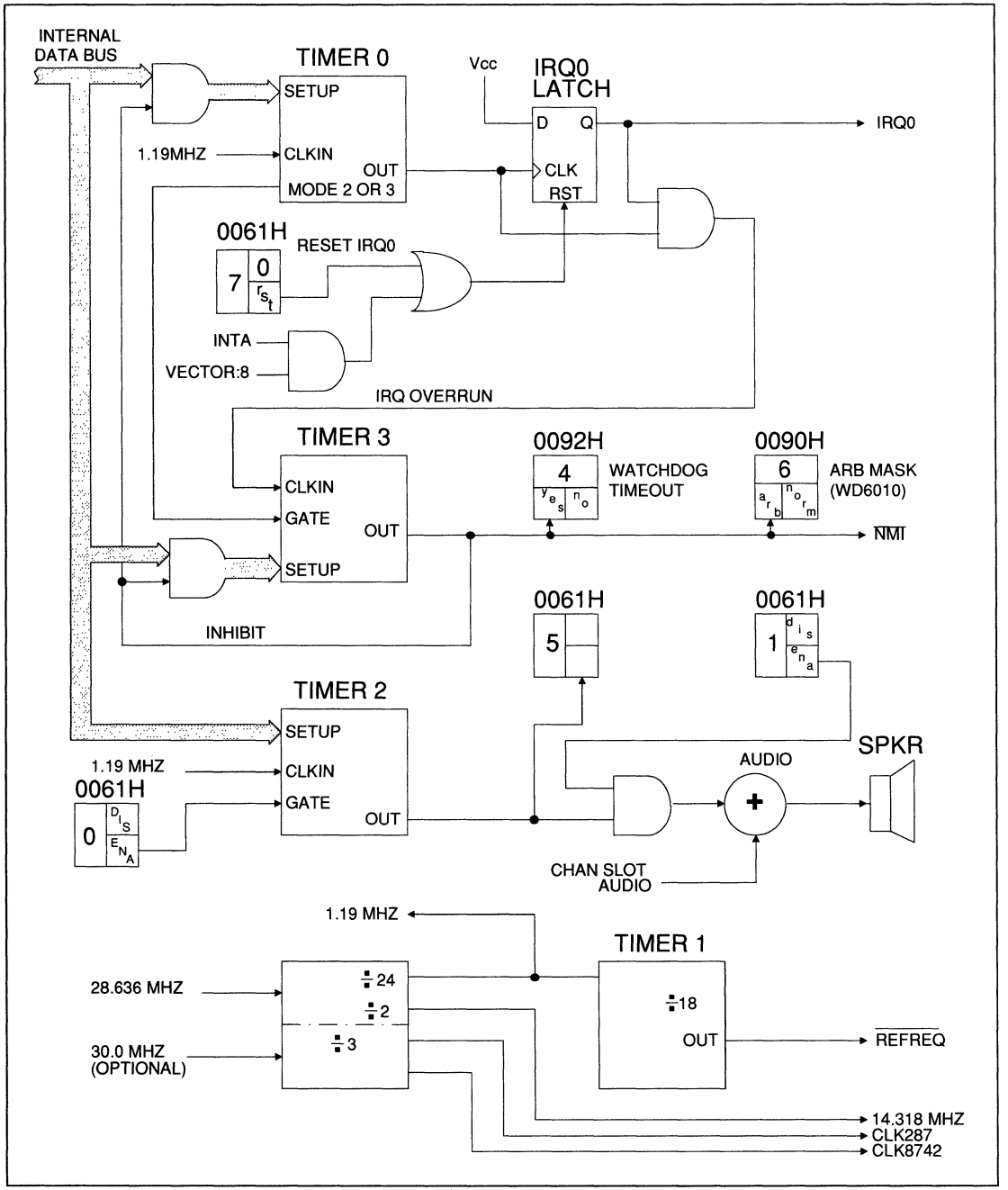


FIGURE 18. SYSTEM TIMER FUNCTIONAL BLOCK DIAGRAM

4.1 TIMERS

Timer 1 generates Refresh requests, and is not programmable. REFREQ is generated based on a 1.19 MHz clock divided by 18 (28.636 MHz divided by 24).

Timer 1 also generates the clocks to the 80387/80387SX and 8742 devices. The MHZ30 clock input is optional, making a lower cost implementation possible. If a MHZ30 clock input is connected to a 30.0 MHz clock, the output clock is 10 MHz. If not, this pin will be connected to a MHZ28 pin, in which case the output to the 8742 device will be 9.54 MHz.

Timers 0 and 2 are 16-bit, programmable binary or BCD down counters. Timer 3 is an 8-bit binary down counter which can be preset. All three timers are fully independent and can be programmed, except as noted, to operate in the modes shown in Table 4. Addresses 0040H, 0042H, and 0044H are the data ports for Timers 0, 2, and 3, respectively. Timers 0 and 2 are 16-bit, programmable, binary or BCD 16-bit synchronous down counters that can be preset.

MODE	DESCRIPTION
0	Interrupt on Terminal Count
1	Hardware Retriggerable One Shot (Timer 2 only)
2	Rate Generator
3	Square Wave
4	Software Retriggerable Strobe

TABLE 4. COUNTER OPERATING MODES

ADDRESS	FUNCTION
040H	Timer 0 Read/Write
042H	Timer 2 Read/Write
044H	Timer 3 Read/Write
043H	Control Word Reg. (Timer 0 or 3) Write Only
047H	Control Word Reg. (Timer 3) Write Only

TABLE 5. COUNTER/TIMER ADDRESS MAP

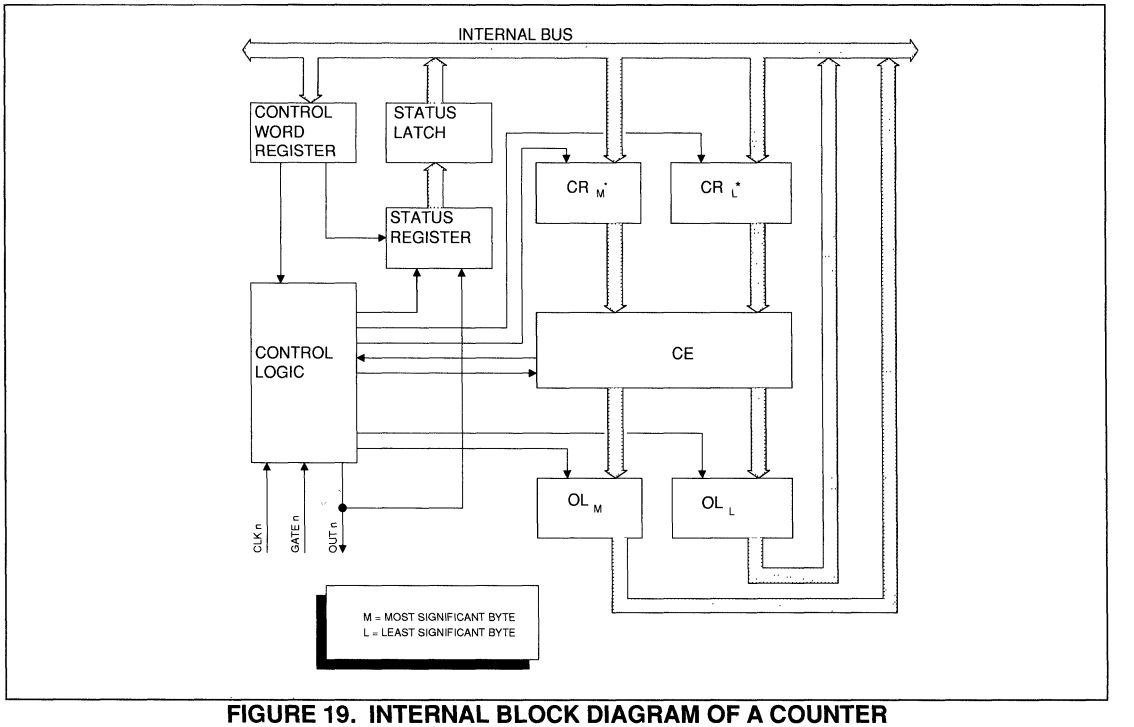


FIGURE 19. INTERNAL BLOCK DIAGRAM OF A COUNTER

4.2 PROGRAMMING

At power-up the counter mode, count value, and output of all counters and registers is undefined. Each counter must be programmed before it can be used.

Counters are programmed by writing a Control Word to the Control Word Register followed by an initial count. The Control Word indicates the counter being programmed and the format of the initial count (e.g. most significant only). Figure 20 shows the format for the Control Word for Timers 0 and 2 and 3 at their respective addresses.

4.2.1 Write Operations

When writing to each counter, the Control Word must be written before the initial count is written and the initial count must follow the format specified in the Control Word. As long as the conventions in the Control Word formats are followed, no particular programming sequence is required.

A new initial count may be written to a counter at any time without affecting the programmed mode of the counter, provided the programmed format is followed. Counting is affected as described in the mode definitions.

---------- Important ----------

When writing two-byte counts, do not transfer control to another routine that writes into the same counter between the first and second bytes. If you do so, the counter is loaded with an incorrect count.

4.2.2 Read Operations

The counters can be read in three ways: a read operation, the Counter Latch Command, and the Read-Back Command. A simple read operation to a counter requires that the CLK input of the selected counter be inhibited by using the GATE input. If it is not inhibited, a false reading could result because the counter may change during the read.

7	6	5	4	3	2	1	0
1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0
SELECT COUNTER		READ/WRITE MODE		PROGRAM MODE			COUNT MODE
SC1	SC0	RW1	RW0	M2	M1	M0	BCD BNY

SC1 SC0	SELECT COUNTER	RW1 RW0	READ/WRITE MODE	M2 M1 M0	PROGRAM MODE
0 0	Select Counter 0	0 0	Counter Latch Command	0 0 0	0
0 1	Reserved		(see Read Operations)	0 0 1	1
1 0	Select Counter 2	0 1	Read/ Write	X 1 0	2
1 1	Read-back Command (See Read Operations)		least significant byte only	X 1 1	3
		1 0	Read/Write	1 0 0	4
			most significant byte only	1 0 1	5
		1 1	Read/Write		
			least significant byte first, then most significant byte		

(Register 0043H W/O)

SELECT COUNTER		SETUP MODE		RESERVED
SC1	SC0	RW1	RW0	0

SC1 SC0	SELECT COUNTER
0 0	Select Counter 3
0 1	Reserved
1 0	Reserved
1 1	Reserved

RW1 RW0	SETUP MODE
0 0	Counter 0 Latch Command
0 1	Read/Write least significant byte only
1 0	Reserved
1 1	Reserved

(Register 0047H W/O)

= Nonprogrammable

FIGURE 20. CONTROL WORD FORMATS

7	6	5	4	3	2	1	0
-	-	STATUS/COUNTER SELECT		COUNTER SELECTED			-
1	1	- CNT	- STS	COUNTER2	COUNTER1	COUNTER0	0

FIGURE 21. READ-BACK COMMAND

Important

When reading two-byte counts, do not transfer control to another routine that reads from the same counter between the first and second byte. This could result in an incorrect count being read.

Counter Latch Command—When a Counter Latch Command is issued in a Control Word (see Figure 20), the output latches OLs of the selected counter latch, the current count of the CE. The count remains latched until read by the CPU or until the counter is reprogrammed. A subsequent counter latch command for the same counter is ignored if issued before the latches are read. A Counter Latch Command may be issued to more than one counter. It does affect the programmed mode of the counter.

Read-Back Command—When a Read-Back Command is issued in a Control Word (see Figure 21), the count, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter(s) can be checked. The Read-Back Command can be used to latch multiple counter output latches OLs by setting D5 = 0 and by selecting the desired counter(s). This command is equivalent to several counter latch commands; one for each counter latched. As with the counter latch command, counts are held until read by the CPU or until the counter is reprogrammed.

OUTPUT	COUNT		READ/WRITE MODE		PROGRAM MODE			COUNT MODE	
STATE	NULL	AVAIL	RW1	RW0	M2	M1	M0	BCD	BNRY

Counter 0, 2 Status Byte

RW1	RW0	READ/WRITE MODE	M2	M1	M0	PROGRAM MODE
0	0	Counter Latch Command	0	0	0	0
		(see Read Operations)	0	0	1	1
0	1	Read/Write least significant byte only	X	1	0	2
1	0	Read/Write most significant byte only	X	1	1	3
1	1	Read/Write least significant byte first, then most significant byte	1	0	0	4
			1	0	1	5

OUTPUT	COUNT		READ/WRITE MODE		RESERVED
STATE	NULL	AVAIL	RW1	RW0	0

Counter 3 Status Byte

RW1	RW0	READ/WRITE MODE
0	0	Counter 0 Latch Command
0	1	Read/Write least signif. byte only
1	0	Reserved
1	1	Reserved

FIGURE 22. COUNTER STATUS BYTES

COMMAND								DESCRIPTION	RESULT
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status-Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count-Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read bacvk count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Cntr 1

FIGURE 23. READ-BACK COMMAND EXAMPLES

Status information of the selected counter(s) can be latched by the Read-Back Command by setting status bit D4 = 0. The status is latched until read by the CPU with a read operation to the counter or until the counter is reprogrammed. Figure 21 shows the format for the counter status. Bits 0–5 indicate the programmed status of the counter as written into the Control Word Register.

D7 (Figure 22) allows the counter output to be monitored. The Null Count (NC) flag indicates the condition of the CE. NC = 1 during a write operation to the Control Word Register or the counter. NC = 0 when a new count is loaded from the CRs to the CE. If the counter is programmed for two-byte counts, NC = 1 when the second byte is written.

Both the count and status of the selected counter(s) may be latched simultaneously by setting D4 and D5 to 0. This command is equivalent to two read-back commands.

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

Note: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

FIGURE 24. MINIMUM AND MAXIMUM INITIAL COUNTS

If both the count and the status are latched with a read-back command, the first read operation to the selected counter(s) returns the status. The next read, or two reads if the counter is programmed for two-byte counts, returns the latched count. Subsequent reads return unlatched counts.

4.3 COUNTER OPERATION

Each counter may be set in one of five modes by writing a Control Word. When a Control Word is written to a counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulse is required.

New counts are loaded and counters are decremented on the falling edge of CLK. The maximum possible initial count is 0-equivalent to 65536 in binary operation or 10000 in BCD. The counter does not stop when it reaches 0. In Modes 0, 1, 4, and 5 it wraps around to the highest count (FFFF in binary operation or 9999 in BCD). In Modes 2 and 3, the counter is reloaded with the initial count and continues counting. Figure 24 shows minimum and maximum initial counts for each mode.

The GATE input is level-sensitive in Modes 0, 2, 3, and 4 and is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. A rising edge (trigger) sets an internal flip-flop whose output is sampled on the next rising edge of CLK. The flip-flop resets immediately after it is sampled. Note that in Modes 2 and 3, the GATE input is both edge-and-level-sensitive.

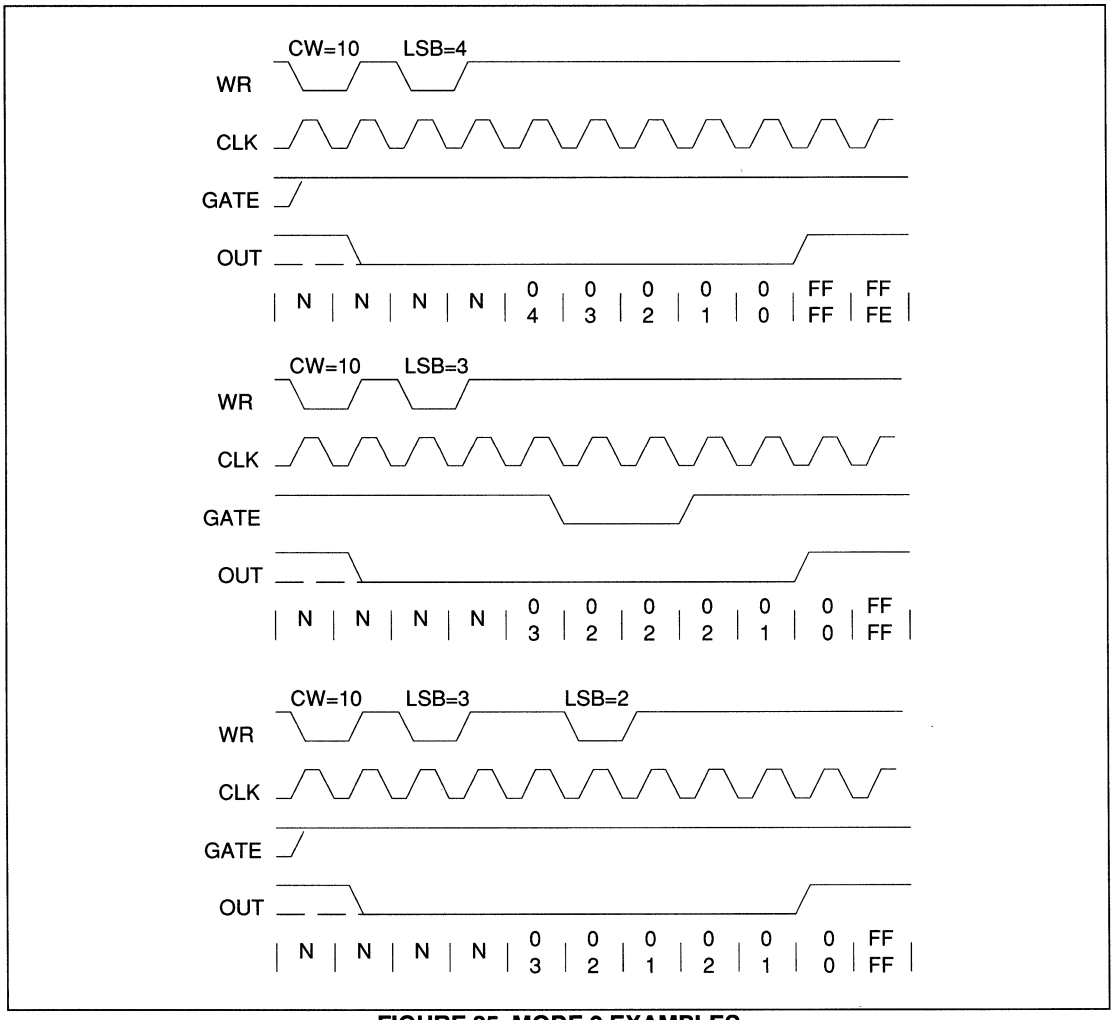


FIGURE 25. MODE 0 EXAMPLES

4.3.1 Mode 0—Interrupt on Terminal Count

Mode 0 is typically used for event counting. Writing the Control Word causes OUT to go low and remain low until the counter reaches 0. At this time OUT goes high and remains high. The counter continues to run until a new count or Control Word is written. Counting is enabled when GATE = 1. Disabling the count (GATE = 0) has no effect on OUT.

The initial count is loaded into the CE on the next CLK pulse after the Control Word and initial count are written. For an initial count of N, OUT goes high N+1 CLK pulses later. Writing a new count reloads the counter (CE) on the next CLK pulse and counting continues from the new count.

When writing a two-byte count, the first byte disables counting and OUT is set low. After writing the second byte, the new count is loaded on the next CLK pulse. This allows the counting sequence to be synchronized by the software.

If an initial count is written when GATE = 0, it is still loaded on the next CLK pulse. When GATE = 1, counting begins and OUT goes high N CLK pulses later. Figure 25 shows examples of Mode 0 operation.

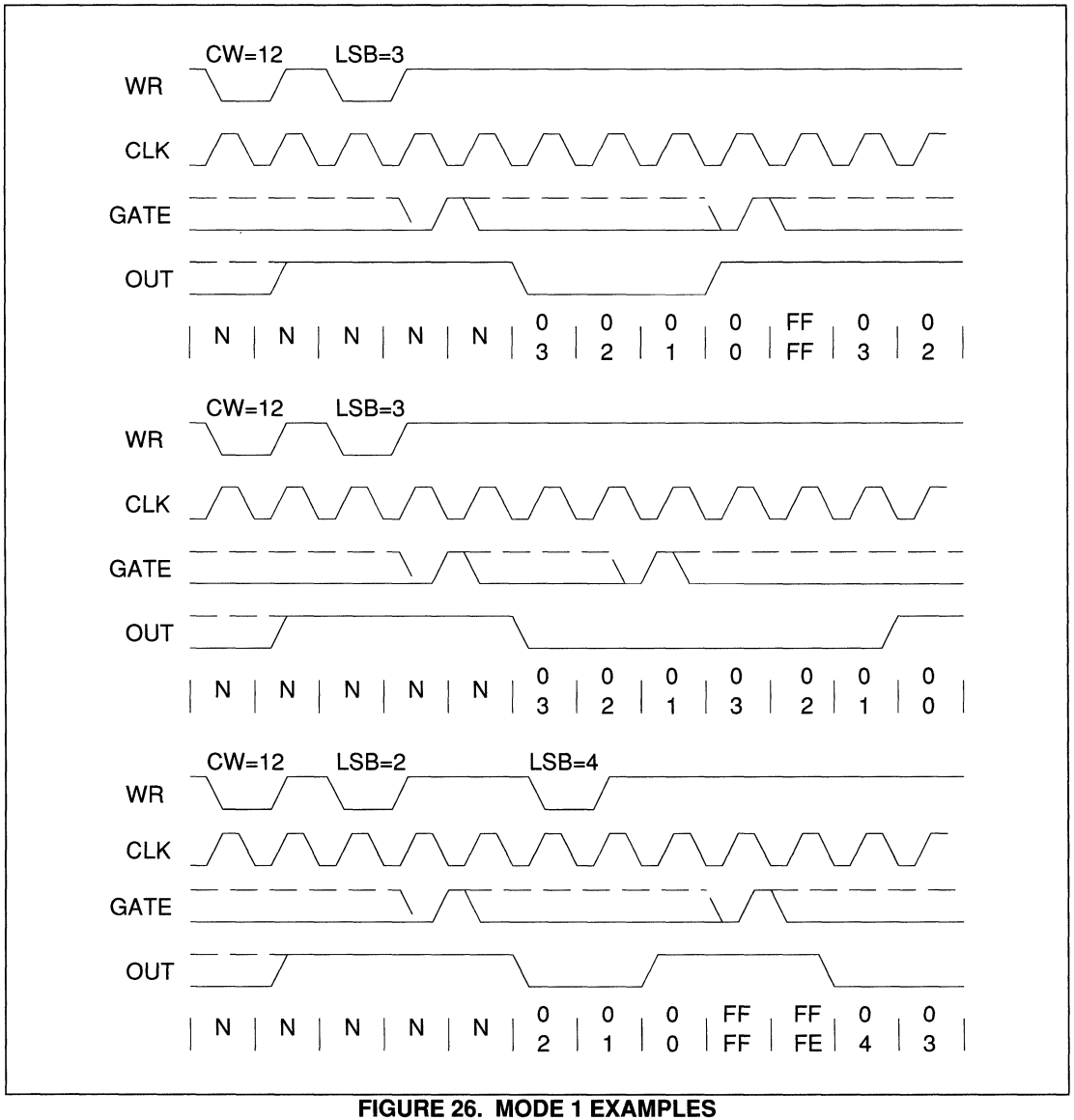


FIGURE 26. MODE 1 EXAMPLES

4.3.2 Mode 1—Hardware Retriggerable One-Shot

Writing the Control Word causes OUT to go high. A trigger (i.e., GATE = 1) causes OUT to go low on the next CLK pulse and remain low until the counter reaches 0; this creates a one-shot pulse. At this time, OUT goes high and remains high until the next trigger. An initial count of N results in a one-shot pulse N CLK cycles long.

Since the one-shot is retriggerable, if another trigger occurs during a one-shot pulse, OUT remains low to extend the pulse for N CLK cycles. Writing a new count during a one-shot pulse has no effect unless the counter is retriggered, in which case the pulse extends from the new count. GATE has no effect on OUT. Figure 26 shows examples of Mode 1 operation. Mode 1 is valid for Counter 2 only.

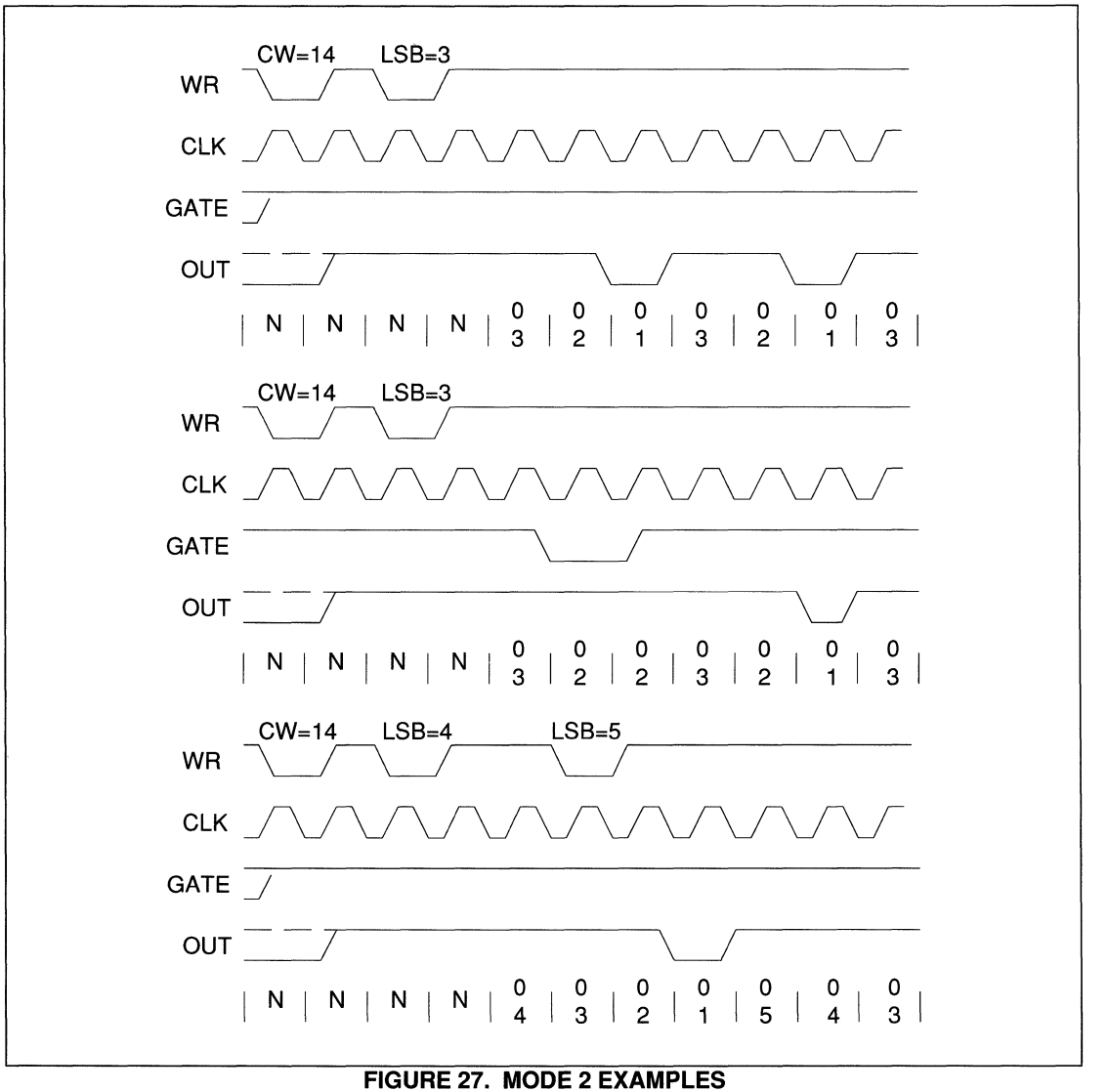


FIGURE 27. MODE 2 EXAMPLES

4.3.3 Mode 2—Rate Generator

Mode 2 functions as a divide-by-N counter. It is typically used to generate a real-time clock interrupt. Writing the Control Word causes OUT to go high. When the initial count reaches 1, OUT goes low for one CLK pulse. When OUT becomes high, the counter reloads the initial count and the process is repeated. For an initial count of N, the sequence repeats every N CLK cycles. Note that a count of one is illegal in Mode 2.

Counting is enabled when GATE = 1. GATE = 0 disables counting and forces OUT to high. A trigger reloads the counter with the initial count on the next CLK pulse. Using the GATE input allows counting to be synchronized with external events.

Writing a new count during a counting sequence has no effect unless the counter is triggered. If triggered, the count is extended by the new count on the next CLK pulse. If not, the new count is loaded at the end of the current counting cycle. Figure 27 shows examples of Mode 2 operation.

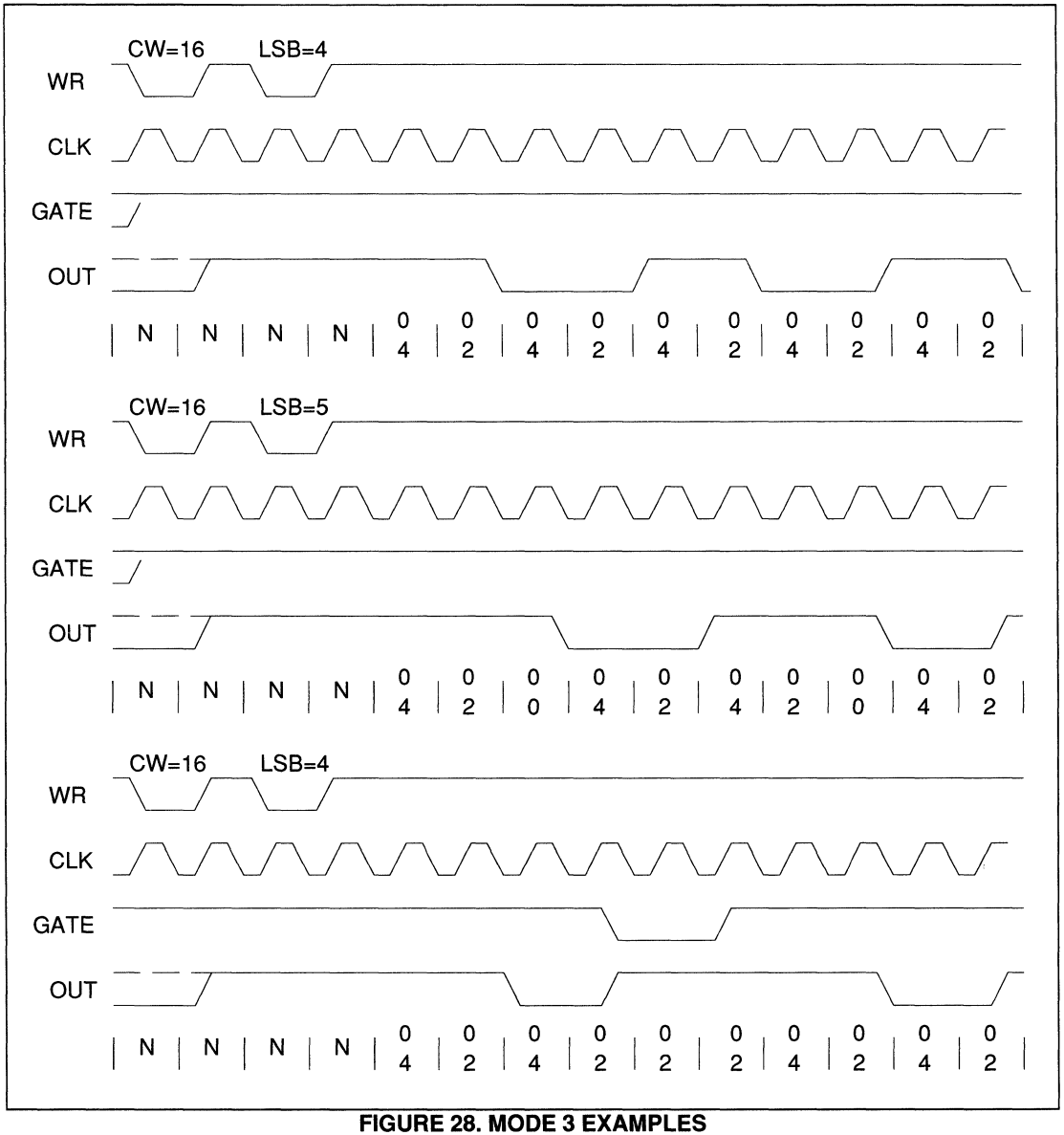


FIGURE 28. MODE 3 EXAMPLES

4.3.4 Mode 3—Square Wave Generator

Mode 3 is typically used for Baud rate generation. This mode is identical to Mode 2 except for the OUT duty cycle. Writing to the Control Word causes OUT to become high and remain high for the first half of the count. Then OUT becomes low and remains low for the remainder of the count. The cycle is repeated, creating a square wave with a period of N CLK cycles when the initial count is N.

If the counter is loaded with an even count, the OUT duty cycle is 50% (i.e., high = low = N2). For odd count values, OUT is high for one CLK cycle longer than it is low (i.e., high = (N+1)/2 and low = (N-1)/2). Figure 28 shows examples of Mode 3 operation.

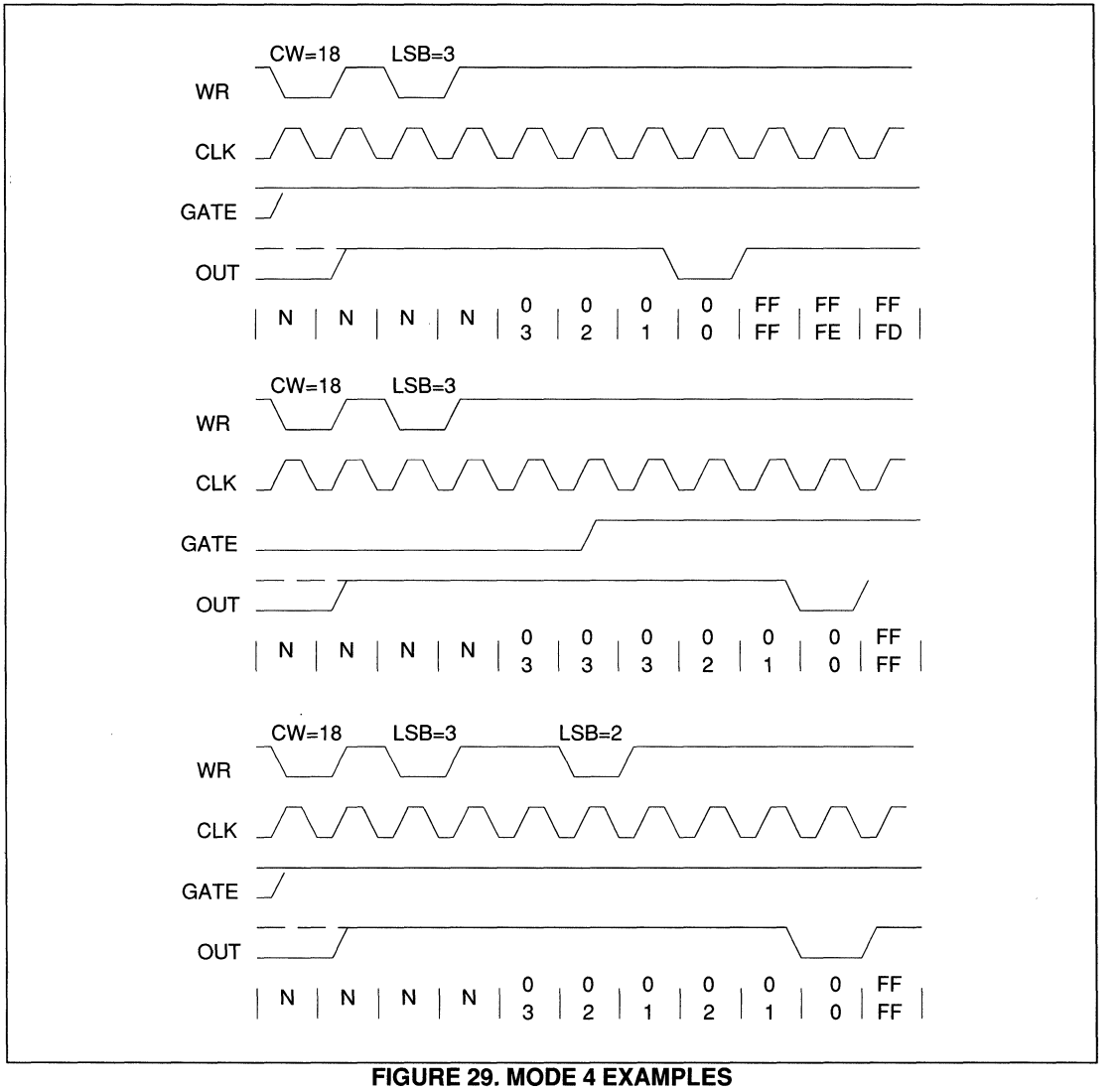


FIGURE 29. MODE 4 EXAMPLES

4.3.5 Mode 4—Software Triggered Strobe

Writing the Control Word causes OUT to go high. When the initial count expires, OUT goes low for one CLK cycle. The sequence is started by writing the initial count. Counting is enabled when GATE = 1. Disabling the count (GATE = 0) has no effect on OUT.

The initial count is loaded on the next CLK pulse after the Control Word and initial count are written. For an initial count of N, OUT goes low for one CLK cycle N+1 CLK cycles later.

If a new count is written during a counting sequence, it is loaded into the CE on the next CLK pulse and counting continues from the new count. When writing a two-byte count, the first byte has no effect on counting. After writing the second byte, the new count is loaded on the next CLK pulse. This allows the counting sequence to be retriggered by the software. Figure 29 shows examples of Mode 4 operation.

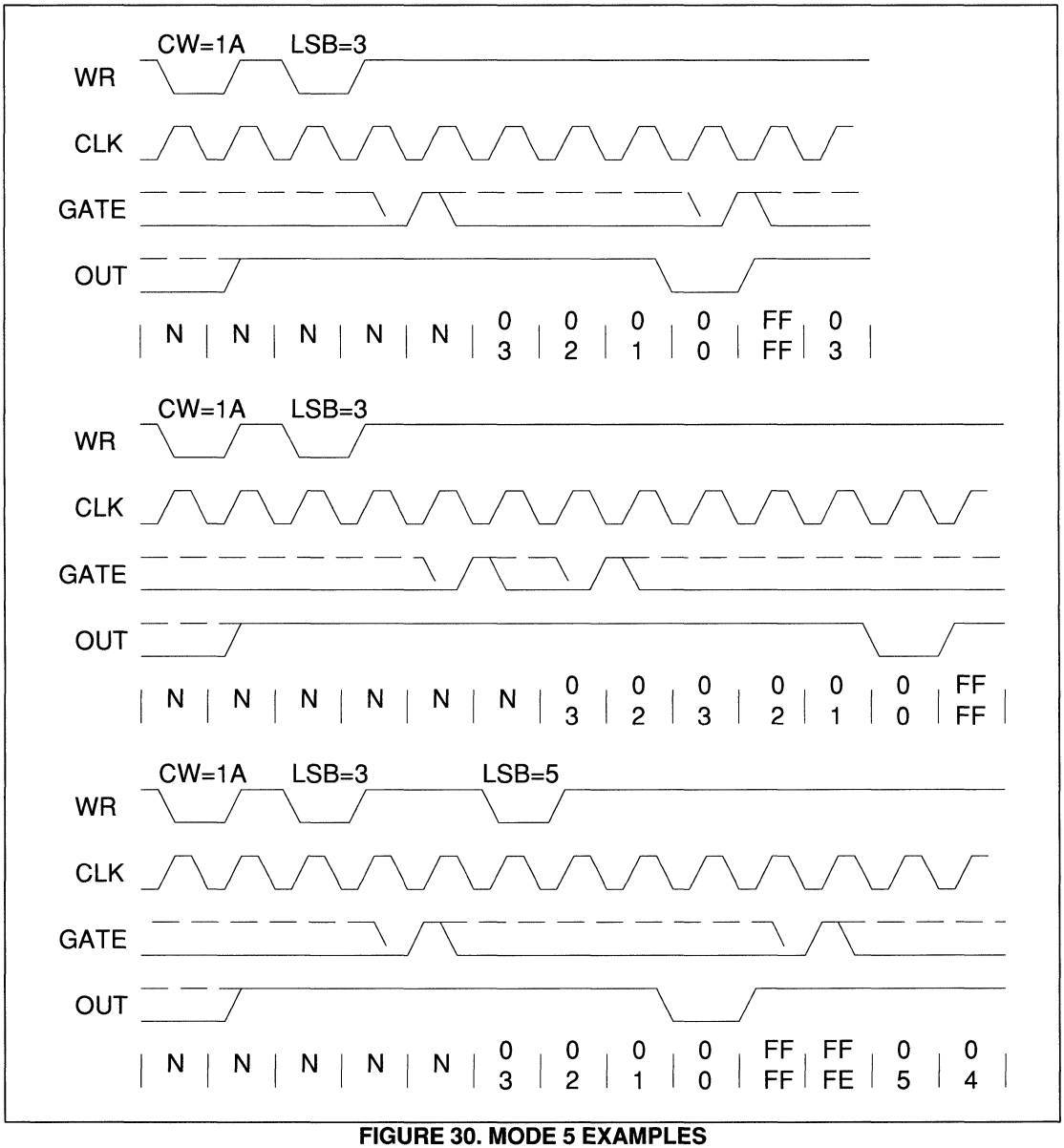


FIGURE 30. MODE 5 EXAMPLES

4.3.6 Mode 5—Hardware Triggered Strobe

Writing the Control Word causes OUT to go high. Count-ing is started by a trigger (i.e., rising edge of GATE) which loads the CE on the next CLK pulse. When the initial count N expires, N CLK cycles later, OUT goes low for one CLK cycle. GATE = 0 disables the counting.

Writing a new count during a counting sequence has no effect unless the counter is triggered. If triggered, the count is extended by the new count on the next CLK pulse. If not, the new count is loaded at the end of the current counting cycle. Figure 30 shows examples of Mode 5 operation. Mode 5 is valid only for Counter 2.

4.4 WATCHDOG TIMER OPERATION

The watchdog timer is set up by writing the control word for Timer 3 to Location 0047H and the count value to Location 0044H. Timer 3 is enabled to count on the first CLK pulse after the count is loaded to the CE. The CLK pulse for the watchdog timer is the output of Timer 0 and occurs every 55.05 ms.

The watchdog timer, Timer 3, can be enabled to monitor the IRQ0 service routine. When Timer 3 is loaded with a count of one and latched IRQ0 is pending for more than one CLK cycle, Timer 3 decrements to zero, generating a watchdog timeout and NMI. Write access to Timer 0 and 3 is not permitted when a watchdog time-out occurs.

The watchdog timer implementation assumes that the NMI vector in low memory has not been corrupted. System recovery may be invoked by the NMI service routine.

The IRQ0 Latch is reset by any of the following:

1. System Reset
2. IOW to 0061H D7 = 1
3. INTA (Interrupt Ack) with vector (D7:0)=8

Timer 3 is disabled by resetting the IRQ0 Latch and then performing the steps described for the watchdog set up.

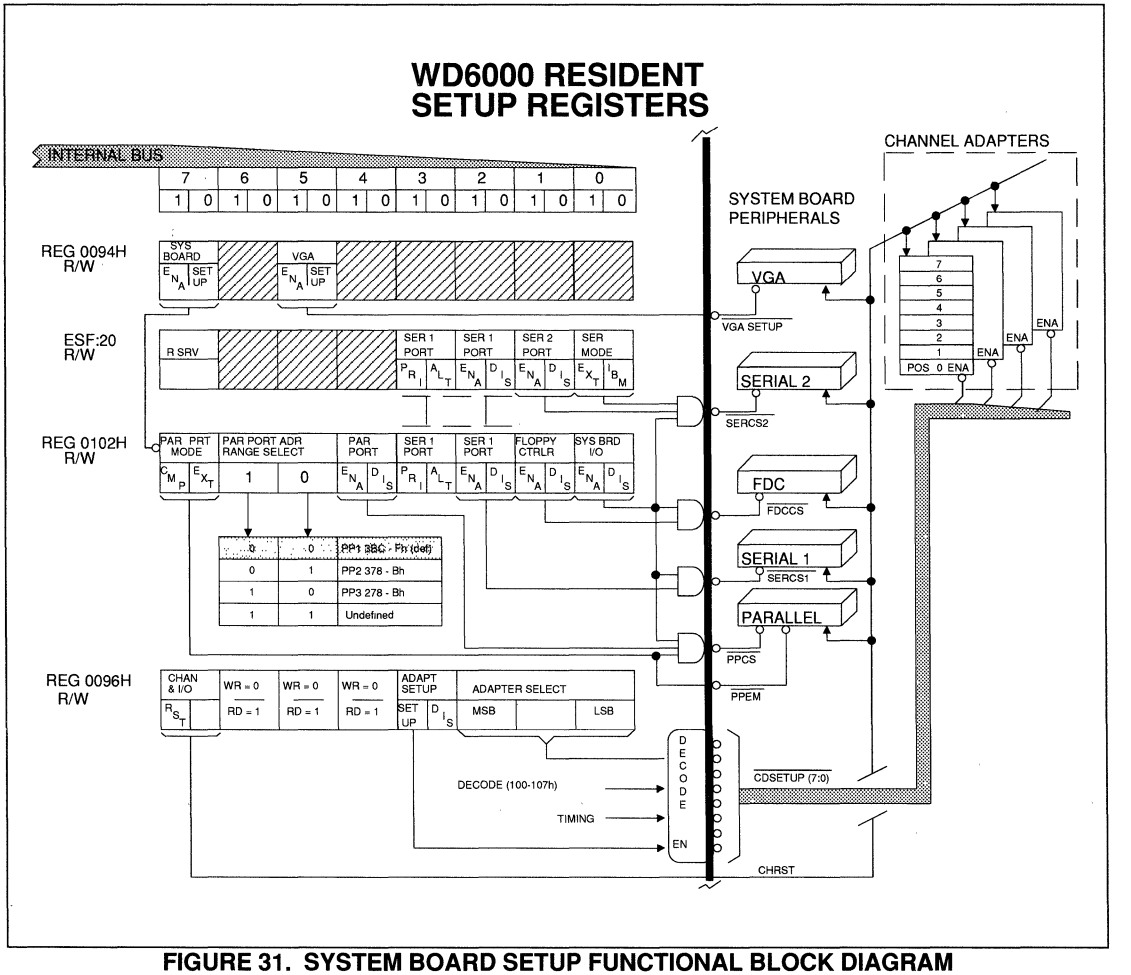


FIGURE 31. SYSTEM BOARD SETUP FUNCTIONAL BLOCK DIAGRAM

5.0 SYSTEM BOARD SETUP

The Programmable Option Select (POS) is implemented by I/O Registers 0091H, 0094H, 0096H, 0100H, 0101H, 0102H, and 0103H. For details, see Figure 31. POS eliminates switches from the system board and Channel adapters by incorporating programmable registers. The programmed configuration data and adapter ID numbers are then stored in battery-backed CMOS RAM. This permits the Power-On Self-Test (POST) to automatically reconfigure the system whenever the system is powered on.

- **System ID Setup**

POS Registers 0100H and 0101H contain the system ID code. These registers are read-only, but can be written once to store the appropriate ID.

- **Parallel Port Setup**

Figure 32 defines the bits in POS Registers 0102H and 0103H. Bit 0 of Register 0102H allows Bits 1, 2, and 4 to enable and disable their respective devices. In Compatible Mode (Bit 7 = 1), the parallel port is compatible with the PC/AT printer port. In Extended Mode, it operates in bi-directional mode, compatible with PS/2 MCA machines. This port is configured by POS Register 0102H, Bits 4–7.

- **Serial Ports Setup**

The configuration of on-board serial ports is controlled by either POS Register 0102H or the Peripheral Control Register (PCR). The PCR is part of the Extended Setup Facility (ESF). The physical ports are identified as SP1 and SP2. There are two logical ports identified as the primary serial port at Locations 03F8–03FFH (IRQ4) and the alternate serial port at Locations 02F8–02FFH (IRQ3). SP1 is configured by POS Register 0102H, Bits 2 and 3. Note that Bits 2 and 3 are overridden in Extended Mode. For more information, see Section 9.0, Extended Setup Facility.

- **Micro Channel Setup**

Figure 33 defines the bits for POS Registers 0091H, 0094H, and 0096H. POS Register 0091H, a read-only register, is used to determine if the PVGA, the system board, or a Channel adapter is present in the systems board peripherals. The Card Select Feedback $\overline{\text{CDSFDBK}}$ is set to zero when the address space of the adapter is accessed. Bit 0 of 0091H is set to one whenever $\overline{\text{CDSFDBK}}$ is asserted or when the system board I/O functions are accessed by an I/O cycle.

- **Video Setup**

The Video Graphics device, system board peripherals and Channel adapters are configured or enabled by specific bit settings in Registers 0094H and 0096H. Bits 5 and 7 of Register 0094H configures Setup Mode and System Board Setup Mode, respectively. Bit 3 of Register 0096H enables Adapter Setup Mode.

Important

Only one category of device can be in Setup Mode at a time. If more than one is in Setup Mode, bus conflicts occur.

11

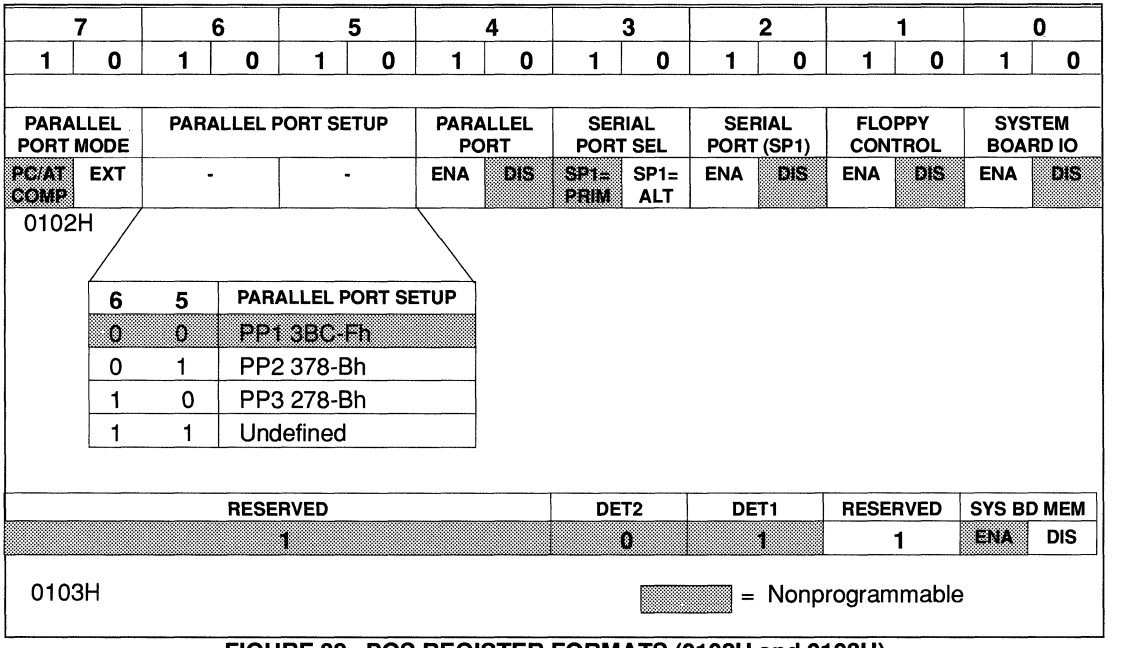


FIGURE 32. POS REGISTER FORMATS (0102H and 0103H)

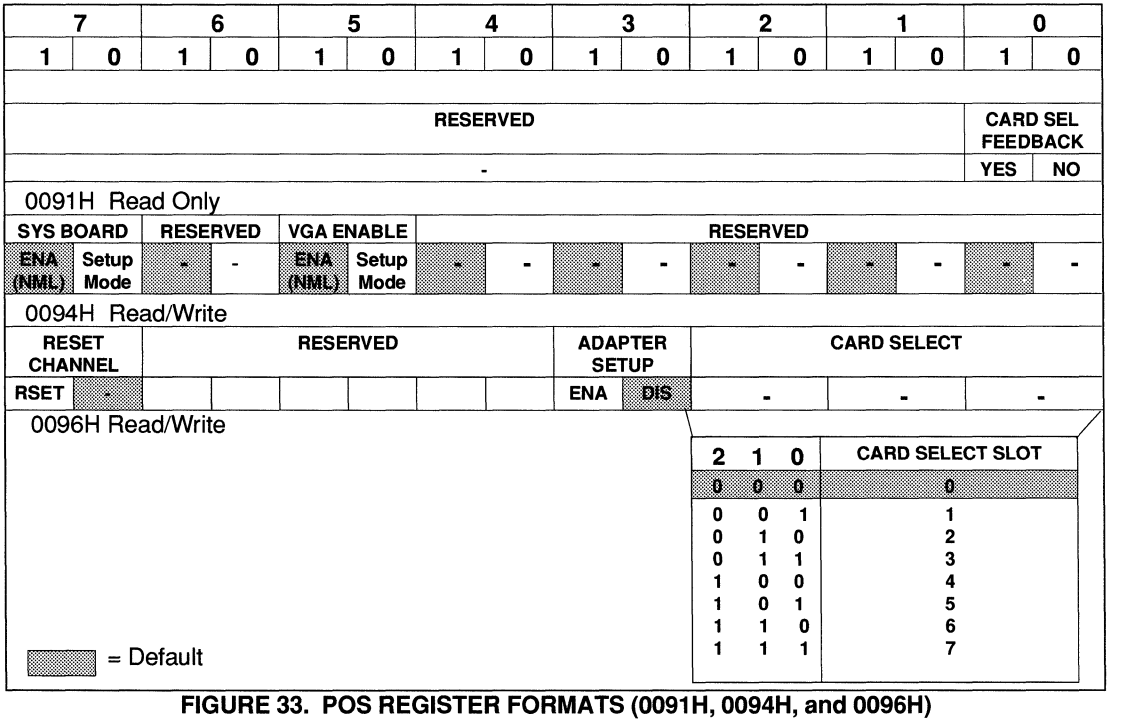


FIGURE 33. POS REGISTER FORMATS (0091H, 0094H, and 0096H)

6.0 SYSTEM CONTROL REGISTERS

The WD6000 has two IBM MC-conmpatible system control registers at 0061H (Control Port B) and 0092H (Control Port A). These ports are defined in Figures 34 and 35.

See Section 10.0 for details of other control registers.

7.0 COPROCESSOR INTERFACE

The coprocessor support function supplies error and control signals between the CPU and coprocessor, if any. An error signal from the coprocessor generates Interrupt IRQ13 in the WD6000. This causes the busy signal to the CPU to be held in the busy state. The interrupt and busy signals are cleared by writing 00H to the Coprocessor Clear Busy register, 00F0H. This interface also holds BUSY386 low during power on reset to initiate self test on the 80386 processor.

For further information, refer to the Pin Table. For an interface to the Weitek 3167 and competition, also refer to the Pin Table.

8.0 EXTERNAL DEVICE ENABLE

The WD6000 enables the following external devices:

Keyboard/Auxiliary Controller (8742)

- Floppy Disk Controller
- Parallel Port
- Serial Ports
- VGA Video
- Real-time Clock/CMOS RAM
- Coprocessor
- Port A/B decodes (programmable decodes)

In general, an IOR or IOW to the address ranges shown in the I/O map in Table 1 activates the various chip select lines. The WD6000 control interface is shared by the Channel. The System Board Setup Functional Block Diagram in Figure 32 indicates the selection of the floppy disk controller FDCCS, the parallel port controller PPCS, and Serial Ports 1 SERCS1 and 2 SERCS2, by enabling the appropriate POS registers.

The keyoard/auxiliary controller is selected through CS8742 when the keyboard data port is accessed at location 0060H, or when a read or write to the keyboard command/status port is executed at location 0064H. The coprocessor is selected through NPS1 when the coprocessor ports are addressed at Locations 00F8–00FFH. CSA and CSB are configurable select lines controlled by Ports A and B. See Section 9.0 for a description of the other control registers.

11

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
PARITY CHECK		CHAN CHECK		TIMER2 STATE		REFERSH TOGGLE		CHAN CHECK		PARITY CHECK		SPKR		TIMER2 GATE	
ERR	OK	ERR	OK	-		-		DIS	ENA	DIS	ENA	ENA	DIS	DIS	ENA
READ															
RESET IRQ0		RESERVED						CHAN CHECK		PARITY CHECK		SPKR		TIMER2 GATE	
RSET	ENA	-						DIS	ENA	DIS	ENA	ENA	DIS	ENA	DIS
WRITE															

FIGURE 34. SYSTEM CONTROL REGISTER FORMATS (0061H)

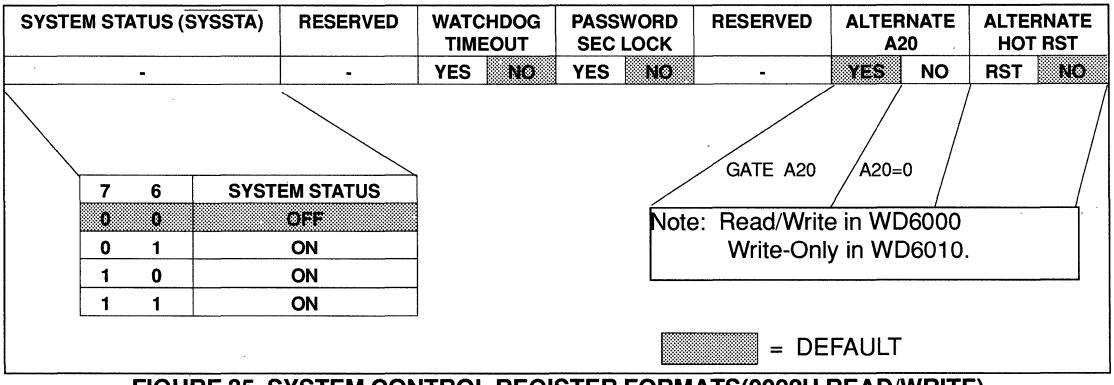


FIGURE 35. SYSTEM CONTROL REGISTER FORMATS(0092H READ/WRITE)

9.0 PERIPHERAL BUS CONTROL

The Peripheral Bus Control generates control signals that interface with the peripheral devices, and are enabled by the External Device Enable function to the CPU complex. $\overline{S0}$, $\overline{S1}$, and M/$\overline{IO}$ encode the information on the type of Channel bus cycle, as shown in Table 6.

$\overline{M/IO}$	$\overline{S1}$	$\overline{S0}$	BUS CYCLE TYPE
0	0	0	Interrupt Acknowledge
0	0	1	IO Read
0	1	0	IO Write
0	1	1	No Cycle
1	0	0	System CPU Halt or Shutdown
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	No Cycle

TABLE 6. CHANNEL COMMAND ENCODING

10.0 EXTENDED CMOS RAM INTERFACE AND EXTENDED SETUP FACILITY

The WD6000 provides external signals that are related to the Extended CMOS RAM (ECR) and the Extended Setup Facility (ESF). The WD6000 shares the implementation of the ECR and ESF with the WD6010. Figure 36 is a block diagram of the ECR and ESF, indicating how functions are divided between the WD6000 and the WD6010.

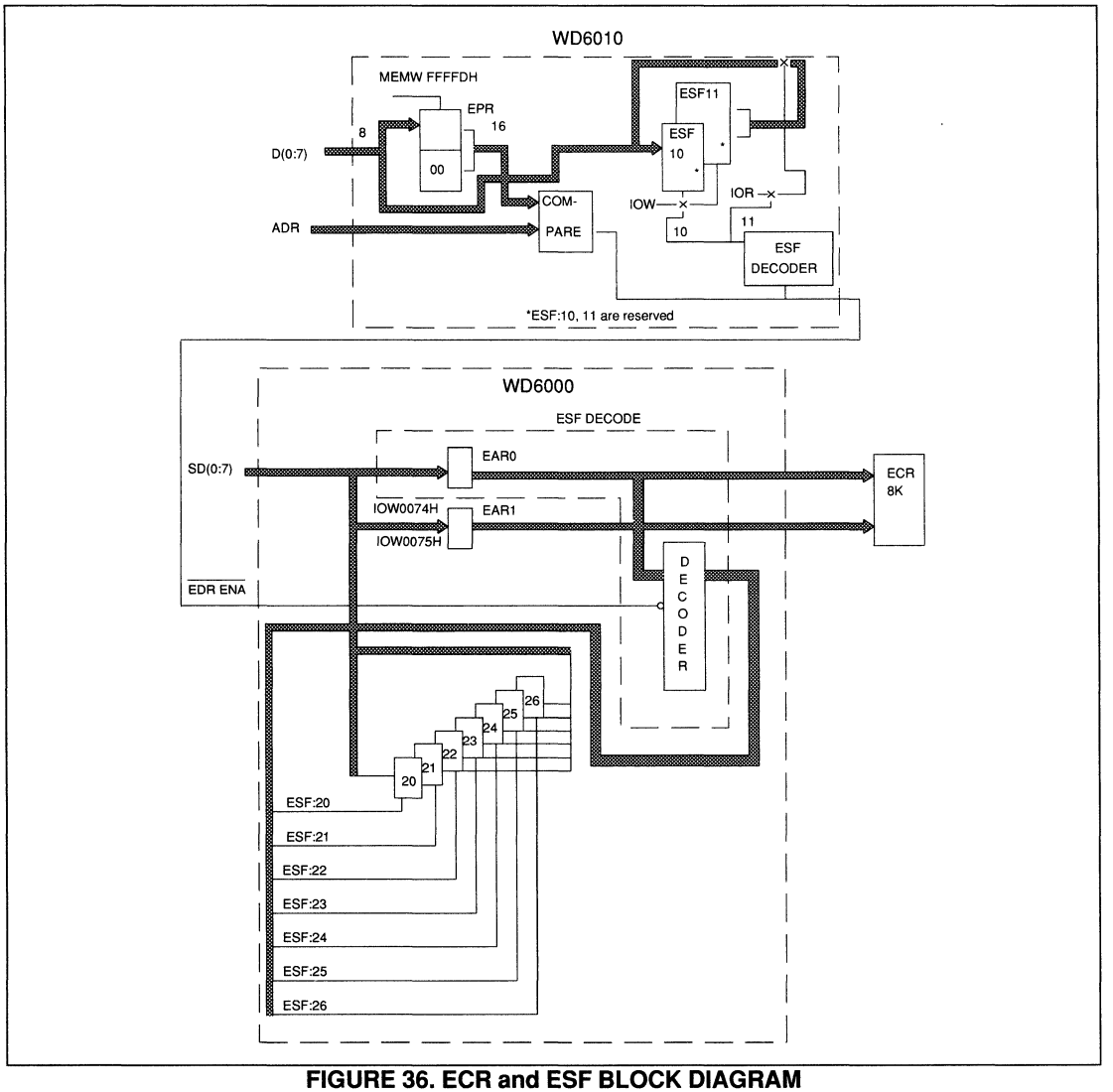


FIGURE 36. ECR and ESF BLOCK DIAGRAM

10.1 EXTENDED CMOS RAM (ECR) INTERFACE

The ECR supports Real-Time Clock (RTC) access and additional storage for POS and the ESF parameters needed for large systems. The RTC function is accessed through I/O Ports 0070H and 0071H. Port 0070H is used to point to the internal register or RAM location. Refer to Figure 37. Port 0071H is the read/write data port. Refer to the IBM Technical Reference for the byte definitions of the CMOS RAM.

The ECR interface allows an additional 8K bytes for storage of POS and/or additional system parameters. This function is accessed through Ports 0074H, 0075H, and 0076H when the RTC CMOS address port (0070H) is set to 8DH. Ports 0074H (EAR0) and 0075H (EAR1) are used to set the desired RAM address. The ECR address bus (CMOSA), consists of EAR0 (the LSB of the ECR address), and bits 0–4 of EAR1 (the MSB of the ECR address). Port 0076H is the data port.

10.2 EXTENDED SETUP FACILITY (ESF)

The ESF function consists of the ESF Pointer Register (EPR) and associated decode logic that generates the ESF Data Register Enable ($\overline{\text{EDRENA}}$) output from the WD6010 to the WD6000. It is designed to extend the configuration architecture established with the POS features. See Figure 38 for an ESF overview.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
NMI		RESERVED		RT/CMOS ADDRESS											
DIS	ENA	-		MSB		-		-		-		-		LSB	

= DEFAULT

FIGURE 37. RTC/CMOS ADDRESS PORT REGISTER (0070H)

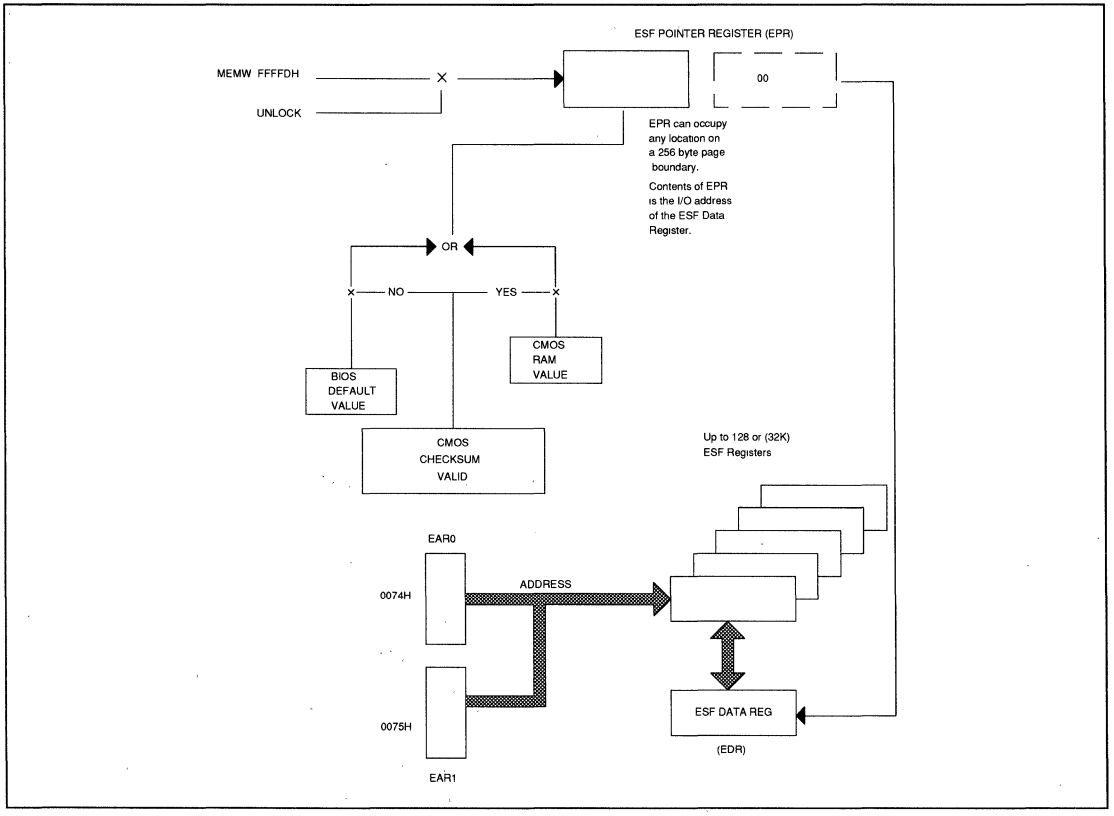


FIGURE 38. EXTENDED SETUP FACILITY OVERVIEW

ESF supports:

- Memory Map Control Registers
- Additional physical serial port
- Programmable Port Enables A and B
- External DRAM control configuration
- Customer specified enhancements that could include:
  System Identification
  System Version
  Miscellaneous system board features

10.2.1 ESF Access

ESF is based on an "alternate I/O space" concept similar to how IBM has implemented their Extended CMOS RAM feature. ESF space (128 locations expandable to 32K) is accessed through a single "real I/O space" window called the ESF Data Register (EDR). ESF space may be implemented as either word or byte-wide at the discretion of the designer.

The EDR is pointed to by the software configurable (write only) ESF Pointer Register (EPR) located in the WD6010. The EPR is loaded by writing to memory location FFFFDH or FFFFFDH (normally a PROM). The power-on default location for the EDR is located at IO address 0700H.

The following procedure is recommended for modifying the EPR:

1. Set the value 8DH in Port 0070H to disable $\overline{\text{NMI}}$.
2. Read the System Control Port B at 0061H and test for a change in the state of Bit 4 (Refresh Toggle) to synchronize with the refresh circuitry.
3. Read EAR0 at 0074H (normally write-only) to unlock the EPR.
4. Write the new value into the EPR (FFFFDH). This locks the EPR again.
5. Enable $\overline{\text{NMI}}$ if required.

Note that the EPR is locked when written or on the next refresh cycle, whichever occurs first.

The value in the EPR becomes the new 8-bit address of the EDR. The EDR can reside at any of 256 locations in the 64K IO space of the CPU from 0400H to FF00H.

To address the ESF I/O space:

1. Write the value 8DH to port 0070H to disable $\overline{\text{NMI}}$.
2. Write the address value to EAR0 at 0074H (and EAR1 if expanded ESF is being used).
3. Issue an I/O Read or Write command to EDR Address.

The selected ESF register is determined by decoding the EAR0 (and EAR1) address value.

10.2.2 ESF Address Maps

The lower 64 bytes (EAR0 = 00H–3FH) are reserved for Western Digital functions and features. The upper 64 bytes (EARO = 40H–7FH) are for customer use (see Table 7). All functions using ESF must include Bit 7 in the decode. Bit 7 of EAR0 must be 0 when addressing only 128 ESF registers. To expand the ESF to 32,768 locations, set EAR0 Bit 7 to 1 and write the second ESF address byte to EAR1.

ESF ADDRESS	FUNCTION
00H-0FH	System Reserved
10H-1FH	System board core functions
20H-3FH	System board peripheral functions

TABLE 7. ESF GENERAL USAGE MAP

The ESF address map in a WD6500 and WD6400SX(LP) system environment is shown in Table 8.

ESF ADDRESS	FUNCTION	R/W	WD6500 DEVICE	WD6400SX(/LP) DEVICE
0-001FH	Reserved	-	-	-
20H	Peripheral Configuration	R/W	WD6000	WD6000
21,24H	Port A, B Control	R/W	WD6000	WD6000
22,25H	Port A, B Address (LSB)	R/W	WD6000	WD6000
23,26H	Port A, B Address (MSB)	R/W	WD6000	WD6000
30-3FH	Reserved	-	-	-
40-7FH	Customer-specified	-	-	-
0180H	Memory Configuration	R/W	WD6030	WD6036SX (/LP)
0181H	Memory Size Register	R/W	WD6030	WD6036SX (/LP)
0182H	Bank Enable Register	R/W	WD6030	WD6036SX (/LP)
0183H	Split Address Extension	R/W	WD6030	N/A
0184H	Memory Window Bank 0	R/W	WD6030	WD6036SX (/LP)
0185H	Memory Window Bank 1	R/W	WD6030	WD6036SX (/LP)
0186H	Memory Window Bank 2	R/W	WD6030	WD6036SX (/LP)
0187H	Memory Window Bank 3	R/W	WD6030	WD6036SX (/LP)
0188H	CAS Pulse Width	R/W	WD6030	WD6036SX (/LP)
0189H	RAS Pre-Charge Delay	R/W	WD6030	WD6036SX (/LP)
018AH	RAS Pulse Width[1] - RAS to CAS Delay [2]	R/W	WD6030	WD6036SX (/LP)
018BH	RAS Access Time[1] -PSRAM Chip Select[2]	R/W	WD6030	WD6036SX (/LP)
018CH	Enhanced Addressing	R/W	WD6010	N/A
018DH	Reserved	-	-	-
018EH	Reserved	-	-	-
018FH	System Control Register[1] System Configuration[2]	R/W ***	WD6030	WD6036SX (LP)

Notes:
1. WD6500 implementation only.
2. WD6400SX(/LP) implementation only.

*** Dependent on the state of the UCHMSTER and A20GTX signals at reset.

TABLE 8. ESF ADDRESS MAP IN A WD6500 or WD6400SX (LP)

SYSTEM ENVIRONMENT

10.2.3 Peripheral Configuration Register (PCR)

The PCR is assigned to ESF location 20H. It allows the additional serial port, SP2, to be configured. When PCR Bit 0 = 1 (Extended Mode enabled), Bits 2 and 3 in the System Board Setup register (0102H) are overridden. Figure 39 shows the PCR format.

10.2.4 Port A/B Decodes

Ports A and B are identical device-enable ports that are configurable by software. The 16-bit starting I/O address, port depth (up to 128 bytes), programmable wait state logic, and enable/disable control are provided by Ports A and B. The starting address must be on an even binary multiple of the port depth. Figure 40 shows the ESF format for Port A and B Control Registers.

11.0 NMI CONTROL

The NMI Control logic generates an $\overline{NMI}$ signal when any of the following events occur:

1. Channel $\overline{CHCK}$ line asserted (Bit 3 = 0 of Control Port B at 0061H).
2. DRAM parity error (Bit 2 = 0 of Control Port B).
3. Watchdog Timer time-out (Enabled by programming the Timer).
4. System channel time-out.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
TIMER		RESERVED					SP1		SP1		SP2		MODE		
TEST	NORM	-		-		-	PRI	ALT	ENA	DIS	ENA	DIS	EXTD	IBM	

= DEFAULT

FIGURE 39. PERIPHERAL CONFIGURATION REGISTER FORMAT (ESF:20 READ/WRITE)

PORT		COMMAND WIDTH SELECT			RESERVED	I/O SPACE DEPTH		
ENA	DIS	2	1	0	-	2	1	0

6	5	4	WIDTH (NS) [1]
0	0	0	70
0	0	1	140
0	1	0	280
0	1	1	420
1	0	0	560
1	0	1	700
1	1	0	840
1	1	1	980

[1] Any I/O device may extend the cycle beyond these times given by driving CDCHRDY inactive.

2	1	0	BYTES
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	Reserved

FIGURE 40. PORT A OR B CONTROL REGISTER (ESF:21, ESF:24 READ/WRITE - TYPICAL)

12.0 TECHNICAL SPECIFICATIONS

12.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum stress ratings for the device are listed below. Permanent device damage can result from exposing the device to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	(V_{DD}-V_{SS})	0	7	V
Input Voltage	V_{IABS}	V_{SS}-0.3	V_{DD}+0.3	V
Bias on output pin	V_{OABS}	V_{SS}-0.3	V_{DD}+0.3	V
Storage Temperature	T_S	-40	125	°C

12.2 NORMAL OPERATING CONDITIONS

Exposure of the device to conditions exceeding the normal operating conditions for extended periods of time can affect the long term reliability of the device.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.75	5.5	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V
Power Dissipation	P_W	-	TBD	mW
Supply Current	I_{DD}	-	TBD	mA

12.3 DC CHARACTERISTICS (UNDER NORMAL OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	MAX	UNITS
*Input capacitance @ f_c=1 MHz	C_I	-	5	pF
*I/O capacitance	C_{IO}	-	10	pF
Logic high input voltage	V_{IH}	2.0	-	V
Logic low input voltage	V_{IL}	-	0.8	V
*Input leakage	I_{IL}	-	±10	µA
*Tri-state output leakage	I_{LO}	-	±30	µA
*I/O pin leakage	I_{IOL}	-	±40	µA
OUTPUTS MHZ14 AND $\overline{\text{CHCK}}$				
*Source current @ V_{OH}=2.4 V	I_{OH}	4	-	mA
*Sink current @ V_{OL}=0.4 V	I_{OL}	24	-	mA
OUTPUTS $\overline{\text{CDSETUP}}$ [0:07]				
Source current @ V_{OH}=2.4 V	I_{OH}	1	-	mA
Sink current @ V_{OL}=0.4 V	I_{OL}	6	-	mA
ALL OTHER OUTPUTS				
*Source current @ V_{OH}=2.4 V	I_{OH}	1	-	mA
*Sink current @ V_{OL}=0.4 V	I_{OL}	4	-	mA

***Notes:**

Pins $\overline{\text{INT1EN}}$ and $\overline{\text{INT2EN}}$ have internal pulldowns of 10 K ohms nominal value. Measurement of input capacitance and input leakage values on these pins will be affected by these resistances.

11

$\overline{\text{CHCK}}$ is an open drain output. An external pullup is required. Only the sink current value applies.

$\overline{\text{NMI}}$ is an open drain output. An external pullup is required. Only the sink current value applies.

13.0 TIMING

See following tables.

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	$\overline{S0}$, $\overline{S1}$(0:1) hold from $\overline{CMD}$ on	30	-	-
T2	SA(0:15) setup to $\overline{CMD}$ on	60	-	-
T3	SD(0:7) setup to $\overline{CMD}$ on	-	25	1
T4	SA(0:15) hold from $\overline{CMD}$ off	0	-	-
T5	SD(0:7) hold from $\overline{CMD}$ off	0	-	-
T6	$\overline{CDSETEN}$ hold from $\overline{CMD}$ on	30	-	-
T7	$\overline{PROMCSL/H}$ setup to $\overline{CMD}$ on	25	-	-
T8	$\overline{PROMCSL/H}$ hold from $\overline{CMD}$ off	0	-	-
T9	M/$\overline{IO}$ hold from $\overline{CMD}$ on	30	-	-
T10	$\overline{CDSFDBK}$ setup to $\overline{CMD}$ on	10	-	-
T11	$\overline{EDRENA}$ setup to $\overline{CMD}$ on	25	-	-
T12	$\overline{EDRENA}$ hold from $\overline{CMD}$ on	0	-	-
T13	$\overline{IOR/W}$, $\overline{MEMRD/WR}$ delay from $\overline{CMD}$ on	40	-	-
T14	$\overline{MEMRD/WR}$ pulse width	-	-	2
T14	$\overline{IOR/W}$, $\overline{CS8742}$	160	-	-
T14	$\overline{IOR/W}$, $\overline{FDCCS}$	90	-	-
T14	$\overline{IOR/W}$, $\overline{SERCS1}$, $\overline{SERCS2}$	125	-	-
T14	$\overline{IOR/W}$, $\overline{PPCS}$	125	-	-
T14	$\overline{IOR/W}$, $\overline{NPS1}$	90	-	-
T14	$\overline{IOR/W}$, $\overline{CSA}$, $\overline{CSB}$	70	980	-
T15	$\overline{IOR/W}$, $\overline{MEMRD/WR}$ off to $\overline{CMD}$ off	60	-	-
T16	$\overline{IODTR}$ setup to $\overline{IODEN}$ on	5	-	-
T17	$\overline{IODTR}$ hold from $\overline{IODEN}$ off	5	-	-
T18	$\overline{IODEN}$ on from $\overline{CMD}$ on	5	-	-
T19	$\overline{IODEN}$ hold from $\overline{CMD}$ off	5	-	-
T20	IODCBA on from $\overline{CMD}$ on	40	-	-
T21	IODCBA off to $\overline{IOW/R}$, $\overline{MEMRD/WR}$ off	5	-	-
T22	$\overline{S0}$(1:0) on to IORDY off	-	20	-
T23	IORDY on to $\overline{CMD}$ off	60	-	-
T24	SD(0:7) read access from $\overline{IOR}$ on	25	-	-
T25	SD(0:7) read hold from $\overline{IOR}$ off	5	-	-
T26	CS (ext.dev) setup to $\overline{IOR/R}$, $\overline{MEMRD/WR}$ on	70	-	-
T27	CS (ext.dev) hold from $\overline{IOR/W}$, $\overline{MEMRD/WR}$ on	25	-	-
T28	$\overline{RTCRD}$, $\overline{RTCWR}$, $\overline{RTCAS}$ delay from $\overline{CMD}$ on	40	-	-
T29	$\overline{RTCRD}$, $\overline{RTCWR}$, $\overline{RTCAS}$ off to $\overline{CMD}$ off	60	-	-
T30	$\overline{RTCRD}$, $\overline{RTCWR}$, $\overline{RTCAS}$ pulse width	325	-	-
T30A	CMOSA(0:12) on from $\overline{CMD}$ on	40	-	-
T31	CDSETUP(0:7) hold from $\overline{CMD}$ on	30	-	-

NOTES: 1. THE WD6000 allows SD bus valid to be later than CMD active.
2. T21 for $\overline{MEMRD/WR}$ follows $\overline{CMD}$ input.

TABLE 9. PERIPHERAL BUS CYCLE (IN NSEC)

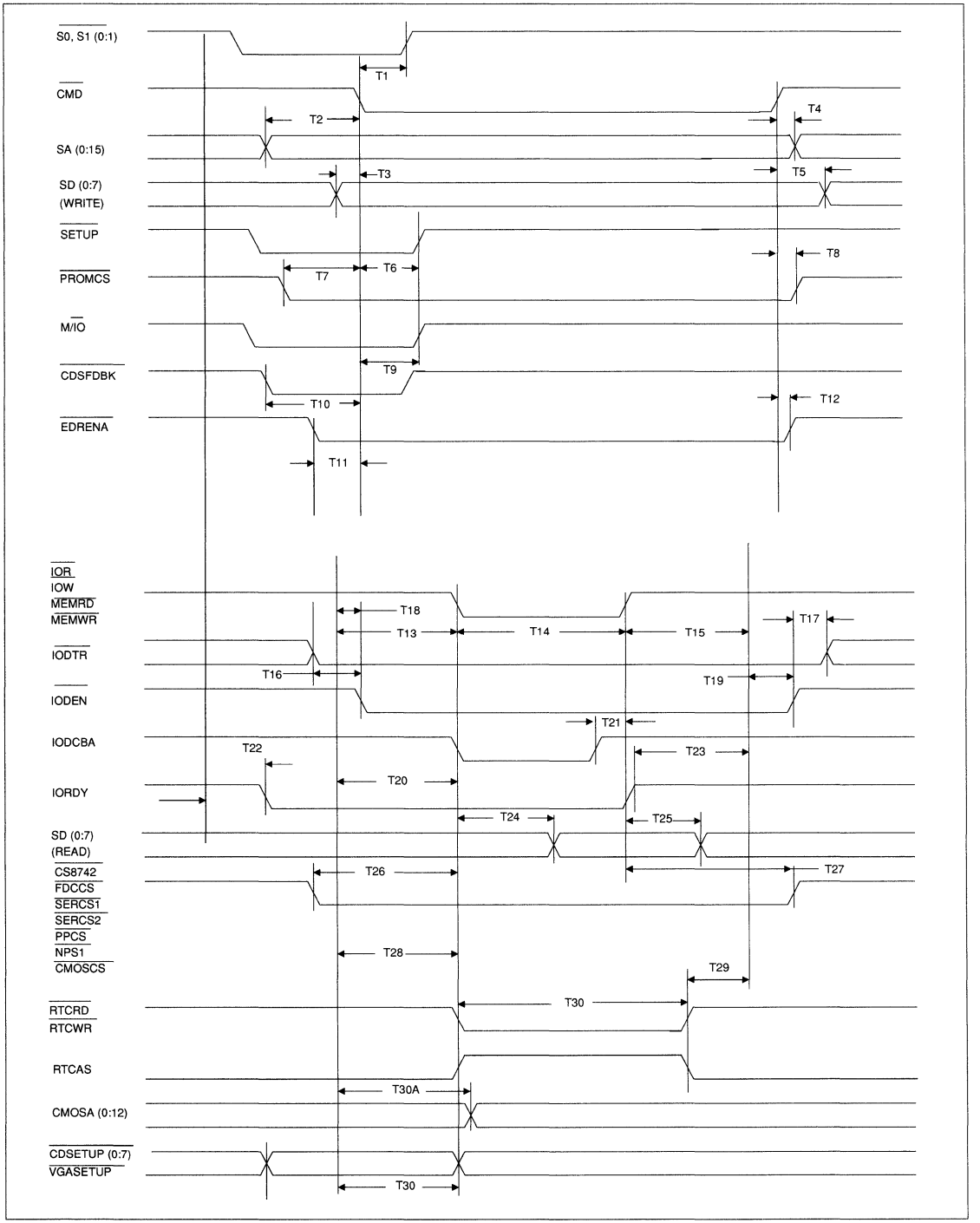


FIGURE 41. PERIPHERAL BUS CYCLE

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	MHZ28 period	35	-	-
T2	MHZ28 low time	17	-	-
T3	MHZ28 high time	16	-	-
T4	MHZ30 period	33	-	-
T5	MHZ30	18	-	-
T6	MHZ30 high time	15	-	-
T7	MHZ14 period	70	-	-
T8	MHZ14 high time	20	-	-
T9	MHZ14 low time	20	-	-
T10	CLK387 period	105/100	-	1
T10F	CLK387 rise time	-	10	3
T10R	CLK387 fall time	-	10	3
T11	CLK387 high time	28	-	4
T12	CLK387 low time	62	-	4
T13	CLK8742 period	105/100	-	1
T14	CLK8742 low time	33	-	-
T15	CLK8742 high time	33	-	-
T16	$\overline{\text{REFREQ}}$ period	15 µs	-	2

NOTES: 1. Clock derived from 28.636 MHz, unless optional 30 MHz is used.
2. 50% duty cycle .
3. Rise and fall times are measured between 0.8 V and 2.0 V.
4. Clock low time measured at 1.0 V, clock high time measured at 3.6 V.

TABLE 10. CLOCK CYCLE TIMES (IN NSEC EXCEPT WHERE NOTED)

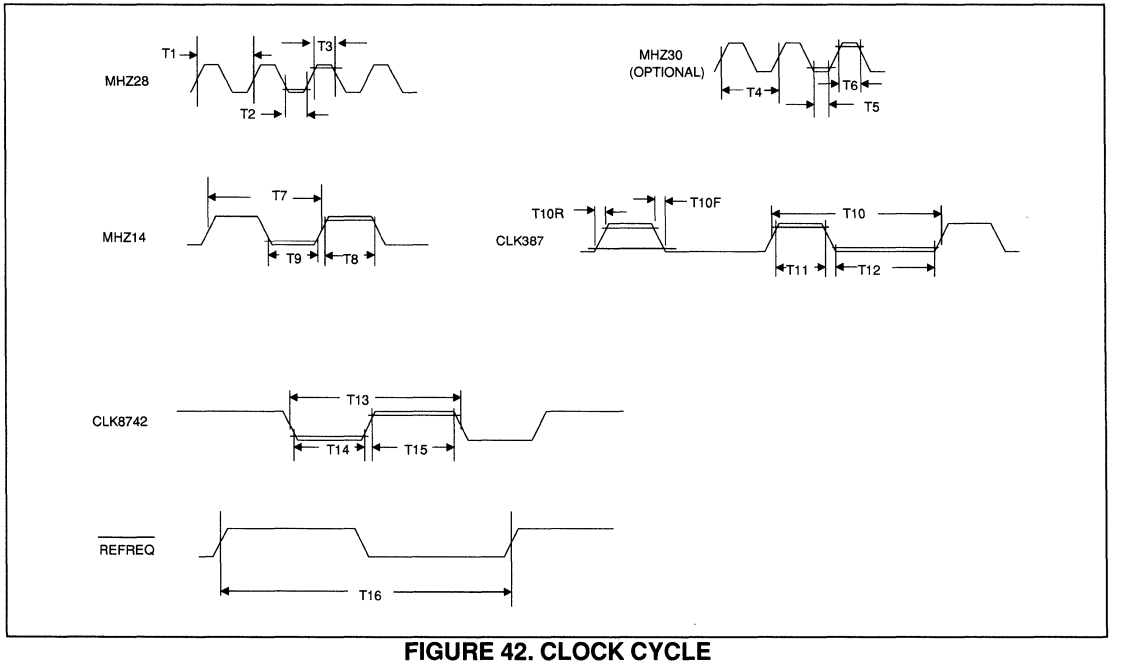


FIGURE 42. CLOCK CYCLE

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	INTR output delay	-	100	-
T2	INTR hold from INTACK on	10	32	1

NOTES: 1. Interrupt inputs must be held until the first Interrupt Acknowledge cycle begins.

TABLE 11. INTERRUPT CYCLE (IN NSEC)

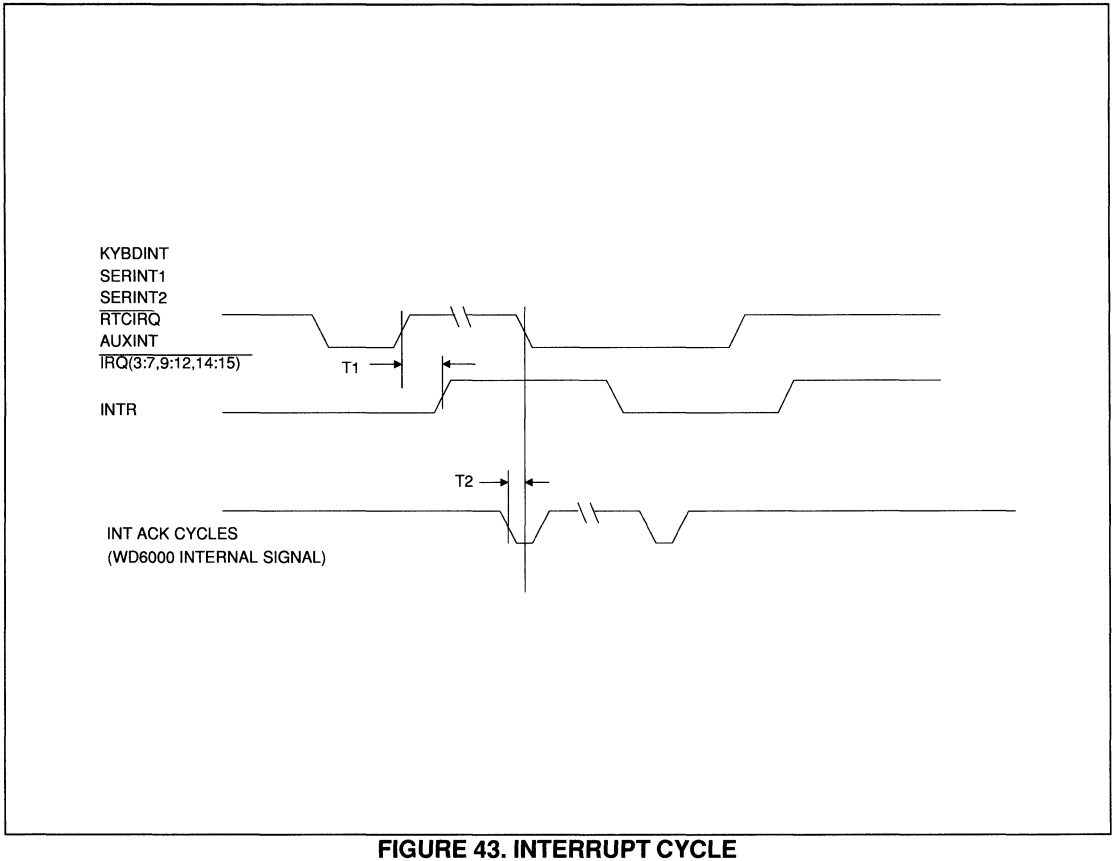


FIGURE 43. INTERRUPT CYCLE

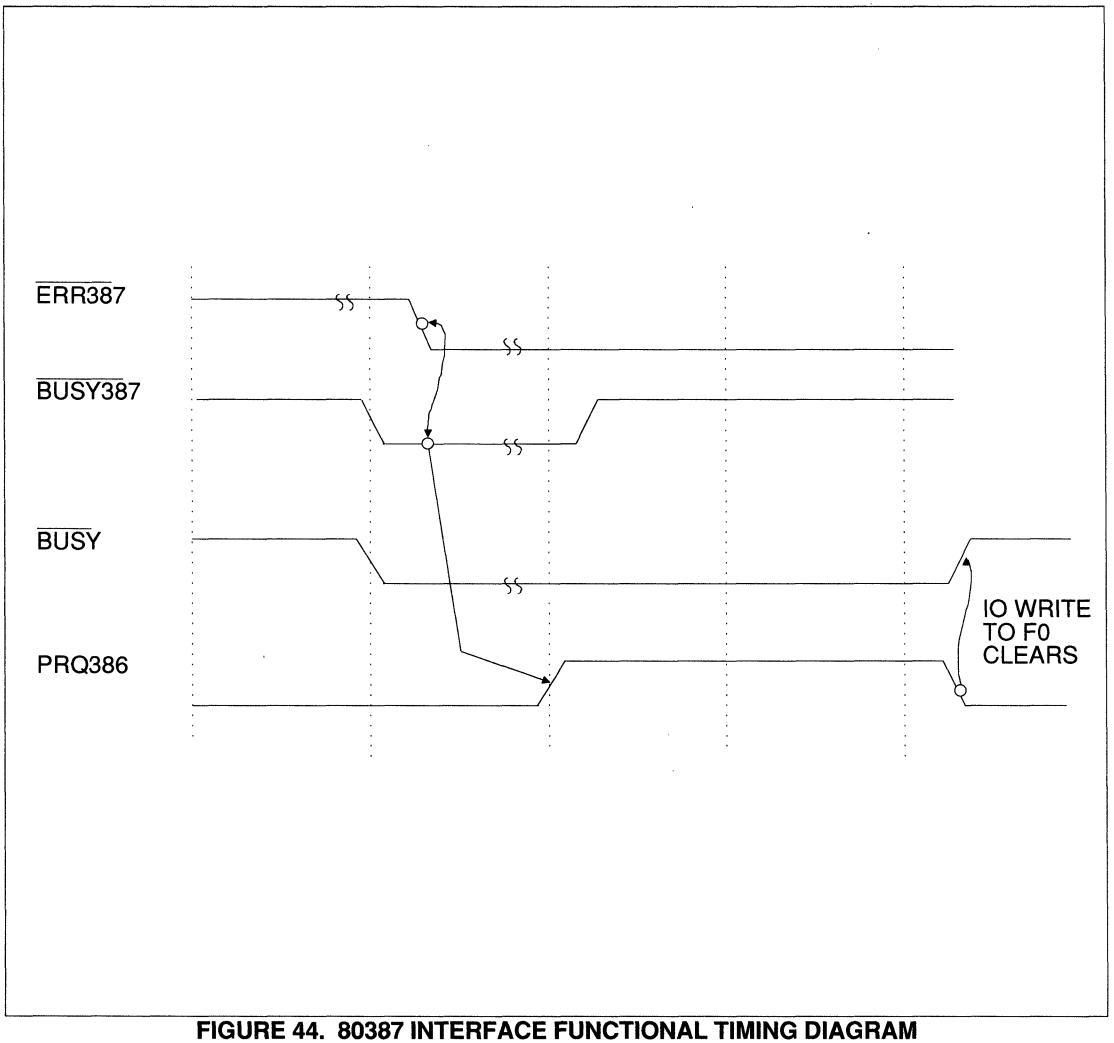
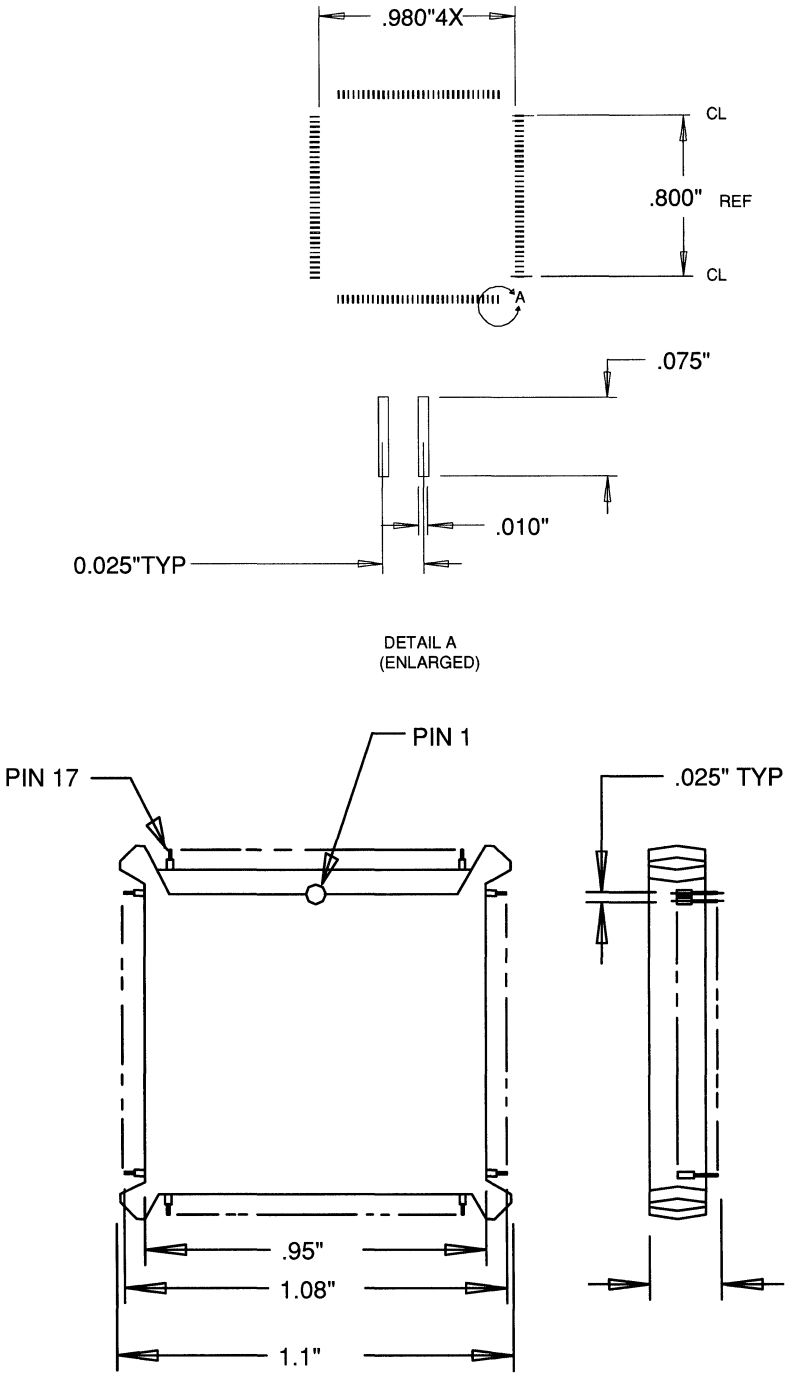
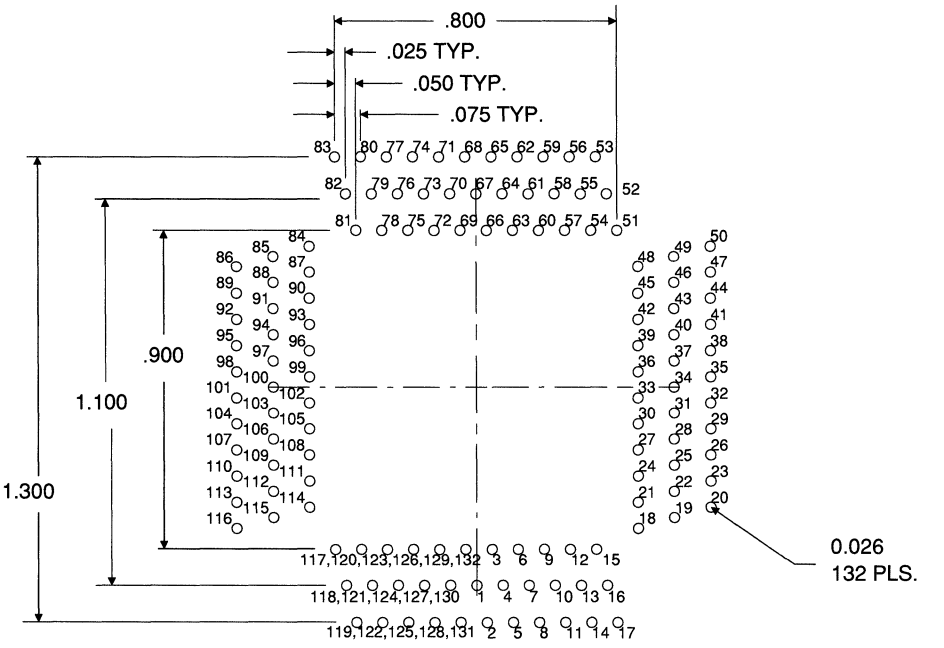


FIGURE 44. 80387 INTERFACE FUNCTIONAL TIMING DIAGRAM



FIFUEW 45. 132-PIN JEDEC FLAT PACK PACKAGING DIAGRAM



RECOMMENDED P.C. BOARD HOLE PATTERN
SOCKET SIDE
132 POSN

Amp Incorporated
Harrisburg PA
Part No. 821932-5

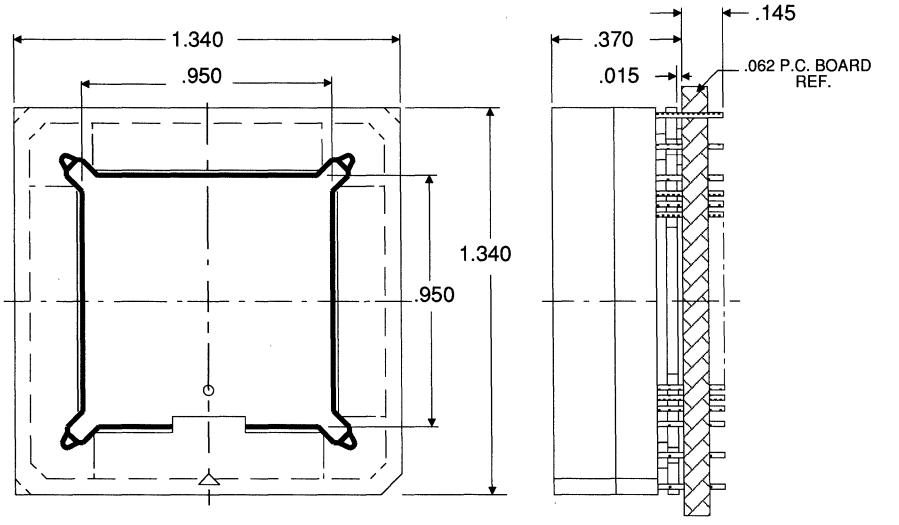


FIGURE 46. SOCKET DIAGRAM

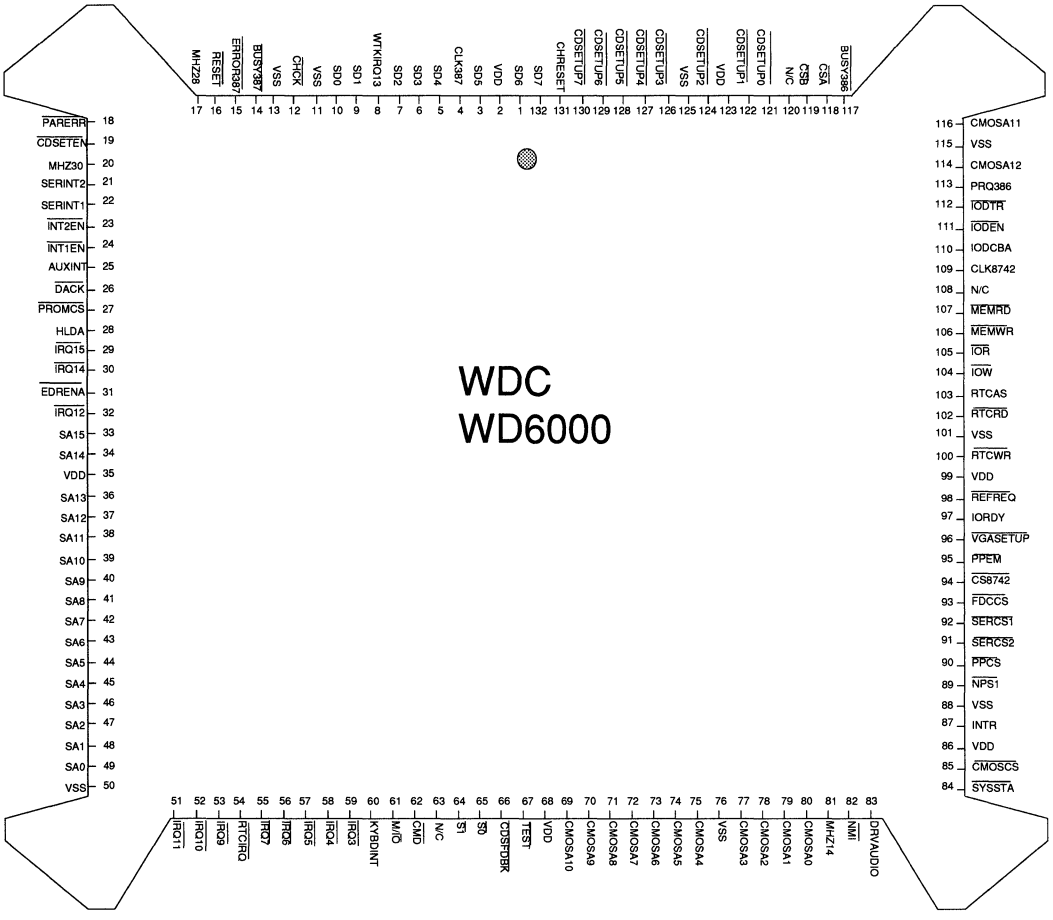


FIGURE 47. PIN LAYOUT DIAGRAM - TOP VIEW

SYSTEMS LOGIC/PERIPHERAL

WD6010

DMA and Arbitration Control Device

12

WESTERN DIGITAL

TABLE OF CONTENTS

12

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

As part of the Western Digital® Micro Channel compatible chip sets (WD6500, WD6400SX, WD6400SX/LP), the WD6010 DMA and Arbitration Control Device significantly facilitates the design and implementation of system boards compatible with IBM's Micro Channel architecture. It decreases design complexity and saves space by combining the functions of many discrete arrays and components, while reducing system cost and increasing system reliability.

The Extended Setup Facility is a Western Digital enhancement, designed to allow more functionality such as a Winchester Controller, LAN Adapter or additional serial port to be added onto the system board. It provides product differentiation at the system level and helps hold down costs. Figure 1 illustrates a typical system using Western Digital's Micro Channel compatible chip sets. Devices with bold outlines are available from Western Digital.

1.1 Features

- Completely compatible with the IBM Personal System/2 Models 70 and 80
- Configurable for systems based on the 80386SX, 80386DX, or 80486
- 16, 20, 25, and 33 MHz Clock Speeds to Maximize Flexibility and Performance
- Half-speed 80387/80387SX Operation
- 4-Gigabyte Enhanced Addressing
- Micro Channel Arbitration Control Logic
- Functionality equivalent to two 8237 DMA controllers with Extended Mode Support
- Clock, Resets, and Parity Latch Control
- Extended Setup Facility™ (ESF)™
- Low Power 0.9 Micron CMOS Technology

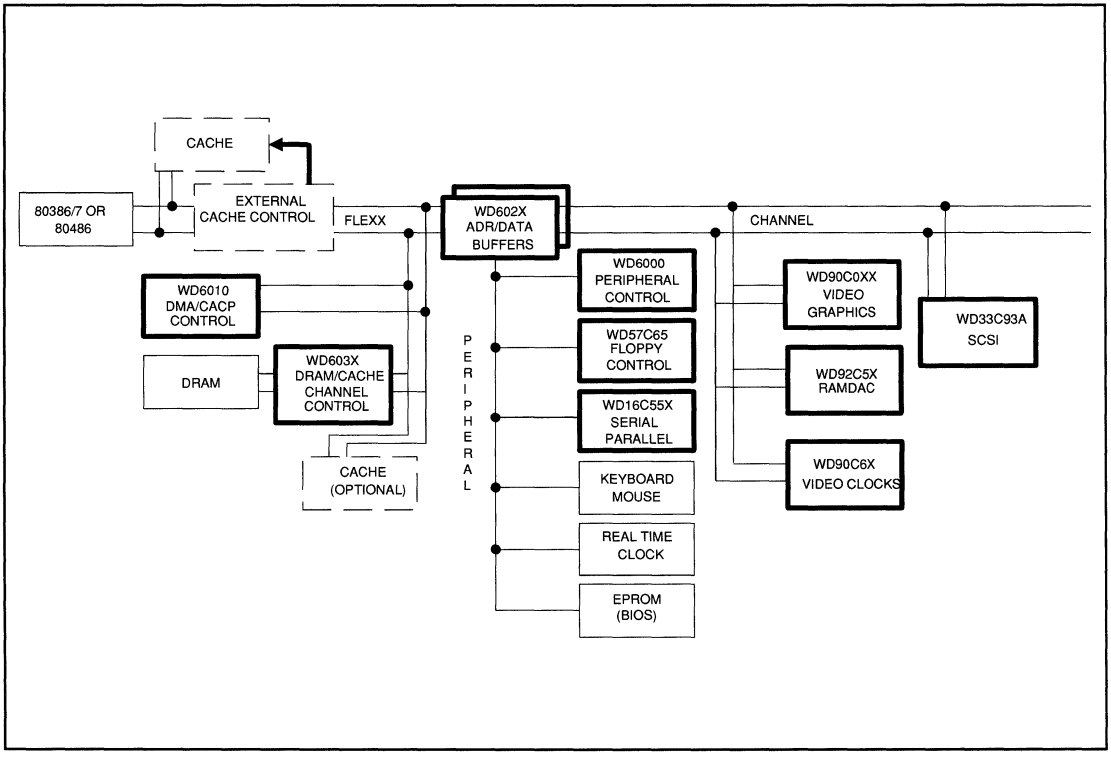


FIGURE 1. SYSTEM DIAGRAM

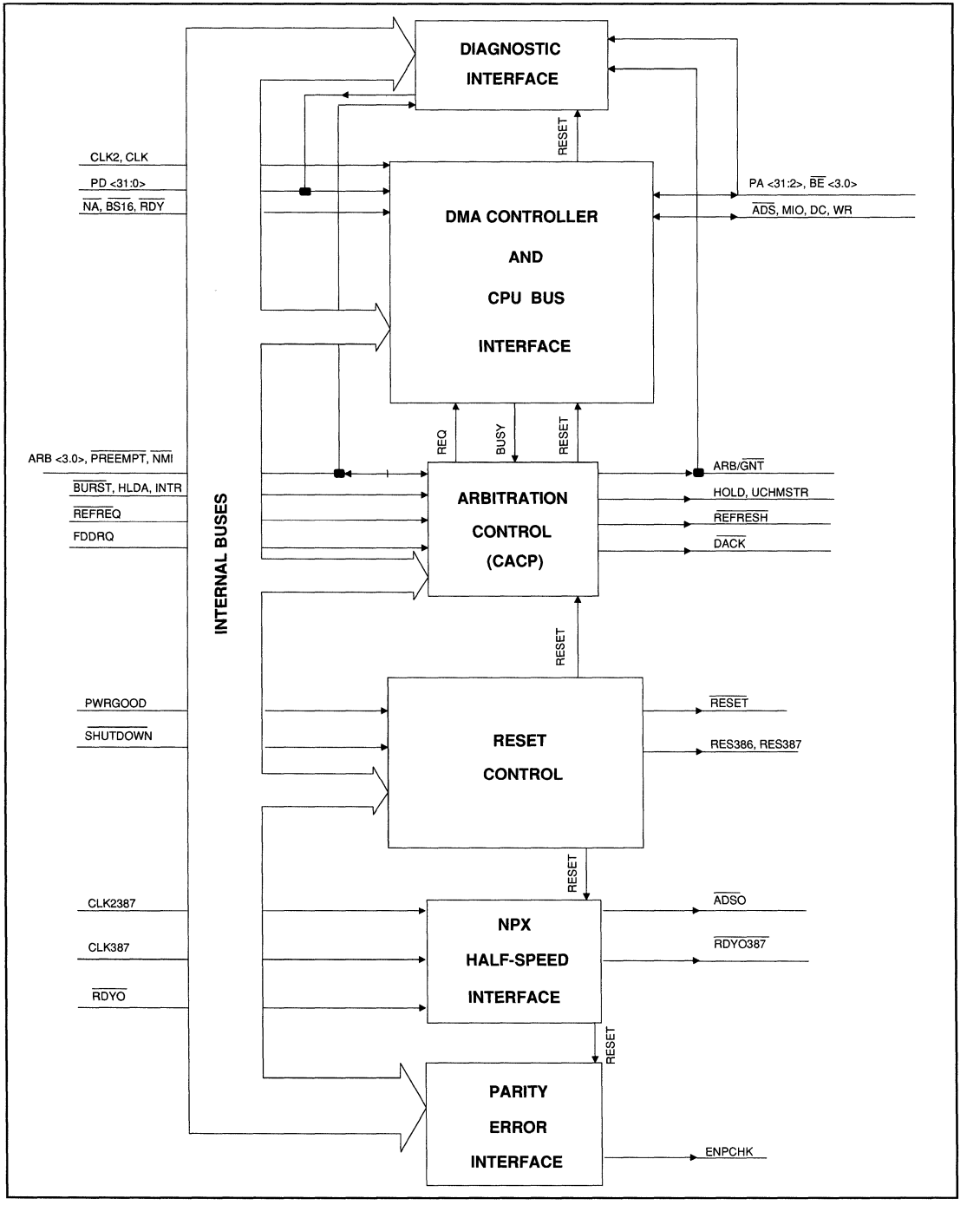


FIGURE 2. WD6010 BLOCK DIAGRAM

2.0 PIN DESCRIPTION

The signals assigned to the different pins are grouped according to their function, and discussed individually in the table on the following pages.

2.1 Diagnostic Interface

This interface is used to diagnose errors in the system. The diagnostic signals recover the state of the bus after an error condition. For more details, see Section 8.6.

2.2 DMA Controller and CPU Bus Interface

The DMA Controller in the WD6010 is fully compatible with the Micro Channel architecture in the basic mode. In addition, the WD6010 provides an enhanced addressing mode, the 4Gig Mode, to enhance the DMA addressing capability.

NOTE: The registers implemented on the WD6010 can only be accessed by the system microprocessor.

2.3 Arbitration Control

The Arbitration Control block in the WD6010 arbitrates between different masters requesting use of the bus at the same time. The Central Arbitration Control Point (CACP) controls the arbitration timing in accordance with Micro Channel specifications.

2.4 Reset Control

The Reset Control block in the WD6010 generates three levels of resets, compatible with the Micro Channel architecture.

A system reset ($\overline{\text{RESET}}$), which resets all the devices in the system.

A CPU reset (RES386), which only resets the microprocessor. The synchronization of this signal to the CPU clock, CLK2, must be done externally.

A numeric coprocessor reset (RES387), which only resets the 80387/80387SX numeric coprocessor. Synchronizing this signal to the numeric coprocessor clock, CLK2387, must be executed externally.

NOTE: The WD6010 is compatible with the 80386SX, 80386DX, and 80486 microprocessors. In the following description, any references to the system microprocessor refer to the 80386SX, 80386DX and 80486, unless specifically stated otherwise. Similarly, any references to the NPX (Numeric coprocessor extension) refer to the 80387SX, and the 80387DX, unless explicitly stated otherwise. Section 10.0 describes the differences in implementation on an 80386SX system versus an 80386DX system.

2.5 Numeric Coprocessor Extension (NPX) Half-speed Interface

The NPX half-speed interface allows the NPX to be operated at half the speed of the CPU. A half-speed NPX interface is useful in systems where the cost-performance requirements dictate an inexpensive coprocessor. In an 80386SX system, the coprocessor used is an 80387SX; on an 80386DX system it is an 80387DX; on an 80486 system, the coprocesser is not required.

2.6 Parity Error Interface

This signal interfaces with external parity latches and provides the capability to latch parity errors.

2.7 Decodes

This block implements the decodes for system-wide functions.

2.8 Miscellaneous

This set of signals include the V_{SS} and V_{DD} signal pins as well as the reserved pins, which should not be connected, but left open in the system.

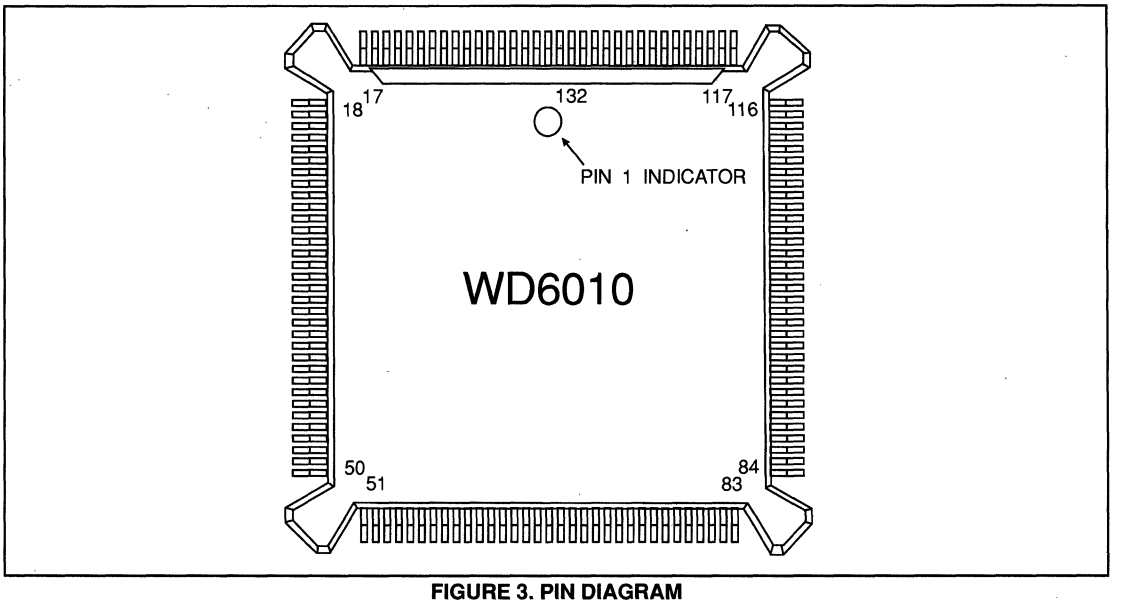


FIGURE 3. PIN DIAGRAM

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	CLK2	34	PD7	67	$\overline{\text{REFRESH}}$	100	V_{DD}
2	V_{SS}	35	V_{SS}	68	$\overline{\text{BE0}}$	101	PA17
3	CLK	36	PD8	69	$\overline{\text{BE1}}$	102	PA16
4	CLK2387	37	PD9	70	$\overline{\text{BE2}}$	103	PA15
5	V_{DD}	38	PD10	71	$\overline{\text{BE3}}$	104	PA14
6	CLK387	39	PD11	71	V_{SS}	105	PA13
7	$\overline{\text{EOT}}$	40	PD12	73	$\overline{\text{ADS}}$	106	PA12
8	$\overline{\text{REFREQ}}$	41	PD13	74	M/$\overline{\text{IO}}$	107	PA11
9	UCHCMD	42	PD14	75	DC	108	V_{SS}
10	A20GATE	43	V_{SS}	76	$\overline{\text{WR}}$	109	PA10
11	N/C	44	PD15	77	$\overline{\text{RESET}}$	110	PA9
12	INTR	45	PD16	78	RES386	111	PA8
13	$\overline{\text{PWRGOOD}}$	46	PD17	79	$\overline{\text{RES387}}$	112	PA7
14	$\overline{\text{SHUTDOWN}}$	47	PD18	80	$\overline{\text{CDSETEN}}$	113	PA6
15	$\overline{\text{BURST}}$	48	PD19	81	$\overline{\text{VGAEN}}$	114	PA5
16	$\overline{\text{TEST}}$	49	PD20	82	$\overline{\text{EDRENA}}$	115	PA4
17	V_{SS}	50	V_{SS}	83	V_{DD}	116	V_{DD}
18	$\overline{\text{PREEMPT}}$	51	PD21	84	PA31	117	PA3
19	ARB0	52	PD22	85	PA30	118	$\overline{\text{PA2}}$
20	ARB1	53	PD23	86	PA29	119	$\overline{\text{NMI}}$
21	ARB2	54	PD24	87	V_{SS}	120	$\overline{\text{ENPCHK}}$
22	ARB3	55	V_{DD}	88	PA28	121	$\overline{\text{DACK}}$
23	V_{SS}	56	PD25	89	PA27	122	$\overline{\text{ADSO}}$
24	$\overline{\text{CHRESET}}$	57	PD26	90	PA26	123	$\overline{\text{RDYO387}}$
24	$\overline{\text{CHCK}}$	58	PD27	91	PA25	124	$\overline{\text{RDYO}}$
26	PD0	59	PD28	92	PA24	125	FDDRQ
27	PD1	60	PD29	93	PA23	126	UCHMSTR
28	PD2	61	PD30	94	PA22	127	A20GTX
29	PD3	62	PD31	95	V_{SS}	128	V_{SS}
30	V_{DD}	63	HOLD	96	PA21	129	$\overline{\text{HLDA}}$
31	PD4	64	V_{SS}	97	PA20	130	$\overline{\text{BS16}}$
32	PD5	65	$\overline{\text{ARB/GNT}}$	98	PA19	131	$\overline{\text{NA}}$
33	PD6	66	$\overline{\text{TC}}$	99	PA18	132	$\overline{\text{RDY}}$

PIN NO.	NAME	TYPE	FUNCTION
			DIAGNOSTIC INTERFACE
127	A20GTX	I/O	ADDRESS BIT 20 GATE – This pin has dual functions. At power-up (trailing edge of RESET), the state of this pin is latched and in conjunction with UCHMSTR, determines the speed at which the system will operate. At all other times, A20GTX, is an output signal acting as a gating signal for address bit 20. This signal is active whenever A20GATE is active or whenever Alternate Gate A20 (port 92H, bit 1) is asserted and the CPU has the bus. **FREQUENCY / UCHMASTER / A20GTX** 16 MHz 0 0 20 MHz 0 1 25 MHz 1 1 33 MHz 1 0
25	CHCK	I	CHANNEL CHECK - This signal which is driven by a master or slave device, indicates that a serious system error has occurred.
24	CHRSET	I	CHANNEL RESET – This signal is generated by the WD6000 to initialize or reset all adapters or on-board peripheral controllers at power-on. The system can also generate this signal through software control (port 96H, bit 7).
10	A20GATE	I	ADDRESS 20 GATE – This signal which is generated by the 8x42 micro-controller activates the A20GTX signal whenever it is active when the CPU generates an address.
9	UCHCMD	I	CHANNEL COMMAND – This signal is the logical OR of the CMD and MMCMD signals, and indicates that a command is present on the Channel.
			DMA CONTROLLER AND CPU BUS INTERFACE
121	DACK	I/O	DMA REQUEST ACKNOWLEDGE – This pin has dual functions. At power-up (trailing edge of RESET), the state of this pin is sampled to determine whether the WD6010 will operate in an 80386SX-compatible or 80386/80486-compatible mode. At all other times, DACK is an output signal to the WD6000 and floppy disk controller. When it is active, it initiates a single I/O read or write transfer. Multiple transfers are initiated only if BURST is also active.

12

PIN NO.	NAME	TYPE	FUNCTION
118 117 115 114 113 112 111 110 109 107 106 105 104 103 102	PA2 PA3 PA4 PA5 PA6 PA7 PA8 PA9 PA10 PA11 PA12 PA13 PA14 PA15 PA16	I/O	CPU ADDRESS BUS – This bi-directional address bus between the CPU and DMA controller. During CPU accesses to the WD6010 registers, these are input signals, and during DMA transfers, these are output signals. During DMA transfers in the IBM compatibility mode, which is the power-on default, the WD6010 drives PA (2:31) according to the programmed address. Bits (24:31) are driven to zero. In Enhanced Addressing Mode bits (24:31) are driven according to the programmed address. When the WD6010 is used in an 80386SX system, CPU Address Bus signals (24:31) should be left unconnected.
101 99 98 97 96 94 93 92 91 90 89 88 86 85 84	PA17 PA18 PA19 PA20 PA21 PA22 PA23 PA24 PA25 PA26 PA27 PA28 PA29 PA30 PA31	I/O	CPU ADDRESS BUS – (Cont'd)

PIN NO.	NAME	TYPE	FUNCTION
62	PD31	I/O	CPU DATA BUS – This bi-directional data bus between the CPU and WD6010 is used to transfer data during DMA transfers and CPU accesses to the WD6010 registers.
61	PD30		
60	PD29		
59	PD28		
58	PD27		
57	PD26		The WD6010 has a 32-bit data bus interface compatible with the 80368/80486. However, DMA Transfers are in 8-bit or 16-bit blocks. The WD6010 performs internal swaps and asserts the correct byte enables to put the data in the right location. It handles misaligned transfers by generating the multiple cycles needed to complete the transfer.
56	PD25		
54	PD24		
53	PD23		
52	PD22		
51	PD21		
49	PD20		
48	PD19		
47	PD18		The WD6010 performs dynamic bus sizing to accommodate 16-bit and 32-bit devices on a cycle-by-cycle basis, accomplishing this by sampling the $\overline{BS16}$ input. The combinations of byte enables asserted for different transfers are tabulated below.
46	PD17		
45	PD16		
44	PD15		
42	PD14		
41	PD13		
40	PD12		
39	PD11		
38	PD10		
37	PD9		
36	PD8		
34	PD7		
33	PD6		
32	PD5		
31	PD4		
29	PD3		
28	PD2		
27	PD1		
26	PD0		

	VALID DATA 80386/80486				
Bus Signals	$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$	Byte/Word
PD(0:7)	1	1	1	0	Byte 0
PD(8:15)	1	1	0	1	Byte 1
PD(16:23)	1	0	1	1	Byte 2
PD(24:31)	0	1	1	1	Byte 3
PD(0:15)	1	1	0	0	Word 0
PD(8:23)	1	0	0	1	Word 1
PD(16:31)	0	0	1	1	Word 2

The next table illustrates the way in which the WD6010 splits misaligned transfers into multiple bus cycles. $\overline{BS16}$ is sampled during each cycle to adjust the transfer accordingly.

DATA TRANSFER SIZE (Bytes)					
	1	2			
CPU Address PA (0:1)	xx	00	01	10	11
Transfer Cycles over PD Bus	B	W	LB HB	W	LB H

Legend:
Transfers in **bold** letters indicate that $\overline{BS16}$ was active when sampled.
B – Byte
W – Word
HB –High Order Byes
LB–Low Order Byte
*–The 80386/80486 will first transfer the HB, and then the LB.

12

<table>
<tr><th>PIN NO.</th><th>NAME</th><th>TYPE</th><th>FUNCTION</th></tr>
<tr><td colspan="3">CPU DATA BUS (con't)</td><td>If the $\overline{BS16}$ input is permanently tied low, the WD6010 data bus interface generates a 16-bit interface compatible with the 80386SX. In this mode, the CPU data bus (16:31) should be left unconnected as they each have a weak internal pull-up. The combinations of byte enables asserted for different transfers in an 80386SX system are tabulated below.

<table>
<tr><th colspan="5">VALID DATA 80386SX</th></tr>
<tr><th>Signal</th><th>$\overline{BE3}$</th><th>$\overline{BE2}$
(PA1)</th><th>$\overline{BE1}$
($\overline{BEH}$)</th><th>$\overline{BE0}$
($\overline{BEL}$)</th><th>Byte/Word</th></tr>
<tr><td>PD(0:7)</td><td>x</td><td>0</td><td>1</td><td>0</td><td>Byte 0</td></tr>
<tr><td>PD(8:15)</td><td>x</td><td>0</td><td>0</td><td>1</td><td>Byte 1</td></tr>
<tr><td>PD(0:7)</td><td>x</td><td>1</td><td>1</td><td>0</td><td>Byte 2</td></tr>
<tr><td>PD(8:15)</td><td>x</td><td>1</td><td>0</td><td>1</td><td>Byte 3</td></tr>
<tr><td>PD(0:15)</td><td>x</td><td>0</td><td>0</td><td>0</td><td>Word 0</td></tr>
<tr><td>PD(0:15)</td><td>x</td><td>1</td><td>0</td><td>0</td><td>Word 1</td></tr>
</table></td></tr>
<tr><td>76</td><td>WR</td><td>I/O</td><td>WRITE/READ – This signal is directly connected to the CPU WR signal. This signal is an input when the CPU has control of the bus and it is an output when the WD6010 DMA controller has control of the bus. Together with DC and M/$\overline{IO}$, these signals identify the type of bus cycle being executed on the CPU bus.</td></tr>
<tr><td>75</td><td>DC</td><td>I/O</td><td>DATA/CONTROL – This signal is directly connected to the CPU DC signal. This signal is an input when the CPU has control of the bus and it is an output when the WD6010 DMA controller has control of the bus. Together with WR and M/$\overline{IO}$, these signals identify the type of bus cycle being executed on the CPU bus.</td></tr>
<tr><td>74</td><td>M/$\overline{IO}$</td><td>I/O</td><td>MEMORY $\overline{I/O}$ –This signal is directly connected to the CPU M/$\overline{IO}$ signal. This signal is an input when the CPU has control of the bus and it is an output when the WD6010 DMA controller has control of the bus. Together with WR and DC, these signals identify the type of bus cycle being executed on the CPU bus.

<table>
<tr><th>M/$\overline{IO}$</th><th>DC</th><th>WR</th><th>WD6010 FUNCTION</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Does not occur</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Does not occur</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>I/O Read</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>I/O Write</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Does not occur</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Does not occur</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Memory Read</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Memory Write</td></tr>
</table></td></tr>
</table>

PIN NO.	NAME	TYPE	FUNCTION
73	ADS	I/O	ADDRESS STROBE – This signal is directly connected to the CPU ADS signal. This signal is an input when the CPU has control of the bus and it is an output when the WD6010 DMA controller has control of the bus. This signal is used to track bus cycles.
71 70 69 68	BE3 BE2 BE1 BE0	I/O	BYTE ENABLE – These signals are used during data transfers to indicate which data bytes are valid on the CPU data bus. During DMA operations these signals are output signals. When the system CPU accesses the WD6010 registers, they are input signals. The definition of these signals changes to match the type of microprocessor (80386SX or (80386/80486), as configured by DACK at power-up.

SIGNAL	80386SX	80386/80486
BE3	BE3	Not connected
BE2	BE2	PA1
BE1	BE1	BEH
BE0	BE0	BEL

132	RDY	I	READ – This signal is directly connected to the CPU READY signal. This signal is used to track bus cycles. It is synchronized with CLK2.
131	NA	I	NEXT ADDRESS – This signal is generated by the WD6030 whenever a pipelined cycle can be supported by the system. If this signal is asserted and the WD6010 has an internal request pending, the WD6010 goes into pipelined mode. For the WD6010 this is an input only signal, that is applicable during DMA transfers. Figure 4 illustrates a non-pipelined transfer and Figure 5 illustrates a typical pipelined transfer.
130	BS16	I	BUS SIZE 16 – This signal is generated by the WD6030 to indicate whether the CPU or WD6010 is accessing a 32-bit or (16-bit or 8-bit) port. The signal is high whenever a 32-bit port is accessed and all the byte enables should be active. BS16 is low whenever a 16-bit port or 8-bit port is accessed. The byte enables are sampled to determine if the access is to a 16-bit or 8-bit port.
3 1	CLK CLK2	I	CLOCKS – CLK is a CMOS-level clock signal which has the same frequency as the CPU. CLK2 is also a CMOS-level clock. CLK2 has a frequency twice that of the CPU clock frequency. The WD6010 shares the CLK2 signal with the CPU.

12

PIN NO.	NAME	TYPE	FUNCTION
66	$\overline{TC}$	O	$\overline{TERMINAL\ COUNT}$ – This signal is generated by the WD6010 DMA controller logic during the last I/O bus cycle of a DMA transfer to indicate that the DMA channel currently servicing the Channel has reached a terminal count condition. This indicates to the DMA slave that this is the last cycle to be performed.
		ARBITRATION CONTROL	
126	UCHMASTR	I/O	CHANNEL MASTER – This pin has dual functions. At power-up (trailing edge of $\overline{RESET}$), the state of this signal is latched and in conjunction with A20GTX, determine the speed at which the system will operate. At all other times, UCHMSTR is an output signal which becomes active whenever a Micro Channel master other than the CPU or the WD6010 DMA controller gets control of the bus. **FREQUENCY / UCHMSTR / A20GTX** 16 MHz / 0 / 0 20 MHz / 0 / 1 25 MHz / 1 / 1 33 MHz / 1 / 0
119	$\overline{NMI}$	I/O	$\overline{NON\text{-}MASKABLE\ INTERRUPT}$ – When driven by the WD6010 to the CPU, $\overline{NMI}$ indicates that the CACP has reached a bus time-out condition while monitoring the bus. When the signal is received from the WD6000, it tells the CACP to initiate an arbitrated cycle to remove any bus masters so that the CPU can service the interrupt.
22 21 20 19	ARB3 ARB2 ARB1 ARB0	I/O	ARBITRATION BUS – These four open collector lines comprise the aribtration bus. These signals are driven by DMA slaves, system master and bus masters when requesting control of the bus during arbitration cycles. When the floppy disk controller requests the bus through FDDRQ, the ARB (0:3) signals are driven by the WD6010.
18	$\overline{PREEMPT}$	I/O	$\overline{PREEMPT}$ – This open collector line signals that an arbitrating device wants to use the bus, and the CACP initiates an arbitration cycle when this line is active. A floppy disk controller request, a refresh cycle request, or the receipt of a $\overline{NMI}$ causes this signal to be driven by the CACP in the WD6010.
129	HLDA	I	HOLD ACKNOWLEDGE – The CPU asserts HLDA in response to a HOLD signal to indicate that it has relinguished the local bus.

PIN NO.	NAME	TYPE	FUNCTION
125	FDDRQ	I	FLOPPY DISK REQUEST – This signal indicates that the floppy disk controller requires the DMA controller to transfer data. The CACP translates this request into a level 2 priority and competes for the bus.
15	$\overline{\text{BURST}}$	I	$\overline{\text{BURST}}$ – This input signals that the current Channel bus owner will continue to hold the bus for more than one transfer. For DMA transfers, $\overline{\text{BURST}}$ is removed during the last I/O bus cycle of the transfer or if a terminal count is reached.
12	INTR	I	INTERRUPT – If bit 4 of the CACP register, port 90H, is set and a master other than the CPU is using the bus, this interrupt signal is used to initiate an arbitration cycle. This allows the CPU to service an interrupt during bus master cycles.
8	$\overline{\text{REFREQ}}$	I	$\overline{\text{REFRESH REQUEST}}$ – This timer output signal is generated by the WD6000 to request a refresh cycle. The WD6010 responds by driving the $\overline{\text{PREEMPT}}$ signal. The CACP enters the ARB state and requests the bus. The refresh cycle is executed and the bus returned to the $\overline{\text{GNT}}$ state. If the CACP is already in the ARB state, the refresh request extends the period by one bus cycle.
7	EOT	I	END OF TRANSFER – This signal from the WD6022 Address Buffer indicates an end of transfer condition. An end of transfer occurs when $\overline{\text{CMD}}$, $\overline{\text{S0}}$ and $\overline{\text{S1}}$ are inactive on the Channel. Internally, EOT is ORed with $\overline{\text{BURST}}$ to show an end of transfer condition.
67	$\overline{\text{REFRESH}}$	O	$\overline{\text{REFRESH}}$ – This Channel signal indicates that the memory read operation on the bus is a refresh cycle. Address lines (2:10) and $\overline{\text{BE}}$(0:3) hold the state of the refresh address counter in the DMA controller. Address lines (11:31) are driven to zero. In response, the WD6030 performs a memory read operation on the Channel and a RAS-only refresh for the motherboard DRAM. On the Channel, any slave can choose to extend the refresh cycle by de-asserting CHRDY.
65	ARB/$\overline{\text{GNT}}$	O	ARBITRATION/$\overline{\text{GRANT}}$ – This signal indicates the state of the CACP. In the arbitration state (high), an arbitration cycle is in progress and all devices wishing to own the bus drive their arbitration levels on the arbitration bus and compete for Channel ownership. At the end of the arbitration cycle (300 ns minimum), ownership of the Channel is given to the owner with the winning arbitration level. The change to a grant cycle is signified by the change in the polarity of the signal to $\overline{\text{GNT}}$ (low).

12

PIN NO.	NAME	TYPE	FUNCTION
63	HOLD	O	HOLD – This signal is synchronous with CLK2. When asserted, it requests the CPU to relinguish the CPU bus for a refresh, DMA, or Channel master transfer.
			RESET CONTROL
14	$\overline{\text{SHUTDOWN}}$	I	$\overline{\text{SHUTDOWN}}$ – This signal initiates a CPU reset and is generated by the 8742 keyboard controller, as commanded by the CPU.
13	PWRGOOD	I	POWERGOOD – This signal originates in the power supply and indicates the state of the power supply voltages. $\overline{\text{RESET}}$ is derived from the state of this line.
79	RES387	O	80387 RESET – This reset signal is generated on a system reset or a NPX soft reset and is an unsynchronized reset for the NPX. It must be externally synchronized with CLK2387 before being sent to the NPX. On a system reset, the pulse width of this signal is determined by the power supply logic. On a NPX soft reset (an I/O write to port F1H), this signal has a pulse width of at least 256 CLK2s. When the NPX is operating at half the frequency of the 80386, the pulse width is 128 CLK2387 periods (CLK2387 period = 2*CLK2 period).
78	RES386	O	80386 RESET – This signal is generated by the WD6010 by the following reset sources; Power-On, Alternate Hot Reset, Keyboard Shutdown or Processor Shutdown. It must be externally synchronized with CLK2 before being sent to the CPU.
77	$\overline{\text{RESET}}$	O	$\overline{\text{RESET}}$ – This signal is derived from the state of the PWRGOOD signal. It is synchronized with CLK2 and resets all the components in the system. While active no memory refreshes take place.
			NUMERIC COPROCESSOR EXTENSION (NPX) HALF-SPEED INTERFACE
124	$\overline{\text{RDYO}}$	I	$\overline{\text{READYOUT}}$ – This signal is the $\overline{\text{READYO}}$ from the NPX. When used in Full Speed Mode, this pin should be connected to VDP. When used in Half-Speed Mode, this signal is used to track bus cycles to the NPX.
6 4	CLK387 CLK2387	I I	80387 CLOCKS – CLK387 is a CMOS-level clock signal which is generated by external circuitry and is synchronized with CLK. CLK2387 is also a CMOS-level clock signal. It is synchronized with CLK2. These two signals should be connected to VDD when the NPX is used in Full-Speed Mode. In Half-Speed Mode, these signals will operate at half the speed of CLK and CLK2 respectively.

PIN NO.	NAME	TYPE	FUNCTION
123	$\overline{\text{RDYO387}}$	O	$\overline{\text{80387 READYOUT}}$ – When the NPX is used in Full-Speed Mode, this signal is left unconnected and the READYO output from the NPX is directly connected to the logic for $\overline{\text{RDY}}$.
122	$\overline{\text{ADSO}}$	O	$\overline{\text{ADDRESS STROBE}}$ – This signal is the address strobe output to the NPX in Half-Speed Mode. In Full-Speed Mode, this pin is a N/C.
			PARITY ERROR INTERFACE
120	ENPCHK	O	ENABLE PARITY CHECK – This signal is a duplication of bit 0 of the Memory Encoding Register 1 (port E1H) in the WD6030. It is used to enable/disable parity checking. The signal directly interfaces with the external parity latches. Refer to the WD6030 Data Sheet for more information.
82	$\overline{\text{EDRENA}}$	O	$\overline{\text{EXTENDED DATA REGISTER ENABLE}}$ – When active, $\overline{\text{EDRENA}}$ enables the selected ESF register to read or write. This signal is generated by comparing the CPU I/O address to the value stored in the ESF Pointer Register (port xxH).
81	VGAEN	O	VIDEO GRAPHICS ADAPTER ENABLE – When enabled by the Video Subsystem Enable Register (port 3C3H, bit 0), this signal decodes the upper address bits (20:31) for the system board video RAM area, A00000H to BFFFFFH.
80	$\overline{\text{CDSETEN}}$	O	$\overline{\text{CARD SETUP ENABLE}}$ – This signal decodes I/O addresses. 100H to 107H with the appropriate timing for the WD6000 for channel setup cycles in the system.
			MISCELLANEOUS
5 30 55 83 100 116	V_{DD}	I	+5 POWER SUPPLY
2 17 23 35 43 50 64 72 87 98 108 128	V_{SS}	I	0V GROUND
11	N/C		Not Connected

12

PIN NO.	NAME	TYPE	FUNCTION
16	$\overline{\text{TEST}}$	I	$\overline{\text{TEST}}$ – This is an active low signal that facilitates board-level testing. When low, this signal tri-states all outputs and bi-directional signal lines, allowing an ATE tester to drive these signals. When high, the outputs and bi-directional lines are enabled by the chip.

Figure 4 illustrates a typical non-pipelined bus cycle for the WD6010, and shows that the bus interface for the WD6010 is identical to the 80386.

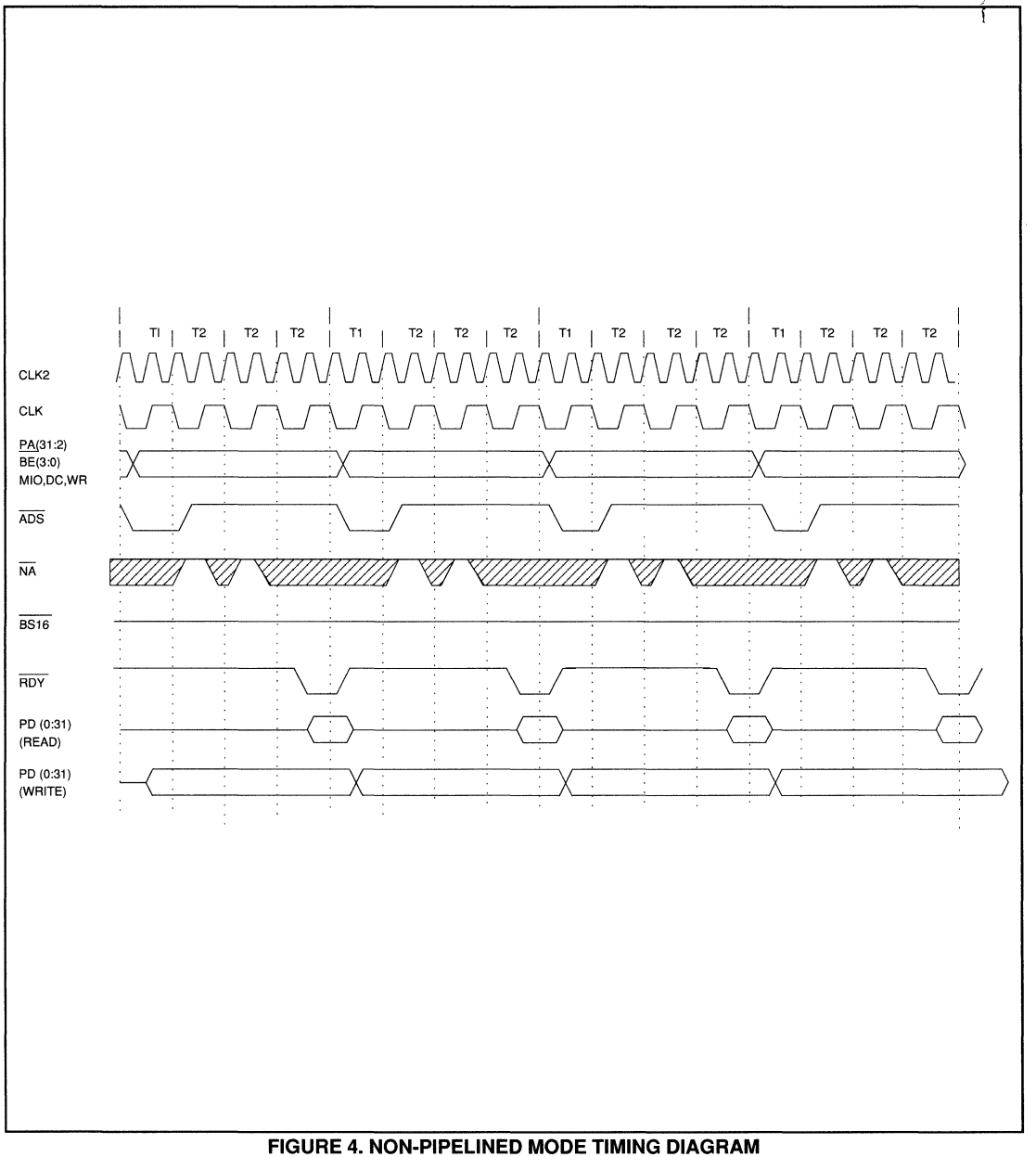


FIGURE 4. NON-PIPELINED MODE TIMING DIAGRAM

Figure 5 illustrates a typical Pipelined bus cycle for the WD6010. The WD6010 generates bus cycles which are identical to the 80386 bus cycles.

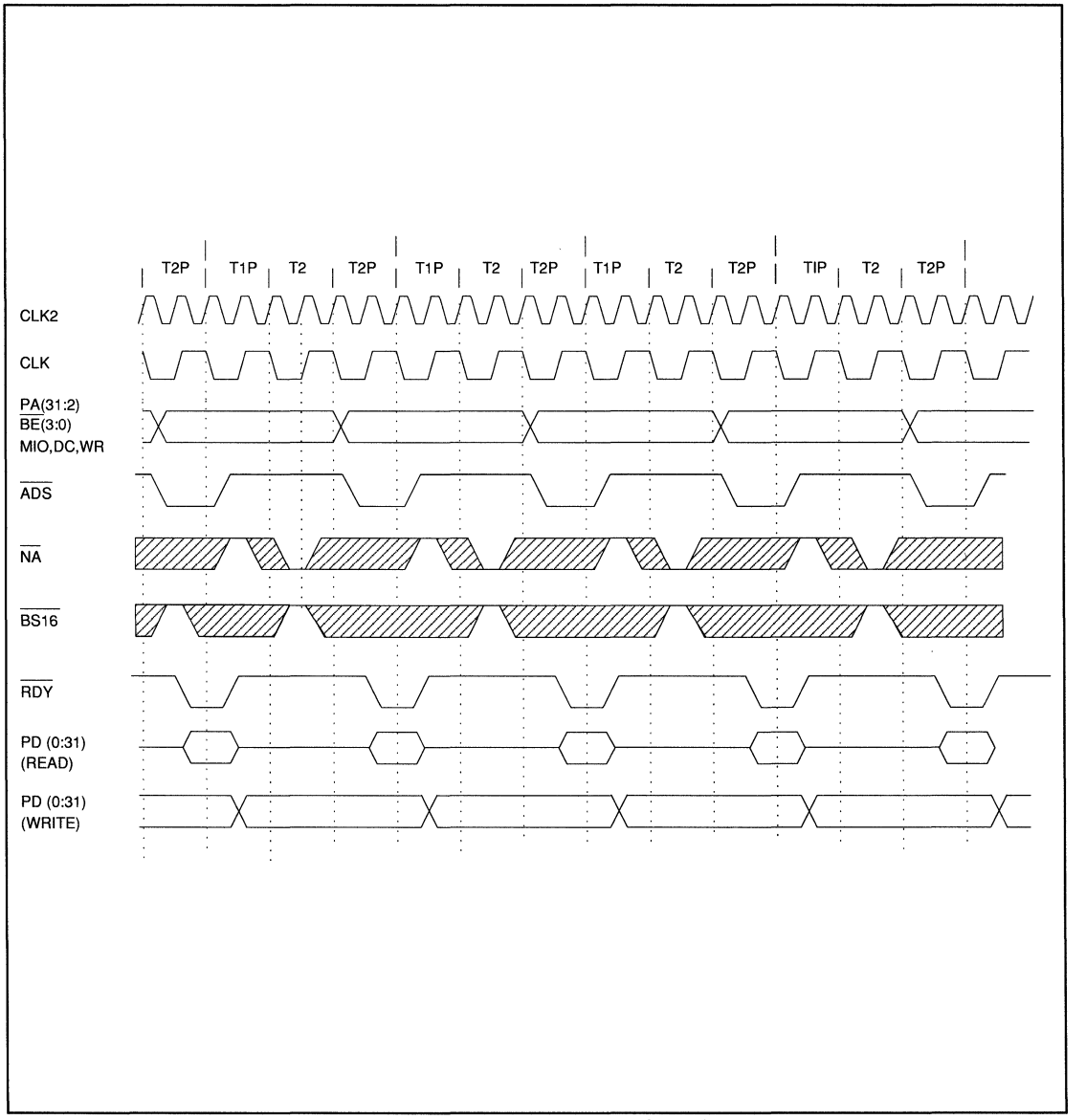


FIGURE 5. PIPLINED MODE TIMING DIAGRAM

ADDRESS RANGE	LOCATION	FUNCTION
0000 to 000FH	WD6010	DMA Controller Chs 0-3*
0018H	WD6010	Extended Function Reg.*
001AH	WD6010	Extended Function Execute*
0020 to 0021H	WD6000	Interrupt Controller 1
0040, 0040-0044, 0047H	WD6000	System Timers
0060H	WD6000	Keyboard Data Port
0061H	WD6000	System Control Port B
0064H	WD6000	Rd - Keyboard Status, Wr –Keyboard Command
0070H	WD6000	RTC/CMOS Address Register, NMI Mask
0071H	WD6000	RTC/CMOS Data Port
0074H	WD6000	EAR0 Extended CMOS RAM, ESF
0075H	WD6000	EAR1 Extended CMOS RAM
0076H	WD6000	Extended CMOS RAM Data Port
0081 to 0083, 0087H	WD6010	DMA Page Registers 0-3*
0089 to 008B, 009FH	WD6010	DMA Page Registers 4-7*
0090H	WD6010	CACP Register*
0091H	WD6000	Card Selected Feedback
0092H	WD6000	System Control Port A
0094H	WD6000	System Board Setup
0096, 0097H	WD6000	POS, Channel Connector Select
00A0, 00A1H	WD6000	Interrupt Controller 2
00C0 to 00DFH	WD6010	DMA Controller (even only)*
00E0 to 00E1H	WD6030	Memory Control Registers
00E2 to 00E7H	WD6010	Diagnostic Registers
00F0H	WD6000	Coprocessor Clear Busy
00F1H	WD6000	Coprocessor Reset
00F8 to 00FFH	NPX	80387/80387SX Coprocessor*
0100, 0101H	WD6000	System ID
0102 to 0107H	WD6000	Board Configuration (POS)
0278 to 027BH	WD6000	Parallel Port 3
02F8 to 02FFH	WD6000	Alternate Serial Port
0378 to 037BH	WD6000	Parallel Port 2
03BC to 03BFH	WD6000	Parallel Port 1
03B4, 03B5, 03BA, 03C0-03C5H	WD90C00	Video Subsystem**
03CE, 03CF, 03D4, 03D5, 03DAH	WD90C00	Video Subsystem
03C6 to 03C9H	WD90C00	Video DAC**
03F0 to 03F7H	WD6000	Diskette Drive Controller
03F8 to 03FFH	WD6000	Primary Serial Port
0700H	WD6010	ESF Data Register (Default)

TABLE 1. SYSTEM LEVEL I/O MAP (WD6500)

* No Channel cycle generated on these addresses.
**The WD90C00 Enable Register (03C3H) is in the WD6010.

3.0 DMA CONTROLLER

The DMA Controller is a serial transfer device compatible with the Intel* 8237, and includes the IBM extended controller interface and functions. Its logic supports eight independent channels, six of which are assigned fixed priorities. The remaining two have programmable priorities.

The WD6010 takes two channel cycles to transfer a word or byte between memory and I/O. Each channel cycle needs two or more CPU clock cycles. Channel and bus arbitration functions are resolved externally.

3.1 DMA Interface

The DMA Controller interfaces to the system on the CPU local bus. As the table in the description of the PD signals shows, it generates and encodes the same control signals as the CPU. The controller may be programmed at any time that Hold Acknowledge (HLDA) from the CPU is inactive. The programming may only be done by the system CPU.

Each of the two transfer bus cycles requires two or more CPU clock cycles. The time taken by the I/O portion of the cycle depends on the response from the system interface: whether it is a local cycle or a Channel cyle. All Channel cycles take at least 200 ns. The time taken by the memory portion of the cycle depends on the response from the system interface, that is, if it is a local cycle versus a Channel cycle, cache hit versus a cache miss, page hit versus a page miss, and so on.

A Channel transfer is established by the CPU setup and initiated from an external slave source through arbitration control in the form of DMAREQ input. The requesting DMA channel is specified on the ARB bus input.

3.2 Internal Architecture

The internal architecture of the DMA Controller in the WD6010 is based on the six basic modules described in the subsections that follow.

3.2.1 Address Translator

This module converts address and data information from the CPU interface that is in PC/AT Compatibility Mode format into the Extended Mode format. This information is then stored for run-time use.

3.2.2 RAM Registers

These RAM locations store the 32-bit base address, the 32-bit current address, the 16-bit base count, the 16-bit current count, and the 16-bit current I/O address, for each channel. The current values are read/write and are written by the CPU at the same time as the base registers. An additional register, the Transfer Holding Register, temporarily stores data between bus cycles of a transfer. This register can not be accessed by the system CPU.

The RAM array is 112 bits x 8 locations, with one location allocated to each channel. The Channel 0 and 4 implement the Virtual DMA feature of the Micro Channel system.

3.2.2.1 Base Memory Address Register

This 32-bit register is initialized by the CPU through byte-wide accesses. This is a write register and can not be read by the CPU. In Compatibility Mode, three writes are executed to program twenty-four address bits, and four writes are executed in Enhanced Addressing Mode to program thirty-two address bits.

3.2.2.2 Current Memory Address Register

The CPU initializes this 32-bit read/write register by byte-wide accesses at the same time that it initializes the Base Memory Address Register. This register can also be read in byte-wide accesses.

During DMA transfers, this register is incremented or decremented after each memory bus cycle. Enabling Auto-Initialize reloads this register at the end of a transfer with the value stored in the Base Memory Address Register. This state is reached when the DMA controller reaches a terminal count condition and the $\overline{TC}$ signal has been generated. Figure 6 illustrates a read cycle with Auto-Initialize, followed by another transfer.

3.2.2.3 Base Transfer Count Register

The CPU initializes this 16-bit register in byte-wide accesses. The number of transfers is the value in the register + 1. The WD6010 does a single transfer when this register is programmed to 0000H.

3.2.2.4 Current Transfer Count Register

The CPU initializes this 16-bit read/write register by byte-wide accesses at the same time that it

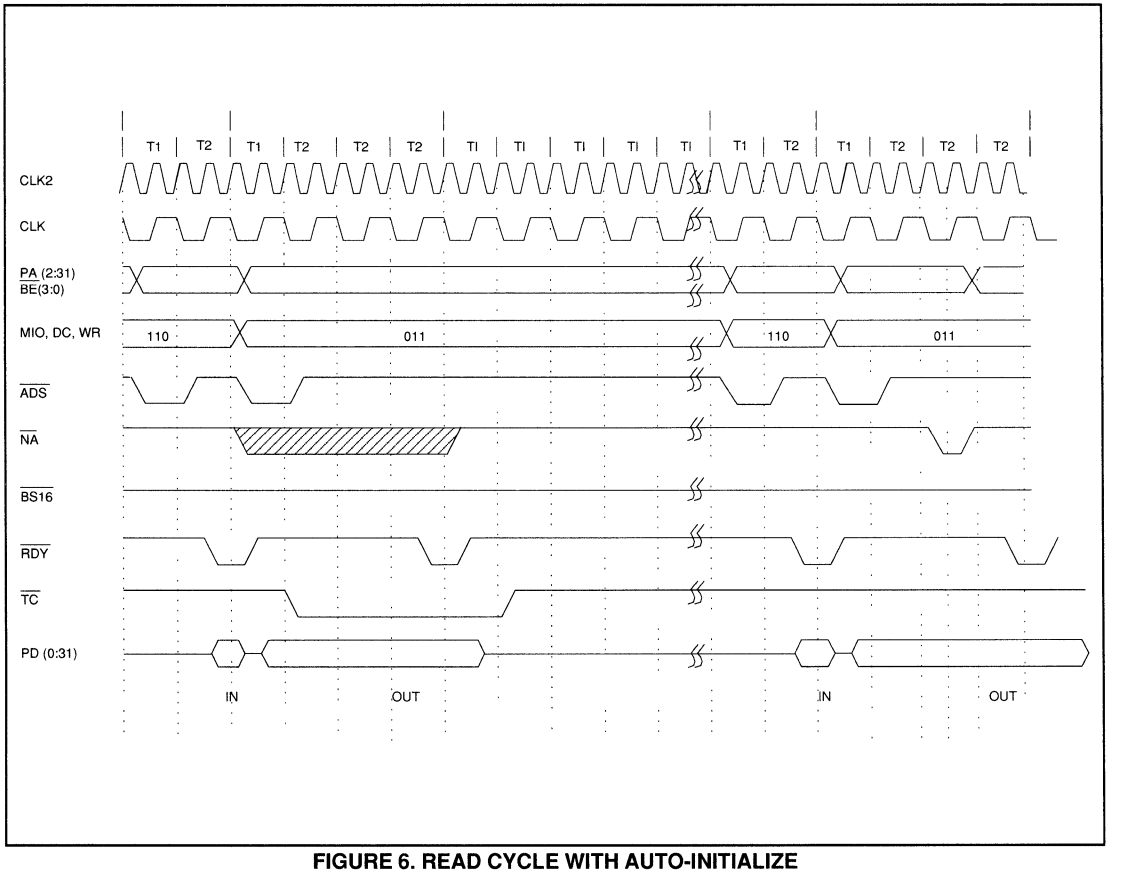


FIGURE 6. READ CYCLE WITH AUTO-INITIALIZE

initializes the Base Transfer Count Register. The CPU can read it in byte-wide accesses.

During DMA transfers, this register is decremented after each memory bus cycle. Enabling Auto-Initialize reloads this register at the End-of-Transfer (EOT) with a value from the Base Transfer Count Register.

3.2.2.5 Current I/O Address Register

This register is initialized by the CPU in Extended Mode only. The value gated to the bus during the I/O bus cycle depends on the state of Bit 0 in the Extended Mode Register. If Programmed I/O Address Mode is set, then the value in the register is used; if not, 0000H is used.

3.2.2.6 Temporary Holding Register

This register temporarily stores data between bus cycles of a transfer. The CPU can not access this register.

3.2.3 DMA Registers

The DMA registers consist of the Mask, Mode, Arbus, and Status registers. Table 2 shows the allocation of these registers.

Figure 7 shows the format for the Mask register, and Figure 8 shows the format for the Mode Register. See Section 3.3 for a description of the various modes and transfer types set in the Mode Register.

REGISTER	SIZE	QTY	ALLOCATION
MASK	8 bits	2	1 for Chs 0-3 1 for Chs 4-7
MODE	8 bits	8	1 per channel
ARBUS	8 bits	2	1 for Ch 0, 1 for Ch 4
STATUS	8 bits	2	1 for Chs 0-31 1 for Chs 4-7

TABLE 2. DMA REGISTER ALLOCATION

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

RESERVED				MASK BIT		CHANNEL SELECT			
0				DIS	ENA	–		–	
						1	0	Channel	
						0	0	0 or 4	
						0	1	1 or 5	
						1	0	2 or 6	
						1	1	3 or 7	
RESERVED		CH 3 OR 7		CH 2 OR 6		CH 1 OR 5		CH 0 OR 4	
0		DIS	ENA	DIS	ENA	DIS	ENA	DIS	ENA

Default = [ ]

FIGURE 7. MASK REGISTER FORMAT

Mode Select		Count Dir		Auto Initial		Transfer Type		Channel Select	
—	—	DEC	INC	ENA	DIS	—	—	—	—

7	6	Mode Select
0	0	Demand
0	1	Single (N)
1	0	Block (N)
1	1	Cascade(N)

3	2	Transfer Type
0	0	Verify
0	1	Write Mem
1	0	Read Mem
1	1	Reserved

1	0	Channel
0	0	0 or 4
0	1	1 or 5
1	0	2 or 6
1	1	3 or 7

PC/AT Compatible Mode

Extended Mode

Reserved	Width		Reserved	Count Dir		Transfer		Transfer		Auto Initial		IO Adr	
0	16 Bit Xfer	8 Bit Xfer	0	DEC	INC	Write Mem	Read Mem	Data	Verify	On	Off	Prog Value	0000H

N=Not Used

FIGURE 8. MODE REGISTER FORMAT

RESERVED				ARBITRATION LEVEL			
–	–	–	–	–	–	–	–

3	2	1	0	Level
0	0	0	0	0 Available
0	0	0	1	1 See Warning
0	0	1	0	2 See Warning
0	0	1	1	3 See Warning
0	1	0	0	4 Available
0	1	0	1	5 See Warning
0	1	1	0	6 See Warning
0	1	1	1	7 See Warning
1	0	0	0	8 Available
1	0	0	1	9 Available
1	0	1	0	A Available
1	0	1	1	B Available
1	1	0	0	C Available
1	1	0	1	D Available
1	1	1	0	E Available
1				F Reserve-System MPU

WARNING:
These levels are assigned to DMA channels 1-3, 5-7. If channel 0 or 4 is assigned to one of these levels, the user must insure that no conflict occurs.

FIGURE 9. ARBUS REGISTER FORMAT

12

Request Status								Terminal Count Status							
Chan 3 or 7		Chan 2 or 6		Chan 1 or 5		Chan 0 or 4		Chan 3 or 7		Chan 2 or 6		Chan 1 or 5		Chan 0 or 4	
Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No
Default =															

FIGURE 10. STATUS REGISTER FORMAT

The two Arbus registers, one each for DMA Channels 0 and 4, implement the "virtual DMA" feature. The software can use these registers to dynamically re-assign the arbitration level to which these channels respond during a DMA operation. This allows Channels 0 and 4 to service devices at any arbitration level. Normally, Channels 0 and 4 are assigned levels 08H to 0EH only, Levels 01-03H and 05-07H are assigned to DMA Channels 1-3 and 5-7. If Channels 0 or 4 are assigned one of these levels, it is up to the user to ensure that there are no conflicts. Figure 9 illustrates the Arbus register format.

In Extended Mode, a status read provides the status of Channels 0-3, and a second read gives the status of Channels 4-7. The byte pointer is initialized when the command is given. Figure 10 shows the format of the Status Register.

3.2.4 Transfer Control

This module provides the interface for the CPU bus. The signals and timings are equivalent to those of the CPU, and are generated from the same CPU clock source.

3.2.5 Register Control

This control function co-ordinates the various modules during a DMA transfer cycle.

3.2.6 Work Registers

These registers are used for the temporary storage of data and parameters during and between DMA transfer bus cycles.

3.3 System CPU Access Modes

The system CPU can access the DMA controller in two modes: PC/AT Compatibility Mode, and PS/2 Extended Mode. At run-time, the mode through which the transfer was set up is not retained.

The WD6010 does not support the Compatibility Mode command, and request and rotating priority functions. The Mode register is only supported to the extent detailed in the following subsections.

3.3.1 Compatibility Mode

Table 3 provides an I/O map of this mode.

I/O ADRS	DESCRIPTION	BIT WIDTH	BYTE PTR
0000H	Ch 0 Memory Adrs. Reg. (R/W)	15-00	yes*
0001H	Ch 0 Transfer Count Reg. (R/W)	15-00	yes*
0002H	Ch 1 Memory Adrs. Reg. (R/W)	15-00	yes*
0003H	Ch 1 Transfer Count Reg. (R/W)	15-00	yes*
0004H	Ch 2 Memory Adrs. Reg. (R/W)	15-00	yes*
0005H	Ch 2 Transfer Count Reg. (R/W)	15-00	yes*
0006H	Ch 3 Memory Adrs. Reg. (R/W)	15-00	yes*
0007H	Ch 3 Transfer Count Reg. (R/W)	15-00	yes*
0008H	Chs 0-3 Status Register	07-00	-
000AH	Chs 0-3 Mask Reg. (Set/Rst)(W)	07-00	-
000BH	Chs 0-3 Mode Register (W)	07-00	-
000CH	Chs 0-3 Clear Byte Pointer (W)	N/A	-
000DH	Chs 0-3 Master Clear (W)	N/A	-
000EH	Chs 0-3 Clear Mask Register (W)	N/A	-
000FH	Chs 0-3 Write Mask Register (W)	07-00	-
0081H	Ch 2 Page Register (R/W)	07-00	-
0082H	Ch 3 Page Register (R/W)	07-00	-
0083H	Ch 1 Page Register (R/W)	07-00	-
0087H	Ch 0 Page Register (R/W)	07-00	-
0089H	Ch 6 Page Register (R/W)	07-00	-
008AH	Ch 7 Page Register (R/W)	07-00	-
008BH	Ch 5 Page Register (R/W)	07-00	-
008FH	Ch 4 Page Register (R/W)	07-00	-
00C0H	Ch 4 Memory Adrs. Reg. (R/W)	15-00	yes*
00C2H	Ch 4 Transfer Count Reg. (R/W)	15-00	yes*
00C4H	Ch 5 Memory Adrs. Reg. (R/W)	15-00	yes*
00C6H	Ch 5 Transfer Count Reg. (R/W)	15-00	yes*
00C8H	Ch 6 Memory Adrs. Reg. (R/W)	15-00	yes*
00CAH	Ch 6 Transfer Count Reg. (R/W)	15-00	yes*
00CCH	Ch 7 Memory Adrs. Reg. (R/W)	15-00	yes*
00CEH	Ch 7 Transfer Count Reg. (R/W)	15-00	yes*
00D0H	Chs 4-7 Status Register	07-00	-
00D4H	Chs 4-7 Mask Reg. (Set/Rst)(W)	07-00	-
00D6H	Chs 4-7 Mode Register (W)	07-00	-
00D8H	Chs 4-7 Clear Byte Pointer (W)	N/A	-
00DAH	Chs 4-7 Master Clear (W)	N/A	-
00DCH	Chs 4-7 Clear Mask Register (W)	N/A	-
00DEH	Chs 4-7 Write Mask Register (W)	07-00	-

TABLE 3. COMPATIBILITY MODE I/O MAP

* Both Memory Address and Transfer Count Registers are loaded on a write operation; only the Current register is readable.

3.3.2 Extended Mode

This mode is accessed through four locations in the I/O space, as Table 4 shows. The format for the Extended Function Register (EFR), 0018H, is shown in Figure 11.

The protocol for Extended Mode is as follows:

1.Write to the EFR (0018H) to set the channel selection and function command. This resets the internal byte pointer to point to least significant byte (LSB). Direct commands only require an I/O write to the EFR. If it is not a direct command, go on to Step 2.

2.Write or read the appropriate number of times to execute the function from the EFE port. The byte pointer increments automatically.

Direct commands written to the EFR include Mask Register Set Bit, Mask Register Reset Bit, and Master Clear. The Mask Register Set Bit command masks or disables all the channels in the Mask Register. The Mask Register Reset Bit command unmasks or enables all the channels in the Mask Register. The Master Clear can be generated by the CPU or by a bus time-out condition. If a Master Clear command is given, the DMA controller must be re-initialized. The Master Clear masks all the channels in the Mask Register, that is, it sets all the bits to one. It also resets all the bits of the Status Register to zero.

I/O ADDRESS	DESCRIPTION
0018H	Extended Function Register (EFR) (W)
0019H	Reserved
001AH	Extended Function Execute (EFE) (W)
001BH	Reserved

TABLE 4. EXTENDED MODE I/O ADDRESS

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Programmed Command (1AH)				Reserved	Channel Selection		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

7	6	5	4	Command	Bit Width	Byte Ptr
0	0	0	0	I/O Adr Reg (R/W)	00–15	yes
0	0	0	1	1 Reserved	—	—
0	0	1	0	2 Mem Adr Reg (R/W)	00–23	yes
0	0	1	1	3 Mem Adr Reg Read	00–23	yes
0	1	0	0	4 Xfer Cnt Reg (R/W)	00–15	yes
0	1	0	1	5 Xfer Cnt Reg Read	00–15	yes
0	1	1	0	6 Status Reg Read	00–07	yes
0	1	1	1	7 Mode Reg (R/W)	00–07	—
1	0	0	0	8 Arbus Reg (R/W)	00–07	—
1	0	0	1	9 Mask Reg Set Bit	Direct	—
1	0	1	0	A Mask Reg Reset Bit	Direct	—
1	0	1	1	B IBM Test DRQ	—	*
1	1	0	0	C IBM Test Clear	—	*
1	1	0	1	D Master Clear	Direct	—
1	1	1	0	E Reserved	—	—
1	1	1	1	F Reserved	—	—

* These functions are not implemented.

2	1	0	Channel
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

FIGURE 11. EXTENDED FUNCTION REGISTER (EFR) (0018H)

3.3.3 Enhanced Mode

The DMA Controller Enhanced Mode is a Western Digital innovation implemented on the WD6010 which extends the DMA address space up to 4 Gbytes. A DMA operation can now take place in Memory Addresses 00000000 to FFFFFFFFH.

The WD6010 powers up in a mode compatible with the Model 80, which allows DMA operation in Compatibility Mode or Extended Mode. The memory address space in which a DMA operation can take place extends from 000000 to FFFFFFH. If the addresses exceed FFFFFFH, they roll over to 000000. Address Bits 24 to 31 are always zero in this mode.

Setting the Mode 4 Gig bit in the Enhanced Addressing Register (ESF:018CH) puts the WD6010 in Enhanced Mode. In this mode, the addresses roll over to 00000000 if they exceed FFFFFFFFH, instead of FFFFFFH.

When in this mode, all the channels generate 32-bit addresses. To program the memory addresses for thirty-two bits, four writes to the Memory Address Register should be executed in Extended Mode. To read back the memory addresses, four reads are executed to the same locations. Internally, the bytes are organized as Bytes 0, 1, 2, and 3. If the upper-most byte is not programmed, the old value is used. Therefore, care must be taken to program all the bytes with their proper values. Figure 12 shows the bit assignment for Register ESF:18CH.

3.4 DMA Operation

The state of the HLDA signal from the CPU distinguishes the operaion of the DMA controller. If HLDA is inactive, the operating mode of the DMA controller can be programmed. See Section 5, Arbitration Control, for more information. If HLDA is active, the DMA can only execute transfer cycles that have been set up previously.

To terminate a transfer, the DMA controller examines the state of the BURST signal. As long as this signal is active and the terminal count (TC) has not been reached, transfers continue to be executed. If BURST is inactive at the beginning of a transfer, a single transfer is executed.

3.4.1 Single Transfer Mode

This mode consists of one I/O bus cycle and one memory bus cycle, in either order. A single transfer is executed when BURST is found to be inactive at the beginning of a cycle.

3.4.2 Demand Transfer Mode

Demand transfers are continous transfers carried out as long ast the BURST signal remains active. They may be either slave-terminated or controller-terminated.

A slave-terminated transfer ends under either of two conditions. The transfer ends when the slave has transferred one byte or word and has not asserted the BURST signal, or when the slave has completed a partial transfer and releases BURST during the last I/O cycle.

A controller-terminated transfer can only end when the TC has been reached for that channel. At EOT, the channel is masked from further operation until the CPU interacts with it. Figures 13 to 15 provide timing diagrams of typical DMA operations in Demand Transfer Mode.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Reserved								**Mode**		**Reserved**				**Addressing**	
Bit 7		**Bit 6**		**Bit 5**		**Bit 4**		**Bit 3**		**Bit 2**		**Bit 1**		**Bit 0**	

0	80386 Mode
1	80386SX Mode

0	16 MByte Addressing
1	4 GByte Addressing

FIGURE 12. ENHANCED ADDRESSING REGISTER ESF:018CH

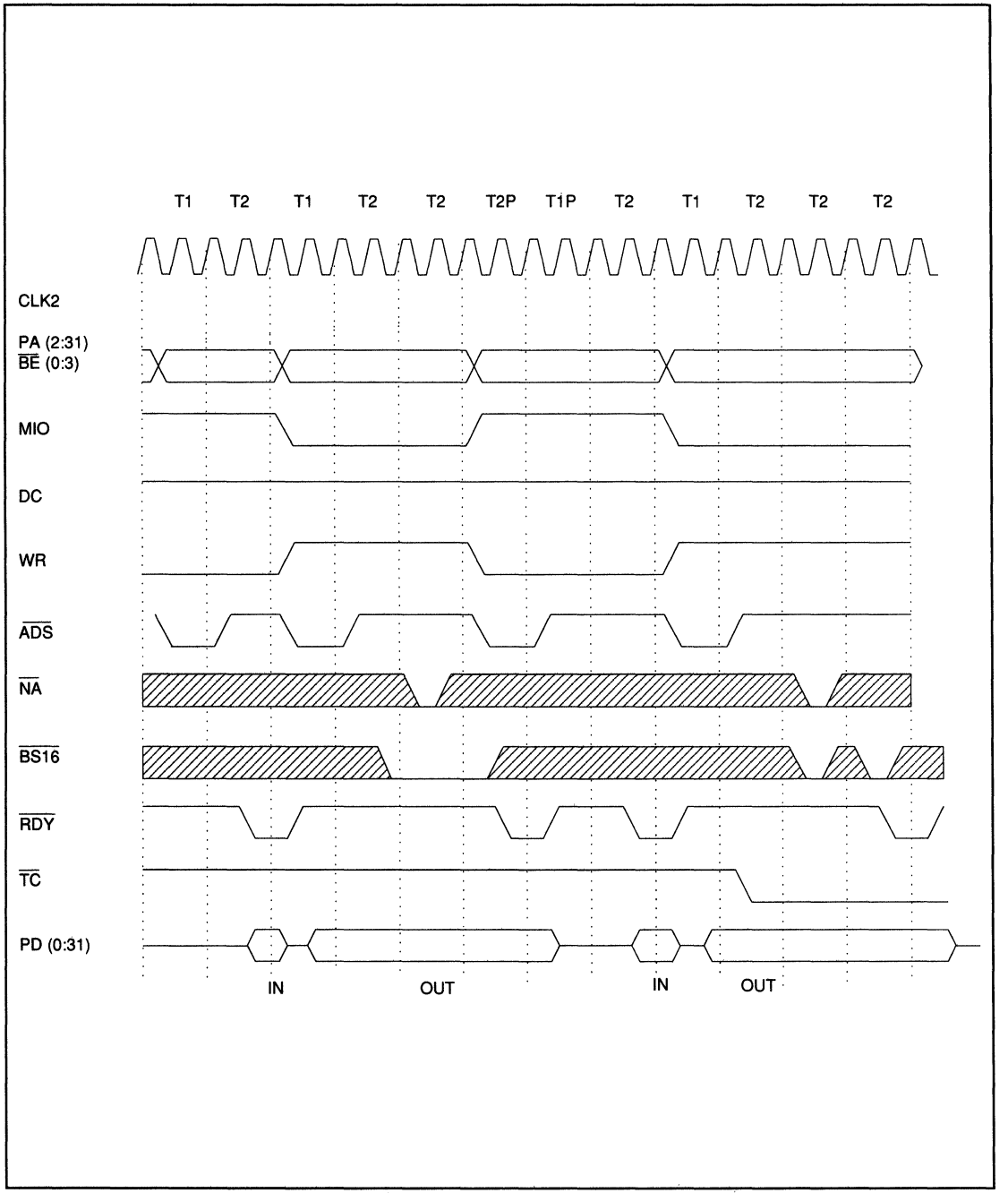


FIGURE 13. 16-BIT READ TRANSFER with COUNT EXPIRATION

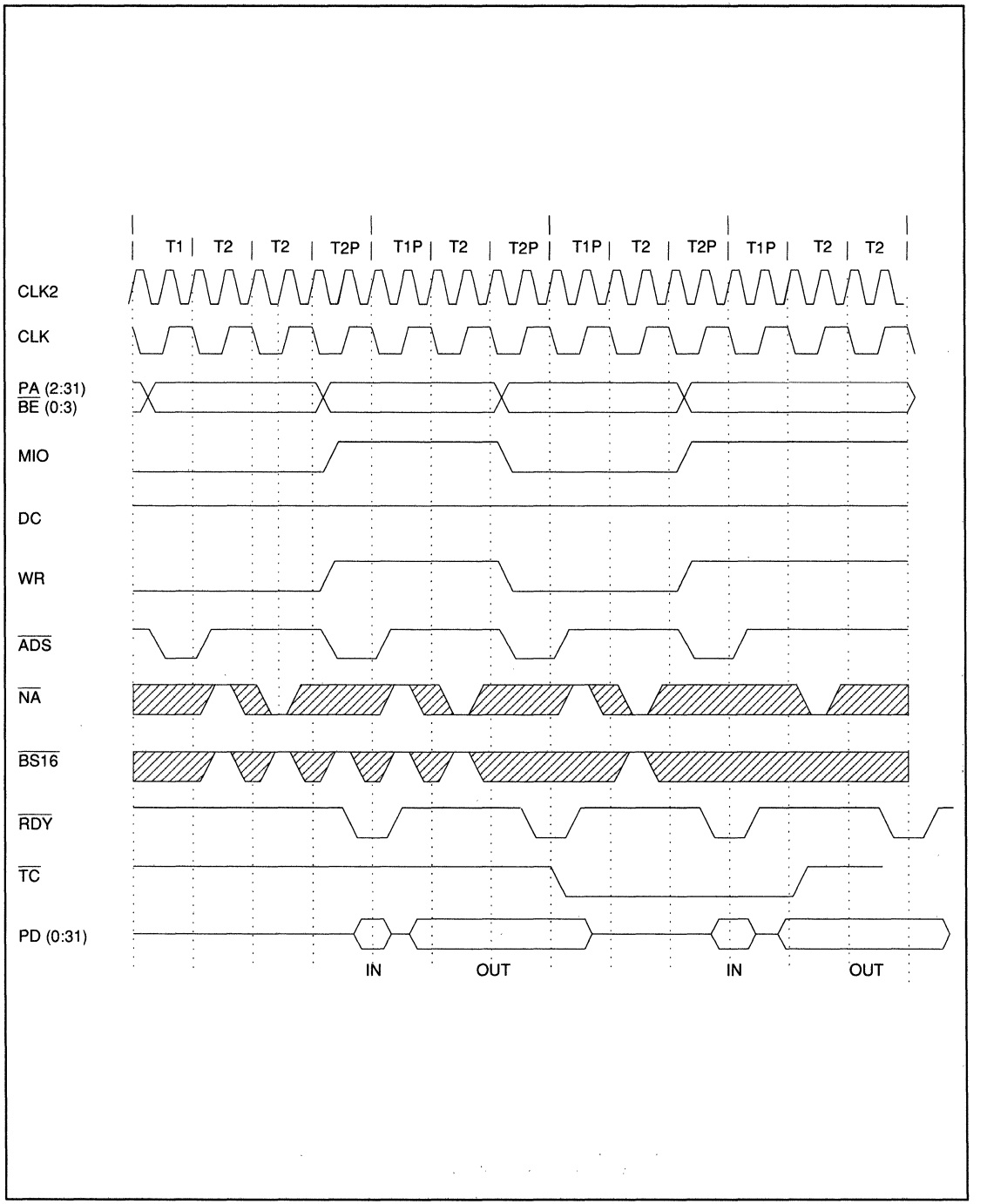


FIGURE 14. 16-BIT WRITE TRANSFER with COUNT EXPIRATION

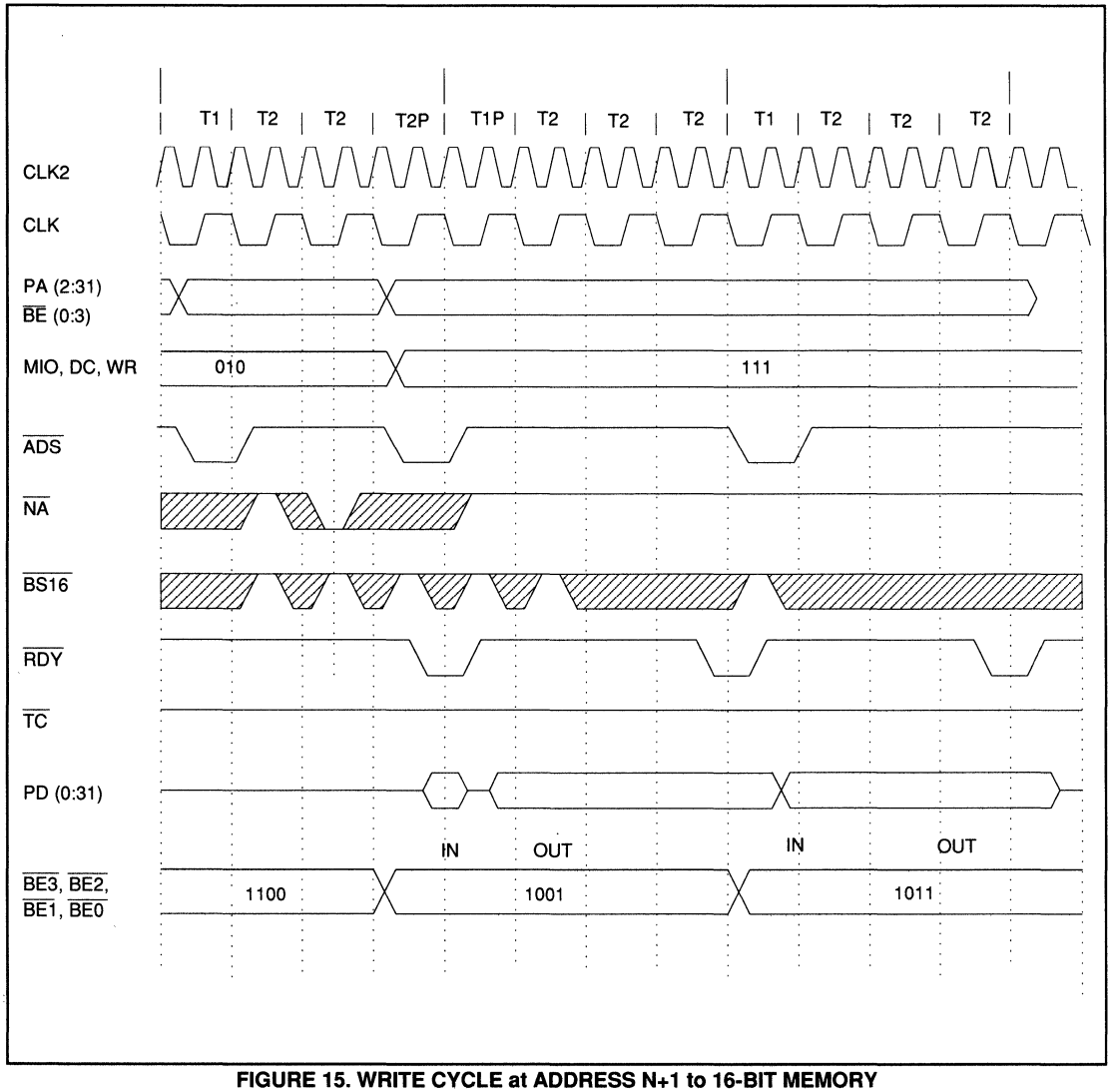


FIGURE 15. WRITE CYCLE at ADDRESS N+1 to 16-BIT MEMORY

3.4.3 Verify Mode

This mode performs address and $\overline{TC}$ generation as in normal transfers, but only initiates memory read commands on the bus. Figures 16 and 17 illustrate this mode through timing diagrams.

3.4.4 Submodes

Auto-initialize Mode allows a channel to operate continuously without interaction from the CPU. At EOT, the values in the Base Memory Address Registers are loaded into the Current Memory Address Registers; the channel remains unmasked.

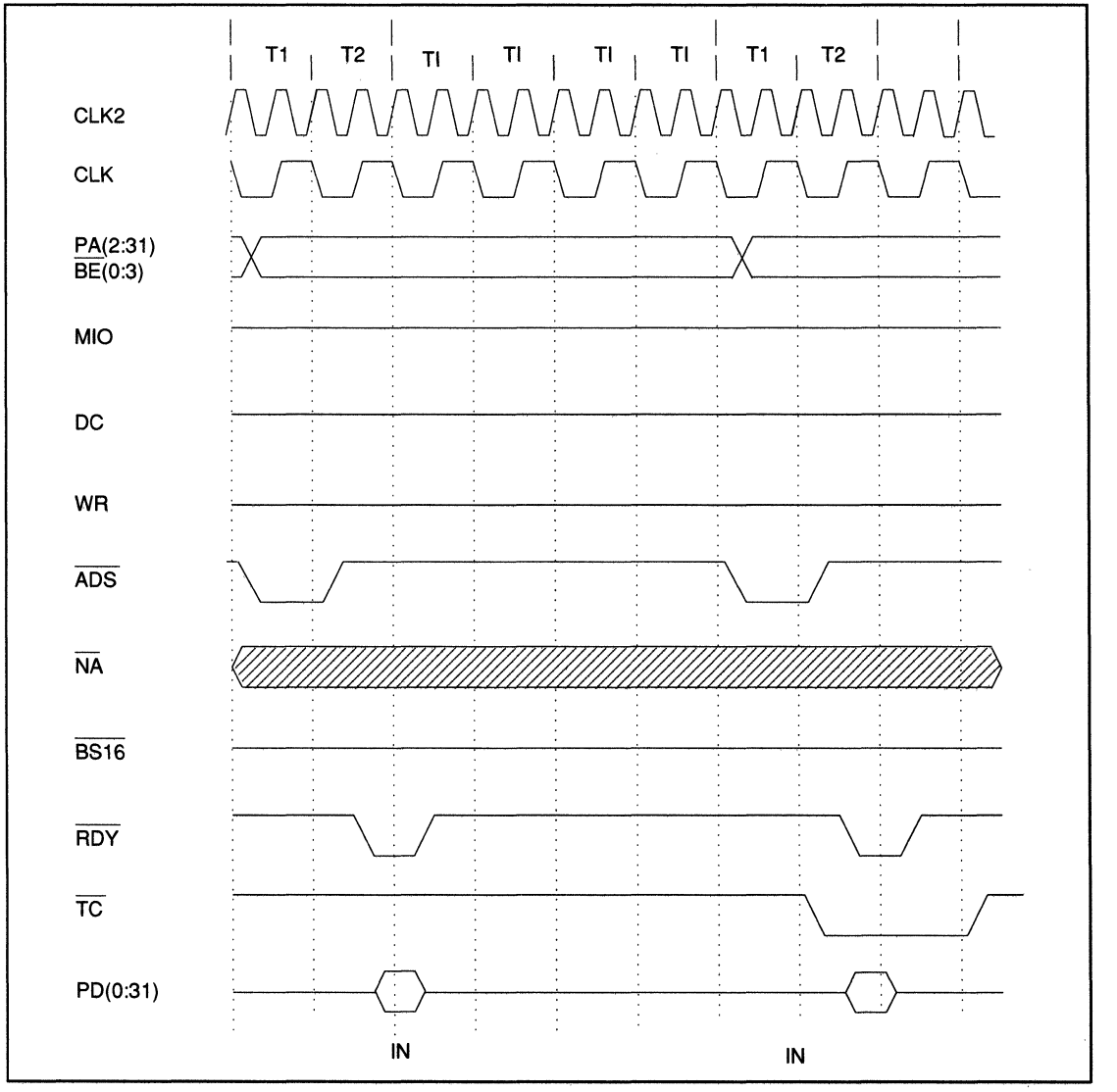


FIGURE 16. VERIFY TRANSFER with TRANSFER COUNT EXPIRATION

The Increment/Decrement submode can set each channel Memory Address Register to increment or decrement.

3.4.5 Boundary and End Conditions

When the Memory Address Register reaches the end of a 64 Kbyte segment of memory, it carries into the upper byte of the counter without indicating this to the CPU.

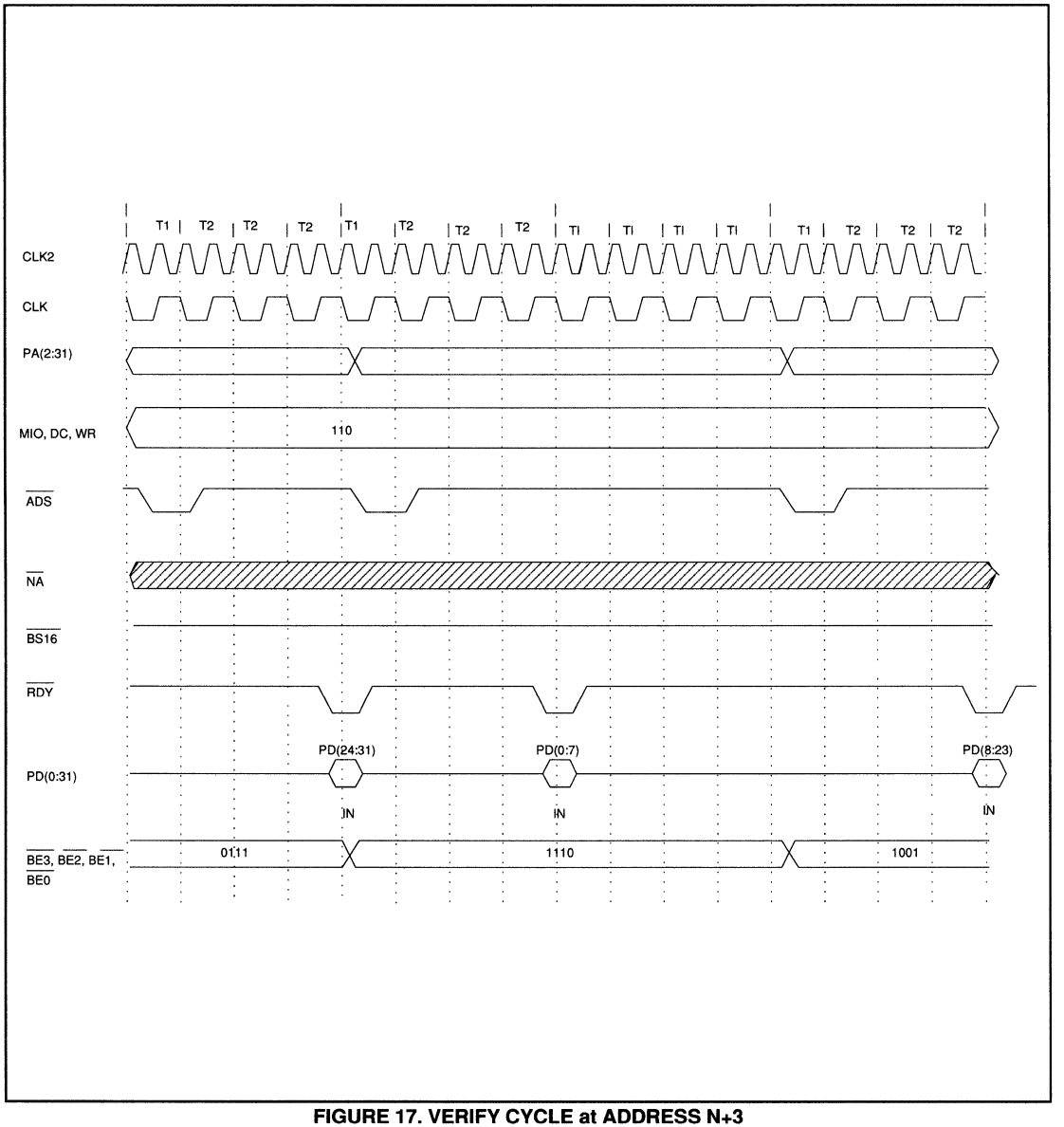


FIGURE 17. VERIFY CYCLE at ADDRESS N+3

With a 16M or 4 GByte physical memory limit, if the Current Transfer Count Register has a valid count remaining and the DMA slave continues to request service, the Current Memory Address Register rolls over to Address 0 and continues. If the transfer is a memory write, no warning is given of the alteration to low memory.

At $\overline{TC}$, the Current Transfer Count Register decrements to FFFFH and stops. If the register was initially set to FFFFH, the counter decrements until it encounters FFFFH again.

At EOT, the mask register bit is not set if Auto-Initialize was selected for that channel, as this would disable the channel.

3.4.6 Direct Commands

The Clear Byte Pointer command initializes the internal byte pointer to point to the least significant byte.

The Master Clear command sets the Mask Register to mask or disable all channels. It also resets all status bits to zeros.

The Clear Mask Register command unmasks or enables all the channels.

The Write All Register Mask Bits command masks or disables all the channels.

3.4.7 Enhanced Mode

Il the DMA operations described in this section are valid when the system is operating in Enhanced Mode. However, it must be remembered that all channels generate 32-bit addresses when in this mode, necessitating four read or write operations to program the memory addresses. See Section 3.3.3 for more information.

4.0 RESET CONTROL

The clock and reset control functions on the WD6010 include the generation of CPU resets, coprocessor resets, and general system resets.

The Alternate Hot Reset Function specified by Control Port A (0092H, Bit 0) is write-only in the WD6010 and read/write on the WD6000. Figure 19 shows the Clock and Reset control function in an WD6010-based system. The block diagram shows an WD6500 system; however, the same architecture applies to any system based on the WD6010.

The generation of different resets is described in the Pin Description Table.

The clock rates and the signal pins are shown in Table 5. The state of three signal pins at power-on reset (POR) determines the clock rates. After POR, the pins revert to their normal functions.

Frequency	UCHMSTR (F_1)	A20GTX (F_0)
16 MHz	0	1
20 MHz	0	0
25 MHz	1	1
33 MHz	1	0

TABLE 5. CLOCK RATE DEFINITIONS

12

5.0 ARBITRATION CONTROL (AC)

Arbitration Control controls and monitors the Channel and local bus arbitration functions. The AC functions are controlled by the bit settings in the Arbitration Register at 0090H. Figure 18 shows the format for the Arbitration Register.

5.1 Arbitration Register

The Arbitration Register (0090H) controls the different functional parameters of the CACP. Figure 18 shows the bit assignments for this register for read and write operations.

5.2 Arbitration Control Functions

The Central Arbitration Control Point (CACP) functions are discussed in more detail in the subsections that follow.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
CPU Cycles		NMI Occurred		Bus Timeout		IRQ Master Preempt		Arbitration Level							
ENA	DIS	Yes	No	Yes	No	ENA	DIS								
Read															
CPU Cycles		ARB State		ARB Cycle		IRQ Master Preempt		Reserved							
ENA	DIS	Arb	Gnt	Extd	Norm	ENA	DIS	—		—		—		—	
Write															
Default=															

FIGURE 18. ARBITRATION REGISTER FORMAT (0090H)

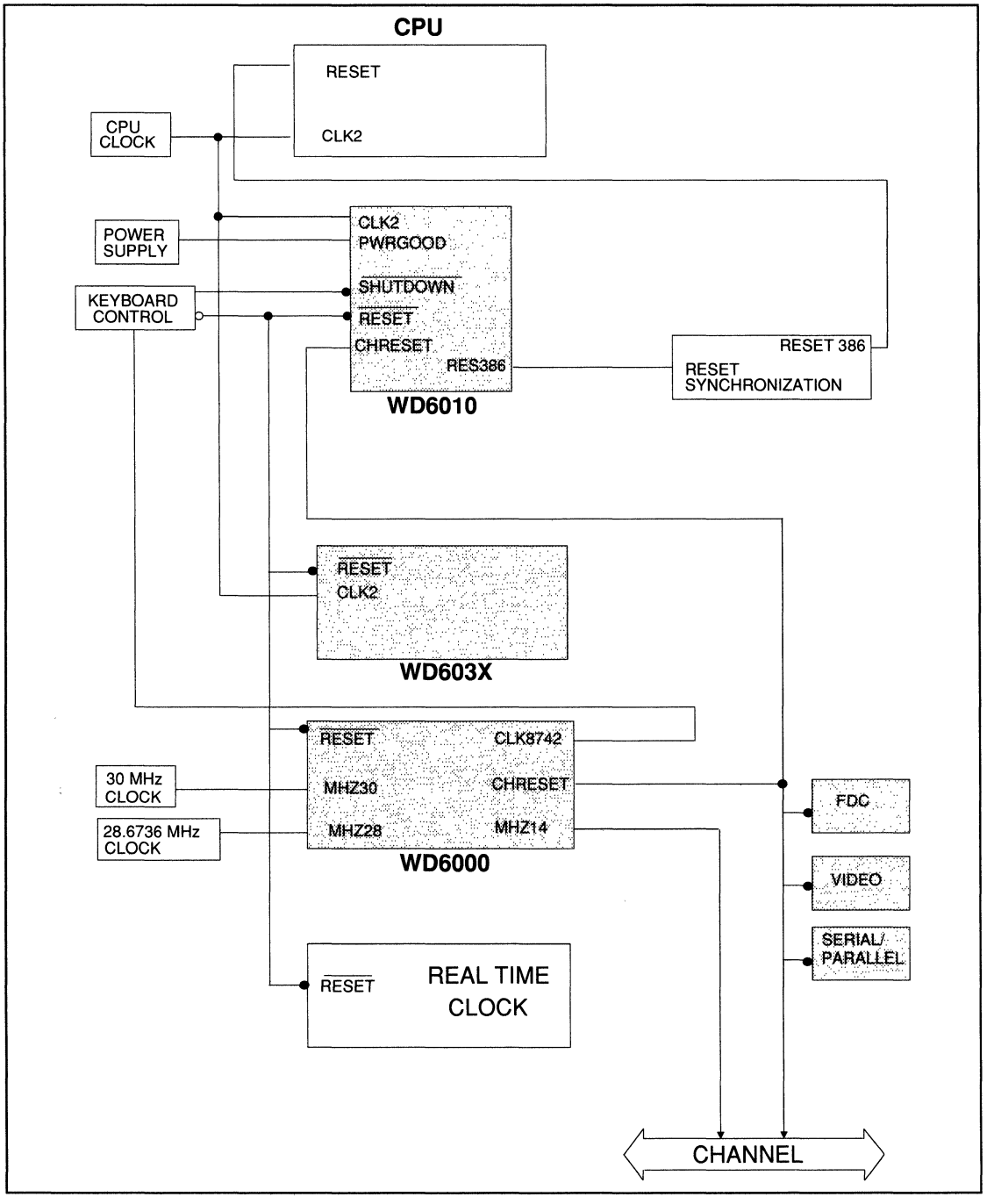


FIGURE 19. SYSTEM CLOCK and RESET CONTROL

5.2.1 Execute Arbitration Cycles

An arbitration cycle is defined as a transition of the ARB/GNT signal from low to high to low, GNT to ARB to GNT. When it is high (ARB), all competing local arbiters may drive ARB (0:3) to determine the new bus owner. Refresh cycles are executed when ARB/GNT is high and extend the arbitration cycle by that amount. An arbitration cycle can be initiated by these external requests:

- Refresh Request
- Bus Time-out
- Competing Bus Master
- Competing DMA Slave
- NMI
- Bus Idle
- Interrupt, When 0090H, Bit 4 is 1

The bus is at an idle state when a Bus Master or DMA slave has been granted the bus, and CMD, and BURST are not active. It indicates a condition when DMA slave or Bus Master transfers have been executed.

5.2.2 Arbitrate the Local CPU Bus

Bus cycles originating from the DMA slave, Channel bus master, or refresh requests require the CPU to give up the local bus. This arbitration request function is performed by the CACP.

5.2.3 Regulate Arbitration Cycle Duration

5.2.3.1 CPU-Programmable

When Bit 5 of the Arbitration Register (0090H) equals one, the default arbitration cycle is extended from a minimum of 300 ns to a maximum of 750 ns, depending on the CPU clock rate. Table 6 defines this relationship.

CPU Clock	Arbitration Control Register	
	Bit 5=0	Bit 5=1
16 MHz	312.5 ns	750 ns
20 MHz	300 ns	750 ns
25 MHz	300 ns	750 ns
33 MHz	300 ns	750 ns

TABLE 6. EXTENDING ARBITRATION

5.2.3.2 ARB (0:3) = 0000 Special Case

If the Arbitration bus changes to 0000 during an arbitration cycle, the arbitration cycle can be shortened to a minimum of 100 ns.

5.2.3.3 Dynamic Extension of Arbitration Time

Arbitration time can be extended by an NMI or Refresh cycle. The NMI sets Bit 6 of the Arbitration Register to one, which forces the ARB/GNT signal to ARB until the CPU resets that bit to zero.

5.2.4 Arbitration Monitor

Since the Channel arbitration mechanism is distributed between the system board and the Micro Channel-based peripherals, a central monitoring point is needed to allow for error recovery. The CACP monitors the Channel bus, and when a bus master does not release the bus as requested by an asserted PREEMPT signal, it hands system control to the CPU, so that the CPU can initiate error recovery.

When a bus time-out occurs, the CACP captures the arbitration level of the device and generates an NMI. The DMA controller is also reset to allow the CPU to attempt error recovery.

The time-out mechanism is based on the refresh timer which cycles approximately every fifteen microseconds. The time-out is armed when a refresh request is pending and when the arbiter is in any state except refresh. If the refresh request is not honored before the next refresh request, a channel time-out condition is said to exist.

The channel time-out and the resulting NMI are held asserted until cleared by a write from the CPU which resets Bit 6 of the Arbitration Register to zero.

5.2.5 Floppy Disk Controller/DMA Interface

On behalf of the floppy disk controller, this function competes for ownership of the system bus by converting DMA requests such as FDDRQ and DACK into the appropriate signals for the CACP.

5.3 PREEEMPT GENERATOR

The WD6010 generates the PREEMPT signal in certain situations, which are described below.

5.3.1 Floppy Disk Controller Request

The CACP generates a $\overline{\text{PREMPT}}$ signal on behalf of the floppy disk controller when the floppy disk controller issues a FDDRQ, and Floppy DMA Controller Channel 2 is not masked. This signal is cleared when a DMA Master Clear command is received or when the bus has been won by Floppy Disk DMA Channel 2 after a bus arbitration cycle.

5.3.2 Refresh Request

A refresh request is made when the $\overline{\text{ARB/GNT}}$ line is in the GNT state will cause a $\overline{\text{PREEMPT}}$ signal to be asserted.

5.3.3 Arbitration Register Bit 6 Set

A $\overline{\text{PREEMPT}}$ is asserted when the ARB/$\overline{\text{GNT}}$ line is in the GNT state and Arbitration Register Bit 6 is set and the ARBUS value is set with any ARB value but a system board value, that is, other than 0FH.

5.3.4 Interrupt Request

A $\overline{\text{PREEMPT}}$ signal is asserted when the ARB/$\overline{\text{GNT}}$ line is in the GNT state, ARB (3:0) $\neq$ 1111B, Arbitration Register Bit 4 is set, and an interrupt request to the CPU is active.

6.0 DECODES

The addresses used by the system control functions are listed below.

1. The ESF Pointer Register (EPR), located at FFFFDH or FFFF, FFFDH, is used to decode the ESF Data Register (EDR).

2. Setup Mode Timing Strobe ($\overline{\text{CDSETEN}}$)

3. The VGA Enable Register (03C3H)

4. Refresh Address Generator (11 bits)

The VGA Enable Register (03C3H) format is defined in Figure 20. When Bit 0 is set to one, an access to an address space below 1 MByte asserts VGAEN, which indicates that the video subsytem is enabled.

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Reserved														VGA Subsystem	
—		—		—		—		—		—		—		ENA	DIS

FIGURE 20. PVGA REGISTER FORMAT

7.0 HALF-SPEED INTERFACE

This interface runs the NPX at half the speed of the CPU, permitting the designer to utilize a slower numeric coprocessor to implement a more cost-effective version. For example, when the CPU is running at 25 MHz, it allows the NPX to operate at 12.5 MHz. When used in half-speed mode, the CLK2387 of the NPX has the same frequency as the CLK signal on the WD6010. The reset signal for the NPX (RES387) must be synchronized to the NPX primary clock (CLK2387) with the proper setup and hold times so that CLK387 has the same phase relationship as the internal CLK of the NPX. The phase relationship and clock frequency are set up at power up, and once set, can not be changed.

Figure 21 shows a block diagram of the NPX half-speed interface, and Figure 22 contains a timing diagram of this interface.

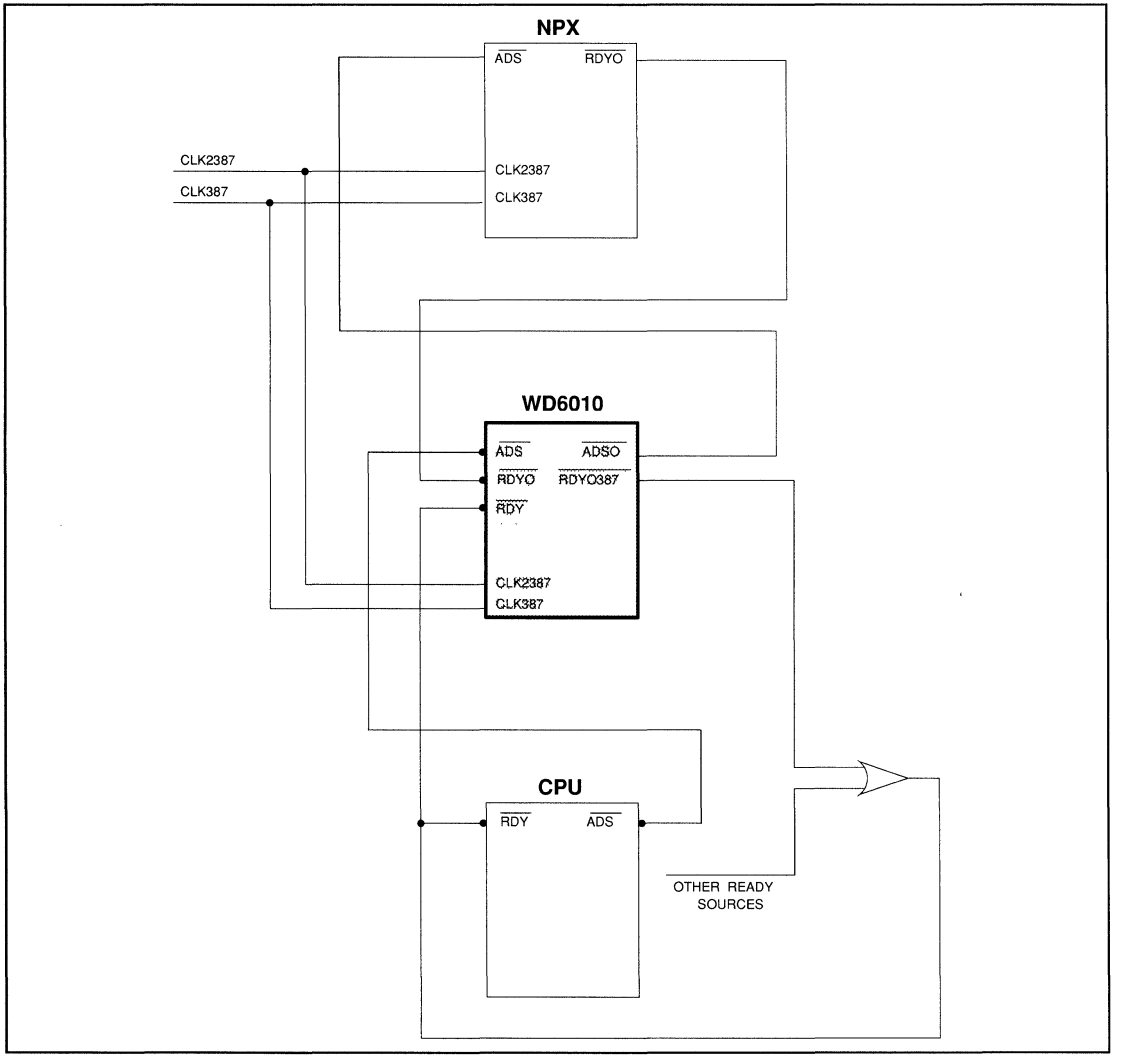


FIGURE 21. NPX HALF-SPEED INTERFACE

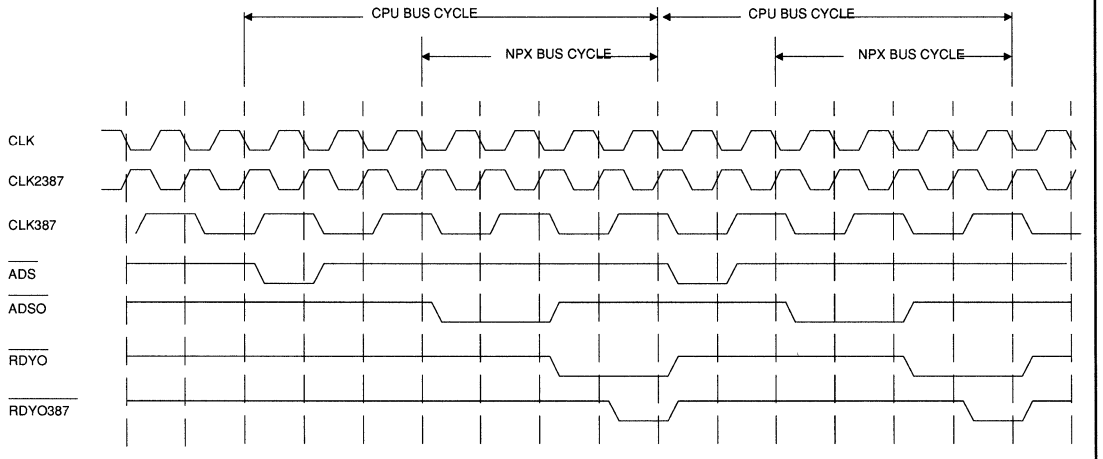


FIGURE 22. NPX HALF-SPEED INTERFACE TIMING DIAGRAM

8.0 DIAGNOSTIC INTERFACE

This logic allows the state of the Micro Channel bus to be latched on a Channel Check condition and is useful to diagnose faults in the system. The error recovery interface is compatible with the Model 80-071.

On a Channel Reset, the latching of the channel state is enabled. At the leading edge of each CMD or MMCMD, the channel state is latched. When a Channel check takes place, the latching is disabled, and the last channel state is retained. The current channel state can be read by the CPU at I/O Locations 00E2H - 00E6H. An I/O Read at 00E7H returns the state of local bus DC pin (Bit 0), and enables the latching again.

The diagnostic signals are described in Section 2. The six read-only diagnostic registers are described here:

- PA (24:31)- 00E2H
- PA (16:23)- 00E3H
- PA (8:15)- 00E4H
- ARB/$\overline{GNT}$, M/$\overline{IO}$, PA (2:7)- 00E5H
- $\overline{BE}$ (0:3), ARB (0:3)- 00E6H
- DC, RESERVED- 00E7H

8.1 Diagnostic Register 1

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
PA31		PA30		PA29		PA28		PA27		PA26		PA25		PA24	

A Read at this location, 00E2H, gives the last latched state of the bus.

8.2 Diagnostic Register 2

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
PA23		PA22		PA21		PA20		PA19		PA18		PA17		PA16	

A Read at this location, 00E3H, gives the last latched state of the bus.

8.3 Diagnostic Register 3

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
PA7		PA6		PA5		PA4		PA3		PA2		M/$\overline{IO}$		ARB/$\overline{GNT}$	

A Read at this location, 00E4H, gives the last latched state of the bus.

8.4 Diagnostic Register 4

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
PA7		PA6		PA5		PA4		PA3		PA2		M/$\overline{IO}$		ARB/$\overline{GNT}$	

A Read at this location, 00E5H, gives the last latched state of the bus.

8.5 Diagnostic Register 5

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
ARB3		ARB2		ARB1		ARB0		$\overline{BE3}$		$\overline{BE2}$		$\overline{BE1}$		$\overline{BE0}$	

A Read at this location 00E6H, gives the last latched state of the bus.

8.6 Diagnostic Register 6

7		6		5		4		3		2		1		0	
1	0	1	0	1	0	1	0	1	9	1	0	1	0	1	0
Reserved														DC	

A Read at this location, 00E7H, gives the last latched state of the bus. It also enables the relatching of the channel state.

9.0 EXTENDED SETUP FACILITY(ESF)

The ESF function consists of the ESF Pointer Register (EPR) and associated decode logic that generates the ESF Data Register Enable (EDRENA) output from the WD6010 to the WD6000. ESF is designed to extend the configuration architecture established with POS features. See Figures 23 and 24 for an overview of the ESF function. ESF supports:

- Memory Map Control Registers
- Additional Physical Serial Port (SP2)
- Programmable Port Enables A and B
- EMS Control Registers
- External DRAM Control Configuration
- System Board LAN Configuration
- Customer-specified Enhancements that include
- System Identification
- System Version

9.1 ESF Access

ESF is based on an "alternate I/O space" concept similar to the way in which the Extended CMOS RAM feature was implemented by IBM. ESF space, which consists of 128 locations, expandable to 32K, is accessed through a single "real I/O space" window called the ESF Data Register (EDR). ESF space may be implemented as word-wide or byte-wide, at the discretion of the designer.

The write-only ESF Pointer Register (EPR), configurable by the software, points to the EDR. It is loaded by writing to memory location FFFFFDH or FFFF, FFFDH, a PROM location. The power-on default location for the EDR is at I/O Address 0700H.

1. Set the value 8DH in Port 0070H to disable NMI.

2. Read System Control Port B at 0061H, and test for a change in the state of Bit 4 (Refresh Toggle) to synchronize it with the refresh circuitry.

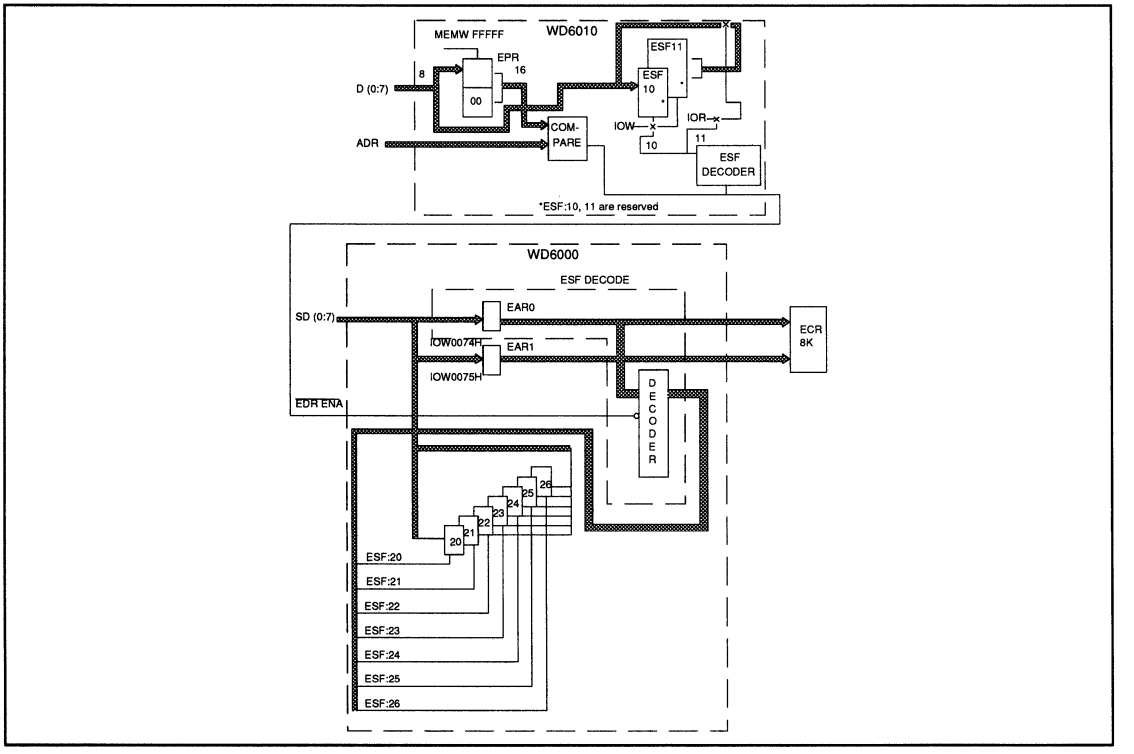


FIGURE 23. ECR & ESF BLOCK DIAGRAM

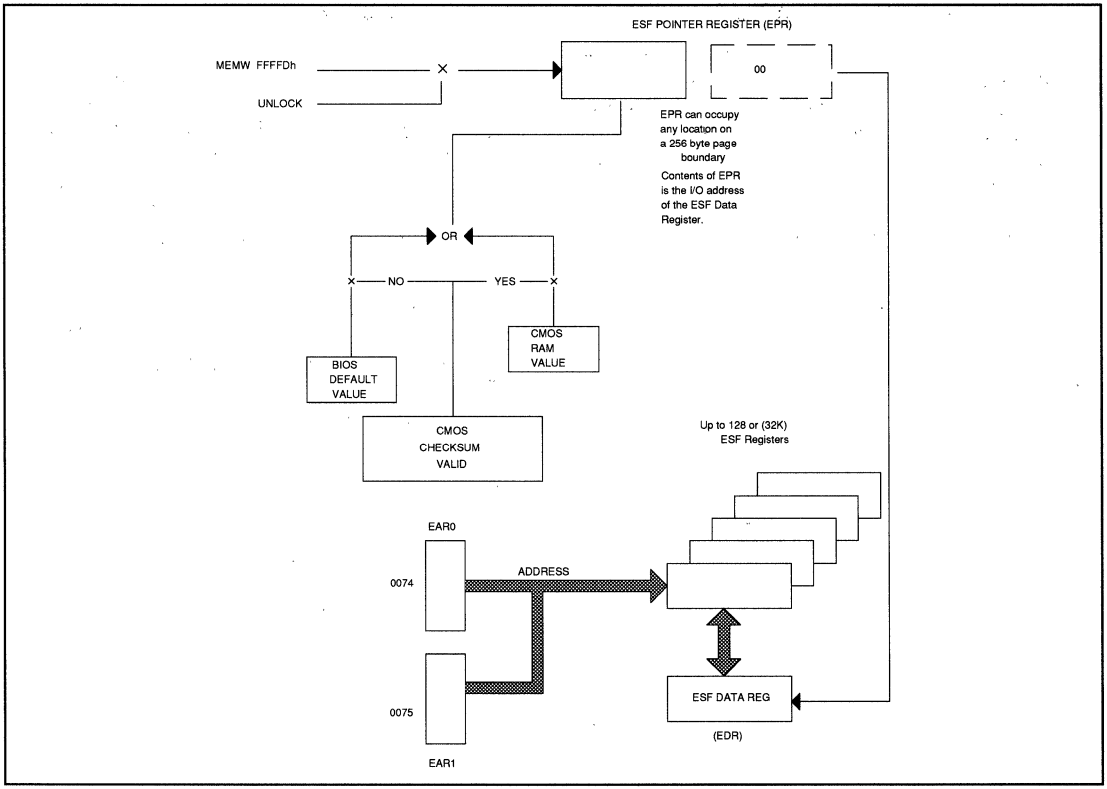


FIGURE 24. EDR and ESF BLOCK DIAGRAM

3. Read EAR0 at 0074H, (normally write-only) to unlock the EPR.

4. Write the new value into the EPR (at FFFFDH). This locks the EPR once again.

5. Enable $\overline{\text{NMI}}$ if required.

Note that the EPR is locked when written, or on the next refresh cycle, whichever occurs first.

The value in EPR becomes the new 8-bit address of the EDR. The EDR can reside at any of 256 locations in the 64K I/O space of the CPU from 0400H to FF00H.

To address the ESF I/O space:

1. Write 8DH to Port 0070H to disable $\overline{\text{NMI}}$.

2. Write the address value to EAR0 at 0074H (and EAR1if expanded ESF is being used).

3. Issue an I/O Read or Write command to the EDR address.

The selected ESF register is determined by decoding the EAR0 address value.

9.2 ESF ADDRESS MAPS

The lower 64 bytes (EAR0 = 00H - 3FH) are reserved for Western Digital functions and features. The upper sixty-four bytes (40H -7FH) can be used by the customer. (see Table 7 for details). All functions using ESF must include Bit 7 of EAR0 in the decode. This bit must be 0 when addressing only 128 ESF registers. To expand the ESF to 32,768 location, set EAR0 Bit 7 to 2 and write the second ESF address byte to EAR1.

ESF ADDRESS	FUNCTION
00H-0FH	System reserved
10H-1FH	System board core functions
20H-3FH	System board peripheral functions

ESF ADDRESS	FUNCTION	R/W	WD6500 DEVICE	WD6400SX/(LP) DEVICE
0 - 001FH	Reserved	-	-	-
20H	Peripheral Configuration	R/W	WD6000	WD6000
21, 24H	Port A,B Control	R/W	WD6000	WD6000
22, 25H	Port A,B Address (LSB)	R/W	WD6000	WD6000
23, 26H	Port A,B Address (MSB)	R/W	WD6000	WD6000
30-3FH	Reserved	-	-	-
40 - 7FH	Customer-specified	-	-	-
0180H	Memory Configuration	R/W	WD6030	WD6036SX/(LP)
0181H	Memory Size Register	R/W	WD6030	WD6036SX/(LP)
0182H	Bank Enable Register	R/W	WD6030	WD6036SX/(LP)
0183H	Split Address Extension	R/W	WD6030	N/A
0184H	Memory Window Bank 0	R/W	WD6030	WD6036SX/(LP)
0185H	Memory Window Bank 1	R/W	WD6030	WD6036SX/(LP)
0186H	Memory Window Bank 2	R/W	WD6030	WD6036SX/(LP)
0187H	Memory Window Bank 3	R/W	WD6030	WD6036SX/(LP)
0188H	CAS Pulse Width	R/W	WD6030	WD6036SX/(LP)
0189H	RAS PreCharge Delay	R/W	WD6030	WD6036SX/(LP)
018AH	RAS Pulse Width	R/W	WD6030	WD6036SX/(LP)
018BH	RAS Access Time	R/W	WD6030	WD6036SX/(LP)
018CH	Enhanced Addressing	R/W	WD6010	N/A
018DH	Reserved	-	-	-
018EH	Reserved	-	-	-
18FH	System Control Register[1] System Configuration[2]	R/W ***	WD6030	WD6036SX/(LP)

TABLE 7. MICRO CHANNEL COMPATIBLE ESF REGISTERS

1. WD6500 implementation only.
2. WD6400SX(LP) implementation only.
*** Dependent on the state of the UCHMASTER and A20GTX signals at reset.

10.0 80386/80486 80386SX ENVIRONMENTS

As described before, the WD6010 can be configured to be used in either an 80386/80486-based system or an 80386SX-based system. The differences in usage in these two environments is summarized in this section.

Certain signals, listed below, have been provided with weak internal pull-ups to ease system design:

- PA (24:31)20K internal pull-up
- PD (16:31)20K internal pull-up
- $\overline{\text{DACK}}$20K internal pull-up
- $\overline{\text{BE}}$ (0:3)20K internal pull-up

When using an 80386/80486-based system, the following points should be noted:

- PD (0:31) connect to the 80386/80486 data lines (0:31)
- PA (2:31) connect to the 80386/80486 address lines (2:31)
- $\overline{\text{BE}}$ (0:3) connect to the 80386 byte enables (0:3).
- The WD6010 $\overline{\text{BS16}}$ connect to the 80386 bus size 16.

When using a 80386SX-based system, the following points should be noted:

- PD (0:15) connect to the 80386SX data lines (0:15), PD (16:51) are left unconnected.
- PA (2:23) connect to the 80386SX address lines (2:23), PA (24:31) are left unconnected.
- $\overline{\text{BE}}$ (0:1) connect to the 80386SX $\overline{\text{BEL}}$ and BEH respectively, BE2 connect the 80386SX address line 1. BE3 is left unconnected.
- BS16 is tied to GND.

11.0 TECHNICAL SPECIFICATIONS

11.1 Absolute Maximum Ratings

The absolute maximum stress ratings for the WD6010 device are tabulated below. Permanent damage to the device could result from exposing it to conditions exceeding these ratings.

11.2 Normal Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	(V_{DD} - V_{SS})	0	7	V
Input Voltage	V_{IABS}	V_{SS} - 0.3	V_{DD} + 0.3	V
Bias on Output Pin	V_{OABS}	V_{SS} - 0.3	V_{DD} + 0.3	V
Storage Temperature	TS	-40	125	°C

Exposure of the device to conditions exceeding the normal operating conditions for extended periods of time can affect the long-term reliability of the device.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.75	5.5	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	-0.3	V_{DD} + 0.3	V
Power Dissipation	PW	-	TBD	mW
Supply Current	I_{DD}	-	TBD	mA

12

11.3 DC Characteristics (under Normal Operating Conditions)

PARAMETER	SYMBOL	MIN	MAX	UNITS
*Input Capacitance @ fc = 1 MHz	CI	–	5	pF
*I/O Capacitance	C_{IO}	–	10	pF
Logic High Input Voltage	V_{IH}	2.0	–	V
Logic Low Input Voltage	V_{IL}	–	0.8	V
*Input Leakage	I_{IL}	–	±10	µA
*Tri-state Output Leakage	I_{OL}	–	±30	µA
*I/O Pin Leakage	I_{IOL}	–	±40	µA
OUTPUTS $\overline{BE}$(0:3), M/$\overline{IO}$, DC, WR, $\overline{ADS}$				
Source Current @ V_{OH} = 2.4V	I_{OH}	–	–	µA
Sink Current @ V_{OH} = 0.4V	I_{OL}	–	24	µA
OUTPUTS $\overline{TC}$, ARB (0:3), $\overline{PREEMPT}$, ARB/$\overline{GNT}$, $\overline{REFRESH}$				
Source Current @ V_{OH} = 2.4V	I_{OH}	–	–	µA
Sink Current @ V_{OH} = 0.4V	I_{OL}	–	24	µA
ALL OTHER OUTPUTS				
Source Current @ V_{OH} = 2.4V	I_{OH}	–	–	µA
Sink Current @ V_{OH} = 0.4V	I_{OL}	–	4	µA

NOTES:

Underlined signals are open collector outputs.

Signals PA (24:31), $\overline{BE3}$, PD(16:31), and $\overline{DACK}$ have internal pullups of 20K.

When $\overline{TEST}$ = 0, all outputs and bi-directional signal lines are tristated.

*Pins ARB (0:3) $\overline{NMI}$ and $\overline{PREEMPT}$ are open collector outputs. Source current value does not apply. External pullups are required on these outputs.

11.4 A.C. Test Loads

OUTPUTS	SYMBOL	MIN	MAX	UNITS
$\overline{BE}$(0:3), WR, M/$\overline{IO}$, DC, $\overline{ADS}$*	CL	-	75	pF
PA(2:31), PD(0:31)*	CL	-	120	pF
ARB(0:3), $\overline{PREEMPT}$	CL	-	200	pF
$\overline{TC}$, ARB/$\overline{GNT}$, $\overline{REFRESH}$	CL	-	240	pF
ALL OTHER OUTPUTS	CL	-	50	pF

NOTE

1.PA(2:31), $\overline{BE}$(0:3), PD(0:31), $\overline{ADS}$, M/IO, DC, WR, ARB(0:3), $\overline{PREEMPT}$, and NMI are bi-directional signals.

2.UCHMSTR, A20GTX, and DACK are inputs only at power-up; they are outputs the rest of the time.

3.$\overline{TC}$ is a tristate output signal.

4.ARB(0:3), $\overline{PREEMPT}$, and NMI are open collector signals and require external pullups.

*These signals are tested at 50 pF for the 25 and 33 MHz frequency.

12

12.0 TIMING

The following inputs are asynchronous to CLK2: A20GATE, PREEMPT, BURST, EOT, FDDRQ, REFREQ, CHCK, CHRESET, UCHCMD, NMI, INTR, SHUTDOWN, PWRGOOD, and ARB(0:3).

The following outputs are asynchronous to CLK2: ARB/GNT, ARB(0:3), DACK, REFRESH, UCHMSTR, A20GTX, RES386, RES387, RESET, and ENPCHK.

The timings in the following table are in nanoseconds, except where specified.

PARAMETER	DESCRIPTION	MIN	MAX	NOTE
T1A	PREEMPT on to EOT	0	7.8 µs	–
T2A	ARB/GNT high from EOT	30	–	1
T3A	PREEMPT off from ARB/GNT low	0	50	–
T4A	BURST on from ARB/GNT low	–	50	–
T5A	ARB/GNT high	300	–	–
T6A	Driver turn-on delay from ARB/GNT high	0	50	–
T7A	Driver turn-off delay from ARB/GNT high	0	50	–
T8A	Driver turn-on delay from higher priority line	0	50	–
T9A	ARB [0:3] stable before ARB/GNT low	10	–	–
T10A	Tristate drivers from ARB/GNT high	–	50	–

TABLE 8. ARBITRATION CYCLES

NOTE
1 EOT signifies the End of Transfer on the Channel with Chs[0:1], BURST, and CMD off.

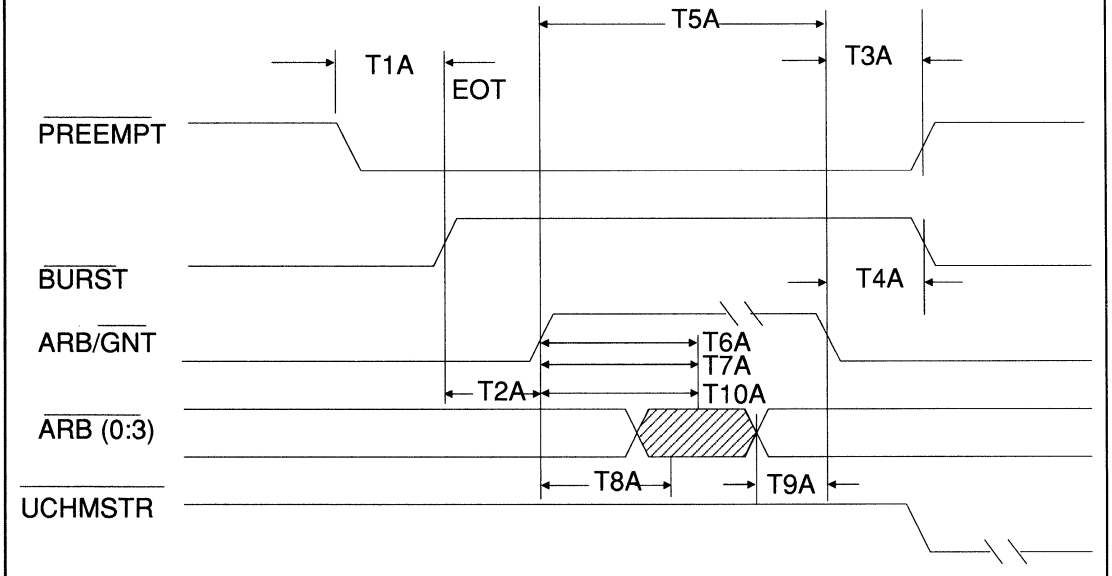


FIGURE 25. ARBITRATION TIMING

Parameter	Description	16 MHz		20 MHz		25 MHz		33 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
T1B	FDDRQ on to $\overline{\text{PREEMPT}}$ on	25	-	20	-	15.6	-	12	-
T2B	ARB/$\overline{\text{GNT}}$ high to $\overline{\text{DACK}}$ off	0	-	0	-	0	-	0	-
T3B	ARB/$\overline{\text{GNT}}$ high to HOLD on	0	-	0	-	0	-	0	-
T4B	ARB/$\overline{\text{GNT}}$ high to HOLD off	0	-	0	-	0	-	0	-
T5B	HLDA to ARB/$\overline{\text{GNT}}$ low	25	-	20	-	15.6	-	12	-

TABLE 9. FLOPPY REQUEST CYCLES (ns)

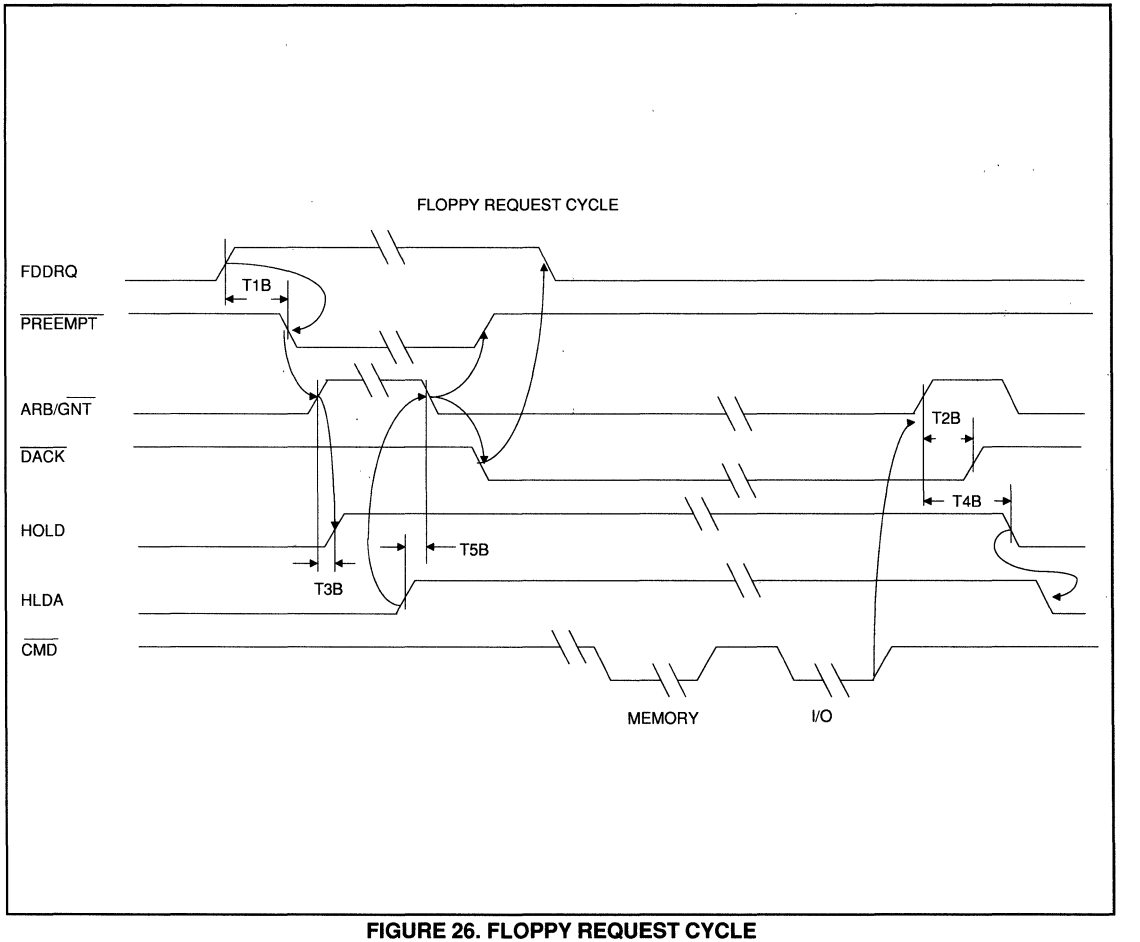


FIGURE 26. FLOPPY REQUEST CYCLE

Parameter	Description	33 M Hz		16 M Hz		20 MHz		25 MHz		Notes
Operating Frequency		8	33	4	16	4	20	4	25	MHz
CLOCKS										
T1C	CLK2 Period	15	62.5	31.25	125	25	125	20	125	@ 2V
T2AC	CLK2 High Time	4.25	-	5	-	5	-	4.5	-	@(V_{DD}-0.8V)
T2BC	CLK2 High Time	6.25	-	9	-	8	-	7	-	@ 2V
T3AC	CLK2 Low Time	4.25	-	7	-	6	-	4.5	-	@ 0.8V
T3BC	CLK2 Low Time	6.25	-	9	-	8	-	7	-	@ 2V
T4C	CLK Period	30	125	62.5	250	50	250	40	250	-
T5C	CLK High Time	8	-	20	-	14	-	10	-	-
T6C	CLK Low Time	8	-	15	-	12	-	10	-	-
T7C	CLK2387 Period	30	12.5	62.5	250	50	250	40	250	-
T8C	CLK2387 HighTime	8	-	-	-	-	-	10	-	-
T9C	CLK2387 Low Time	8	-	-	-	-	-	10	-	-
T10C	CLK387 Period	60	125	12.5	500	100	500	80	-	-
T11C	CLK387 High Time	12	-	-	-	-	-	17	-	-
T12C	CLK387 Low Time	12	-	-	-	-	-	17	-	-

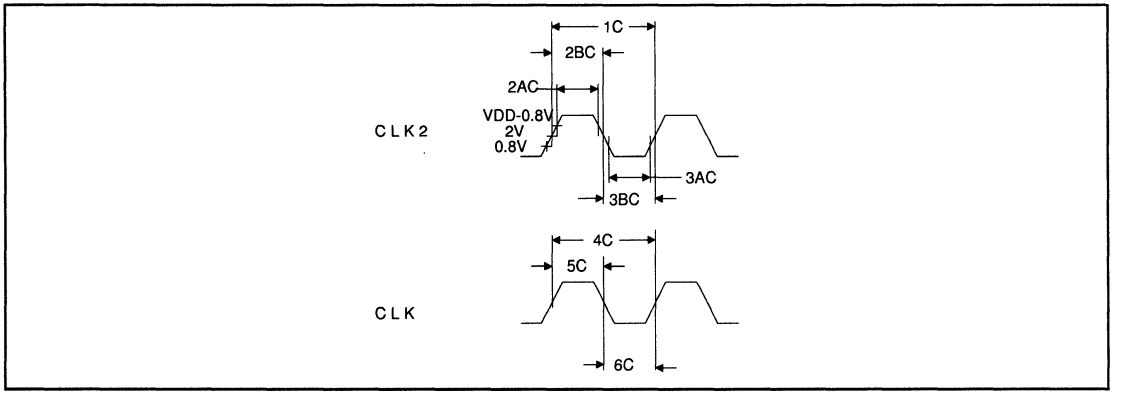


FIGURE 27. INPUT CLOCK TIMING SPECIFICATIONS

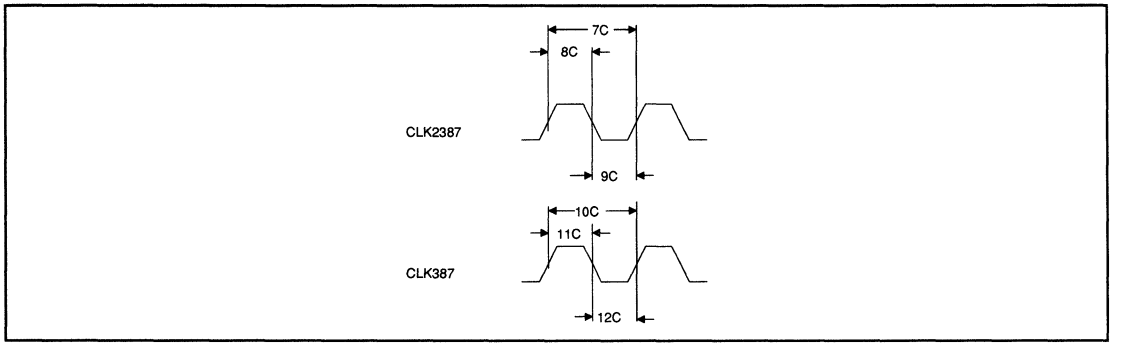


FIGURE 28. INPUT CLOCK SPECIFICATIONS II

DMA OPERATION - OUTPUTS										
Parameter	**Description**	**16 MHz**		**20 MHz**		**25 MHz**		**33 MHz**		**Notes**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
	PA (31:2), $\overline{BE}$ (3:0)									
T1D	VALID	2	38	2	32	2	24	2	15	
T2D	DISABLE	2	38	2	32	2	24	2	15	
	M/$\overline{IO}$, DC, WR, $\overline{ADS}$									
T3D	VALID	4	35	4	30	2	21	2	15	
T4D	DISABLE	4	35	4	30	4	21	2	15	
	REGISTER READ									
T5D	PD (31:0) VALID	2	75	2	75	2	75	2	75	
T6D	PD (31:0) DISABLE	2	75	2	75	2	75	2	75	
	DMA WRITE									
T7D	PD (31:0) VALID	2	50	2	40	2	27	2	24	
T8D	PD (31:0) DISABLE	2	35	2	27	2	22	2	17	
	HOLD									
T9D	VALID	4	35	4	30	4	24	2	19	
T10D	DISABLE	4	35	4	30	4	24	2	19	
	TC									
T11D	VALID	4	25	4	25	4	25	4	25	
T12D	DISABLE	4	25	4	25	4	25	4	25	

NOTE:
1. LOADING CAPACITANCE = 120 Pf for16 and 20 MHz, 50 Pf for 25 and 33 MHz.
2. LOADING CAPACITANCE = 75 Pf for 16 and 20 MHz, 50 Pf for 25 and 33 MHz.

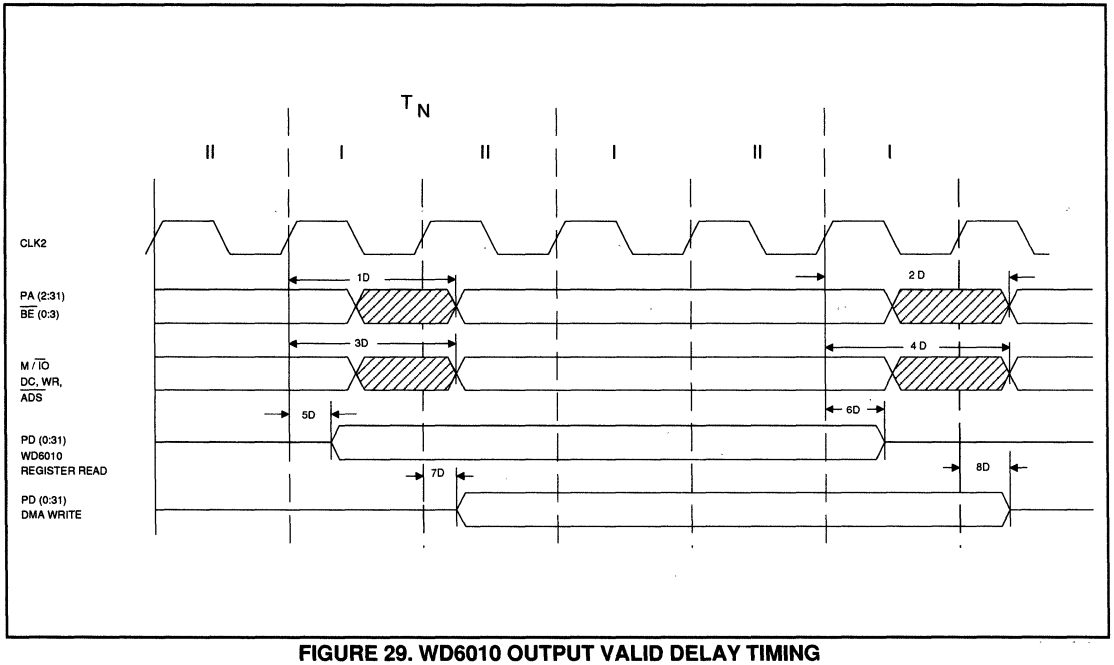


FIGURE 29. WD6010 OUTPUT VALID DELAY TIMING

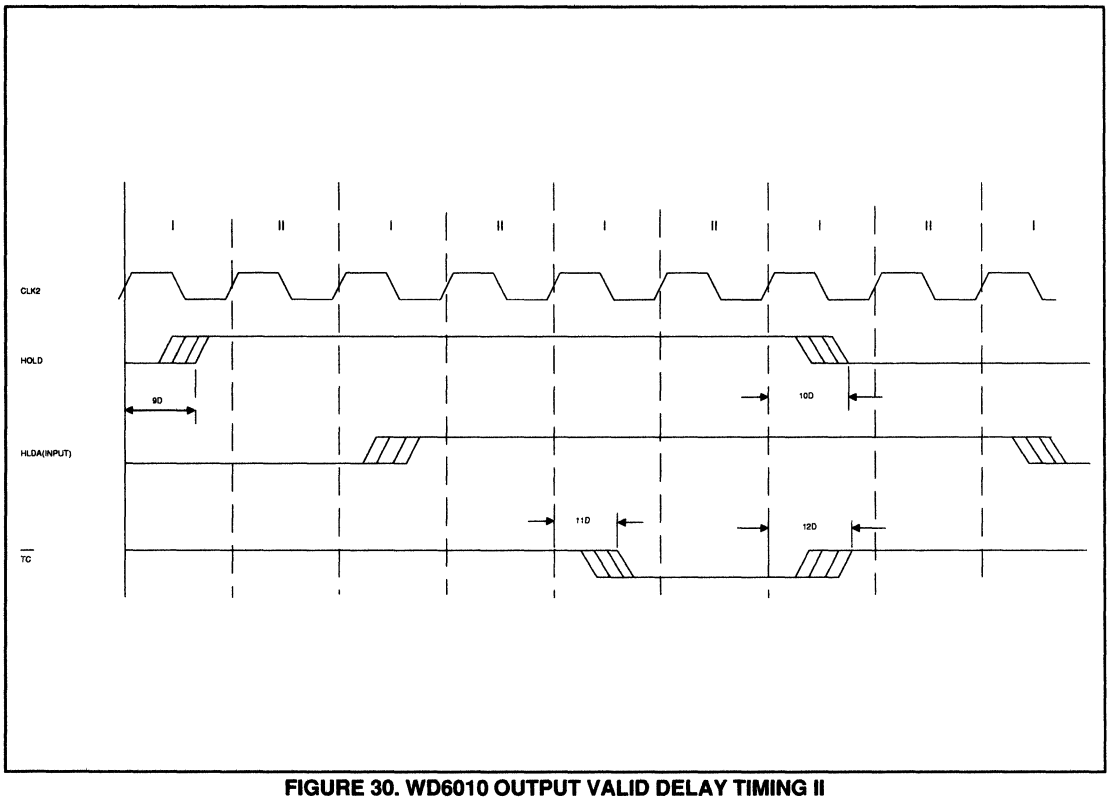


FIGURE 30. WD6010 OUTPUT VALID DELAY TIMING II

DMA OPERATION - INPUTS										
Parameter	**Description**	**16 MHz**		**20 MHz**		**25 MHz**		**33 MHz**		**Notes**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
	RDY									
T13D	SETUP TIME	20	-	11	-	10.5	-	7.5	-	
T14D	HOLD TIME	3	-	3	-	3	-	3	-	
	HLDA									
T15D	SETUP TIME	25	-	18	-	16	-	10	-	
T16D	HOLD TIME	3	-	3	-	3	-	3	-	
	PA (2:31), $\overline{BE}$(0:3)									
T17D	SETUP TIME	22	-	20	-	16	-	15	-	
T18D	HOLD TIME	2	-	2	-	2	-	2	-	
	M/$\overline{IO}$, DC, WR, $\overline{ADS}$,									
T19D	SETUP TIME	22	-	20	-	16	-	15	-	
T20D	HOLD TIME	2	-	2	-	2	-	2	-	
	REGISTER WRITE									
T21D	PD (0:31) SETUP TIME	75	-	75	-	75	-	7.5	-	
T22D	PD (0:31)HOLD TIME	15	-	15	-	15	-	15	-	
	DMA READ									
T23D	PD (0:31) SETUP TIME	10	-	10	-	10	-	10	-	
T24D	PD (0:31)HOLD TIME	5	-	5	-	5	-	5	-	
	NA, $\overline{BS16}$									
T25D	SETUP TIME	20	-	20	-	20	-	15	-	
T26D	HOLD TIME	5	-	5	-	5	-	5	-	
	$\overline{NMI}$, INTR									
T27D	SETUP TIME	15	-	15	-	15	-	15	-	
T28D	HOLD TIME	5	-	5	-	5	-	5	-	

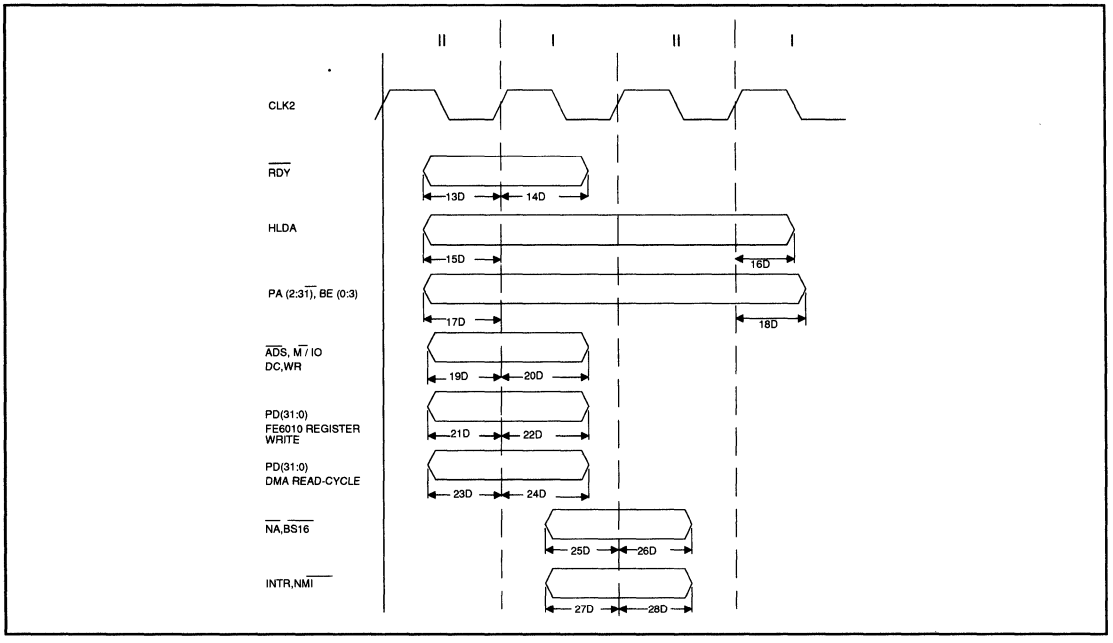


FIGURE 31. INPUT SETUP AND HOLD TIMINGS

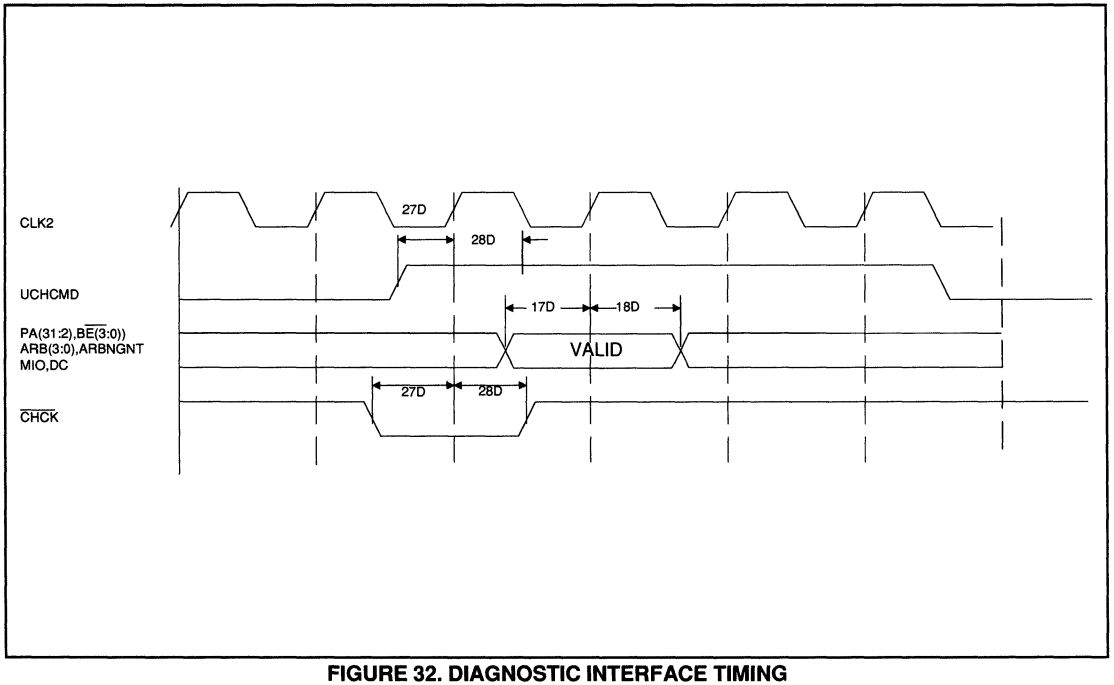


FIGURE 32. DIAGNOSTIC INTERFACE TIMING

12

80387 HALF-SPEED INTERFACE									
Parameter	Description	16 MHz		20 MHz		25 MHz		33 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
T1H	ADSO	6	34	6	28	3	24	-	21
	Valid from CLK2387								
T2H	Setup Time to CLK2387 RDY0 rising edge	20	-	11	-	9	-	-	7
T3H	Hold Time from CLK2387 RDY0 rising edge	4	-	4	-	3	-	-	3
T4H	Valid from CLK2387	2	25	2	25	2	19	2	15
	NRDY0387								
DEVICE ENABLE TIMINGS									
T1E	CDSETEN, VGAEN, EDRENA Valid from CLK2387	-	20	-	20	-	20	-	20

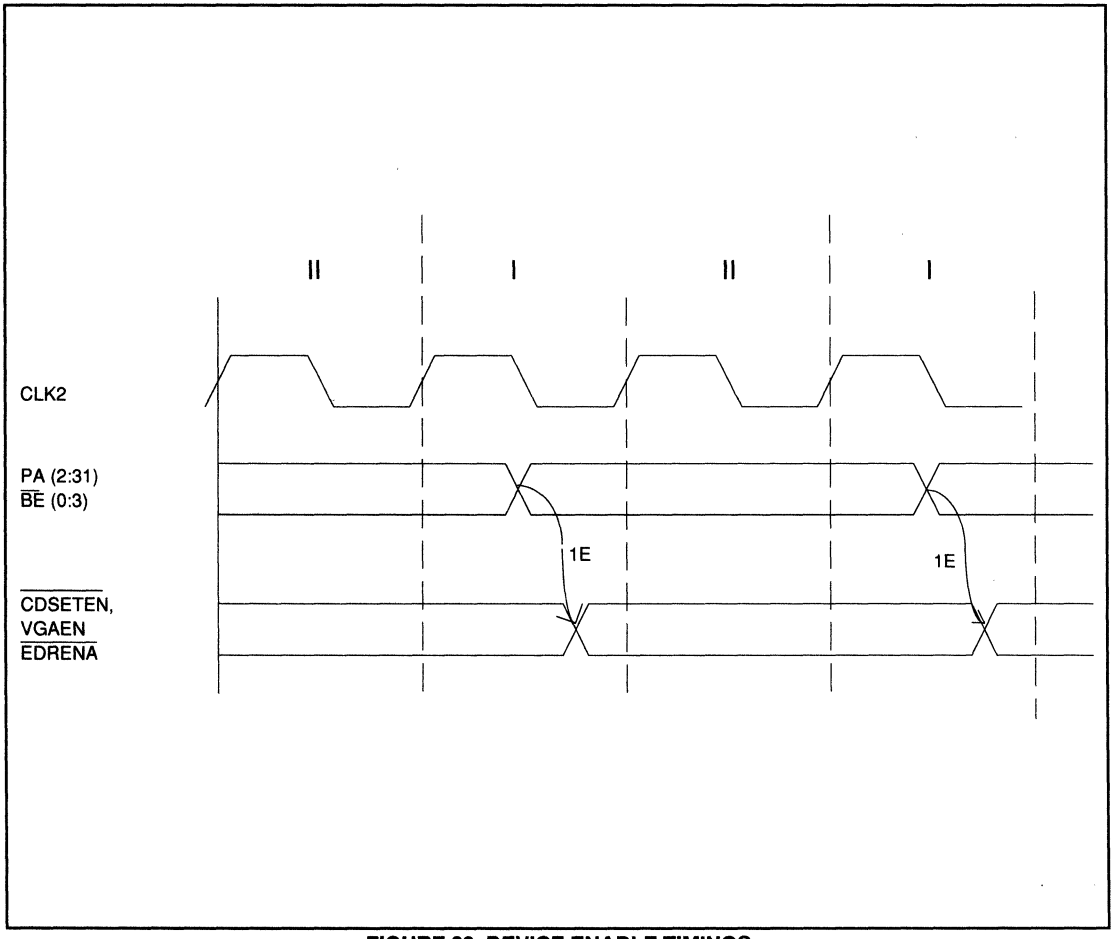


FIGURE 33. DEVICE ENABLE TIMINGS

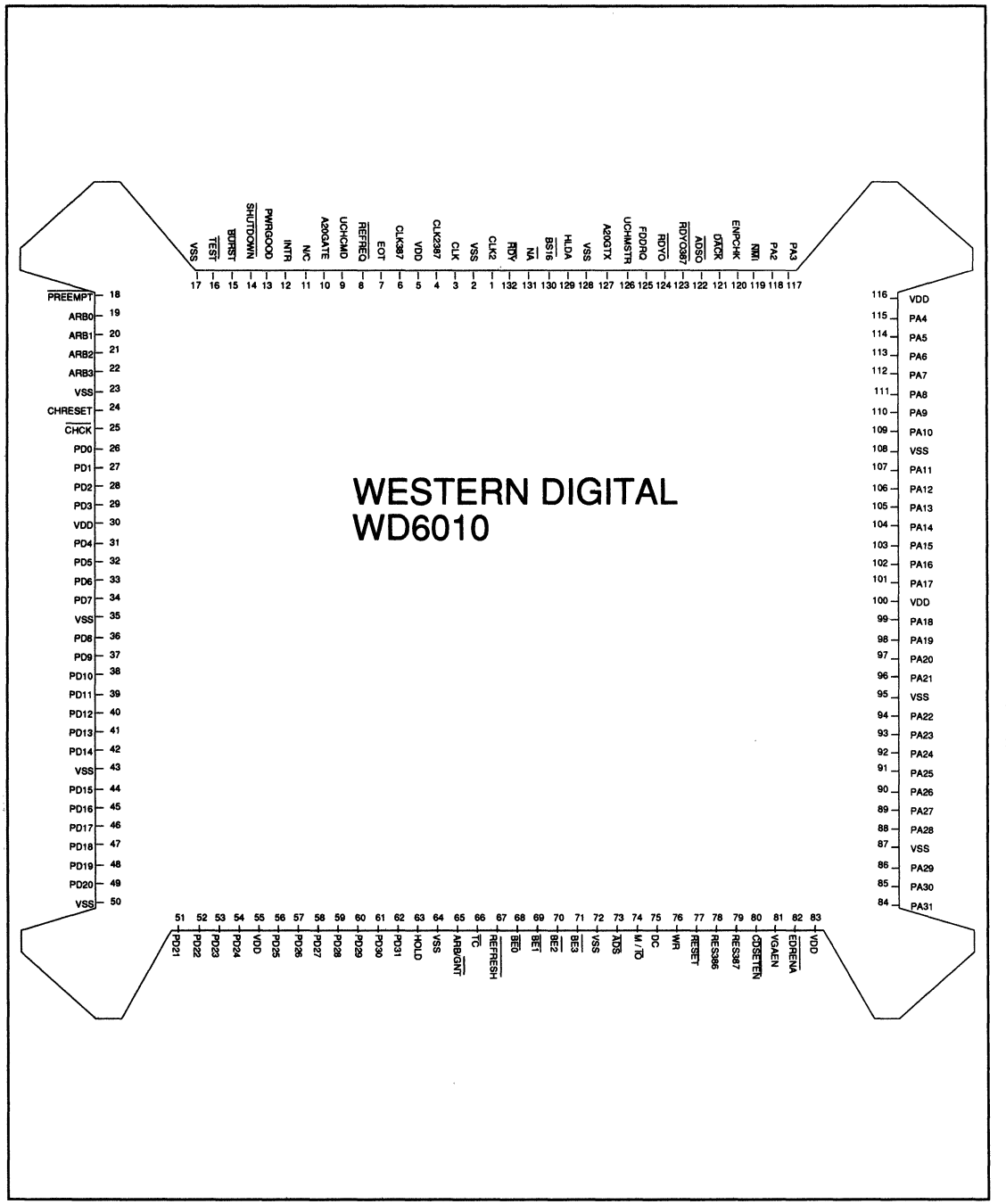


FIGURE 34. PIN LAYOUT DIAGRAM-TOP VIEW

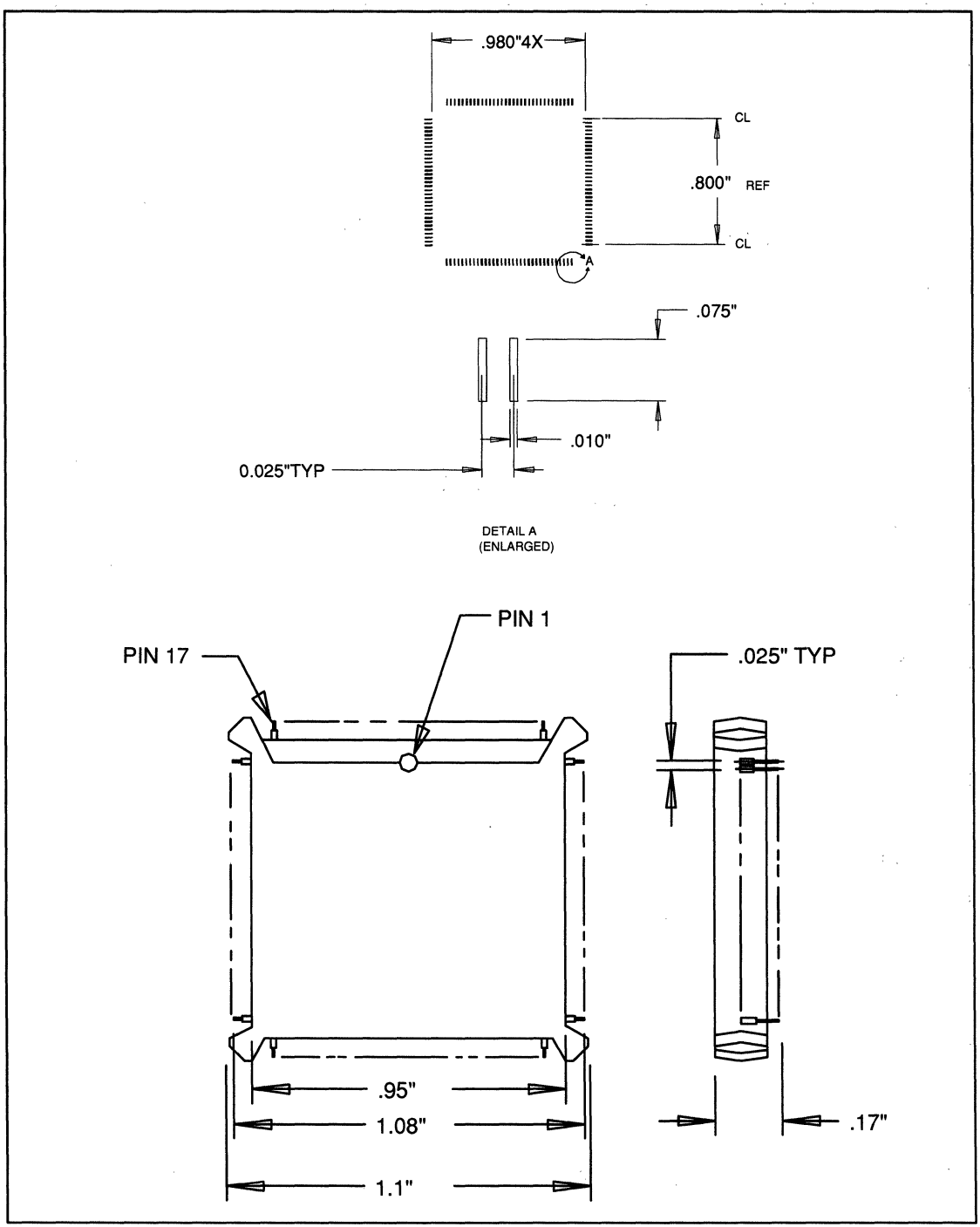
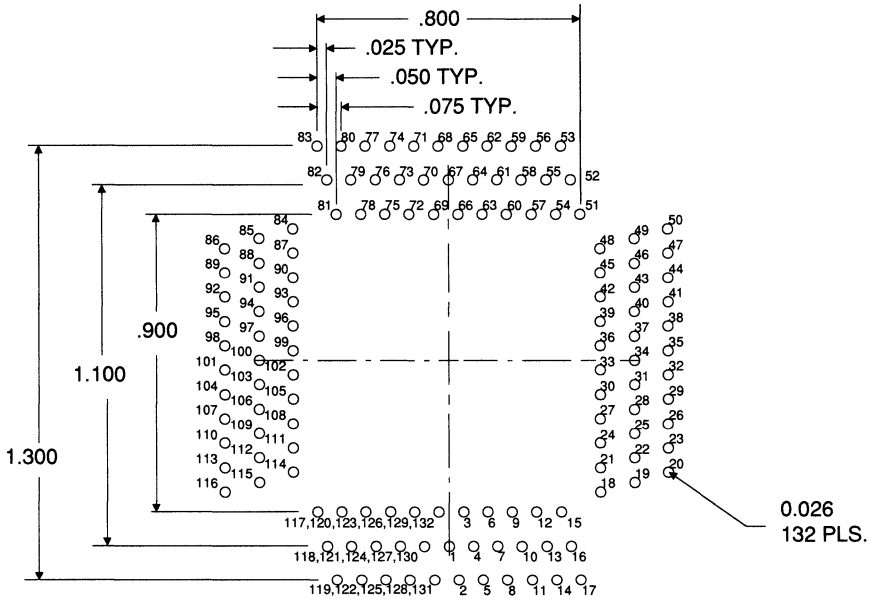


FIGURE 35. 132-PIN JEDEC FLAT PACK PACKAGE DIAGRAM



RECOMMENDED P.C. BOARD HOLE PATTERN
SOCKET SIDE
132 POSN

Amp Incorporated
Harrisburg PA
Part No. 821932-5

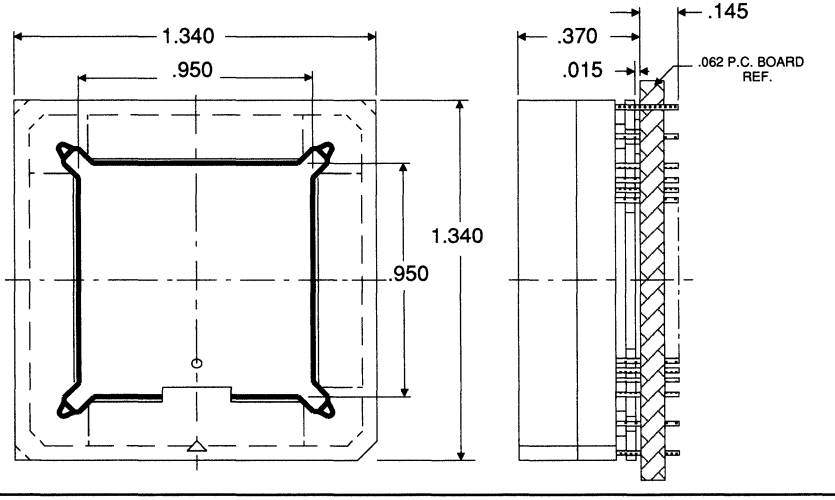


FIGURE 36. SOCKET DIAGRAM

SYSTEMS LOGIC/PERIPHERAL

WD6020

Address and Data Buffer Device

13

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

1.1 DESCRIPTION

As part of the Western Digital WD6400SX or WD6400SX/LP Chip Set, the WD6020 Address and Data Buffer Device significantly facilitates the design and implementation of an 80386SX based IBM PS/2 compatible system boards. By combining functionality normally implemented in 10 discrete components, the WD6020 decreases design complexity, saves space, reduces system cost, and increases system reliability. Figure 1-1 shows a typical system diagram using the WD6400 Chip Set.

1.2 FEATURES

- Provides Address and Data Buffers that Interface to the Micro Channel
- Meets Micro Channel AC/DC Specifications
- Contains Peripheral Bus Address and Data Buffers
- Runs in Systems with Clock Speeds to 25 MHz
- 24 Milliamp Output Drive Capability
- Low Power 1.25 Micron CMOS Technology
- Surface Mountable 132 Lead JEDEC Plastic Quad Flat Pack

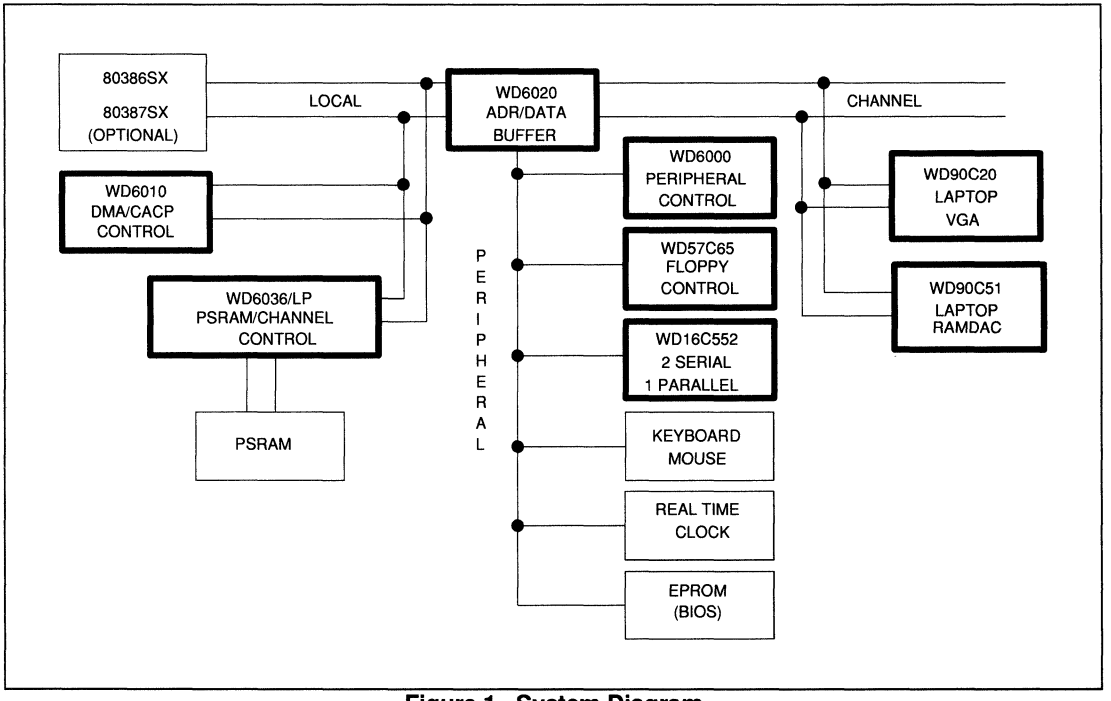
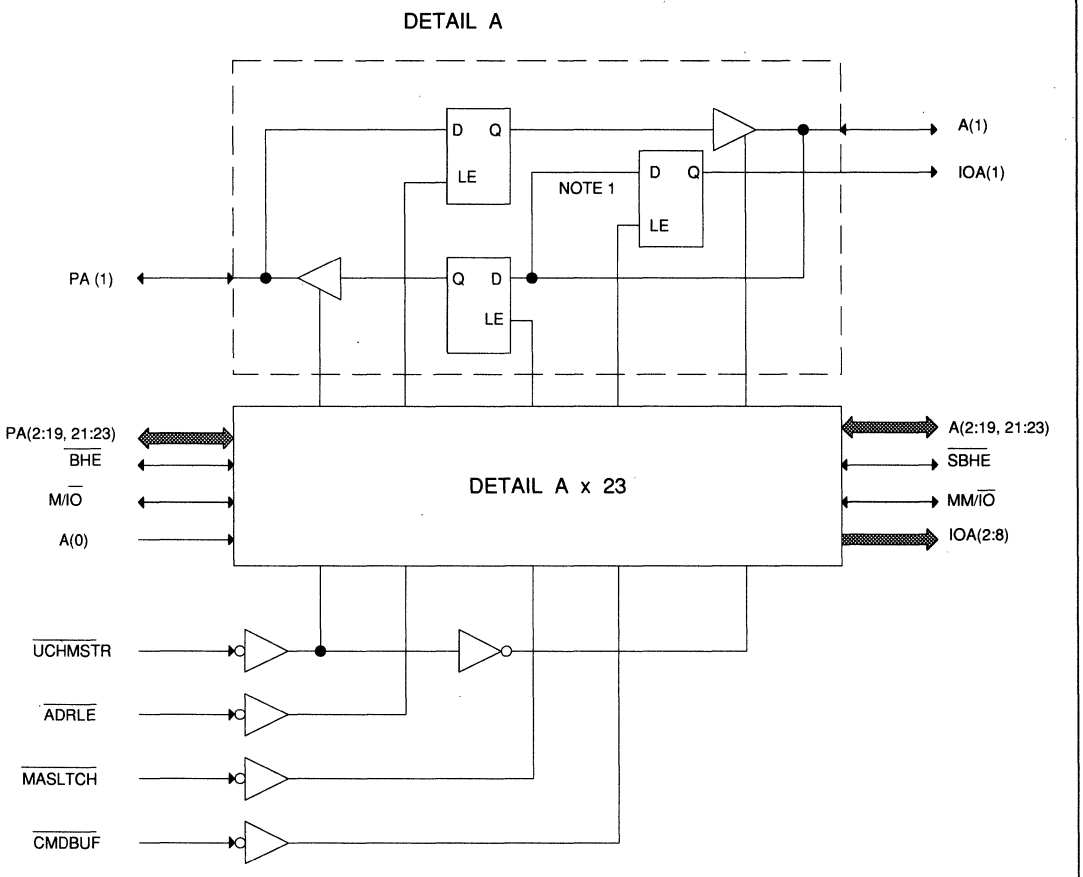


Figure 1. System Diagram

13



NOTES:

[1] This latch exists only 9 times. IOA0 latch is driven by separate MA0 input.

Figure 2. WD6020 Address Buffer Block Diagram

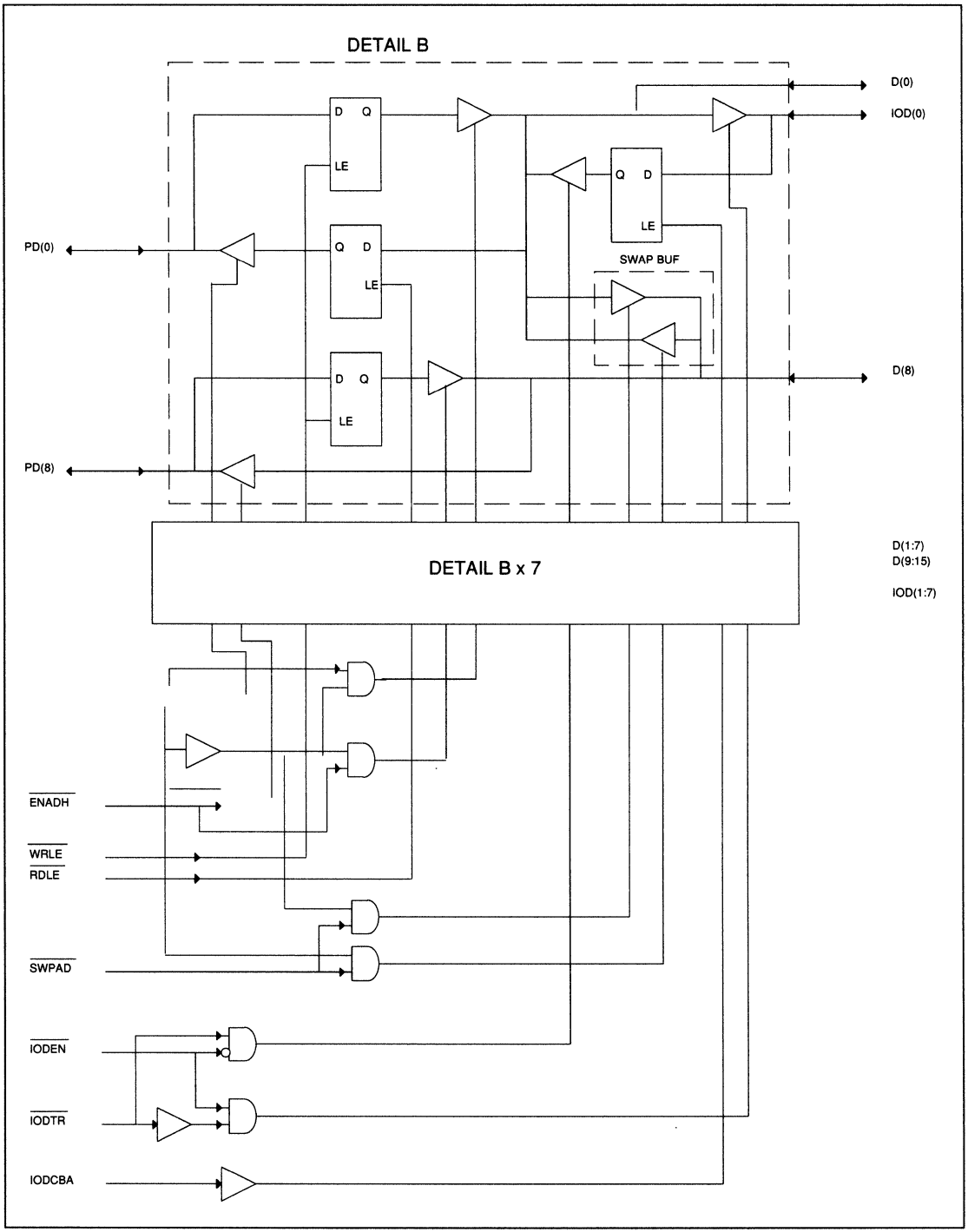
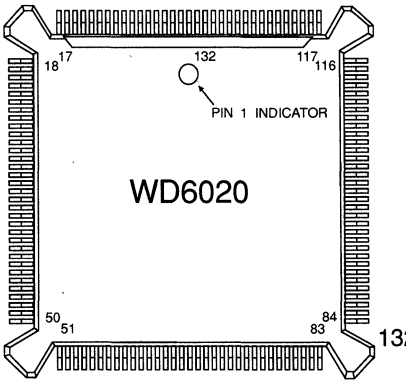


Figure 3. WD6020 Data Buffer Block Diagram



132 Pin JEDEC Flat Pack

Figure 4. Pin Diagram

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	A12	34	PA16	67	D6	100	IOD7
2	A11	35	PA17	68	V_{SS}	101	IOD6
3	A10	36	PA18	69	D7	102	IOD5
4	V_{SS}	37	PA19	70	D8	103	IOD4
5	A9	38	PA21	71	D9	104	IOD3
6	A8	39	PA22	72	V_{SS}	105	IOD2
7	A7	40	PA23	73	D10	106	IOD1
8	V_{SS}	41	V_{SS}	74	D11	107	IOD0
9	A6	42	ENADL	75	D12	108	V_{SS}
10	A5	43	IODTR	76	V_{SS}	109	M/IO
11	A4	44	WRLE	77	D13	110	BHE
12	V_{SS}	45	ADRLE	78	D14	111	IOA8
13	A3	46	MASLTCH	79	D15	112	IOA7
14	A2	47	RDLE	80	BIAS	113	IOA6
15	A1	48	IODCBA	81	V_{DD}	114	IOA5
16	V_{DD}	49	CMDBUF	82	PD0	115	IOA4
17	PA1	50	UCHMSTR	83	PD1	116	IOA3
18	PA2	51	A0	84	PD2	117	IOA2
19	PA3	52	IODEN	85	PD3	118	IOA1
20	PA4	53	ENADH	86	PD4	119	IOA0
21	PA5	54	DTRAD	87	PD5	120	A23
22	PA6	55	SWPAD	88	PD6	121	A22
23	PA7	56	V_{DD}	89	PD7	122	A21
24	V_{DD}	57	MM/IO	90	PD8	123	V_{SS}
25	PA8	58	SBHE	91	PD9	124	A19
26	PA9	59	D0	92	PD10	125	A18
27	PA10	60	V_{SS}	93	V_{SS}	126	A17
28	PA11	61	D1	94	PD11	127	A16
29	V_{SS}	62	D2	95	PD12	128	V_{SS}
30	PA12	63	D3	96	PD13	129	A15
31	PA13	64	V_{SS}	97	PD14	130	A14
32	PA14	65	D4	98	PD15	131	A13
33	PA15	66	D5	99	V_{DD}	132	V_{SS}

Table 1. WD6020 Pin Assignments

2.0 PIN DESCRIPTIONS

PIN NO.	NAME	TYPE	FUNCTION
			ADDRESS BUS LATCHES
17 18 19 20 21 22 23 25 26 27 28 30 31 32 33 34 35 36 37 38 29 40	PA1 PA2 PA3 PA4 PA5 PA6 PA7 PA8 PA9 PA10 PA11 PA12 PA13 PA14 PA15 PA16 PA17 PA18 PA19 PA21 PA22 PA23	I/O	PROCESSOR ADDRESS BUS Bi-directional address bus connected to the 80386SX and the WD6010. A0 and A20 come directly from the WD6010.
51 15 14 13 11 10 9 7 6 5 3 2 1 131 130 129 127 126 125 124 122 121 120	A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A21 A22 A23	I/O	CHANNEL ADDRESS BUS Bi-directional Channel address bus.

Table 2. Pin Descriptions

O = Output, I = Input, I/O = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
110	$\overline{BHE}$	I/O	$\overline{BYTE\ HIGH\ ENABLE}$ This signal is connected to the WD6010 and CPU and indicates whether a high byte is being transferred during the current cycle.
109	M/$\overline{IO}$	I/O	MEMORY $\overline{INPUT/OUTPUT}$ This signal is connected to the WD6010 and CPU and is used to encode the local bus cycle type information.
58	$\overline{SBHE}$	I/O	$\overline{SYSTEM\ BYTE\ HIGH\ ENABLE}$ This signal is connected to the Channel and indicates whether a high byte is being transferred during the current cycle.
57	MM/$\overline{IO}$	I/O	CHANNEL MEMORY $\overline{INPUT/OUTPUT}$ This signal and CHS(0:1) from the WD6010 encode the Channel bus cycle type information.
50	$\overline{UCHMSTR}$	I	$\overline{CHANNEL\ MASTER}$ This signal determines the direction of the address.
49	$\overline{CMDBUF}$	I	$\overline{BUFFERED\ CHANNEL\ COMMAND}$ This signal latches the address for the local bus.
46	$\overline{MASLTCH}$	I	$\overline{MASTER\ LATCH}$ This signal latches the address from the Channel.
45	$\overline{ADRLE}$	I	$\overline{ADDRESS\ LATCH\ ENABLE}$ This signal latches the address to the Channel.
119 118 117 116 115 114 113 112 111	IOA0 IOA1 IOA2 IOA3 IOA4 IOA5 IOA6 IOA7 IOA8	O	I/O ADDRESS BUS These signals are the address bus to the on-board peripherals.
			DATA BUS LATCHES
82 83 84 85 86 87 88 89 90 91 92	PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7 PD8 PD9 PD10	I/O	PROCESSOR DATA BUS Bi-directional data bus connected to the CPU and the WD6010.

Table 2. Pin Descriptions (Contd)

O = Output, I = Input, I/O = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
94 95 96 97 98	PD11 PD12 PD13 PD14 PD15	I/O	PROCESSOR DATA BUS (contd) Bi-directional data bus connected to the CPU and the WD6010.
59 61 62 63 65 66 67 69 70 71 73 74 75 77 78 79	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	I/O	CHANNEL DATA BUS Bi-directional Channel data bus.
107 106 105 104 103 102 101 100	IOD0 IOD1 IOD2 IOD3 IOD4 IOD5 IOD6 IOD7	I/O	I/O DATA BUS These signals are the peripheral data bus.
55	$\overline{\text{SWPAD}}$	I	$\overline{\text{ENABLE SWAP ADDRESS}}$ This signal enables a byte swap on the Channel.
54	$\overline{\text{DTRAD}}$	I	$\overline{\text{DATA TRANSFER DIRECTION}}$ This signal indicates the direction of the data transfer on the Channel. When asserted low, Channel to CPU is enabled.
53	$\overline{\text{ENADH}}$	I	$\overline{\text{ENABLE DATA HIGH}}$ This signal enables the high byte from the Channel.
52	$\overline{\text{IODEN}}$	I	$\overline{\text{I/O DATA ENABLE}}$ This signal enables the local data bus.
48	IODCBA	I	I/O DATA CLOCK This signal latches the data from the peripheral bus.
47	$\overline{\text{RDLE}}$	I	$\overline{\text{READ LATCH ENABLE}}$ This signal latches Channel low read data.
44	$\overline{\text{WRLE}}$		$\overline{\text{WRITE LATCH ENABLE}}$ This signal latches write data to the Channel.

Table 2. Pin Descriptions (Contd)

13

O = Output, I = Input, I/O = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
43	$\overline{\text{IODTR}}$	I	I/O DATA TRANSMIT/RECEIVE This signal indicates the direction of the local data bus.
42	$\overline{\text{ENADL}}$	I	ENABLE DATA LOW This signal enables the low byte from the Channel.
			MISCELLANEOUS
80	$\overline{\text{BIAS}}$	I	$\overline{\text{BIAS}}$ This pin provides a bias for internal current drivers. It should be connected through a 1% 1.25K Ohm resistor to ground externally.
16,24,56, 81,99	V_{DD}	I	+5V Power Supply
4,8,12, 29,41,60, 64,68,72, 76,93,108, 123,128, 132	V_{SS}	I	0V Ground

Table 2. Pin Descriptions (Contd)

O = Output, I = Input, I/O = Bidirectional

3.0 TECHNICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS

These are absolute maximum stress ratings for the device. Permanent device damage can result from exposing the device to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	(V_{DD}–V_{SS})	0	7	V
Input Voltage	V_{IABS}	V_{SS}–0.3	V_{DD}+0.3	V
Bias on Output Pin	V_{OABS}	VSS–0.3	V_{DD}+0.3	V
Storage Temperature	T_S	–40	125	°C

3.2 NORMAL OPERATING CONDITIONS

Exposure of the device to conditions exceeding the normal operating conditions for extended periods of time can affect the long term reliability of the device.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	–0.3	VDD+0.3	V
Power Dissipation	P_W	—	TBD	mW
Supply Current	I_{DD}	—	TBD	mA

3.3 DC CHARACTERISTICS (UNDER NORMAL OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	MAX	UNITS
*Input Capacitance @ f_C= 1 MHz	C_I	—	10	pF
I/O Capacitance	C_{IO}	—	15	pF
*Logic High Input Voltage	V_{IH}	2.0	—	V
*Logic Low Input Voltage	V_{IL}	—	0.8	V
*Input Leakage	I_{IL}	—	±10	uA
Tri-state Output Leakage	I_{OL}	—	±30	uA
I/O Pin Leakage	I_{IOL}	—	±40	uA
OUTPUTS A [23:21], A [19:1], D [15:0], MM/$\overline{IO}$, $\overline{SBHE}$				
Source Current @ V_{OH}= 2.4 V	I_{OH}	4	—	mA
Sink Current @ V_{OL}= 0.4 V	I_{OL}	24	—	mA
ALL OTHER OUTPUTS				
Source Current @ V_{OH}= 2.4 V	I_{OH}	1	—	mA
Sink Current @ V_{OL}= 0.4 V	I_{OL}	4	—	mA

Note: The input pin "BIAS" is connected externally to ground through a 1% 1.25K Ohm resistance and is part of an internal biasing circuit. Capacitance, leakage, and threshold measurements on this pin do not apply.

4.0 TIMING

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	PA(21:23,1:19) delay to A(21:23,1:19)	0	25	1
T2	PA(21:23,1:19) delay to A(21:23,1:19)	0	25	1
T3	PA(1:8) delay to IOA(1:8)	0	50	1
T4	PA(1:8) delay to IOA(1:8)	0	50	1
T5	A(0) delay to IOA(0)	0	25	2
T6	A(0) delay to IOA(0)	0	25	2
T7	$\overline{BHE}$, M/$\overline{IO}$ delay to $\overline{SBHE}$, MM/$\overline{IO}$	0	25	1
T8	$\overline{BHE}$, M/$\overline{IO}$ delay to $\overline{SBHE}$, MM/$\overline{IO}$	0	25	1
T9	$\overline{UCHMSTR}$ on to A(21:23,1:19) tristate	0	15	1
T10	$\overline{UCHMSTR}$ off to PA(21:23,1:19) tristate	0	15	1
T11	$\overline{UCHMSTR}$ on to $\overline{SBHE}$, MM/$\overline{IO}$ tristate	0	15	1
T12	$\overline{UCHMSTR}$ off to $\overline{BHE}$, M/$\overline{IO}$ tristate	0	15	1
T13	PA(21:23,1:19), $\overline{BHE}$, M/$\overline{IO}$ setup to $\overline{ADRLE}$ on	10	—	1
T14	PA(21:23,1:19), $\overline{BHE}$, M/$\overline{IO}$ hold after $\overline{ADRLE}$ on	5	—	1
T15	PA(21:23,1:19), $\overline{BHE}$, M/$\overline{IO}$ setup to $\overline{CMDBUF}$ on	10	—	—
T16	PA(21:23,1:19), $\overline{BHE}$, M/$\overline{IO}$ hold after $\overline{CMDBUF}$ on	5	—	—
T17	A(21:23,1:19), $\overline{SBHE}$, MM/$\overline{IO}$ setup to $\overline{CMDBUF}$ on	10	—	2
T18	A(21:23,1:19), $\overline{SBHE}$, MM/$\overline{IO}$ hold after $\overline{CMDBUF}$ on	5	—	2
T19	A(21:23,1:19), $\overline{SBHE}$, MM/$\overline{IO}$ setup to $\overline{MASLTCH}$ on	10	—	1
T20	A(21:23,1:19), $\overline{SBHE}$, MM/$\overline{IO}$ hold after $\overline{MASLTCH}$ on	5	—	1
T21	A(21:23,1:19) delay to PA(23:21,1:19)	0	25	1
T22	A(21:23,1:19) delay to PA(23:21,1:19)	0	25	1
T23	$\overline{SBHE}$, MM/$\overline{IO}$ delay to $\overline{BHE}$, M/$\overline{IO}$	0	25	1
T24	$\overline{SBHE}$, MM/$\overline{IO}$ delay to $\overline{BHE}$, M/$\overline{IO}$	0	25	1

Table 3. Address Buffer Timing (in nsec)

Notes: 1. Refer to CPU/Channel Address Control Function Table for control states.
2. Refer to Channel/Peripheral Bus Address Control Function Table for control states.

		INPUT	OUTPUT
$\overline{\text{ADRLE}}$	$\overline{\text{UCHMSTR}}$	PA(1:23), M/$\overline{\text{IO}}$, $\overline{\text{BHE}}$	A(1:25), M/$\overline{\text{IO}}$, $\overline{\text{SBHE}}$
0	0	Storing	Tristate
0	1	Transparent	Current Inputs
1	0	Storing	Tristate
1	1	Storing	Previous Inputs
		INPUT	**OUTPUT**
$\overline{\text{MASLTCH}}$	$\overline{\text{UCHMSTR}}$	A(1:23), MM/$\overline{\text{IO}}$, $\overline{\text{SBHE}}$	PA(1:23), M/$\overline{\text{IO}}$, $\overline{\text{BHE}}$
0	0	Transparent	Current Inputs
0	1	Storing	Tristate
1	0	Storing	Previous Inputs
1	1	Storing	Tristate

Table 4. CPU/Channel Address Control Functions

	INPUT	OUTPUT
$\overline{\text{CMDBUF}}$	A(0:23)	IOA(0:8)
0	X	Previous A(0:23)
1	—	A(0:23)

Table 5. Channel/Peripheral Bus Address Control Functions

13

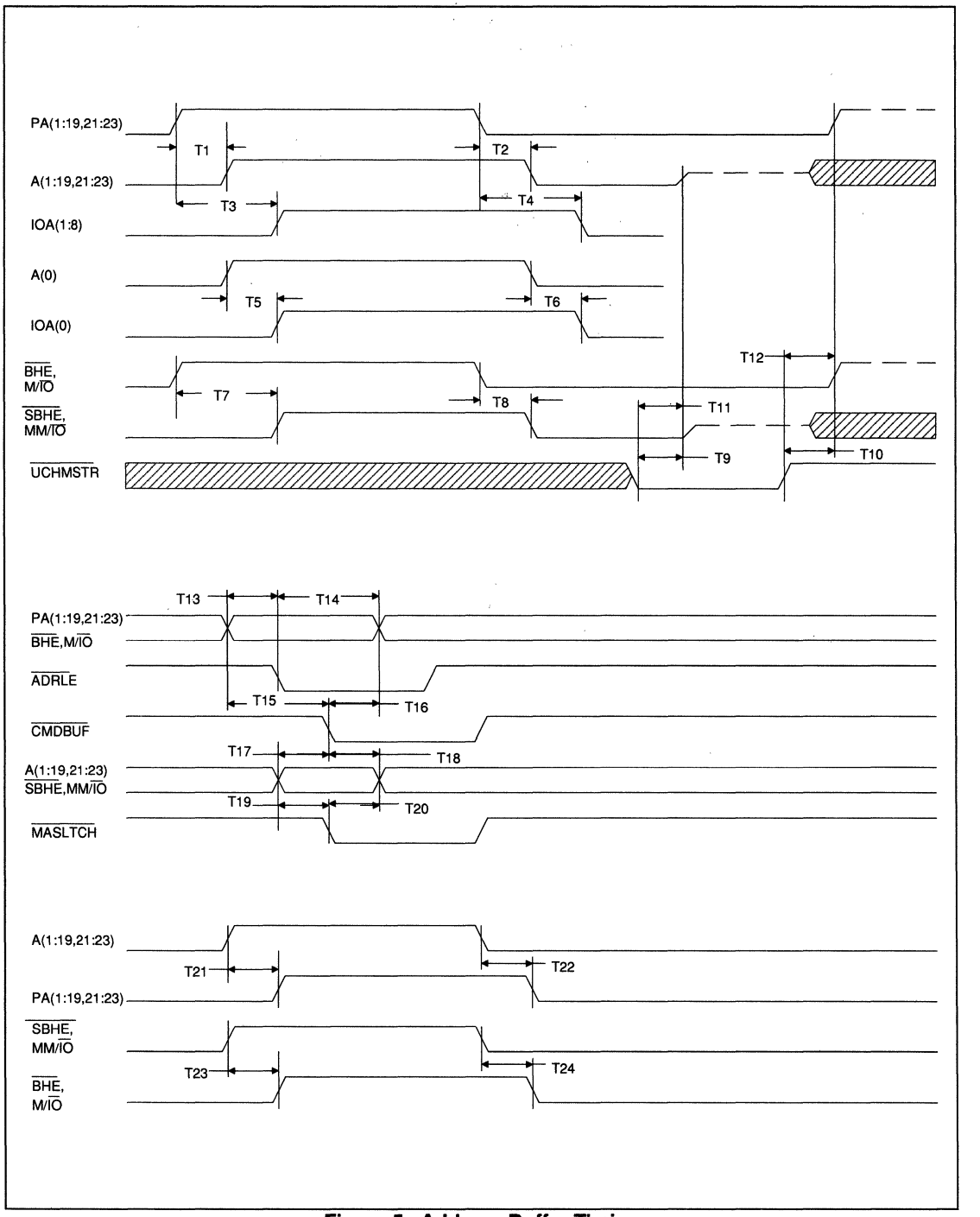


Figure 5. Address Buffer Timing

PARAM	DESCRIPTION	MIN	MAX	NOTE
T1	PD(0:15) delay to D(0:15)	0	25	1
T2	PD(0:15) delay to D(0:15)	0	25	1
T3	PD(0:7) delay to IOD(0:7)	0	50	—
T4	PD(0:7) delay to IOD(0:7)	0	50	—
T5	PD(8:15) delay to D(0:7)	0	25	1
T6	PD(8:15) delay to D(0:7)	0	25	1
T7	PD(8:15) delay to IOD(0:7)	0	50	—
T8	PD(8:15) delay to IOD(0:7)	0	50	—
T9	D(0:15) delay to PD(0:15)	0	25	1
T10	D(0:15) delay to PD(0:15)	0	25	1
T11	IOD(0:7) delay to PD(0:7)	0	50	—
T12	IOD(0:7) delay to PD(0:7)	0	50	—
T13	D(0:7) delay to PD(8:15)	0	25	1
T14	D(0:7) delay to PD(8:15)	0	25	1
T15	IOD(0:7) delay to PD(8:15)	0	25	—
T16	IOD(0:7) delay to PD(8:15)	0	25	—
T17	PD(0:15) setup to $\overline{\text{WRLE}}$ high	10	—	1
T18	PD(0:15) hold after $\overline{\text{WRLE}}$ high	5	—	1
T19	D(0:7) setup to $\overline{\text{RDLE}}$ high	10	—	1
T20	D(0:7) hold after $\overline{\text{RDLE}}$ high	5	—	1
T21	IOD(0:7) setup to $\overline{\text{RDLE}}$ high	10	—	—
T22	IOD(0:7) hold after $\overline{\text{RDLE}}$ high	5	—	—
T23	IOD(0:7) setup to IODCBA low	10	—	2
T24	IOD(0:7) hold after IODCBA low	5	—	2
T25	PD(0:7) tristate from $\overline{\text{ENADL}}$ or $\overline{\text{DTRAD}}$	0	15	1
T26	PD(8:15) tristate from $\overline{\text{ENADH}}$ or $\overline{\text{DTRAD}}$ high	0	15	1
T27	D(0:7) tristate from $\overline{\text{ENADL}}$ high	0	15	1
T28	PD(8:15) tristate from $\overline{\text{ENADH}}$ high	0	15	1
T29	D(0:15) tristate from $\overline{\text{DTRAD}}$ high	0	15	1
T30	IOD(0:7) tristate from $\overline{\text{IODDEN}}$ high	0	15	2
T31	IOD(0:7) tristate from $\overline{\text{IODTR}}$ low	0	15	2
T32	D(0:7) tristate from $\overline{\text{SWPAD}}$ or $\overline{\text{DTRAD}}$ high	0	15	1
T33	D(8:15) tristate from $\overline{\text{DTRAD}}$ low	0	15	1
T34	D(8:15) tristate from $\overline{\text{SWPAD}}$ high	0	15	1
T35	D(0:7) tristate from $\overline{\text{IODEN}}$ or $\overline{\text{IODTR}}$ high	0	15	2,3
T36	D(0:7) delay to IOD(0:7)	0	25	2
T37	D(0:7) delay to IOD(0:7)	0	25	2
T38	IOD(0:7) delay to D(0:7)	0	25	2
T39	IOD(0:7) delay to D(0:7)	0	25	2

Table 6. Data Buffer Timing (in nsec)

Notes: 1. Refer to CPU/Chhannel Data Control Function Table for control states.
2. Refer to Channel/Peripheral Bus Data Control Function Table for control status.
3. Data Sourced from IOD bus latch.

13

RDLTCH	WRLE	DTRAD	ENADL	ENADH	SWPAD	PD (8:15)	PD (0:7)	D (8:15)	D (0:7)
0	X	0	0	0	1	D(8:15)	D(0:7)	—	—
0	X	0	0	0	0	D(0:7)	D(0:7)	—	—
1	X	0	0	0	1	D(1:15)	Previous D(0:7)	—	—
1	X	0	1	1	1	Tristate	Tristate	—	—
X	0	1	0	0	1	—	—	PD(8:15)	PD(0:7)
X	0	1	0	0	0	—	—	PD(8:15)	PD(0:15)
X	1	1	0	0	1	—	—	Previous D(15:8)	Previous D(7:0)
X	1	1	1	1	1	—	—	Tristate	Tristate

Table 7. CPU/Channel Data Control Functions

IODTR	IODEN	IODCBA	D(0:7)	IOD(0:7)
0	0	0	IOD(0:7)	—
0	0	1	Previous IOD(0:7)	—
X	1	X	Tristate	—
1	0	X	—	D(0:7)
1	1	X	—	Tristate

Table 8. Channel/Peripheral Bus Data Control Functions

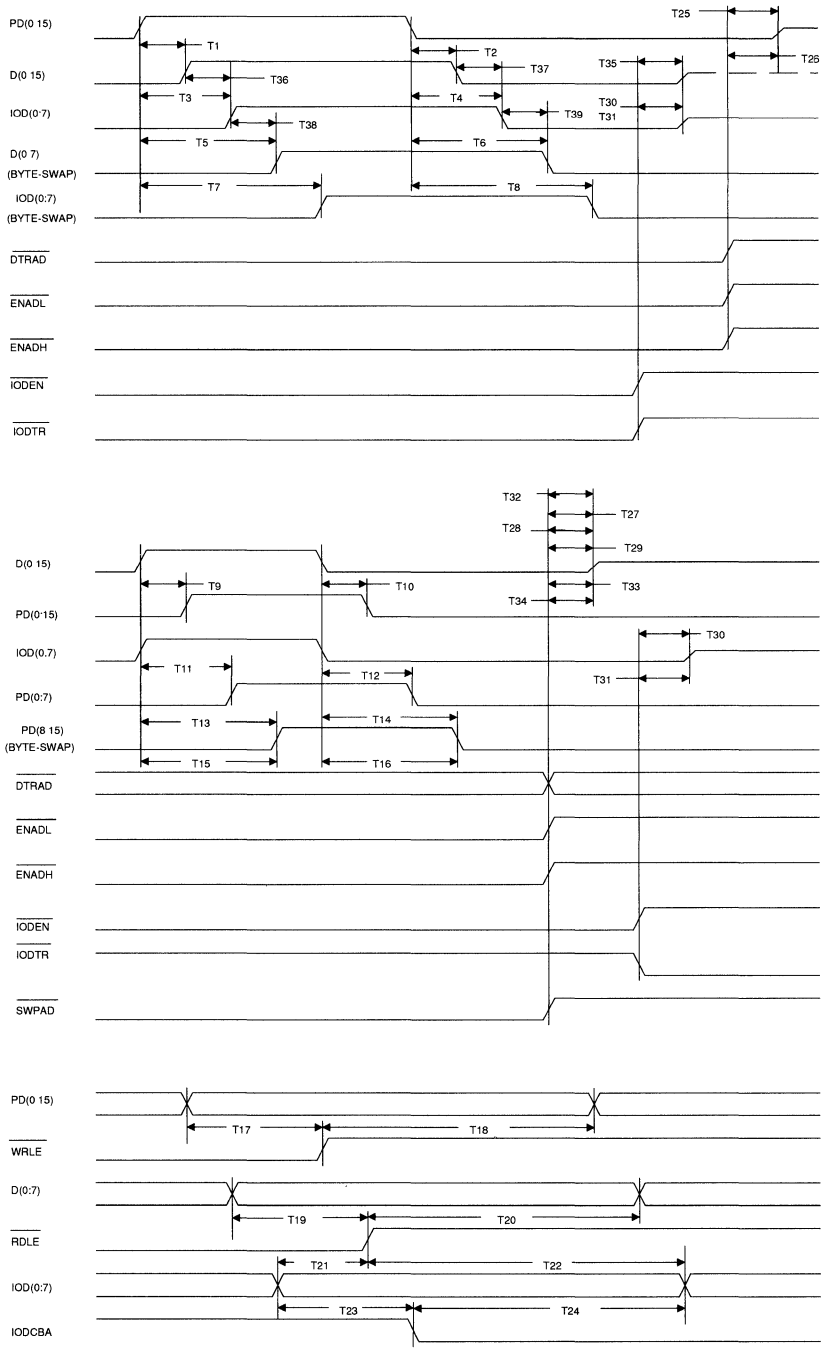


Figure 6. Data Buffer Timing

13

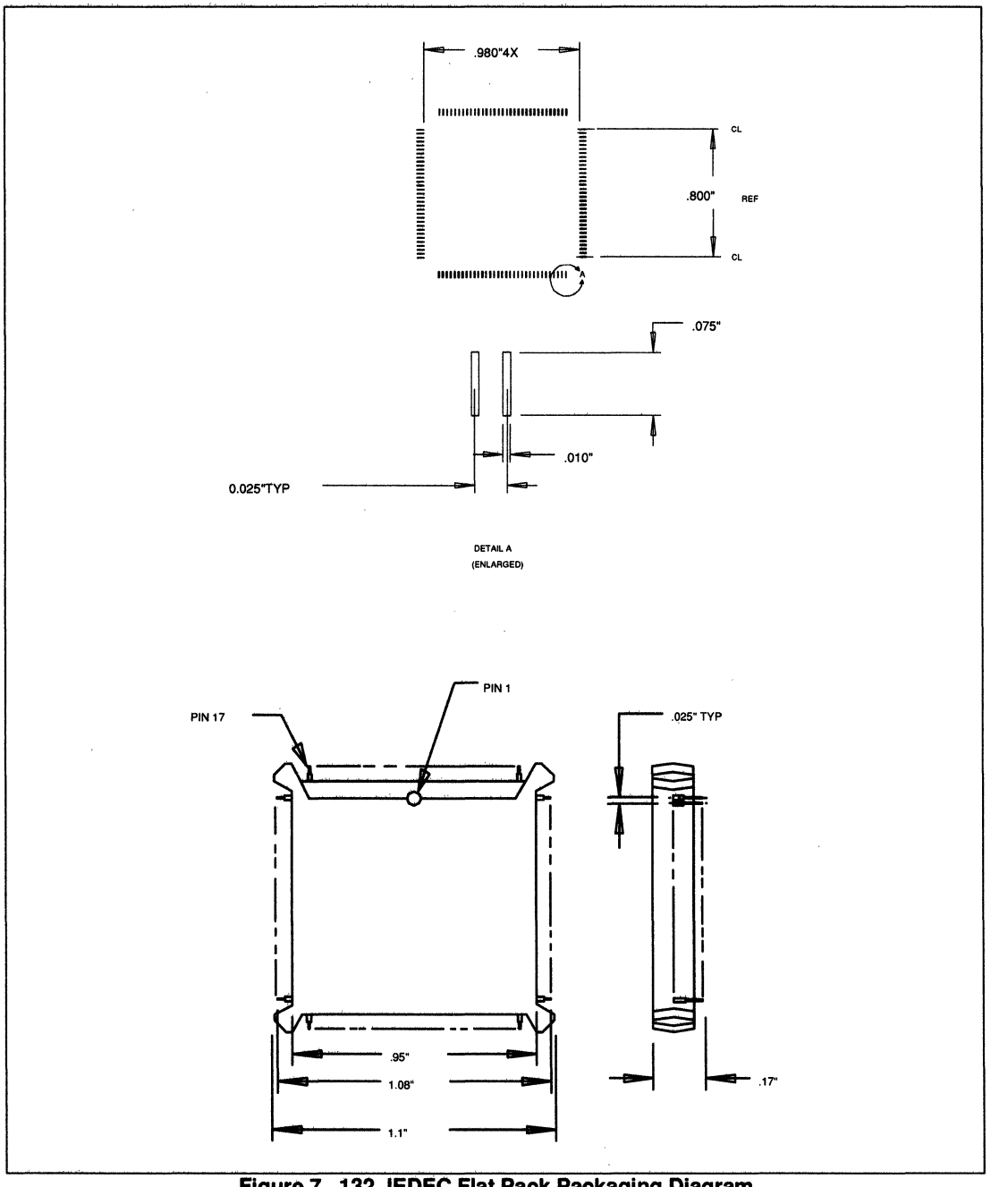
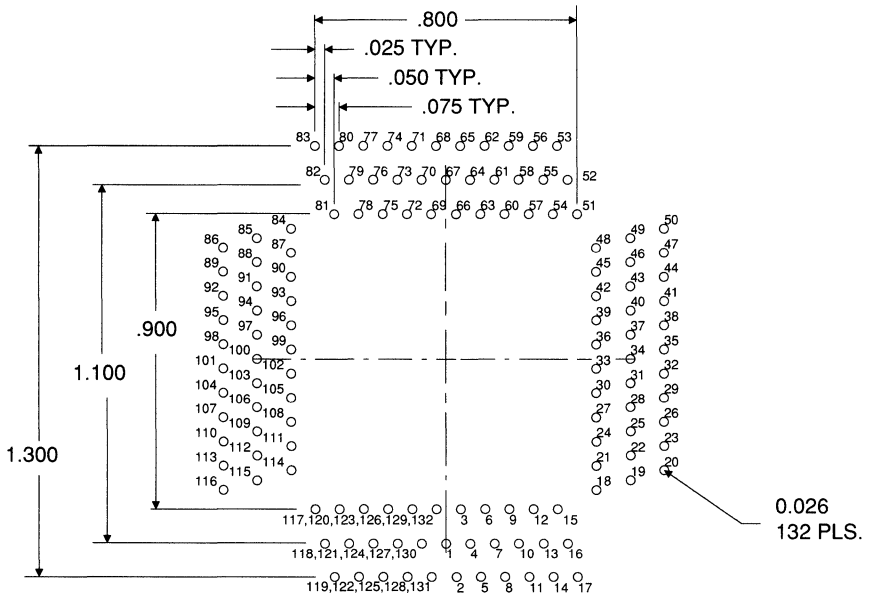


Figure 7. 132 JEDEC Flat Pack Packaging Diagram



RECOMMENDED P.C. BOARD HOLE PATTERN
SOCKET SIDE
132 POSN

Amp Incorporated
Harrisburg PA
Part No. 821932-1

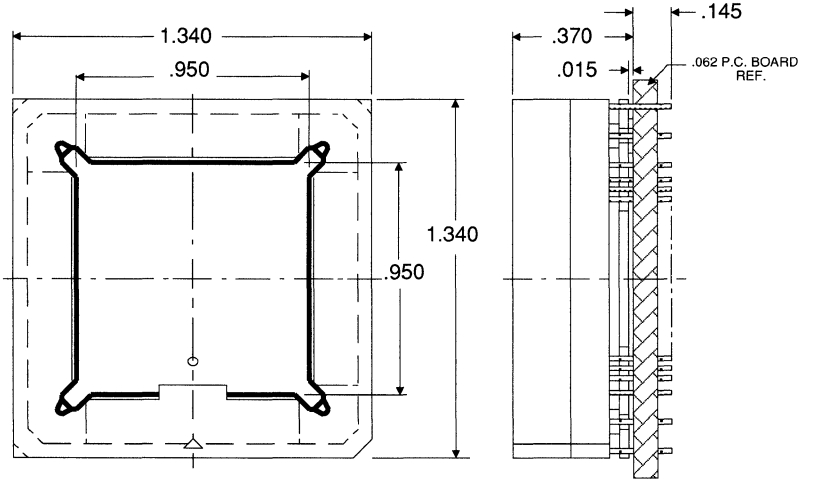


Figure 8. Socket Diagram

13

SYSTEMS LOGIC/PERIPHERAL

WD6022

Address or Data

Buffer Device

14

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

1.1 DESCRIPTION

The WD6022 devices form part of Western Digital's® innovative WD6500 chip set, which facilitates the design and implementation of 32-bit Micro Channel system boards. It decreases design complexity and saves space by combining the functions of many discrete arrays and components, also reducing system cost and increasing system reliability.

The chip set contains two WD6022 devices, one configured as an Address Buffer Device, and the other as a Data Buffer Device. Configuration is determined by a Mode pin. When this is zero, the device is configured as an address buffer; when it is one, the device is configured as a data buffer.

The block diagram in Figure 1 illustrates a typical system using the WD6500 chip set, and shows the two WD6022 devices. Devices with bold outlines are available from Western Digital Corporation.

1.2 FEATURES

- Provides Address and Data Buffers that interface to the Micro Channel
- Meets Micro Channel AC/DC Specifications
- Contains Peripheral Bus Address and Data Buffers
- Low Power 1.25 Micron CMOS Technology
- 132-Lead JEDEC Plastic Quad Flat Pack

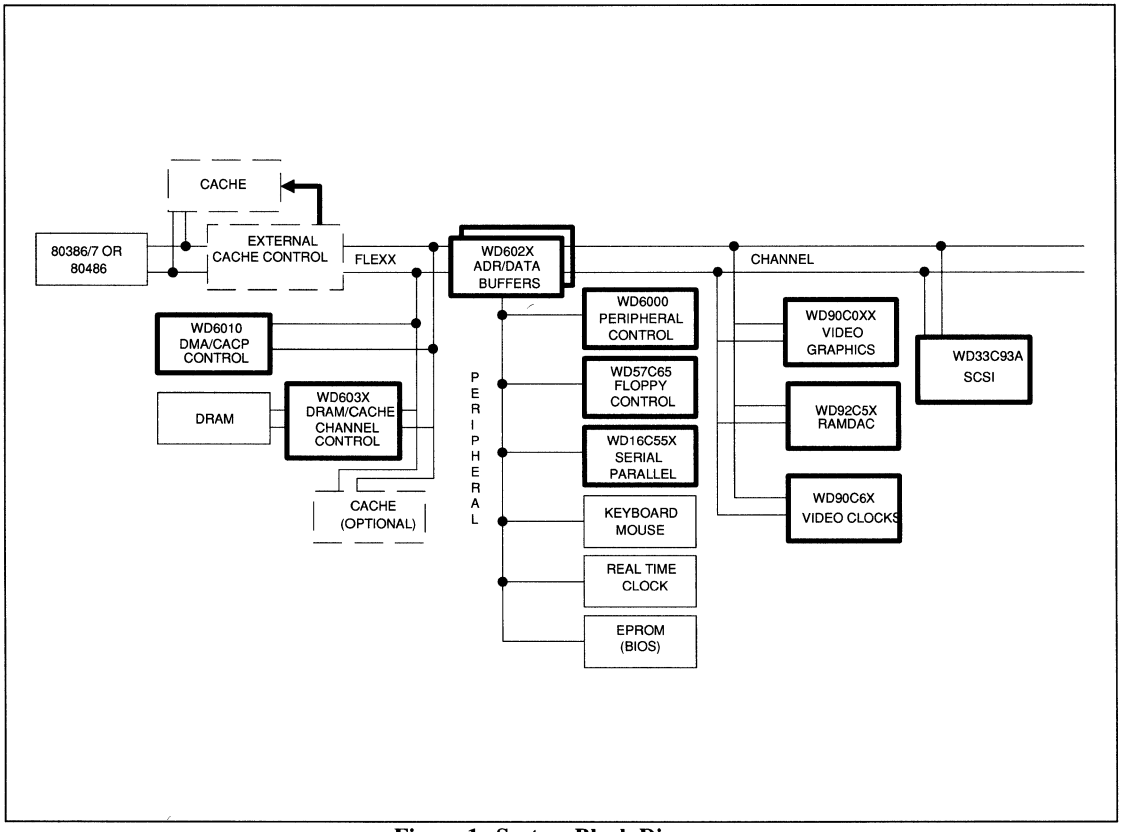


Figure 1. System Block Diagram

14

2.0 ADDRESS AND DATA BUFFER DEVICES

The WD6500 chip set contains two WD6022 Address and Data Buffer Devices, one configured as an Address Buffer Device, and the second as a Data Buffer Device.

Address Buffer Configuration

To configure the WD6022 as an address buffer, the MODE signal (pin 66) is tied to ground. When configured as an address buffer, the WD6022 performs address bus latches, implements the Central Translator function for the Micro Channel and provides decodes for the BIOS EPROMs.

Data Buffer Configuration

To configure the WD6022 as a data buffer, the MODE signal is tied to power. In this mode, the WD6022 performs data bus latches, Micro Channel data steering and data swaps for 80386/80486 and DMA operations.

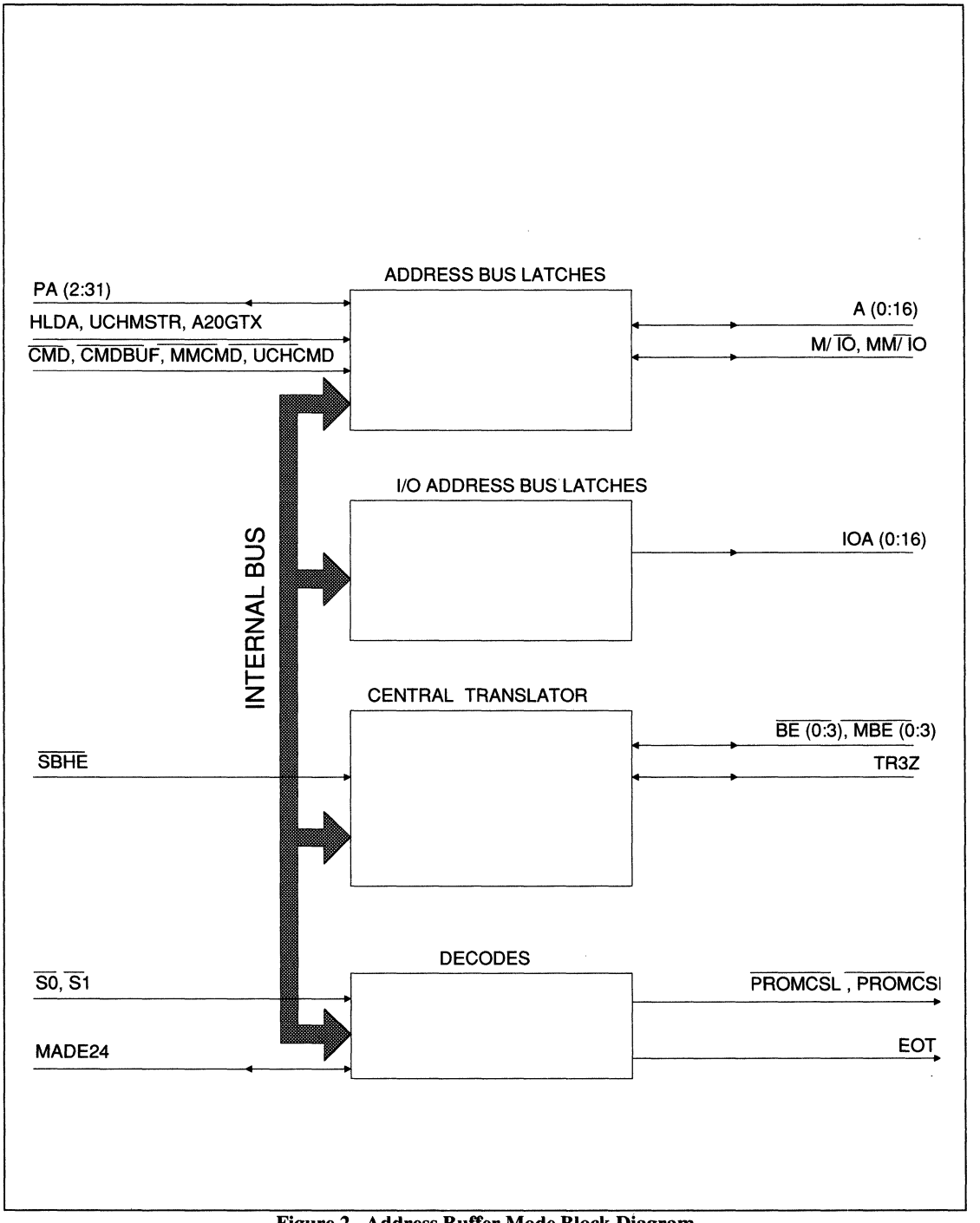


Figure 2. Address Buffer Mode Block Diagram

14

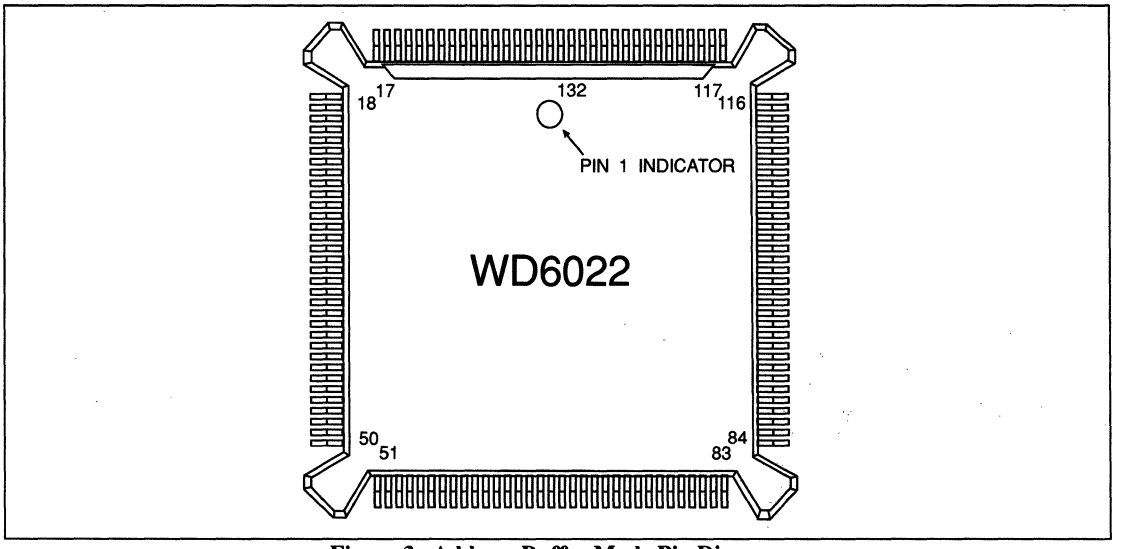


Figure 3. Address Buffer Mode Pin Diagram

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	IOA9	34	A9	67	$\overline{\text{TEST}}$	100	V_{DD}
2	IOA8	35	V_{DD}	68	MM/$\overline{\text{IO}}$	101	PA20
3	V_{DD}	36	A10	69	UCHCMD	102	PA19
4	IOA7	37	A11	70	$\overline{\text{EOT}}$	103	PA18
5	IOA6	38	V_{SS}	71	$\overline{\text{PROMCSL}}$	104	PA17
6	IOA5	39	A12	72	$\overline{\text{PROMCSH}}$	105	PA16
7	IOA4	40	A13	73	RESERVED	106	PA15
8	IOA3	41	A14	74	$\overline{\text{BE2}}$	107	PA14
9	IOA2	42	A15	75	$\overline{\text{BE3}}$	108	PA13
10	IOA1	43	V_{SS}	76	V_{SS}	109	V_{SS}
11	IOA0	44	A16	77	$\overline{\text{MBE0}}$	110	PA12
12	MADE24	45	A17	78	$\overline{\text{MBE1}}$	111	PA11
13	$\overline{\text{TR32}}$	46	V_{DD}	79	$\overline{\text{MBE2}}$	112	PA10
14	$\overline{\text{CMDBUF}}$	47	A18	80	$\overline{\text{MBE3}}$	113	PA9
15	$\overline{\text{A20GTX}}$	48	A19	81	M/$\overline{\text{IO}}$	114	PA8
16	$\overline{\text{S1}}$	49	A20	82	BIAS	115	PA7
17	V_{SS}	50	V_{SS}	83	V_{DD}	116	V_{DD}
18	V_{SS}	51	V_{SS}	84	HLDA	117	V_{SS}
19	$\overline{\text{S0}}$	52	A21	85	$\overline{\text{MMCMD}}$	118	PA6
20	$\overline{\text{CMD}}$	53	A22	86	$\overline{\text{SBHE}}$	119	PA5
21	UCHMSTR	54	A23	87	V_{SS}	120	PA4
22	A0	55	A24	88	PA31	121	PA3
23	A1	56	A25	89	PA30	122	$\overline{\text{PA2}}$
24	V_{DD}	57	V_{DD}	90	PA29	123	$\overline{\text{BE1}}$
25	A2	58	A26	91	PA28	124	$\overline{\text{BE0}}$
26	A3	59	A27	92	PA27	125	IOA16
27	V_{SS}	60	V_{SS}	93	PA26	126	IOA15
28	A4	61	A28	94	PA25	127	IOA14
29	A5	62	A29	95	PA24	128	IOA13
30	A6	63	A30	96	PA23	129	IOA12
31	A7	64	A31	97	PA22	130	IOA11
32	V_{SS}	65	V_{SS}	98	V_{SS}	131	IOA10
33	A8	66	MODE	99	PA21	132	V_{SS}

Table 1. Address Buffer Mode (Mode = 0) Pinout

2.1 ADDRESS BUFFER MODE PIN DESCRIPTIONS

PIN NO.	NAME	TYPE	FUNCTION
			ADDRESS BUS LATCHES
22 23 25 26 28 29 30 31 33 34 36 37 39 40 41 42 44 45 47 48 49 52 53 54 55 56 58 59 61 62 63 64	A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A34 A25 A26 A27 A28 A29 A30 A31	I	CHANNEL ADDRESS BUS This Channel address bus interfaces directly to the Channel. It is an input during 80386/DMA cycles. Note that A0 is always an input, and is generated by the WD6030 during 80386/DMA cycles.
124 123 122 121 120 119 118 115 114 113 112 111 110 108 107 106	PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7 PA8 PA9 PA10 PA11 PA12 PA13 PA14 PA15	I/0	PROCESSOR ADDRESS BUS This is the local processor address bus on the motherboard, and interfaces directly with the processor address bus. It is an input for 80386/80486/DMA cycles and output for master cycles.

14

PIN NO.	NAME	TYPE	FUNCTION
105 104 103 102 101 99 97 96 95 94 93 92 91 90 89 88	PA16 PA17 PA18 PA19 PA20 PA21 PA22 PA23 PA24 PA25 PA26 PA27 PA28 PA29 PA30 PA31	I/O	PROCESSOR ADDRESS BUS (CONT)
11 10 9 8 7 6 5 4 2 1 131 130 129 128 127 126 125	IOA0 IOA1 IOA2 IOA3 IOA4 IOA5 IOA6 IOA7 IOA8 IOA9 IOA10 IOA11 IOA12 IOA13 IOA14 IOA15 IOA16	O	I/O ADDRESS BUS This is the I/O address bus on the system board. It is the latched version of the addresses on the Channel. The I/O address bus supplies the addresses to all the Channel peripherals on the system board, such as the video, floppy, serial port, parallel port, timer and interrupt controllers, and EPROM.
84	HLDA 80386/ 80486	I	HOLD ACKNOWLEDGE The CPU generates this signal in response to a HOLD signal from the DMA controller. When active, it indicates that the CPU has relinquished control of the local bus.
21	UCHMSTR	I	CHANNEL MASTER This signal is generated by the CXACP in the WD6010. When active, it indicates that a Channel master has control ofthe bus. It is used to control the direction of the address buffers.
15	A20GTX	I	ADDRESS BIT 20 GATE SIGNAL This signal is generated by the WD6010, and has no effect on the address when the DMA or Micrh Channel master is generating the addresses. It is encoded in the following manner: **HLDA UCHMSTR A20GTX A20 SOURCE DEVICE** **0 0 0 0 80386/80486** **0 0 1 PA20 80386/80486** **1 0 x PA20 DMA** **1 1 x A20 Micro Channel Master**

PIN NO.	NAME	TYPE	FUNCTION
20	$\overline{CMD}$	I	$\overline{COMMAND}$ The Command signal generates the latch signal that latches the Channel addresses when a Channel master has the bus.
14	$\overline{CMDBUF}$	I	$\overline{BUFFERED\ CHANNEL\ COMMAND}$ This signal latches the Channel addresses for the IOA (16:0) address bus. The input to this signal is the CMD signal which is generated by the WD6030.
85	$\overline{MMCMD}$	I	$\overline{CHANNEL\ MATCHED\ MEMORY\ COMMAND}$ This is the Matched Memory Command signal on the Channel. This signal is pulled-up as MMC is not supported.
69	UCHCMD	O	CHANNEL COMMAND This signal is the logical OR of the $\overline{CMD}$ and $\overline{MMCMD}$ signals, and indicates that a command is present on the Channel. It is used in the WD6010 diagnostic interface.
81	M/$\overline{IO}$	I/O	LOCAL BUS M/IO The M/IO signal is on the local bus, and interfaces directly with the M/$\overline{IO}$ signal on the CPU. When a Channel master accesses the system board DRAM, this signal is a latched version of the MM/IO signal.
68	MM/$\overline{IO}$	I/O	CHANNEL M/$\overline{IO}$ This signal interfaces directly with the Channel M/$\overline{IO}$ signal, a delayed version of the CMD signal generated by the WD6000. When the 80386 or the DMA accesses the Channel, this signal is the same as M/IO.
			CENTRAL TRANSLATOR
86	$\overline{SBHE}$	I	$\overline{SYSTEM\ BYTE\ HIGH\ ENABLE}$ The System Byte High Enable signal on the Channel interfaces directly to $\overline{SBHE}$ on the Channel. When the address flow is from the processor bus to the Channel bus, the WD6030 generates this signal as a decode of $\overline{BE}$ (0:3). When the address flow goes from the Channel bus to the processor bus, this signal is used in the central translator function.
13	TR32	I/O	TRANSLATE 32 The Translate 32 signal on the Channel is used in the central translator logic. When it is active, the central translator translates A0, A1, and $\overline{SBHE}$ to $\overline{BE}$ (0:3). TR32 is used for a 16-bit master communicating with a 32-bit slave.
124 123 74 75	$\overline{BE0}$ $\overline{BE1}$ $\overline{BE2}$ $\overline{BE3}$	I/O	$\overline{BYTE\ ENABLES}$ These byte enables on the local bus interface directly with the 80386/80486 byte enables. When the address flow is from the processor address bus to the Channel address bus, these signals generate Address Bit 1 (A1). A0 is generated by the WD6030. When the address flow is from the Channel address bus to the processor address bus, these signals are generated by a 32-bit master on the Channel or the central translator for a 16-bit master.
77 78 79 80	$\overline{MBE0}$ $\overline{MBE1}$ $\overline{MBE2}$ $\overline{MBE3}$	I/O	$\overline{CHANNEL\ BYTE\ ENABLES}$ These Channel byte enable signals interface directly to the $\overline{BE}$ (0:3) on the Micro Channel. During an 80386/80486/DMA cycle, these signals are outputs. For a master cycle they are not input signals.
			DECODES
19 16	$\overline{S0}$ S1	I	CHANNEL CONTROL SIGNALS These two signals interface directly to the Channel $\overline{S}$(0:1) signals. Together with MADE24, MM/IO, and the Channel address, it generates the PROM chip selects.

14

PIN NO.	NAME	TYPE	FUNCTION
12	MADE24	I/O	CHANNEL MADE24 SIGNAL This signal directly interfaces with the Channel MADE24 signal. In combination with S(0:1) and MM/IO, it generates the PROM chip selects. During 80386/80486/DMA cycles, this signal is an output signal. **ADDRESSES** **MADE24** 0-16 MBytes 1 >16 MBytes 0
71 72	PROMCSL PROMCSH	O O	PROM CHIP SELECT (Low) PROM CHIP SELECT (High) These signals select the two 64K by 8 (27512) PROMs which together form the 128K of PROM on the system board. The two PROMs are organized into even and odd banks, providing a 16-bit wide interface. PROMCSL selects the even banks and PROMCSH selects the odd banks. Configurations with 8-bit wide, 1 M bit PROMs (27010) are also possible. In such a case, PROM Chip Select is generated by executing a logical OR of PROMCSL and PROMCSH. To get the BIOS to execute faster, the PROM can be mapped to the DRAM and executed from there. The PROMs are located at 000E0000H - 000FFFFFH and at FFFE0000 - FFFFFFFFH. An access to either of these locations generates the chip selects for the PROM. However, a Channel cycle to access the PROM will only be run if an access is made to FFFE0000 - FFFFFFFFH, or if a read access is made to E0000 -FFFFF, and the PROM is not mapped to RAM. Writes to these addresses are ignored.
70	EOT	O	END-OF-TRANSFER This signal is activated when $\overline{CMD}$ and $\overline{S}$(1:0) are inactive. The CACP controller inside the WD6010 uses this signal and BURST to detect an End-of-Transfer condition.
			MISCELLANEOUS
66	MODE	I	MODE PIN This pin determines the mode of operation for the WD6022 device. When tied to V_{DD}, it puts the WD6022 into the data buffer mode; when it is tied to ground, it puts it into the address buffer mode
67	TEST	I	$\overline{TEST}$ PIN This is an active low pin to facilitate board-level testing. When low, this signal tristates all outputs and bi-directional signal lines so that an ATE tester can drive these signals instead.
82	BIAS	I	BIAS PIN This pin controls the biasing of the internal buffers, and should be pulled low with a 1.25K ±1% resistor.
3, 24, 35, 46,57, 83, 100, 116	V_{DD}	I	+5 V Power Supply
17, 18, 27, 32, 38, 43, 50, 51, 60, 65, 76, 87, 98, 109, 117, 132	V_{SS}	I	O V Ground

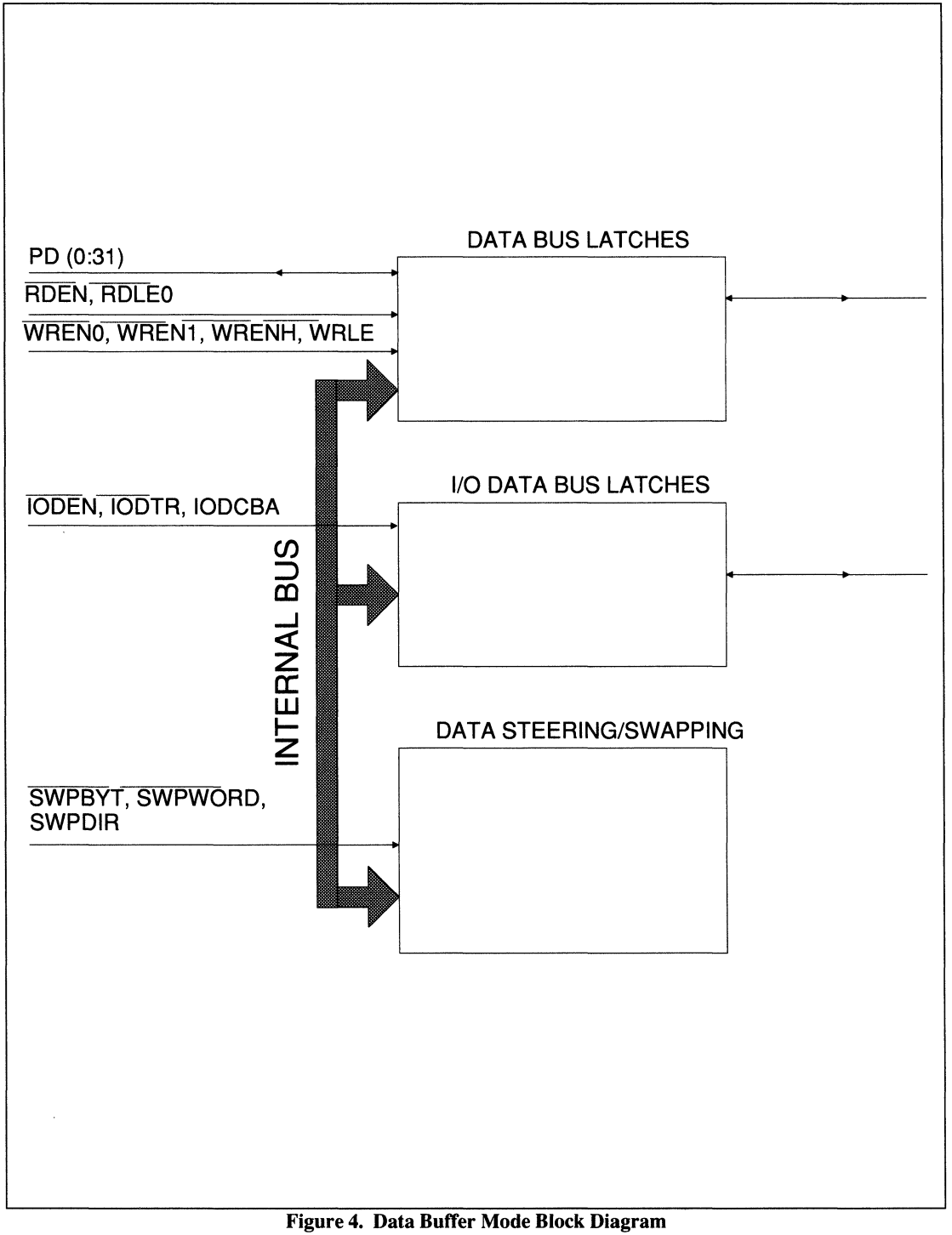


Figure 4. Data Buffer Mode Block Diagram

14

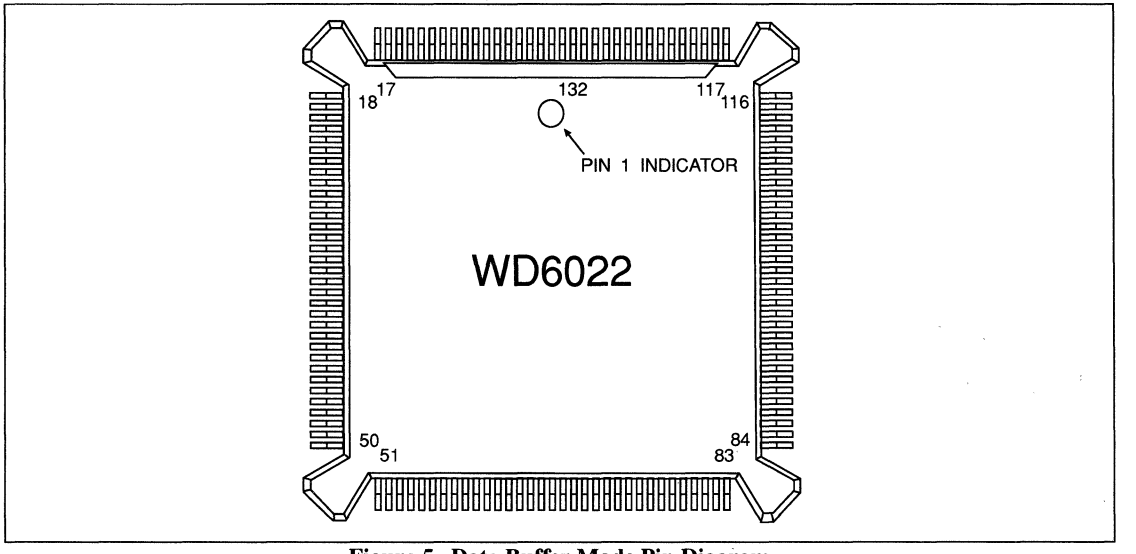


Figure 5. Data Buffer Mode Pin Diagram

PIN	–	NAME	PIN	–	NAME	PIN	–	NAME	PIN	–	NAME
1	–	IOD9	34	–	D9	67	–	$\overline{\text{TEST}}$	100	–	V_{DD}
2	–	IOD8	35	–	V_{DD}	68	–	RESERVED	101	–	PD20
3	–	V_{DD}	36	–	D10	69	–	RESERVED	102	–	PD19
4	–	IOD7	37	–	D11	70	–	RESERVED	103	–	PD18
5	–	IOD6	38	–	V_{SS}	71	–	RESERVED	104	–	PD17
6	–	IOD5	39	–	D12	72	–	RESERVED	105	–	PD16
7	–	IOD4	40	–	D13	73	–	RESERVED	106	–	PD15
8	–	IOD3	41	–	D14	74	–	RESERVED	107	–	PD14
9	–	IOD2	42	–	D15	75	–	RESERVED	108	–	PD13
10	–	IOD1	43	–	V_{SS}	76	–	V_{SS}	109	–	V_{SS}
11	–	$\overline{\text{IOD0}}$	44	–	D16	77	–	RESERVED	110	–	PD12
12	–	$\overline{\text{IODEN}}$	45	–	D17	78	–	RESERVED	111	–	PD11
13	–	$\overline{\text{IODTR}}$	46	–	V_{DD}	79	–	RESERVED	112	–	PD10
14	–	$\overline{\text{WRLE}}$	47	–	D18	80	–	RESERVED	113	–	PD9
15	–	$\overline{\text{WRENH}}$	48	–	D19	81	–	RESERVED	114	–	PD8
16	–	$\overline{\text{WREN1}}$	49	–	D20	82	–	BIAS	115	–	PD7
17	–	V_{SS}	50	–	V_{SS}	83	–	V_{DD}	116	–	V_{DD}
18	–	V_{SS}	51	–	V_{SS}	84	–	$\overline{\text{SWPDIR}}$	117	–	V_{SS}
19	–	$\overline{\text{WREN0}}$	52	–	D21	85	–	$\overline{\text{SWPWORD}}$	118	–	PD6
20	–	$\overline{\text{RDLE0}}$	53	–	D22	86	–	$\overline{\text{SWPBYT}}$	119	–	PD5
21	–	$\overline{\text{RDEN}}$	54	–	D23	87	–	V_{SS}	120	–	PD4
22	–	D0	55	–	D24	88	–	PD31	121	–	PD3
23	–	D1	56	–	D25	89	–	PD30	122	–	PD2
24	–	V_{DD}	57	–	V_{DD}	90	–	PD29	123	–	PD1
25	–	D2	58	–	D26	91	–	PD28	124	–	PD0
26	–	D3	59	–	D27	92	–	PD27	125	–	IODCBA
27	–	V_{SS}	60	–	V_{SS}	93	–	PD26	126	–	IOD15
28	–	D4	61	–	D28	94	–	PD25	127	–	IOD14
29	–	D5	62	–	D29	95	–	PD24	128	–	IOD13
30	–	D6	63	–	D30	96	–	PD23	129	–	IOD12
31	–	D7	64	–	D31	97	–	PD22	130	–	IOD11
32	–	V_{SS}	65	–	V_{SS}	98	–	V_{SS}	131	–	IOD10
33	–	D8	66	–	MODE	99	–	PD21	132	–	V_{SS}

Table 2. Data Buffer Mode (Mode = 1) Pinout

2.2 DATA BUFFER MODE PIN DESCRIPTIONS

PIN NO.	NAME	TYPE	FUNCTION
			DATA BUS LATCHES
22 23 25 26 28 29 30 31 33 34 36 37 39 40 41 42 44 45 47 48 49 52 53 54 55 56 58 59 61 62 63 64	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 D31	I/O	CHANNEL DATA BUS These Channel data bus signal lines connect directly to the Channel data bus.
124 123 122 121 120 119 118 115 114 113 112 111 110 108 107 106	PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7 PD8 PD9 PD10 PD11 PD12 PD13 PD14 PD15	I/O	PROCESSOR DATA BUS These processor data bus signal lines connect directly to the 80386 data bus.

14

PIN NO.	NAME	TYPE	FUNCTION
105 104 103 102 101 99 97 96 95 94 93 92 91 90 89 88	PD16 PD17 PD18 PD19 PD20 PD21 PD22 PD23 PD24 PD25 PD26 PD27 PD28 PD29 PD30 PD31	I/O	PROCESSOR DATA BUS (CONT)
11, 9-4, 3-1, 13-125	IOD (0:15) to IOD (0:0)	I/O	16-BIT I/O DATA BUS This is the 16-bit I/O data bus, which provides support for devices eight bits or sixteen bits wide.
21	$\overline{\text{RDEN}}$	I	$\overline{\text{READ ENABLE}}$ This read-enable signal enables for the processor data bus (PD (0:31)) when data flows from the Channel data bus to the processor data bus. This signal is active when the CPU or the DMA performs a read from the Channel, or when a Channel master writes to the system board DRAM.
20	$\overline{\text{RDLE0}}$	I	$\overline{\text{READ LATCH ENABLE 0}}$ This signal is the latch enable signal for Byte 0 (0:7). When the CPU or the DMA performs a cycle to an 8-bit device on the Channel, the cycle is split in two. This signal latches the first 8 bits (0:7) during the first cycle, reads the next 8 bits (8:15) during the second cycle, and this presents the 16 bits to the CPU.
19 16 15	$\overline{\text{WREN0}}$ $\overline{\text{WREN1}}$ WRENH	I	$\overline{\text{WRITE ENABLE (HIGH, 0:1)}}$ This signal enables the buffer during data flow from the processor data bus to the Channel data bus D (0:31). These signals control Byte 0 (0:7) (WREN0), byte 1 (8:15) (WREN1), and the upper word (16:31) (WRENH). These signals are valid when the CPU or the DMA performs a write operation to the Channel or when a Channel master performs a read from the motherboard DRAM.
14	$\overline{\text{WRLE}}$	I	$\overline{\text{WRITE LATCH ENABLE}}$ This write latch enable signal latches the write data during a CPU or DMA write operation to the Channel. It also provides the write-data-hold time required by the Channel during these operations. This signal also latches the data when the CPU or DMA writes to an 8-bit port and the cycle has to be split in two.
12	$\overline{\text{IODEN}}$	I	$\overline{\text{I/O DATA ENABLE}}$ The I/O Data Enable signal enables the I/O data buffers and is generated by the WD6000. When it is active, the WD6022 drives either D(0:15) or IOD(0:15), depending on the direction set by the IODTR signal.
13	$\overline{\text{IODTR}}$	I	$\overline{\text{I/O DATA TRANSMIT/RECEIVE}}$ The I/O Data Transmit/Receive signal controls the direction of the I/O data buffers inside the WD6022. The signal itself is generated by the WD6000 device. **IODTR** **DIRECTION** 1 D(0:15) to IOD(0:15) 0 IOD(0:15) to D(0:15)

PIN NO.	NAME	TYPE	FUNCTION
125	IODCBA	I	I/O DATA CLOCK The I/O Data Clock signal is used to latch the data during reads from the Channel peripherals on the I/O bus. The MEMRD, MEMWR, IORD, and IOWR commands to the peripherals are shorter than the Channel CMD signal. This signal ensures that the data being read meets the timings of the Channel CMD signal.
			DATA STEERING/SWAPPING
86	$\overline{\text{SWPBYT}}$	I	$\overline{\text{BYTE SWAP}}$ When the CPU or DMA accesses an 8-bit port the cycle is split into two. This signal is used to swap the data to the correct byte: D(0:7) are swapped to D(8:15) for a read operation; D(8:15) are swapped to D(0:7) for a write operation.
85	$\overline{\text{SWPWORD}}$		$\overline{\text{WORD SWAP}}$ This signal swaps words when a 16-bit Channel master communicates with a 32-bit slave. The cycle is split into two and SWPWORD is used to swap data to the correct word: D(16:31) is swapped to D(0:15) for a Channel master read operation and D(0:15) is swapped to D(16:31) for a Channel master write operation. This function is known as data steering.
84	SWPDIR (COPRES)	I	SWAP DIRECTION At power-up, the state of this signal is latched by the WD6030 to determine the presence of the numeric coprocessor. At all other times, SWPDIR determines the direction of the byte and word swap buffers. A low on SWPDIR indicates a read operation (byte swap D(0:7) to D(8:15) or a Channel master write operation (word swap D(0:15) to D(16:31)). A high on SWPDIR indicates a write operation (byte swap D(8:15) to D(0:7)).
			MISCELLANEOUS
66	MODE	I	MODE PIN This pin determines the mode of operation for the WD6022 device. When tied to V_{DD}, it puts the WD6022 into the data buffer mode; when it is tied to ground, it puts it into the address buffer mode..
67	$\overline{\text{TEST}}$	I	$\overline{\text{TEST PIN}}$ This is an active low pin to facilitate board-level testing. When low, this signal tristates all outputs and bi-directional signal lines so that an ATE tester can drive these signals instead.
82	BIAS	I	BIAS PIN This pin controls the biasing of the internal buffers, and should be pulled low with a 1.25K ±1% resistor.
3, 24, 35, 46,57, 83, 100, 116	V_{DD}	I	+5 V Power Supply
17, 18, 27, 32, 38, 43, 50, 51, 60, 65, 76, 87, 98, 109, 117, 132	V_{SS}	I	0 V Ground

14

PIN NO.	NAME	TYPE	FUNCTION
68, 69, 70, 71, 72, 73, 74, 75, 77, 78, 79, 80, 81	Reserved	-	RESERVED PINS These pins should not be connected.

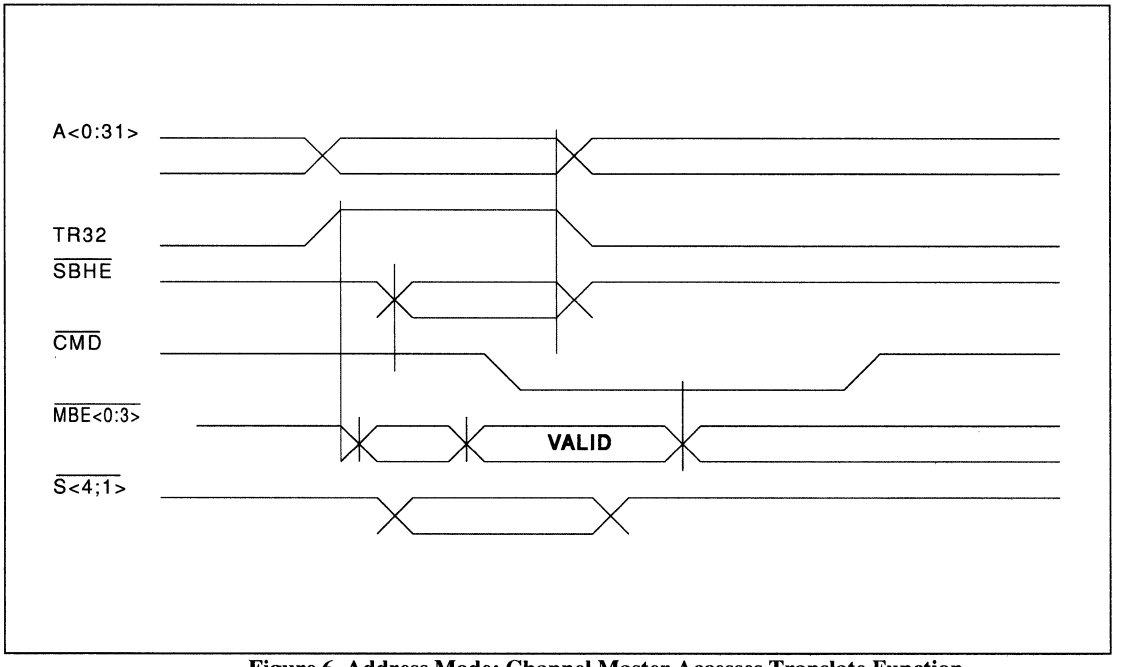


Figure 6. Address Mode: Channel Master Accesses Translate Function

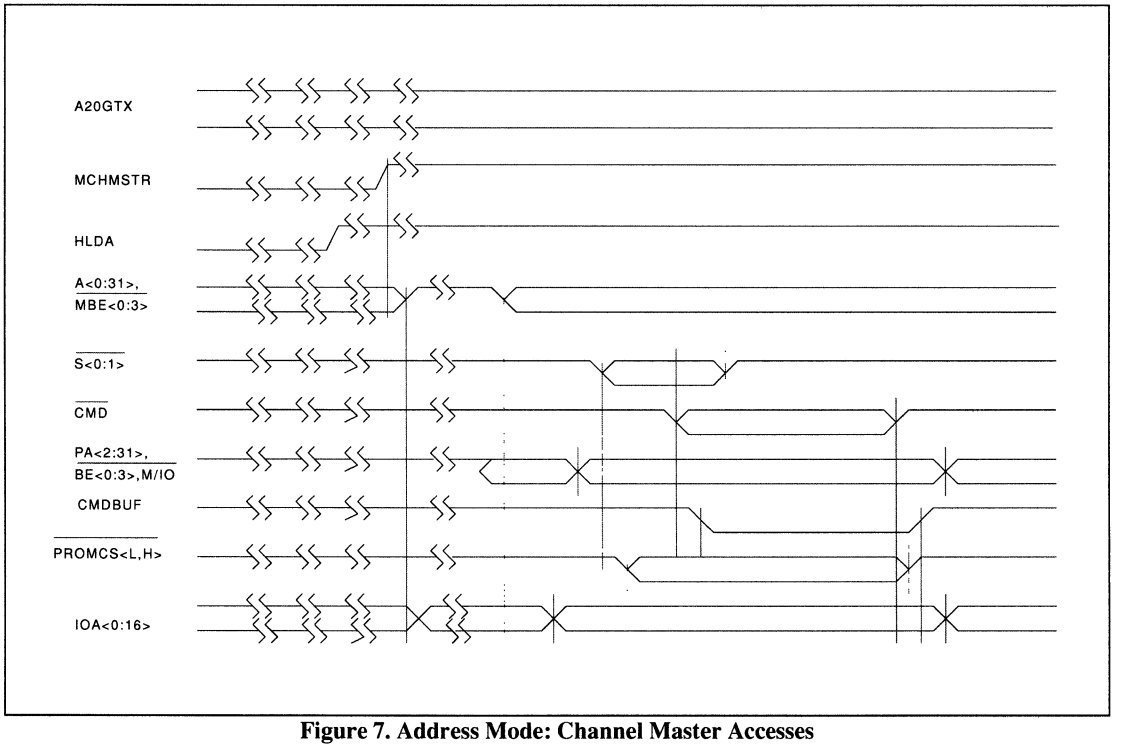


Figure 7. Address Mode: Channel Master Accesses

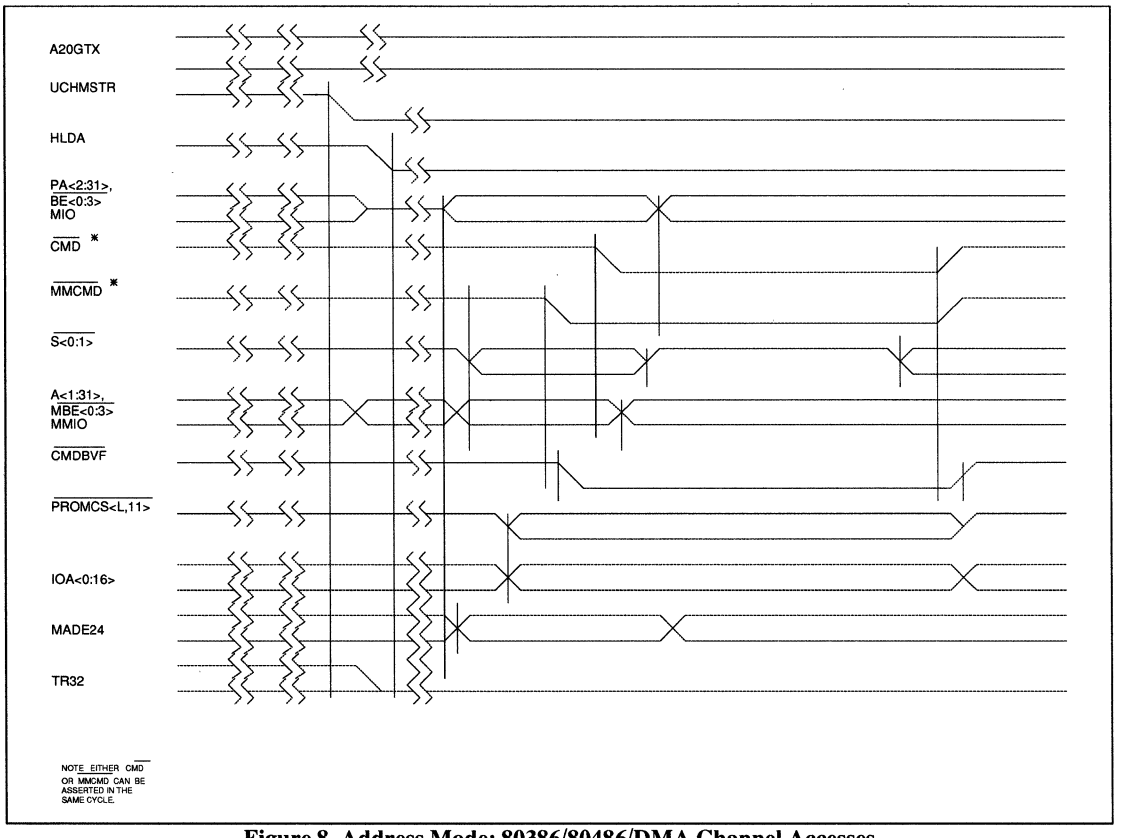


Figure 8. Address Mode: 80386/80486/DMA Channel Accesses

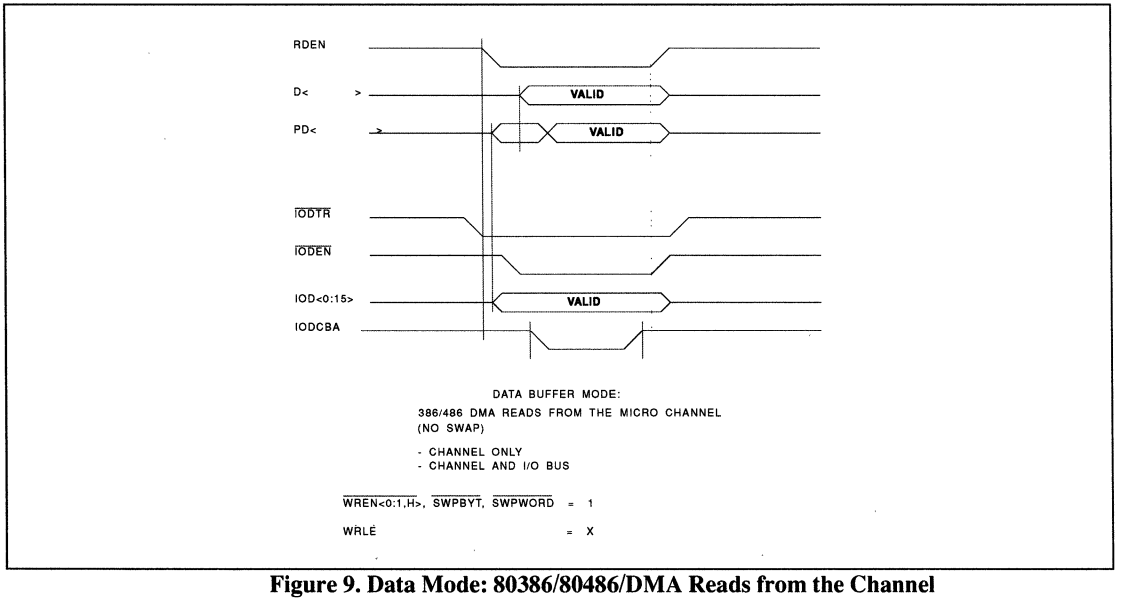
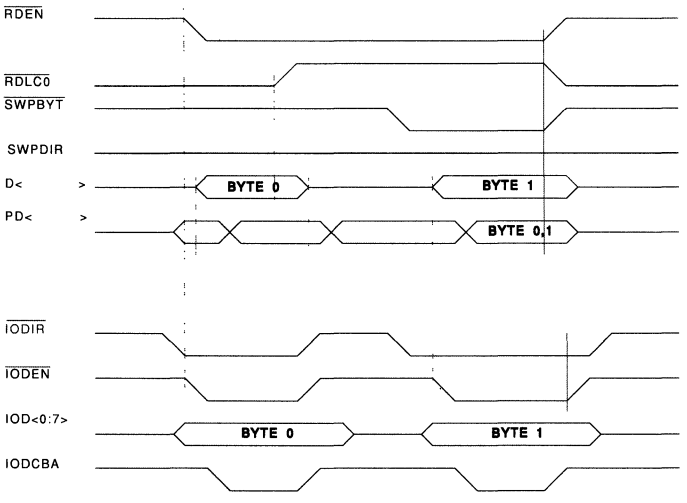


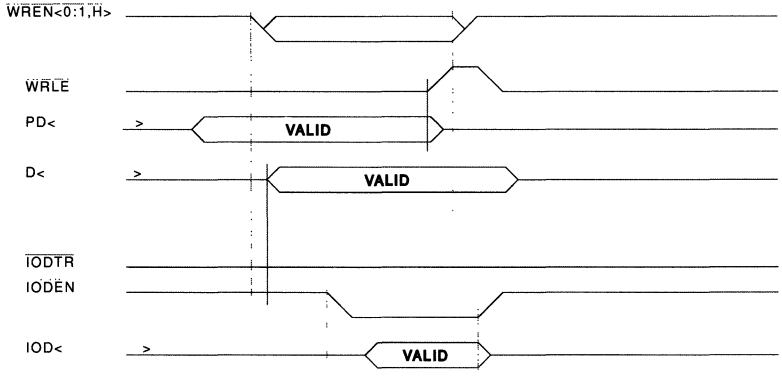
Figure 9. Data Mode: 80386/80486/DMA Reads from the Channel



WD6021: 386/486 DMA READS FROM THE MICRO CHANNEL
(WITH SWAP)
- CHANNEL ONLY
- CHANNEL AND I/O BUS

WREN<0:1,H>, SWPWORD = 1
WRLE = X

Figure 10. Data Mode: 80386/80486/DMA Reads from the Channel with Swap

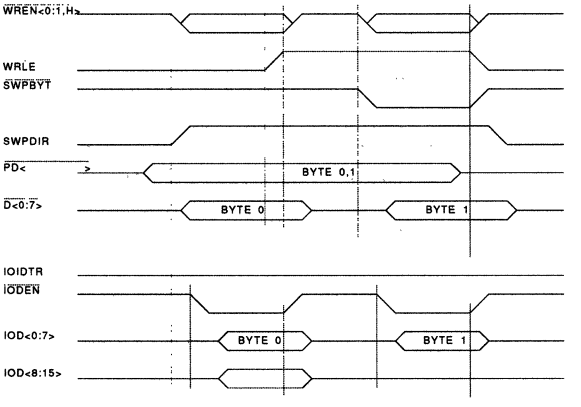


WD6021: 386/486 DMA - WRITES TO THE MICRO CHANNEL
(NO SWAP)
- CHANNEL ONLY
- CHANNEL AND I/O BUS

RDEN, SWPBYT, SWPWORD = 1
RDLE0, SWPDIR, IODCBA = X

Figure 11.Data Mode: 80386/80486/DMA Writes to the Channel

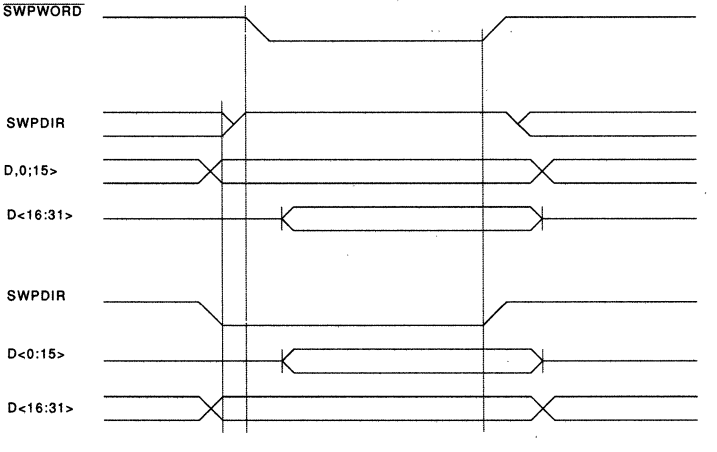
14



WD6021: 386/486 DMA WRITE TO THE WORD CHANNEL
(WITH SWAP)
- MICRO CHANNEL ONLY
- MICRO CHANNEL AND I/O BUS

RDEN, SWPWORD = 1
RDLE0, IODCBA = X

Figure 12. Data Mode: 80386/80486/DMA Writes to the Channel with Swap



WD6021: MICRO CHANNEL MASTER - WORD SWAP

SWPBYT, NWRLE, NRDLE0 = 1

CODTR, NIODEN, NRDEN = X

WREN<0:1,H>

Figure 13. Data Mode: Channel Master Word Swap

3.0 TECHNICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum stress ratings for the WD6022 devices are tabulated below. Permanent damage to the devices could result from exposing it to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD} - V_{SS}	0	7	V
Input Voltage	V_{IABS}	VSS - 0.3	V_{DD} + 0.3	V
Bias on Output Pin	V_{OABS}	V_{SS} - 0.3	V_{DD} + 0.3	V
Storage Temperature	T_S	-40	125	°C

3.2 NORMAL OPERATING CONDITIONS

Exposing the WD6022 to conditions exceeding the normal operating conditions for extended periods of time can affect the long-term reliability of the device.

VSS = 0 V

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	-0.3	VDD + 0.3	V
Power Dissipation	P_W	-	TBD	mW
Supply Current	I_{DD}	-	TBD	mA

3.3 DC CHARACTERISTICS (UNDER NORMAL OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance @ fc = 1 MHz	C_I	-	5	pF
I/O Capacitance	C_{IO}	-	10	pF
Logic High Input Voltage	V_{IH}	2.0	-	V
Logic Low Input Voltage	V_{IL}	-	0.8	V
Input Leakage	I_{IL}	-	+-10	µA
Tristate Output Leakage	I_{OL}	-	+-30	µA
I/O Pin Leakage	I_{IOL}	-	+-40	µA
WD6022 ADDRESS BUFFER MODE (MODE = 0)				
OUTPUTS $\overline{\text{PROMCSL}}$, $\overline{\text{PROMCSH}}$, EOT, UCHCMD, PA(2:31)*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	4	-	mA
OUTPUTS $\overline{\text{BE}}$(0:3), M/$\overline{\text{IO}}$*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	6	-	mA
OUTPUT IOA(0:16)				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	8	-	mA
ALL OTHER OUTPUTS*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	24	-	mA

14

PARAMETER	SYMBOL	MIN	MAX	UNITS
WD6022 DATA BUFFER MODE (MODE = 1)				
OUTPUTS PD(0:31)*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	4	-	mA
OUTPUTS IOD(0:15)*				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	6	-	mA
OUTPUT D(0:31)				
Source Current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	24	-	mA

*The following signals are bi-directional: PA(31:2), $\overline{BE}$(3:0), M/$\overline{IO}$, MADE24, TR32, MM/$\overline{IO}$, $\overline{MBE}$(3:0), A(31:1), $\overline{SBHE}$, PD(31:0), IOD(15:0), and D(31:0).

NOTE
1. The input pin "BIAS" is connected externally to ground through a 1% 1.25 K ohm resistor, and is part of an internal biasing circuit. Capicitance, leakage, and threshold measurements on this pin do not apply.
2. The following signals have internal pullups of 20K: $\overline{BE}$(3:2), $\overline{MBE}$(3:0), MM/$\overline{IO}$, M/$\overline{IO}$.
3. When $\overline{TEST}$ = 0, all outputs and bi-directional signal lines are tristated.

PARAMETER	SYMBOL	MIN	MAX	UNITS
WD6022 ADDRESS BUFFER MODE (MODE = 0)				
$\overline{PROMCSL}$, $\overline{PROMCSH}$, EOT, UCHCMD	CL	50	-	pF
$\overline{BE}$(0:3), M/$\overline{IO}$*	CL	120	-	pF
PA(2:31), IOA(0:16)*	CL	120	-	pF
MADE24, TR32, MM/$\overline{IO}$, $\overline{MMC}$, $\overline{MBE}$(0:3), A(1:31), $\overline{SBHE}$*	CL	240	-	pF
WD6022 DATA BUFFER MODE (MODE = 1)				
PD(0:31), IOD(0:15)*	CL	120	-	pF
D(0:31)*	CL	240	-	pF

3.4 A.C. LOAD SPECIFICATIONS

*The following signals are bi-directional: PA(31:2), $\overline{BE}$(3:0), M/$\overline{IO}$, MADE24, TR32, MM/$\overline{IO}$, $\overline{MBE}$(3:0), A(31:1), $\overline{SBHE}$, PD(31:0), IOD(15:0), and D(31:0).

NOTE
1. The following signals have internal pullups of 20K: $\overline{BE}$(3:2), $\overline{MBE}$(3:0), MM/$\overline{IO}$, M/$\overline{IO}$.

4.0 TIMING

PARAM	DESCRIPTION	MIN	MAX	UNITS
T1	Propagation Delay			ns
	A1, SBHE, MBE(0:3) to BE(0:3)		28	ns
	PA(2:31), to A(2:32)		26	ns
	A(0:31) to PA(2:31), BE(0:3)		26/28	ns
	A20GTX to A20		26	ns
	M/IO to MM/IO		25	ns
	MM/IO to M/IO		25	ns
	TR32, A(0:1), SBHE to MBE(0:3) or		28	ns
	BE(0:3)	-	28	ns
T2	CMD, MMCMD, to UCHCMD	-	20	ns
T3	S(0:1), CMD to EOT	-	25	ns
T4A	M/IO, S(0:1), MADE24, A(0, 31:17)	-	27	ns
	SBHE to PROMCSL, PROMCSH	-	27	ns
T4B	PA(13:17), A20GTX, HLDA, UCHMSTR to	-	54	ns
	PROMCSL, PROMCSH	-	54	ns
T5A	A(0:16), to IOA(0:16)	-	25	ns
T5B	PA(2:16), BE(3:0) to IOA(0:16)	-	50	ns
T6	HLDA to MMC or MADE24	-	25	ns
T7A	Setup to Falling Edge of CMD, MADE24, 5432, M/IO,	10	-	ns
	MM/IO, PA(2:31), BE(0:3), A(0:31), MBE(0:3),	10	-	ns
	SBHE, S(0:1)	10	-	ns
T7B	Setup to Falling Edge of CMD	40	-	ns
	A20GTX, UCHMSTR, HLDA	40	-	ns
T8A	Hold from Falling Edge of MCMD, MADE24, TR32,	10	-	ns
	M/IO, MM/IO, PA(2:31), BE(0:3), A(0:31),	10	-	ns
	MBE(0:3), SBHE, S(0:1)	10	-	ns
T8B	Hold from Falling Edge of CMD	15	-	ns
	A20GTX, UCHMSTR, HLDA	15	-	ns
T9	CMD Inactive Pulse Width	30	-	ns
T10A	Setup to Rising Edge of CMDBUF	10	-	ns
	PA(2:31), BE(0:3), A(0:15)	10	-	ns
T10B	Setup to Rising Edge of CMD	5	-	ns
T11	Hold from Rising Edge of CMDBUF	5	-	ns
	PA (2:31), BE(0:3), A(0:15)	5	-	ns
T12	CMDBUF Inactive Pulse Width	30	-	ns
T13A	Disable - from UCHMSTR	21	-	ns
	A(1:31), MBE(0:3), MM/IO, MADE24,	21	-	ns
	TR32, SBHE, PA(2:31), BE(0:3), M/IO	21	-	ns
T13B	Enable - from UCHMSTR	26	-	ns
	A(1:31), MBE(0:3), MM/IO, MADE24	26	-	ns
	TR32, SBHE, PA(2:31), BE(0:3), M/IO	26	-	ns

Table 3. Address Buffer Mode Timings (ns)

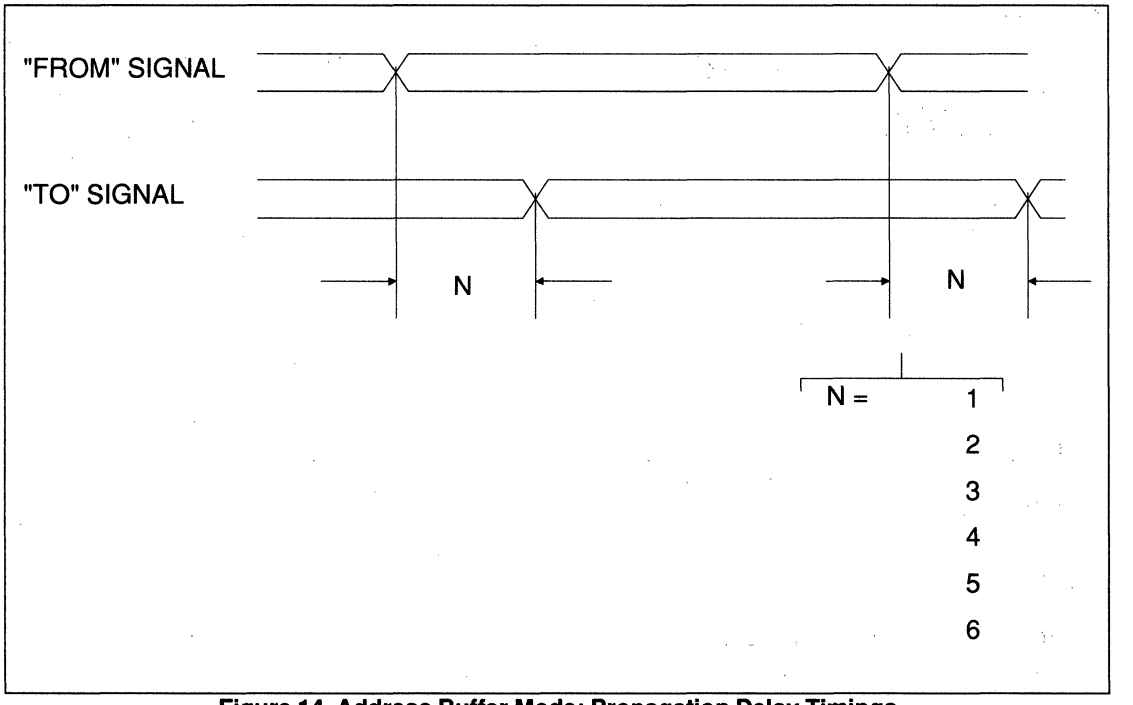


Figure 14. Address Buffer Mode: Propagation Delay Timings

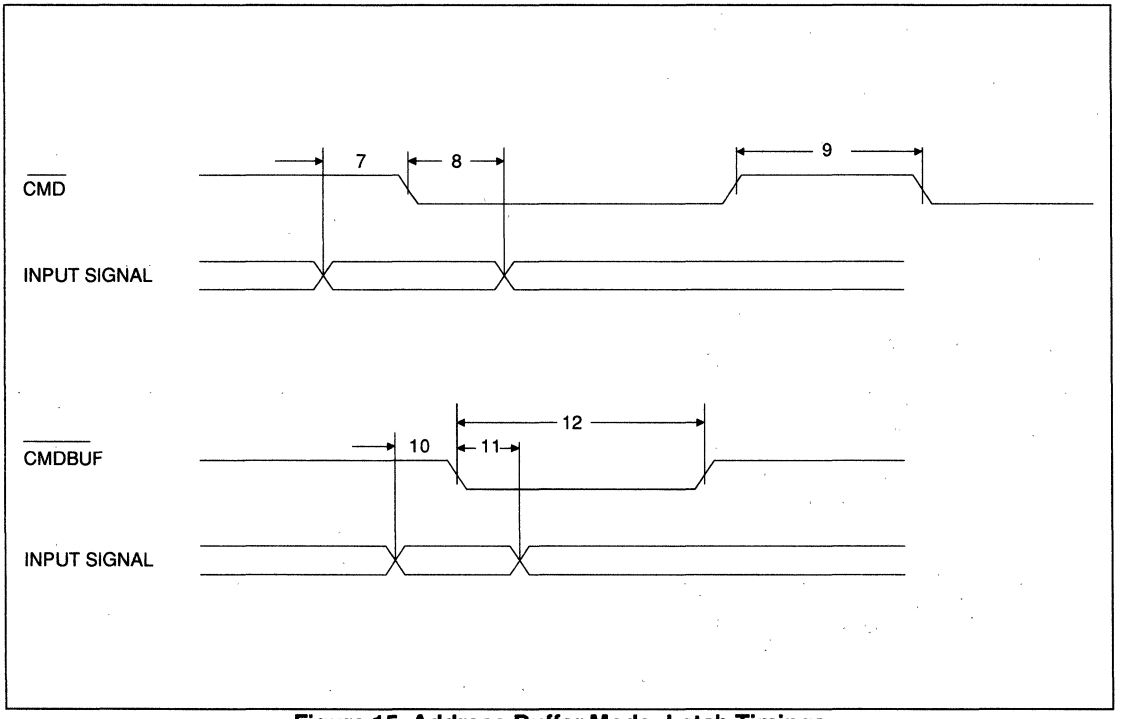


Figure 15. Address Buffer Mode: Latch Timings

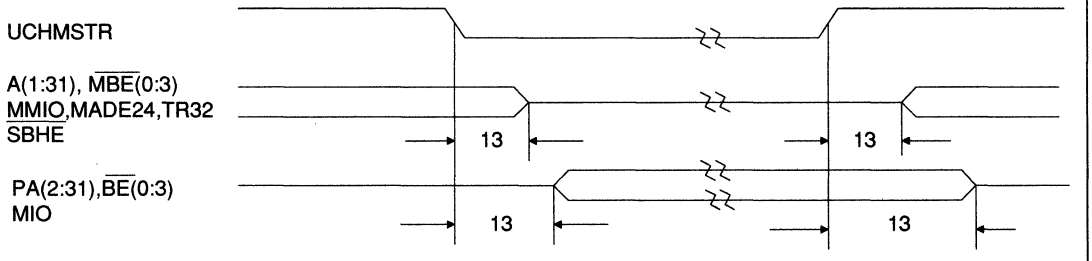


Figure 16. Address Buffer Mode: Float/Enable Timings

14

PARAM	DESCRIPTION	MIN	MAX	UNITS
T1	Output Enable/Disable	-	-	ns
	$\overline{\text{WREN0}}$ to D(0:7)	-	26	ns
	$\overline{\text{WREN1}}$ to D(8:15)	-	26	ns
	$\overline{\text{WRENH}}$ to D(16:31)	-	26	ns
	$\overline{\text{RDEN}}$ to PD(0:31)	-	28	ns
	$\overline{\text{IODEN}}$ or $\overline{\text{IODTR}}$ to D(0:15) or IOD(0:15)	-	25	ns
T2	Propagation Delay in Transparent Mode	-	-	ns
	PD(0:31) to D(0:31)	-	26	ns
	D(0:31) to PD(0:31)	-	26	ns
T3	Latch Enable to Data	-	-	ns
	$\overline{\text{WRLE}}$ to D(0:31) ($\overline{\text{WRENX}}$ active)	-	15	ns
	$\overline{\text{RDLE0}}$ to PD(0:7) ($\overline{\text{RDENL}}$ active)	-	15	ns
T4A	Data Setup to Latch Enable	-	-	ns
	D(0:7) to $\overline{\text{RDLE0}}$	10	-	ns
	IOD(0:15) to IODCBA	10	-	ns
T4B	Data Setup to Latch Enable	20	-	ns
	PD(0:31) to $\overline{\text{WRLE}}$	20	-	ns
T5	Data Hold from Latch Enable	5	-	ns
	D(0:7) from $\overline{\text{RDLE0}}$	5	-	ns
	IOD(0:15) from IODCBA	5	-	ns
	PD(0:31) from $\overline{\text{WRLE}}$	5	-	ns
T6A	Latch Enable Active Pulse Width	15	-	ns
	$\overline{\text{WRLE}}$, $\overline{\text{RDLE0}}$, IODCBA	15	-	ns
T6B	Latch Enable Active Pulse Width	30	-	ns
	$\overline{\text{WRLE}}$, $\overline{\text{RDLE0}}$, IODCBA	30	-	ns
T7	Propagation Delay	-	-	ns
	$\overline{\text{SWPDIR}}$ to D( ) or PD( )	-	30/28	ns
	$\overline{\text{SWPBYT}}$ to D( ) or PD( )	-	28/28	ns
	$\overline{\text{SWPWORD}}$ to D( ) or PD( )	-	28/28	ns

Table 4. Data Buffer Mode Timings (ns)

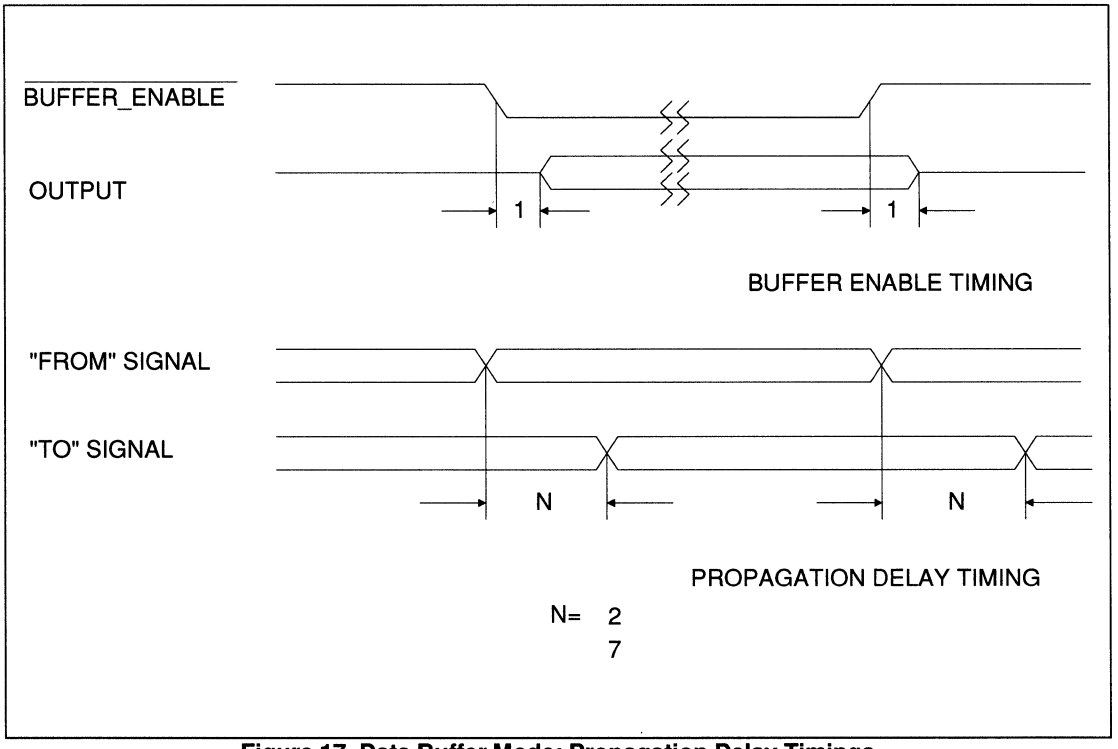


Figure 17. Data Buffer Mode: Propagation Delay Timings

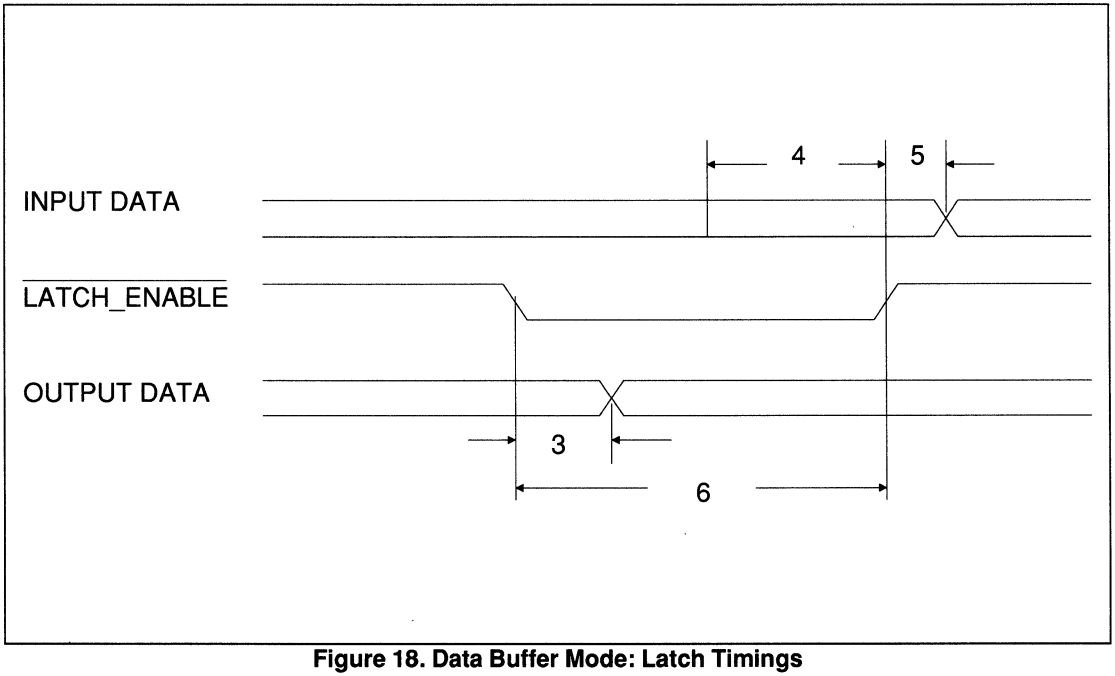


Figure 18. Data Buffer Mode: Latch Timings

14

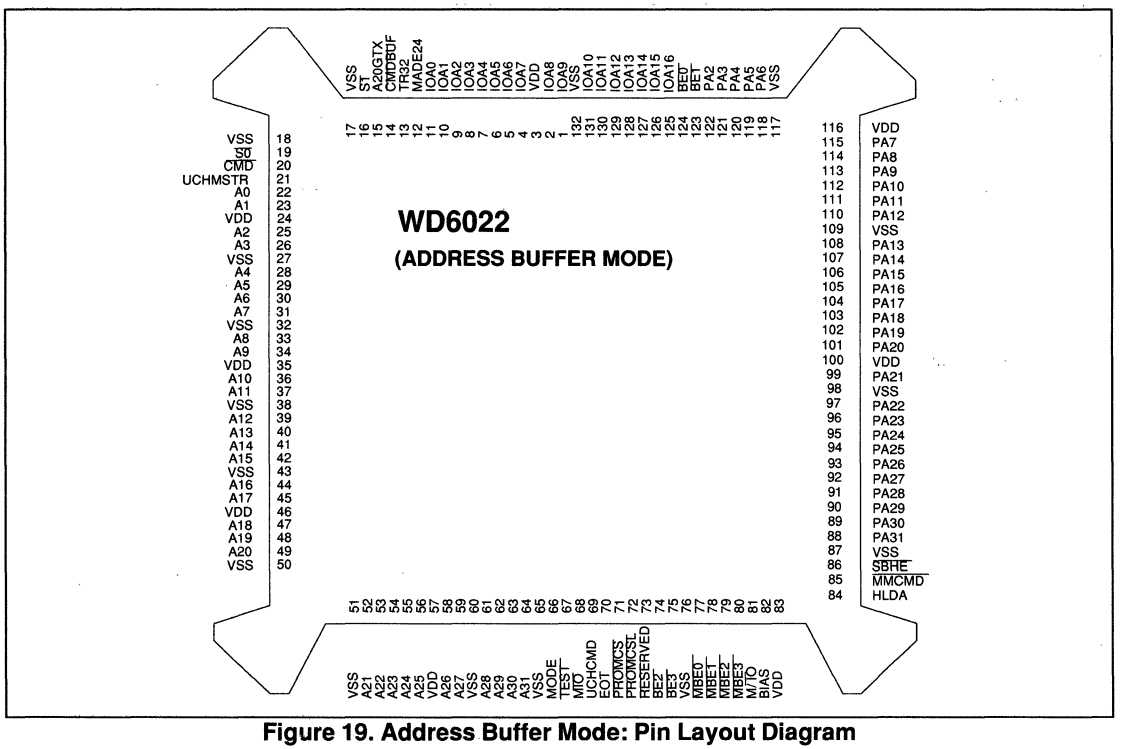


Figure 19. Address Buffer Mode: Pin Layout Diagram

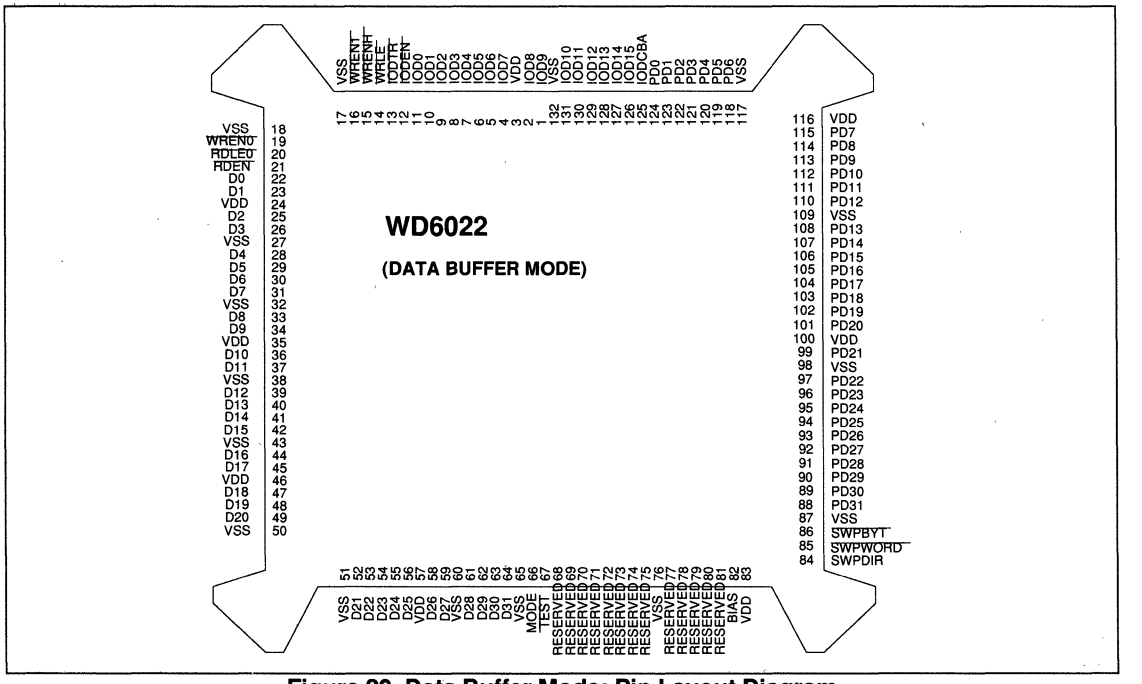


Figure 20. Data Buffer Mode: Pin Layout Diagram

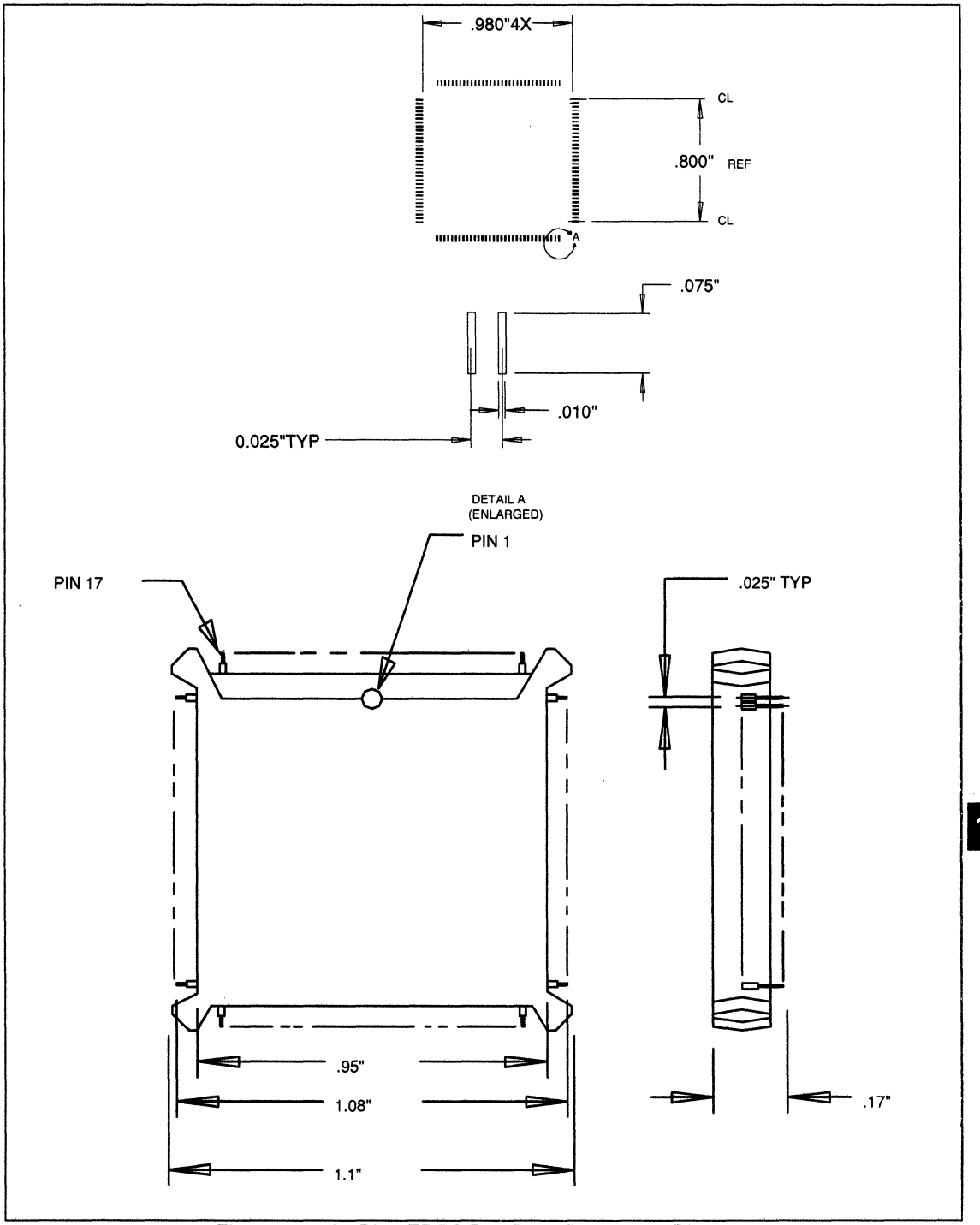
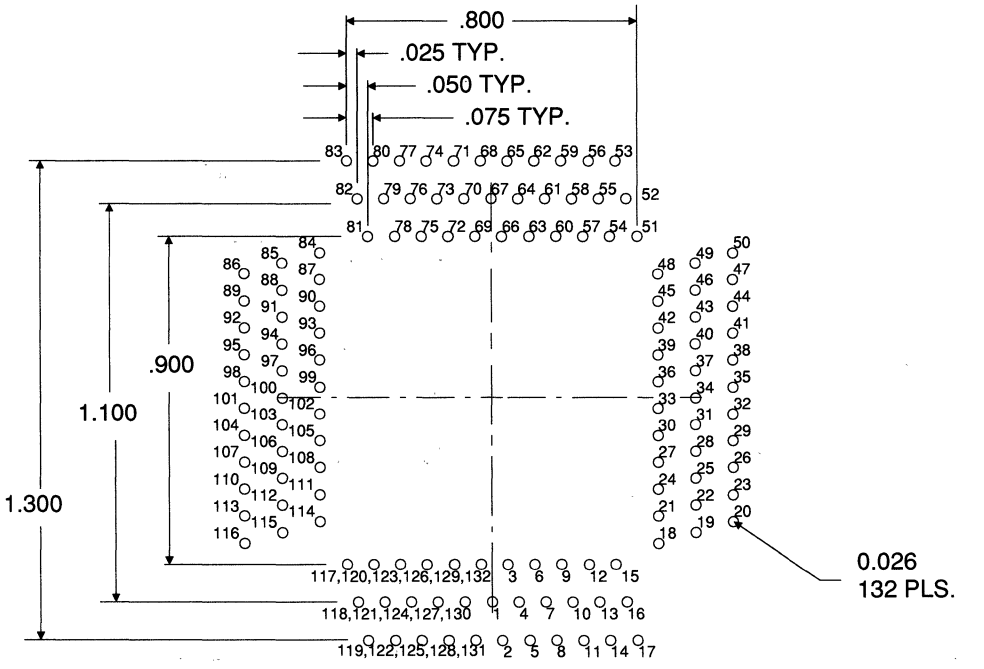


Figure 21. 132-Pin JEDEC Flat Pack Packaging Diagram



RECOMMENDED P.C. BOARD HOLE PATTERN
SOCKET SIDE
132 POSN

Amp Incorporated
Harrisburg PA
Part No. 821932-5

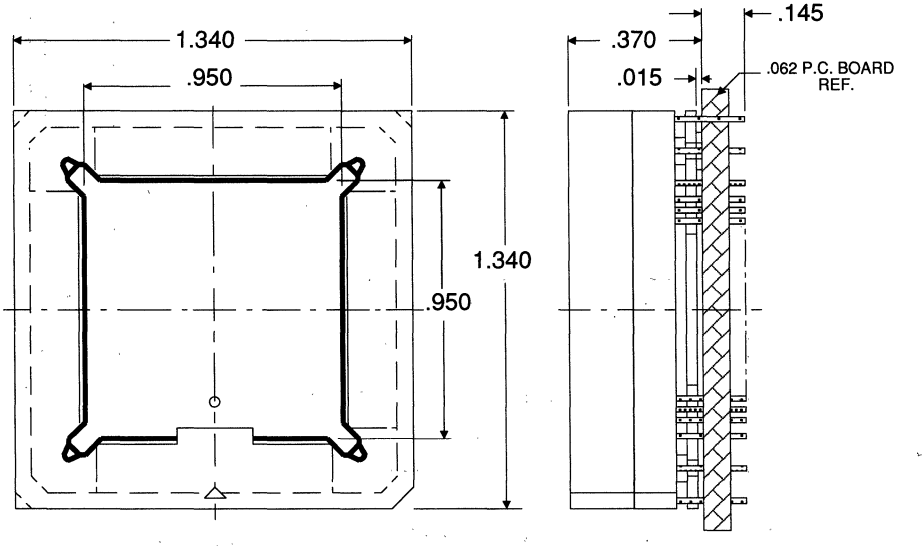


Figure 22. Socket Diagram

SYSTEMS LOGIC/PERIPHERAL

WD6030

Cache/DRAM and

Channel Control Device

15

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

ADDITIONAL REFERENCES

IBM PS/2 Model 70 Technical Reference Manual
IBM PS/2 Model 80 Technical Reference Manual
Intel Microprocessor and Peripheral Handbook

1.0 INTRODUCTION

1.1 DESCRIPTION

The WD6030 integrated circuit forms part of Western Digital's innovative WD6500 chip set. It facilitates the design and implementation of system boards compatible with IBM's Micro Channel architecture, decreases design complexity, saves space by combining the functions of many discrete arrays and components, and reduces system cost and increases system reliability.

The Extended Setup Facility, or ESF, is a Western Digital enhancement designed to allow more functionality such as a Winchester Controller, LAN Adapter, or additional Serial Port to be added onto the system board. It provides product differentiation at the system level and helps reduce costs. The block diagram in Figure 1 illustrates a typical system utilizing the WD6500 chip set. Devices with bold outlines are available from Western Digital Corporation.

1.2 FEATURES

- Hardware (register level) and software compatible to the IBM Personal System/2 Micro Channel implementations
- Direct-Mapped Cache Controller
  - Direct-mapped, write-through implementation
  - Line size equals four bytes
  - Page mode hits on cache misses
- DRAM Controller
  - Memory Configuration Registers
  - Complete 256 KB, 1 MB, and 4 MB DRAM support
  - Ability to mix DRAM sizes in different banks
  - Support for up to four banks (up to 64 M-Bytes) of memory
- Channel Controller
- Channel Buffer Controls
- Programmable Wait States
- Shadow RAM for fast BIOS execution
- Extended Setup Facility (ESF)
- Low Power 0.9 Micron CMOS Technology
- 132-Lead JEDEC Plastic Quad Flat Pack

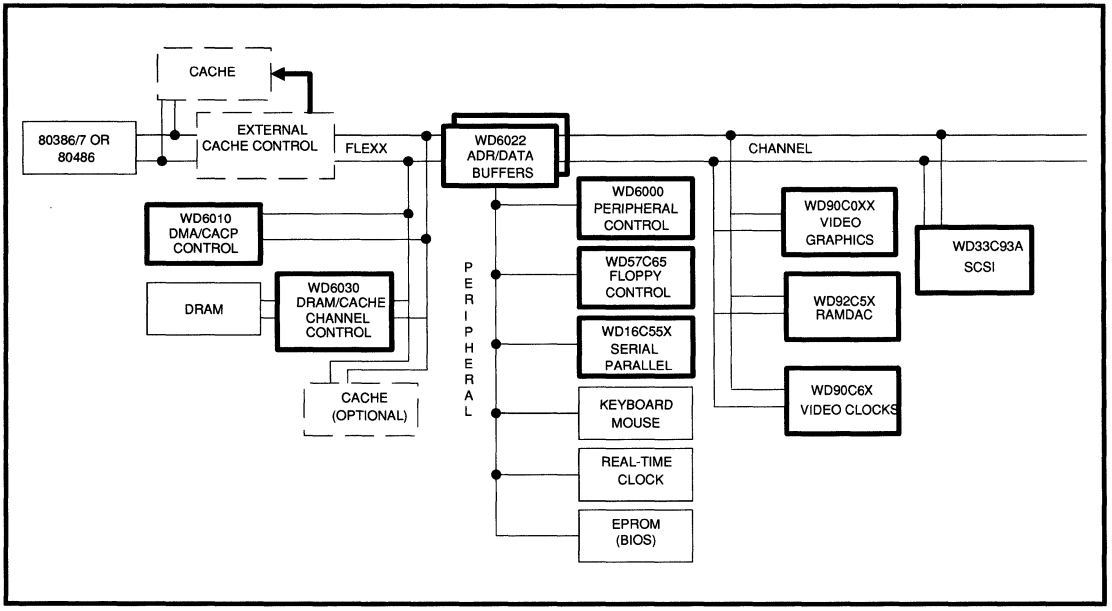


Figure 1. System Block Diagram

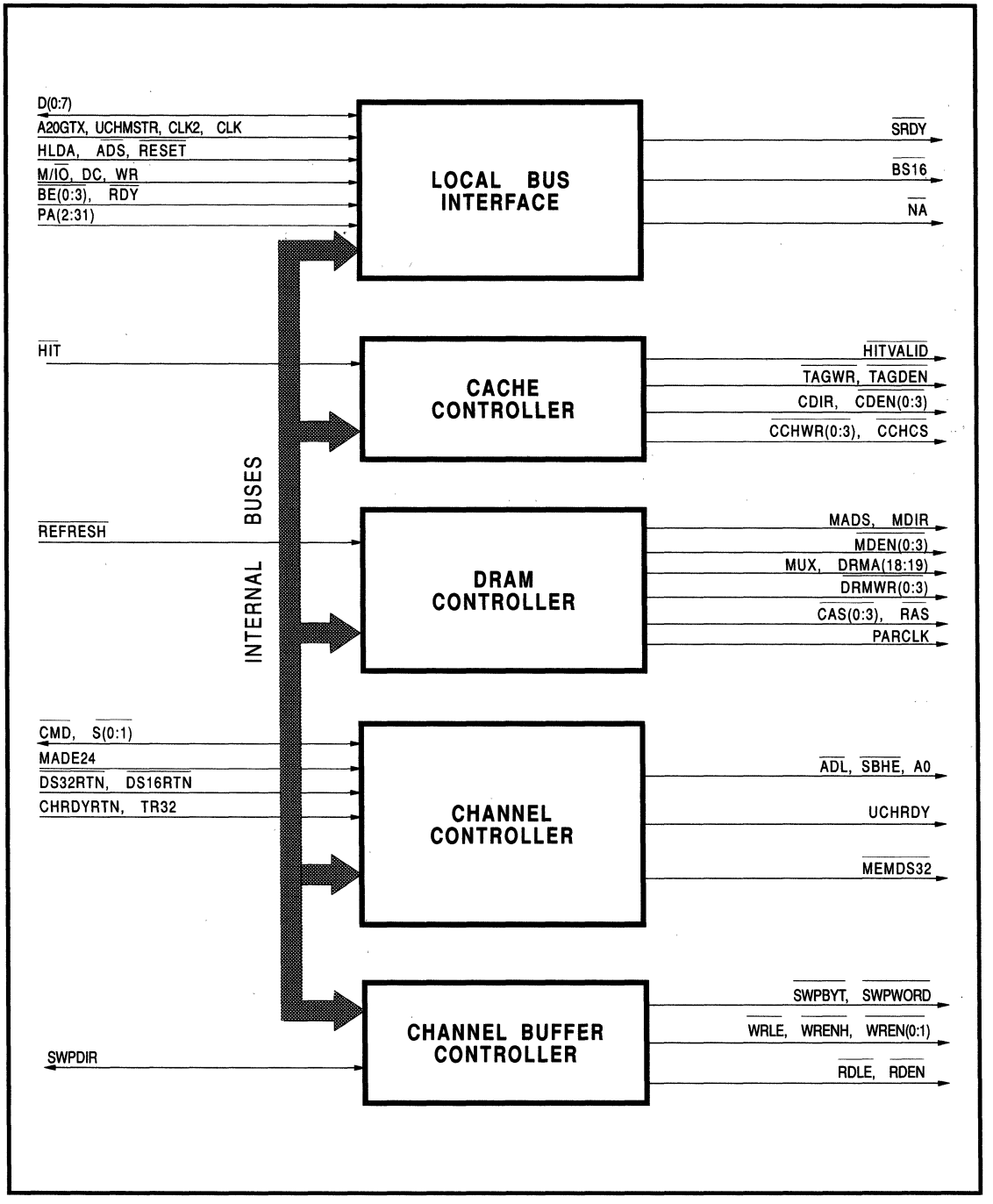


Figure 2. WD6030 Block Diagram

2.0 PIN DESCRIPTION

The signals assigned to different pins are grouped according to their function and discussed individually in Table 1.

2.1 LOCAL BUS INTERFACE

The WD6030 sits directly on the CPU bus, controlling the CPU/DMA accesses to local memory, I/O, and the Channel. The WD6030 also controls Micro Channel master accesses to the local memory.

2.2 CACHE CONTROLLER

The Cache Controller in the WD6030 implements a direct-mapped cache for the 80386, which improves performance significantly by allowing the majority of memory cycles to be run at zero wait states. These signals form part of the interface between the cache controller and the external cache and TagRAMs. See Section 3.0 for a detailed description of the cache controller.

2.3 DRAM CONTROLLER

The DRAM Controller supports Page Mode and allows DRAMs of different sizes to be used together. Pipelined operation, which allows fast accesses to the DRAMs, is also supported.

2.4 CHANNEL CONTROLLER

The Channel controller implements the interface to the system board. The WD6030 generates the Channel interface signals whenever the CPU or the DMA controller accesses any resource on the Channel.

2.5 CHANNEL BUFFER CONTROLLER

The Channel Buffer signals control the data buffers between the local processor data bus and the Channel data bus. The data buffers are integrated in the WD6022 device providing the interface to that device. Note that the WD6022 must be strapped in the Data Buffer Mode.

2.6 MISCELLANEOUS

This set of signals includes the V_{SS} and V_{DD} signal pins, as well as the reserved pins, which should not be connected but left open in the system.

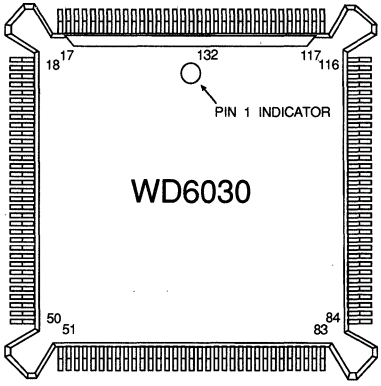


Figure 3. 132-PIN PLASTIC QUAD FLAT PACK

PIN	–	NAME	PIN	–	NAME	PIN	–	NAME	PIN	–	NAME
1	–	PA2	34	–	N.C.	67	–	WREN1	100	–	CDEN2
2	–	PA3	35	–	TR32	68	–	WRENH	101	–	CDEN1
3	–	PA4	36	–	CHRDYRTN	69	–	WRLE	102	–	CDEN0
4	–	PA5	37	–	DS16RTN	70	–	SWPWORD	103	–	CDIR
5	–	PA6	38	–	DS32RTN	71	–	V_{SS}	104	–	TAGWR
6	–	PA7	39	–	V_{DD}	72	–	SWPBYT	105	–	TAGDEN
7	–	PA8	40	–	MEMDS32	73	–	SWPDIR	106	–	V_{SS}
8	–	PA9	41	–	UCHRDY	74	–	RAS	107	–	HITVALID
9	–	PA10	42	–	S0	75	–	CAS0	108	–	SRDY
10	–	PA11	43	–	S1	76	–	CAS1	109	–	MADS
11	–	PA12	44	–	V_{SS}	77	–	CAS2	110	–	RDY
12	–	PA13	45	–	CMD	78	–	CAS3	111	–	HIT
13	–	PA14	46	–	A0	79	–	DRMWR0	112	–	MADE24
14	–	PA15	47	–	SBHE	80	–	DRMWR1	113	–	BE0
15	–	PA16	48	–	ADL	81	–	DRMWR2	114	–	BE1
16	–	PA17	49	–	N.C.	82	–	DRMWR3	115	–	BE2
17	–	V_{SS}	50	–	V_{SS}	83	–	V_{SS}	116	–	V_{SS}
18	–	PA18	51	–	PARCLK	84	–	DRMA19	117	–	BE3
19	–	PA19	52	–	NA	85	–	DRMA18	118	–	W/R
20	–	PA20	53	–	BS16	86	–	MUX	119	–	D/C
21	–	PA21	54	–	D0	87	–	MDEN3	120	–	M/IO
22	–	PA22	55	–	D1	88	–	MDEN2	121	–	ADS
23	–	PA23	56	–	D2	89	–	MDEN1	122	–	V_{DD}
24	–	V_{DD}	57	–	D3	90	–	MDEN0	123	–	REFRESH
25	–	PA24	58	–	V_{SS}	91	–	MDIR	124	–	RESET
26	–	PA25	59	–	D4	92	–	V_{DD}	125	–	HLDA
27	–	PA26	60	–	D5	93	–	CCHCS	126	–	UCHMSTR
28	–	V_{SS}	61	–	D6	94	–	CCHWR3	127	–	A20GTX
29	–	PA27	62	–	D7	95	–	V_{SS}	128	–	N.C.
30	–	PA28	63	–	RDEN	96	–	CCHWR2	129	–	TEST
31	–	PA29	64	–	RDLE	97	–	CCHWR1	130	–	CLK
32	–	PA30	65	–	WREN0	98	–	CCHWR0	131	–	CLK2
33	–	PA31	66	–	VDD	99	–	CDEN3	132	–	V_{SS}

PIN NO.	NAME	TYPE	FUNCTION
			LOCAL BUS INTERFACE
127	A20GTX	I	GATE At power-up, the state of A20GTX is latched at the trailing edge of $\overline{\text{RESET}}$ and, in conjunction with UCHMSTR, determines the frequency at which the WD6030 operates. The following table lists the clock frequencies available. **FREQUENCY / UCHMSTR / A20GTX** 16 MHz / 0 / 0 20 MHz / 0 / 1 25 MHz / 1 / 1 33 MHz / 1 / 0 After power-up, A20GTX is used to wrap around addresses in the Real and Virtual 8086 modes of the processor. The signal is generated by the WD6010 and is a combination of the A20GATE generated by the 8742 and the Alternate Gate A20 signal from Port 0092H, bit 1. The WD6030 uses this signal internally to generate the address for memory accesses. Depending on the frequency configuration required, this signal should be pulled up/down with a 470K resistor.
126	UCHMSTR	I	CHANNEL MASTER At power-up, the state of UCHMSTR is latched at the trailing edge of $\overline{\text{RESET}}$, and in conjunction with A20GTX, determines the frequency at which the WD6030 operates. After power-up, UCHMSTR functions as a signal from the Central Arbitration Control Point (CACP) in the WD6010. When active, it indicates that a Channel master has the bus. A 2.7K resistor is used to pull up/down this signal.
54 - 57 59 - 62	D0 - D7	I/O	CHANNEL DATA BUS The WD6030 internal registers are programmed via the Channel Data Bus. These registers can only be accessed by 8-bit operations. When the registers are accessed, a Channel cycle ($\overline{\text{S0}}$, $\overline{\text{S1}}$, $\overline{\text{CMD}}$, etc.) is initiated, and the controls for the Channel buffers are activated to complete the cycle.
131 130	CLK2 CLK	I I	CLOCKS Both CLK and CLK2 are CMOS level signals. CLK is of the same frequency as the processor clock, while CLK2 is twice the frequency of the processor clock. The WD6030 shares CLK2 with the CPU.
125	HLDA	I	HOLD ACKNOWLEDGE HLDA indicates that the CPU has given control of the system local bus to a different master (Channel Bus Master or DMA Controller). HLDA prevents non-system CPU accesses to locations 0000-00FFH in the WD6000 during master cycles.

Table 1. Pin Description

15

PIN NO.	NAME	TYPE	FUNCTION
124	$\overline{\text{RESET}}$	I	$\overline{\text{RESET}}$ $\overline{\text{RESET}}$ is driven by the WD6010 and is asserted at power-on. It initializes all internal state machines and registers to the power-up default values.
121	$\overline{\text{ADS}}$	I	$\overline{\text{ADDRESS STROBE}}$ The WD6030 uses $\overline{\text{ADS}}$ to keep track of bus cycles on the CPU address, data, and status busses.
120 119 118	M/$\overline{\text{IO}}$ D/$\overline{\text{C}}$ W/$\overline{\text{R}}$	I	MEMORY $\overline{\text{I/O}}$, DATA/$\overline{\text{CONTROL}}$, WRITE/$\overline{\text{READ}}$ The M/IO, D/C, and W/R signals define the type of bus cycle being executed on the CPU local bus. When the CPU is in control of the CPU local bus, M/IO, D/C, and W/R are input from the CPU. When the WD6010 DMA Controller is in control of the CPU local bus, M/IO, D/C, and W/R are input from the WD6010.
117 115 114 113	$\overline{\text{BE3}}$ $\overline{\text{BE2}}$ $\overline{\text{BE1}}$ $\overline{\text{BE0}}$	I	$\overline{\text{BYTE ENABLES}}$ These Byte-Enable signals are driven by the CPU, the WD6010 DMA controller, or the Channel master.
110	$\overline{\text{RDY}}$	I	$\overline{\text{READY}}$ The Ready signal is used to track bus cycles on the CPU local bus. The $\overline{\text{READY}}$ signals from the chip set are combined externally to generate one $\overline{\text{RDY}}$ signal to the CPU.
1 - 16 18 - 23 25 - 27 29 - 33	PA2 - PA17 PA18 - PA23 PA24 - PA26 PA27 - PA31	I	PROCESSOR ADDRESS BUS PA2 through PA31 is the local processor address bus on the motherboard and interfaces directly with the 80386/80486 address bus. This address bus is driven by the CPU, DMA Controller, or a Channel Master.
108	SRDY	O	SYSTEM READY The WD6030 generates a READY signal for system resources not on the local bus, including the local DRAM. The SRDY signal is generated whenever the 80386, 80486, or DMA Controller performs a bus cycle that is neither an access to the numeric coprocessor (80387 or Weitek 3167) nor a memory access resulting in a cache hit. This signal is logically ORed on the system board with the other sources of READY to generate READY to the CPU. Note that the default for the READY signal to the 80386, 80486, or DMA Controller is a "not ready" interface.

M/$\overline{\text{IO}}$	D/$\overline{\text{C}}$	W/$\overline{\text{R}}$	WD6030 OPERATION
0	0	0	Reserved
0	0	1	Reserved
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Memory Code Read
1	0	1	Reserved
1	1	0	Memory Read
1	1	1	Memory Write

Table 1. Pin Description (Continued)

PIN NO.	NAME	TYPE	FUNCTION
53	BS16	O	BUS SIZE 16 BS16 is used to indicate whether the CPU or WD6030 is accessing a 32-bit, 16-bit, or 8-bit port. When a 32-bit port is accessed, BS16 is de-asserted and all byte enables should be active. When a 16-bit or 8-bit port is accessed, BS16 is asserted and the byte enables are sampled to determine whether the access is to a 16-bit or 8-bit port.
52	NA	O	NEXT ADDRESS The Next Address signal is asserted when a pipelined cycle can be supported by the system. The WD6030 requests a pipeline cycle whenever a cycle other than a Cache-Read-Hit occurs.
			CACHE CONTROLLER
111	HIT	I	CACHE HIT The external tag subsystem sends this signal to the WD6030 to indicate that the current cycle resulted in a match of the Tag. Depending on whether or not the DRAM cycle can be cached, this signal is internally qualified to generate a cache hit indication. If a cache hit occurs on a memory read cycle, a zero wait state operation is accomplished.
107	HITVALID	O	CACHE HIT QUALIFIER The WD6030 asserts the HITVALID signal to indicate that the HIT signal from the tag subsystem is valid and can be sampled by the external logic. HIT and HITVALID are logically ANDed externally to assert the READY signal to the 80386, 80486, or DMA Controller, resulting in a zero wait state cycle on a Cache-Read-Hit. For a cycle requiring a cache update, HIT may be inactive in the early part of the cycle and active in the latter part when the Tag is updated. HITVALID is de-asserted in the latter part of the cycle to prevent generating a spurious READY signal to the CPU.
105	TAGDEN	O	TAG DATA ENABLE TAGDEN opens a "Tag Buffer", such as a 74F244, during a Tag update cycle. Tag updates occur on a Cache-Miss cycle on cachable memory areas.
104	TAGWR	O	TAG WRITE TAGWR updates the Tag in the TagRAM for a Cache-Update cycle. A pipelined cycle is requested and TAGWR updates the Tag value when a Cache-Miss occurs.
103	CDIR	O	CACHE BUFFER DIRECTION CDIR determines the direction of the data flow between the Processor Data Bus (PD) and Cache Data Bus (CD) for the 74F245 buffers. The 74F245 buffers minimize the loading on the CPU local bus and permit more relaxed timings on the Cache Data SRAMs. The 74F245 buffers also permit the use of SRAMs which do not require the Output Enable function. **CDIR** **Direction** 0 CD(0:31) to PD(0:31) 1 PD(0:31) to CD(0:31)

Table 1 Pin Description (Continued)

15

PIN NO.	NAME	TYPE	FUNCTION
102 101 100 99	CDEN0 CDEN1 CDEN2 CDEN3	O	CACHE BUFFER ENABLES CDEN(0:3) provides the enable signals for the 74F245 buffers between the Processor Data Bus (PD) and the Cache Data Bus (CD). Each data byte has a separate enable which is qualified internally by the byte enable from the 80386, 80486, or DMA Controller. Figure 4 illustrates a typical cache cycle with page hits.
98 97 96 94	CCHWR0 CCHWR1 CCHWR2 CCHWR3	O	DATA CACHE WRITE CCHWR(0:3) individually enables each of the four bytes of the cache data. The WD6030 asserts the write signal corresponding to the byte enable asserted during the cycle.
93	CCHCS	O	DATA CACHE CHIP SELECT CCHCS is the Chip Select signal to the Cache Data SRAMs. CCHCS is always asserted at the beginning of a cycle, permitting the slowest possible SRAMs to be used. CCHCS is only de-asserted for a cache update operation.
			DRAM CONTROLLER
123	REFRESH	I	REFRESH REFRESH from the WD6010 indicates that a Refresh cycle is in progress and a Memory Read cycle is taking place run on the local bus. When REFRESH is asserted, the DRAM controller initiates a RAS-only cycle, with the address supplied by the WD6010. Simultaneously, a Memory Read cycle is initiated on the Channel. A READY signal is generated when both cycles have been completed.
109	MADS	O	MEMORY ADDRESS STROBE The MADS signal from the WD6030 latches all addresses for the external cache data and DRAM to the external address latches 74AS373. Figures 5 through 8 illustrate a typical cycle to the DRAM.
91	MDIR	O	DRAM BUFFER DIRECTION MDIR determines the direction of the data flow for the 74F657 bidirectional transceivers between the Processor Data Bus (PD), and the DRAM Data Bus (MD). **MDIR** **Direction** 0 MD(0:31) to PD(0:31) 1 PD(0:31) to MD(0:31)
90 89 88 87	$\overline{\text{MDEN0}}$ $\overline{\text{MDEN1}}$ $\overline{\text{MDEN2}}$ $\overline{\text{MDEN3}}$	O	$\overline{\text{DRAM BUFFER ENABLES}}$ $\overline{\text{MDEN}}$(0:3) are the enable signals for the 74F657 transceivers between the Processor Data Bus (PD) and DRAM Data Bus (MD). Each data byte has its own enable which is qualified internally by the byte enables from the 80386, 80486, or DMA Controller.

Table 1 Pin Description (Continued)

PIN NO.	NAME	TYPE	FUNCTION
86	MUX	O	ADDRESS MULTIPLEXER MUX interfaces with the external address multiplexers and controls the generation of the row and column addresses to the DRAM. **MUX** **Function** 0 Row Address 1 Column Address
85 84	DRMA18 DRMA19	O	DRAM SPLIT MEMORY ADDRESS DRMA(18:19) provide Address Bits 18 and 19 for DRAM accesses, which are sent to the external DRAM address multiplexers. These signals implement the split addressing memory feature.
82 81 80 79	DRMWR3 DRMWR2 DRMWR1 DRMWR0	O	DRAM WRITE DRMWR(3:0) are the enable signals to the system DRAM. Each data byte has a separate enable which is internally qualified by the byte enables from the 80386, 80486, or DMA Controller. The four write enable signals to the DRAM should be buffered by a 74AS1832.
78 77 76 75	CAS3 CAS2 CAS1 CAS0	O	DRAM CAS Each of the four banks has its own CAS signal. The bank being accessed has its CAS signal asserted during a cycle. At the end of the cycle, all CAS signals are de-asserted. These signals should be buffered by a 74AS1832. Page Mode DRAMs can be employed because the WD6030 de-asserts this signal at the end of each cycle. Static Column DRAMs may also be used, however, they will operate in Page Mode.
74	RAS	O	DRAM RAS RAS connects to the RAS inputs of all the DRAMs and should be buffered by a 74AS1832. This signal is active in Page Mode as long as the accesses remain within the same row. RAS remains active even if the accesses are made to addresses in different memory banks which share the same row address, because the row addresses are shared by the different memory banks. In normal RAS/CAS Mode, a RAS precharge takes place for every DRAM access.
51	PARCLK	O	PARITY ERROR CLOCK PARCLK is used as a clock to latch in parity error information during DRAM read cycles. At the rising edge of this signal, the parity error information is latched in. The Parity Error Latch function is implemented on the system board.
			CHANNEL CONTROLLER
45	CMD	I/O	COMMAND CMD defines when data to or from the Channel is valid. CMD is an input during Channel Master Cycles and an output during all other cycles.
43 42	S1 S0	I/O	CHANNEL STATUS S1 and S0, along with M/IO, identify the type of cycle taking place on the channel. S1 and S0 are input signals during a Channel Master Cycle and an output during all other cycles.

Table 1 Pin Description (Continued)

PIN NO.	NAME	TYPE	FUNCTION
112	MADE24	I	MEMORY ADDRESS ENABLE 24 MADE24 is asserted by the channel when an address greater than 16 Mbytes is placed on the Processor Address Bus (PA). The WD6022 Address Buffer Device de-asserts MADE24 whenever the CPU or DMA Controller performs a Channel Memory access above the 16 Mbyte boundary.
38	DS32RTN	I	DATA SIZE 32 RETURN DS32RTN corresponds to, and directly interfaces with, the DS32RTN signal on the Channel and is generated by ORing all the CDDS32N signals on the Channel. Asserting DS32RTN during a Channel cycle indicates that the slave being addressed is capable of transferring 32 bits of data.
37	DS16RTN	I	DATA SIZE 16 RETURN DS16RTN corresponds to, and directly interfaces with, the DS16RTN signal on the Channel and is generated by ORing all the CDDS16N signals on the Channel. Asserting DS16RTN during a Channel cycle indicates that the slave being addressed is capable of transferring 16 bits of data.
36	CHRDYRTN	I	CHANNEL READY RETURN CHRDYRTN is an AND of all CDCHRDY signals present on the Channel, i.e., the individual Channel slots, video subsystem, WD6000 (IORDY) and the system board DRAM (UCHRDY). A Channel slave uses CHRDYRTN to extend the Channel cycle.
35	TR32	I	TRANSLATE 32 TR32 facilitates communication between a 16-bit master and a 32-bit slave. TR32 generates the necessary control signals used in data swapping. When asserted, it indicates that a 16-bit master has the Channel and that the Central Translator function should be turned on. The CPU and DMA Controller are 32-bit masters, therefore, the WD6022 de-assertes TR32 when the Channel is accessed by the CPU or DMA Controller.
48	ADL	O	ADDRESS DECODE LATCH ADL provides the slave with an appropriate method to latch valid addresses and status signals.
47 46	SBHE A0	O	SYSTEM BYTE HIGH ENABLE ADDRESS BIT 0 SBHE and A0 are used by 16-bit slaves to determine the byte that contains data during the current transfer of data. **A0 SBHE DATA AVAILABLE** 0 0 D(0:15) 0 1 D(0:7) 1 0 D(8:15) 1 1 Reserved Note that this signal is not used by 8-bit or 32-bit slaves. The latter uses BE(0:3) signals to perform the same function.

Table 1 Pin Description (Continued)

PIN NO.	NAME	TYPE	FUNCTION
41	UCHRDY	O	LOCAL DRAM CHANNEL READY UCHRDY is used to extend cycles when a Channel Master accesses the system board DRAM. UCHRDY is also used in the external logic to generate CHRDYRTN. Figures 9 through 12 indicate typical Channel Master cycles to the system board DRAM.
40	$\overline{\text{MEMDS32}}$	O	LOCAL DRAM MEMORY SIZE 32 $\overline{\text{MEMDS32}}$ is used in external logic on the system board to generate the $\overline{\text{DS16RTN}}$ and $\overline{\text{DS32RTN}}$ signals. $\overline{\text{MEMDS32}}$ is driven by the WD6030 when a Channel Master accesses the system board DRAM and indicates that the memory accessed is 32 bits wide.
			CHANNEL BUFFER CONTROLLER
73	SWPDIR	I/O	SWAP DIRECTION At power-up, the state of SWPDIR is latched by the trailing edge of RESET to determine the presence or absence of the numeric processor. **SWPDIR** **RESET STATE FUNCTION** 0 Numeric coprocessor present 1 Numeric coprocessor absent After power-up, SWPDIR indicates the direction of the byte and word swap buffers. SWPDIR de-asseted indicates a read operation, byte swap D(0:7) to D(8:15) or a Channel Master write operation, word swap D(0:15) to D(16:31). SWPDIR asserted indicates a write operation, byte swap D(8:15) to D(0:7) or a Channel Master read operation, word swap D(16:31) to D(0:15).
72	SWPBYT	O	BYTE SWAP When the CPU or DMA accesses an 8-bit port, the cycle is split into two. This signal is used to swap data to the correct bytes. D(0:7) is swapped to D(8:15) for a read and normal operation D(8:15) is swapped to D(0:7) for a write operation
70	SWPWORD	O	WORD SWAP SWPWORD swaps words when a 16-bit Channel Master communicates with a 32-bit slave. The cycle is split into two and SWPWORD is used to swap data to the correct word. D(16:31) is swapped to D(0:15) for a Channel Master read operation, D(0:15) is swapped to D(16:31) for a Channel Master write operation. This function is known as steering.
69	WRLE	O	WRITE LATCH ENABLE WRLE latches the write data during a CPU or DMA write operation to the Channel. It provides the write-data-hold time required by the Channel during these operations. WRLE also latches data when the CPU or DMA writes to an 8-bit port and the cycle must be split in two.

Table 1 Pin Description (Continued)

PIN NO.	NAME	TYPE	FUNCTION
68 67 65	WRENH WREN1 WREN0	O	WRITE ENABLE (HIGH, 0:1) These signals enable the buffer during data flow from the Processor Data Bus (PD) to the Channel Data Bus (D). These signals control byte 0 (0:7) (WREN0), byte 1 (8:15) (WREN1), and the upper word (16:31) (WRENH). These signals are valid when the CPU or DMA controller performs a write operation to the Channel or when a Channel Master performs a read operation from the system board DRAM.
64	$\overline{\text{RDLE}}$	O	$\overline{\text{READ LATCH ENABLE}}$ $\overline{\text{RDLE}}$ is the latch enable signal for byte 0 (0:7). When the CPU or DMA controller performs a cycle to an 8-bit device on the Channel, the cycle is split in two. This signal latches the first 8 bits (0:7) during the first cycle, reads the next 8 bits (8:15) during the second cycle, and then presents the 16 bits to the CPU.
63	$\overline{\text{RDEN}}$	O	$\overline{\text{READ ENABLE}}$ $\overline{\text{RDEN}}$ enables the buffer for the Processor Data Bus (PD) when the data flows from the Channel Data Bus (D) to the Processor Data Bus (PD). $\overline{\text{RDEN}}$ is asserted when the CPU or DMA controller performs a read from the Channel or when a Channel Master writes to the system board DRAM.
			MISCELLANEOUS
24, 39, 66, 92, 122	V_{DD}	I	+5 V Power Supply
17, 28, 44, 50, 58, 71, 83, 95, 106, 116, 132	V_{SS}	I	0 V Ground
34, 49, 128	N.C.		Not connected
129	$\overline{\text{TEST}}$	I	$\overline{\text{TEST PIN}}$ This is an active low signal that facilitates board-level testing. When low, this signal tri-states all outputs and bidirectional signal lines, allowing an ATE tester to drive these signals. When high, the outputs and bidirectional lines are enabled by the WD6030.

Table 1 Pin Description (Continued)

Table 2 details the state of the pins on the WD6030 after a reset.

SIGNAL	BUS STATE AFTER RESET
D (0:7)	Z*
NA, BS16	High
S (0:1), ADL, CMD	High
SBHE, A0	High
MEMDS32	High
UCHRDY, SRDY	High
MADS	High
HITVALID	High
CCHCS	High
CDIR, MDIR	Low
CCHWR (0:3), CDEN (0:3)	High
TAGWR, TAGDEN	High
RAS, CAS (0:3)	High
MUX, PARCLK	Low
DRMWR (0:3)	High
DRMA (18:19)	High
MDEN (0:3)	High
RDEN	High
RDLE	Low
WREN (0:1), WRENH	High
WRLE	Low
SWPBYT, SWPWORD	High
SWPDIR	High
* Z = High Impedance	

Table 2. Pin State After Reset

15

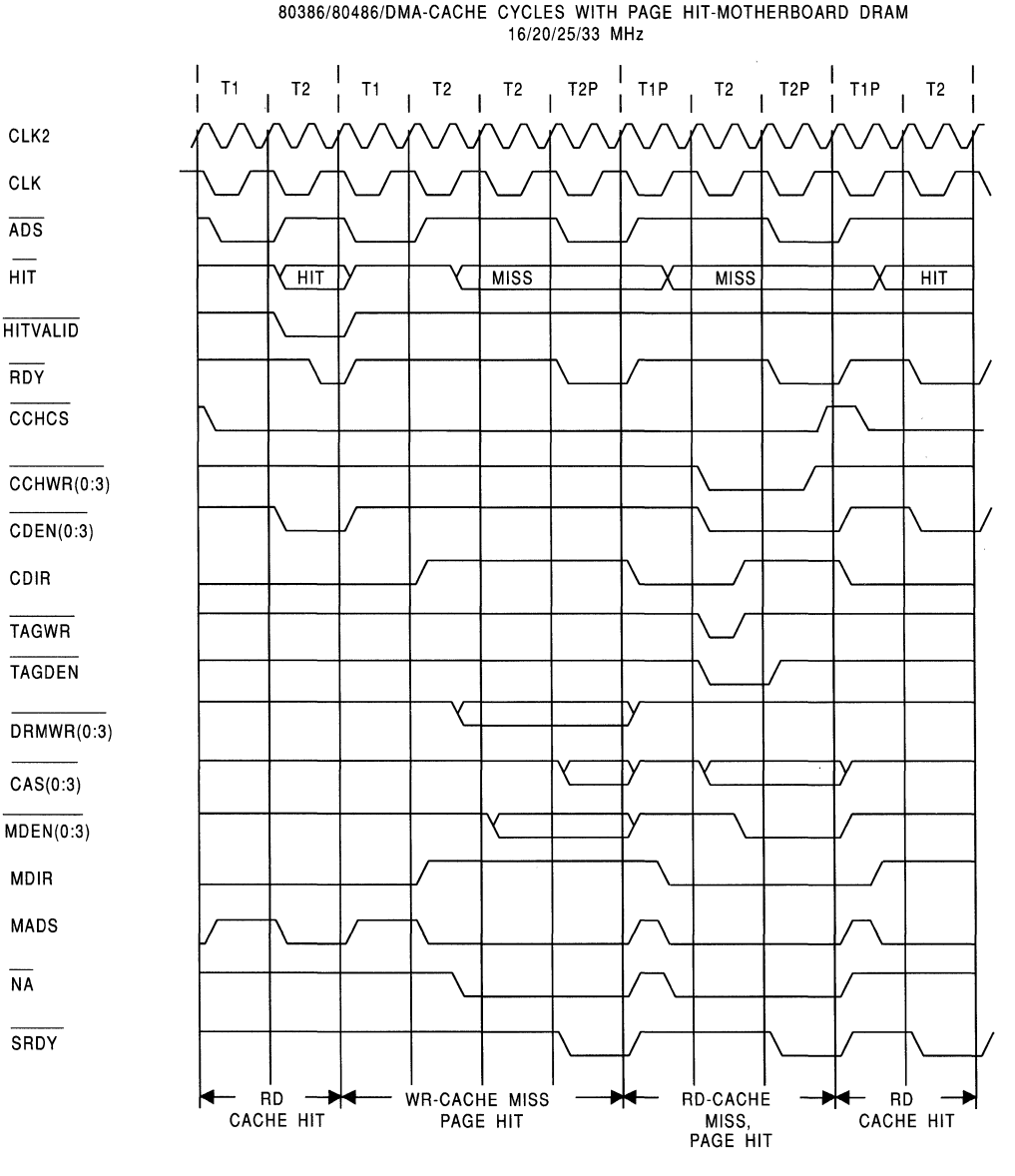


Figure 4. Cache Cycle with Page Hits

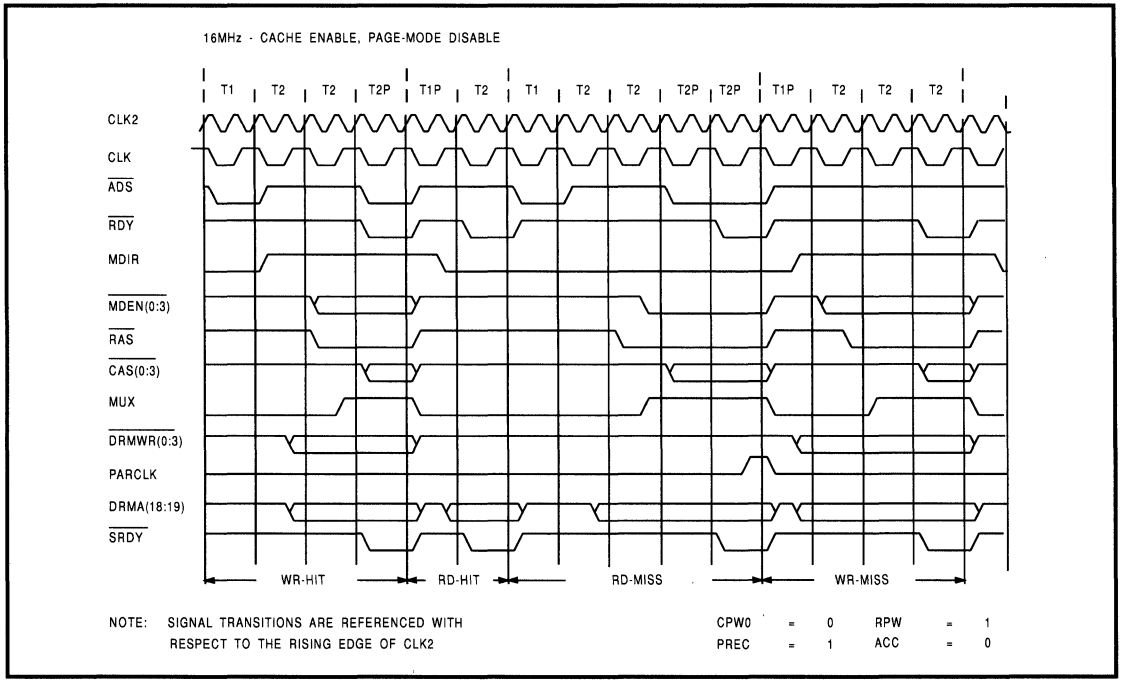


Figure 5. 80386/80486/DMA 16 MHz DRAM Access

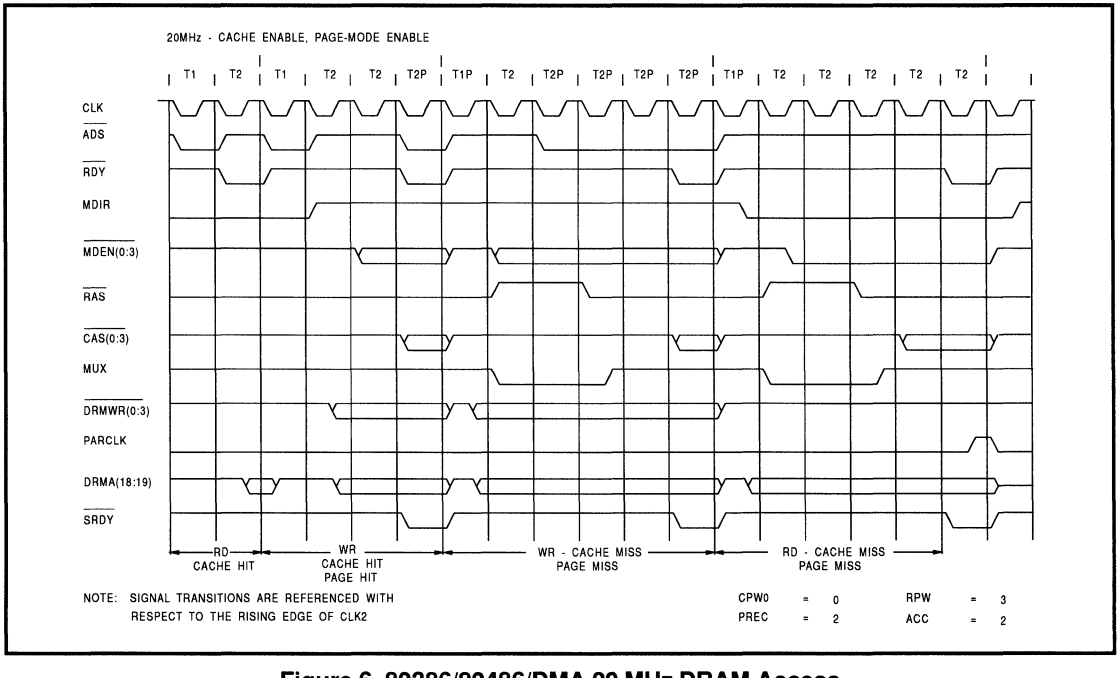


Figure 6. 80386/80486/DMA 20 MHz DRAM Access

15

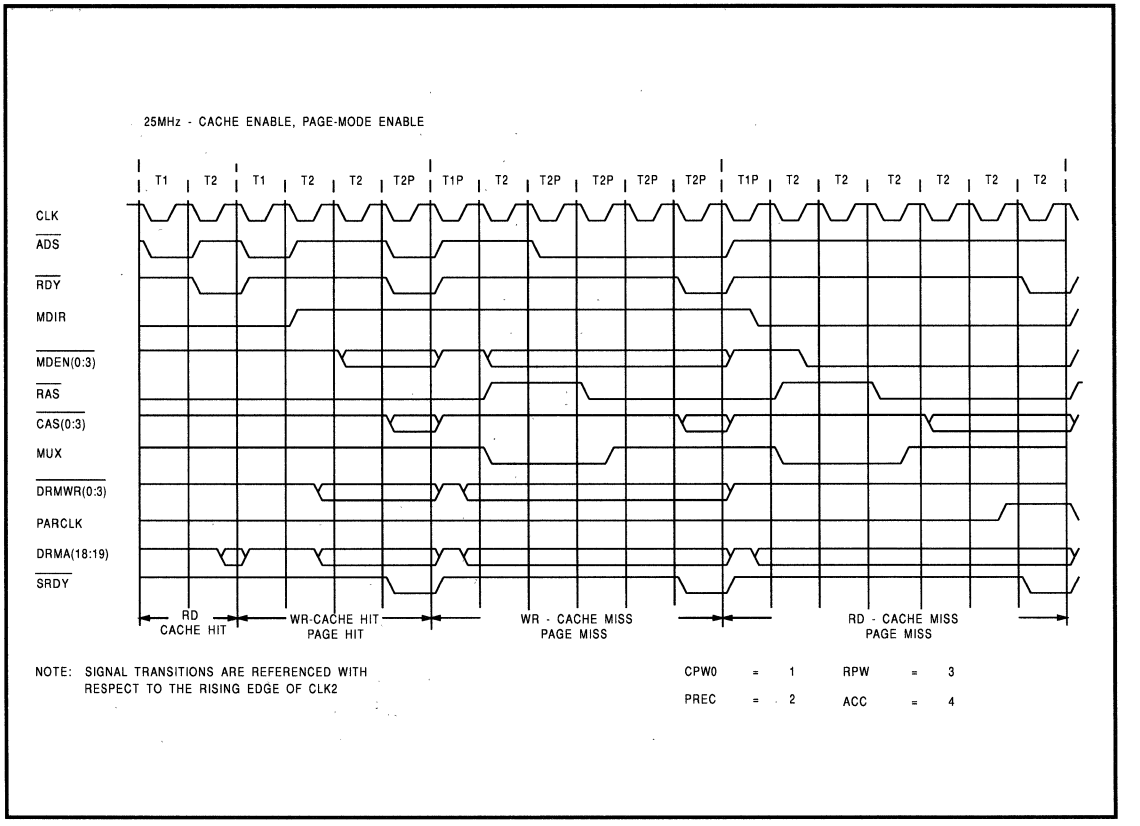
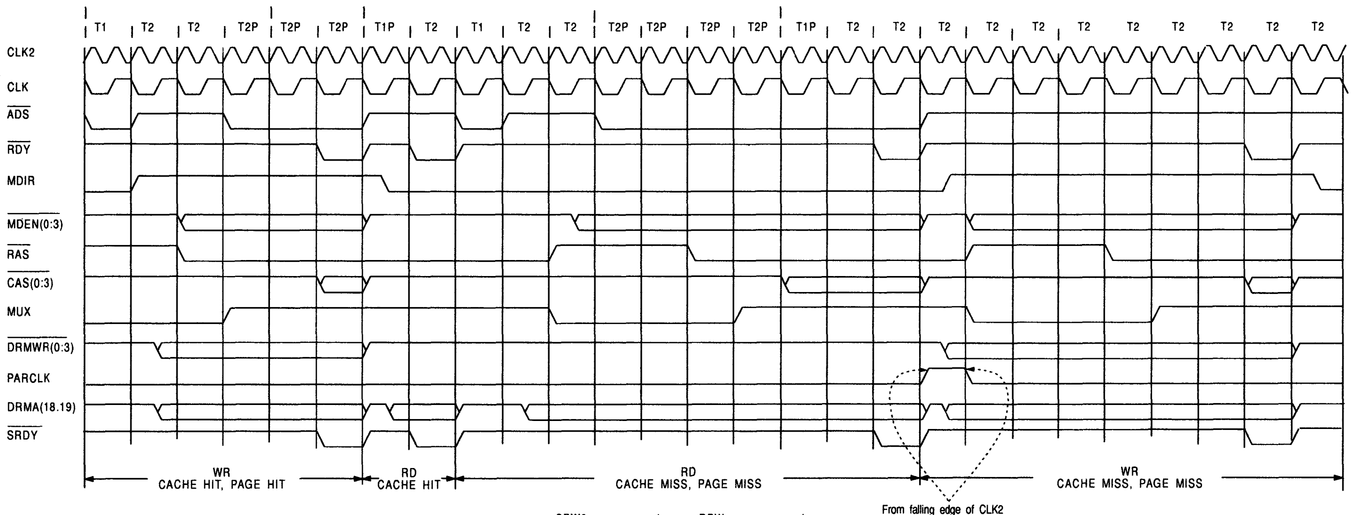


Figure 7. 80386/80486/DMA 25 MHz DRAM Access

Figure 8. 80386/80486/DMA 33 MHz DRAM Access

33 MHz - CACHE ENABLE, PAGE-MODE ENABLE



NOTE: SIGNAL TRANSITIONS ARE REFERENCED WITH RESPECT TO THE RISING EDGE OF CLK2

CPW0	=	1	RPW	=	4
PREC	=	4	ACC	=	5

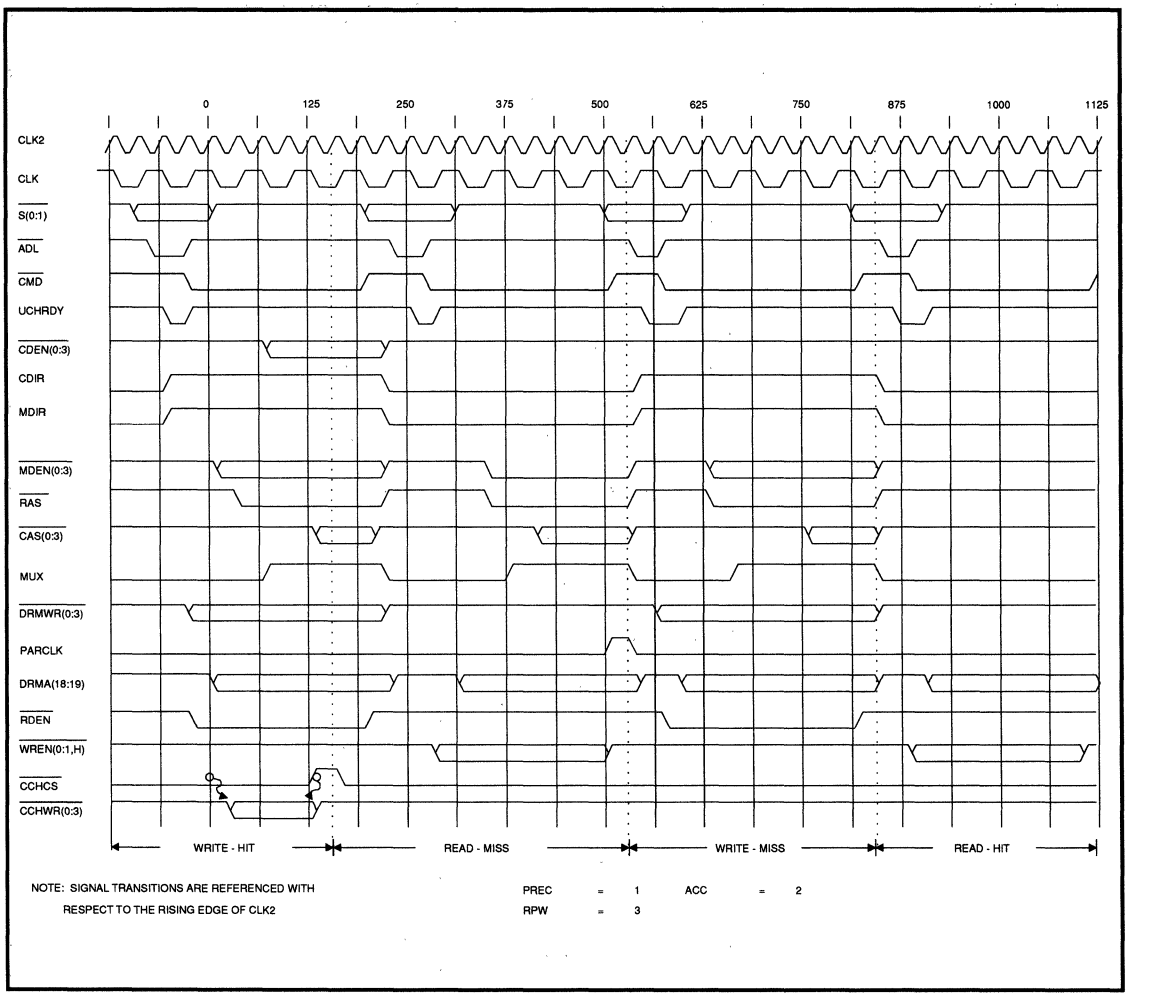


Figure 9. 16 MHz Synchronous Extended Master Cycle

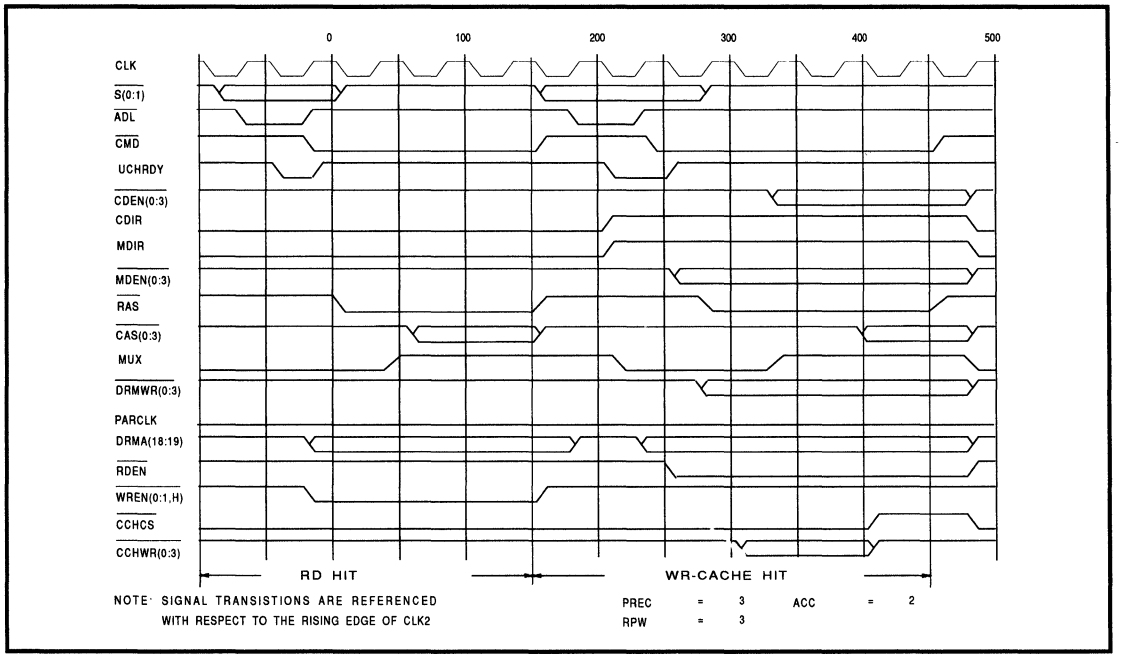


Figure 10. 20 MHz Sysnchronous Extended Master Cycle

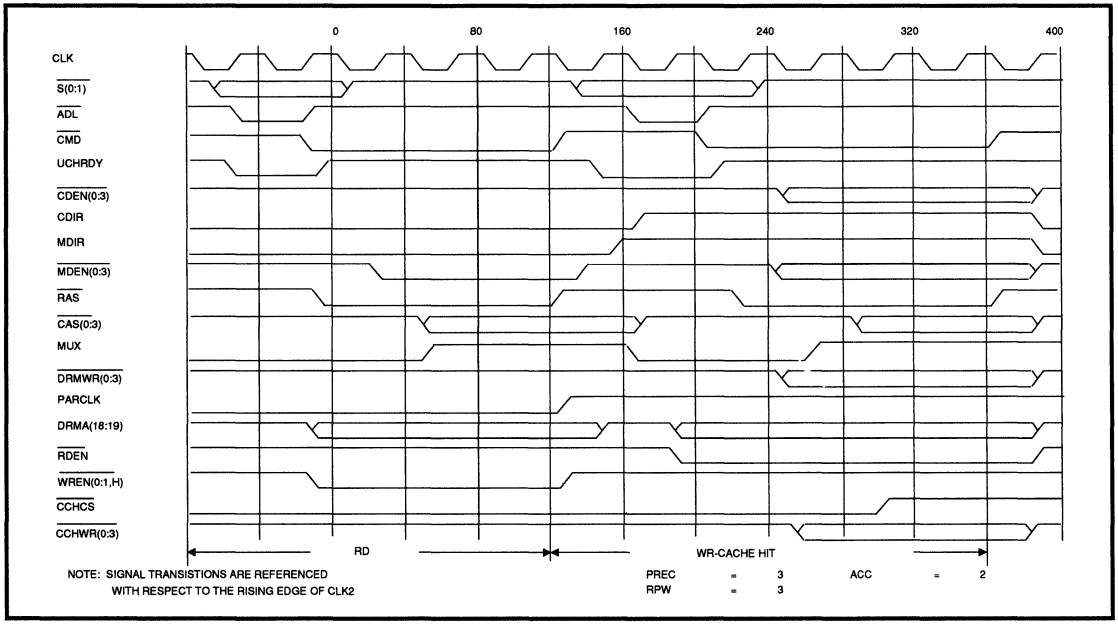


Figure 11. 25 MHz Synchronous Extended Master Cycle

15

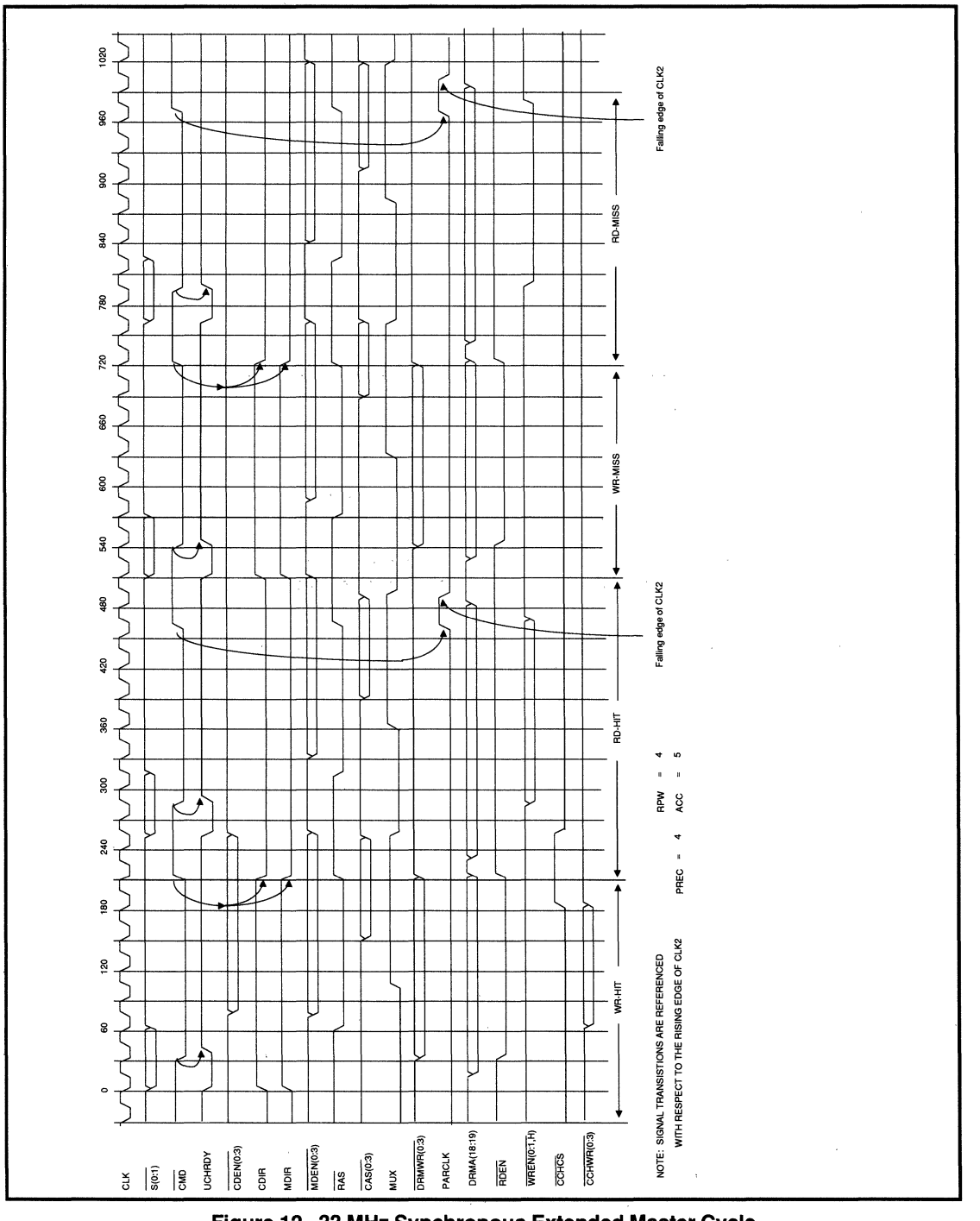


Figure 12. 33 MHz Synchronous Extended Master Cycle

3.0 DRAM CONTROLLER

3.1 MEMORY ORGANIZATION

The WD6030 supports up to four banks of DRAMs, each consisting of 36 bits, with each byte having an associated parity bit. The total memory capacity on the system board is dependent on the type of memory used and the number of banks populated, and could range from 1 MB to 64 MB. Table 3 lists the memory size options that are available.

DRAM TYPE	MEMORY CAPACITY
256K x 1	1 MB x (Number of Banks)
1M x 1	4 MB x (Number of Banks)
4M x 1	16 MB x (Number of Banks)

Table 3. Memory Size Options

The Model 80-071 provides two banks, each with 1 MB of memory. The Model 80-111 has two banks of 2 MB each. The WD6030 default setting at power-up is compatible with the Model 80-071 and Model 80-111: two 1 MB memory banks. The Extended Setup Facility feature can be used to enable more memory on the board.
Each of the banks can be enabled or disabled by programming the Memory Configuration Register. In addition, banks can be swapped, in order to map around defective memory banks.

The WD6030 permits DRAMs of different sizes to be used in the four banks. However, all the DRAMs within a bank should be of the same size. For example, if Bank 0 were composed of 1M x 1 DRAMs, Bank 1 of 256K x 1 DRAMs, and Banks 2 and 3 were unpopulated, this would be a valid use of different-sized DRAMs. Certain restrictions that apply to mixing DRAM sizes should be noted carefully:

- The WD6030 does not support Page Mode operation when DRAMs of different sizes are used in different banks; therefore, in such cases, the DRAMs must be set in Forced Row Misses Mode through the Memory Configuration register. This will result in degraded performance when compared to Page Mode operation for the DRAMs.
- When using a mixture of DRAM sizes, always place the larger-sized DRAMs in the lower banks, or the system will not function. A system populating three banks with 4M x 1, 1M x 1, and 256K x 1 DRAMs should organize them such that Bank 0 consists of 4M x 1, Bank 1 of 1M x 1, and Bank 2 of 256K x 1 DRAMs, with Bank 3 unpopulated.
- When DRAMs of different sizes are used together and the Split RAM is placed in the memory map, the BIOS must ensure that the split RAM starting address is located at an address that is a multiple of the largest DRAMs. Thus, for 4M x 1 DRAMs, it should be located at a 16 Mbyte boundary, for 1M x 1 DRAMs at a 4 Mbyte boundary, for 256K x 1 DRAMs on a 1 Mbyte boundary. See Section 2.1.2.4 for further information.

When the DRAMs are used in Page Mode, the following address assignments should be used for the external multiplexers. REF refers to the addresses for Refresh Cycles. The DA bus is the address bus for the physical DRAM. RAS, CAS, and REF are from the MA or Latched Memory Addresses Bus.

When DRAMs of different sizes are used in the banks, the following address assignments are recommended for use with the external multiplexers. Other address assignments may be used; however, care should be taken to ensure that the addressing for the smaller DRAMs is a subset of the addressing for the larger DRAMs, so that the DRAMs are addressed correctly even though different sizes are used in different banks.

The DA bus is the address bus for the physical DRAMs. The address bits for RAS, CAS, and REF are from the MA bus. REF refers to the addresses for Refresh cycles.

256K x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8		
CAS	2	3	4	5	6	7	9	10	8		
RAS	11	12	13	14	15	16	17	18	19		
REF	2	3	4	5	6	7	0	1	X		
1M x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8	9	
CAS	2	3	4	5	6	7	8	10	11	9	
RAS	20	21	13	14	15	16	17	18	19	12	
REF	2	3	4	5	6	7	8	0	1	X	
4M x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8	9	10
CAS	2	3	4	5	6	7	8	9	10	11	12
RAS	20	21	13	14	15	16	17	18	19	22	23
REF	2	3	4	5	6	7	8	9	0	1	X

Table 4. Page Mode DRAM Address Assignments

256 K x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8		
CAS	2	3	4	5	6	7	9	10	8		
RAS	11	12	13	14	15	16	17	18	19		
REF	2	3	4	5	6	7	0	1	X		
1 M x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8	9	
CAS	2	3	4	5	6	7	9	10	8	20	
RAS	11	12	13	14	15	16	17	18	19	21	
REF	2	3	4	5	6	7	0	1	8	X	
4 M x 1 DRAMS											
DA	0	1	2	3	4	5	6	7	8	9	10
CAS	2	3	4	5	6	7	9	10	8	20	22
RAS	11	12	13	14	15	16	17	18	19	21	23
REF	2	3	4	5	6	7	0	1	8	9	X

Table 5. Addresses For Different Sized DRAMs

3.1.1 Memory Maps

The first 640K of memory is used for system RAM. Additional banks of RAM are mapped in contiguous blocks, starting at 1 MB. The 256/384K of extra RAM from the first 1 MB is the Split RAM, and is remapped to the top of the last block of memory on the system after the BIOS has determined the total memory size.

Tables 6 through 13 provide memory maps for a typical system. In these tables, 'A' represents the amount, in Mbytes, of system board memory installed and enabled, starting at 00000000H; 'B' represents the amount, in Mbytes, of memory available on the Channel, starting at or above 000100000H.

ENSPLIT = 1 **SIX40 = 1** **ROMEN = 1** **Split Address = Disabled**	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0007FFFFH	512K System Board RAM
00080000 - 0009FFFFH	Not Used
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board ROM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - FFFDFFFF	Not Used
FFFE0000 - FFFFFFFFH	128K System Board ROM (same as 000E0000 - 000FFFFFH)

Table 6. Memory Map 1

ENSPLIT = 1 **SIX40 = 0** **ROMEN = 1** **Split Address = Disabled**	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0009FFFFH	640K System Board RAM
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board ROM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - FFFDFFFF	Not Used
FFFE0000 - FFFFFFFFH	128K System Board ROM (same as 000E0000 - 000FFFFFH)

Table 7. Memory Map 2

ENSPLIT = 0 SIX40 = 1 ROMEN = 1 Split Address = 1 + A + B	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0007FFFFH	512K System Board RAM
00080000 - 0009FFFFH	Not Used
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board ROM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - (00100000+A+B+384K)	384K System Board RAM
(00100000+A+B+384K) - FFFDFFFF	Not used
FFFE0000 - FFFFFFFFH	128K System Board ROM (same as 000E0000 - 000FFFFFH)

Table 8. Memory Map 3

ENSPLIT = 0 SIX40 = 0 ROMEN = 1 Split Address = 1 + A + B	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0009FFFFH	640K System Board RAM
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board ROM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - (00100000+A+B+256K)	256K System Board RAM
(00100000+A+B+256K) - FFFDFFFF	Not used
FFFE0000 - FFFFFFFFH	128K System Board ROM (same as 000E0000 - 000FFFFFH)

Table 9. Memory Map 4

ENSPLIT = 1 SIX40 = 1 ROMEN = 0 Split Address = Disabled	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0007FFFFH	512K System Board RAM
00080000 - 0009FFFFH	Not Used
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board RAM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - FFFDFFFF	Not Used
FFFE0000 - FFFFFFFFH	128K System Board ROM

Table 10. Memory Map 5

ENSPLIT = 1 SIX40 = 0 ROMEN = 0 Split Address = Disabled	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0009FFFFH	640K System Board RAM
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board RAM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - FFFDFFFF	Not Used
FFFE0000 - FFFFFFFFH	128K System Board ROM

Table 11. Memory Map 6

ENSPLIT = 0 SIX40 = 1 ROMEN = 0 Split Address = 1 + A + B	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0007FFFFH	512K System Board RAM
00080000 - 0009FFFFH	Not Used
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board RAM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - (00100000+A+B+384K)	384K System Board RAM
(00100000+A+B+384K) - FFFDFFFF	Not used
FFFE0000 - FFFFFFFFH	128K System Board ROM

Table 12. Memory Map 7

ENSPLIT = 0 SIX40 = 0 ROMEN = 0 Split Address = 1 + A + B	
ADDRESS RANGE (Hex)	**FUNCTION**
00000000 - 0009FFFFH	640K System Board RAM
000A0000 - 000BFFFFH	128K Video ROM
000C0000 - 000DFFFFH	Channel ROM
000E0000 - 000FFFFFH	128K System Board RAM
00100000 - (00100000+A)	System Board RAM
(00100000+A) - (00100000+A+B)	Channel RAM
(00100000+A+B) - (00100000+A+B+256K)	256K System Board RAM
(00100000+A+B+256K) - FFFDFFFF	Not used
FFFE0000 - FFFFFFFFH	128K System Board ROM

Table 13. Memory Map 8

3.1.2 MEMORY CONFIGURATION

The tables in this section describe the format of the ESF and I/O registers that are used to configure memory on the system board. Note that the registers on the WD6030 can only be accessed by the CPU. In this description of the registers that can be written to, bits marked RESERVED should always be written with zeros; this will ensure compatibility with future Western Digital products.

3.1.2.1 Memory Control Register 0103H (W)

The Memory Control Register is implemented in the WD6000. At power-on, a refresh rate compatible with that of the Model 80, 0.8 µs refreshes, is selected, but the BIOS later changes this to 15.1 µs.

Bit 0	Reserved
Bit 1	$\overline{\text{FREF}}$ Fast Refresh 0 = Refresh of 0.8 µs 1 = Refresh of 15.1 µs
Bits 2-7	Reserved
(Power-on Default = 00000000)	

Table 14. Memory Control Register

3.1.2.2 Memory Card Definition Register 0103H (R)

In the Western Digital chip set, this register is implemented in the WD6000. The power-on default, 256K x 1 DRAMs, is compatible with both the 80-071 and the 80-111.

The IBM Memory Card Definition register is implemented on the Model 80 to detect the presence of two memory modules on the system board.

This register treats memory on the system board as being installed in two connectors. The Model 80-071 has connectors with 1 MB each; the Model 80-111 connectors can have up to 2 MB. Bits T1 and R1 are the encodings for Connector 1, and Bits T2 and R2 are the encodings for Connector 2. Some bits that were reserved on the 80-071 have been coded on the 80-111, but are compatible with the 80-071.

There are certain differences between the Western Digital and IBM implementations of this register. The Western Digital Memory Card Definition register does not support the detection of memory connectors, so it always indicates 11110000. Further, it views the system board memory sequentially in four banks of 1 MB, 4 MB, or 16 MB each. However, to maintain compatibility with the Model 80, at power-up the 256K x 1 DRAMs are mapped to correspond to the IBM connector mappings. Table 16 shows the mapping used in the Model 80 Compatibility Mode (256K x 1 DRAMs).

Bits 1, 0	R1, T1 00 - 1 MB RAM in Connector 1 10 - 2 MB RAM in Connector 1 X1 - No RAM (Should be at least 1 MB)
Bits 3, 2	R2, T2 00 - 1 MB RAM in Connector 2 10 - 2 MB RAM in Connector 2 X1 - No RAM
Bits 4-7	1 = Reserved
(Power-on Default = 11110000)	

Table 15. Memory Card Definition Register

W D-Implementation	IBM Model 80 Implementation
Bank 0	Lower 1 MB of Connector 1
Bank 2	Upper 1 MB of Connector 1
Bank 1	Lower 1 MB of Connector 2

Table 16. Model 80 Compatibility Mode

15

3.1.2.3 Memory Encoding Register 1 00E1H And Shadow RAM (R/W)

The bit encodings of this register on the 80-071 and the 80-111 differ, requiring several extra I/O writes to make the 80-111 compatible with the 80-071.

Western Digital implements this register on the WD6030 with all the bits being read/write. The register is compatible with the 80-111. Bit 0, ENPLRPCH, is duplicated in the WD6010, where it is a write-only bit used to control the ENPCHK signal. Table 17 shows the bit assignment for this register.

This register implements the Shadow RAM function and controls the copying of ROM to RAM, and the subsequent execution out of RAM.

When ROMEN is one, all read accesses are directed to the ROM, and all write accesses are directed towards the RAM. When it is zero, all read accesses are directed to the RAM, and write accesses are directed to the Channel, where they are ignored. Physical RAM locations E0000H-FFFFFH are always reserved for this purpose.

To use the Shadow RAM, execute the following steps:

1. Set ROMEN to one.
2. Read Locations E0000 - FFFFFH, and write to the same locations. This copies the ROM code to the RAM.
3. Set ROMEN to zero. The code will now execute out of RAM.

Bit 0	ENPLRPCH 0 - Enable Parity Checking of DRAM 1 - DisableParityCheckingof DRAM
Bit 1	ROMEN 0 - ROM Address Space (E0000-FFFFFH) in DRAM 1 - ROM Address Space in ROM
Bit 2	SIX40 0 - First Meg Split at 640K 1 - First Meg Split at 512K
Bit 3	ENSPLIT 0 -Split Memory Mapped by Split Address Register 1 - Split Memory Disabled
Bits 4-5	EN01, EN02 00 - 2 MB Enabled in Connector 1 10 - First 1 MB Disabled in Connector 1 01 - 1 MB Enabled in Connector 1 11 - Invalid (Memory Disabled in Connector 1)
Bits 6-7	Reserved
(Power-on Default = 11101011)	

Table 17. Memory Encoding Register 1

NOTE
Do not perform any ESF operations while these three steps are being executed, as the ESF register may be corrupted.

Table 18 details different memory configurations generated under the combinations of ENSPLIT, SIX40 and ROMEN.

ENSPLIT	SIX40	ROMEN	CONFIGURATION
0	0	0	ROM Disabled. 256 KB at Split Address
0	0	1	ROM Enabled. 256 KB at Split Address
0	1	0	ROM Disabled. 384 KB at Split Address
0	1	1	ROM Enabled. 384 KB at Split Address

Table 18. ENSPLIT, SIX40, and ROMEN Memory Configurations

3.1.2.4Memory Encoding Register 2 00E0H (R/W)

The bit encodings of this register on the 80-071 and the 80-111 differ, requiring several extra I/O writes to make the 80-111 compatible with the 80-071.

Western Digital implements this 80-111 compatible register on the WD6030. Bits 0 - 3 of this register define the starting address for the Split Memory and should not be set to zero unless ENSPLIT is one. The Split Address can be used in conjunction with the Split Address Extension Register to map the Split Memory anywhere in the 4 Gigabyte memory space. The only restriction being that the split memory should always be remapped at an address that is a multiple of the largest bank size, for example, with 1M x 1 DRAMs, it should be remapped at a 4 MByte boundary. Table 19 contains the bit assignments for this register.

Bit 0	SPA20 Split Address 20
Bit 1	SPA21 Split Address 21
Bit 2	SPA22 Split Address 22
Bit 3	SPA23 Split Address 23
Bits 4-5	$\overline{EN11}$, $\overline{EN12}$ 00 - 2 MB Enabled in Connector 2 10 - First 1 MB Disabled in Connector 2 01 - 1 MB Enabled in Connector 2 11 - Invalid (Memory Disabled in Connector 2)
Bits 6-7	1 - Reserved
(Power-on Default = 11100010)	

Table 19. Memory Encoding Register 2

The Western Digital implementation of the memory encoding registers differs from the IBM implementation. Bits 4 and 5 of these registers ($\overline{EN12}$, $\overline{EN11}$, $\overline{EN01}$, $\overline{EN02}$) are only applicable when all the banks are populated with 256K x 1 DRAMs, the IBM-compatible power-on default. When other DRAMs are used, the encodings in Table 20 are used. In this table, the "x" in $\overline{ENx2}$ and $\overline{ENx1}$ indicates either a zero or a one.

REGISTER	$\overline{ENx2}$	$\overline{ENx1}$	FUNCTION
00E1	0	0	Bank 0 Enabled
	1	1	Bank 0 Disabled
	0	1	Reserved
	1	0	Reserved
00E0	0	0	Bank 1 Enabled
	1	1	Bank 1 Disabled
	0	1	Reserved
	1	0	Reserved

Table 20. DRAM Encodings

3.1.2.5 Split Address Extension Register ESF:0183H (R/W)

This read/write register is a Western Digital enhancements and is accessed through the Extended Setup Facility. It is used in combination with the Split Address Register to relocate the Split Address at any 1 MByte boundary in the 4 Gigabyte memory address space of the 80386/80486. Most systems will place the split address above the Channel adapter memory in the memory map. Table 21 contains the bit assignment for this register.

Bit 0	- Split Address Bit 24
Bit 1	- Split Address Bit 25
Bit 2	- Split Address Bit 26
Bit 3	- Split Address Bit 27
Bit 4	- Split Address Bit 28
Bit 5	- Split Address Bit 29
Bit 6	- Split Address Bit 30
Bit 7	- Split Address Bit 31
(Power-on Default = 00000000)	

Table 21. Split Address Extension Register

15

3.1.2.6 Bank Enable And Version Number Register ESF:0182H (R/W)

This read/write register is a Western Digital enhancement, and does not exist on the Model 80. It disables or enables Memory Banks 2 and 3 and provides the version number of the WD6030 device. Table 22 provides the bit assignment for this register.

Bits 0, 1	$\overline{EN22}$, $\overline{EN21}$ 00 - Enables Bank 2 11 - Disables Bank 2 10 - Reserved 01 - Reserved
Bits 2, 3	$\overline{EN32}$, $\overline{EN31}$ 00 - Enables Bank 3 11 - Disables Bank 3 01 - Reserved 10 - Reserved
Bits 4-7	WD6030 Version Number
(Power-on Default = xxxx1111) The value of 'x' is dependent upon the version number of the WD6030.	

Table 22. Bank Enable And Version Number Register

3.1.2.7 Memory Size Register ESF:0181H (R/W)

This read/write register is a Western Digital enhancement that does not exist on the Model 80. It indicates the type of DRAM chips being used in the memory banks, information that is used internally to implement the memory maps. The software must initialize these bits appropriately, as outlined in Section 3.1.3. Table 23 shows the bit assignment. All the bits are read/write.

Certain points must be kept in mind when using this register.

- When the system integrator uses different-sized DRAMs in the memory banks, the software programming and the hardware must ensure that the larger DRAMs are always placed in the lower banks and the smaller DRAMs placed in the higher banks.
- To get the best performance from the system, Page Mode DRAMs should be used in Page Mode. This mode requires the system to have DRAMs of the same size in all the banks.

Bits 0, 1	- MSIZ00, MSIZ01 Memory Size in Bank 0 00 - 256K x 1 DRAMs 10 - 1M x 1 DRAMs 11 - 4M x 1 DRAMs 01 - Reserved
Bits 2, 3	- MSIZ10, MSIZ11 Memory Size in Bank 1 00 - 256K x 1 DRAMs 10 - 1M x 1 DRAMs 11 - 4M x 1 DRAMs 01 - Reserved
Bits 4, 5	- MSIZ20, MSIZ21 Memory Size in Bank 2 00 - 256K x 1 DRAMs 10 - 1M x 1 DRAMs 11 - 4M x 1 DRAMs 01 - Reserved
Bits 6, 7	- MSIZ30, MSIZ31 Memory Size in Bank 3 00 - 256K x 1 DRAMs 10 - 1M x 1 DRAMs 11 - 4M x 1 DRAMs 01 - Reserved
(Power-on Default = 00000000)	

Table 23. Memory Size Register

3.1.2.8 Memory Window Bank 0 Register ESF:0184H (R/W)

This read/write register is a Western Digital enhancement and is accessed through the ESF. It relocates Memory Bank 0 to anywhere up to 64 MBytes, the maximum memory supported by the board. For 256K x 1, 1M x 1, and 4M x 1 DRAMs, it relocates Memory Bank 0 at a 1 MByte boundary, a 4 MByte boundary and a 16 MByte boundary respectively, in the processor address space.

To program any of the Memory Window registers correctly, the software must make sure that the address re-mapping does not cause any address conflicts. This means that it has to account for the size of the DRAMs installed in the banks and must program the register so that Bank 0 has unique addresses.

Table 24 details the bit assignment for this register. Note that only the combination of bits indicated by the + in the table needs to be programmed for the different DRAM sizes. This applies to the other memory window registers as well, described in Sections 3.1.2.9 - 3.1.2.11.

		256K	1M	4M
Bit 0	- Address Bit 20	+		
Bit 1	- Address Bit 21	+		
Bit 2	- Address Bit 22	+	+	
Bit 3	- Address Bit 23	+	+	
Bit 4	- Address Bit 24	+	+	+
Bit 5	- Address Bit 25	+	+	+
Bits 6, 7	- Reserved			
Power-on Default = 00000000 (256K x 1 DRAMs)				

Table 24. Memory Window Bank 0 Register

3.1.2.9 Memory Window Bank 1 Register ESF:0185H (R/W)

This read/write register is a Western Digital enhancement and is accessed through the ESF. It relocates Memory Bank 1 to anywhere up to 64 MBytes, the maximum memory supported by the board. For 256K x 1, 1M x 1, and 4M x 1 DRAMs, it relocates Memory Bank 1 at a 1 MByte boundary, a 4 MByte boundary, and a 16 MByte boundary respectively, in the processor address space. Table 25 details the bit assignment for this register.

		256K	1M	4M
Bit 0	- Address Bit 20	+		
Bit 1	- Address Bit 21	+		
Bit 2	- Address Bit 22	+	+	
Bit 3	- Address Bit 23	+	+	
Bit 4	- Address Bit 24	+	+	+
Bit 5	- Address Bit 25	+	+	+
Bits 6, 7	- Reserved			
Power-on Default = 00000001 (256K x 1 DRAMs)				

Table 25. Memory Window Bank 1 Register

2.1.2.10 Memory Window Bank 2 Register ESF:0186H (R/W)

This read/write register is a Western Digital enhancement and is accessed through the ESF. It relocates Memory Bank 2 to anywhere up to 64 MBytes, the maximum memory supported by the board. For 256K x 1, 1M x 1, and 4M x 1 DRAMs, it relocates Memory Bank 2 at a 1 MByte boundary, a 4 MByte boundary, and a 16 MByte boundary respectively, in the processor address space.

Table 26 details the bit assignment for this register.

15

		256K	1M	4M
Bit 0	- Address Bit 20	+		
Bit 1	- Address Bit 21	+		
Bit 2	- Address Bit 22	+	+	
Bit 3	- Address Bit 23	+	+	
Bit 4	- Address Bit 24	+	+	+
Bit 5	- Address Bit 25	+	+	+
Bits 6, 7	- Reserved			
Power-on Default = 00000010 (256K x 1 DRAMs)				

Table 26. Memory Window Bank 2 Register

3.1.2.11 Memory Window Bank 3 Register ESF:0187H (R/W)

This read/write register is a Western Digital enhancement, accessed through the ESF. It relocates Memory Bank 3 to anywhere up to 64 MBytes, the maximum memory supported by the board. For 256K x 1, 1M x 1, and 4M x 1 DRAMs, it relocates Memory Bank 3 at a 1 MByte boundary, a 4 MByte boundary, and a 16 MByte boundary respectively, in the processor address space.

While re-mapping banks, the software should ensure that no holes are created in memory and that the system board memory always starts at Address 00000000H. Further, all system board memory should be placed contiguously in the memory map. The only exception is the split addresses, which are placed contiguously above the Channel RAM. Table 27 details the bit assignment for this register.

		256K	1M	4M
Bit 0	- Address Bit 20	+		
Bit 1	- Address Bit 21	+		
Bit 2	- Address Bit 22	+	+	
Bit 3	- Address Bit 23	+	+	
Bit 4	- Address Bit 24	+	+	+
Bit 5	- Address Bit 25	+	+	+
Bits 6, 7	Reserved			
Power-on Default = 00000011 (256K x 1 DRAMs)				

Table 27. Memory Window Bank 3 Register

3.1.2.12 Memory Configuration Register ESF:0180H (R/W)

This read/write register is a Western Digital ESF enhancement. It controls the enabling and disabling of the cache and Page Mode for the DRAMs. Table 28 details the bit assignment for this register.

At power-on, the software must read the Memory Size Register and ensure that all the banks have DRAMs of the same size before setting Bit 4, FRMISS, to zero. When the cache is set for Forced Misses at power-up to ensure proper cache initialization, read data for the Memory Read cycle comes from the DRAM and writes go to the DRAM. The TagRAM and cache are updated on each Read Miss. When the DRAMs are set in Forced Row Misses, the DRAMs are not operated in Page Mode, and a RAS/CAS precharge is performed for every DRAM cycle. This mode should be used if there are no Static Column or Page Mode DRAMs being used in the system.

Bit 0	FMISS Cache Forced Miss 0 - Cache Operating in Normal Mode 1 - Cache Operating in Forced Misses Mode
Bits 1-3	Reserved
Bit 4	FRMISS Forced Row Miss 0 - DRAMs Operating in Page Mode 1 - DRAMs Operating in Normal RAS/CAS Mode
Bits 5-6	Reserved
Bit 7	RASTMOUT RAS Time-out 0 - 10 microseconds RAS Time-out Disabled 1 - 10 microseconds RAS Time-out Enabled
Power-on Default = 00010001	

Table 28. Memory Configuration Register

When Bit 7, RASTMOUT, is set, it enables an internal timer which monitors the length of the NRAS pulse and precharges it every 10 ms. The bit must be set for DRAMs requiring the maximum pulse width on NRAS to be less than or equal to 10 ms. Do not, however, enable Bit 7 for DRAMs that do not require it, as this will degrade memory performance.

The approximate RAS time-out periods at different operating frequencies is tabulated below.

FREQ.	APPROXIMATE RAS TIME-OUT PERIOD
16 MHz	9 µs
20 MHz	9.6 µs
25 MHz	8.96 µs
33 MHz	8.64 µs

Western Digital allows memory performance to be fine-tuned to the CPU frequency through a series of Memory Timing Registers which allow the critical DRAM parameters in the memory cycle to be directly programmed. This enables DRAMs with different parameters, including different access times, to be used. The memory wait states obtained are a result of this programming and can not be explicitly programmed. The system's primary (CLK2) and phase clock (CLK) signals provide the time granularity for programming. Refer to Section 3.3, Timing Configuration, for further details on programming.

3.1.2.13CAS Pulse Width Register ESF:0188H (R/W)

This read/write register is a Western Digital ESF enhancement; Table 29 describes its format.

Bit 0 programs the CAS pulse width for DRAM read cycles when the DRAM being used has a CAS access time greater than 35 ns, or when the system is using 100 ns DRAMs and is being run at a frequency higher than 25 MHz. DRAM write cycles cannot be programmed. The programming of this bit determines the number of wait states to be provided by the WD6030 wait state generator.

When a Channel master performs a read to system board memory, Bit 1 extends the cycle if the DRAM being used has a CAS access time greater than 35 ns, or when the system is using 100 ns DRAMs and is being run at a frequency higher than 25 MHz. DRAM write cycles can not be programmed. Bit 1 (CPW1) also controls the reassertion of CHRDY, as shown in Table 29. Note that CLK2 in this table denotes a frequency twice that of the processor. Bit 2 allows timing between RAS to MUX and MUX to CAS to be controlled by sofware. For 33 MHz systems this bit can be programmed to one, and the DRAM controller in the WD6030 will change MUX after two CLK2s and CAS will drop two CLK2s after MUX. Bit 3 CPW allows programming of UCHRDY signal. For asynchronous extended cycles during Master accesses, the UCHRDY is removed as CMD falling edge. This feature improves system performance for Master accesses for 25 and 33 MHz systems.

Bit 0	CPW0 CAS Pulse Width from 386/486/DMA cycles 0 - CAS Pulse Width = 2CLK (1 WS with Page Hit) 1 - CAS Pulse Width = 3CLK (2 WS with Page Hit)
Bit 1	CPW1 CHRDY Re-assertion for Channel Master cycle 0 - UCHRDY released after leading edge of CAS 1 - UCHRDY released after leading edge of CLK2
Bit 2	RAS to MUX to CAS 0 - 1 CLK2 (default) 1 - 2 CLK2
Bit 3	0 - Sync extended Master cycle 1 - Async Master cycle
Bits 4-7	Reserved
(Power-on Default = 00000111)	

Table 29. CAS Pulse Width Register

3.1.2.14 RAS Precharge Delay Register ESF:0189H (R/W)

This read/write register is a Western Digital ESF enhancement, which permits the RAS precharge time to be programmed in CLK2 (twice the processor frequency) increments to suit the type of DRAM being used. The range extends from a minimum delay of 2 CLK2s (62.5 ns at 16 MHz) up to a maximum of 6 CLK2s (90 ns at 33 MHz).

Bits 2-0	PREC (2:0) RAS Precharge 000 - 2 CLK2s 001 - 3 CLK2s 010 - 4 CLK2s 011 - 5 CLK2s 100 - 6 CLK2s 101 - Reserved 110 - Reserved 111 - Reserved
Bits 3-7	Reserved
(Power-on Default = 00000100)	

Table 30. RAS Precharge Delay Register

3.1.2.15 RAS Pulse Width Register ESF:018AH (R/W)

This read/write register is a Western Digital ESF enhancement, which permits the RAS pulse width to be programmed and tailored to the DRAM. The pulse width obtained in actual operation is equal to or greater than the programmed value. It can range from 3 CLK2s (93.75 ns at 16 MHz) to 7 CLK2s (105 ns at 33 MHz).

Bits 2:0	RPW (2:0) RAS Pulse Width 000 - 3CLK2 001 - 4CLK2 010 - 5CLK2 011 - 6CLK2 100 - 7CLK2 101 - Reserved 110 - Reserved 111 - Reserved
Bits 3-7	Reserved
(Power-on Default = 00000100)	

Table 31. RAS Pulse Width Register

3.1.2.16 RAS Access Time Register ESF:018BH (R/W)

This read/write register is a Western Digital ESF enhancement; it programs the RAS pulse width to meet the DRAM RAS access times. The pulse widths can range from 4 CLK2s (125 ns at 16 MHz) up to a maximum of 9 CLK2s or (135 ns at 33 MHz). Actual pulse widths will be equal to or greater than the value programmed.

For Memory Configuration Registers ESF:188, ESF:189, ESF:18A, and ESF 18B (Sections 3.1.2.13 - 3.1.2.16), the software must program these registers appropriately before accessing them if the DRAMs being used have parameters that differ from the default values.

Bits 2:0	ACC (2:0) RAS Pulse Width due to access time 000 - 4 CLK2s 001 - 5 CLK2s 010 - 6 CLK2s 011 - 7 CLK2s 100 - 8 CLK2s 101 - 9 CLK2s 110 - Reserved 111 - Reserved
Bits 3-7	Reserved
(Power-on Default = 00000101)	

Table 32. RAS Access Time Register

3.1.2.17 System Configuration Register ESF:018FH (R/W)

This read/write register is a Western Digital ESF enhancement that provides configuration data for the system. Bit 0 is used to detect the presence/absence of an optional numeric coprocessor device, Intel's 80387. If it is present, the I/O bus cycles with Address Bit 31 (PA31) set are directed towards the 80387, and the 80387 generates a Ready signal. If the coprocessor is absent, the Ready signal for those bus cycles is generated by the WD6030.

Bit 1 enables/disables the optional Weitek 3167 or compatible coprocessor. When Bit 1 is enabled, memory accesses in the range C0000000 - C000FFFFH are directed to the Weitek coprocessor and the coprocessor generates the Ready signal. When it is disabled, the WD6030 generates the Ready signal for those addresses.

Bits 7 and 6 latch the state of the frequency configuration bits. The software uses this information to determine the speed at which the system is operating.

When the system is powered on, the state of the UCHMSTR, A20GTX and SWPDIR signals are latched into WD6030 internal signals F1, F0 and COPRES, respectively.

Bit 0	80387 Present/Absent (R/O) 0 - 80387 Present 1 - 80387 Absent
Bit 1	WTKEN Weitek 1167 Enable/Disable (R/W) 0 - Module Disabled 1 - Module Enabled
Bits 2-5	Reserved
Bits 6-7	UCHMSTR, A20GTX (R/O) 00 - 16 MHz 01 - 20 MHz 11 - 25 MHz 10 - 33 MHz
(Power-on Default = xx00000x)	

Table 33. System Configuration Register

The value of "x" in the power-on default above depends on the configuration of the system, and may vary.

3.1.3 Operating Modes

The DRAM controller is optimized for Page Mode DRAMs. They allow one wait state operation on a cache miss if the access was to the same DRAM row, thus keeping the cache miss overhead low.

The first cache miss takes two wait states, but subsequent misses only take one wait state, because of the operation of the CPU and the WD6010 in Pipelined Mode.

Page Mode and ordinary RAS/CAS DRAMs are also supported. Note that the Static Column Mode should be turned off in the DRAM controller when using RAS/CAS DRAMs, or degraded performance could result.

The system requires 100 ns DRAMs. Faster DRAMs can be used, but all accesses to the DRAMs will still take at least one wait state because of the use of the cache.

3.2 MEMORY INITIALIZATION

The system power-on default configuration follows:

- 1 MByte per bank
- Banks 0 and 1 enabled; all other banks disabled
- Split Address at 000100000H
- ROM enabled through Memory Encoding Register 1
- Split Memory enabled through Memory Encoding Register 1
- 640 enabled through Memory Encoding Register 1
- Page Mode disabled
- Cache disabled
- 80386 in Protected Mode at power-on

The following steps describe one possible way to initialize the system board DRAM in a system using a mixture of DRAM sizes.

1. Determine the first bank in the system, which contains Addresses 00000000 - 0007FFFFH.

   To determine the bank, enable Bank n (0, 1, 2 or 3) and disable the others. Execute a RAM test on the first 512K. If the test passes, Bank n is the first bank. If it fails, disable that bank, and identify it as a failed bank. Repeat the test with the next bank, until you find a bank that passes the test. If all the banks fail the test, the system is non-functional.

2. Determine the size of the DRAMs in the first bank that passes the RAM test.

> **NOTE**
> If any portion of a bank is found to be bad, that bank can still be used by setting the memory size bits to the next lower value. For example, if MBytes 8-16 are found to be bad with 4M x 1 DRAMs, set the memory size to 1M x 1, and use that bank as a 1M x 1 bank.

Enable Bank n (0, 1, 2, or 3), and disable the others. Set the Memory Window Bank n register to 0000H, and set the memory size bits for the bank to 256K x 1.

Do a RAM test on the first MByte.
FAIL - Bank is bad; disable it
PASS ↓
Set the memory size bits to 1M x 1
FAIL - Bank is bad; disable it
PASS ↓
Do a RAM test on Mbytes 0-4
FAIL - DRAMs in this bank are 4M x 1
PASS ↓
Set the memory size bits to 4M x 1
Do a RAM test on Mbytes 0 - 16
FAIL - DRAMs are 1M x 1
PASS - Leave the memory size bits at 4M x 1

By the end of Step 2, the Memory Size register and the Bank Enable bits should have been correctly programmed.

3. Set ROMEN = 1, read Locations 000E0000-000FFFFFH and write to the same addresses. This copies the ROM to the physical DRAM. Then set ROMEN = 0. This directs all read accesses to the RAM, which now holds the contents of the ROM, and also write-protects these RAM locations. The shadow RAM is now in operation.

4. Perform the RAM tests described in Step 2 on each of the remaining untested banks to determine their availability and memory size. If any bank is bad or is unpopulated, re-assign the addresses through the Memory Window registers.

At the end of this step, the memory size bits for all the populated banks should be known. The software should now re-assign the addresses for the banks using the Memory Window registers, and avoiding address conflicts. All the addresses should be contiguous, starting at 00000000H.

5. If the banks are found to contain DRAMs of different sizes, during address assignment the software must ensure that the larger DRAMs are always mapped to the lower banks. If the DRAMs are of the same size, Page Mode can be turned ON through the Memory Configuration register after initializing the cache as described in Section 4.3. The cache may also be turned ON at this point, using the same register.

3.3 TIMING CONFIGURATION

The WD6030 supports DRAMs with different timing parameters by reprogramming the Memory Timing Registers. To facilitate programming, the critical RAM parameters in the memory cycle can be directly programmed. These parameters include RAS access time (ESF:018B), RAS pulse width (ESF:018A), RAS precharge (ESF:0189) and CAS pulse width (ESF:0188). Thus, the system can be programmed for the best memory performance at different CPU and memory speeds.

At power-up, the WD6030 defaults to the largest value of each parameter so as to accomodate the slowest RAMs. The Memory Timing Registers must then be re-programmed by the BIOS to extract the best possible performance from the system.

The WD6030 automatically inserts the wait states to satisfy all the programmed parameters. The wait states in the system can not be explicitly programmed.

The minimum time granularity for programming is the primary clock, CLK2: 15 ns with a 66 MHz CLK2 for a system operating at 33 MHz. Note that the system always operates at half the clock speed. The RAS CAS time is always guaranteed to be 2*CLK2.

Table 34 shows the programming for a typical DRAM.

NOTE
This is intended as an example only; system designers must complete a full timing analysis of the memory cycles for the DRAMs used in their particular systems.

System Operation 25 MHz CLK2: Frequency= 50 MHz CLK2: Period= 20 ns DRAM: 1M x 1 Fast Page Mode DRAM	
TIMING	DESCRIPTION
tRAC	RAS Access Time = 100 ns RAS Access Time Register 01H. (Programmed for 5 CLK2s)
tRAS	RAS Pulse Width = 100 ns (min) 100,000 ns (max) RAS Pulse Width Register 02H. (Programmed for 5 CLK2s)
tRP	RAS Precharge = 80 ns RAS Precharge Delay Register 02H. (Programmed for 4 CLK2s)
tCAC	Access Time from CAS = 25 ns CAS Pulse Width Register, Bit 0 = 0. Programmed for CAS pulse width of 4 CLK2s = 80 ns, which ensures that a pipelined one-wait state operation to the DRAM can complete. CAS Pulse Width Register, Bit 0 = 1. CHRDY re-asserted from the leading edge of CAS for Master cycles.
tRCD	RAS to CAS Delay Time = 25 ns (min), 75 ns (max) RAS to CAS Delay = 2 CLK2s = 40 ns

Table 34. Typical DRAM Program Parameters

4.0 CACHE CONTROLLER

The cache is organized in sets. Each set contains one or more lines, a line being the basic unit of data transfer between the cache and the DRAM. The cache controller in the WD6030 implements a direct-mapped, write-through cache for the 80386/80486 with a line-size of four bytes, that executes 80386 bus cycles, DMA, and Channel master bus cycles. Each set in an WD6030-based system contains one line.

The cache subsystem delivers high performance by ensuring zero wait state cache read-hits, and a low, one wait state miss overhead. Zero wait state access is achieved on a cache read-hit, and cache misses are supported by the page mode DRAMs which provide fast, one wait state access for a page hit.

4.1 CACHE ORGANIZATION

The WD6030 implements the cache controller on the chip, but the Tag subsystem is implemented externally to ensure more flexibility in design. The cache controller allows the system designer to determine the amount of DRAM to be cached and the size of the cache according to the cost and performance requirements. A typical cache system uses 64 KBytes of cache, caching 16 MB of DRAM.

To build a direct-mapped cache, the processor addresses are organized in the following manner:

$\overline{\text{BE}}$ (0:3)

They select the bytes in the line for transfer. A write-hit causes only the selected bytes to be replaced, but a cache update operation executed after a cache miss will replace the entire line.

PA (2:N)

They form the index for the cache and determine which line is to be transferred to the device requesting the transfer. "N" depends on the size of the implemented cache.

PA (N+1:M)

They form the tag for the cache. These bits are compared to the ones stored in the TagRAM for that particular index. If they match bit-for-bit, the requested data lies in the cache. "M" depends on the size of the DRAM being cached. The table below shows the values when 16 Mbytes of DRAM are cached.

CACHE SIZE	TAG	INDEX
32 Kbytes	PA(15:23)	PA(2:14)
64 Kbytes	PA(16:23)	PA(2:15)
128 Kbytes	PA(17:23)	PA(2:16)
256 Kbytes	PA(18:23)	PA(2:17)

Table 35. Typical Cache Values

4.2 CACHE POLICY

The cache policy used in an WD6030-based system is described in Table 36. Only the local DRAM, that is, the DRAM set by the Memory Window registers, is cached. All other bus cycles, such as I/O cycles or accesses to the Channel, are treated as non-cachable areas and are not cached.

80386/80486 BUS CYCLES		
TYPE	**CACHE HIT**	**OPERATION**
Read	Yes No	Read from cache Read from DRAM, Update cache
Write	Yes No	Write to the cache and DRAM Write to the DRAM only
DMA (WD6010) CYCLE		
TYPE	**CACHE HIT**	**OPERATION**
Read	Yes No	Read from cache Read from DRAM
Write	Yes No	Write to the cache and DRAM Write to the DRAM only
CHANNEL MASTER BUS CYCLES		
TYPE	**CACHE HIT**	**OPERATION**
Read	X	Read from DRAM
Write	Yes No	Write to Cache and DRAM Write to DRAM

Table 36. Cache Operation in Different Bus Cycles

4.3 CACHE INITIALIZATION AND DIAGNOSTICS

At power-up, invalid tags are stored in the TagRAMs. These tags in the tag directory must be correctly initialized before the cache can be used. To initialize the tags, the power-up default for the cache controller is Forced Misses Mode. The software reads the cache size data (e.g. 64 Kbytes for a 64K cache) from the DRAM, and this action updates the cache and tags to their correct values. The cache can then be programmed in Normal Mode and is ready for use.

There are several ways to conduct system-level diagnostics and verify the correct operation of the cache and DRAM in a cache-based system. Examples of software DRAM testing and cache testing follow.

To test the DRAMs, a typical write-read-compare operation can be performed on the data. Before doing this, ensure that the data always comes from the DRAMs, by using the Memory Configuration Register to program the cache to Forced Misses Mode; this directs all read and write accesses to the DRAM. The cache is updated on a read operation, but a write operation does not affect the cache. To prevent the code executing this diagnostic routine from being overwritten in the cache, either make the code ROM-based, or ensure that the area being tested does not overlap the area where the code resides. Then execute the write-read-compare operation:

1. Write a pattern of data.

2. Read it back and compare it.

To test the cache, perform another write-read-compare operation, using the following sequence:

1. Disable the cache by setting it in Forced Misses Mode.

   Write Pattern 1:
   DRAM = Pattern 1, Cache = unknown
   Read Pattern 1:
   DRAM = Pattern 1, Cache = Pattern 1
   Write Pattern 2:
   DRAM = Pattern 2, Cache = Pattern 1

2. Enable the cache by setting it to Normal Mode. Read and compare the results. If it is Pattern 1, the cache is functioning properly. If it shows Pattern 2, it indicates that the Hit/Miss circuitry has failed. Any other pattern indicates that the cache is bad.

15

4.4 CACHE TIMING

Table 37 shows the typical speeds for the SRAMs required to build the data cache and the TagRAMs required for zero wait state operation.

NOTE
This is intended as an example only; system designers must complete a full timing analysis of the memory cycles for the SRAMs used in their particular systems.

TIMING/FREQUENCY	16 MHz	20 MHz	25 MHz	33 MHz
Processor Address to HIT generation*	57 ns	47 ns	38 ns	20 ns
Data Cache SRAM Access Time (Address to data)	64 ns	45 ns	35 ns	21 ns

*The parameters take into account a 6 ns delay to generate A20 externally.

Table 37. Cache Timing

5.0 CHANNEL CONTROLLER

The Channel Controller in the WD6030 controls the CPU and the DMA accesses to the Micro Channel. Accesses by a Channel master to the system board DRAM are controlled by the DRAM controller in the WD6030. The timing generated by the WD6030 are compatible with the IBM Micro Channel specifications. Figures 24 through 27 illustrates typical accesses to the Channel.

Control is provided for default and extended memory or I/O Channel cycles. 8-bit, 16-bit and 32-bit data can be transferred to the Channel. The CPU always treats a port as being at least sixteen bits wide. Therefore, on an access to an 8-bit port, the WD6030 splits a 16-bit cycle into two cycles and performs any necessary byte swaps. Though the byte-swap is implemented by the WD6022 in Data Buffer Mode, the Channel controller provides the controls for it. It also controls the word swaps, which are necessary when a 16-bit master talks to a 32-bit slave. Figures 26 through 29 illustrates typical byte-swap cycles.

The special timings required by the Channel setup cycles are also implemented by the Channel controller. The Channel Controller also functions as a buffer controller, controlling all data transfers to or from the Channel.

Since the Channel timing remain constant in a system, the WD6030 determines the speed of the processor and optimizes its Channel bus cycles to match Channel specifications. This allows the controller to support the 80386 and 80486 processors at different frequencies: 16, 20, 25, and 33 MHz. The speed of the processor is determined by the state of signals UCHMSTR and A20GTX at power-up. Table 38 supplies a frequency table.

FREQUENCY	UCHMSTR	A20GTX
16 MHz	0	0
20 MHz	0	1
25 MHz	1	1
33 MHz	1	0

Table 38. Frequency Table

15

6.0 EXTENDED SETUP FACILITY (ESF)

The Extended Setup Facility (ESF) is a Western Digital enhancement that permits additional functionality to be configured on the board. Based on the concept of "alternate I/O space", it uses memory space that is currently unused on the Model 80 to add more features, or to tailor the board to meet specific needs. The ESF is flexible and can be reprogrammed to other locations if a conflict should arise with future IBM enhancements to the Model 80 design.

The ESF function consists of the ESF Pointer Register (EPR) and associated decode logic that generates the ESF Data Register Enable (EDRENA) output from the WD6010 to the WD6000. The ESF is designed to extend the configuration architecture established with POS features. Refer to Figures 13 and 14 for an overview of the ESF function. ESF supports:

- System Configuration Registers
- Memory Map Control Registers
- Additional Physical Serial Port
- Programmable Port Enables A and B
- EMS Control Registers
- External DRAM Control Configuration
- System Board LAN Configuration
- Customer-specified Enhancements that include:
  System Identification
  System Version

6.1 ESF ADDRESS MAP

The lower sixty-four bytes (EAR0 = 00H - 3FH) of the ESF are reserved for Western Digital functions and features. The upper sixty-four bytes (40H -7FH) can be used by the customer. Refer to Table 39 for details. All functions using ESF must include Bit 7 of EAR0 in the decode. This bit must be zero when addressing only 128 ESF registers. To expand the ESF to Location 32,768, set EAR0 Bit 7 to one and write the second ESF address byte to EAR1.

FUNCTION	ESF ADDRESS	R/W	WD6500 DEVICE
Reserved	0 - 001FH	-	-
Peripheral Configuration	20H	R/W	WD6000
Port A, B Control	21, 24H	R/W	WD6000
Port A, B Address (LSB)	22, 25H	R/W	WD6000
Port A, B Address (MSB)	23, 26H	R/W	WD6000
Reserved	30 - 3FH	-	-
Customer-specified	40 - 7FH	-	-
Memory Configuration	0180H	R/W	WD6030
Memory Size Register	0181H	R/W	WD6030
Bank Enable Register	0182H	R/W	WD6030
Split Address Extension	0183H	R/W	WD6030
Memory Window Bank 0	0184H	R/W	WD6030
Memory Window Bank 1	0185H	R/W	WD6030
Memory Window Bank 2	0186H	R/W	WD6030
Memory Window Bank 3	0187H	R/W	WD6030
CAS Pulse Width	0188H	R/W	WD6030
RAS PreCharge Delay	0189H	R/W	WD6030
RAS Pulse Width	018AH	R/W	WD6030
RAS Access Time	018BH	R/W	WD6030
Enhanced Addressing	018CH	R/W	WD6010
Reserved	018DH	-	-
Reserved	018EH	-	-
System Control Register	018FH	R/W	WD6030

Table 39. ESF Address Map In A WD6500 System Environment

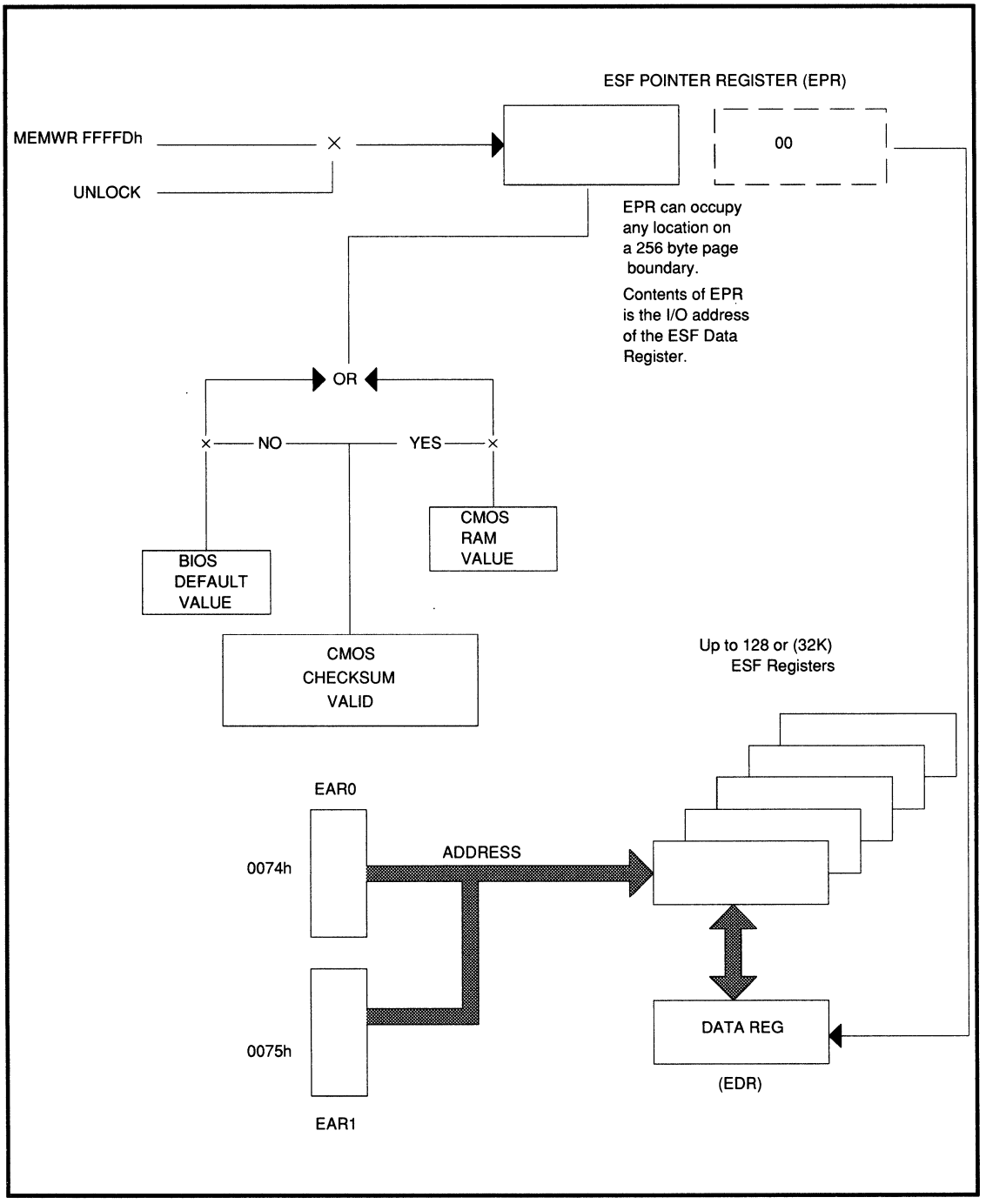


Figure 13. ECR And ESF Block Diagram

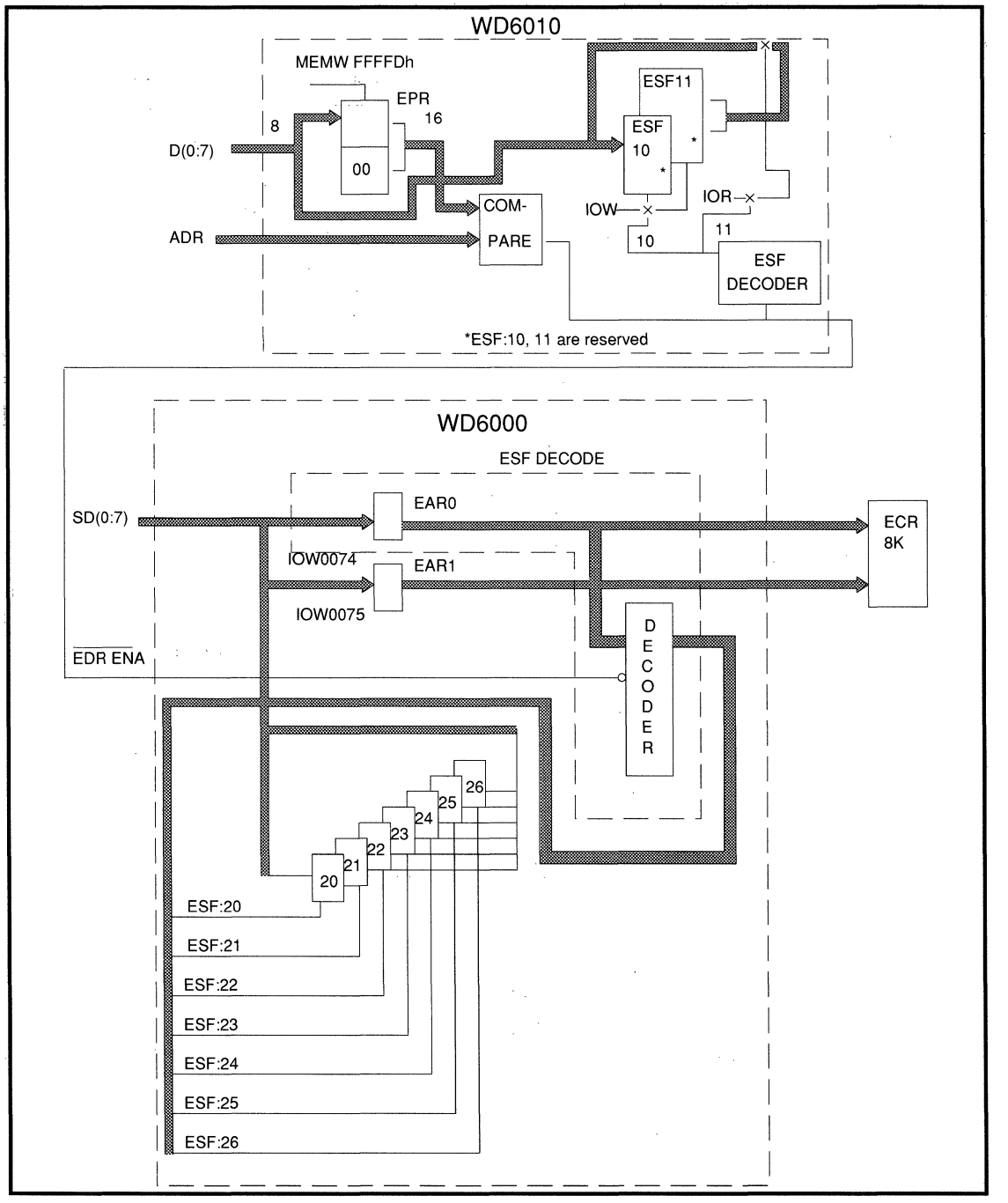


Figure 14. Extended Set-UP Facility Overview

6.2 ESF ACCESS

ESF space consists of 128 locations expandable to 32K, and may be implemented as word-wide or byte-wide, at the discretion of the designer. Table 39 provides an address map of the ESF registers, access to which is accomplished through the Extended Data registers EAR0 and EAR1, and a "real I/O space" window, the Extended Data register (EDR). Registers that are not documented in this table are reserved and should not be used. For a discussion of some ESF registers, see Section 3.1.2.

The write-only ESF Pointer Register (EPR), configurable by the software, points to the EDR. It is loaded by writing to memory location FFFFDH or FFFF, FFFDH, a PROM. The power-on default location for the EDR is at I/O Address 0700H.

The following procedure is recommended to modify the EPR:

1. Set Port 0700H to 8DH to disable NMI.

2. Read System Control Port B at 0061H, and test for a change in the state of Bit 4, Refresh Toggle, to synchronize it with the refresh circuitry.

3. To unlock the EPR, read EAR0 at 0074H, normally a write-only address.

4. Write the new value into the EPR at FFFFDH. This locks the EPR once again.

5. Enable NMI if required. Note that the EPR is locked when written, or on the next refresh cycle, whichever occurs first. The value in EPR becomes the new 8-bit address of the EDR. The EDR can reside at any of 256 locations in the 64K I/O space of the CPU from 0400H to FF00H.

To address the ESF I/O space, follow these steps:

1. Write 8DH to Port 0070H to disable NMI.

2. Write the address value to EAR0 at 0074H. If Expanded ESF is being used, also write the value to EAR1.

3. Issue an I/O Read or Write command to the EDR address.

The selected ESF register is determined by decoding the EAR0 address value.

15

7.0 PERFORMANCE

7.1 MEMORY PERFORMANCE

The performance of a system using a cache depends on several factors, such as the hit rate, the miss overhead, etc. A 64K direct-mapped cache typically produces an 85 - 90% hit rate, with a 30% improvement in performance over a 2 wait state memory design for memory-intensive applications. In DOS environments, the hit rates can exceed 99%. Table 40 shows the performance that can be obtained from the memory subsystem.

NOTE

The performance figures noted above could vary with the software being run.

7.2 TYPICAL CHANNEL ACCESS PERFORMANCE

Table 41 shows typical performance obtained on 80386/80486 or DMA accesses to the Channel. The numbers refer to the cycle times.

Notes

1. For DRAM accesses, the Page Miss performance may vary, depending on the timing parameters of the DRAMs used and the programming in the registers for the CAS pulse width, RAS precharge delay, RAS pulse width and RAS access time.

2. The CAS access time in Page Mode must be equal to or better than 35 ns to achieve the performance shown in Table 41.

3. The numbers in parentheses denote the wait states.

As described above, when operating in Pipelined Mode, the default Page Mode results in one wait state on a cache miss.

CACHE/PAGE MODE ENABLE	16 MHz	20 MHz	25 MHz	33MHz
CACHE HIT	125 ns (0)	100 ns (0)	80 ns (0)	62.5 ns (0)
CACHE MISS AND PAGE HIT, PIPELINED	187.5 (1)	150 ns (1)	120 ns (1)	93.75 ns (1)

Table 40. Typical Performance Of A Memory Subsystem

CHANNEL BUS CYCLE	16 MHz	20 MHz	25 MHz	33 MHz
I/O or Memory without wait*	321.5 ns	300 ns	280 ns	281.25 ns
I/O or Memory with wait*	375+ ns	350+ ns	360+ ns	375 + ns
*The timings shown are for Pipelined Mode. For Non-Pipelined Mode, add an extra wait state.				

Table 41. Channel Bus Cycle

7.3 PERFORMANCE FOR OTHER BUS CYCLES

The wait state controller within the WD6030 generates the required number of wait states on an 80386/80486 or DMA bus cycle, by delaying the SRDY signal until the cycle is completed. It does not, however, respond to accesses to the 80387, as the 80387 generates its own signal RDY0 (READY0), nor to memory accesses that result in a cache hit.

The wait states generated by the controller obey the following rules:

- Local memory accesses that do not generate cache hits result in wait states as shown in Table 42.
- Accesses to the local I/O, including the registers on the WD6010 and the WD6030, and the ESF registers, but excluding Port 00F1H, require an access time of 100 ns, which results in the wait states shown in Table 42.
- Channel cycles, including Interrupt Acknowledge cycles, are determined by the assertion of CHRDYRTN.
- With Halt or Shutdown cycles, a zero wait state operation is completed.
- When a write operation is carried out to Port 00F1H to reset the 80387, 130 wait states are inserted.

I/O CYCLE	16 MHz	20 MHz	25 MHz	33 MHz
Cycle following pipelined cycle	3 WS	3 WS	5 WS	7 WS
Cycle following non-pipelined cycle	4 WS	4 WS	6 WS	8 WS

Table 42. Typical Performance for Accesses to Local I/O

15

8.0 TECHNICAL SPECIFICATIONS

8.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum stress ratings for this device are listed below. Note that permanent device damage could result from exposing the device to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	(V_{DD}-V_{SS})	0	7	V
Input Voltage	V_{IABS}	V_{SS}-0.3	V_{DD}+0.3	V
Bias on Output Pin	V_{OABS}	V_{SS}-0.3	V_{DD}+0.3	V
Storage Temperature	T_S	-40	125	°C

8.2 NORMAL OPERATING CONDITIONS

Exposure of the device to conditions exceeding the recommended normal operating conditions for extended periods of time could affect the long-term reliability of the device.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V
Power Dissipation	P_W	-	850	mW
Supply Current	I_{DD}	-	165	mA

8.3 DC CHARACTERISTICS (UNDER NORMAL OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance @ fc = 1 MHz	C_I	-	5	pF
I/O Capacitance	C_{IO}	-	10	pF
Logic High Input Voltage	V_{IH}	2.0	-	V
Logic Low Input Voltage	V_{IL}	-	0.8	V
Input Leakage	I_{IL}	-	±10	µA
Tristate Output Leakage	I_{OL}	-	±30	µA
I/O Pin Leakage	I_{IOL}	-	±40	µA
OUTPUT $\overline{CCHCS}$				
Source current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink current @ V_{OL} = 0.4 V	I_{OL}	-	6	mA
OUTPUTS D(0:7), $\overline{S(0:1)}$, $\overline{ADL}$, $\overline{CMD}$, A0, $\overline{SBHE}$				
Source current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink current @ V_{OL} = 0.4 V	I_{OL}	-	24	mA
ALL OTHER OUTPUTS				
Source current @ V_{OH} = 2.4 V	I_{OH}	-	-	mA
Sink current @ V_{OL} = 0.4 V	I_{OL}	-	4	mA

Note:
When $\overline{TEST}$ = 0, all outputs and bidirectional lines are tri-stated.

8.4 AC LOAD SPECIFICATIONS

OUTPUTS	SYMBOL	MIN	MAX	UNITS
$\overline{CCHCS}$	C_L	-	75	pF
D(0:7), $\overline{S(0:1)}$, $\overline{ADL}$, $\overline{CMD}$, A0, $\overline{SBHE}$	C_L	-	240	pF
All other outputs	C_L	-	50	pF

9.0 TIMING

PARAM/DESCRIPTION	16 MHz MIN/MAX	20 MHz MIN/MAX	25 MHz MIN/MAX	33 MHz MIN/MAX	NOTES
CLOCKS					
Operating Frequency	4/16	4/20	4/25	8/33	MHz
T1C/CLK2 Period	31.25/125	25/125	20/125	15/62.5	=CLK2
T2AC/CLK2 High Time	9/-	8/-	7/-	6.25/-	@ 2 V
T2BC/CLK2 High Time	5/-	5/-	4/-	4.5/-	@ V_{CC}
T3AC/CLK2 Low Time	9/-	8/-	7/-	6.25/-	@ 2 V
T3BC/CLK2 Low Time	7/-	6/-	4/-	4.5/-	@ 0.8 V
T4C/CLK Period	62.5/250	50/250	40/250	30/125	=CLK
T5C/CLK High Time	20/-	14/-	10/-	8/-	
T6C/CLK Low Time	15/-	12/-	10/-	8/-	
80386/80486 BUS INTERFACE					
$\overline{RDY}$					
T1B/Setup Time	20/-	12.5/-	10.5/-	7.5/	
T2B/Hold Time	3/-	3/-	3/-	4	
HLDA					
T3B/Setup Time	20/-	20/-	18/-	10	
T4B/Hold Time	3/-	3/-	3/-	4	
PA(2:31), $\overline{BE(0:3)}$					
T5B/Setup Time	22/-	18/-	19 (PA2:31) 16 (BE0:3)	15	
T6B/Hold Time	2/-	2/-	4	4	
M/$\overline{IO}$, $\overline{DC}$, $\overline{WR}$, $\overline{ADS}$					
T7B/Setup Time	22/-	20/-	19	15	
T8B/Hold Time	2/-	2/-	4	4	
$\overline{NA}$, $\overline{BS16}$, $\overline{SRDY}$					
T9B/Valid	2/15	2/20 ($\overline{SRDY}$) 2.25 (NA, BS16)	2/18 ($\overline{SRDY}$) 2/20 (NA, BS16)	2/12 ($\overline{SRDY}$) 2/15 (NA, BS16)	
WD6030 Register Read					
T10B/D (0:31) Valid	2/50	2/40	2/31	2/31	
T11B/D (0:31) Disable	2/50	2/40	2/22	2/22	
WD6030 Register Write					
T12B/D (0:31) Setup	30/-	30/-	30/-	301	
T13B/D (0:31) Hold	30/-	30/-	30/-	19	

15

PARAM/DESCRIPTION	16 MHz MIN/MAX	20 MHz MIN/MAX	25 MHz MIN/MAX	33 MHz MIN/MAX	NOTES
CACHE INTERFACE					
HIT					
T1I/Setup Time	25/-	20/-	15/-	11	
T2I/Hold Time	5/-	5/-	5/-	5	
MADS, HITVALID, CDIR, CDEN(0:3), TAGWR, TAGDEN, CCHCS T3I/Valid	2/20	2/24 (MADS, CDIR, CCHCS) 2/20 [HITVALID, CDEN(0:3), TAGWR, TAGDEN]	2/20 (MADS, CDIR, CCHCS) 2/17 [HITVALID, CDEN(0:3), TAGWR, TAGDEN]	2/15 (MADS, CDIR, CCHCS) 2/12 [HITVALID, CDEN(0:3), TAGWR, TAGDEN]	4
CCHWR(0:3)					
T4I/Assertion	2/20	2/25	2/20	2/15	
T5I/De-assertion	-/20	-/25	/20	/15	
T6I/Pulse Width	1.5CLK/-	1.5CLK/-	1.5CLK/-		
DATA CACHE TIMINGS REQUIRED (EXTERNAL SRAMS) **					
ADDRESS					
T1S/Access Time	-/64	-/45	-/30	-/20	
OUTPUT HOLD					
T2S/From Address Change	2/-	2/-	2/-	2/	
CHIP SELECT					
T3S/Access Time	-/64	-/45	-/35	-/20	
WRITE					
T4S/Pusle Width	-/1.5CLK	-/1.5CLK	-/1.5CLK	-/1.5CLK	
ADDRESS					
T5S/Hold from WRITE	-/2	-/2	-/2	-/2	
CACHE-WRITE					
T6S/Data Setup	-/CLK-7	-/CLK-7	-/CLK-7	-/CLK-7	
T7S/Data Hold	-/0	-/0	-/0	-/0	
TAGRAM TIMINGS REQUIRED (EXTERNAL TAGRAM) ***					
HIT					
T1T/From Address	-/57	-/47	-/38	-/23	
WRITE					
T2T/Pulse Width	-/CLK2	-/CLK2	-/CLK2	-/CLK2	
DRAM INTERFACE					
RAS, MUX, CAS(0:3), DRMWR(0:3), MDEN(0:3), MDIR, PARCLK, DRMA(18:19) T1D/Valid	2/20	2/25 [MDEN(0:3), DRMWR(0:3), PARCLK MDIR] 2/20 [RAS, MUX, CAS(0:3), DRMA(18:19)]	2/20 [MDEN(0:3), DRMWR(0:3), PARCLK] 2/25 (MDIR) 2/17 [RAS, MUX, CAS(0:3), DRMA(18:19)]	2/15 [MDEN(0:3), DRMWR(0:3), PARCLK MDIR] 2/12 [RAS, MUX, CAS(0:3), DRMA(18:19)]	1
DRMWR(0:3)					
T2D/Hold from CAS	0/-	0/-	0/-	0/-	

PARAM/DESCRIPTION	16 MHz MIN/MAX	20 MHz MIN/MAX	25 MHz MIN/MAX	33 MHz MIN/MAX	NOTES
CHANNEL CONTROLLER					
CHRDYRTN*					
DS16RTN, DS32RTN					
T1E/Setup	25	25	20	20/-	2
T2E/Hold	5/-	5/-	5/-	5/-	2
A0					
T3E/Valid from BE(0:3)	-/25	-/35	-/35	-/30	
T4E/Hold from S(0:1)	0/-	0/-	0/-	0	
ADL, S(0:1), CMD, RDEN, RDLE, WREN(0:1, H), WRLE, SWPBYT, SWPWORD, SWPDIR			2/25 [ADL, CMD, S(0:1)]	2/20 (ADL,CMD)	
T5E/Valid	2/20	2/25	2/20 (Rest)	2/15 (Rest)	
CHANNEL MASTER ACCESSING SYSTEM BOARD DRAM					
PA (2:31), BE(0:3), M/IO, SBHE, MADE24, S(0:1), ADL, CMD, TR32					
T1M/Setup to CLK2	15/-	15/-	15/-	15/-	2
T2M/Hold from CLK2	2/-	2/-	2/-	2/	2
UCHRDY					
T3M/De-assert from address	-/35	-/35	-/35	/35	
T4M/De-assert from S(0:1)	0/30	-/30	-/30	-/30	
T5M/Valid from CLK2	-/15	-/20	-/20	-/20	
MEMDS32					
T6M/Assert from Addr, M/IO	-/25	-/25	-/25	-/25	
RDEN, WREN(0:1, H)					
T7M/Valid from CMD	-/20	-/20	-/20	-/20	
READ DATA					
T8M/From UCHRDY	-/60	-/60	-/60	-/60	3
CENTRAL TRANSLATOR					
SWPWORD from S(0:1), CMD, TR32, DS32RTN, BE(0:3) T1X/Valid	-/25	-/25	-/25	-/25	

15

NOTES

1. These outputs should track each other and the cache control outputs.
2. These inputs can be asynchronous to CLK2.
3. This is a system level specification.
4. These outputs should track each other and the DRAM controller outputs.

* CHRDYRTN can tolerate a 20 ns setup.

** The SRAMs used should have parameters equal to or better than those listed in this table. The numbers shown are only representative numbers for a typical system; designers should do a complete timing analysis for their own systems to select the SRAMs.

*** The TagRAMs used, whether built out of discrete components or not, should have parameters equal to or better than those listed in this table. The numbers shown are only representative numbers for a typical system; designers should do a complete timing analysis for their own systems to select the SRAMs.

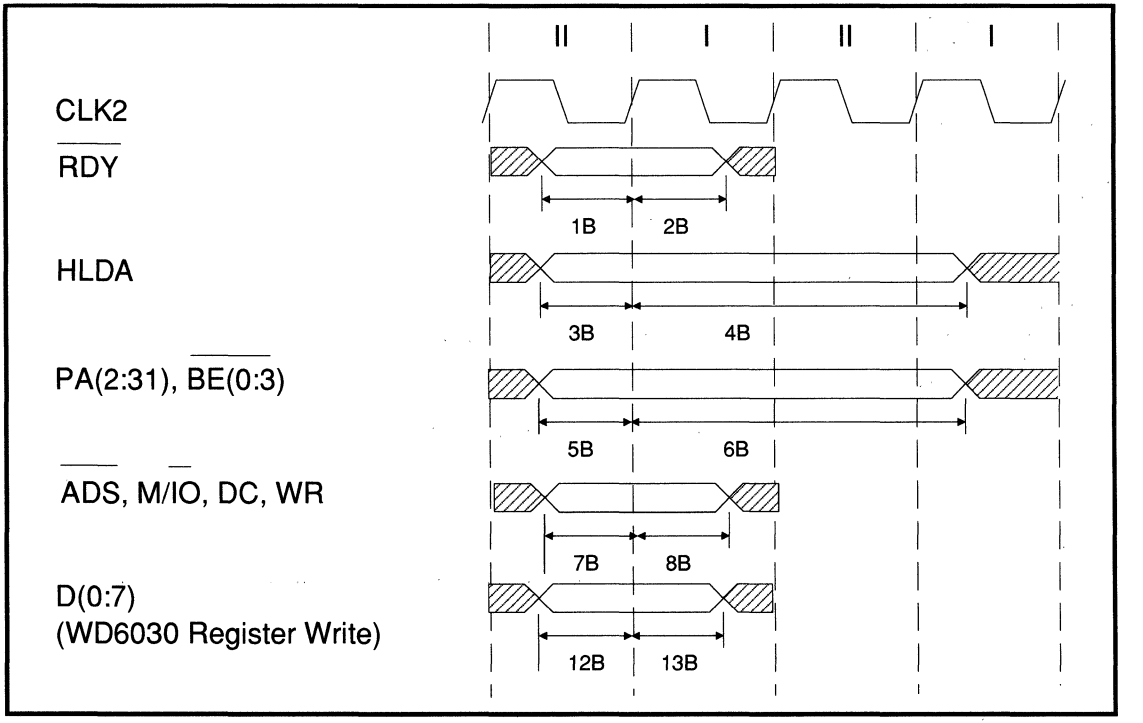


Figure 15. 80386/80486 Bus Interface Input Setup And Hold

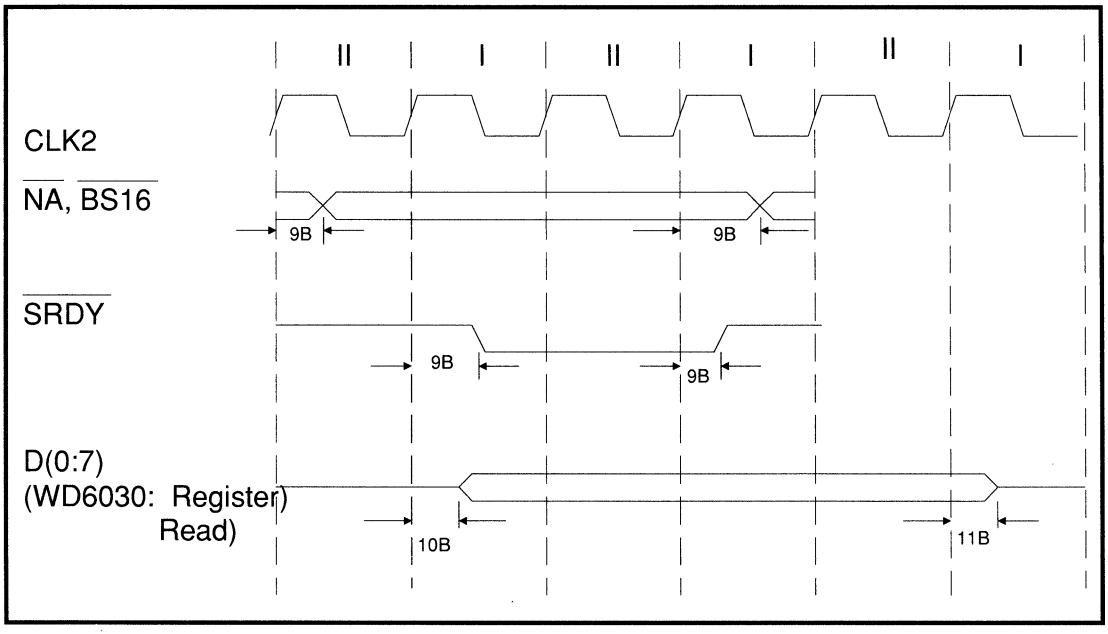


Figure 16. 80386/80486 Bus Interface Output Valid Delay

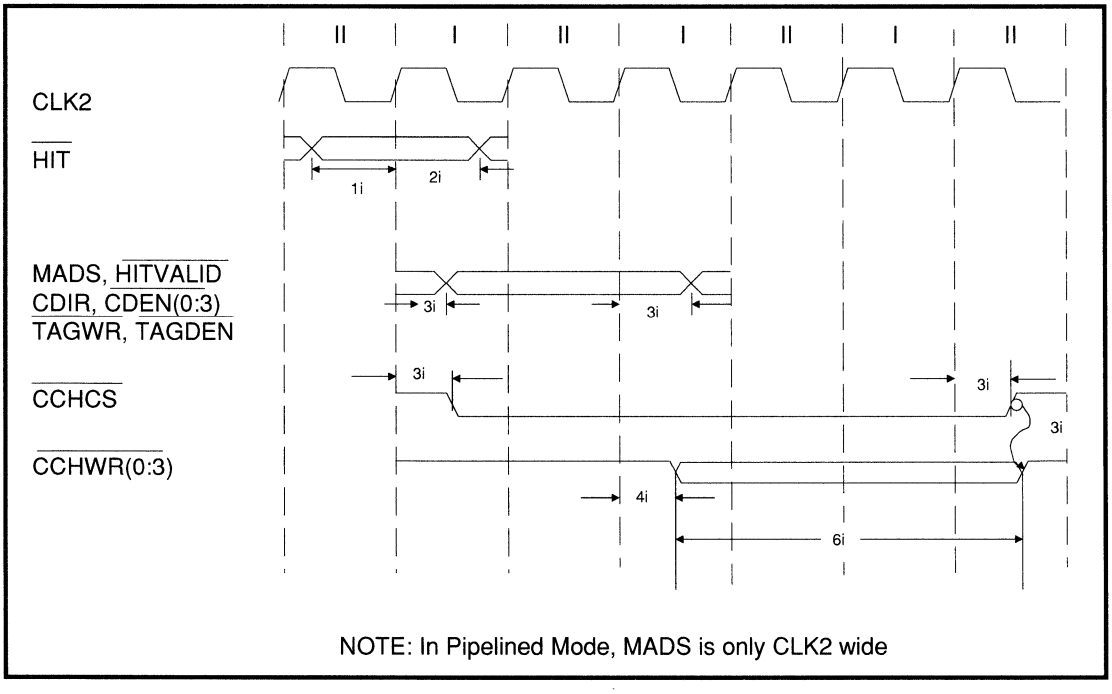


Figure 17. WD6030 Cache Interface Timing

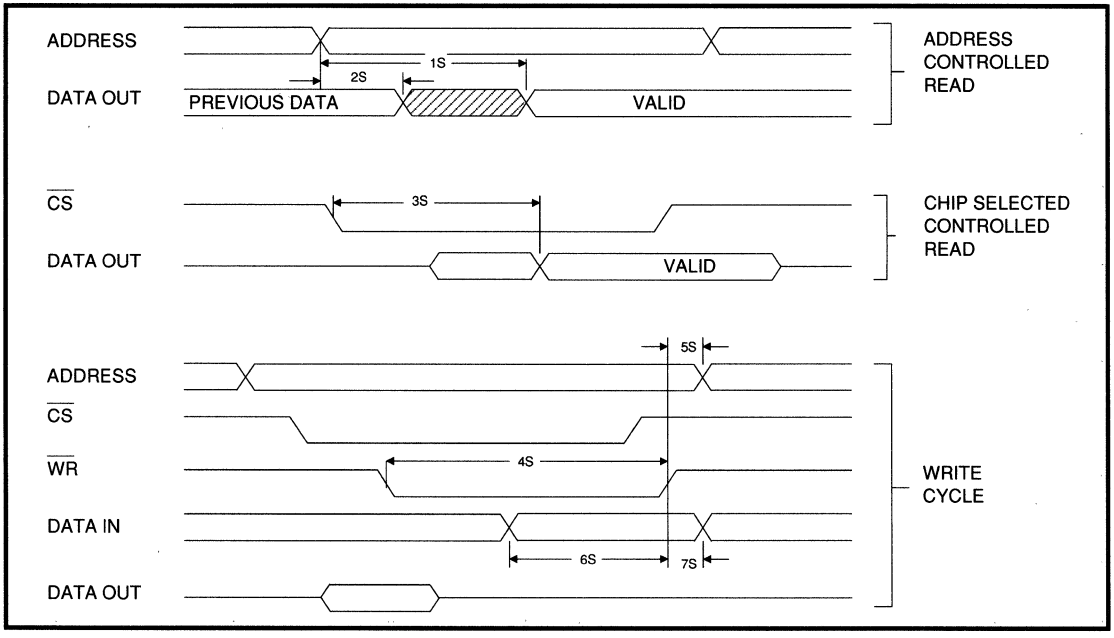


Figure 18. Data Cache SRAM Timing

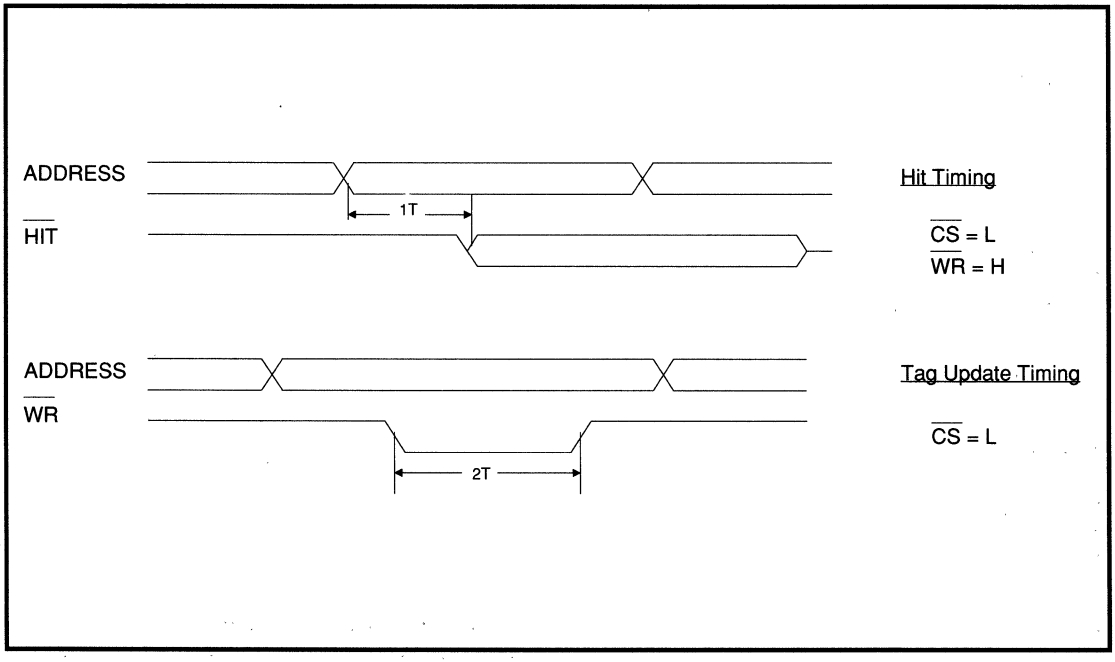


Figure 19. WD6030 TagRAM Timing

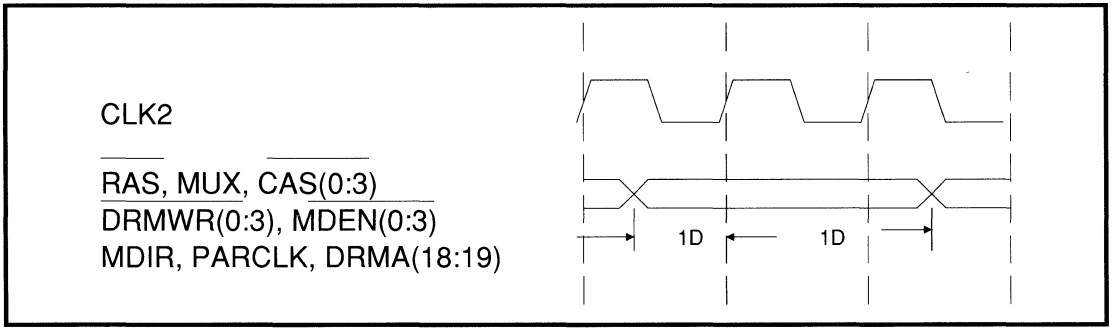


Figure 20. DRAM Interface Output Valid Delay Timing

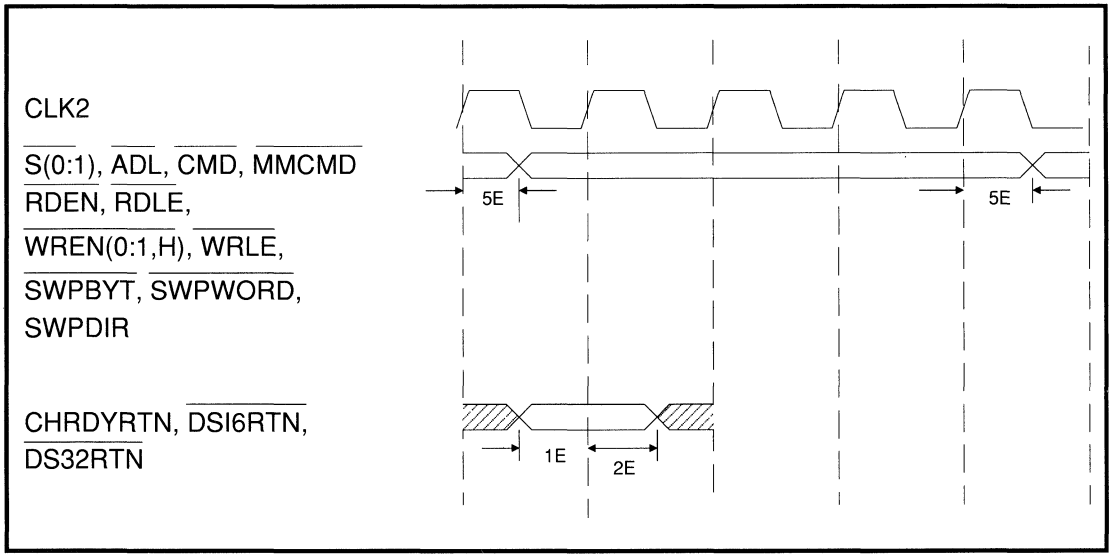


Figure 21. Channel Controller Timing

15

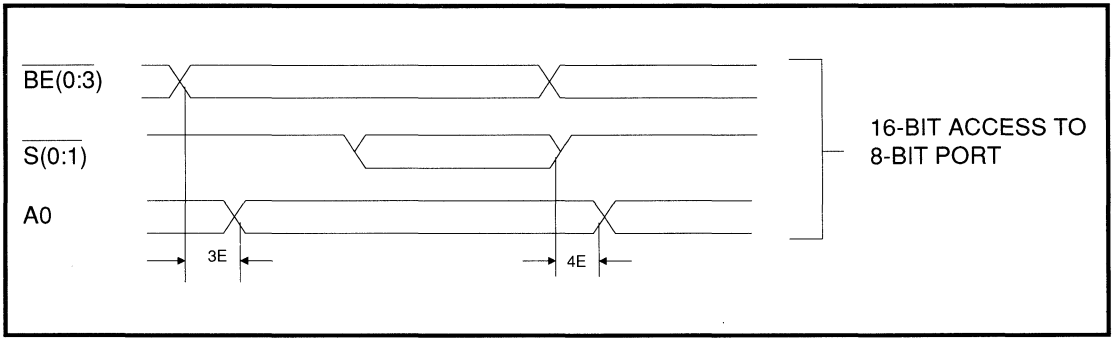


Figure 22. Channel Controller: 16-Bit Access to 8-Bit Port

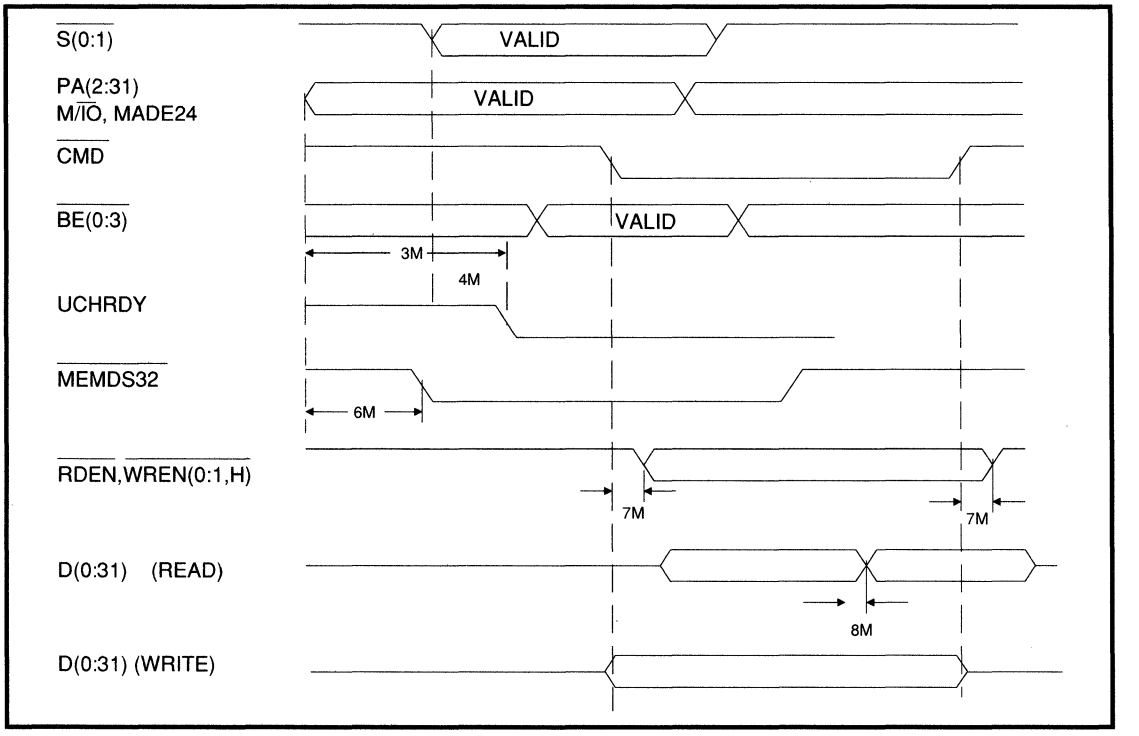


Figure 23. Channel Master Accesses to System Board DRAM

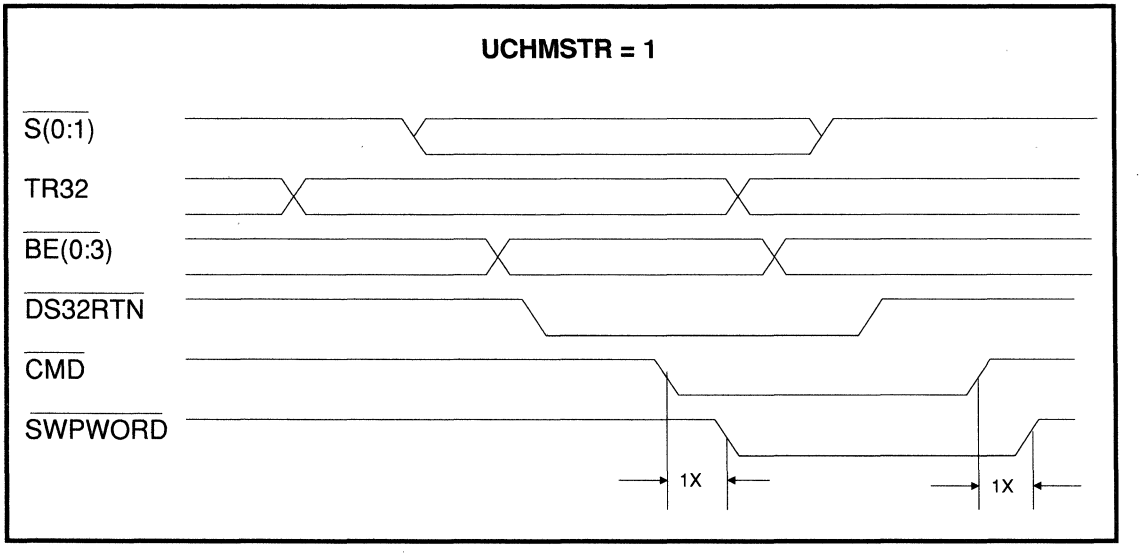


Figure 24. Central Translator Function

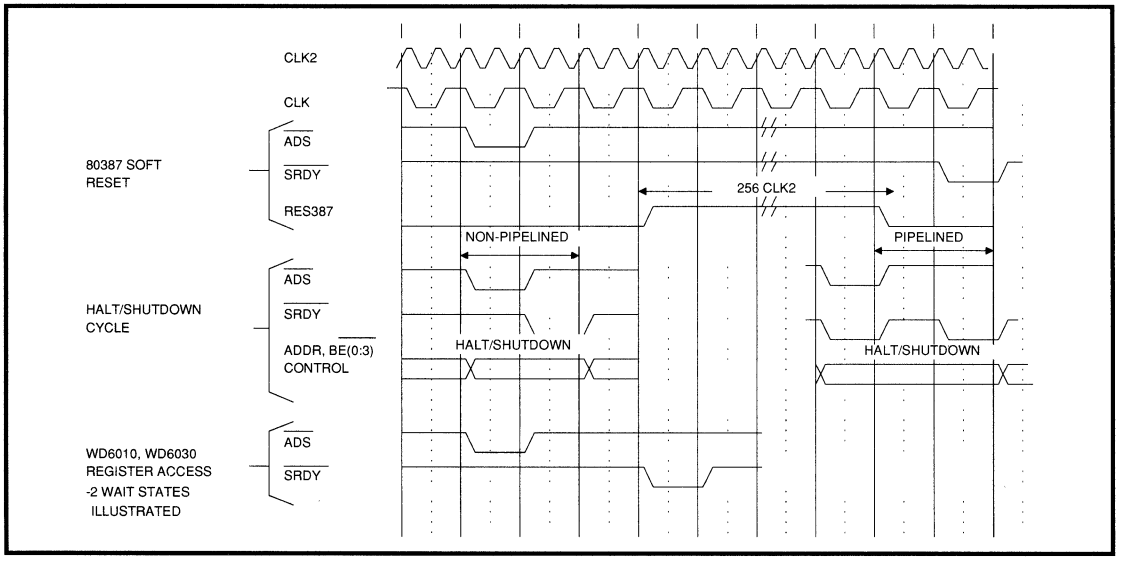


Figure 25. Miscellaneous Cycles

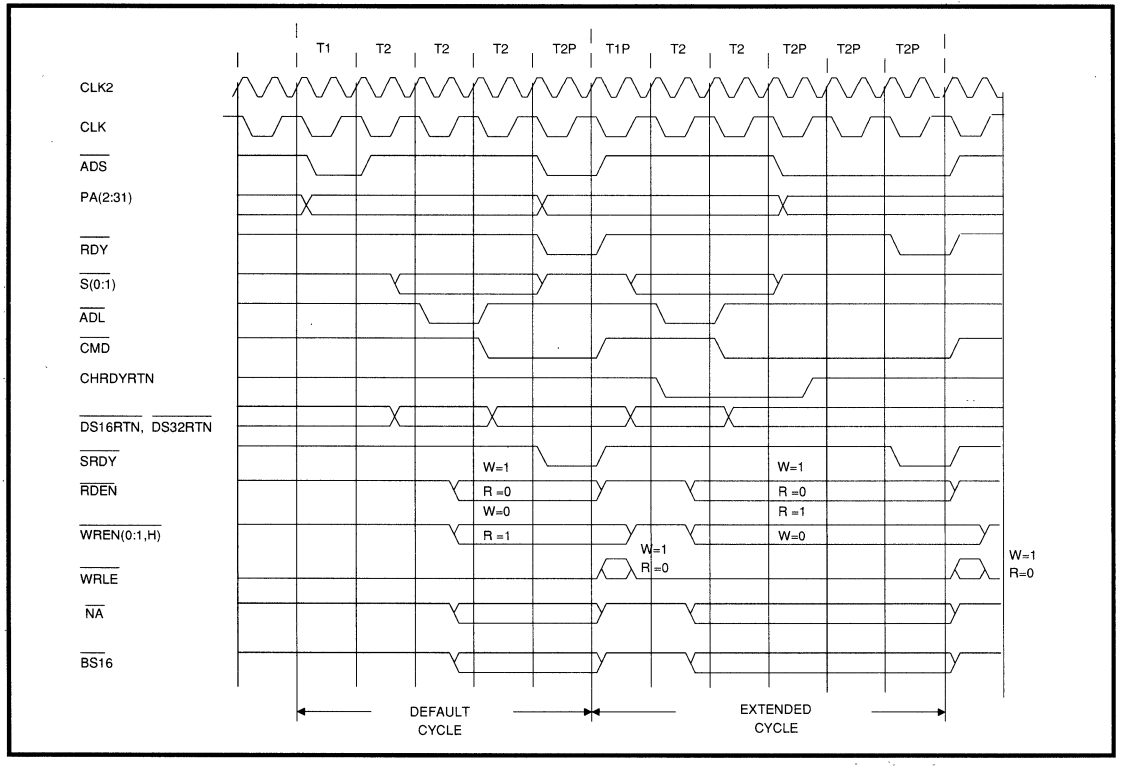


Figure 26. Channel Accesses 16 MHz Back-to-Back Cycles

15

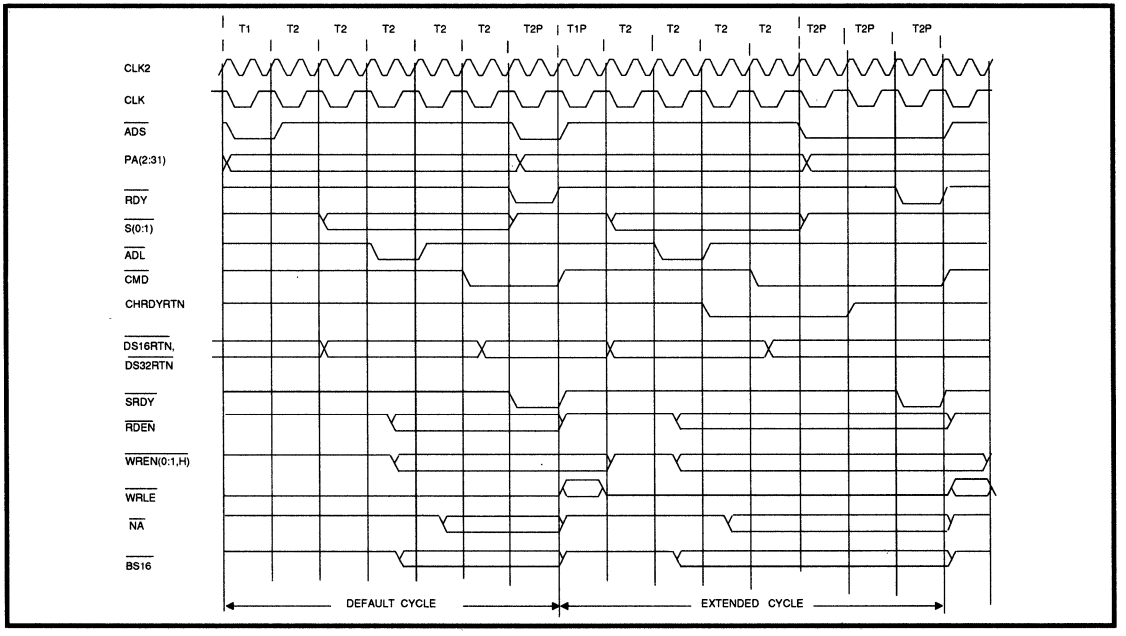


Figure 27. Channel Accesses 20 MHz Back-to-Back Cycles

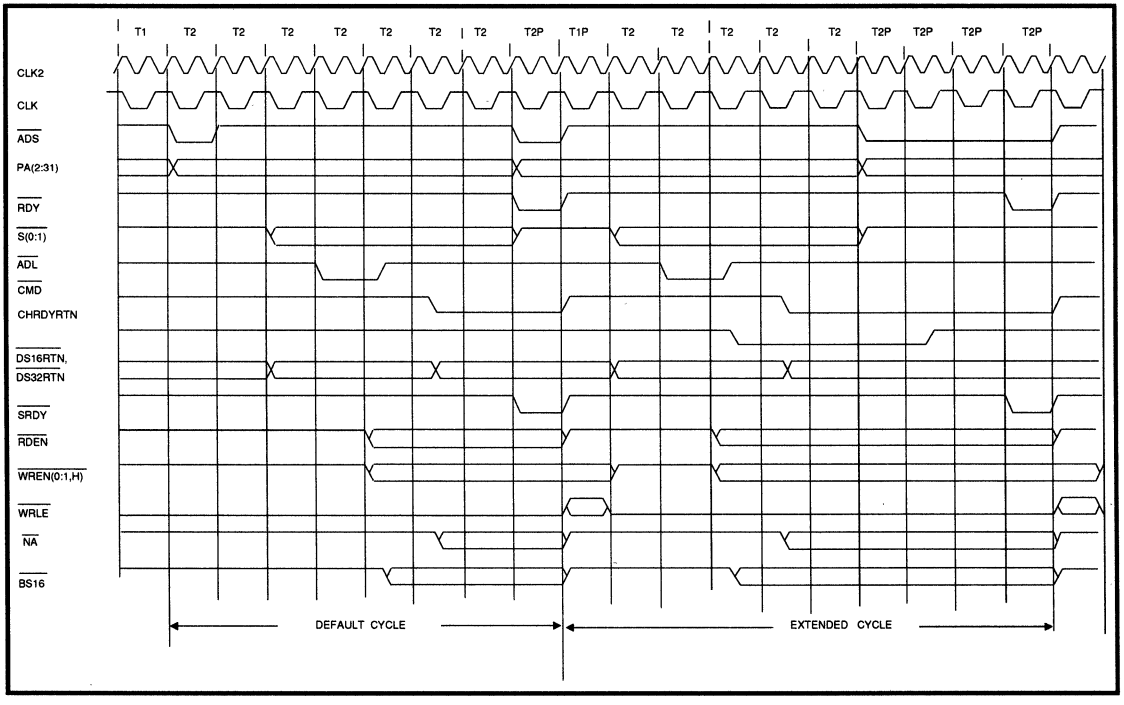


Figure 28. Channel Access 25 MHz Back-to-Back Cycles

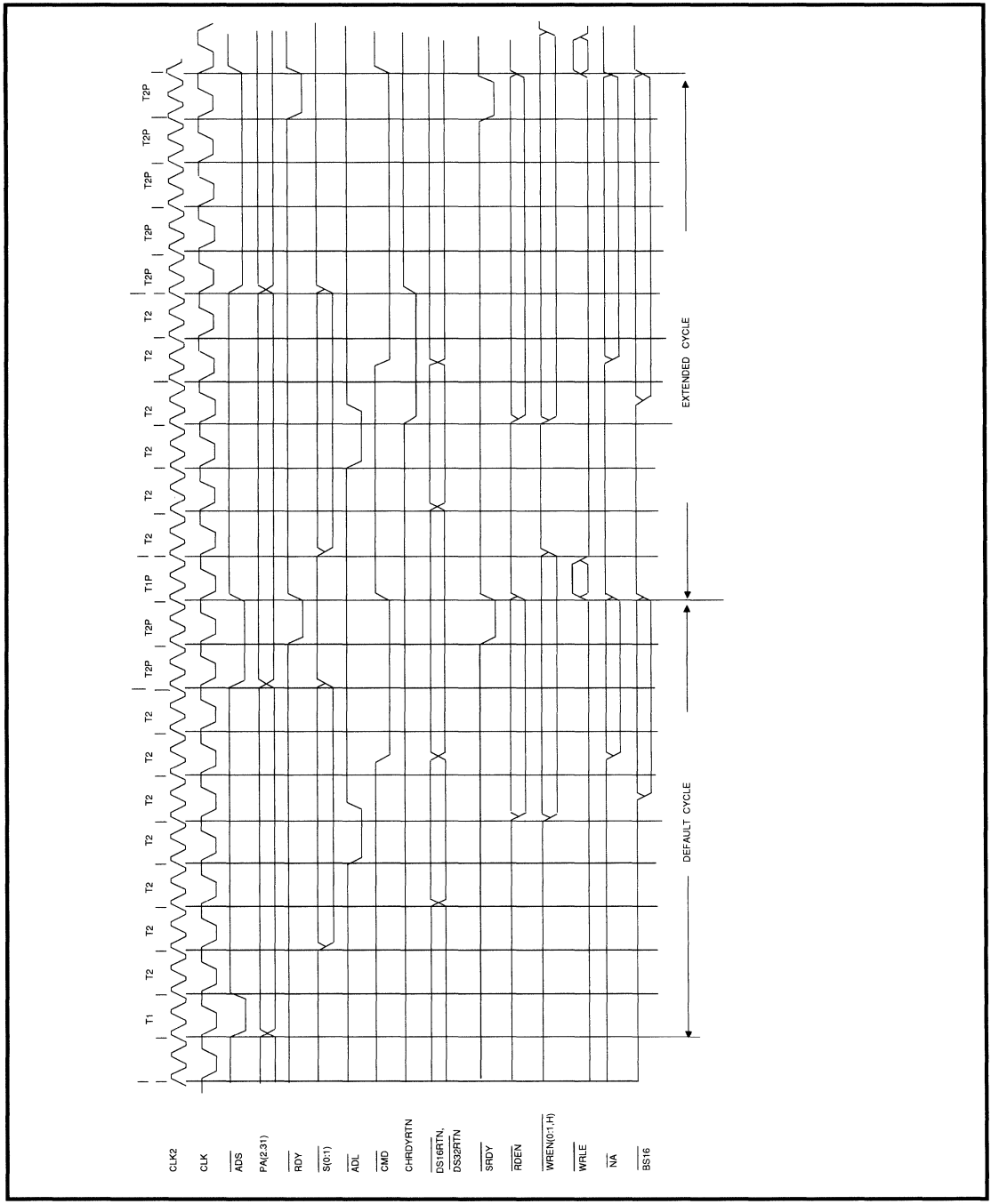


Figure 29. Channel Acess 33 MHz Back-to-Back Cycles

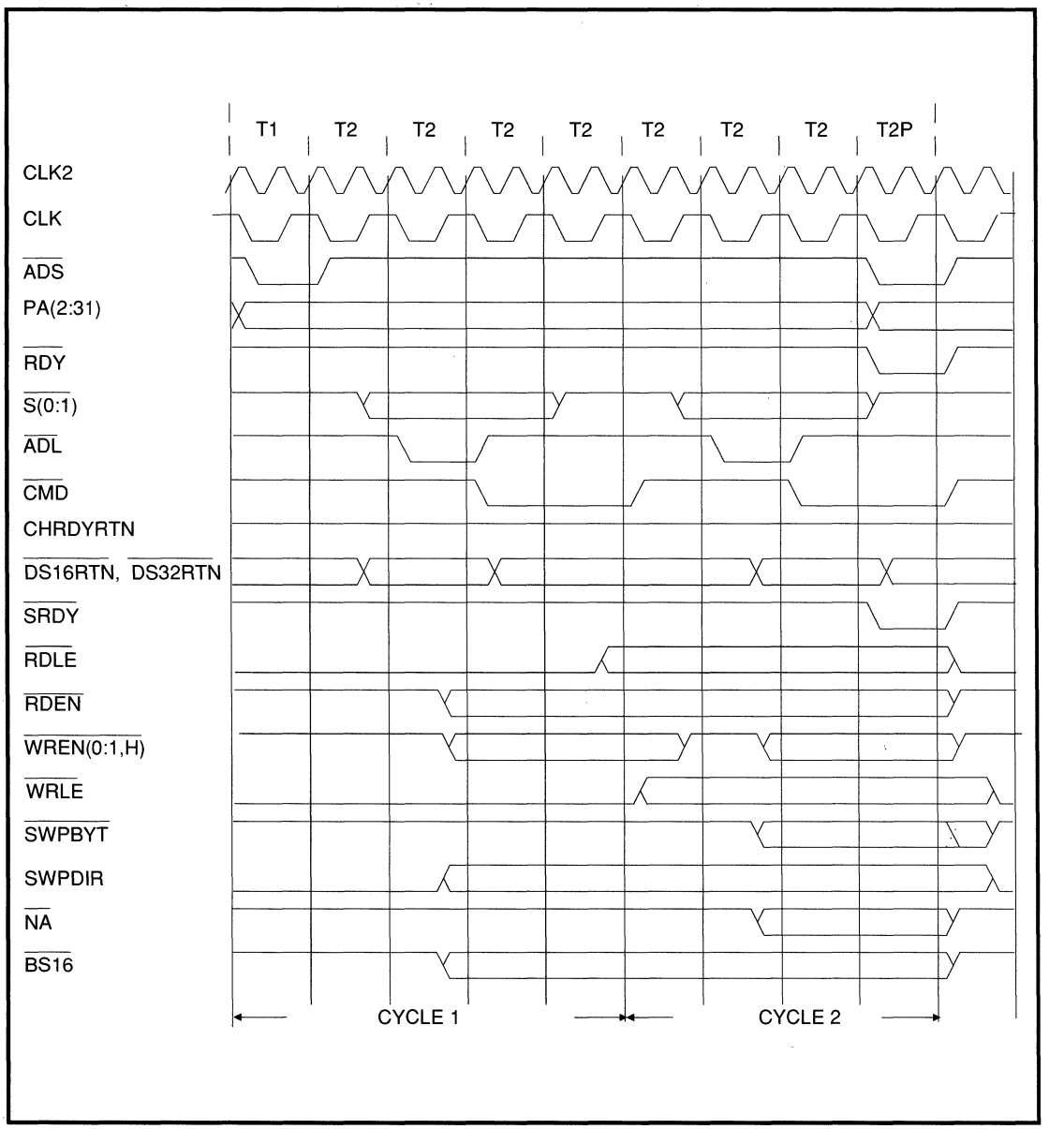


Figure 30. 16 MHz 16-Bit Access To 8-Bit Channel Port

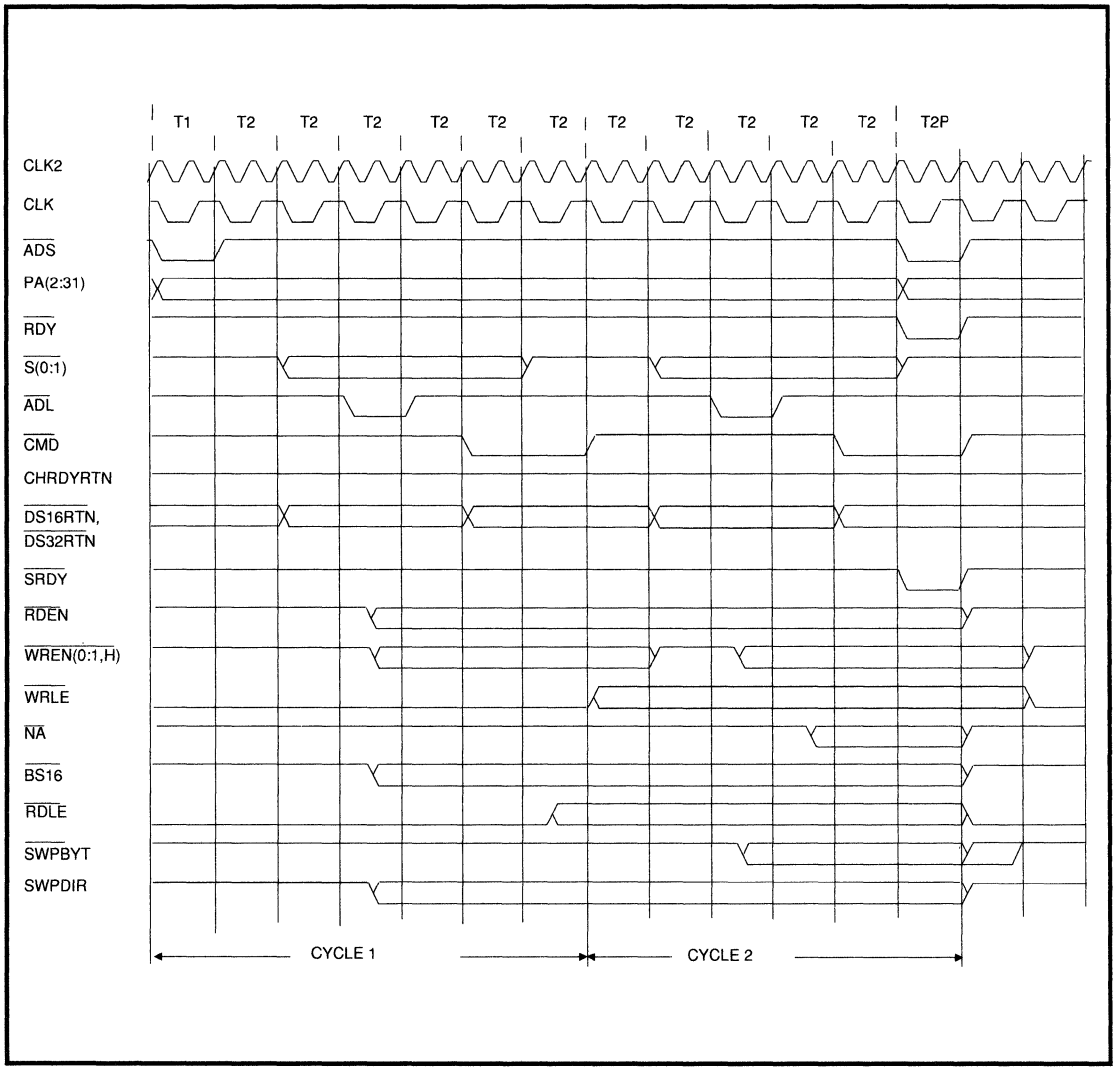


Figure 31. 20 MHz 16-Bit Access To 8-Bit Channel Port

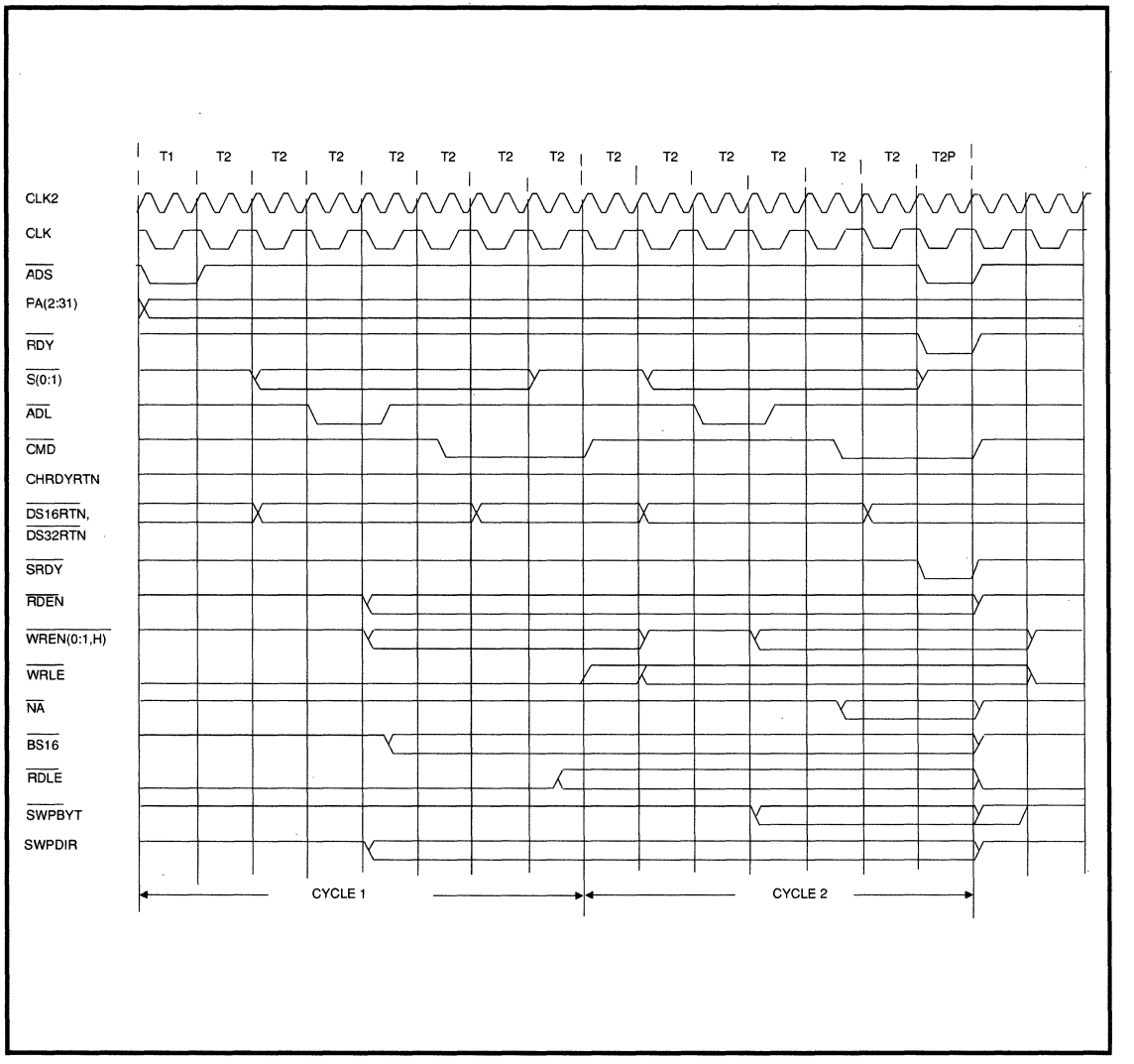


Figure 32. 25 MHz 16-Bit Access To 8-Bit Channel Port

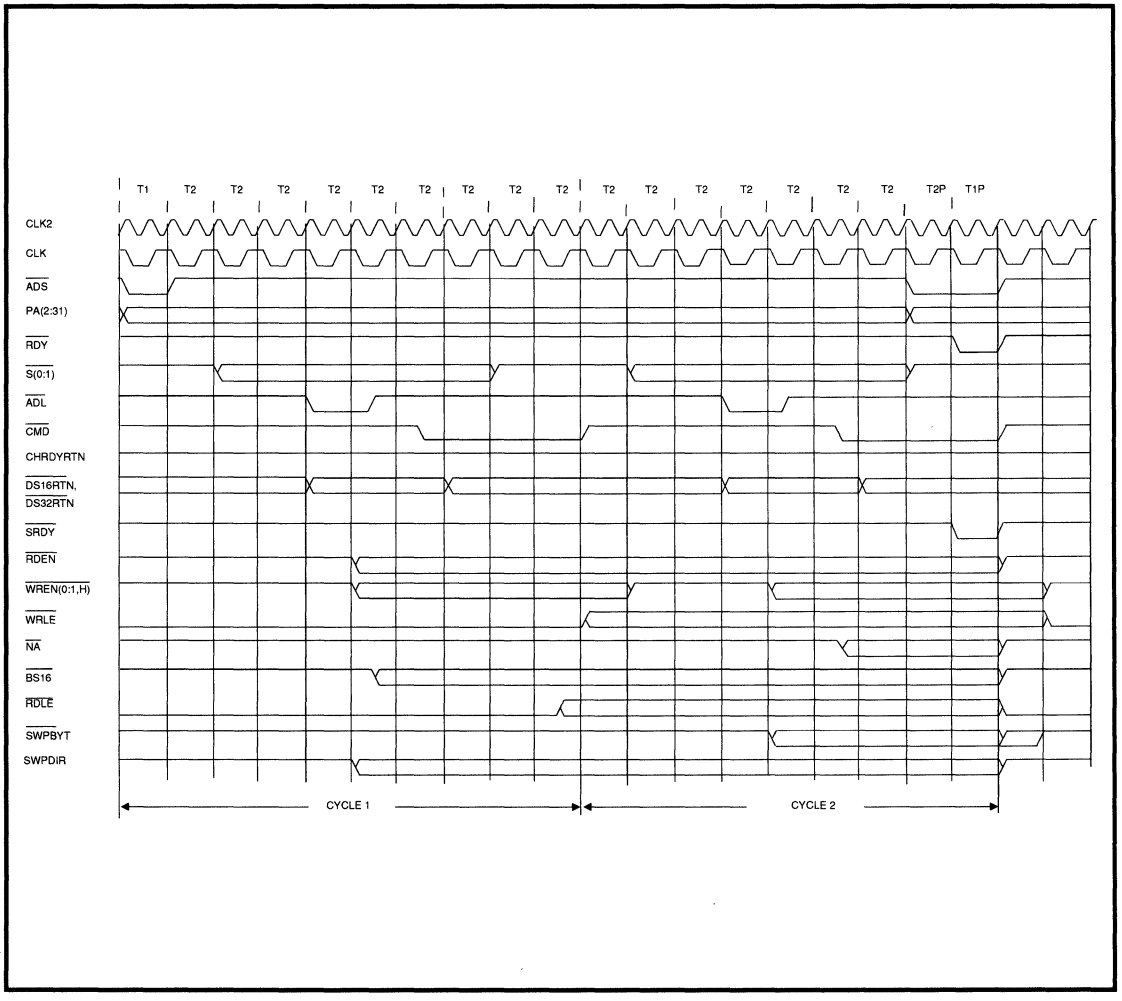


Figure 33. 33 MHz 16-Bit Access To 8-Bit Channel Port

15

10.0 PACKAGE DIMENSIONS

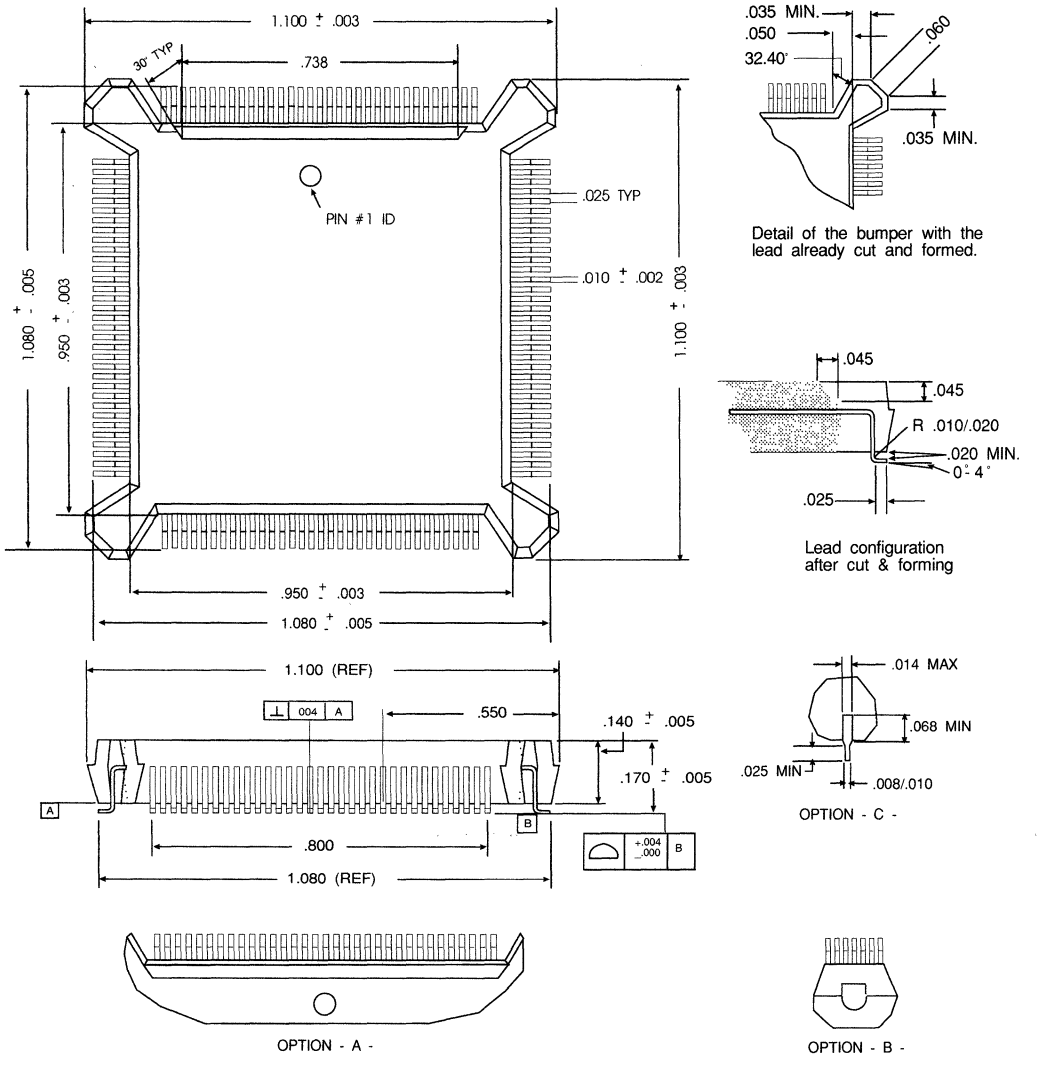


Figure 34. 132-Pin JEDEC Flat Pack Packaging Diagram

WD75C10, WD76C10, WD76C10LP System Controller for 80386SX and 80286 Desktop and Portable Compatibles

WESTERN DIGITAL

TABLE OF CONTENTS

16

Page

Page

16

LIST OF TABLES

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

1.1 DOCUMENT SCOPE

This document describes the function and operation of the WD75C10, WD76C10, and WD76C10LP System Controller devices. It includes the description of external logic necessary for efficient use of these devices. In most instances the WD75C10, WD76C10, and WD76C10LP operate similarly and will be referred to in this document as the "System Controller". Where there are differences, the devices will be identified specifically.

1.2 FEATURES

Features Common to WD75C10, WD76C10, and WD76C10LP

- Interfaces with 80286 CPU at speeds of up to 12.5 MHz
- Non-Page mode, zero wait state access, with two-way 100 nsec interleaved memory banks
- Supports 8 Mbytes of real memory, or up to 8 Mbytes of EMS 4.0 using 40 EMS multitasking registers and fast task switching
- Supports memory in four banks with 64 Kbit, 256 Kbit, or 1 Mbit DRAMs
- Employs an internal self-tuning delay line for DRAM control
- Self-adjusting output drivers minimize output rise/fall time variations and reduces EMI and ground noise
- DRAM address multiplexer drives 350 pF with adjustable strength drivers.
- Main and EGA BIOS may be mapped into one physical PROM
- Advanced 64K and 128K ROM shadowing allows main BIOS and video BIOS shadowing along with 320K and 256K remap to extended or expanded memory
- Parity generation and checking
- Low power 1.25 micron CMOS technology
- 132-pin JEDEC plastic QUAD flat package

Additional Features Of WD76C10 and WD76C10LP

- Operates at speeds of 16 MHz, 20 MHz, and 25 MHz
- Interfaces with 80286, or 80386SX CPUs
- Maintains controlled propagation delay for 80386SX reset
- Page mode zero wait state access at 25 MHz with 70 ns DRAM
- Supports 4 Mbit DRAM, up to 16 Mbyte of real memory, or 32 Mbyte of EMS memory
- Supports low-cost cache memory control for any speed 80286 or 80386SX

Additional Features Of WD76C10LP Only

- Power control with suspend and resume
- Processor stop clock
- CAS before RAS refresh for portable applications
- Automatic processor clock speed switching

1.3 GENERAL DESCRIPTION

The WD75C10 is designed for use by low cost AT compatible desktop computers using an 80286 processor at up to 12.5 MHz. The WD76C10 has all the capabilities of the WD75C10 plus the ability to operate in a high performance desktop AT computer using an 80286 or 80386SX processor up to 25 MHz. The WD76C10LP has the features of the WD76C10 and is designed to operate in a high performance laptop AT compatible computer using an 80286 or 80386SX processor.

1.3.1 WD75C10

The WD75C10 contains a high performance memory controller with programmable modes of operation. It supports two-way interleaved, non-page, zero wait state read and write memory control. A maximum of four banks of 64 Kbit, 256 Kbit, or 1 Mbit DRAM may be controlled, allowing up to 8 Mbytes of real or EMS (Expanded Memory Specification) memory. Any combination of DRAM sizes may be used.

The eight Mbytes of on-board memory can be allocated either to extended or EMS memory in 128 Kbyte increments. Forty EMS registers support EMS 4.0 multitasking.

16

An internal self-tuning delay line is used for DMA and Bus Master memory cycles. Delay line information is also used to adjust the strength of the output drivers. This stabilizes the output rise and fall times, which reduces ground noise and electromagnetic interference (EMI).

1.3.2 WD76C10

The WD76C10 supports all of the features provided by the WD75C10, as well as controlling page mode DRAM or static column DRAM with page mode operation. The WD76C10 also controls 4 Mbit DRAM, allowing up to 16 Mbytes of real memory or 32 Mbytes of EMS memory, for a maximum of 32 Mbytes of on-board memory.

EMS access to external RAM or ROM may be used to support Kanji or other extended character sets.

An external discrete logic cache controller is supported through the use of a processor ready input signal ($\overline{\text{RDYIN}}$ pin 51). If the external cache makes a zero wait state cache hit cycle, the WD76C10 aborts the DRAM cycle. The WD76C10 only makes DRAM accesses on write cycles and cache read misses.

The WD76C10 interfaces with either an 80286 or 80386SX processor. The processor type is automatically sensed at power-up. No extra logic is required to interface with the 80386SX. The variation in processor reset propagation delay is controlled to meet the strict reset timing of the 80386SX.

1.3.3 WD76C10LP

In addition to supporting all the features of the WD75C10 and WD76C10, the WD76C10LP also supports laptop portables. To provide this support, the WD76C10LP makes use of Power Management Control (PMC) for powering down peripherals or the processor, processor stop clock, slow clock and auto speed clock modes and CAS before RAS refresh. Suspend and resume is supported, where low power DRAM is refreshed while the processor and other power consuming devices are turned off. The power drain for the core logic and VGA controller is less than 1 mA in this mode. Power and clock speed may be controlled by the keyboard processor, transparently to the 80286 or 80386SX.

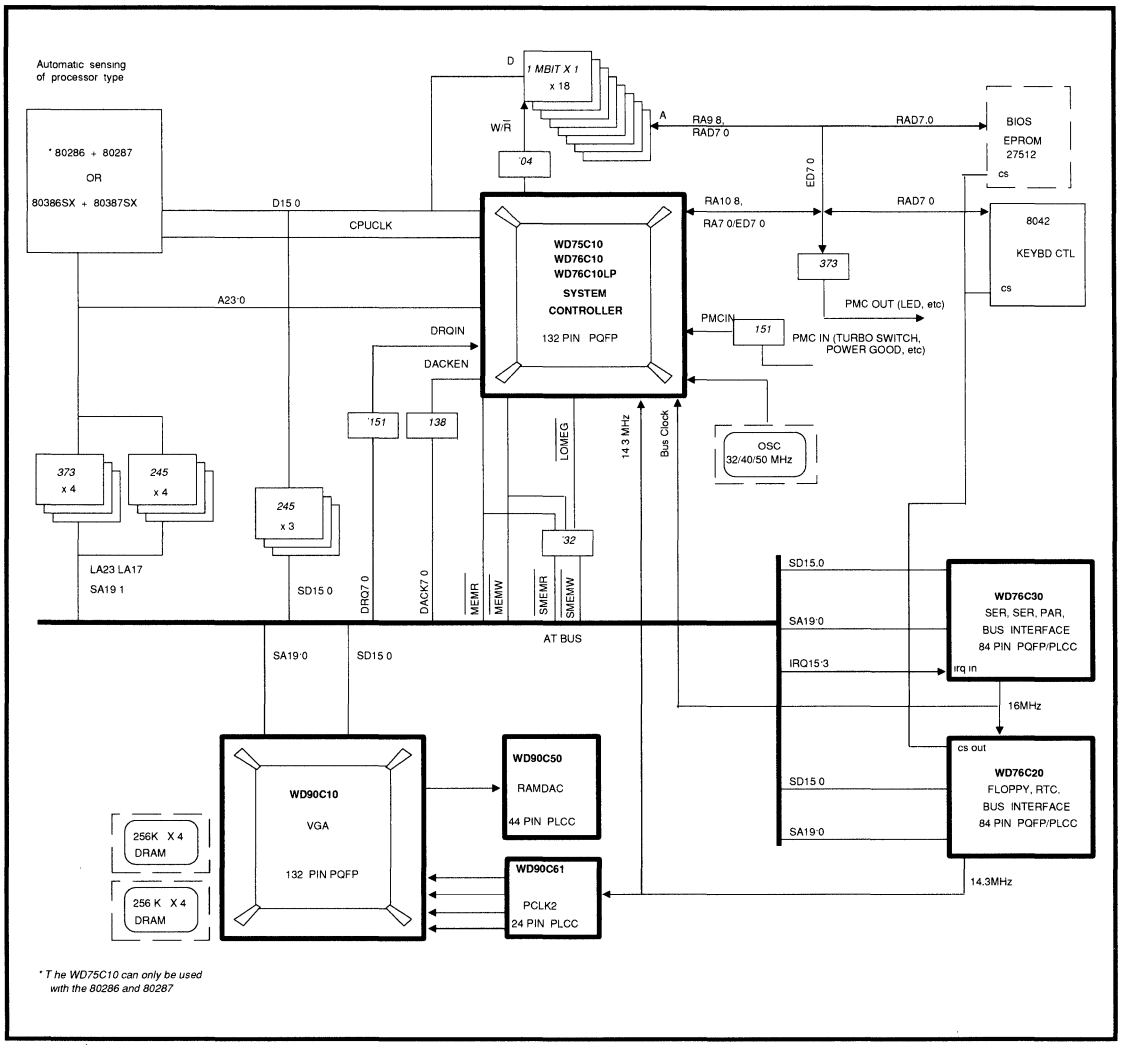


FIGURE 1-1. SYSTEM BLOCK DIAGRAM

16

2.0 ARCHITECTURE

All versions of the System Controller are comprised of eight major blocks:

- Initialization and clocking
- AT bus
- 80286/80387SX processor control
- 80287/80387SX numeric processor control
- Data bus
- Memory and EMS control
- Power Management Control
- Register File

Sections 2.1 through 2.8 provide an overview of these blocks. They are described in more detail in sections 4 through 9.

2.1 INITIALIZATION AND CLOCKING

At power up, the System Controller receives the RSTIN signal which it in turn uses to reset the AT bus and assert CPURES and NPRST to reset the main and numeric processors. The processor and AT bus resets are held for 84 processor clocks beyond the removal of the RSTIN signal. It is at this time that the type of processor in use (286, 287 or 386SX, 387SX) is determined.

CLK14 is a 14.318 MHz clock for the 8254 compatible timers and is switched by the WD76C20 to 32 KHz during a suspend and resume operation.

BCLK2 is used to generate an 8 MHz or 10 MHz bus clock and may also be used as the source for the main processor clock, CPUCLK.

2.2 AT BUS

The AT bus provides the logic necessary to control the system clock, memory read and write access, I/O read and write cycles, data bus direction, data and interrupt requests, and speaker driver.

2.3 MAIN PROCESSOR CONTROL

At the termination of reset, this block determines whether the local processor is an 80286 or 80386SX by examining the S1[W/R#] signal. The WD75C10 only interfaces with an 80286. This block also controls whether the CPUCLK is to be an input or output. While all three devices have the ability to reduce the processor clock rate, only the WD76C10LP has the ability to stop the clock to the processor. The WD76C10LP also has the ability to power down the processor, at which time it tri-states signals CPUCLK, READY, HOLD, INTRQ, and NMI.

The WD76C10 and WD76C10LP use RDYIN to support an external discrete logic cache controller.

2.4 NUMERIC PROCESSOR CONTROL

While all three System Controllers support an 80287 processor, only the WD76C10 and WD76C10LP support the 80387SX.

2.5 DATA BUS

The Data Bus is a 16 bit (two bytes) bidirectional bus that connects to the processors, System Controllers, DRAM, and to AT data bus transceivers. The parity of each DRAM byte is indicated by DPL and DPH.

2.6 MEMORY AND EMS CONTROL

This block controls the access to 16 Mbytes of real memory or 32 Mbytes of expanded memory (for the WD75C10 it is 8 Mbytes of real or 8 Mbytes of expanded memory). All versions of the System Controller supports non-page mode two-way interleaved memory. The WD76C10 and WD76C10LP also provide independent two-way or four-way interleave page mode access to the RAM banks.

2.7 POWER MANAGEMENT CONTROL

The Power Management Control (PMC) is internal logic which interfaces with external multiplexers and latches. Only the WD76C10LP makes full use of the PMC. It has the ability to power down only the main processor or the main processor and peripherals, conserving power essential to portable laptop computers. When in a power down state, the WD76C10LP tri-states the CPUCLK, READY, HOLD, INTRQ, and NMI output signals to the main processor.

2.8 REGISTER FILE

The register file provides software control of the interface signals. The function of each register is described in the same section as the logic block which it controls. Some registers, such as the Bus Timing and Power Down Control Register at port 1872, serve more than one area. In this instance the register description appears only in one section, but is referred to in all appropriate sections.

The registers and the section in which they are described are listed in Table 2-1.

In most cases, the registers are addressed by all 16 address bits, A15 through A00. Within the text, when the address is expressed as a three digit number, i.e., 092 - ALT A20 GATE and HOT RESET, only address bits A09 through A00 are used, A15 through A10 are ignored. If the address is expressed as a four digit number, all 16 address bits are used.

With the exception of the EMS Registers at port E072 and E872, all registers located at Ports 1072 through F872 are locked and inaccessible until unlocked by performing an eight bit I/O write of DA to the Lock/Unlock Register at Port F073. Writing anything other than DA locks the registers. The lock/unlock status can be determined by reading the Lock/Unlock Status Register at Port FC72 twice. If the T bit (bit 15) toggles, the registers are unlocked. If the registers are locked, the read cycle is directed to the AT bus, and the data is undetermined.

2.8.1 Lock Status Register

Port Address FC72 - Read only

15	14	13	12	11	10	09	08
T				DMA #2			
				CH3	CH2	CH1	CH0

07	06	05	04	03	02	01	00
DMA #1				P			
CH3	CH2	CH1	CH0				

Bits 11-03 are particularly usefull in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices.

Bit 15 - T, Toggle

Changes state after every read of this port.

Bits 14-12 - Not used, state is ignored

Bits 11-08 - DMA #2, Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #2. For a description of the Mask Registers refer to section 5.4.11.

0 = Channel enabled

1 = Channel disabled

Bits 07-04 - DMA #1, Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #1. For a description of the Mask Registers refer to section 5.4.11.

0 = Channel enabled

1 = Channel disabled

Bit 03 - P, Parallel Port direction

The P bit represents the state of the Direction Bit (bit 5) of the parallel port Write Control Register. For a description of this bit refer to the WD76C30 Data Book, section 6.2.5

Bits 02-00 - Not used, state is ignored

16

2.8.2 Lock/Unlock Register

Port Address F073 - Write only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
L/UL							

Bits 15-08 - Not used, state is ignored

Bits 07-00 - L/UL, Lock/Unlock

L/UL = DA -
11011010 unlocks the registers, allowing read and write access to the registers. Refer to Table 2-1 for the registers capable of being locked.

L/UL ≠ DA -
Anything other than 11011010 locks the registers. Any attempt to access a locked register I/O port address goes to the AT bus rather than the locked register.

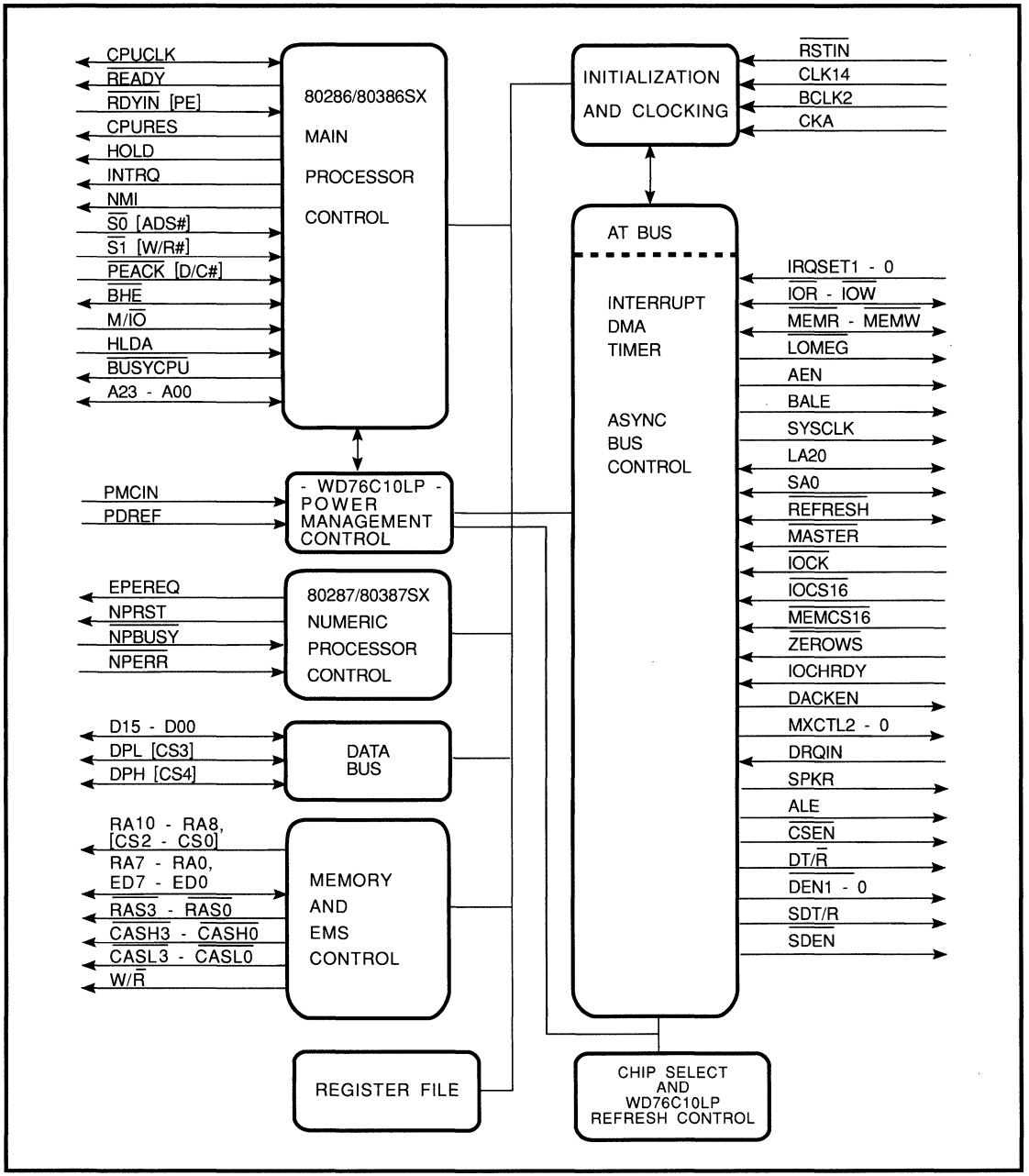


FIGURE 2-1. WD75C10, WD76C10, AND WD76C10LP BLOCK DIAGRAM

16

PORT ADDRESS	REGISTER NAME	LOCK/ UNLOCK	SECTION
000 - 00F ①	DMA Control #1 (Channel 0:3)	No	5.4, 5.6,
020 - 021 ②	Interrupt Controller #1	No	5.5
040	Timer 0, Time Of Day	No	5.7
041	Timer 1, Refresh	No	5.7
042	Timer 2, Speaker	No	5.7
043	Control Word	No	5.7
060 - 06E even	Keyboard Controller	No	7.5, Table 7-1
061 - 06F odd	Port B Parity Error And I/O Channel Check	No	5.9
070 - 07E even	Real Time Clock Address Register	No	5.8.1
071 - 07F odd	Real Time Clock Data Register	No	5.8.2
080 - 09F	(except 092) DMA Page Registers	No	
092	ALT A20 Gate and Hot Reset	No	5.8.3
0A0 - 0A1 ②	Interrupt Control Slave #2	No	5.4, 5.6
0C0 - 0DE ①	DMA Control #2 (Channel 4:7)	No	5.4
00F0	CLEAR 287 BUSY	No	5.3.2
00F1	RESET 287/387SX	No	5.3.3
1072	Clock Control	Yes	4.2.4
1872	Bus Timing And Power Down Control	Yes	5.3.1
2072	Refresh Control, Serial And Parallel Chip Selects	Yes	7.1
2872	Chip Selects	Yes	7.2
3072	Programmable Chip Select Address	Yes	7.3
3872	Memory Control	Yes	6.2.1
4072	Non-page Mode DRAM Memory Timing	Yes	6.3.1
4872	Bank 1 And Bank 0 Start Address	Yes	6.2.2
5072	Bank 3 And Bank 2 Start Address	Yes	6.2.2
5872	Split Start Address	Yes	6.2.3
6072	RAM Shadow And Write Protect	Yes	6.2.4
6872	EMS Control And Lower EMS Boundary	Yes	6.4.1
7072	PMC Output Control 7:0	Yes	8.1
7872	PMC Output Control 15:8	Yes	8.1
8072	PMC Timers	Yes	8.2
8872	PMC Inputs 7:0	Yes	8.3
9072	NMI Status	Yes	8.5
9872	Diagnostic	Yes	9.1
A072	Delay Line	Yes	9.2
B872	DMA Control Shadow	Yes	5.4.15
C072	High Memory Write Protect Boundary	Yes	6.2.5
C872	PMC Interrupt Enables	Yes	8.4
D072	Shadow Register		8.6
E072	EMS Page Register Pointer	No	6.4.2
E872	EMS Page Register	No	6.4.3
F072	48 MHz Oscillator Disable	Yes	7.5, Table 7-1
F472	48 MHz Oscillator Enable	Yes	7.5, Table 7-1
F872	Cache Flush	Yes	7.4
FC72	Lock Status	Yes	2.8.1
F073	Lock/Unlock	Yes	2.8.2

① See Table 5-4. DMA Controller/Channel Function Map
② See Table 5-6. Interrupt Controller Function Map

TABLE 2-1. REGISTER INDEX

3.0 PIN DESCRIPTION

The signals are listed according to their pin number in Table 3-1. The signals are grouped according to their application and described in Table 3-2.

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
1 - RA5/ED5	36 - LOMEG	68 - D11	103 - A8
2 - Vcc	37 - MEMW	69 - Vcc	104 - A7
3 - RA4/ED4	38 - MEMR	70 - D12	105 - A6
4 - RA3/ED3	39 - IOW	71 - D13	106 - A5
5 - Vss	40 - IOR	72 - D14	107 - A4
6 - RA2/ED2	41 - BHE	73 - D15	108 - A3
7- -RA1/ED1	42 - NPERR	74 - DT/R	109 - A2
8 - RA0/ED0	43 - PEACK [D/C#]	75 - DEN1	110 - IRQSET1
9 - CASH2	43 - WD75C10	76 - DEN0	111 - IRQSET0
10 - CASL2	NOT USED	77 - SYSCLK	112 - MXCTL0
11 - RAS2	44 - M/IO	78 - CPURES	113 - MXCTL1
12 - CASH3	45 - S0 [ADS#]	79 - BALE	114 - MXCTL2
13 - CASL3	46 - S1 [W/R#]	80 - A23	115 - CSEN
14 - RAS3	47 - READY	81 - A22	116 - DACKEN
15 - DPH [CS4]	48 - HLDA	82 - A21	117 - RESERVED -
16 - DPL [CS3]	49 - HOLD	83 - IOCK	WD75C10
17 - RSTIN	50 - BCLK2	84 - CLK14	117 - PDREF -
18 - DRQIN	51 - RDYIN [CKA]	85 - NPBUSY	WD76C10LP
19 - IOCHRDY	[PE]	86 - A0 [BLE#]	118 - PMCIN
20 - ZEROWS	52 - CPUCLK	87 - A1	119 - W/R
21 - IOCS16	53 - BUSYCPU	88 - A20	120 - CASH0
22 - MEMCS16	54 - NMI	89 - A19	121 - CASL0
23 - SPKR	55 - INTRQ	90 - A18	122 - RAS0
24 - SA0	56 - D0	91 - A17	123 - CASH1
25 - LA20	57 - D1	92 - A16	124 - CASL1
26 - MASTER	58 - D2	93 - A15	125 - RAS1
27 - ALE	59 - D3	94 - A14	126 - RA10 [CS2]
28 - AEN	60 - D4	95 - A13	127 - RA9 [CS1]
29 - SDEN	61 - D5	96 - A12	128 - RA8 [CS0]
30 - SDT/R	62 - D6	97 - A11	129 - Vss
31 - Vcc	63 - D7	98 - Vss	130 - RA7/ED7
32 - REFRESH	64 - D8	99 - Vss	131 - RA6/ED6
33 - Vss	65 - D9	100 - A10	132 - Vss
34 - EPEREQ	66 - D10	101 - Vcc	
35 - NPRST	67 - Vss	102 - A9	

TABLE 3-1. PIN ASSIGNMENTS

NOTE: Some pins are multi-functional depending upon the mode of operation. The alternate signal for these pins is enclosed in [].

16

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		INITIALIZATION AND CLOCKING		
17	$\overline{\text{RSTIN}}$	System Reset	I	$\overline{\text{RSTIN}}$ drives a CMOS input level Schmitt Trigger and is used to reset the entire system at power up. For a detailed description, refer to Section 4, Initialization And Clocking.
50	BCLK2	Bus Clock	I	BCLK2 is used to generate an 8 MHz or 10 MHz expansion bus clock. For an 8 MHz bus, BCLK2 is a 16 MHz or 32 MHz signal. For a 10 MHz bus clock, BCLK2 is a 20 or 40 MHz input. BCLK2 may also be used to drive the processor clock. For additional information, refer to section 4, Initialization And Clocking.
84	CLK14	Clock 14	I	CLK14 is derived from a 14.3 MHz oscillator and is used internally for the 8254 compatible timers. CLK14 is externally switched to 32 KHz during a suspend and resume.
		AT BUS		
40	$\overline{\text{IOR}}$	I/O Read	I/O	$\overline{\text{IOR}}$ is an output and asserted by the System Controller during processor or DMA access to indicate that an I/O read operation is to take place on the AT bus. $\overline{\text{IOR}}$ is an input during Master Mode.
39	$\overline{\text{IOW}}$	I/O Write	I/O	$\overline{\text{IOW}}$ is an output and asserted by the System Controller during processor or DMA access to indicate that an I/O write operation is to take place on the AT bus. $\overline{\text{IOW}}$ is an input during Master Mode.
38	$\overline{\text{MEMR}}$	Memory Read	I/O	$\overline{\text{MEMR}}$ is an output and is asserted by the System Controller when a memory read access to the AT bus is to take place. $\overline{\text{MEMR}}$ is an input during Master Mode.

TABLE 3-2. PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		AT BUS (cont.)		
37	$\overline{\text{MEMW}}$	$\overline{\text{Memory Write}}$	I/O	$\overline{\text{MEMW}}$ is an output and asserted by the System Controller when a memory write access to the AT bus is to take place. $\overline{\text{MEMW}}$ is an input during Master Mode.
36	$\overline{\text{LOMEG}}$	First Megabyte	O	$\overline{\text{LOMEG}}$ is asserted when the AT bus address is below 1 Mbyte. Used with $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ to generate $\overline{\text{SMEMR}}$ and $\overline{\text{SMEMW}}$.
28	AEN	Address Enable	O	AEN is asserted by the System Controller while performing DMA and Refresh cycles.
79	BALE	AT Bus Address Latch Enable	O	Address Latch Enable for the AT bus. BALE is synchronous with the Bus Clock (BCLK2).
77	SYSCLK	System Clock	O	In asynchronous bus mode, SYSCLK is equal to BCLK2 divided by two when BCLK2 is less than 28 MHz, and divided by four when BCLK2 is greater than 28 MHz. In synchronous bus mode, SYSCLK is equal to CPUCLK divided by two or four, depending on the programming.
25	LA20	Early Address 20	I/O	When not in Master Mode, LA20 is an output and is asserted by the System Controller to place address 20 on the AT Bus LA20 line. When in Master Mode, LA20 is an input and is asserted by the Bus Master to place address on A20.
24	SA0	System Address 0	I/O	When not in Master Mode, SA0 is an output and is asserted by the System Controller to place address 00 on the AT Bus SA0 line. When in Master Mode, SA0 is an input and is asserted by the Bus Master to place address on A0.

TABLE 3-2. PIN DESCRIPTION cont.

16

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		AT BUS (cont.)		
32	$\overline{\text{REFRESH}}$	$\overline{\text{Refresh}}$	I/O	As an output, $\overline{\text{REFRESH}}$ is asserted by the System Controller to refresh memory on the AT Bus. As an input, $\overline{\text{REFRESH}}$ is asserted by the Bus Master in conjunction with $\overline{\text{MEMR}}$ to refresh memory on the AT Bus and DRAM controlled by the System Controller.
26	$\overline{\text{MASTER}}$	$\overline{\text{Master}}$	I	$\overline{\text{MASTER}}$ is asserted by the Bus Master to indicate that a Bus Master cycle is occurring. This causes LA20, SA0, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$, and $\overline{\text{IOW}}$ to become input signals.
83	$\overline{\text{IOCK}}$	$\overline{\text{I/O Check}}$	I	When asserted, $\overline{\text{IOCK}}$ indicates a bus or memory error is on the AT bus and generates an NMI to the processor.
21	$\overline{\text{IOCS16}}$	$\overline{\text{16 Bit I/O Cycle}}$	I	Initiates a 16 bit I/O AT bus cycle.
22	$\overline{\text{MEMCS16}}$	$\overline{\text{16 Bit Memory Cycle}}$	I	Initiates a 16 bit memory AT bus cycle.
20	$\overline{\text{ZEROWS}}$	$\overline{\text{Zero Wait States}}$	I	Initiates a zero wait AT bus cycle.
19	IOCHRDY	I/O Channel Ready	I	Initiates wait states during AT bus cycles.
116	DACKEN	DACK Enable	O	When DACKEN is asserted, MXCTL2-0 are used to generated DACK7-5, 3-0, and BUS_RST. Refer to Table 5-1 and Figure 5-1.
114	MXCTL2	Multiplexer Control 2	O	MXCTL2 - MXCTL0, along with DRQIN, DACKEN, IRQSET1, IRQSET0, and PMCIN, control the external multiplexer for the selection of DRQs, DACKs, IRQs, ROM8, and A20GT. Refer to Table 5-1 and Figure 5-1.
113	MXCTL1	Multiplexer Control 1	O	
112	MXCTL0	Multiplexer Control 0	O	

TABLE 3-2. PIN DESCRIPTION cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		AT BUS (cont.)		
18	DRQIN	Multiplexed DRQ Inputs	I	DRQIN, along with MXCTL2 - 0, selects one of the DRQs or CLOCK_DIR_IN. Refer to Table 5-1 and Figure 5-1.
110	IRQSET1	Interrupt Request Set 1	I	IRQSET1, along with MXCTL2 - 0, selects one of the of the following: A20GT, IRQ1, IRQ3 - IRQ7, IRQ12. Refer to Table 5-1 and Figure 5-1.
111	IRQSET0	Interrupt Request Set 0	I	IRQSET0, along with MXCTL2 - 0, selects one of the following: ROM8, CPURES, IRQ8, IRQ9 - IRQ11, IRQ14, and IRQ15. Refer to Table 5-1 and Figure 5-1.
23	SPKR	Speaker	O	SPKR drives the speaker transistor and is used for diagnostics.
27	ALE	Address Latch Enable	O	ALE is used to clock the SA1 - SA19 address latches.
115	$\overline{\text{CSEN}}$	Chip Select Enable	O	When asserted, DPH, DPL, and RA10-RA8 are used to generate one of 24 different chip selects.
74	DT/$\overline{\text{R}}$	Data Transmit/ Receive	O	DT/$\overline{\text{R}}$ controls the direction of the AT Data Bus D00 - D15. When DT/$\overline{\text{R}}$ is high, data is directed to the AT Bus. When DT/$\overline{\text{R}}$ is low, data is transferred from the AT bus.
76	$\overline{\text{DEN0}}$	Data Bus Enable 0	O	When asserted, $\overline{\text{DEN0}}$ enables the low order byte data buffer.
75	$\overline{\text{DEN1}}$	Data Bus Enable 1	O	When asserted, $\overline{\text{DEN1}}$ enables the high order byte data buffer.
29	$\overline{\text{SDEN}}$	Swap Data Enable	O	$\overline{\text{SDEN}}$ enables the data transfer between high and low bytes of the AT Bus.

TABLE 3-2. PIN DESCRIPTION cont.

16

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		AT BUS (cont.)		
30	SDT/$\overline{R}$	Swap Data Transmit/ $\overline{\text{Receive}}$	O	When SDT/$\overline{R}$ is high, it directs data from the low byte of the AT Bus to the high byte. When SDT/$\overline{R}$ is low, it directs data from the high byte of the AT bus to the low byte.
		MAIN PROCESSOR CONTROL		
52	CPUCLK	Processor Clock	I/O	CPUCLK speed and whether it is to be an input or output, is selected by the CPU Clock Control Register at port address 1072. It is normally selected as an output to drive the processor but may be selected as an input from an external processor clock driver.
47	$\overline{\text{READY}}$	$\overline{\text{Processor Ready}}$	O	$\overline{\text{READY}}$ is an output to the processor.
51	$\overline{\text{RDYIN}}$/CKA/ PE	$\overline{\text{Processor Ready In}}$/ Alternate Clock/ Parity Error	I	Whether pin 51 is to be used as $\overline{\text{RDYIN}}$, CKA, or PE is determined by the Memory Control Register at port address 3872. $\overline{\text{RDYIN}}$ is used in a discrete cache system and indicates a hit or miss. CKA may be used as an alternate source for CPUCLK processor clock. When used as PE, it indicates a parity error from an external memory controller.
78	CPURES	Main Processor Reset	O	CPURES is a synchronous processor reset signal.
49	HOLD	Hold Request	O	Processor hold cycle request.
55	INTRQ	Interrupt Request	O	Processor interrupt cycle request.
54	NMI	Non-Maskable Interrupt	O	Processor non-maskable interrupt cycle request.
45	$\overline{\text{S0}}$ [ADS#]	$\overline{\text{Processor Status 0}}$ [Address Status]	I	In the 80286 mode this pin is $\overline{\text{S0}}$. In the 80386SX mode this pin is ADS#.

TABLE 3-2. PIN DESCRIPTION cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		MAIN PROCESSOR CONTROL (cont.)		
46	$\overline{S1}$ [W/R#]	Processor Status 1 [Write Read]	I	In the 80286 mode pin 46 is $\overline{S1}$. In the 80386SX mode pin 46 is W/R#
4	$\overline{BHE}$	Bus High Enable	I/O	As an input, $\overline{BHE}$ indicates a transfer of the high byte on the processor data bus. $\overline{BHE}$ is an output during DMA transfers.
43	$\overline{PEACK}$ [D/C#]	Processor Extension Acknowledge [Data/Control]	I	In the 80286 mode pin 43 is $\overline{PEACK}$. In the 80387SX mode pin 43 is D/C#. This pin is not used by the WD75C10.
44	M/$\overline{IO}$	Memory or $\overline{I/O}$	I	Processor Memory cycle or $\overline{I/O}$ Status cycle.
48	HLDA	Hold Acknowledge	I	Processor hold acknowledge.
53	$\overline{BUSYCPU}$	Processor Busy	O	Numeric Processor Busy (80287 or 80387SX) signal to CPU (80286 or 80386SX).
80 - 82 88 - 97 100 102 - 109 87 86	A23 - A21 A20 - A11 A10 A9 - A2 A1 A0, [BLE#]	Processor Address A23 through A00, Bus Low Enable	I/O	A23 through A1 are address lines from the 80286 or 80386SX. A0 is address bit A0 for the 80286, BLE# for the 80386SX, and is controlled by SA0 (AT Bus pin 24) during Master Mode operations. A21, A19 through A1 are outputs during refresh and DMA cycles and inputs in other modes. A20 and A0 are outputs during refresh, DMA and Master mode cycles, and inputs in other modes.

TABLE 3-2. PIN DESCRIPTION cont.

16

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		NUMERIC PROCESSOR CONTROL		
34	EPEREQ	Extend PERQ	O	PERQ extend signal to the 80386 for IRQ13 handling. Used only for the 80386SX.
35	NPRST	Numeric Processor Reset	O	Reset to the numeric processor 80287 or 80387SX.
42	NPERR	Numeric Processor Error	I	Error signal from the numeric processor 80287 or 80387SX.
85	NPBUSY	Numeric Processor Busy	I	Busy signal from the numeric processor 80287 or 80387SX.
		DATA BUS		
73 - 70 68 66 - 56	D15 - D12 D11 D10 - D0	Data Bit 15 - Data Bit 12, Data Bit 11 Data Bit 10 - Data Bit 0	I/O	The Data Bits are connected directly to the Local and Numeric processors, DRAM data, and AT Bus data transceivers.
16	DPL [CS3]	Data Parity Low Byte [Chip Select 3}	I/O	For DRAM cycles, DPL is the low byte parity bit. For I/O cycle, CS3 is bit three of the encoded chip select bus.
15	DPH [CS4]	Data Parity High Byte [Chip Select 4]	I/O	For DRAM cycles, DPH is the high byte parity bit. For I/O cycle, CS4 is bit four of the encoded chip select bus.
		MEMORY AND EMS CONTROL		
126 - 128	RA10/CS2 RA9/CS1 RA8/CS0	DRAM Address Bit 10 through DRAM Address Bit 8, Chip Select 2 through Chip Select 0	O	The DRAM Address Bus is multi-functional. During DRAM cycles, RA10 through RA0 select the DRAM Row and Column.
130, 131 1, 3, 4, 6 - 8	RA7/ED7 RA6/ED6 RA5/ED5 RA4/ED4 RA3/ED3 RA2/ED2 RA1/ED1 RA0/ED0	DRAM Address Bit 7 through DRAM Address Bit 0, EDATA 7 through 0	I/O	During I/O cycles, CS2 through CS0, along with CS4 and CS3, are decoded by external logic to one of 32 possible Chip Selects. ED7 through ED0 represents the data from such devices as the Keyboard Controller on the EDATA bus.

TABLE 3-2. PIN DESCRIPTION cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		MEMORY AND EMS CONTROL (cont.)		
14, 11, 125, 122	$\overline{RAS3}$ $\overline{RAS2}$ $\overline{RAS1}$ $\overline{RAS0}$	Row Address Select 3 through Row Address Select 0	O	$\overline{RAS3}$ through $\overline{RAS0}$ are designed to access the DRAM without the use of external drivers.
12, 9, 123, 120	$\overline{CASH3}$ $\overline{CASH2}$ $\overline{CASH1}$ $\overline{CASH0}$	Column Address Select High 3 through Column Address Select High 0	O	$\overline{CASH3}$ through $\overline{CASH0}$ are designed to access the DRAM without the use of external drivers.
13, 10, 124, 121	$\overline{CASL3}$ $\overline{CASL2}$ $\overline{CASL1}$ $\overline{CASL0}$	Column Address Select Low 3 through Column Address Select Low 0	O	$\overline{CASL3}$ through $\overline{CASL0}$ are designed to access the DRAM without the use of external drivers.
119	W/$\overline{R}$	Write/$\overline{Read}$	O	W/$\overline{R}$ is output as a high signal to write to memory and output as a low signal to read from memory. W/$\overline{R}$ should be buffered before use.
		POWER MANAGEMENT CONTROL		
117	PDREF	Power Down Refresh	I	PDREF is a 64 KHz signal from the WD76C20. During power down, PDREF is passed internally to pin 32 ($\overline{REFRESH}$).
118	PMCIN	Power Management Control Input	I	PMCIN is used to sample eight PMC inputs. See Table 5-1 and Figure 5-1.
		MISCELLANEOUS		
5, 33, 67, 98, 99, 129 132	Vss		I	Ground (7 pins)
2, 31, 69, 101	Vcc		I	+5 Volts (4 pins)

TABLE 3-2. PIN DESCRIPTION cont.

16

4.0 INITIALIZATION AND CLOCKING

This section describes the system Master Reset (RSTIN) operation, control of internal clock (CLK14), bus clock (SYSCLK), and the processor clock (CPUCLK).

4.1 POWER UP RESET

The system reset signal, RSTIN, is generated externally at power up and is used to reset the entire system. When asserted, the System Controller outputs the CPURES signal to reset the Main Processor and also resets the AT bus by asserting DACKEN and MXCTL2-0 = 100, which is decoded externally as DACK4. DACK4 is used to drive the bus reset signal. An external RC circuit can be used to extend the time that RSTIN is asserted until the power supply reaches a proper level. CPURES and the AT bus reset signals are de-asserted 84 clock pulses after RSTIN reaches its switching threshold. It is during the reset period that the type of processor is detected by examining the state of the S1 signal. If S1 is asserted, the WD76C10 or WD76C10LP enter the 80386SX mode. If S1 is de-asserted, it enters the 80286 mode. The WD75C10 only operates with an 80286. If an 80386SX has been detected, BUSYCPU is asserted so that the processor may perform its self-test operation immediately following the power up reset.

4.2 CLOCKING

The System Controller makes use of five clocks, CLK14, BCLK2, CPUCLK, CKA, and SYSCLK. Figure 4-1 shows how the clocks interact with each other and the register used to select the clock and speed.

4.2.1 Internal Clock (CLK14)

CLK14 is an input signal from a 14.3 MHz oscillator and is used for the control of the 8254 compatible timers. CLK14 is switched by the WD76C20 to 32 KHz during save and resume operations.

4.2.2 System Bus Clock (SYSCLK)

The AT bus is driven by the SYSCLK, which is derived from either the BCLK2 or CPUCLK, as selected by the Bus Timing Register at Port Address 1872. SYSCLK will always be one half or one fourth the value of the selected input clock (refer to Figure 4-1).

4.2.3 Processor Clock (CPUCLK)

The processor clock may be an output or input, depending on whether the System Controller generates CPUCLK or an external oscillator is used. At speeds of 40 MHz or higher, CPUCLK may need to be generated by an external oscillator, making it possible to control the processor duty cycle more closely. At lower speeds, the System Controller may use BCLK2 to generate CPUCLK or, in a system without discrete cache, the System Controller may use CKA to generate CPUCLK.

During reset, CPUCLK is an output.

If the CPUCLK is initially placed in the input mode, it may be changed to the output mode by writing to the PMC Control Register at Port Address 7872. The PMC control output 0 tri-states the external clock oscillator. A processor reset (CPURES) is automatically generated during the clock switching process.

When the CPUCLK is an output, it may be stopped by Port Address 1072 bits 1 or 0, or divided down by bits 14, 13 and 12. Only the WD76C10LP supports the CPUCLK stop function. When CPUCLK is stopped, it is in phase two of the 80C286. CPUCLK is restarted by an NMI or IRQ interrupt, qualified by the normal NMI and IRQ masking circuitry or by an NMI generated PMC logic.

There are two methods for slowing the processor execution rate to provide software compatibility with programs expecting a particular CPU speed, such as game software. One method is to divide the CPUCLK by a factor of 2, 4 or 8. Dividing the clock rate may also have an effect on the CPU power consumption, so bits 14, 13 and 12 also provide some choices of clock duty cycle. The other method is used when the CPUCLK is an input and generated by an external oscillator. In this case, bits 6, 5 and 4 are used to extend the hold request time to the processor after every refresh.

In a system without a cache or external memory controller, pin 51 can be defined as Clock A (CKA) and used in place of the BCLK2. This choice is established by the setting of bit 15 at Port Address 1072.

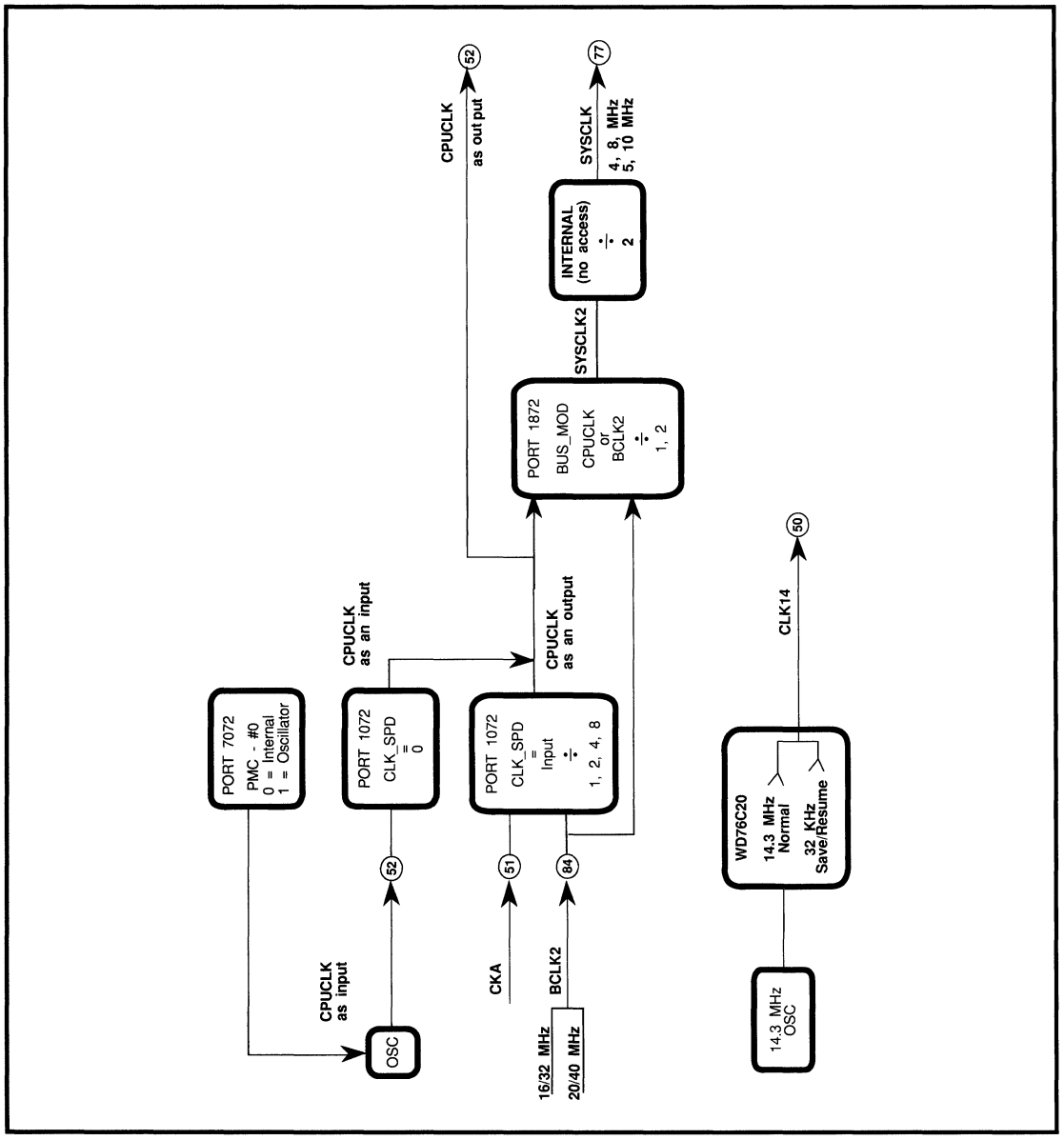


FIGURE 4-1. CLOCK CONTROL

16

4.2.4 CPU Clock (CPUCLK) Control Register

Port Address 1072 - Read and Write

15	14 13 12	11	10 09 08
SRC	CLK_SPD	AUT_ FST	ALT_CLK_SP

07	06 05 04	03	02	01	00
	EXT_HOLD			SCH	SCHH

Signal Name	Default At RSTIN
SRC	0/1
CLK_SPD	001
AUT_FST ☆	0
ALT_CLK_SPD ☆	000
EXTEND_HOLD	000
SCH ☆	0
SCHH ☆	0

☆ Featured only in the WD76C10LP

Bit 15 - SRC, CPUCLK clock source

When CPUCLK is selected as an output by bits 14 - 12, SRC determines whether it is to be driven by BCLK2 or CKA.

SRC is set to 1 and CKA is used as the CPUCLK clock source if CKA changes state within 64 clocks after $\overline{\text{RSTIN}}$ is de-asserted.

SRC is set to 0 and BLCK2 is used as the CPUCLK clock source if CKA does not change state during this period.

SRC = 0 -
BCK2 is the CPUCLK source.

SRC = 1 -
CKA is the CPUCLK source.

Bits 14-12 - CLK_SPD, CPUCLK clock speed

CLK_SPD determines whether CPUCLK is to be an input or output. When selecting CPUCLK as an output, CLK_SPD also determines the divisor and duty cycle values. The CLK_SPD defaults to 001 at power up. Changing the CPUCLK from an input (000) to an output automatically asserts the processor reset (CPURES) and the CPUCLK Driver Enable from the PMC latch is forced low, tristating the external clock oscillator. One µs later, CPUCLK becomes active as an output. One µs and 16 CPUCLK clocks (or one ms) later, the CPURES is de-asserted. This method allows switching the clock source while tolerating glitches in the CPUCLK, generated because the clock driver cannot synchronously switch the clock. The one µs and 16 clocks or one ms. selection is made through the Diagnostic Register at Port 9872.

CLK_SPD
14 13 12

- 0 0 0 - CPUCLK pin is an input, speed determined by external driving source.
- 0 0 1 - CPUCLK pin is an output, source divided by 1 (Default value).
- 0 1 0 - OUT, source divided by 2.
- 0 1 1 - OUT, source divided by 4, 25% duty cycle.
- 1 0 0 - OUT, source divided by 4, 75% duty cycle.
- 1 0 1 - OUT, source divided by 8, 12% duty cycle.
- 1 1 0 - OUT, source divided by 8, 88% duty cycle.

Bit 11 - AUT_FST, Auto clock speed
Featured only in the WD76C10LP

When automatic CPUCLK switching is enabled, the processor clock is switched between high and low clock speeds, depending upon activity. If the external $\overline{\text{TURBO}}$ signal is de-asserted when auto-speed is enabled, the CPUCLK is normally at the alternate clock or slower rate. When speedup activity occurs, the clock speed switches to the nominal clock rate, normally the higher, for a period of time determined by Table 4-1. When no further activity occurs, the clock speed switches back down to the alternate speed. If the external $\overline{\text{TURBO}}$ signal is asserted, the clock rate is set to the nominal clock rate specified by the CLK_SPD field.

A halt state also causes the clock rate to slow, unless the SCH or SCHH field is programmed to stop the clock. The clock

restarts or returns to the faster rate when any interrupt occurs.

Table 4-1 shows the activity that triggers a higher clock rate.

AUT_FST = 0 -
No Automatic Clock Switching

AUT_FST = 1 -
Automatic CPUCLK Switching. The EXT_HOLD field must be 000 when AUT_FST = 1

SPEEDUP ACTIVITY	TIME PERIOD
Hard disk interrupt, Hard disk or numeric processor I/O, SCSI, floppy, port B I/O	1 second
Keyboard interrupt	1 second or until next video access
Video access	1 millisecond
Any NMI or IRQ interrupt, except keyboard or hard disk	1 millisecond

TABLE 4-1. SPEEDUP ACTIVITY

Bits 10-08 - ALT_CLK_SPD, Alternate clock speed
Featured only in the WD76C10LP

ALT_CLK_SPD
10 09 08

0 0 0 - CPUCLK unchanged from CLK_SPD (Default value)

0 0 1 - Equals source

0 1 0 - Equals source div by 2

0 1 1 - Equals source div by 4, 25% duty cycle

1 0 0 - Equals source div by 4, 75% duty cycle

1 0 1 - Equals source div by 8, 12% duty cycle

1 1 0 - Equals source div by 8, 88% duty cycle

Bits 07-04 - EXT_HOLD, Extend processor hold

Processor execution may be slowed for software compatibility by extending the processor hold request after refresh cycles. If the external $\overline{\text{TURBO}}$ signal is asserted, EXT_HOLD is forced to 000. When the external $\overline{\text{TURBO}}$ signal is de-asserted, the EXT_HOLD returns to its programmed value, allowing an external TURBO switch to slow the processing speed.

EXT_HOLD
07 06 05 04

0 0 0 0 - No hold extension, (Default value)

0 0 0 1 - 1 µs hold after refresh

0 0 1 0 - 2 µs hold after refresh

0 0 1 1 - 3 µs hold after refresh

0 1 0 0 - 4 µs hold after refresh

↕

1 1 0 1 - 13 µs hold after refresh

1 1 1 0 - 14 µs hold after refresh

1 1 1 1 - 15 µs hold after refresh

Bits 03-02 - Reserved for future use, should be set to zero

Bit 01 - SCH, Stop CPUCLK at next Hold
Featured only in the WD76C10LP

SCH is applicable only for 80286 type processors in which the clock may be stopped. This option should only be used when the clock source is the WD76C10LP instead of an external oscillator.

Any unmasked processor interrupt or NMI restarts the CPUCLK and sets the SCH bit to zero. DRAM refresh continues while the processor clock is stopped. The refresh rate may be as programmed by the Refresh Timer at port address 041, or at the slower rate as selected by the Refresh Control Register at Port 2072.

SCH = 0 -
Normal processor clock (Default value)

SCH = 1 -
Stop processor clock at next processor hold cycle

16

Bit 00 - SCHH, Stop CPUCLK at next Halt and Hold. Featured only in the WD76C10LP

SCHH is applicable only for 80286 type processors in which the clock may be stopped. This option should only be used when the clock source is the WD76C10LP instead of an external oscillator.

Any unmasked processor interrupt or NMI restarts the CPUCLK. The SCHH bit remains set and the clock will be stopped again if a halt and hold condition is detected. The refresh rate may be as programmed by the Refresh Timer at port address 041, or at the slower rate selected by the Refresh Control Register at Port 2072.

SCHH = 0 -
Normal processor clock (default value)

SCHH = 1 -
Stop processor clock at next halt and hold cycle

5.0 AT BUS

This section describes the logic required to control the interrupts and timing between the AT bus and the System Controller.

5.1 INTERRUPT MULTIPLEXING

To reduce the number of pins required, the System Controller generates and outputs the MXCTL2-0 and DACKEN signals used by external logic to multiplex the DACKs, DRQs and IRQs down to single inputs. See Figure 5-1.

MXCTL2-0 are set to 100 during a System Reset ($\overline{RSTIN}$) to provide a Bus Reset (BUS_RST), and to determine the ROM width (ROM8), and processor clock (CPUCLK) pin direction. See Table 5-1.

5.1.1 Data Acknowledge DACK7-5, 3-0

An external '138 3 to 8 decoder uses MXCTL2-0 to generate the DACK7-5 and DACK3-0, which are applied to the AT bus. The unused combination develops the AT BUS_RST (bus reset). The decoder is enabled by the DACKEN signal from the System Controller.

5.1.2 Data Request DRQIN

The MXCTL2-0 signals are also used by an external 8 to 1 multiplexer to develop the DRQIN signal received by the System Controller. The MXCLT2-0 signals are held stable during DMA transfers.

Immediately following a System Reset ($\overline{RSTIN}$), DRQIN input 100 is sampled. If low, the processor clock (CPUCLK) pin is an output. If high, the CPUCLK starts as an output but is switched to an input shortly after $\overline{RSTIN}$ is de-asserted. See Table 5-1 and Figure 5-1.

5.1.3 Interrupt Requests

The Interrupt Requests are multiplexed by the WD76C30. The multiplexing is performed as shown in Table 5-1 and Figure 5-1, and provides the System Controller with the IRQSET1 and IRQSET0 signals.

DRQIN, IRQSET1 and IRQSET0 are sampled by the System Controller at every rising edge of SYSCLK2. This allows all DMA DRQ and IRQ lines to be sampled within 500 ns, when SYSCLK is 8 MHz.

The ROM8 input is sampled at the completion of a $\overline{RSTIN}$ to determine ROM data width (ROM8). The CPURES and A20GT inputs come from the 8042 keyboard controller.

5.1.4 AT Address Bus, Data Bus And Terminal Count (TC) Signal

The AT Address Bus SA19-00 and $\overline{BHE}$ are generated from A19-00 with external latches and tri-state buffers.

The AT Data Bus SD15-00 uses D15-00 and external bidirectional buffers.

The TC signal is generated by an external gate when DACKEN and $\overline{CSEN}$ are both asserted.

5.2 POWER MANAGEMENT CONTROL PMCIN

The power control signals are placed on the PMCIN input pin by way of an eight to one multiplexer, controlled by the MXCTL2-0 signals from the System Controller. In the WD75C10 and WD76C10, the TURBO signal may be connected directly to PMCIN. In the WD76C10LP, the external 8:1 MUX is always used. See Figure 5-1. Bits 14 and 13 of port 1872 (Section 5.3) control the power down of the processor and peripheral.

16

MXCTL 2 1 0	DRQIN	DACKEN	IRQSET0	IRQSET1	PMCIN
0 0 0	DRQ0	DACK0	$\overline{\text{IRQ8}}$	IRQ12	$\overline{\text{TURBO}}$
0 0 1	DRQ1	DACK1	IRQ9	IRQ1	PROC_PWR_GOOD
0 1 0	DRQ2	DACK2	IRQ10	A20GT	LCL_RQ or USER DEF.
0 1 1	DRQ3	DACK3	IRQ11	IRQ3	USER DEF.
1 0 0	CLOCK_ DIR_IN	BUS_RST	ROM8	IRQ4	USER DEF.
1 0 1	DRQ5	DACK5	CPURES	IRQ5	USER DEF.
1 1 0	DRQ6	DACK6	IRQ14	IRQ6	USER DEF.
1 1 1	DRQ7	DACK7	IRQ15	IRQ7	USER DEF.

TABLE 5-1. MXCTL2 - 0 DECODING

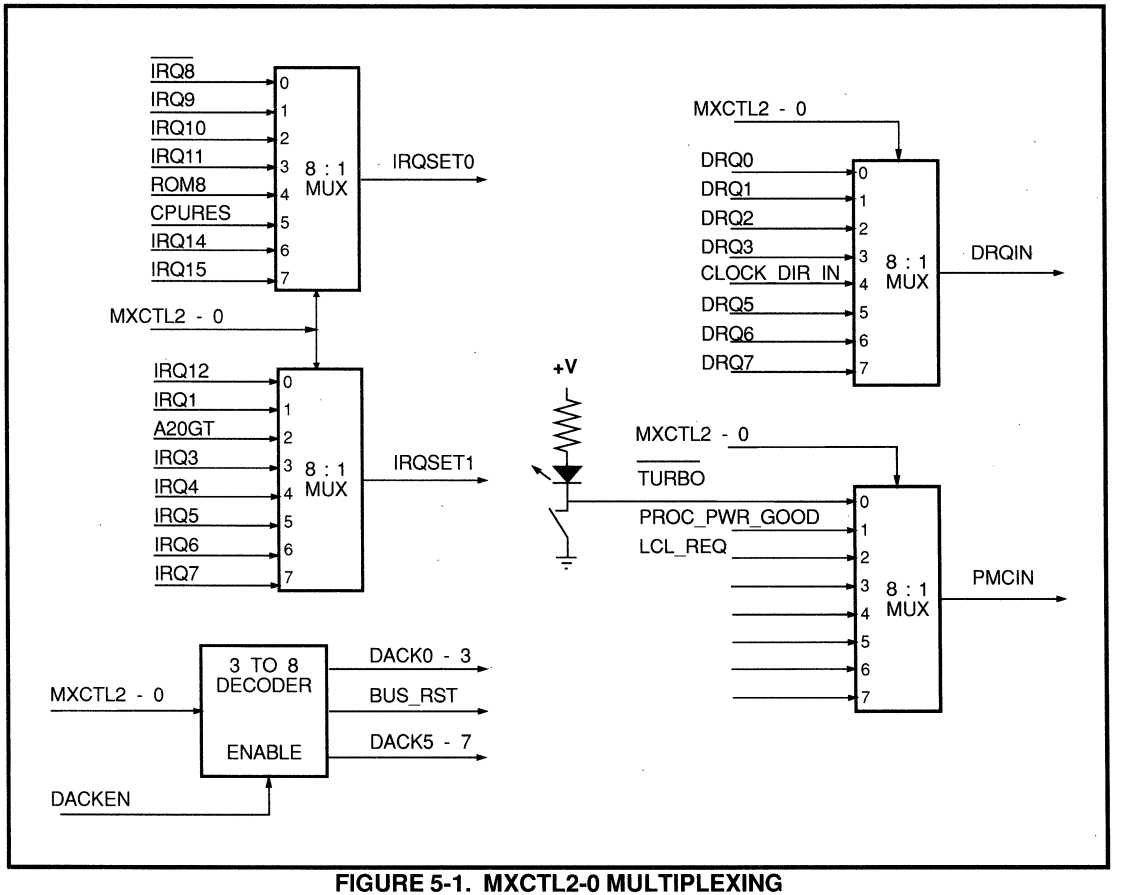


FIGURE 5-1. MXCTL2-0 MULTIPLEXING

5.3 NUMERIC PROCESSOR

5.3 .1 Numeric Processor Busy, Bus Timing, And Power Down Register

Port Address 1872 - Read and Write

15	14	13	12	11	10	09	08
NP_ BSY	PRO_ PD	FPD		BUS_MOD		BRQ_DEL	

07	06	05	04	03	02	01	00
BAK_DEL		WSI_ 16	WSM_ 16	WSI8		WSM8	

Signal Name	Default At RSTIN
NP_BSY	0
PRO_PD ☆	0
FPD ☆	0
BUS_MOD	0 0
BRQ_DEL	0 0
BAK_DEL	1 1
WSI_16	0
WSM_16	0
WS18	1 0
WSM8	1 0

☆ Featured only in the WD76C10LP

Bit 15 - NP_BSY, Numeric processor busy

For systems using an 80286 CPU, the 80287 numeric processor must have the NPBUSY signal generated earlier to meet the processor timing specifications when the processor runs faster than the bus. Bit 15 is ignored when an 80386SX is used.

NP_BSY = 0 -
Forces an early $\overline{\text{BUSYCPU}}$ when the co-processor address is F8 through FF and IOW (Default value)

NP_BSY = 1 -
Numeric processor busy

Bit 14 - PRO_PD, Processor power down
Featured only in the WD76C10LP

When PRO_PD has been changed from a zero to one, a power down sequence for the 80286 or 80386SX processor will be initiated and the expansion bus continues to operate normally. The processor should not be powered down if DMA cycles are likely to occur. When PRO_PD is set and a halt state occurs, the processor inputs are ignored and appear to the WD76C10LP to be in the passive state.

The input buffers connected to the processor signals do not consume power even if the processor signals do not reach ground. The internal pullups on inputs connecting to the processor are disabled to reduce power. PMC output 5 from port 7072 (Processor Power Down) is set. This can be used to control the power transistor and turn off the power to the processor. All outputs going to the processor will be tri-stated.

When an unmasked interrupt, DRQ or NMI occurs, PMC output 5 is reset, re-powering the processor. A voltage comparator should be used to generate a "Processor Power Good" signal. The PPG signal is sampled by bit 01 of the NMI Status Register at Port Address 9072. When PPG is high, the outputs to the processor are driven and the processor is reset.

PRO_PD = 0 -
Normal processor power
(Default value)

PRO_PD = 1 -
Start processor power down sequence

Bit 13 - FPD, Full power down
Featured only in the WD76C10LP

When FPD equals one and a halt state occurs, all processor and peripheral outputs except the PMC, DRAM controls and $\overline{\text{RA/ED}}$ bus are tri-stated and all inputs except $\overline{\text{RSTIN}}$, CLK14 and PMC inputs are ignored. CAS before RAS refresh will be performed if enabled by Port 2072. All circuitry except the PMC and refresh timer logic is stopped. PMC output 7 (Full Power Down) from port 7072 is set. This enables the powering down of all chips except DRAM, WD76C10LP, WD76C20, WD76C30 and WD90C00. The WD76C20 provides PDREF (a 64 KHz refresh signal on input pin 117) during the power down mode. This signal is then gated by the System Controller to the $\overline{\text{REFRESH}}$ signal as an output on pin 32.

When a PMC interrupt occurs, PMC output 7 at port 7072 is reset, enabling the power up sequence. A $\overline{\text{CPURES}}$ and $\overline{\text{RSTIN}}$ is asserted until the PMCIN 01 "processor power good"

16

at port 9072 input is high. The tri-stated outputs are restored and the inputs are no longer masked.

FPD remains a 1 until replaced by a 0.

FPD = 0 -
No power down (Default value).

FPD = 1 -
Full power down and in standby mode.

Bit 12 - Ignored by the System Controller, may be 0 or 1.

Bits 11, 10 - BUS_MOD, Bus mode

The System Controller defaults to mode 00 at power up. Therefore, the bus clock (SYSCLK) is controlled by BCLK2 and is asynchronous with CPUCLK (see Figure 4-1). This allows CPUCLK to be slower than SYSCLK and vary without affecting the bus timing. Normally, BCLK2 is either 16 MHz or 32 MHz. SYSCLK is divided by two, regardless of the mode selected by BUS_MOD, and if BCLK2 is 16 MHz at power up, it is divided by two again, providing a SYSCLK clock rate of 4 MHz until programmed to mode 01. In mode 01, the SYSCLK rate is 8 MHz for a BCLK2 of 16 MHz. Both mode 00 and 01 are asynchronous and require the appropriate synchronization delays to be established by BRQ_DEL and BAK_DEL of this register.

In modes 10 and 11, the SYSCLK is synchronous with the CPUCLK and synchronization delays are eliminated. The bus clock mode may need to be reprogrammed when the processor clock changes.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BUS_MOD
11 10

0 0 - Bus logic uses BCLK2 divided by 2 (Default value).

0 1 - Bus logic uses BCLK2 divided by 1.

1 0 - Bus logic uses CPUCLK divided by 2.

1 1 - Bus logic uses CPUCLK divided by 1.

Bits 09, 08 - BRQ_DEL, Bus request delay

An asynchronous AT bus state machine requires a synchronization delay at the start of the bus cycle.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BRQ_DEL
09 08

0 0 - 1 Bus clock delay (Default value)

0 1 - .5 Bus clock delay

1 0 - No clock delay

1 1 - Reserved

Bits 07, 06 - BAK_DEL, Bus acknowledge delay

An asynchronous AT bus state machine requires a synchronization delay at the end of the bus cycle.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BAK_DEL
07 06

0 0 - No delay

0 1 - -.5 Bus clock delay

1 0 - -1 Bus clock delay

1 1 - +.5 Bus clock delay (Default value)

Bit 05 - WSI16, Wait state for 16 bit I/0

WSI16 = 0 -
1 Bus clock wait state (Default value)

WSI16 = 1 -
2 Bus clock wait state

Bit 04 - WSM16, Wait state for 16 bit memory

WSM16 = 0 -
1 Bus clock wait state (Default value)

WSM16 = 1 -
2 Bus clock wait state

Bits 03, 02 - WSI8, Wait state for 8 bit I/O

WSI8
03 02

0 0 - 2 Bus clock wait state

0 1 - 3 Bus clock wait state

1 0 - 4 Bus clock wait state (Default value)

1 1 - 5 Bus clock wait state

Bits 01, 00 - WSM8, Wait state for 8 bit memory

WSM8
01 00

0 0 - 2 Bus clock wait state

0 1 - 3 Bus clock wait state

1 0 - 4 Bus clock wait state (Default value)

1 1 - 5 Bus clock wait state

5.3.2 Numeric Processor Busy (NPBUSY) Reset

Port Address 0F0 - Write only

7	6	5	4	3	2	1	0

Writing any data to this port resets the 80287 busy signal (de-asserts NPBUSY).

5.3.3 Numeric Processor Reset (NPRST)

Port Address 0F1 - Write only

7	6	5	4	3	2	1	0

Writing any data to this port asserts NPRST and resets the 80287. The main processor is wait stated for 128 clocks when writing to this port.

CPU TYPE	CPU SPEED	AT BUS SPEED	AT BUS MODE	BUS MOD	BRQ DEL	BAK DEL
80286	25 MHz	8 MHz	ASYNC	0X	00	00
	20 MHz	10 MHz	SYNC	10	10	10
	16 MHz	8 MHz	S YNC	10	10	10
	12.5 MHz	8 MHz	ASYNC	0X	01	10
	10 MHz	10 MHz	SYNC	11	10	10
	8 MHz	8 MHz	SYNC	11	10	10
80386SX	25 MHz	8 MHz	ASYNC	0X	01	00
	20 MHz	10 MHz	SYNC	10	10	10
	20 MHz	8 MHz	ASYNC	0X	01	10
	16 MHz	8 MHz	SYNC	10	10	10
	12.5 MHz	8 MHz	ASYNC	0X	01	10

TABLE 5-2. BUS TIMING PARAMETERS

5.4 DMA CONTROL

The System Controller contains two 8237 equivalent DMA controllers. DMA controller #1 is in the I/O address space from 000 to 00F and is used for 8-bit transfers. DMA controller #2 is in the I/O space from 0C0 to 0DE and is used for 16-bit transfers. Channel 0 of DMA controller #2 is used to cascade DMA controller #1.

AT Bus DMA Channel	DMA Controller	Transfer Type
0	#1 Channel 0	8-bit
1	#1 Channel 1	8-bit
2	#1 Channel 2	8-bit
3	#1 Channel 3	8-bit
4	#2 Channel 0	Cascade DMA Cont. #1
5	#2 Channel 1	16-bit
6	#2 Channel 2	16-bit
7	#2 Channel 3	16-bit

TABLE 5-3. DMA TRANSFER TYPES

5.4.1 Transfer Modes

Each DMA channel may be programmed in Single Transfer Mode, Block Transfer Mode, Demand Transfer Mode or Cascade Mode.

Refer to Section 5.4.12 - Mode Register, bits 7 and 6 for programming.

5.4.1.1 Demand Mode - 00

In demand mode, a transfer continues to take place until DRQ is de-asserted or a TC is reached. If the DRQ is de-asserted, the bus will be released. If DRQ is re-asserted, the transfer will resume. The address and word count behave as in single mode.

5.4.1.2 Single Transfer Mode - 01

In single transfer mode the channel makes one transfer for each request. The word count is decremented and the address is incremented or decremented at the end of each transfer. When the word count goes from 0000 to FFFF, a terminal count (TC) is generated. To start a transfer, the DRQ should be asserted until a DACK is received. If the DRQ is asserted through the cycle, only one transfer will take place. The DRQ must be de-asserted and then re-asserted to start another transfer. The bus is released between transfers.

5.4.1.3 Block Transfer Mode - 10

A transfer is started in block mode by a DRQ and continues until a TC is reached. The DRQ should be held active until DACK is asserted. Block mode should be used with caution since refresh is locked out. The address and word count behave as in single mode.

5.4.1.4 Cascade Mode - 11

Cascade mode is used to cascade DMA controller #2 to DMA controller #1, and for bus master transfers. A channel in cascade mode gets the bus when a DRQ is asserted, but the word count and address are ignored. The channel holds the bus until DRQ is de-asserted. The $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ and $\overline{MEMW}$ signals must be generated by the bus master device. The addresses from the System Controller are tri-stated when the $\overline{MASTER}$ signal is asserted.

5.4.2 Transfer Types

There are three types of transfers: write, read and verify.

Refer to Section 5.4.12 - Mode Register, bits 3 and 2 for programming.

5.4.2.1 Verify - 00

A verify transfer is a pseudo transfer that does not generate $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ or $\overline{MEMW}$ signals.

5.4.2.2 Write - 01

A write transfers data from an I/O device to memory.

5.4.2.3 Read - 10

A read transfers data from memory to an I/O device.

5.4.3 Autoinitialize

A channel may be programmed to autoinitialize for any transfer type. In this mode, when a TC is reached, the channel is loaded with the original word count and address and is ready to start another transfer.

Refer to Section 5.4.12 - Mode Register, bit 4 for programming.

5.4.4 Priority

Each DMA controller has two types of priority, fixed and rotating. For fixed priority, channel 0 has the highest priority and channel 3 has the lowest. In rotating priority, the last channel to be serviced has the lowest priority. The DMA controller #2 has priority over the DMA controller #1.

5.4.5 Extended Write

In normal timing the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$ pulse is two clock cycles and the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ is one clock cycle. If extended write is selected, the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ will be the same as the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$.

5.4.6 Base and Current Address

Each channel has a 16-bit base and current address register. The current address register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current address register is incremented or decremented during a transfer.

Addresses are driven to the bus while $\overline{\text{REFRESH}}$ is asserted, indicating a refresh cycle. Only address bits A23-A16 (from the page register) and bits A10-A0 (from the refresh counter) are meaningful during refresh. The address counter is incremented on the rising edge of $\overline{\text{REFRESH}}$.

5.4.7 Base and Current Word Count

Each channel has a 16-bit base and current word count register. The current word count register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current word count is decremented during a transfer.

I/O Address	Read/Write	DMA Controller	Function
000	Read/Write	1	Channel 0 Address
001	Read/Write	1	Channel 0 Word Count
002	Read/Write	1	Channel 1 Address
003	Read/Write	1	Channel 1 Word Count
004	Read/Write	1	Channel 2 Address
005	Read/Write	1	Channel 2 Word Count
006	Read/Write	1	Channel 3 Address
007	Read/Write	1	Channel 3 Word Count
008	Read	1	Status
008	Write	1	Command Register
009	Write	1	Request Register
00A	Write	1	Single Mask
00B	Write	1	Mode Register
00C	Write	1	Clear Pointer
00D	Write	1	Master Clear
00E	Write	1	Clear Mask
00F	Write	1	Mask All
0C0	Read/Write	2	Channel 0 Address
0C2	Read/Write	2	Channel 0 Word Count
0C4	Read/Write	2	Channel 1 Address
0C6	Read/Write	2	Channel 1 Word Count
0C8	Read/Write	2	Channel 2 Address
0CA	Read/Write	2	Channel 2 Word Count
0CC	Read/Write	2	Channel 3 Address
0CE	Read/Write	2	Channel 3 Word Count
0D0	Read	2	Status
0D0	Write	2	Command Register
0D2	Write	2	Request Register
0D4	Write	2	Single Mask
0D6	Write	2	Mode Register
0D8	Write	2	Clear Pointer
0DA	Write	2	Master Clear
0DC	Write	2	Clear Mask
0DE	Write	2	Mask All
B872	Read	1, 2	DMA Mode Shadow

TABLE 5-4. DMA CONTROLLER/CHANNEL FUNCTION MAP

5.4.8 Command Register

Port Addresses 008, 0D0 - Write only

7	6	5	4	3	2	1	0
		EX_ WR	RO_ PRI	0	CO_ DIS		

The Command Register is reset by a reset or Master Clear Command.

Bits 7, 6 - Not used, state is ignored

Bit 5 - EX_WR, Extended Write

Bit 4 - RO_PRI, Rotating Priority

Bit 3 - Must be set to 0

Bit 2 - CO_DIS, Controller Disabled

Bits1, 0 - Not used, state is ignored

5.4.9 Status Register

Port Addresses 008, 0D0 - Read only

7	6	5	4	3	2	1	0
CH3_ DRQ	CH2_ DRQ	CH1_ DRQ	CH0_ DRQ	CH3_ TC	CH2_ TC	CH1_ TC	CH0 TC

Bits 3-0 are reset by a reset, a Master Clear Command, or when read by a Status Read Command.

Bit 7 - CH3_DRQ, Channel 3 DRQ active

Bit 6 - CH2_DRQ, Channel 2 DRQ active

Bit 5 - CH1_DRQ, Channel 1 DRQ active

Bit 4 - CH0_DRQ, Channel 0 DRQ active

Bit 3 - CH3_TC, Channel 3 has reached TC

Bit 2 - CH2_TC, Channel 2 has reached TC

Bit 1 - CH1_TC, Channel 1 has reached TC

Bit 0 - CH0_TC, Channel 0 has reached TC

5.4.10 Request Register

Port Addresses 009, 0D2 - Write only

Each channel may be started by a software request. These requests are not affected by the Mask Register. The Request Register is reset by a reset or a Master Clear command.

7	6	5	4	3	2	1	0
					CRQ	CH#	

Bits 7-3 - Not used, state is ignored

Bit 2 - CRQ, Channel Requested

Bits 1, 0 - CH#, Channel Number Requested

CH# 1 0

0 0 - Channel 0

0 1 - Channel 1

1 0 - Channel 2

1 1 - Channel 3

5.4.11 Mask Registers

Each channel has a mask bit associated with it. If it is set, the channel is disabled. The bits may be set or reset by software or set by a TC if the channel is not in autoinitialize mode. All the bits are set by a reset or a Master Clear function.

5.4.11.1 Single Mask Register

Port Addresses 00A, 0D4 - Write only

7	6	5	4	3	2	1	0
					SE_ MA	CH#	

Bits 7-3 - Not used, state is ignored

Bit 2 - SE_MA, Set Mask

SE_MA = 0 -
Clear Mask

SE_MA = 1 -
Set Mask

16

Bits 1, 0 - CH#, Channel Number Requested

CH# 1 0

0 0 - Channel 0

0 1 - Channel 1

1 0 - Channel 2

1 1 - Channel 3

5.4.11.2 Clear Mask Register

Port Addresses 00E, 0DC - Write only

7	6	5	4	3	2	1	0

Bits 7-0 - Not used, state is ignored.

5.4.11.3 Mask All Register

Port Addresses 00F, 0DE - Write only

7	6	5	4	3	2	1	0
				CH3_MA	CH2_MA	CH1_MA	CH0_MA

Bits 7-4 - Not used, state is ignored.

Bit 3 - CH3_MA, Channel 3 Mask

Bit 2 - CH2_MA, Channel 2 Mask

Bit 1 - CH1_MA, Channel 1 Mask

Bit 0 - CH0_MA, Channel 0 Mask

5.4.12 Mode Register

Port Addresses 00B, 0D6 - Write only

This register selects the mode and type of transfer for each channel. Refer to Sections 5.4.1 through 5.4.1.4 for a description of the Transfer Modes, Sections 5.4.2 through 5.4.2.3 for a description of the Transfer Types, and Section 5.4.3 for a description of Autoinitialize.

7	6	5	4	3	2	1	0
TRA_MOD		AD_DEC	AUTO	TRA_TYP		CHA# SEL	

Bits 7, 6 - TRA_MOD, Transfer mode

TRA_MOD

7 6

0 0 - Demand

0 1 - Single

1 0 - Block

1 1 - Cascade

Bit 5 - AD_DEC, Address Decrement

AD_DEC = 0
Address is incremented.

AD_DEC = 1
Address is decremented after each DMA cycle.

Bit 4 - AUTO, Autoinitialize

AUTO = 0
Autoinitialization is disabled

AUTO = 1
Autoinitialization is enabled

Bits 3, 2 - TRA_TYP, Transfer Type

TRA_TYP

3 2

0 0 - Verify

0 1 - Write

1 0 - Read

1 1 - Not used

Bits 1, 0 - CHA#_SEL, Channel Select

CHA#_SEL

1 0

0 0 - Channel 0

0 1 - Channel 1

1 0 - Channel 2

1 1 - Channel 3

5.4.13 Clear Pointer Register

Port Addresses 00C, 0D8 - Write only

Each DMA controller has a pointer flip flop that indicates which half of the word count or address is being accessed. Each time a word count or address is written or read, the pointer changes state. When the flip flop is reset, bits 7-0 are accessed," and when it is set, bits 15-8 are accessed. The pointer is reset by writing any data to the Clear Pointer Register. The data is ignored.

7	6	5	4	3	2	1	0

Bits 7-0 - Not used, state is ignored.

5.4.14 Master Clear Rgister

Port Addresses 00D, 0DA - Write only

Writing any data to the Master Clear Register will:

1. Clear the Command Register
2. Clear the Status Register
3. Clear the Request Register
4. Set the Mask Register
5. Clear the Pointer Flip Flop

All data is ignored.

7	6	5	4	3	2	1	0

Bits 7-0 - Not used, state is ignored.

5.4.15 DMA Mode Shadow Register

Port Address B872 - Read only

15	14	13	12	11	10	09	08
DMA1 MODE							

07	06	05	04	03	02	01	00
DMA2 MODE							

Signal Name	Default At RSTIN
DMA1 MODE	0
DMA 2 MODE	0

Bits 15-08 - DMA1 MODE

DMA 1 MODE contains a copy of the data written into the DMA1 Mode Register located at I/O address 00B (see Table 5-4).

Bits 07-00 - DMA 2 MODE

DMA 2 MODE contains a copy of the data written into the DMA2 Mode Register located at I/O address 0D6 (see Table 5-4).

16

5.5 SYSTEM CONTROLLER 8259 INTERRUPT CONTROLLERS

The System Controller contains two 8259 equivalent interrupt controllers. Interrupt controller #1 is in the I/O space of 020 to 021, and interrupt controller #2 is in the I/O space of 0A0 to 0A1. Interrupt 2 of interrupt controller #1 is used to cascade interrupt controller #2.

5.5.1 Interrupt Sequence

1. When an interrupt arrives from a peripheral device, the interrupt may be programmed to be level or edge sensitive. In the level mode, the interrupts occur as long as the interrupt is kept high. In the edge mode, it must go low and high for each interrupt. The interrupt sets the appropriate bit in the Interrupt Request Register (IRR).

System Interrupt	Interrupt Controller	Use
0	#1 Level 0	Timer
1	#1 Level 1	Keyboard
2	#1 Level 2	Cascade
3-7	#1 Level 3 - 7	AT Bus
8	#2 Level 0	R.T.C.
9-12	#2 Level 1-4	AT Bus
13	#2 Level 5	Co-Processor
14-15	#2 Level 6-7	AT Bus

TABLE 5-5. INTERRUPT SEQUENCE

2. If the interrupt has not been masked off, it is passed to the priority circuit. There are three types of priority.

   Fixed

   In fixed priority, interrupt 0 has the highest priority and interrupt 7 has the lowest.

   Automatic Rotation

   In automatic rotation, the last interrupt serviced has the lowest priority.

   Specific Rotation

   In this mode, the lowest priority interrupt can be set by software. The next interrupt will have the highest priority. For example if interrupt 4 is set to the lowest level, the priority will be 5, 6, 7, 0, 1, 2, 3 and 4.

3. The interrupt controller sends an IRQ to the CPU.

4. The CPU responds with an INTA cycle that freezes priority.

5. The CPU sends another INTA that causes the interrupt controller to send a vector to the CPU and set the appropriate bit in the Interrupt Service Register (ISR) and clear the corresponding bit in the IRR, if it is in the edge triggered mode. As long as the bit in the ISR is set, all interrupts at the same level or lower are inhibited unless programmed for special mask mode.

6. An EOI is issued to end the interrupt. This clears the appropriate bit in the Interrupt Service Register. For the slave adapter (interrupt controller #2), two EOI's must be issued. There are three types of EOI's.

   Specific

   An EOI is issued by software for a specific interrupt.

   Non-Specific

   A non-specific EOI is issued by software. The hardware generates an EOI for the highest level active interrupt.

   Automatic

   An automatic EOI is a non-specific EOI that is caused by the second INTA.

   The interrupt controllers may also be operated in a polled mode. In this mode, the CPU is set to disable the interrupt input. In this case, software must issue a poll command. This takes the place of an INTA, and the software can then read the interrupt level to determine the interrupt to be serviced.

   When cascading is used and the slave has issued an interrupt, other interrupts from the slave are locked out. If it is desired to preserve priority in the slave (i.e., allow higher interrupts

to occur when a lower interrupt is being serviced), Special Fully Nested Mode should be programmed in the master. After a non-specific EOI has been sent to the slave, the ISR should be checked to see whether any other interrupts are active. If there are no interrupts active, a non-specific EOI should be sent to the master.

5.5.2 Setup - Initialization Command Words (ICW)

The interrupt controllers are setup by writing a series of Initialization Command Words (ICW). The sequence is started by writing a one to bit 4 of ICW1. If ICW 4 is to be included in the sequence, a one must also be written to bit 0 of the ICW1.

5.5.2.1 ICW1 - Initialization Command Word 1

Port Addresses 020, 0A0 - Write only

Bit 4 of this register must be set to 1 or it will be interrpreted as OCW2 or OCW3.

7	6	5	4	3	2	1	0
			S_S	L_T		N C_M	ICW 4

Bit 7-5 - Not used, state is ignored

Bit 4 - S_S, Start Sequence

S_S Must be set to 1.

Interrupt Controller	Address	Function	Read/Write
1	020	ICW1	Write
1	021	ICW2	Write
1	021	ICW3	Write
1	021	ICW4	Write
1	021	OCW1	Write
1	020	OCW2	Write
1	020	OCW3	Write
1	020	IRR	Read
1	020	ISR	Read
1	021	Mask	Read
1	020, 021	Interrupt Level	Read
2	0A0	ICW1	Write
2	0A1	ICW2	Write
2	0A1	ICW3	Write
2	0A1	ICW4	Write
2	0A1	OCW1	Write
2	0A0	OCW2	Write
2	0A0	OCW3	Write
2	0A0	IRR	Read
2	0A0	ISR	Read
2	0A1	Mask	Read
2	0A0, 0A1	Interrupt Level	Read

TABLE 5-6. INTERRUPT CONTROLLER FUNCTION MAP

Bit 3 - L_T, Level Trigger

The state of this bit is ignored. Edge triggered interrupts are always selected.

Bit 2 - Not Used, state is ignored

Bit 1 - N C_M, Not Cascade Mode

N C_M = 0 -
Cascade Mode selected

N C_M = 1 -
Single Mode selected

Bit 0 - ICW4, Initialization Control Word 4

ICW4 = 0 -
ICW4 not included in sequence

ICW4 = 1 -
ICW4 is included in sequence

5.5.2.2 ICW2 - Initialization Command Word 2

Port Addresses 021, 0A1 - Write only

7	6	5	4	3	2	1	0
Interrupt Vector							

Bits 7-3 - Interrupt Vector

Bits 2-0 - Not used, state is ignored

5.5.2.3 ICW3 - Initialization Command Word 3

Port Addresses 021 - Write only

This address accesses only Interrupt Controller 1.

7	6	5	4	3	2	1	0
0	0	0	0	0	I2 H_L	0	0

Bits 7-3 - Not used, must be set to 0

Bit **2 - I2 H_L**, Interrupt 2 has slave

I2 H_L = 0 -
Interrupt 2 does not have the Slave

I2 H_L = 1 -
Interrupt 2 has the Slave

Bits 1-0 - Not used, must be set to 0

Port Addresses 0A1 - Write only

This address accesses only Interrupt Controller 2.

7	6	5	4	3	2	1	0
0	0	0	0	0	Slave ID		

Bits 7-3 - Not used, must be set to 0

Bits 2-0 - Slave ID

5.5.2.4 ICW4 - Initialization Command Word 4

Port Addresses 021, 0A1 - Write only

7	6	5	4	3	2	1	0
0	0	0	S F N M	0	0	AUT EOI	1

Bits 7-5 - Not used, must be set to 0

Bit 4 - S F N M, Special Fully Nested Mode

S F N M = 0 -
Special Fully Nested Mode not selected

S F N M = 1 -
Special Fully Nested Mode selected

Bits 3-2 - Not used, must be set to 0

Bit 1 - AUT_EOI, Auto End Of Interrupt

AUT_EOI = 0 -
Normal EOI

AUT_EOI = 1 -
Automatic end of interrupt

Bit 0 - Not used, must be set to 1

5.5.3 Operation

Once the interrupt controllers are set up, they may be programmed by Operation Control Words One through Three (OCW1:3).

5.5.3.1 OCW1 - Operation Control Word 1

Port Address 021, 0A1 - Write only

7	6	5	4	3	2	1	0
INT 7_M	INT 6_M	INT 5_M	INT 4_M	INT 3_M	INT 2_M	INT 1_M	INT 0_M

Bit 7 - Interrupt 7 Mask

Bit 6 - Interrupt 6 Mask

Bit 5 - Interrupt 5 Mask

Bit 4 - Interrupt 4 Mask

Bit 3 - Interrupt 3 Mask

Bit 2 - Interrupt 2 Mask

Bit 1 - Interrupt 1 Mask

Bit 0 - Interrupt 0 Mask

16

5.5.3.2 OCW2 - Operation Control Word 2

Port Address 020, 0A0 - Write only

7	6	5	4	3	2	1	0
EOI_CONT			0	0	INT_LEV		

Bits 7-5 - EOI_CONT, End Of Interrupt

EOI_CONT 7	6	5	
0	0	0	- Clear Rotate On Automatic EOI
0	0	1	- Non-specific EOI
0	1	0	- Not used
0	1	1	- Specific EOI
1	0	0	- Select Rotate on Automatic EOI
1	0	1	- Rotate on Non-Specific EOI
1	1	0	- Set Priority
1	1	1	- Rotate on Specific EOI

Bits 4, 3 - Must be set to 0

Bits 2-0 - INT_LEV, Interrupt Level

INT_LEV 2	1	0	
0	0	0	- Interrupt Level 0
	↕		
1	1	1	- Interrupt Level 7

5.5.3.3 OCW3

Port Address 020, 0A0 - Write only

7	6	5	4	3	2	1	0
0	SMM		0	1	P_C	IRR_ ISR	

Bit 7 - Must be set to 0

Bits 6, 5 - SMM, Special Mask Mode

SMM 6	5	
0	0	Not used
0	1	Not used
1	0	Reset Special Mask Mode
1	1	Set Special Mask Mode

Bit 4 - Must be set to 0

Bit 3 - Must be set to 1

Bit 2 - P_C, Poll Command

P_C = 0 - No Poll Command

P_C = 1 - Poll Command

Bits 1-0 - IRR_ISR

IRR_ISR 1	0	
0	0	- Not used
0	1	- Not used
1	0	- Read Interrupt Request Register
1	1	- Read Interrupt Service Register

5.6 SYSTEM CONTROLLER 8254 TIMER

The System Controller contains an 8254 equivalent timer containing three independent counters. All the timers run off of a 1.19 MHz clock derived from the 14.318 MHz clock input. The GATE0 and GATE1 signals are tied high. The GATE2 signal is tied to register 61, bit 0. The counters decrement when counting. The largest possible count is 0.

Each counter may be programmed for different counting modes and the count may be read back. To initialize a counter, the Control Word must be written followed by one or two bytes of count if needed. Refer to Table 5-7 for the correct Control Word Format. Each counter may be programmed to count in BCD or binary.

I/O Address	Use	Read/Write
040	Timer 0 Count/Status	Read/Write
041	Timer 1 Count/Status	Read/Write
042	Timer 2 Count/Status	Read/Write
043	Control Word	Write

Timer Channel	Use
0	Time of Day (Interrupt)
1	Refresh Request
2	Speaker

CONTROL WORD (FORMAT 1) - I/O Address 043			
0	BCD		
1-3	Mode	000	Mode 0
		001	Mode 1
		X10	Mode 2
		X11	Mode 3
		100	Mode 4
		101	Mode 5
4-5	Function	00	Counter Latch Command
		01	Read/Write Low Byte
		10	Read/Write High Byte
		11	Read/Write Low Byte then High Byte
6-7	Counter	00	Counter 0
		01	Counter 1
		10	Counter 2
CONTROL WORD (FORMAT 2) - I/O Address 043			
0		0	
1		Select Counter 0	
2		Select Counter 1	
3		Select Counter 2	
4		Latch Status	
5		Latch Count	
6-7		11	

TABLE 5-7. CONTROL WORD FORMAT

16

5.6.1 Setup

Each counter may be set in one of five modes by writing a Control Word (format 1). The Control Word must specify the counter and the number of count bytes to be written. A new count may be written at any time.

5.6.1.1 Mode 0 Interrupt on Terminal Count

The counter starts when the count is loaded. When the count = 0 the counter continues counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting.

OUT goes low when the counter starts. It goes high when the count = 0, and stays high until a new count or mode is written.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.6.1.2 Mode 1 Hardware Retriggerable One Shot

The counter starts when GATE goes from low to high. When the count = 0, the counter continues counting from FFFF in binary mode or 9999 in BCD mode.

Any time GATE goes from low to high, the counter is reloaded with the original count and the counter started.

OUT goes low when GATE goes from low to high. It goes high when the count = 0. If a new count is written while the counter is counting, it will be loaded the next time GATE goes from low to high.

5.6.1.3 Mode 2 Rate Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter is started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

OUT is initially high. When the count = 1, OUT goes low for one clock.

If a new count is written while the counter is counting it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.1.4 Mode 3 Square Wave Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

When the counter starts, OUT is high. When the count is half done, OUT goes low. If GATE goes low, then OUT will go high.

If a new count is written while the counter is counting it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.1.5 Mode 4 Software Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. OUT is initially high. When the count = 0, OUT goes low for one clock.

If a new count is written while the counter is counting it will be loaded on the next clock pulse.

5.6.1.6 Mode 5 Hardware Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded. OUT is high when the counter starts. When count = 0, OUT goes low for one clock. If a new count is written while the counter is counting it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.2 Reading The Counter

There are three ways of reading the counters:

1. The count is read directly. This mode can cause false readings due to the fact that the counter may be changing while it is read.

2. The count may be read via a Counter Latch Command. (See Control Word format 1). This command latches the count so that it may be read without changing.

3. The count may be read via a Read Back Command. (See Control Word format 2). This command is the equivalent of multiple Counter Latch Commands.

5.6.3 Reading Status

The status of a counter may be read by issuing a Read Back Command with data bit 4 = 0. (See Control Word format 2). Bits 0-5 are the same as the command word for the counter. Bit 6 tells whether the last count that was written has been loaded into the counter. Bit 7 reflects the state of the OUT pin.

STATUS WORD	
0	BCD
1-3	Mode
4-5	Function
6	New Count Written
7	Out Status

5.6.4 Page

The page register is an 8-bit by 16-byte dual-ported RAM. It is used during refresh cycles and to generate address bits 16 to 23 for 8-bit DMA transfers and address bits 17 to 23 for 16-bit DMA transfers. One port of the RAM is a read-only port for DMA or refresh cycles and the other is a read/write port for the 80286 CPU.

5.6.5 Refresh Address

This block contains an 11-bit counter that is used for the address during a refresh.

5.7 SYSTEM CONTROLLER DECODE

Address 9	8	7	6	5	4	3	2	1	0	Decodes	Hex
0	0	0	0	0	X	X	X	X	X	DMA Controller 1 (Ch 0-3)	000-00F
0	0	0	0	1	X	X	X	X	X	Interrupt Controller Master	020-03F
0	0	0	1	0	X	X	X	X	X	Timer	040-05F
0	0	0	1	1	0	X	X	X	1	Port B (PI0)	061-06F (odd)
0	0	0	1	1	1	X	X	X	0	Real Time Clock (Address)	070-07E (even)
0	0	0	1	1	1	X	X	X	1	Real Time Clock (Data)	071-07F (odd)
0	0	1	0	0	X	X	X	X	X	Page Register (except 092)	080-09F
0	0	1	0	0	1	0	0	1	0	ALT 20 GATE, Hot Reset	092
0	0	1	0	1	X	X	X	X	X	Interrupt Controller Slave	0A0-0BF
0	0	1	1	0	X	X	X	X	X	DMA Controller 2 (Ch 4-7)	0C0-0DF

TABLE 5-8. DECODE ADDRESSES

5.7.1 Page Register Decodes

Address	Decode
0087	DMA Channel 0
0083	DMA Channel 1
0081	DMA Channel 2
0082	DMA Channel 3
008B	DMA Channel 5
0089	DMA Channel 6
008A	DMA Channel 7
008F	Refresh

TABLE 5-9. PAGE REGISTER DECODES

Note: Page register data appears on address bits A23-A16 during refresh and 8-bit DMA cycles. For 16-bit DMA cycles (channels 5-7), the LSB of the page register does not appear.

5.8 NMI AND REAL TIME CLOCK

5.8.1 Real Time Clock Address Register

Port Address 070-07E even - Write only

There is only one RTC Address Register. All even number addresses from 070 through 07E access this register.

7	6	5	4	3	2	1	0
D_ NMI	RTC A6	RTC A5	RTC A4	RTC A3	RTC A2	RTC A1	RTC A0

Signal Name	Default At RSTIN
D_NMI	1

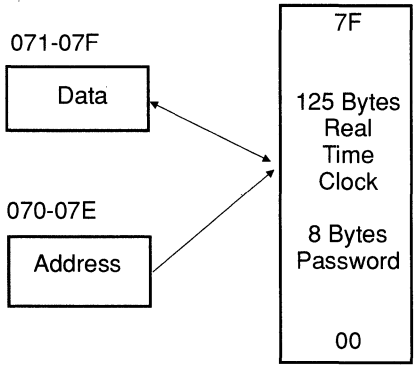
Bit 7 - D_NMI, Disable Non-Maskable Interrupt

D_NMI = 0 -
Non-Maskable Interrupt enabled

D_NMI = 1 -
Non-Maskable Interrupt disabled (Default value)

Bits 6-0 - RTCA6 through RTCA0, Real Time Clock Address

RTCA6 through RTCA0 provide the 128 addresses of the Real Time Clock area. The data selected by this address is available by reading the RTC Data Register at the odd numbered locations, 071-07F.



5.8.2 Real Time Clock Data Register

Port Address 071-07F odd - Read and Write

There is only one RTC Data Register. All odd number addresses from 071 through 07F access this register.

Data is transferred between this register and the memory location selected by the RTC Address Register. The data bus used is selected by bit 15 of the register at port address 2872 (refer to Section 7.2).

7	6	5	4	3	2	1	0
Real Time Clock Data							

5.8.3 Lock Pass, Alternate A20, And Hot Reset

Port Address 092 - Read and Write

7	6	5	4	3	2	1	0
				LOCK_ PASS		ALT_ A20G	HOT_ RST

Signal Name	Default At RSTIN
LOCK_PASS	0
ALT_A20G	0
HOT_RST	0

Bit 3 - LOCK_PASS

LOCK_PASS is used to prevent access to the eight byte password located in the Real Time Clock area. The protected addresses are 38H through 3FH. Before LOCK_PASS can be set, bit 02 of the register at port address 2872 must be set to 0. Once LOCK_PASS is set, it can only be reset by RSTIN.

LOCK_PASS = 0 -
The eight byte password area is accessible.

LOCK_PASS = 1 -
The eight byte password area is not accessible.

16

Bit 1 - ALT_A20G, Alternate A20 Gate

Normally, the state of ALT_A20G is ORed with the external A20GT signal. If either ALT_A20G or A20GT is high, the A20 line is ungated. If both ALT-A20G and A20GT are low, A20 will be gated low.

As an option, ALT_A20G may be programmed by the Diagnostic Register at Port Address 9872, to automatically change state to match that of the Keyboard's A20GATE. In this mode, the ALT_A20G signal is used exclusively, and the keyboard A20GATE signal is ignored.

Bit 0 - HOT_RST, Host reset

A processor reset (CPURES) is generated 128 CPUCLKs after the HOT_RST changes from a 0 to 1. The CPURES is 16 clock pulses wide.

5.9 PARITY ERROR AND I/O CHANNEL CHECK

Odd numbered port addresses 061 through 06F provide access to parity error and I/O channel check of the expansion bus.

Port Address 061- 06F odd
Bits 7-4 - Read only, Bits 3-0 - Read and Write

7	6	5	4	3	2	1	0
PE	IOCK	OUT 2	REF DT	D_ IOC	D_ PE	ENS PK	TMR 2G

Signal Name	Default At RSTIN
PE	0
IOCK	0
OUT2	NA
REFDT	1
D_IOC	0
D_PE	0
ENSPK	0
TMR2G	0

Bit 7 - PE, Parity error (read only)

PE = 0 -
No Parity Error

PE = 1 -
Parity Error

Bit 6 - IOCK, I/O channel check from the expansion bus (read only)

IOCK = 0 -
No I/O channel check error

IOCK = 1 -
I/O channel check error

Bit 5 - OUT2, from timer channel 2 (read only)

OUT2 represents the state of the Timer 2 output.

Bit 4 - REFDT, changes state on each refresh (read only)

Bit 3 - D_IOC, Disable I/O channel check (read and write)

D_IOC = 0 -
I/O channel check from the expansion bus is not disabled.

D_IOC = 1 -
I/O channel check from the expansion bus is disabled.

Bit 2 - D_PE, Disable parity error check (read and write)

D_PE = 0 -
Parity error checking not disabled. This may be overridden by port address register 6072, bit 10 for systems without parity RAM.

D_PE = 1 -
Parity error checking disabled.

Bit 1 - ENSPK, Enable speaker

ENSPK = 0 -
Speaker is not enabled

ENSPK = 1 -
Speaker is enabled

Bit 0 - TMR2G, Gate for timer channel 2

TMR2G = 0 -
Timer Channel 2 gated low

TMR2G = 1 -
Timer Channel 2 output enabled

6.0 MEMORY AND EMS CONTROL

This section describes the DRAM address bus and the EMS memory configuration and control registers.

6.1 DRAM ADDRESS AND DATA BUS

The memory address bus is multi-functional. During DRAM cycles, the DRAM row and column addresses are present on RA10 through RA0. During I/O cycles, RA10, RA9 and RA8 become CS2, CS1 and CS0 and, along with CS3, are used to decode 16 possible Chip Selects. Also, during I/O cycles to devices such as the Keyboard Controller, RA7 through RA0 become the Data Bus bits ED7 through ED0.

The RAS and CAS lines are designed to drive the DRAM array directly without the use of external drivers. RA10 through RA0 are capable of driving 350 pF, the equivalent load of two banks of one bit wide RAM plus two banks of four bit wide RAM (48 DRAMs).

The W/$\overline{R}$ signal at pin 119 should be buffered before use. Write protection is accomplished by not asserting CAS to the local DRAM while $\overline{MEMW}$ at pin 37 is asserted.

The on-board DRAM may be disabled so that external cards such as EMS may provide memory. The DRAM may be disabled in three stages, from 128K to 640K, 256K to 640K, and 512K to 640K.

The WD76C10 and WD76C10LP provide support for DRAM banks to be independent, two-way, or four-way page interleaved. DRAM banks that are interleaved must be of the same DRAM size. The WD75C10, WD76C10 and WD76C10LP support non-page mode two-way interleaved memory.

16

6.2 MEMORY CONFIGURATION

6.2.1 Memory Control

Port Address 3872 - Read and Write

15	14	13	12	11	10	09	08
PG_ CAS		CA		PG		ILV_	

07	06	05	04	03	02	01	00
SIZE BNK3		SIZE_ BNK2		SIZE_ BNK1		SIZE_ BNK0	

Signal Name	Default At RSTIN
PG_CAS ☆	0
CA☆	0 0
PG ☆	0
ILV	0 0
SIZE_BNK3 ☆ ☆	0 0
SIZE_BNK2 ☆ ☆	0 0
SIZE_BNK1 ☆ ☆	0 0
SIZE_BNK0 ☆ ☆	0 0

☆ Not featured in the WD75C10
☆ ☆ The WD75C10 does not support 4 Mb DRAM

Bit 15 - PG_CAS, Page mode CAS width
Not featured in the WD75C10

PG_CAS = 0 - Read CAS pulse width is 2.5 CPUCLK clocks (Default value).

PG_CAS = 1 - Read CAS pulse width is 2 CPUCLK clocks.

Bit 14 - Reserved for future use, should be set to 0.

Bits 13, 12 - CA, Cache mode
Not featured in the WD75C10

Enabling the Cache Mode adds an additional wait state to the beginning of on-board read cycles. On-board read cycles occur only for cache misses. If the RDYIN signal indicates that the external cache has experienced a zero wait state read hit, the DRAM read cycle is aborted.

Pin 51 of the System Controller serves one of three functions, depending upon the mode selected by CA. Pin 51 may represent the RDYIN (Ready In), CKA (Alternate Clock) or PE (Parity Error).

When CA is changed, a hold acknowledge cycle is required before the change goes into effect.

CA 13 12

0 0 - Cache Mode not enabled. Pin 51 may be used as the alternate clock CKA. (Default value)

0 1 - Cache Mode enabled. RDYIN at pin 51 indicates discrete cache hit or miss.

1 0 - External Memory Controller. Pin 51 becomes PE and is connected to the parity error line of the Discrete Cache controller.

Bit 11 - PG, Page mode
Not featured in the WD75C10

PG = 0 - Non-page mode (Default value)
Word interleaving is employed when bank interleaving is enabled by ILV.

PG = 1 - Page mode
Page mode interleaving is employed when bank interleaving is enabled by ILV.

Bits 10-08 - ILV, Interleave

In non-page mode (PG = 0), word interleaving is used. In Page Mode (PG = 1), page mode interleaving is used. Four way interleave is only supported in Page Mode and therefore, is not available to the WD75C10. Interleave of 64K DRAM is not supported by any of the System Controllers.

DRAM banks must be of the same size when they are interleaved together.

ILV 10 09 08

0 0 0 - No interleaving performed.
0 0 1 - Banks 0 and 1 are interleaved. Banks 2 and 3 are not interleaved. Banks 0 and 1 must be the same size.
0 1 0 - Banks 0 and 1 are not interleaved. Banks 2 and 3 are interleaved.
0 1 1 - Banks 0 and 1 are interleaved. Banks 2 and 3 are interleaved. Each pair must be the same size. Banks 0 and 1 may be a different size from Banks 2 and 3.
1 0 0 - Page Mode four way interleave.

Bits 07, 06 - SIZE_BNK3, Size of bank 3

The WD75C10 does not support 4 Mbit DRAM. The WD76C10 and WD76C10LP support all DRAM sizes. The DRAM sizes may be mixed.

SIZE_BNK3
07 06

0 0 - 64 Kbit X 16 (Default value)
0 1 - 256 Kbit X 16
1 0 - 1 Mbit X 16
1 1 - 4 Mbit X 16

Bits 05, 04 - SIZE_BNK2, Size of bank 2

The WD75C10 does not support 4 Mbit DRAM. The WD76C10 and WD76C10LP support all DRAM sizes. The DRAM sizes may be mixed.

SIZE_BNK2
05 04

0 0 - 64 Kbit X 16 (Default value)
0 1 - 256 Kbit X 16
1 0 - 1 Mbit X 16
1 1 - 4 Mbit X 16

Bits 03, 02 - SIZE_BNK1, Size of bank 1

The WD75C10 does not support 4 Mbit DRAM. The WD76C10 and WD76C10LP support all DRAM sizes. The DRAM sizes may be mixed.

SIZE_BNK1
03 02

0 0 - 64 Kbit X 16 (Default value)
0 1 - 256 Kbit X 16
1 0 - 1 Mbit X 16
1 1 - 4 Mbit X 16

Bits 01, 00 - SIZE_BNK0, Size of bank 0

The WD75C10 does not support 4 Mbit DRAM. The WD76C10 and WD76C10LP support all DRAM sizes. The DRAM sizes may be mixed.

SIZE_BNK0
01 00

0 0 - 64 Kbit X 16 (Default value)
0 1 - 256 Kbit X 16
1 0 - 1 Mbit X 16
1 1 - 4 Mbit X 16

6.2.2 Memory Bank 3 Through Bank 0 Starting Address

Port Address 4872 - Read and Write

15	14	13	12	11	10	09	08
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 1 start address					

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 0 start address					

Port Address 5072 - Read and Write

15	14	13	12	11	10	09	08
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 3 start address					

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17
		Bank 2 start address					

The starting address of the bank must be programmed on boundaries corresponding to the bank size. Smaller banks must be placed at a higher starting address than larger banks. The size of the bank is automatically set by the type and size of the RAM. When banks are interleaved, in either page or non-page mode, the interleaved banks should be enabled and programmed to the same starting address.

The bank size is doubled for two-way interleave and quadrupled for four-way interleave. For example, if bank 0 has 256 Kbit DRAMs and banks 2 and 3 have 1 Mbit DRAMs, the starting address for banks 2 and 3 should be zero. Both banks should be enabled. The size of the combined banks is 4 Mbytes, double the size of the individual banks. The starting address for bank 0 should then be at 4 Mbytes.

RAM SIZE	PAGE SIZE	BANK SIZE
64 Kbits X 1	512 Bytes	128 KBytes
256 Kbits X 1	1024 Bytes	512 KBytes
1 Mbits X 1	2048 Bytes	2048 KBytes
4 Mbits X 1	4096 Bytes	8192 KBytes

6.2.3 Split Starting Address

Port Address 5872 - Read and Write

15	14	13	12	11	10	09	08
EN_ BK3	EN_ BK2	EN_ BK1	EN_ BK0	DRAM_ DRV		SPLIT SIZE	

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19		

Signal Name	Default At RSTIN
EN_BK3	0
EN_BK2	0
EN_BK1	0
EN_BK0	0
DRAM_DRV	0 0
SPLIT_SIZE	0 0

Bit 15 - EN_BK3, Enable bank 3

EN_BK3 = 0 -
Bank 3 is disabled (Default value).

EN_BK3 = 1 -
Bank 3 is enabled.

Bit 14 - EN_BK2, Enable bank 2

EN_BK2 = 0 -
Bank 2 is disabled (Default value).

EN_BK2 = 1 -
Bank 2 is enabled.

Bit 13 - EN_BK1, Enable bank 1

EN_BK1 = 0 -
Bank 1 is disabled (Default value).

EN_BK1 = 1 -
Bank 1 is enabled.

Bit 12 - EN_BK0, Enable bank 0

EN_BK0 = 0 -
Bank 0 is disabled (Default value).

EN_BK0 = 1 -
Bank 0 is enabled.

Bits 11, 10 - DRAM_DRV, DRAM driver strength

The DRAM address driver strength may be adjusted for capacitive load. When adjusted properly, output overshoot and undershoot is minimized while still meeting worst case DRAM timing. The DRAM RAS, CAS and address buffers also automatically compensate for variations in temperature, voltage, and manufacturing process.

DRAM_DRV
11 10

0 0 - Full strength DRAM address drive, up to 350 pF. (Default value)

0 1 - Low strength DRAM address drive, up to 100 pF.

1 0 - Medium strength DRAM address drive, up to 180 pF.

1 1 - High strength DRAM address drive, up to 260 pF.

Bits 09, 08 - SP_SIZE, Split size

The split is implemented by moving the block of memory between 0A0000 through 0FFFFF to another area. The destination area must start on a 512K boundary. If BIOS is to be shadowed, the split size must be 320K for a 64K shadow or 256K for a 128K shadow, and the RAM Shadow And Write Protect Register (Port 6072) must also be programmed.

Figure 6-1 illustrates that the memory from 0A0000 hex (640K) to 100000 hex (1024K) is available for remapping. The remapping may start at 100000 hex, providing 384K of extended memory, or may start at 0F0000 hex to allow BIOS shadowing, with 320K of extended memory. Only a single bank may be split. The bank to be split must be at least 512K or larger.

SPLIT SIZE
09 08

0 0 - No split (Default value)
0 1 - 256K split, memory moved from 0A0000 to 0DFFFF
1 0 - 320K split, memory moved from 0A0000 to 0EFFFF
1 1 - 384K split, memory moved from 0A0000 to 0FFFFF

Bits 07-02 - A24-A19, Split starting address

Bits 01, 00 - Not used, state is ignored

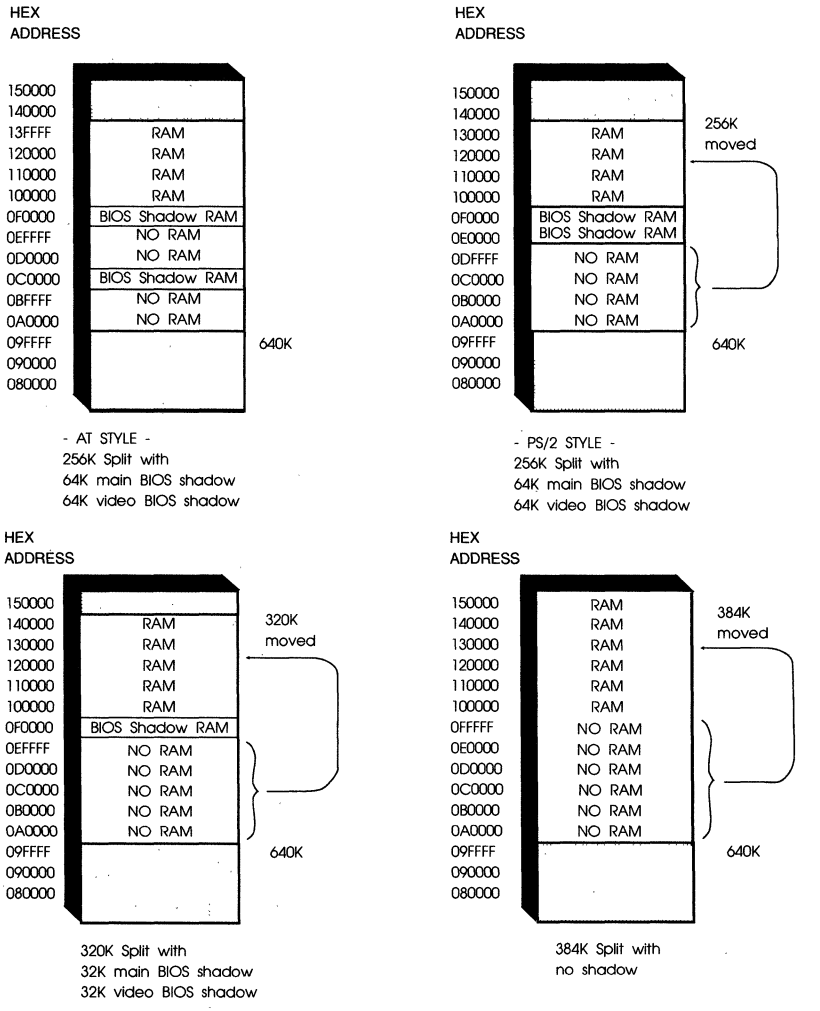


FIGURE 6-1. SPLIT SIZE

6.2.4 RAM Shadow And Write Protect

Port Address 6072 - Read and Write

15	14	13	12	11	10	09	08
DIS_MEM		HM_ WP	WP	INV_ PAR	PAR_ DIS	SHD	

07	06	05	04	03	02	01	00
0		VB_SIZ		ROM_ TYP		BL_MOU	

Signal Name	Default At RSTIN
DIS_MEM	0 0
HM_WP	0
WP	0
INV_PAR	0
PAR_DIS	0
SHD	0 0
Bit 7	0
VB_SIZ	0 0
ROM_TYP	0 0
BL_MOU	0 0

Bit 15, 14 - DIS_MEM, Disable on-board memory

DIS_MEM
15 14

0 0 - On-board memory from 128K to 640K not disabled (Default value)

0 1 - On-board memory from 512K to 640K disabled

1 0 - On-board memory from 256K to 640K disabled

1 1 - On-board memory from 128K to 640K disabled

Bit 13 - HM_WP, High memory write protect enable

This bit enables the write protection for the memory boundary established by the register at port C072.

HM_WP = 0 -
High memory write protect not enabled (Default value)

HM_WP = 1 -
High memory write protect enabled

Bit 12 - WP, Shadowed BIOS write protect enable

WP = 0 -
Write protect for shadowed BIOS not enabled (Default value)

WP = 1 -
Write protect for shadowed BIOS enabled

Bit 11 - INV_PAR, Invert parity

INV_PAR = 0 -
Normal parity when writing to on-board DRAM (Default value)

INV_PAR = 1 -
Invert parity when writing to on-board DRAM

Bit 10 - PAR_DIS, Parity checking disabled

Parity checking is normally enabled or disabled by port 061. Setting PAR_DIS overrides the port 061 setting and disables parity checking. This ability is provided for systems without parity RAM.

PAR_DIS = 0 -
Parity checking as selected by port 061 (Default value)

PAR_DIS = 1 -
Parity checking disabled

Bits 09, 08 - SHD, Shadow BIOS

ROM at FE0000 - FFFFFF, the top of 16 MB address space is never shadowed.

Option SHD 11 should be used when video and system BIOS combined equal more than 64K.

64K of system BIOS at 0F0000 - 0FFFFF, and up to 64K of video BIOS at 0C0000 - 0CFFFF, may be shadowed. This type of shadowing is accomplished by setting SHD = 10 and then writing the system and video BIOS into 0E0000 - 0FFFFF. When SHD is set to 11, the video BIOS appears at 0C0000 - 0CFFFF rather than 0E0000 - 0EFFFF.

The video shadow size at 0C0000 - 0CFFFF is determined by VB_SIZ, the video BIOS size field.

16

SHD
09 08

- 0 0 - No BIOS shadowing, allows 384K remap (Default value)
- 0 1 - 64K system BIOS shadow, 0F0000-0FFFFF, allows 320K remap
- 1 0 - 128K system BIOS shadow, 0E0000-0FFFFF, allows 256K remap
- 1 1 - 64K system BIOS shadow, 0F0000-0FFFFF and video BIOS shadow, allows 256K remap

Bits 07 - Reserved for future use, must be set to 0

Bit 06 - Not used, state is ignored

Bits 05, 04 - VB_SIZ, Video BIOS size

VB_SIZ
05 04

- 0 0 - 16K video BIOS (Default value)
- 0 1 - 32K video BIOS
- 1 0 - 48K video BIOS
- 1 1 - 64K video BIOS

Bits 03, 02 - ROM_TYP, ROM type

For ROM type 00, $\overline{\text{CSPROM}}$ is asserted when the address is 0E0000 - 0FFFFF or FE0000 - FFFFFF.

For ROM type 01, $\overline{\text{CSPROM}}$ is asserted when the address is 0F0000 - 0FFFFF or FF0000 - FFFFFF.

For ROM type 10, $\overline{\text{CSPROM}}$ is asserted when the address is 0F0000 - 0FFFFF, FF0000 - FFFFFF or 0C0000 - 0CXFFF where X is determined by VB_SIZ. This allows either a 128K BIOS, with a 64K system BIOS and a 64K video BIOS, or a 64K BIOS, with a 32K system BIOS and a 32K video BIOS. The 32K video BIOS portion must be in the bottom half of the EPROM and is accessed both at C0000 - CX000 and F0000 - FX000. A 64K EPROM needs addresses SA15 - SA0. A128K EPROM needs addresses SA16 - SA0. Neither EPROM needs translated addresses.

$\overline{\text{CSPROM}}$ is CS4 through CS0, decoded as the value of 00.

ROM_TYP
03 02

- 0 0 - 128K system BIOS, located at E0000 - FFFFF.
- 0 1 - 64K system BIOS, located at F0000 - FFFFF (Default value).
- 1 0 - 64K or 128K shared BIOS. System BIOS located at F0000 - FFFFF, video BIOS is located at C0000 - CX000.

Bits 01, 00 - BL_MOU, Back Light Mouse Control

Enabling the Back Light Mouse Control increases the CPU speed for one second if the Autofast is on. The AUT_FST bit is located at port 1072 bit 11.

BL_MOU
01 00

- 0 0 - No mouse control (Default value)
- 0 1 - INT12 mouse
- 1 0 - INT4 mouse
- 1 1 - INT3 mouse

6.2.5 High Memory Write Protect Boundary

Port Address C072 - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17

Signal Name	Default At RSTIN
A24 - A17	00

Bits 07-00 - A24-A17, Boundary address

Memory above the high memory write protect boundary is write protected when enabled by the HM_WP, bit 13 of the RAM Shadow And Write Protect Register at port 6072. This provides an additional write protect region for disk caching.

6.3 MEMORY TIMING

The DRAM timing is determined by an internal delay line for DMA and Master Mode transfers. The RAS leading edge becomes active from the active level of $\overline{MEMR}$ and $\overline{MEMW}$. The delay line is automatically tuned to fixed delays, using the 14.318 MHz clock CLK14 as reference.

When writing to the DRAM memory timing register at port 4072, the memory timing mode changes immediately, so the code that programs this register should be in ROM and not shadowed in RAM.

For non-page mode DRAM operations, the row address hold time is fixed at one CPUCLK.

6.3.1 Non-page Mode DRAM Memory Timing

Port Address 4072 - Read and Write

15	14	13	12	11	10	09	08
	NP_MODE		NP_ RAW	NP_WR_ DEL		NP_RD_ DEL	

07	06	05	04	03	02	01	00
	NP_RAS_ HLD		NP_CAS			NP_WS	

Signal Name	Default At RSTIN
NP_MODE	0 0
NP_RAW	0
NP_WR_DEL	0 0
NP_RD_DEL	0 0
NP_RAS_HLD	0 0
NP_CAS	0 0 0
NP_WS	0 0

Bit 15 - Not used, state is ignored

Bits 14, 13 - NP_MODE, Non-page RAS delay

The start of RAS is normally measured from the middle of $\overline{S0}$ or $\overline{S1}$. When operating in the 80386SX mode, the WD76C10 and WD76C10LP generate the $\overline{S0}$ and $\overline{S1}$ internally (the WD75C10 operates only with an 80286). The timing specifications in section 10 show the relationship of ADS to the internal $\overline{S0}$ and $\overline{S1}$ when in the 80386SX mode.

For 12.5 MHz 80286 operation, the RAS can be started from the status signals $\overline{S0}$ and $\overline{S1}$. This allows interleaved zero wait state operation from 120 ns. DRAM.

For 16 MHz 80386SX operation, the RAS can be started from the translated 80286 status signals. This allows interleaved zero wait state operation in pipeline mode from 100 ns. DRAM.

These two types of operation are selected by setting NP_MODE = 11.

For non-page mode operation with an 80286 at 16 MHz or 80386SX at 20 MHz, NP_MODE should be set to 00.

Discrete cache mode is not supported in non-page mode memory operation.

See Table 6-1 for more information regarding non-page mode operation.

RAS is delayed until the middle of the first command cycle when the non-page mode interleave is selected and back-to-back memory accesses are made to the same bank of DRAM.

This guarantees a RAS precharge time of three CPUCLK clocks.

NP_MODE
14 13

0 0 - RAS starts with 0 clock delay

1 1 - RAS starts from $\overline{S0}$ or $\overline{S1}$

Bit 12 - NP_RAW, Non-page disable RAW

NP_RAW = 0 -
Read after write cycles have additional wait states. See Table 6-2 for situations where wait states are added.

NP_RAW = 1 -
Read after write cycles do not have additional wait states.

Bits 11, 10 - NP_WR_DEL, Non-page write cycle delay

If RAS has been programmed by NP_RAS_DEL (bits 14, 13 = 11) to start from $\overline{S0}$ or $\overline{S1}$ active, the CAS delay is referenced to the middle of $\overline{S0}$ or $\overline{S1}$.

If the NP_WR_DEL is set to 01 or 10, the write CAS pulse width is shortened by .5 clock from the value programmed by the NP_CAS field (bits 4, 3 and 2).

NP_WR_DEL
11 10

0 0 - 1 CPUCLK (non-page)

0 1 - 1.5 CPUCLK (non-page)

1 0 - 2.0 CPUCLK (non-page)

1 1 - 2.5 CPUCLK (non-page)

Bits 09, 08 - NP_RD_DEL, Non-page read cycle delay

If RAS has been programmed by NP_RAS_DEL (bits 14, 13 = 11) to start from $\overline{S0}$ or $\overline{S1}$ active, the CAS delay is referenced to the middle of $\overline{S0}$ or $\overline{S1}$.

If the NP_RD_DEL is set to 01 or 10, the read CAS pulse width is shortened by .5 clock from the value programmed by the NP_CAS field (bits 4, 3, and 2).

NP_RD_DEL
11 10

0 0 - 1 CPUCLK (non-page)
0 1 - 1.5 CPUCLK (non-page)
1 0 - 2.0 CPUCLK (non-page)
1 1 - 2.5 CPUCLK (non-page)

Bit 07 - Not used, state is ignored

Bits 06, 05 - NP_RAS_HLD, Non-page CAS to RAS hold time

The CAS to RAS hold time is reduced by half a clock if the RAS to CAS delay is 1.5 or 2.5 clocks.

For example:

If NP_RAS_HLD is set for RAS active until 1.5 clocks after CAS and NP_RD_DEL is set for a 2.0 CPUCLK, the CAS to RAS hold time is 1.0 CPUCLK.

If NP_RAS_HLD is set for RAS active until 1.5 clocks after CAS and NP_RD_DEL is set for 1.5 or 2.5 CPUCLKs, the CAS to RAS hold time is reduced to .5 CPUCLKs.

NP_RAS_HLD
06 05

0 0 - RAS active until 1.0 clock after CAS
0 1 - RAS active until 1.5 clock after CAS
1 0 - RAS active until 2.0 clock after CAS
1 1 - RAS active until 2.5 clock after CAS

Bits 04-02 - NP_CAS, Non-page CAS pulse width

NP_CAS
04 03 02

0 0 0 - 1 CPUCLK (non-page)
0 0 1 - 1.5 CPUCLK (non-page)
0 1 0 - 2.0 CPUCLK (non-page)
0 1 1 - 2.5 CPUCLK (non-page)
1 0 0 - 3.0 CPUCLK (non-page)
1 0 1 - 3.5 CPUCLK (non-page)
1 1 0 - 4.0 CPUCLK (non-page)
1 1 1 - 4.5 CPUCLK (non-page)

Bits 01, 00 - NP_WS, Non-page wait states

NP_WS establishes the minimum duration of a DRAM cycle. If a read after write miss EMS access or interleave miss cycle occurs, an additional wait state is generated.

The System Controller holds the DRAM data until latched by the processor. If CAS ends at the command cycle boundary, to prevent data bus contention, an additional wait state should be programmed by NP_WS. Contention on the data bus can occur on a write cycle immediately following a read cycle, when the processor drives the data bus before the DRAM can tri-state its outputs.

NP_WS
01 00

0 0 - 0 Wait states
0 1 - 1 Wait states
1 0 - 2 Wait states
1 1 - 3 Wait states

16

NON-PAGE MODE	PROCESSOR SPEED	MIN W.S.	RAS START	ADDITIONAL WAIT STATES RD	WR	
00	16-20 MHz 80286, 20-25 MHz 80386SX	0	Tsm	No add'l	No add'l	Non-EMS, not interleave wait, not read after write.
			Tsm+1	+1	NA	Read after write, Non-EMS.
			Tsm+2	+2	+1	EMS or Interleave wait.
			Tsm+4	+3	NA	Simultaneous read after write and interleave wait.
11	8-12 MHz 80286, 16 MHz 80386SX	0	By $\overline{S0}$ $\overline{S1}$	No add'l	No add'l	Non-EMS, not interleave wait, not read after write.
			Tsm+1	+1	NA	Read after write, Non-EMS.
			Tsm+2	+2	+1	EMS or Interleave wait.
			Tsm+4	+3	NA	Simultaneous read after write and interleave wait.

NOTE: NA = Not Applicable
Tsm = middle of status cycle, Tsm+1 = 1 CPUCLK after Tsm = end of status cycle
Tsm+2 = 2 CPUCLKs after Tsm, Tsm+4 = 4 CPUCLKs after Tsm.
Non-Page Mode column represents the NP_MODE setting in Non Page Mode Register at port 4072.

TABLE 6-1. NON-PAGE MODE WAIT STATES

6.3.2 Page Mode

Table 6-2. identifies the type of DRAM cycle and number of wait states for the 80286 and 80386SX processors.

	PAGE MODE DRAM CYCLE	WAIT STATES
80286	Write page hit	0
	Write page first access ☆	1
	Write page miss	2
	Read page hit	0
	Read after write page hit	1
	Read page first access ☆	2
	Read page miss	3
80286 With Discrete Cache	Write page hit	0
	Write page first access ☆	1
	Write page miss	3
	Read cache hit	0
	Read cache miss, page hit	1
	Read cache miss, page first access ☆	2
	Read cache miss, page miss	4
80386SX	Write page hit, pipeline mode	0
	Write page hit, non-pipeline mode	1
	Write page first access ☆	1
	Write page miss, pipeline mode	2
	Write page miss, non-pipeline mode	3
	Read page hit, pipeline mode	0
	Read page hit, non-pipeline mode	1
	Read after write page hit ☆	1
	Read page first access ☆	3
	Read page miss, pipeline mode	3
	Read page miss, non-pipeline mode	4
80386SX With Discrete Cache, Non-pipe	Write page hit	0
	Write page first access ☆	1
	Write page miss	3
	Read cache hit	0
	Read cache miss, page hit	1
	Read cache miss, page first access ☆	2
	Read cache miss, page miss	4

TABLE 6-2. PAGE MODE WAIT STATES

☆ Equal Bank sizes, non-EMS cycle

16

6.3.3 Memory Address Multiplexer

The memory address multiplexer generates the DRAM row and column address. The DRAM address multiplexer is designed so that the same type socket may be used for 64K, 256K, 1 Mb or 4 Mb SIMM memory modules.

	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
64K NON-INTERLEAVE											
ROW	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A9
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
64K 2-WAY INTERLEAVE OR 256K NON-INTERLEAVE											
ROW	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
64K 4-WAY, 256K 2-WAY INTERLEAVE OR 1 Mb NON-INTERLEAVE											
ROW	A22	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
256K 4-WAY, 1 Mb 2-WAY INTERLEAVE OR 4 Mb NON-INTERLEAVE											
ROW	A22	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
1 Mb 4-WAY OR 4 Mb 2-WAY INTERLEAVE											
ROW	A22	A20	A18	A16	A15	A14	A13	A23	A21	A19	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
4 Mb 4-WAY INTERLEAVE											
ROW	A22	A20	A18	A16	A15	A14	A24	A23	A21	A19	A17
COL	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
REFRESH ADDRESS											
ROW	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

TABLE 6-3. PAGE MODE DRAM ADDRESS MULTIPLEXER CONFIGURATION

	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	
ROW	ALL	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	ALL
COL	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A9	64 Kb
COL	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A17	256 Kb
COL	A22	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17	1 Mb
COL	A22	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17	4 Mb

TABLE 6-4. NON-PAGE NON-INTERLEAVE ADDRESS CONFIGURATION

	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	
ROW	ALL	A11	A9	A8	A7	A6	A5	A4	A3	A2	A13	ALL
COL	A22	A20	A18	A16	A15	A14	A17	A12	A11	A10	A9	64 Kb
COL	A22	A20	A18	A16	A15	A14	A19	A12	A11	A10	A17	256 Kb
COL	A22	A20	A18	A16	A15	A14	A21	A12	A11	A19	A17	1 Mb
COL	A22	A20	A18	A16	A15	A14	A12	A23	A21	A19	A17	4 Mb

TABLE 6-5. NON-PAGE 2-WAY INTERLEAVE ADDRESS CONFIGURATION

16

6.4 EMS

6.4.1 EMS Control And Lower EMS Boundary

Port Address 6872 - Read and Write

15	14	13	12	11	10	09	08
INC	PF_LOC			EMS_EN			

07	06	05	04	03	02	01	00
EN_RES	A23	A22	A21	A20	A19	A18	A17
	LOWER_EMS_BOUNDARY						

Signal Name	Default At RSTIN
INC	0
PF_LOC	0 0
EMS_EN	0 0
EN_RES	0
A23-A17	0

Bit 15 - INC, Increment EMS pointer

The INC bit controls whether the EMS Pointer at port E072 is to be incremented after each read or write of the EMS Page Register at port E872.

INC = 0 -
The EMS pointer does not increment (Default value).

INC = 1 -
EMS pointer increments after access to EMS Page Register.

Bits 14-13 - PF_LOC, Upper page frame location

PF_LOC determines the starting location of a block eight frames. See Table 6-6 for the upper page frame assignments.

PF_LOC
14 13

0 0 - Upper page frame starts at C4000 (Default value)

0 1 - Upper page frame starts at C8000

1 0 - Upper page frame starts at CC000

1 1 - Upper page frame starts at D0000

Bit 12 - Not used, state is ignored

Bits 11, 10 - EMS_EN, EMS enable

EMS_EN determines whether all EMS frames are to be enabled, only the upper page frames or no page frames. Tables 6-6 and 6-7 show the upper and lower page frame assignments.

EMS_EN
11 10

0 0 - Disable EMS (Default value)

0 1 - Enable EMS Register programming

1 0 - Enable upper page frame assignments

1 1 - Enable upper and lower page frame assignments

Bits 09, 08 - Not used, state is ignored

Bits 07 - EN_RES, Enable lower boundary

EN_RES determines whether A23 through A17 (bits 06 through 00 of this register) are to be used as the lower EMS boundary or ignored.

When the LOWER_EMS_BOUNDARY is enabled, the memory above the boundary is removed from the extended memory and reserved for EMS.

EN_RES = 0 -
Ignore LOWER_EMS_BOUNDARY (Default value)

EN_RES = 1 -
Enable LOWER_EMS_BOUNDARY

Bits 06-00 - A23-A17,
LOWER_EMS_BOUNDARY

The lower_EMS_boundary provides address bits A23 through A17 and determines the starting address.

This address must be set to 128K below the actual start address. For example, to start EMS at the 1 Meg boundary, this field should be set to 07H (000 0111) binary).

6.4.2 EMS Page Register Pointer

Port Address E072 - Bits 15-06 Read only,
Bits 05-00 Read and Write

15	14	13	12	11	10	09	08
0	0	0	0	0	0	0	0

07	06	05	04	03	02	01	00
0	0	POINTER					

Signal Name	Default At RSTIN
POINTER	0

The EMS Page Register Pointer is used as an indirect address register. It is loaded with the EMS Page Register Number, ranging from 00 to 39 decimal. If the INC bit is set in port 6872, the EMS Page Register Pointer is incremented after each read or write of the EMS Page Register at port E872. Tables 6-6 and 6-7 shows the EMS Page Register Pointer value and the page frame assignments.

EMS REG NUM	PF_LOC = 00	EMS REG NUM	PF_LOC = 01	EMS REG NUM	PF_LOC = 10	EMS REG NUM	PF_LOC = 11
32	E0000-E3FFF	33	E4000-E7FFF	34	E8000-EBFFF	35	EC000-EFFFF
39	DC000-DFFFF	32	E0000-E3FFF	33	E4000-E7FFF	34	E8000-EBFFF
38	D8000-DBFFF	39	DC000-DFFFF	32	E0000-E3FFF	33	E4000-E7FFF
37	D4000-D7FFF	38	D8000-DBFFF	39	DC000-DFFFF	32	E0000-E3FFF
36	D0000-D3FFF	37	D4000-D7FFF	38	D8000-DBFFF	39	DC000-DFFFF
35	CC000-CFFFF	36	D0000-D3FFF	37	D4000-D7FFF	38	D8000-DBFFF
34	C8000-CBFFF	35	CC000-CFFFF	36	D0000-D3FFF	37	D4000-D7FFF
33	C4000-C7FFF	34	C8000-CBFFF	35	CC000-CFFFF	36	D0000-D3FFF

EMS registers 32 through 39 can be individually enabled or disabled by the EN (bit 15) of the EMS Page Register. See port E872 description.

TABLE 6-6. UPPER PAGE FRAME ASSIGNMENTS

EMS REG NUM	HEX	DEC	EMS REG NUM	HEX	DEC
23	5C000-5FFFF	368K-384K	7	9C000-9FFFF	624K-640K
22	58000-5BFFF	352K-368K	6	98000-9BFFF	608K-624K
21	54000-57FFF	336K-352K	5	94000-97FFF	592K-608K
20	50000-53FFF	320K-336K	4	90000-93FFF	576K-592K
19	4C000-4FFFF	304K-320K	3	8C000-8FFFF	560K-576K
18	48000-4BFFF	288K-304K	2	88000-8BFFF	544K-560K
17	44000- 47FFF	272K-288K	1	84000-87FFF	528K-544K
16	40000-43FFF	256K-272K	0	80000-83FFF	512K-528K
15	3C000-3FFFF	240K-256K	31	7C000-7FFFF	496K-512K
14	38000-3BFFF	224K-240K	30	78000-7BFFF	480K-496K
13	34000-37FFF	208K-224K	29	74000-77FFF	464K-480K
12	30000-33FFF	192K-208K	28	70000-73FFF	448K-464K
11	2C000-2FFFF	176K-192K	27	6C000-6FFFF	4320-448K
10	28000-2BFFF	160K-176K	26	68000-6BFFF	416K-432K
9	24000-27FFF	144K-160K	25	64000-67FFF	400K-416K
8	20000-23FFF	128K-144K	24	60000-63FFF	384K-400K

EMS registers 0 through 31 are enabled or disabled as a block. If the EMS_EN field of port 6872 is 11, the EMS registers 0 through 31 are enabled and the EN (bit 15) of the EMS Page Register is treated as a one. See port E872 description.

TABLE 6-7. LOWER PAGE FRAME ASSIGNMENTS

6.4.3 EMS Page Register

Port Address E872 - Bits 14-12 Read only, Bits 15, 11-00 Read and Write

15	14	13	12	11	10	09	08
EN	0	0	0	P11	P10	P9	P8

07	06	05	04	03	02	01	00
P7	P6	P5	P4	P3	P2	P1	P0

Signal Name	Default At RSTIN
EN	0
P11-P00	0

There are 40 EMS Page Registers accessible through port E872. Only EMS registers 32 through 39 are initialized to zero, EMS registers 0 through 31 are not initialized. The EMS Page Register Pointer at port E072 provides the offset location for port E872.

Bit 15 - EN, Enable EMS Page Register

EMS Page Registers 32 through 39 can be individually enabled or disabled by the EN bit. EMS Page Registers 0 through 31 are enabled or disabled as a block by the setting of the EMS_EN field in the EMS Control Register at port 6872. When EMS_EN equals 11, the EN bit in this register is treated as a one.

EN = 0 -
This EMS Page Register is disabled

EN = 1 -
This EMS Page Register is enabled

Bits 14-12 - Read only, not used by the System Controller

Bits 11-00 - P11 through P00, EMS Page Number

EMS page numbers 8 through 39 and 64 through 2047 are supported for on-board memory, equal to 31.5 MB of EMS memory. The memory address is generated by reading the EMS page number from the System Controller and multiplying it by 16K, then adding the lower 14 bits of the processor address to the product. This results in EMS page numbers zero through seven being mapped to the lower 128K of memory, and On-board extended memory being able to be accessed in real mode via the EMS logic.

EMS page numbers 2048 through 2303, equal to 4 MB, are used for external EMS memory, providing a method of accessing plug-in RAM or ROM cards. If P11 is 1 when an external EMS access occurs, EMS page number bits P7 through P0 are output on RA0-7/ED0-7 and the EMS chip select is asserted. The RAM/ROM card should access data on the expansion data bus, using $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{MEMCS16}}$ and IOREADY to make the transfer.

7.0 PORT CHIP SELECT AND WD76C10 REFRESH CONTROL

This section describes refresh control logic peculiar to the WD76C10LP, and used by the power down feature. This section also describes the registers used to control the following functions:

- Port chip select and control
- High speed hard disk access
- AT hard disk IDE mode
- 8/16 bit 80287 bus timing
- Real Time Clock bus location
- Access to the CMOS RAM password

Table 7-1 identifies the ports, their Chip Select number, I/O address, and function.

7.1 REFRESH CONTROL, SERIAL AND PARALLEL CHIP SELECTS

Port Address 2072 - Read and Write

15	14	13	12	11	10	09	08
M_ REF	V_ REF	CBR_ REF	CBR_ SR	SCSI	PAR		PAR_ L

07	06	05	04	03	02	01	00
SER_A			SER_ AL	SER_B			SER_ BL

Signal Name	Default At RSTIN
M_REF ☆	0
V_REF ☆	0
CBR_REF ☆	0
CBR_SR	0
SCSI	0
PAR	0 0
PAR_L	0
SER_A	0 0 0
SER_AL	0
SER_B	0 0 0
SER_BL	0

☆ Featured only in the WD76C10LP

Bit 15 - M_REF, Memory refresh power down mode
Featured only in the WD76C10LP

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at port 1872, and M_REF = 1, the on-board DRAM is refreshed with every eighth PDREF. PDREF is a 64 KHz input signal supplied by the WD76C20.

M_REF = 0 -
Normal refresh period for main on-board memory (Default value)

M_REF = 1 -
Slow refresh main on-board memory

Bit 14 - V_REF, Video refresh power down mode
Featured only in the WD76C10LP

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at port 1872, and V_REF = 1, the on-board DRAM is refreshed with every eighth PDREF. PDREF is a 64 KHz input signal supplied by the WD76C20.

V_REF = 0 -
Normal refresh period for video memory (Default value)

V_REF = 1 -
Slow refresh video memory

Bit 13 - CBR_REF, CAS before RAS refresh for on-board DRAM
Featured only in the WD76C10LP

CBR_REF = 0 -
Normal refresh for on-board DRAM (Default value)

CBR_REF = 1 -
CAS before RAS refresh

Bit 12 - CBR_SR, CAS before RAS self refresh

CBR_SR = 0 -
No CAS before RAS self refresh (Default value)

CBR_SR = 1 -
CAS before RAS self refresh of DRAM is supported during suspend and resume, where CAS is held low continuously while in suspend.

Bit 11 - SCSI, Small Computer System Interface chip select

The SCSI is selected by chip select number 12. See Table 7-1.

SCSI = 0 -
SCSI chip select disabled (Default value)

SCSI = 1 -
SCSI chip select at I/O port 353X

Bits 10, 09 - PAR, parallel port chip select

The parallel port is selected by chip select number 0F and may be located at I/O address 278 through 27B, 378 through 37F, or 3BC through 3BF. Bits 10 and 09 may disable the chip select or locate it at one of three areas. See Table 7-1.

PAR
10 09

0 0 - PAR chip select disabled (Default value)

0 1 - PAR chip select at I/O port 3BC - 3BF

1 0 - PAR chip select at I/O port 378 - 37F

1 1 - PAR chip select at I/O port 278 - 27F

Bit 08 - PAR_L, parallel port bus location

PAR_L = 0 -
Parallel port is located on the RA0-7/ED0-7 bus.

PAR_L = 1 -
Parallel port is located on the expansion data bus.

Bits 07, 06, 05 - SER_A, serial port A chip select

The serial port A is selected by chip select number 0E and may be located at I/O address 2E8 through 2EF, 2F8 through 2FF, 3E8 through 3EF or 3F8 through 3FF. Bits 07, 06, and 05 may disable the chip select or locate it at one of the four areas. See Table 7-1.

It is possible to select the same I/O port address for serial port A and serial port B. Selecting the same address for both ports results in an unpredictable response and should not be done.

SER_A
07 06 05

0 0 0 - Serial port A chip select disabled (Default value)

0 0 1 - Serial port A chip select at I/O port 3F8 - 3FF

0 1 0 - Serial port A chip select at I/O port 2F8 - 2FF

0 1 1 - Serial port A chip select at I/O port 3E8 - 3EF

1 0 0 - Serial port A chip select at I/O port 2E8 - 2EF

Bit 04 - SER_AL, serial A port bus location

SER_AL = 0 -
Serial port A is located on the RA0-7/ED0-7 bus.

SER_AL = 1 -
Serial port A is located on the expansion data bus.

Bits 03, 02, 01 - SER_B serial port B chip select

The serial port B is selected by chip select number 10 and may be located at I/O address 2E8 through 2EF, 2F8 through 2FF, 3E8 through 3EF or 3F8 through 3FF. Bits 03, 02 and 01 may disable the chip select or locate it at one of the four areas. See Table 7-1.

It is possible to select the same I/O port address for serial port B and serial port A. Selecting the same address for both ports results in an unpredictable response and should not be done.

16

SER_B
03 02 01

0 0 0 - Serial port B chip select disabled (Default value)

0 0 1 - Serial port B chip select at I/O port 3F8 - 3FF

0 1 0 - Serial port B chip select at I/O port 2F8 - 2FF

0 1 1 - Serial port B chip select at I/O port 3E8 - 3EF

1 0 0 - Serial port B chip select at I/O port 2E8 - 2EF

Bit 00 - SER_BL, serial B port bus location

SER_BL = 0 -
Serial port B is located on the RA0-7/ED0-7 bus

SER_BL = 1 -
Serial port B is located on the expansion data bus

7.2 RTC, PVGA, 80287 TIMING, DISK CHIP SELECTS

Port Address 2872 - Read and Write

15	14	13	12	11	10	09	08
RTC_L	FST_VGA	FST_SCSI	EN_PCS	U_MSK	L_MSK		

07	06	05	04	03	02	01	00
PRG_L	HS_HD		P/S	HS_287	LK_PSW	DS_HD	DS FLP

Signal Name	Default At RSTIN
RTC_L ☆	0
FST_VGA ☆	0
FST_SCSI	0
EN_PCS ☆	0
U_MSK	0 0
LMSK	0 0
PRG_L	0
HS_HD	0 0 0
P/S	0 0 0
HS_287	0
LK_PSW	0
DS_HD	0
DS_FLP	0

☆ Featured only in the WD76C10 AND WD76C10LP

Bits 12 through 07 and port location 3072 control the use and location of the Programmable Chip Select.

Bit 15 - RTC_L, Real Time Clock

The Real Time Clock is normally on the RA0-7/ED0-7 bus but may be placed on the expansion data bus.

RTC_L = 0 -
Real Time Clock is on the RA0-7/ED0-7 bus (Default value).

RTC_L = 1 -
Real Time Clock is on the expansion data bus.

Bit 14 - FST_VGA, Fast VGA video

The performance of Paradise PVGA display controllers may be enhanced by terminating video access earlier than normal. This feature should only be used with Western Digital Imaging/Paradise PVGA1A and PVGA1B devices. I/O cycles to ports 3C0 - 3CF are made with one wait state cycles.

FST_VGA = 0 -
Normal PVGA control (Default value)

FST_VGA = 1 -
Early PVGA wait state generation

Bit 13 - FST_SCSI, Fast SCSI

The performance of the WD33C93 is enhanced by perfroming eight-bit accesses with one wait state rather than four wait states.

FST_SCSI = 0 -
Four Wait States (Default value)

FST_SCSI = 1 -
One Wait State

Bit 12 - EN_PCS, Enable programmable chip select

The programmable chip select logic is selected with chip select 11 and may be disabled or enabled. See Table 7-1.

EN_PCS = 0 -
Disable programmable chip select. (Default value)

EN_PCS = 1 -
Enable programmable chip select

Bit 11 - U_MSK, Upper address bits masked

U_MSK determines whether the upper address bits A15 through A10 are to be used as designated in the Programmable Chip Select Address Register at port 3072.

U_MSK = 0 -
A15 through A10 are ignored (Default value).

U_MSK = 1 -
A15 through A10 are included in the address.

Bits 10, 09, 08 - L_MSK, Lower address bits masked

L_MSK determines whether the lower four address bits A03 through A00 are to be used as designated in the Programmable Chip Select Address Register at port 3072.

L_MSK
10 09 08

0 0 0 - A09 through A00 are included in the address (Default value)

0 0 1 - A00 is ignored

0 1 0 - A00, A01 are ignored

0 1 1 - A00, A01, A02 are ignored

1 0 0 - A00, A01, A02, A03 are ignored

Bit 07 - PRG_L, Programmable chip select bus location

PRG_L = 0 -
Programmable chip select is on the RA0-7/ED0-7 bus (Default value).

PRG_L = 1 -
Programmable chip select is on the expansion bus.

Bit 06 - HS_HD, High speed hard disk data transfer rate

Enabling the high speed data transfers results in hard disk, 16-bit data transfers to be performed at a compressed timing rate rather than at the compatible bus rate. When operating in the high speed mode, the first data transfer is made at the compatible bus rate. Subsequent accesses to the hard disk port are made at high speed, with BALE (pin 79) suppressed, and the expansion bus addresses remain fixed at the hard disk data I/O port address.

HS_HD = 0 -
Compatible bus timing enabled (Default value)

HS_HD = 1 -
High speed hard disk accesses enabled

Bit 05 - Not used, the state is ignored

Bit 04 - P/S, Primary or secondary disk

The P/S bit is only used to select the floppy disk chip select address in the IDE mode. See Table 7-1, chip select numbers 08 through 0B.

P/S = 0 -
Primary hard disk and Floppy address selected (Default value)

P/S = 1 -
Secondary hard disk and Floppy address selected

Bit 03 - HS_287, Co-processor 80287 high speed timing

Normal I/O read and write access to the 80287 is made with eight bit bus timing. Setting HS_286 results in 16 bit bus timing.

HS_287 = 0 -
Normal 80287 timing (Default value)

HS_287 = 1 -
Fast 80287 timing

Bit 02 - LK_PSW, Prevent locking password

Port 092 bit 3 (Lock_Pass) is used to prevent access to the CMOS RAM password area located at 38H through 3FH. Setting LK_PSW before attempting to set Lock_Pass, inhibits the setting of Lock_Pass. In this instance, it is possible to access the CMOS RAM password area. If Lock_Pass is set before LK_PSW, LK_PSW will have no effect.

LK_PSW = 0 -
Port 092 bit 3, Lock_Pass can be set (Default value)

LK_PSW = 1 -
Port 092 bit 3, Lock_Pass can not be set

Bit 01 - DS_HD, Hard disk chip select 0C, 0D

DS_HD = 0 -
Hard disk chip select is enabled (Default value).

DS_HD = 1 -
Hard disk chip select is not generated.

Bit 00 - DS_FLP, Floppy disk chip select 08, 09, 0A, 0B

DS_FLP = 0 -
Floppy disk chip select is enabled (Default value).

DS_FLP = 1 -
Floppy disk chip select is not generated.

7.3 PROGRAMMABLE CHIP SELECT ADDRESS

Port Address 3072 - Read and Write

15	14	13	12	11	10	09	08
A15	A14	A13	A12	A11	A10	A09	A08

07	06	05	04	03	02	01	00
A07	A06	A05	A04	A03	A02	A01	A00

7.4 CACHE FLUSH

Port Address F872 - Write only

15	14	13	12	11	10	09	08
X	X	X	X	X	X	X	X

07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X

7.5 I/O PORT ADDRESSES AND CHIP SELECT ASSIGNMENTS

Table 7-1 lists the I/O addresses and chip selects generated for each fixed port type. Address bits A15 through A10 are ignored for the I/O addresses listed with three digits. The ports are listed in the sequence of the chip select value

PORT	I/O ADDRESS	CS #	FUNCTION
ROM Chip Select	N/A	00	Chip Select For BIOS ROM
Keyboard ControL	060 - 06E Even	01	Chip Select For 8042
80287	00E0 - 00FF	02	Chip Select For Numeric Processor
Power Control	7072	03	PMC Write Strobe 0
Reserved		04	Reserved
Real Time Clock	070	05	RTC ALE
Real Time Clock	071	06	RTC Write Strobe
Real Time Clock	071	07	RTC Read Strobe
Floppy Operation Chip Select	3F2 372	08	Primary Address Secondary Address
Floppy Chip Select	3F4, 3F5 374, 375	09	Primary Address Secondary Address
Floppy Control Chip Select	3F7 377	0A	Primary Address Secondary Address (Floppy Enabled, HD Disabled)
Floppy And HD Control Chip Select	3F7 377	0B	Primary Address Secondary Address (Floppy Enabled, HD Enabled)
Hard Disk Chip Select	1F0, 1F1 - 1F7 170, 171 - 177	0C	Primary Address Secondary Address

TABLE 7-1. I/O ADDRESS AND CHIP SELECT ASSIGNMENTS

16

PORT	I/O ADDRESS	CS # ②	FUNCTION
Hard Disk Chip Select	3F6 3F7 ① 376 377 ①	OD	Primary Address, IDE Mode Only Secondary Address, IDE Mode Only
Serial Port A Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	0E ②	
Parallel Port 0 Chip Select	278 - 27B 378 - 37F 3BC - 3BF	0F	
Serial Port B Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	10 ②	
Program Chip Select	PROG	11	
SCSI	3530 - 353X	12	
Cache Flush	F872	13	
EMS	 F072 F472	14 15 16	External EMS 48 MHz Clock Disabled 48 MHz Clock Enabled
Power Control	7872	17	PMC Write Strobe 1
Reserved		1E	Reserved
Reserved		1F	Reserved

① IDE Hard disk enabled, floppy disabled

② The CS # (Chip Select number) is the decoded value of CS4 - CS0. If the programmed chip select corresponds to any other decode, the programmed chip select is suppressed. If serial port A and B are programmed for the same address, serial port B chip select is suppressed.

TABLE 7-1. I/O PORT ADDRESS CHIP SELECT ASSIGNMENTS cont.

8.0 POWER MANAGEMENT CONTROL

The WD75C10 and WD76C10 support only the PMC inputs and do not support any of the PMC outputs or PMC interrupt functions. The WD76C10LP supports all PMC input, output and interrupt functions.

The processor power down mode is initiated by writing to the PMC control registers located at ports 7072 and 7872. The CPURES signal is asserted, then tri-stated. An internal 200K pullup resistor holds the CPURES active. The Processor Power Down (PMC # 5) signal from the PMC Control register is used to control the power converter from the processor. The WD76C10LP holds CPUCLK, READY, HOLD, INTRQ and NMI low to the processor.

The same conditions used to restart a stopped clock also initiate the power up mode. The power up mode is entered by an unmasked DRQ, unmasked IRQ interrupt or a PMC input change resulting in an unmasked NMI to port 9072. A Processor Power Good signal is then input on the PMCIN pin. After 1 ms., PMC Processor Power Good signal is checked for a logic 1 state. At this time, CPURES is driven high and the CPUCLK, READY, HOLD, INTRQ and NMI signals are driven to their correct states. CPURES remains asserted for 64 additional CPUCLKs.

The PMC unit is composed of two external chips, 74HCT373 octal latch used for the eight PMC outputs from data bus ED0 - ED7 and a 74HCT151 8:1 multiplexer used for the PMCIN signal. The PMC output latches are cleared at power up (see Figure 5-1).

The keyboard processor may access the WD76C10LP's internal registers by way of the PMC logic. The keyboard processor starts a local access by asserting LCL_REQ, which causes PMCIN 2 to be asserted and written in the PMC input register at port 8872 (see Figure 5-1 and Table 8-2). The WD76C10LP arbitrates with refresh, DMA and master for a hold cycle from the processor. When the processor returns a hold acknowledge (HLDA), the WD76C10LP asserts LCL_ACK (PMC output 3 from port 7072) on the ED0 - ED7 data bus. The keyboard processor then passes the opcode/address byte to the WD76C10LP on the data bus and drops the LCL_REQ. The WD76C10LP responds by de-asserting LCL_ACK.

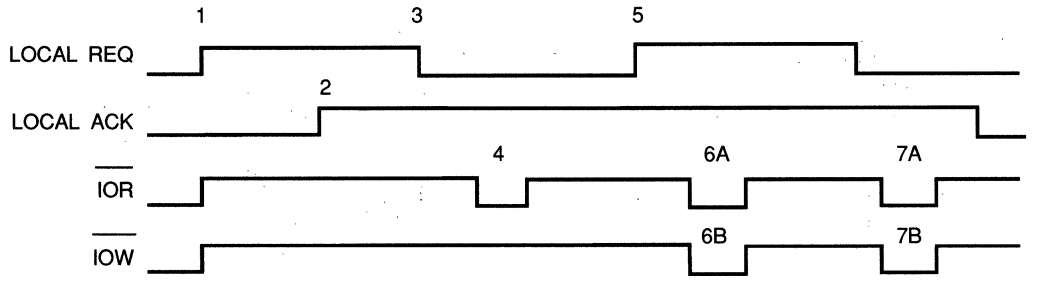
If the opcode specified a register write, data high (DEN1, D15 through D00) and data low (DEN0, D15 through D00) bytes are passed to the WD76C10LP. If the opcode specified an I/O read, the data high and data low bytes are sent from the WD76C10LP to the keyboard processor.

All special operation registers within the WD76C10LP may be accessed in this manner without first unlocking the register. See Section 2.8.2, port address F073, for lock/Unlock Register. This method allows the keyboard processor to control speed switching and other parameters without host processor intervention.

Figure 8-1 shows the handshake procedure, followed by the keyboard controller and the WD76C10LP.

Figures 8-2 and 8-3 represents the power down and power up sequence and control.

16



1 8042 Requests local data transfer

2 WD76C10LP returns LOCAL_ACK after receiving HLDA from the host processor

3 8042 loads address and OPCODE into data register, then drops LOCAL_REQ

4 WD76C10LP reads address and OPCODE

5 8042 Reloads data register with high byte, then asserts LOCAL_REQ

6A WD76C10LP Reads high byte

7A WD76C10LP Read low byte, writes to internal register

FOR READ CYCLE OF WD76C10LP INTERNAL REGISTER:

6B WD76C10LP Writes high byte to 8042

7B WD76C10LP writes low byte to 8042

OP_CODE FORMAT

7	6	5	4	3	2	1	0
DIR	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	RSV

DIR = 1 - Read register (generates IOW to 8082)

DIR = 0 - Write register (generates IOR to 8082)

FIGURE 8-1. REGISTER ACCESS BY KEYBOARD CONTROLLER

8.1 PMC OUTPUT CONTROL REGISTERS

PMC OUTPUT CONTROL 7:0

Port Address 7072 - Bits 07-00 are read only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
OUT 7	OUT 6	OUT 5	OUT 4	OUT 3	OUT 2	OUT 1	OUT 0

Featured only in the WD76C10LP

PMC OUTPUT CONTROL 15:08

Port Address 7872 - Bits 07-00 are read only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
OUT F	OUT E	OUT D	OUT C	OUT B	OUT A	OUT 9	OUT 8

PMC NO.	PMC OUTPUT SIGNAL PORT 7072	PMC NO.	OUTPUT SIGNAL PORT 7872
0	CPU Clock driver enable	8	User defined
1	LCD Enable	9	User defined
2	Backlight enabled	A	User defined
3	LCL_ACK	B	User defined
4	LCL_ATN	C	User defined
5	Processor power down	D	User defined
6	Gate A20	E	User defined
7	Full power down	F	User defined

TABLE 8-1. PMC OUTPUT SIGNALS

16

8.2 PMC TIMERS

Port Address 8072 - Read and Write

15	14	13	12	11	10	09	08
BL_TIMEOUT							

07	06	05	04	03	02	01	00
LCD_TIMEOUT							

Signal Name	Default At RSTIN
BL_TIMEOUT ☆	0 0 hex
LCD_TIMEOUT ☆	0 0 hex

☆ Featured only in the WD76C10LP

When no keyboard interrupts have occurred for the time specified by BL_TIMEOUT or LCD_TIMEOUT, PMC Output 1 or 2 is written to the PMC OUTPUT CONTROL 7:0 register at Port Address 7072 (see Table 8-1) to disable the LCD or Backlight. The timer is reset and the Backlight and LCD control re-enabled at the refresh cycle following a keyboard interrupt. The same timer is used for the Backlight and LCD timeout.

The timeout delay may be programmed in increments of five seconds, to a maximum of 1,270 seconds, or 21 minutes and 16 seconds.

Bits 15-08 - BL_TIMEOUT, Backlight Time Out

00 hex - Backlight always disabled
01 hex - Enabled for 5 seconds
02 hex - Enabled for 10 seconds

Through

FE hex - enabled for 254 X 5 seconds
FF hex - Backlight enabled

Bits 07-00 - LCD_TIMEOUT, LCD Time Out

00 hex - LCD always disabled
01 hex - Enabled for 5 seconds
02 hex - Enabled for 10 seconds

Through

FE hex - enabled for 254 X 5 seconds
FF hex - LCD enabled

8.3 PMC INPUTS

Port Address 8872 - Read and Write

15	14	13	12	11	10	09	08
PMC_UPD	EN_LCL	AF 7	AF 6	AF 5	AF 4	AF 3	AF 2

07	06	05	04	03	02	01	00
IN 7	IN 6	IN 5	IN 4	IN 3	IN 2	IN 1	IN 0

Signal Name	Default At RSTIN
PMC_UPD ☆☆	0
EN_LCL ☆	0
AF7-AF2 ☆	0
IN7-IN0	NA

☆ Featured only in the WD76C10LP

☆☆ Not Featured in the WD75C10

Bit 15 - PMC_UPD, Enable PMC update
Not featured in the WD75C10

PMC_UPD = 0 -
No update cycles occur.

PMC_UPD = 1 -
A change of state of PMC outputs 7 through 0 (port address 7072) or the internal A20 GATE, causes an update cycle of the PMC 7:0 output latch.

Bit 14 - EN_LCL, Enable local request
Featured only in the WD76C10LP

EN_LCL enables the PMCIN 2 to initiate a local access of the WD76C10LP internal registers from the keyboard controller.

EN_LCL = 0 -
PMCIN 2 is user defined

EN_LCL = 1 -
PMCIN 2 is LOCAL_REQ

Bits 13-08 - AF7-AF2, ATN (attention flags)
Featured only in the WD76C10LP

Transitions of certain PMC inputs (IN7-0 of this register) generate an ATN to the keyboard controller and set the PMC interrupt flags at port 9072. A PMC interrupt flag is cleared by writing a 0 to the particular IF7-IF2 bit in port 9072. Writing a 1 does not set the interrupt flag. The corresponding PMC input (IN7-0) cannot be changed until the interrupt flag at port 9072 is cleared. The interrupt enables (EI7-EI2) are controlled by port C872. AF7-AF2 operate independently from EA7-EA2 in port C872.

AF7-AF2 = 0 -
A PMC ATN is not generated

AF7-AF2 = 1 -
A PMC ATN is generated

Bits 07-00 - IN7-IN0, PMC inputs 7-0

The state of IN7 through IN0 are available to all three System Controllers. In the WD76C10LP, the individual IN7 - IN0 bits are locked when an interrupt is generated and can not be changed until the corresponding interrupt enable (EI7 - EI2) in port C872 is reset (see Table 8-2).

16

8.4 PMC INTERRUPT ENABLES

Port Address C872 - Read and Write

15	14	13	12	11	10	09	08
EI7	EI6	EI5	EI4	EI3	EI2		
Interrupt Enable							

07	06	05	04	03	02	01	00
EA7	EA6	EA5	EA4	EA3	EA2		
Attention Enable							

Signal Name	Default At RSTIN
EI7-EI2 ☆	0-0
EA7-EA2 ☆	0-0

☆ Featured only in the WD76C10LP

Bits 15-10 - EI7-EI2, Interrupt enable 7 through 2

EI7 through EI2 enable the generation of an NMI when the corresponding PMC input in port 8872 changes state. For example, when EI7 is a 1 and IN_7 changes from a 0 to 1 an NMI will be generated.

EI7-EI2 = 0 -
Interrupts not enabled

EI7-EI2 = 1 -
Interrupts are enabled

Bits 09, 08 - Not used, state is ignored

Bits 07-02 - EA7-EA2, Attention enable

EA7 through EA2 enable the generation of an ATN by the corresponding IN_7 through IN_2. ATN is the attention signal to the keyboard controller.

EA7-EA2 = 0 -
ATN is not enabled

EA7-EA2 = 1 -
ATN is enabled

Bits 01, 00 - Not used, state is ignored

PMC INPUT NUMBER ①	PMC INPUT NAME	INTERRUPT ON	SETS FLAG NUMBER ②
00	$\overline{\text{TURBO}}$		
01	PROC_PWR_ GOOD		
02	LCL_REQ or User Defined	Transition	IF2
03	User Defined	Transition	IF3
04	User Defined	Transition	IF4
05	User Defined	Transition	IF5
06	User Defined	Transition	IF6
07	User Defined	Active Edge	IF7

① Port Address 8872, section 8.3

② Port Address 9072, section 8.5

TABLE 8-2. PMCIN INPUTS

8.5 NMI STATUS

Port Address 9072 - Read and Write

15	14	13	12	11	10	09	08
0	0	0	0	0	0	0	0

07	06	05	04	03	02	01	00
IF7	IF6	IF5	IF4	IF3	IF2	0	0
		Interrupt Flags					

Signal Name	Default At RSTIN
IF7-IF2 ☆	0-0

☆ Featured only in the WD76C10LP

Bits 15-08 - Not used, must be 0

Bits 07-02 - IF7-IF2, Interrupt flags 7 through 2
Featured only in the WD76C10LP

An NMI is generated and the PMC interrupt flags (IF7-IF2) are set by transitions of the PMC inputs listed in Table 8-2. IF7 through IF2 may be reset by writing a 0 to the corresponding EI7 through EI2 or EA7 through EA2. If both EI and EA are set, both must be reset to clear the interrupt flag. The corresponding PMC input cannot be changed until the interrupt flag is reset. EI and EA are located at port C872.

Bits 01, 00 - Not used, must be 0

8.6 Shadow Register

Port Address D072 - Read only

15	14	13	12	11	10	09	08
SP_A		SP_B		PP_2			

07	06	05	04	03	02	01	00
PP_0							

Signal Name	Default At RSTIN

This register is particulary usefull in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices.

Bits 15, 14 - SP_A, Serial Port A Register 2

This field represents bits 7 and 6 of Serial Port A Register 2.

Bits 13, 12 - SP_B, Serial Port B Register 2

This field represents bits 7 and 6 of Serial Port B Register 2.

Bits 11-08 - PP_2, Parallel Port Register 2

This field represents bits 3-0 of Parallel Port Register 2

Bits 07-00 - PP_0, Parallel Port Register 0

This field represents bits 7-0 of Parallel Port Register 0.

16

8.7 SAVE AND RESUME

When the WD76C10LP is in the Save And Resume mode, the power supply current for the WD76C10LP is typically less than 500 µA.

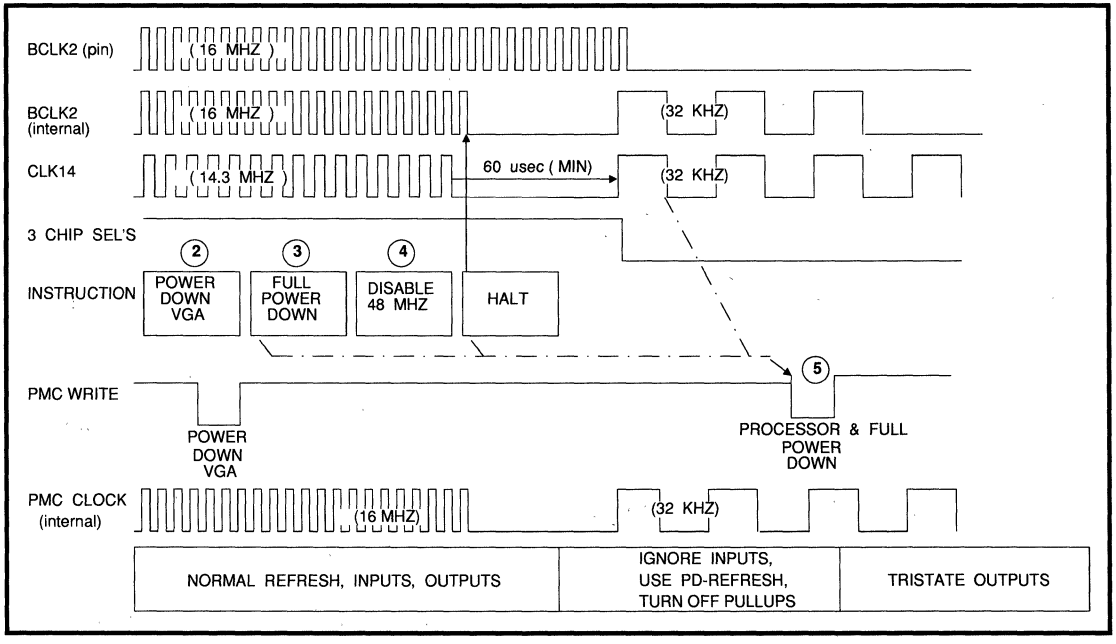


FIGURE 8-2. POWER DOWN

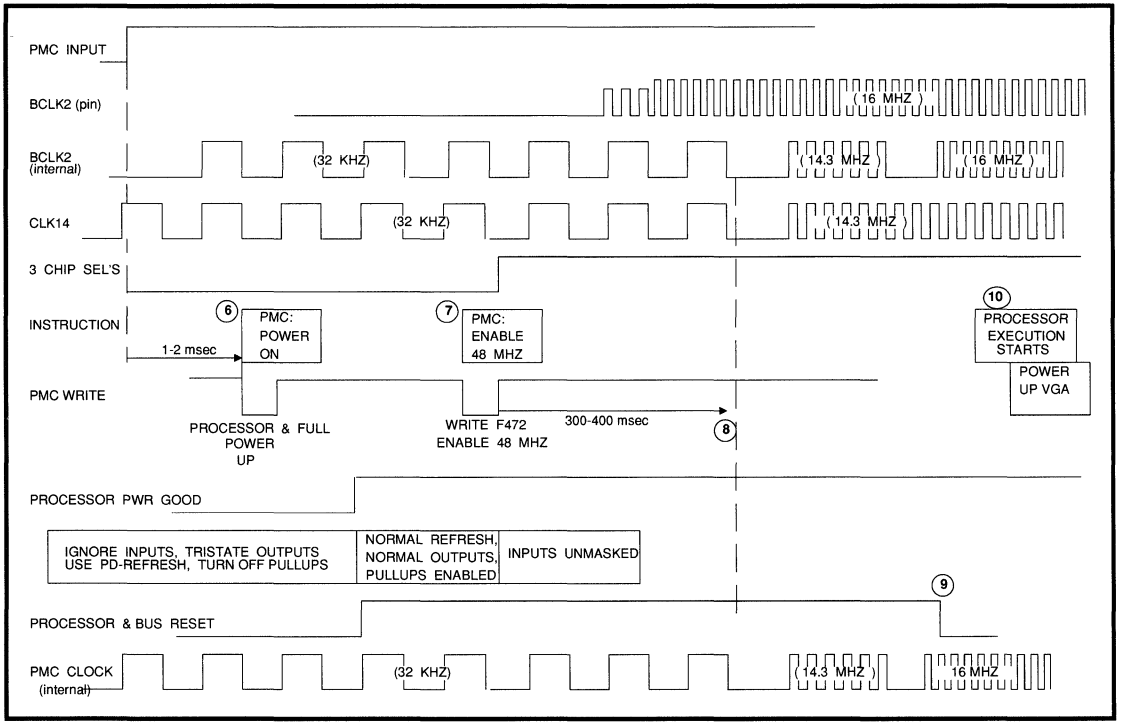


FIGURE 8-3. POWER UP

16

9.0 DIAGNOSTIC MODE

Simultaneously asserting $\overline{\text{MASTER}}$, $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$, while $\overline{\text{RSTIN}}$ is asserted, causes all output pins to become tri-stated. The outputs remain tri-stated if $\overline{\text{RSTIN}}$ is de-asserted while $\overline{\text{MASTER}}$, $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ are asserted. The outputs become active drivers when $\overline{\text{RSTIN}}$ is asserted and any of the $\overline{\text{MASTER}}$, $\overline{\text{MEMR}}$ or $\overline{\text{MEMW}}$ are not asserted. This all output tri-state mode allows an in-circuit board tester to drive the System Controller's output pins.

9.1 DIAGNOSTIC REGISTER

Port Address 9872 - Read and Write

15	14	13	12	11	10	09	08
VER			CLK_ TST	REF_ MAS	ALT_ A20		CLK SW

07	06	05	04	03	02	01	00
SX	DS	DIAG					

Signal Name	Default At RSTIN
VER	VER #
CLK_TST	0
REF_MAS	0
ALT_A20	0
CLK_SW	0
SX	X
DS	0
DIAG	00000

Bits 15, 14 ,13 - VER, version number

The initial version number is 000 and is incremented with every mask change.

Version
- 000 Initial
- 010 Early production
- 011 Production

Bit 12 - CLK_TST, Clock Test

Diagnostics for factory use only.

Bit 11 - REF_MAS, bus master refresh

Additional external logic may be required to support the bus master initiated refresh.

REF_MAS = 0 -
Does not support bus master initiated refresh (Default value).

REF_MAS = 1 -
Supports bus master initiated refresh.

Bit 10 - ALT_A20, Alternate Gate A20

Normally, the Alternate Gate A20 signal from port 092 is OR'ed with the 8042 Gate A20.

When the ALT_A20 bit is set, the Alternate Gate A20 control bit automatically changes state to match the keyboard's Gate A20. Bit 1 (ALT_A20G) of port 092 is set or reset according to the way 8042 is programmed. When the keyboard data port is read using the D1 keyboard controller command, the state of the Gate A20 is replaced by that of ALT_A20.

The state of the A20 gating signal is available on PMC output 6 by reading port 7072 (see Table 8-1). The state of PMC output 6 changes immediately if port 092 is used, and changes at the next refresh if the keyboard A20 gate function is used.

ALT_A20 = 0 -
Normal Alternate Gate A20 (Default value).

ALT_A20 = 1 -
Automatic Gate A20

Bit 09 - Not used, state is ignored.

Bit 08 - CLK_SW, clock switch

The short clock switch reset pulse width is 1 µs plus 16 CPUCLKs.

CLK_SW = 0 -
Short clock switch reset width (Default value)

CLK_SW = 1 -
1 ms clock switch reset width

Bit 07 - SX, 80386SX processor

At power up the System Controller samples the type of processor in the system.

SX = 0 -
80286 processor was detected.

SX = 1 -
80386SX processor was detected.

Bit 06 - DS, diagnostic signal

DS represents the state of the diagnostic signal selected by DIAG (bits 05 through 00).

Bits 05-00 - DIAG, diagnostic function

DIAG selects the diagnostic function to be performed. The DS bit represents the state of the signal selected. Table 9-1. lists the tests available.

DIAG = 00000 - Diagnostic output disabled, speaker normal.

DIAG = 00001 - Diagnostic output disabled, speaker disabled.

DIAG	FUNCTION	DIAG	FUNCTION
00000	Normal Speaker	10000	Reserved
00001	Speaker Disabled	10001	"
00010	Reserved	10010	"
00011	"	10011	"
00100	"	10100	"
00101	"	10101	"
00110	"	10110	"
00111	"	10111	"
01000	"	11000	"
01001	"	11001	"
01010	"	11010	"
01011	"	11011	"
01100	"	11100	"
01101	"	11101	"
01110	"	11110	"
01111	"	11111	"

TABLE 9-1. DIAGNOSTIC TESTS

16

9.2 DELAY LINE DIAGNOSTIC REGISTER

Port Address A072 - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
LAT	DL	DELAY					

Signal Name	Default At RSTIN
LAT	0
DL	0
DELAY	NA

Bit 07 - LAT, Latch output strength

The delay line count value (bits 05-00) is used to control the output buffer strength. The output buffer strength is normally adjusted every time the delay count changes. LAT may be used to lock the buffer strength at its present value.

LAT = 0 -
The output buffer strength is adjusted when the delay count changes.

LAT = 1 -
The output buffer strength is locked at its present value.

Bit 06 - DL, Delay freeze

The internal self tuning delay line normally is updated by one delay element during every refresh cycle. For test purposes, the delay may be forced to stop generating calibration cycles. When delay line updates are frozen, the tester may write different delay line counter values in bits 05-00.

DL = 0 -
Normal delay line operation (Default value)

DL = 1 -
Freeze delay line

Bits 05-00 - DELAY, Delay counter value

The delay line counter value is used to control the output buffer strength.

This register may be written to when DL is set to one.

10.0 ELECTRICAL SPECIFICATIONS

10.1 MAXIMUM RATINGS

Supply Voltage (VCC) with respect to VSS (ground) . . . . Volts

Voltage on any pin with respect to VSS (ground) . . . . . Volts

Operating Temperature . . . . . 0°C (32°F) to 70°C (158°F)

Storage Temperature . . . . . -C (-F) to C (F)

Power Dissipation . . . . . mW

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

10.2 DC OPERATING CHARACTERISTICS

TA = 0°C (32°F) to 70°C (158°F)

Vcc = +5V ±.5V (10%) for WD76C10LP

Vcc = +5V ±.25V (5%) for WD75C10 and WD76C10

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Leakage		± 10	µA	Vin = .4 to Vcc
IOZ	Tri-state And Open Drain Output Leakage		± 10	µA	Vout = .4 to Vcc
VIH	Input High Voltage	2.0		V	
VIL	Input Low Voltage		.8	V	
VIHC	CPUCLK Input High	3.6		V	
VIL	CPUCLK Input Low		.6	V	
ICC	Supply Current		200 150	mA mA	Inputs at 2.0V Inputs at 5.0V Outputs Open, CPUCLK = 32 MHz
ICCSB	Typical Supply Current, Power Down Mode For WD76C10LP	.5		mA	Typical, CPUCLK Off, CLK14 = 32 KHz

TABLE 10-1. DC OPERATING CHARACTERISTICS

16

FOR PINS WITH INTERNAL PULLUPS:

MASTER, IOCK, IOCS16, MEMCS16, ZEROWS, IOCHRDY, RDYIN, S0, S1, BHE, M/IO, HLDA, PEACK, NPBUSY, NPERR, PDREF

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-12	-50	µA	Not save and resume mode

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

DACK2-0, DACKEN, D15-D0, READY, CPURES, HOLD, INTRQ, A23-A0, NMI, DPH, DPL, RA10-RA8, RA7/ED7-RA0/ED0, BHE, RAS3-RAS0, CASL3-CSL0, CASH3-CASH0, W/R, DT/R, DEN1, DEN0, SDT/R, SDEN, CSEN, LOMEG

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	Vcc -.8		V	IOUT = -100 µA
VOH	Output High Voltage	2.4		V	IOUT = -2 mA
VOL	Output Low Voltage		.4	V	IOUT = 2 mA

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

MXCTL2-0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	Vcc - .8		V	IOUT = -200 µA
VOH	Output High Voltage	2.4		V	IOUT = -4 mA
VOL	Output Low Voltage		.4	V	IOUT = 4 mA

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:
$\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$, AEN, SYSCLK, BALE, LA20, SA0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT = -3 mA
VOL	Output Low Voltage		.5	V	IOUT = 24 mA

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUT:
$\overline{REFRESH}$

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOL	Output Low Voltage		.5	V	IOUT = 24 mA

TABLE 10-1. DC OPERATING CHARACTERISTICS cont.

16

10.3 AC OPERATING CHARACTERISTICS

Table 10-2 lists the timing categories and their Figure and Table numbers.

FIGURE NUMBER	TABLE NUMBER	TITLE
10-1	10-3	Page Mode

TABLE 10-2. TIMING FIGURE/TABLE NUMBERS

50 pF	MXCTL2-0, DACKEN, SPKR, CPUCLK, $\overline{\text{READY}}$, CPURES, HOLD, INTRQ, NMI, W/$\overline{\text{R}}$, DT/$\overline{\text{R}}$, $\overline{\text{DENO}}$, $\overline{\text{DEN1}}$, $\overline{\text{CSEN}}$, ALE, $\overline{\text{BUSYCPU}}$, SDT/$\overline{\text{R}}$, $\overline{\text{SDEN}}$, LOMEG, $\overline{\text{BHE}}$
100 pF	D15-D0, DPH, DPL, A23-A0, $\overline{\text{CASH3}}$-$\overline{\text{CASH0}}$, $\overline{\text{CASL3}}$-$\overline{\text{CASL0}}$
200 pF	$\overline{\text{IOR}}$, $\overline{\text{IOW}}$, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, AEN, SYSCLK, $\overline{\text{REFRESH}}$, BALE, LA20, SA0, $\overline{\text{RAS3}}$-$\overline{\text{RAS0}}$
350 pF	RA10-RA8, RA7/ED7-RA0/ED0

TABLE 10-3. LOAD CAPACITANCE

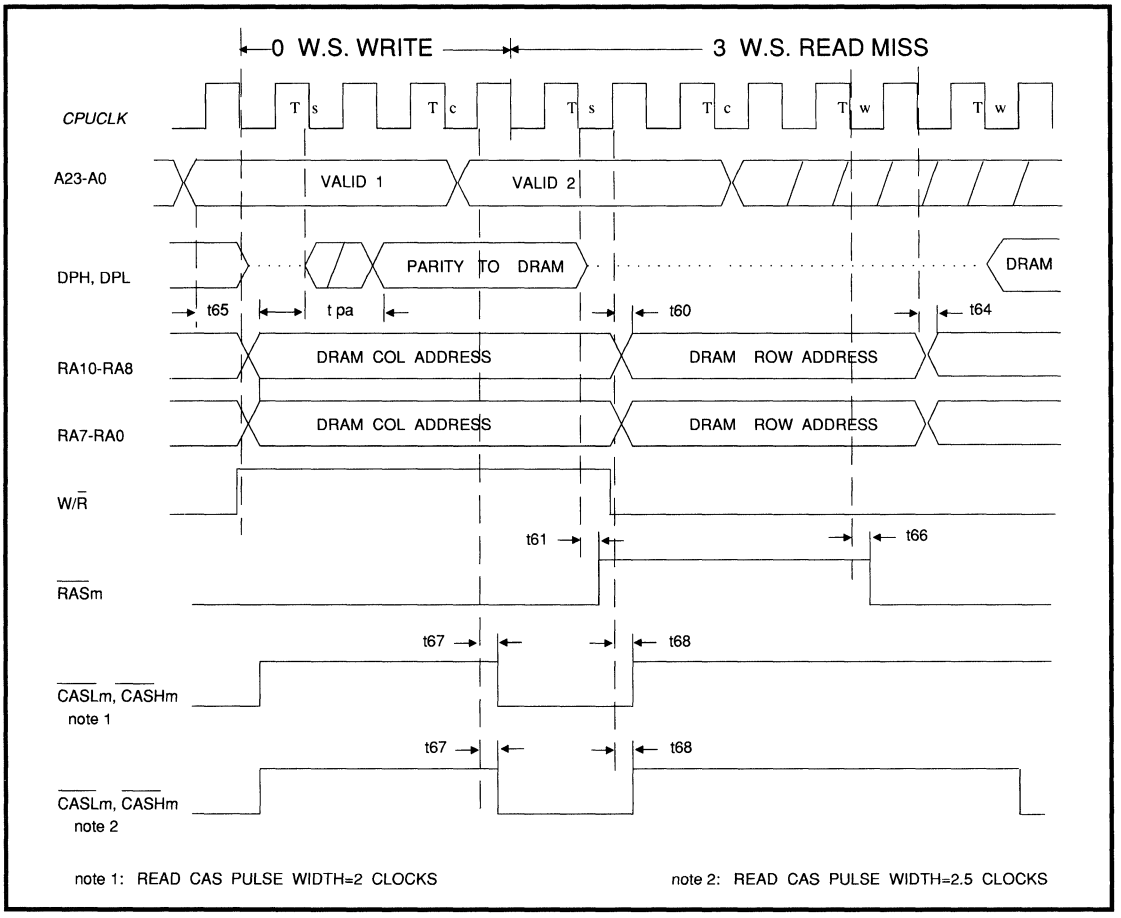


FIGURE 10-1. PAGE MODE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITION
tWR	Clock, $\overline{S0}$, or $\overline{S1}$ to W/$\overline{R}$		20	ns	Load 50 pF
t67, t68	Clock to $\overline{CAS}$		20	ns	Load 100 pF
t61, t66	Clock to $\overline{RAS}$		25	ns	Load 200 pF
t65	Column Address from A23-A0		35	ns	Load 350 pF
tPA	Parity Data from D15-D0		25	ns	Load 100 pF
t60	Clock to Row Address		35	ns	Load 350 pF
t64	Clock to Column Address		35	ns	Load 350 pF

TABLE 10-4. PAGE MODE TIMING

16

11.0 PACKAGE DIMENSIONS

Figure 11-1. Illustrates the 132-Pin PQFP package showing the dimensions in inches.

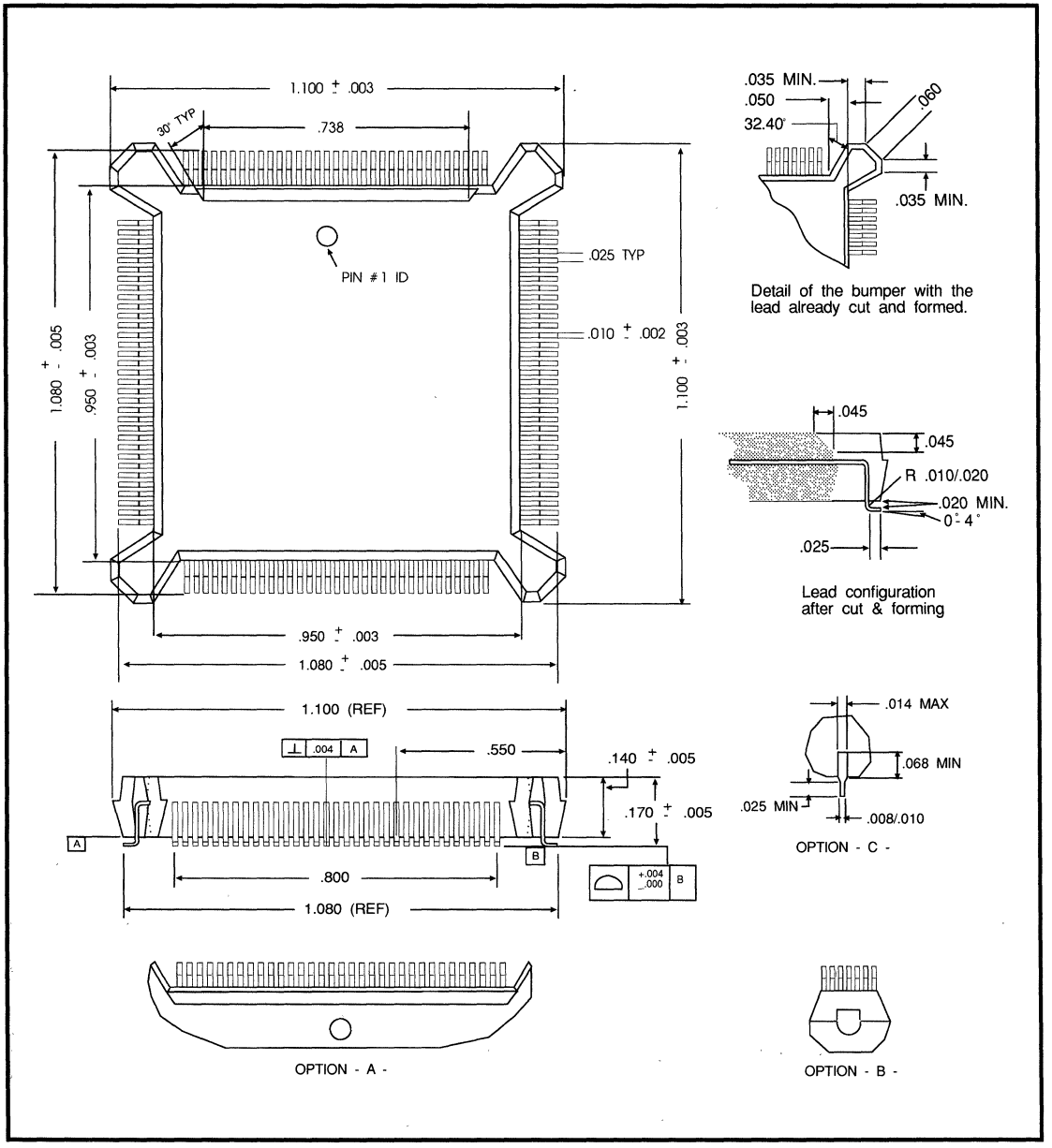


FIGURE 11-1. 132-PIN PQFP PACKAGE

SYSTEMS LOGIC/PERIPHERAL

WD76C20

Floppy Disk Controller,

Real Time Clock, IDE Interface,

and Support Logic Device

17

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

RELATED PUBLICATIONS

The following publications contain information relating to the operation and application of the WD76C20:

Western Digital WD37C65-series Data Book
Western Digital WD76C10 Data Book
Western Digital WD7600 Data Book

1.0 INTRODUCTION

1.1 DESCRIPTION

The Floppy Disk Controller (FDC) portion of the WD76C20 is a VLSI Super Cell that provides all needed functions between the host processor peripheral bus and the cable connector to the floppy disk drive. This provides a total solution to floppy subsystem control. The FDC has a software transparent power down mode feature which broadens its use in laptop and portable systems.

On the disk drive interface, the FDC includes data separation and write precompensation in addition to the usual formatting, encoding/decoding, stepper motor control and status sensing functions. All inputs are TTL compatible, and outputs are high-current, open-drain drivers meeting the ANSI specification of 48 mA.

The host interface has been designed to support up to 12 MHz bus speeds without the use of wait states. Additionally, input strobes are Schmitt Triggers. The data bus drive capability is12 mA IOL, and 5 mA IOH, allowing, in most applications, direct interconnection to bus structures without the use of buffers or transceivers. For PC and PC /AT applications, qualification of interrupt request and DMA request is provided.

Traditionally, data rate selection, drive selection, and motor control have been output ports of the host processor architecture. In the PC AT, these functions were latched into registers addressed within the I/O mapping of the system. These registers, Operations and Control, are incorporated into the FDC.

All clock generation necessary for the floppy disk subsystem is included in the FDC portion of the WD76C20. A 16 MHz crystal oscillator circuit provides the necessary signals for internal timing when external clocks are unavailable. The 16 MHz signal handles all standard data rates (500 and 250 Kbits/sec) used in PC/AT designs, and a non-standard data rate (300 Kbits/sec.). If neither the board space nor the 16 MHz TTL clock is available, FCLK1/FX1 can be driven with a 16 MHz TTL level clock, and FCLK2 with a 9.6 MHz TTL clock. This will handle standard data rates (500, 250, and 125 Kbits/sec.), and a non-standard data rate (300 Kbits/sec.).

The Real Time Clock plus SRAM provides all the functionality of a Motorola MC146818A usable in the PC/AT environment. It provides a complete time-of-day clock with alarm, calendar, periodic interrupt generator, and 114 bytes of low power static RAM.

The Bus Interface Logic (BIL) section of the WD76C20 provides the DB7 multiplexing necessary to implement a PC/AT compatible IDE drive interface and the Chip Select Logic section incorporates miscellaneous chip selects and control strobes necessary for the implementation of a PC/AT compatible system. The Suspend/Resume section supports the chip set power down mode by providing a 14.318 MHz clock during Resume and a 32.768 KHz clock during Suspend mode. An external DRAM refresh signal is also provided by the Suspend/Resume section to support the chip set.

The WD76C20 is designed with Western Digital's 1.25 micron CMOS process. It is available in 84-lead PLCC and PQFP packages.

1.2 FEATURES

- 84-pin PLCC and PQFP packages
- 5V only supply requirement
- 3.0V battery backup supply for the RTC and 114 byte SRAM
- Implemented in a low-power, high performance CMOS technology
- Floppy Disk Controller (FDC) software transparent power-down mode with low standby ICC current. FDC features:
  - 256 tracks support
  - 100% software compatible with NEC 765A
  - Integrated high performance DPLL data separator:
    - 125, 250, 300, 500 Kbits/sec and 1 MB/sec data rates
    - Option to select 150 Kb/sec FM and 300 KB/sec MFM data rates only
    - Automatic Write Precompensation:
    - Defeat option
    - Inner track value of 125 or 187 ns pin selectable
  - On chip clock generation:
    - 2 TTL clock inputs, or
    - Single 16 or 32 MHz crystal circuit and one TTL clock input
  - Host interface read/write accesses compatible with 80286 microprocessors at speeds up to 12 MHz with 0 wait states
  - Direct floppy disk drive interface - no buffers needed
    - 48 mA sink output drivers
    - Schmitt Trigger input line receivers
  - FDC direct PC XT/AT interface compatibility
    - Floppy Control and Operations Registers on chip
    - In PC/AT mode, provides required signal qualification to DMA channel
    - IBM BIOS compatible
    - Dual-speed spindle drive support
  - PS/2 type drive support
- Real Time Clock (RTC) features:
  - Software compatible with Motorola MC146818A.
  - Internal time base and oscillator circuitry
  - Counts seconds, minutes and hours
  - Counts days of the week, date, month, and year
  - Time base input for 32.768 KHz square wave
  - Time base oscillator for parallel resonant crystals
  - Binary or BCD representation of time, calendar, and alarm
  - 12 or 24 hour clock with AM and PM in 12-hour mode
  - Daylight savings time option
  - Automatic leap year compensation
  - Interfaced with sofware as 128 RAM locations
  - 114 bytes of general purpose RAM
  - Status bit indicates data integrity
  - Bus compatible interrupt signals (IRQ)
  - Three interrupts are separately software maskable and testable:
    - Time-of-day alarm, once-per-second to once-per-day
    - Periodic interrupt rates from 122 us to 500 ms
    - End-of-clock update cycle

2.0 ARCHITECTURE

This section contains a general architectural overview of the WD76C20 which provides a cost-effective, power-efficient solution to PC systems design problems, especially those relating to "laptop" devices. The section also illustrates the WD76C20's packaging and includes a listing of pin numbers with associated signal mnemonics and functions.

2.1 FUNCTIONAL COMPONENTS

Referring to Figure 2-1, the WD76C20 has three principal functional boundaries. First, it exchanges control signals with the WD76C10 System Controller. Then, under control of the WD76C10, it exchanges data and qualified operational/status information with the host via the system's AT Bus. Finally, on the media side, it provides complete control and data read/write services for from one to four floppy disk units.

Internally, the WD76C20 has the following functional components:

- Chip Select Logic
- Bus Interface Logic
- Floppy Disk Controller

Additional supporting components are:

- Real Time Clock
- 114-byte SRAM (affiliated with the Real Time Clock)
- Suspend/Resume Logic

These functional components are briefly described in the following sections with detailed descriptions provided in Section 3. Signals mentioned in the following narratives are listed and described in Tables 2-1 and 2-2 later in this section.

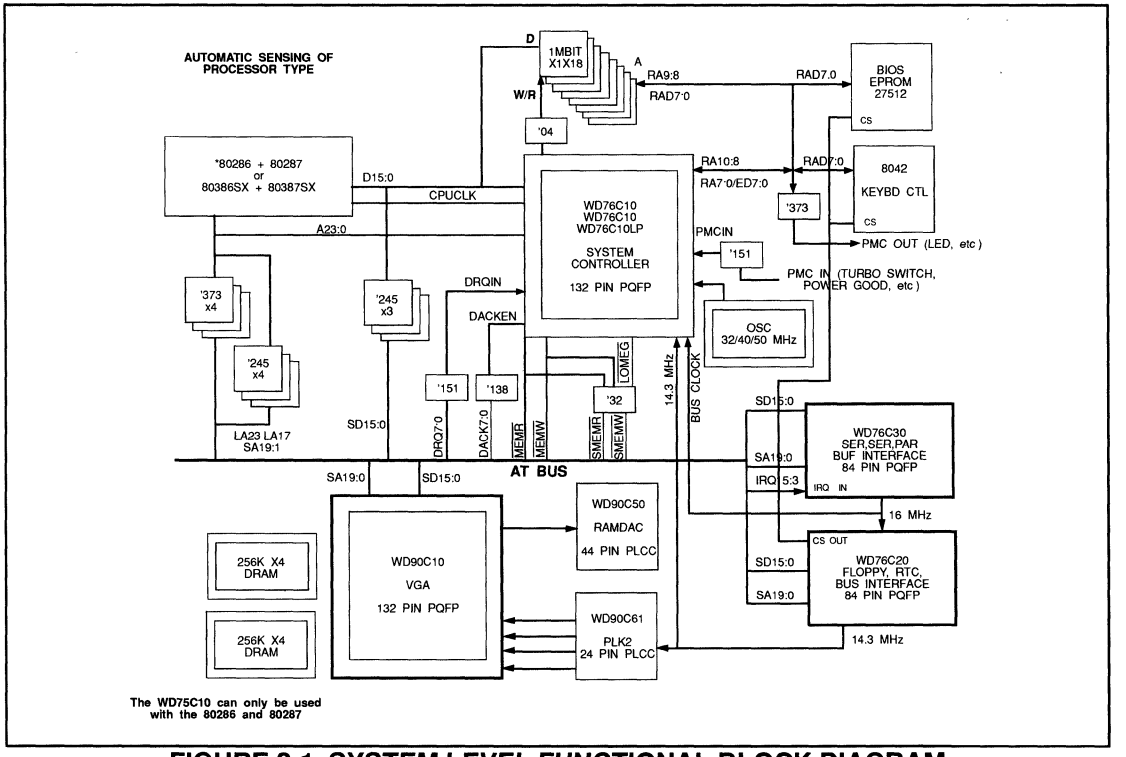


FIGURE 2-1. SYSTEM LEVEL FUNCTIONAL BLOCK DIAGRAM

17

2.1.1 Chip Select Logic

The Chip Select Logic (CSL) component of the WD76C20 provides the decoding needed both for selecting chip functions within the WD76C20 and on the PC/AT motherboard as well. It gets the DPL, DPH, and RA8-RA10 signals from the WD76C10 Systems Controller and outputs appropriately decoded chip select signals (detailed in Section 3.) Overall control of the decoding processes is effected with the CSEN and DACKEN signals from the WD76C10. CSEN enables the decoded output, while DACKEN causes the CSL to ignore the inputs from the WD76C10. Optionally, the chip select inputs (CSEN, DPH, DPL, RA10, RA9, RA8) can be latched by dropping the BALE from a logic 1 to a logic 0. These latches are transparent when BALE is held high or left unconnected.

2.1.2 Bus Interface Logic

The Bus Interface Logic (BIL) component of the WD76C20 controls the buffering of bits D0-D7 between the system's AT Bus and any WD76C20 internal source/destination 8-bit storage cell via the internal bus. It gets the IOR and IOW signals from the WD76C10, and with the appropriate chip selects from the CSL, the BIL parallel-passes D0-D7 from the AT Bus to an internal WD76C20 cell, or vice-versa. The internal cells are:

- The Control, Master Status, Data, or Operation Registers in the Floppy Disk Controller
- The 128 registers in the SRAM affiliated with the Real Time Clock.

The BIL also provides a controlled bidirectional path for bit D7 between the AT Bus and the IDE Drive Port.

2.1.3 Floppy Disk Controller

765A Core - The core of the 765A floppy disk controller has been maintained so the micro-sequencer is functionally equivalent and all commands will execute identically, hence software compatibility is assured. The floppy control state machine on the front-end is also functionally equivalent. The micro-sequencer and control state machine operate at 8 times the selected bit data rate in MFM and 16 times the bit data rate in FM.

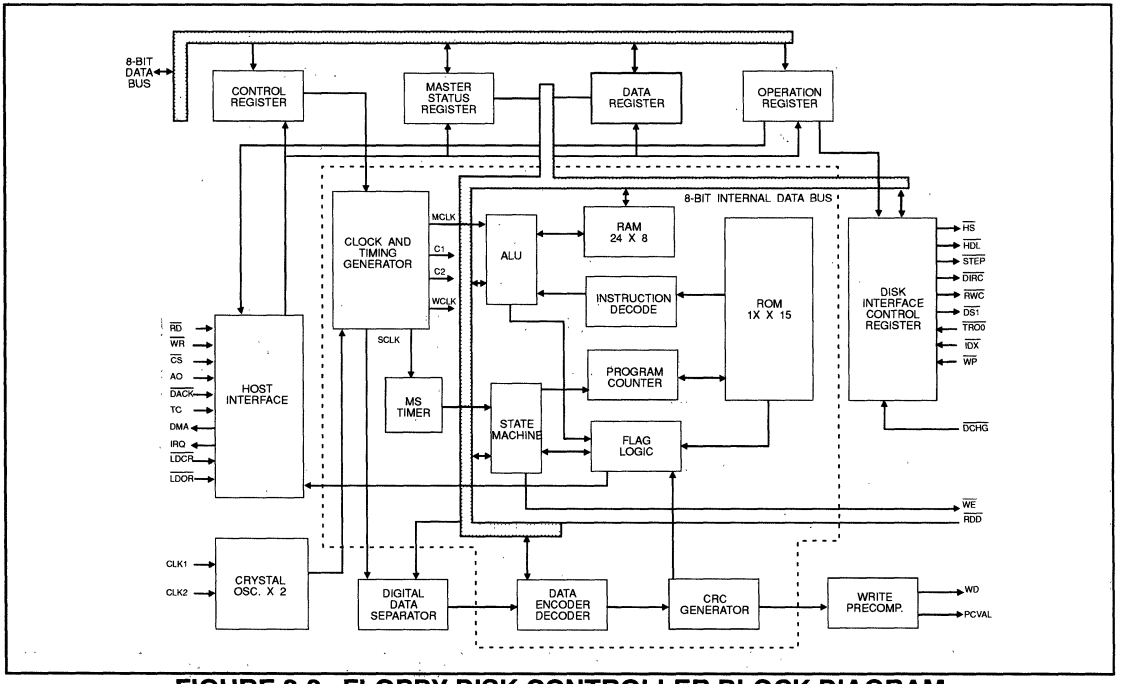


FIGURE 2-2. FLOPPY DISK CONTROLLER BLOCK DIAGRAM

Host Interface - The host access signals are identical to 765A floppy disk controller, but timings have been enhanced. The FDC has 8 internal registers.

The 8-bit main status register contains status information of the FDC and may be accessed any time. Another 4 status registers under system control also give various status and error information. The Control Register provides support logic that latches the two LSB's used to select the desired data rate that controls internal clock generation. Bit 2 of this register is also used to disable the write precompensation logic. The Operations Register provides all the control signals required to select the drive and the spindle motor. In PC/AT mode, Interrupt Request and DMA Request are tri-stated and qualified by DMA Enable, internally provided by the Operations Register. The data bus is designed to handle 20 LSTTL loading.

Automatic Power Down Mode - In this mode, the FDC powers down all circuitry except for the Data Register, the Operations Register, the Control Register, the Master Status Register and the I/O path leading to and from the data bus. Since the crystal oscillator controller circuitry and all non-essential linear circuitry is turned off, the controller will draw very low current. The FDC can return from power down mode by simply polling the Master Status Register, after which the crystal oscillator will turn on, along with the other circuitry.

Data Separator - The FDC incorporates the patent pending digital phase lock loop used in the WD92C32 product. The sample clock rate, SCLK, must be 32 times the data rate.

Write Precompensation - The FDC maintains the standard first level algorithm to determine when write precompensation should be applied. These EARLY and LATE signals are used internally to select the appropriate delay in the Write Data pulse stream. The encoded write data signal is synchronized to the 32 MHz clock, if this is the frequency on pin FCLK1, and clocked through a shift register, FX1. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexer gates the chosen bit to the output. The output data pulse width has 25% duty cycle, i.e. 1/4 of the bit cell period, also equal to 1/2 the WCLK period.

With PCVAL pin = 1, all data will be precompensated by +/- 125 ns regardless of track number and data rate, but only for MFM encoding (no write precomp for FM). If PCVAL = 0, and if a track inside number 28 is accessed, then +/- 187 ns of precomp will be generated. For frequencies other than 32 MHz on FX1, these precomp values will be 2 and 3 SCLK clock cycles respectively.

When a non-standard data rate using FCLK2 is chosen, the precompensation logic is run from this frequency. In this case, the PCVAL function is disabled. Hence precomp values will always be 2 clock cycles. For 9.6 MHz this value is +/- 208 ns. The write precomp can be disabled by the use of bit 2 of Control register for PC AT. With no write precomp, the PCVAL input to the chip is ignored.

Drive Interface - The FDC no longer supports certain pin functions provided for in the 765 predecessor. The output RW/SEEK is used in the 765 based subsystem as a multiplexer select line to allow a pin to have 2 functions depending on whether a read, write or seek type command are under execution. This signal is no longer available externally, but is used within the WD76C20 to assure that no improper pin functionality occurs.

The LCT function has been renamed $\overline{\text{RWC}}$ and resides on a pin of its own with slightly altered active conditions and in PC/AT mode is RPM. $\overline{\text{DIRC}}$ is the only function on that pin and is enabled only during seeks as a power conservation measure.

$\overline{\text{STEP}}$ is also only enabled during seeks and a fault rest (FR) is no longer needed since FLT, fault detects, are not sensed. FLT status, status register #3, bit 7, will always be a logic 0 Track zero, /TR00, status is only sensed during seeks as well.

TS, two-sided, drive status is no longer supported, and status register #3, bits 6 and 3 will both now reflect Write Protect status. The FDC device assumes the drive is ready all the time as DRDY signal is set to logic = 1 internal. This will still result in a FIRQ. This action is acknowledged as a change in status and demands a Sense Interrupt Status command execution in order to clear the FIRQ. Also note that the signals MFM, RDW, WCK and VCO are no longer necessary since all logic associated with these is wholly contained within the FDC.

17

2.1.4 Clock Generation

This logical block provides all the clocks needed by the FDC, including SCLK (Sampling Clock), WCLK (Write Clock) and MCLK(Master Clock). SCLK is the clock which drives the digital phase lock loop data separator during data recovery. This clock frequency is always 32 times the selected data rate, and its frequency is directly the frequency of the signals on FX1 (FCLK1) and FCLK2, whether or not standard data rates are being used (see Table 1). The use of the 32 MHz oscillator output /FX1 is optional if the 1 Mb/sec data rate is not required. If the oscillator is not used, either a 32 MHz or a 16 MHz TTL clock should be applied at FCLK1 (FX1).

WCLK is used by the encoder logic to place MFM or FM on the serial Write Data stream to the disk. WCLK always has a frequency 2 times the selected data rate.

MCLK is used by the microsequencer. MCLK and $\overline{MCLK}$ clock all latches in a 2 phase scheme. One micro-instruction cycle is 4 MCLK cycles. MCLK has a frequency equal to 8 times the selected MFM data rate or 16 times the FM data rate.

In the power down mode, the crystal oscillator and all the clock circuitry is turned off. The FDC will turn on the crystal oscillator, which will in turn activate all the clock circuitry on the chip once the device returns from power down mode.

FX1 FCLK1	FCLK2	SCLK STANDARD	SCLK NON STANDARD
16.0 MHz TTL	9.6 MHz TTL	16.0 MHz	9.6 MHz
16.0 MHz TTL	TIED LOW	16.0 MHz	DISABLED
32.0 MHz XTAL[1]	9.6 MHz TTL	32.0 MHz	9.6 MHz
32.0 MHz XTAL[1]	TIED LOW	32.0 MHz	DISABLED

TABLE 2-1. FDC SAMPLING CLOCK (SCLK) GENERATION

[1] Can be either a crystal or 32 MHz TTL level clock

DATA RATE	CODE	SCLK	MCLK	WCLK
1Mb/s	MFM	32.0 MHz	8.0 MHz	2.0 MHz
500 Kb/s	MFM	16.0 MHz	4.0 MHz	1.0 MHz
500 Kb/s	FM	16.0 MHz	8.0 MHz	1.0 MHz
250 Kb/s	FM	9.0 MHz	4.0 MHz	500 KHz
250 Kb/s	MFM	8.0 MHz	2.0 MHz	500 KHz
300 Kb/s	MFM	9.6 Mhz	2.4 Mhz	600 Khz

TABLE 2-2. FDC MCLK AND WCLK GENERATION

2.1.5 Real Time Clock and SRAM

The Real Time Clock (RTC) component of the 76C20, in conjunction with the 128 byte-register file, provides calendar (day-of-week, day-of-month, month, and year) and clock (hours, minutes, and seconds) information, along with clocked alarms and a periodic interrupt. Referring to Figure 2-3, ten SRAM data registers contain all the clock/time/alarm information with the RTC crystal-controlled oscillator and frequency divider providing the appropriate clock "ticks" that keep them current. Control and status information for the RTC is contained in Registers A-D of the SRAM (detailed in Section 3). Remaining SRAM registers (114) are user-available.

Read and/or write access to the SRAM (control/status, calendar/clock/alarm, and general purpose registers) is through the RTC bus interface. This interface gets signals from the 76C20 Bus Interface and Chip Select Logic functions and appropriately buffers bits D0-D7 between the 76C20 internal bus and the RTC internal bus accessing the SRAM. Calendar/clock/alarm information is processed through Update Logic that:

- Increments calendar/clock counts based on "ticks" received from the Frequency Divider,
- Attends to Daylight/Standard Time and Leap Year adjustments, and
- Formats/deformats the information as straight binary or binary coded decimal data, as selected.

Input power to the RTC component is from the VBAT pin. Switching from System VDD to battery power is accomplished through two diodes as seen in Figure 2-3a.

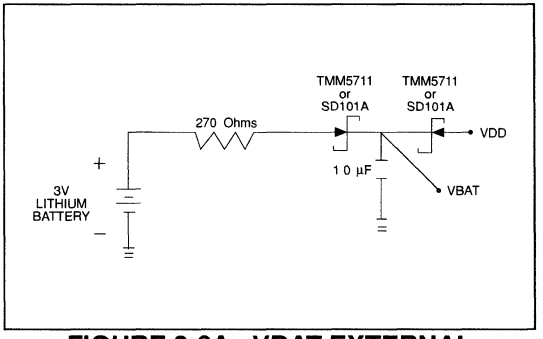


FIGURE 2-3A. VBAT EXTERNAL SUPPORT

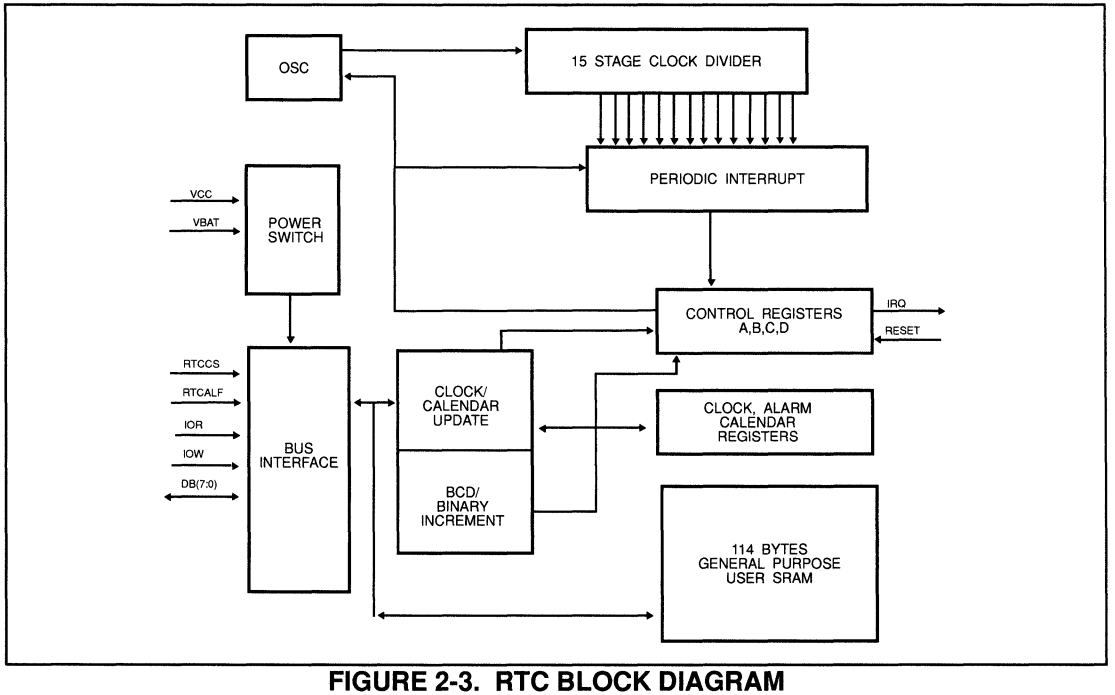


FIGURE 2-3. RTC BLOCK DIAGRAM

17

Time Base Oscillator Circuit - The oscillator used to provide the time base for the RTC requires the external circuit shown in Figure 2-4 with the values listed in Table 2-3. The crystal to be used in parallel with the on-chip oscillator should be an AT-cut crystal, with a 32.768 KHz resonant frequency as described in Figure 2-5 and Table 2-3. When in battery backup mode, this circuit is still active, and providing the rest of the RTC with a valid time base.

Power Switch - This functional block is used to detect when the system power is shutting down and the RTC needs to go into battery backup mode. In the event of a full chip power down without a battery backup, the VRT bit of register D will be reset to zero, indicating that the contents of the SRAM and RTC operational registers are not guaranteed. In order to reset the bit, register D must be read after a full power up.

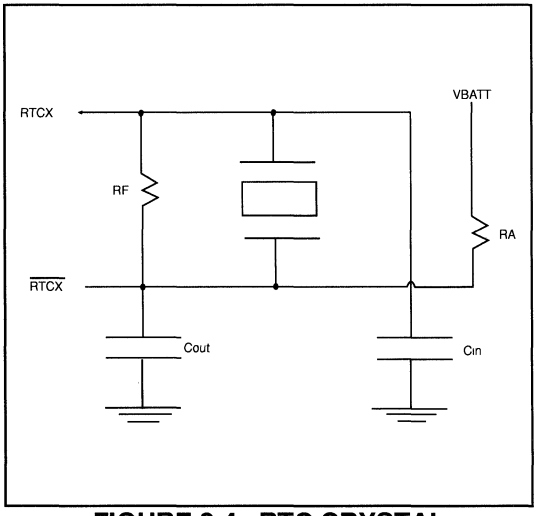


FIGURE 2-4. RTC CRYSTAL OSCILLATOR CONNECTIONS

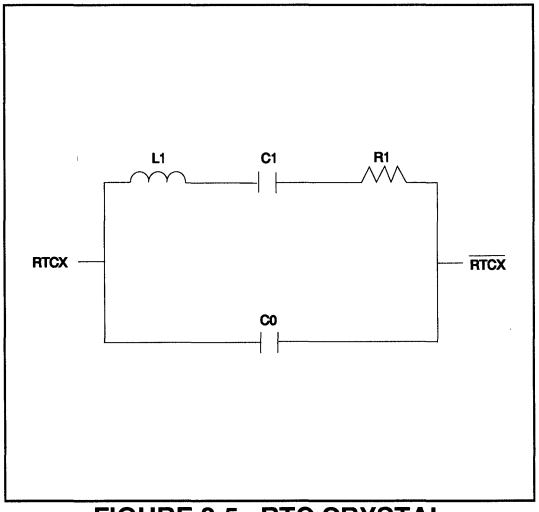


FIGURE 2-5. RTC CRYSTAL PARAMETERS

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
R1	Crystal Motional Resistance		40	K Ohm
C0	Crystal Shunt Capacitance		1.7	pF
C1	Crystal Motional Capacitance		0.0035	pF
Q	Crystal Quality Factor	50		K
Clin	Crystal Circuit Input Capacitance	30	± 5%	pF
Cout	Crystal Circuit Output Capacitance	22	± 5%	pF
RA	Crystal Circuit Drive Level Resistor	340	± 1%	K Ohm
Rf	Crystal Circuit Feedback Resistor	15	22	M Ohm

TABLE 2-3. RTC CRYSTAL CIRCUIT SPECIFICATION

Bus Interface - The RTC Bus Interface block is used to access the internal bus for the WD76C20. Protocol is maintained between the BIL block (Bus Interface Logic) and the RTC Bus Interface. The BIL block generates the RD and WR strobes, and the CS signals are decoded from the external bus by the Chip Select Logic.

Clock Divider - This functional block uses clock divider logic to divide the 32.768 KHz time base into a 1 Hz signal used by the timekeeping blocks. As a side duty, it provides the periodic interrupt block with access to all stages of the division.

Periodic Interrupt - This functional block has access to the various stages of the Clock Divider. With these signals, and under the direction of register A, an RTCIRQ pulse can be periodically generated for the processor from once every 122 µS to once every 500 ms. The Periodic Interrupt function is enabled by the PIE bit in register B.

BCD/Binary Increment & Clock/Calendar Update - This dual purpose logic block is used to increment and update the 10 timing registers and to check for the existence of an alarm condition. Several register bits are used to control this block to prevent contention between a processor access to the information registers and the occurrence of an update cycle.

2.1.6 Suspend/Resume Logic

This functional block is used in conjunction with the RTC time base to provide a 14.318 MHz clock output to the WD76C10, which will switch to a 32.768 KHz clock during the chip set low power suspend mode. The Suspend/Resume block also provides the external DRAM refresh signal, PDREF, that will pulse active low once every 15.26 µS. This block also supports a latched signal that causes CSSERA, CSSERB and CSPAR0 to remain low during Suspend mode, signaling the WD76C30 to disable the 48 MHz crystal.

2.2 PINOUT

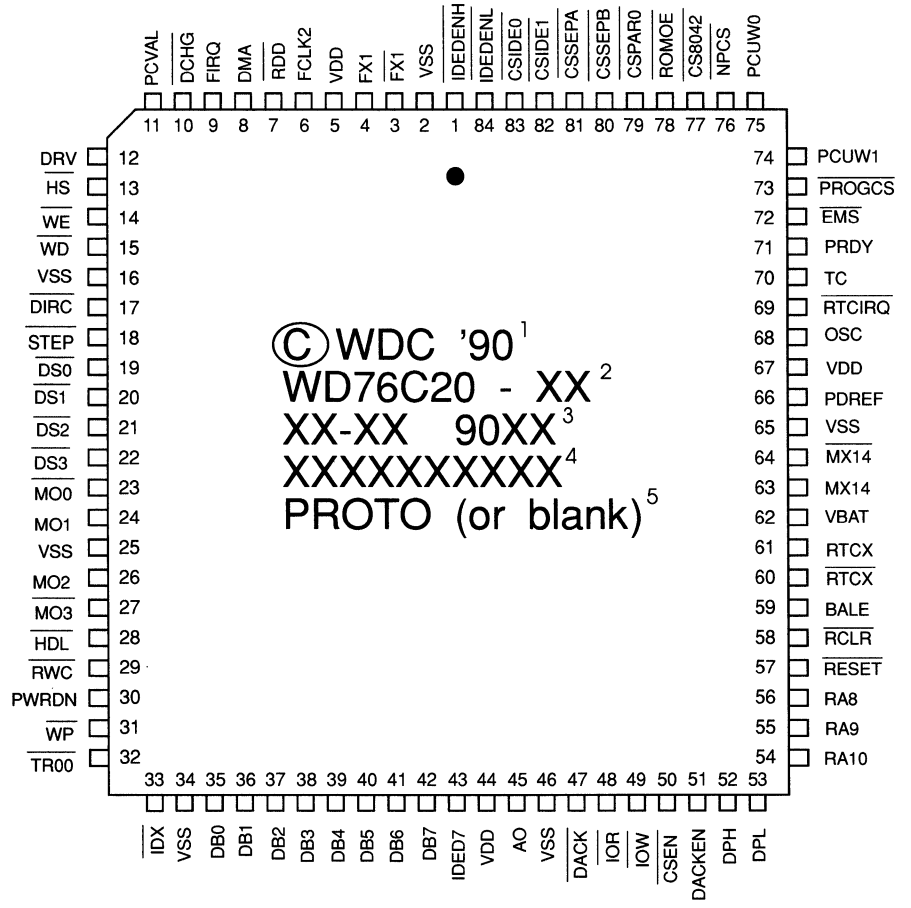
Figure 2-6 illustrates the signal names and pin locations on the 84-pin PLCC/PQFP WD76C20 package. Table 2-4a lists the signal names alphabetically and Table 2-4b lists the signal names in pin number order. Table 2-5 lists the signal names and descriptions, grouped by function.

NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN
A0	45	DS1	20	MO2	26	ROMOE	78
BALE	59	DS2	21	MO3	27	RPM/RWC	29
CSEN	50	DS3	22	MX14	63	RTCIRQ	69
CSIDE0	83	EMS	72	MX14	64	RTCX	60
CSIDE1	82	FIRQ	9	NPCS	76	RTCX	61
CSPAR0	79	FCLK1/FX1	4	OSC	68	RWC/RPM	29
CSSERB	80	FCLK2	6	PCUW1	74	STEP	18
CSSERA	81	FX1	3	PCUW0	75	TC	70
CS8042	77	FX1/FCLK1	4	PCVAL	11	TR00	32
DACK	47	HDL	28	PDREF	66	VBAT	62
DACKEN	51	HS	13	PRDY	71	VDD	5,44,67
DB0-DB7	35-42	IDEDENH	1	PROGCS	73	VSS	2,16,25,34,46,65
DCHG	10	IDEDENL	84	PWRDN	30	WD	15
DIRC	17	IDED7	43	RA8	56	WE	14
DMA	8	IDX	33	RA9	55	WP	31
DPH	52	IOR	48	RA10	54		
DPL	53	IOW	49	RCLR	58		
DRV/PS2	12	MO0	23	RDD	7		
DS0	19	MO1	24	RESET	57		

TABLE 2-4A. PIN ASSIGNMENTS (ALPHABETIC ORDER)

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	IDEDENH	22	DS3	43	IDED7	64	MX14
2	VSS	23	MO0	44	VDD	65	VSS
3	FX1	24	MO1	45	A0	66	PDREF
4	FX1	25	VSS	46	VSS	67	VDD
5	VDD	26	MO2	47	DACK	68	OSC
6	FCLK2	27	MO3	48	IOR	69	RTCIRQ
7	RDD	28	HDL	49	IOW	70	TC
8	DMA	29	RWC	50	CSEN	71	PRDY
9	FIRQ	30	PWRDN	51	DACKEN	72	EMS
10	DCHG	31	WP	52	DPH	73	PROGCS
11	PCVAL	32	TR00	53	DPL	74	PCUW1
12	DRV/PS2	33	IDX	54	RA10	75	PCUW0
13	HS	34	VSS	55	RA9	76	NPCS
14	WE	35	DB0	56	RA8	77	CS8042
15	WD	36	DB1	57	RESET	78	ROMOE
16	VSS	37	DB2	58	RCLR	79	CSPAR0
17	DIRC	38	DB3	59	BALE	80	CSSEPB
18	STEP	39	DB4	60	RTCX	81	CSSEPA
19	DS0	40	DB5	61	RTCX	82	CSIDE1
20	DS1	41	DB6	62	VBAT	83	CSIDE0
21	DS2	42	DB7	63	MX14	84	IDEDENL

TABLE 2-4B. PIN ASSIGNMENTS (NUMERIC ORDER)



1 Copyright Information

2 Part Number - Package Type
XX = UU (Low Profile 84 Lead PQFP
LU (Standard 84 Lead PQFP)
JU (PLCC)
GU (CLCC)

3 ROM Version-Test Bin Date
XX-XX = 06 (Current ROM Version)
02 (Current Passing Test Bin)

4 In-House Control Code

5 Proto-Type Indicator
PROTO indicates unreleased device

FIGURE 2-6. PLCC/PQFP PINOUT DIAGRAM

17

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
				Integrated Drive Electronics (IDE)
1	$\overline{\text{IDEDENH}}$	IDE High Byte Drive Enable	O	CMOS level output goes active low to enable the IDE Drive Interface Bus transceivers for the high byte of of the 16-bit interface. The signal is used with the $\overline{\text{CSIDE0}}$ card select oupt signal to the IDE drive only during 16-bit IDE data transfers.
43	IDED7	IDE Data Bit 7	I/O	TTL level I/O providing a data path for bit 7 between the Host and the IDE drive interface. IDED7 is an output, passing data to the IDE drive from DB7 of the Host data bus whenever an $\overline{\text{IOW}}$ to the IDE drive interface is detected. IDED7 is an input, passing data from the IDE drive to DB7 of the Host data bus whenever an $\overline{\text{IOR}}$ of the IDE drive interface is detected, except when reading from address 3F7H. During an $\overline{\text{IOR}}$ of 3F7H, the floppy DCHG status is output on the Host data bus pin DB7.
82	$\overline{\text{CSIDE1}}$	IDE Card Selected Aux. Registers	O	CMOS level output is used by the Host to address and communicate with the IDE drive auxiliary registers. Host activates the signal through a decode in the CSL logic block, while at the same time asserting IDEDENL.
83	$\overline{\text{CSIDE0}}$	IDE Card Selected Registers 0-7	O	CMOS level output is used by the Host to address and communicate with the IDE drive on the I/O channel. The Host activates the signal through a decode in the CSL logic block, while at the same time asserting IDEDENL or both IDEDENL and $\overline{\text{IDEDENH}}$.
84	$\overline{\text{IDEDENL}}$	IDE Low Byte Drive Enable	O	CMOS level output goes active low to enable the IDE drive interface bus transceivers for the high byte of the 16-bit Interface. The signal is used with the CSIDE0 card select output signal to the IDE drive only during 16-bit IDE data transfers.
				Host Interface
8	DMA	FDC DMA Request	O	DMA request for byte transfers of data. In PC/AT mode, this pin is tri-stated, enabled by DMAEN signal from the Operations Register.
45	AO	BIL Address Line	I	Address line selecting data (=1) or status (=0) information for the FDC. A0 = logic 0 during $\overline{\text{IOW}}$ is illegal except when putting the FDC into sleep mode.
47	$\overline{\text{DACK}}$	FDC DMA Acknowledge	I	Used by DMA controller to transfer data from FDC onto the bus. Logical equivalent to $\overline{\text{FDCS}}$ and A0=1. In PCAT mode, this signal is qualified by DMAEN from the Operations Register.

TABLE 2-5. PIN DESCRIPTIONS

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
				Host Interface, Continued
48	$\overline{IOR}$	BIL Input/Output Read	I	Read enable allowing data or status information to be transferred onto data bus by the WD76C20.
49	$\overline{IOW}$	BIL Input/Output Write	I	Write enable latching data from the bus into sub-system buffer registers.
57	$\overline{RESET}$	Chip Reset	I	TTL input resets the WD76C20 with the exception of the normal timekeeping operations which will remain uninterrupted. Resets all device outputs. Resets FDC controller, placing microsequencer in idle, and puts FDC in base mode, not PC/AT mode.
				Data To/From Floppy - Floppy Control
3	$\overline{FX1}$	FDC XTAL Output #1	I/O	This pin is an oscillator drive output for a 32 MHz resonant crystal. $\overline{FX1}$ should be left floating if a TTL level clock is used at pin FX1.
4	FX1	FDC XTAL Input #1	I	XTAL oscillator input requiring 32 MHz resonant crystal. This oscillator is used for all standard data rates, and may be driven with either a 32 MHz or 16 MHz TTL level signal instead of using the 32 MHz or 16 MHz crystal.
	FCLK1	FDC CLK Input #1	I	
6	FCLK2	FDC CLK Input #2	I	TTL level input used for non-standard data rates; can be driven with a 9.6 MHz clock for 300 Kbs MFM data rate and only be selected from the control register.
7	$\overline{RDD}$	FDC Read Disk	I	This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of the encoded data.
9	FIRQ	FDC Interrupt Request	O	Interrupt request indicating completion of command execution or data transfer requests (non-DMA mode). In PCAT mode, this pin is tri-stated, enabled by DMAEN signal from the Operations Register.
10	$\overline{DCHG}$	FDC Disk Changed	I	This Schmitt Trigger (ST) input senses status from the disk drive indicating active low and drive door is open or that the diskette has possibly changed since last drive selection. The pin has an internal pull-up register.
11	PCVAL	FDC Precompensation Value Select	I	This pin determines the amount of write precompensation used on the inner tracks of the diskette. Logic 1 = 125 ns, 0 = 187 ns. In the defeat option, the PCVAL input is a don't care, and internally the precomp value is disabled.

TABLE 2-5. PIN DESCRIPTIONS, continued

17

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		Data To/From Floppy - Floppy Control, Continued		
12	DRV PS2	FDC Drive Type FDC PS2 Drive Type	I O	In the input mode, a logic 0 indicates to the FDC that a 2-speed spindle motor is present and that FCLK2 should be grounded because it will not be used. As an option, this pin can be defined as an output to support the floppy drive connector pin 2 for PS/2 style drives, indicating the FDC is set internally for a single spindle motor. The pin has an internal pull-up resistor.
13	$\overline{HS}$	FDC Head Select	O	This high current driver (HCD) output selects the head, i.e., side, of the floppy disk that is being read or written. Logic 1 = side 0, logic 0 = side 1.
14	$\overline{WE}$	FDC Write Enable	O	This HCD output becomes true, active low, just prior to writing on the diskette. This allows current to flow through the write head.
15	$\overline{WD}$	FDC Write Data	O	This HCD is the write data output. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
17	$\overline{DIRC}$	FDC Stepper Direction	O	This HCD output determines the direction of head stepper motor. Logic 1 = outward motion, logic 0 = inward motion.
18	$\overline{STEP}$	FDC Stepper Step	O	This HCD output issues an active low pulse for each track to track movement of the head.
28	$\overline{HDL}$	FDC Head Load	O	This HCD output, when active low, causes the head to be loaded against the media in the selected drive.
29	$\overline{RWC}$ $\overline{RPM}$	FDC Reduce Write Current Revolutions Per Minute	O O	This HCD output, when active low, causes a reduced write current when bit density is increased toward the inner tracks, becoming active when tracks > 2. In PCAT mode, this signal can be used on 2-speed drives to select 300 RPM, active low, when 250 MFM or 125 FM KBs is selected and DRV = 0.
30	PWRDN	FDC Power Down	O	CMOS output, when active high, indicates the FDC portion of the WD76C20 has gone into power down mode. This signal can be used to power down the floppy drive if supported.
31	$\overline{WP}$	FDC Write Protected	I	This Schmitt Trigger (ST) input senses status from the disk drive indicating active low when a diskette is write protected.

TABLE 2-5. PIN DESCRIPTIONS, continued

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		Data To/From Floppy - Floppy Control, Continued		
32	$\overline{\text{TR00}}$	FDC Track Zero	I	This ST input senses status from the drive indicating active low, when the head is positioned over the outermost track, track 00.
33	$\overline{\text{IDX}}$	FDC Index Hole	I	This ST input senses status from the drive indicating active low when the head is positioned over the beginning of a track, marked by an index hole.
		Chip Select		
50	$\overline{\text{CSEN}}$	CSL Chip Select Enable	I	Chip Select Enable TTL input used to output enable the appropriate CSL control line as decoded from the RA8, RA9, RA10, DPL and DPH inputs. When DACKEN is asserted low, the function of $\overline{\text{CSEN}}$ is negated. When used to enable and disable the WD76C30 48 MHz clock, $\overline{\text{CSEN}}$ acts as a strobe to a latch. When it and DACKEN are both asserted, the TC output will go high.
51	DACKEN	CSL Dack Enabled	I	TTL input that indicates the host is performing a DMA transfer unrelated to the WD76C20. When active high, it is used to disqualify all CSL input lines.
52	DPH	CSL Address Parity High	I	Decoded chip select TTL input pad, bit CS4.
53	DPL	CSL Address Parity Low	I	Decoded chip select TLL input pad, bit CS3.
54	RA10	CSL Address Line 10	I	Decoded chip select TTL input pad, bit CS2.
55	RA9	CSL Address Line 9	I	Decoded chip select TTL input pad, bit CS1.
56	RA8	CSL Address Line 8	I	Decoded chip select TTL input pad, bit CS0.
58	BALE	CSL Bus ALE	I	TTL input which, when active high, causes latches on the CSL Input Code ($\overline{\text{CSEN}}$, DPH, DPL, RA10, RA9, RA8) to become transparent. When BALE is forced low, the data in the transparent latches is latched. This pin has an internal pull-up resistor so the pin can be left unconnected and the latches transparent.
70	TC	CSL Host Terminal Count	O	CMOS level output used to indicate the final count has been reached during a host DMA transfer unrelated to the WD76C20. It is also used internally by the FDC to indicate a DMA transfer to the floppy drive is complete. TC asserts high when both DACKEN and $\overline{\text{CSEN}}$ are asserted. (DACKEN=1, CSEN=0).

TABLE 2-5. PIN DESCRIPTIONS, continued

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
			Chip Select, Continued	
71	PRDY	CSL Processor Ready	I	ST input senses processor ready status to help latch the CSL inputs correctly during system byte swapping activities. This pin has an internal pull-up resistor so that it can be left unconnected when not needed. The PRDY input should be used in system designs that use the BALE pin.
72	$\overline{\text{EMS}}$	CSL External EMS Access	O	CMOS card select output decoded from CSL input lines and issued to select external EMS.
73	$\overline{\text{PROGCS}}$	CSL Program Chip Select	O	CMOS chip select output decoded from CSL input lines and issued as a programmable chip select.
74	PCUW1	CSL Power Control Unit Write Strobe #1	O	CMOS write strobe output decoded from CSL input lines and issued to write to the PCU #1.
75	PCUW0	CSL Power Control Unit Write Strobe #0	O	CMOS write strobe output decoded from CSL input lines and issued to write to the PCU #0.
76	$\overline{\text{NPCS}}$	CSL Numerical Processor Chip Select	O	CMOS chip select output decoded from CSL input lines and issued to select the numerical processor, the 80287.
77	$\overline{\text{CS8042}}$	CSL 8042 Chip Select	O	CMOS chip select output decoded from CSL input lines and issued to select the 8042.
78	$\overline{\text{ROMOE}}$	CSL ROM Output Enable	O	CMOS chip select output decoded from CSL input lines and issued to output enable the BIOS ROM.
79	$\overline{\text{CSPAR0}}$	CSL Parallel Port #0 Chip Select	O	CMOS chip select output decoded from CSL input lines and issued as a chip select to the WD76C30 to enable the parallel port #0.
80	$\overline{\text{CSSSEB}}$	CSL Serial Port B Chip Select	O	CMOS chip select output decoded from CSL input lines and issued as a chip select to the WD76C30 to enable the serial port B.
81	$\overline{\text{CSSERA}}$	CSL Serial Port A Chip Select	O	CMOS chip select output decoded from CSL input lines and issued as a chip select to the WD76C30 to enable the serial port A.
			Real Time Clock	
58	$\overline{\text{RCLR}}$	RTC RAM Clear	I	A dual function pin. As long as it is held low, all 76C20 outputs are held in a high impedance state to facilitate testing. It is also used as a ST input to clear all 114 bytes of the general purpose RAM. None of the clock or calendar functions are interrupted, and the 14 registers that are used by the RTC are left unchanged. This pin has an internal pull-up so it can be left unconnected.

TABLE 2-5. PIN DESCRIPTIONS, continued

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
			Real Time Clock, Continued	
60	$\overline{\text{RTCX}}$	RTC Time Base XTAL Out	O	XTAL oscillator output for parallel resonant AT cut crystal at 32.768 KHz.
61	RTCX	RTC Time Base XTAL In	I	32.768 KHz XTAL oscillator input for use with crystal oscillator circuit.
62	VBAT	RTC Battery Backup	NA	Battery backup power supply VDD pin. A 3-volt battery connector can be attached to maintain the RTC timekeeping functions and SRAM integrity during system power downs. (See Figure 2-3a)
69	$\overline{\text{RTCIRQ}}$	RTC Interrupt Request	O	Open-drain CMOS output that is set to tri-state unless the RTC needs to interrupt the processor, when the pin goes low and stays low until register C is read, or the part is reset through the RESET pin.
			Suspend/Resume Support	
63	MX14	S/R 14.318 MHz Crystal In	I	Crystal oscillator input for the 14.318 MHz oscillator.
64	$\overline{\text{MX14}}$	S/R 14.318 MHz Crystal Out	O	Crystal oscillator output for the 14.318 MHz oscillator.
66	PDREF	Suspend/Resume DRAM Refresh	O	External DRAM refresh line used to support the WD76C10 when it goes into Suspend/Resume mode. During Suspend/Resume mode, this pad provides a 1.0 µS ± 0.5 µS pulse once every 15.26 µS and is used to maintain the DRAM integrity with as little power as possible. Suspend/Resume mode is entered when a CSL address of 15H is detected and exited when a CSL address of 16H is issued.
68	OSC	S/R WD76C10 Clock Driver	O	CMOS level clock driver output used to support the WD76C10. When not in the WD76C10's suspend/ resume mode, the output waveform is a 14.318 MHz square wave, and when in suspend/resume mode, it becomes a 32.768 KHz square wave. The WD76C10 suspend/resume mode is entered when a CSL address of 15H is detected and exited when a CSL address of 16H is issued.
			Data Bus	
35-42	DB(0-7)	BIL Processor Data/Address Bus	I/O	8-bit bi-directional, tri-stateable data bus.

TABLE 2-5. PIN DESCRIPTIONS, continued

17

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
				Motor Control
23	$\overline{MO0}$	FDC Motor on #0	O	This HCD output, when active low, is motor on enable for disk drive #0, in PCAT mode.
24	$\overline{MO1}$	FDC Motor on #1	O	This HCD output, when active low, is motor on enable for disk drive #1, in PCAT mode.
26	$\overline{MO2}$	FDC Motor on #2	O	Reserved for 4 Mbyte support (density select).
27	$\overline{MO3}$	FDC Motor on #3	O	Reserved for 4 Mbyte support (density select).
				Drive Select
19	$\overline{DS0}$	FDC Drive Select #0	O	This HCD output, when active low, is Drive #0 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the MOEN0 bit.
20	$\overline{DS1}$	FDC Drive Select #1	O	This HCD output when active low is Drive #1 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the MOEN1 bit.
21	$\overline{DS2}$	FDC Drive Select #2	O	This HCD output, when active low, is Drive #2 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the MOEN2 bit.
22	$\overline{DS3}$	FDC Drive Select #3	O	This HCD output, when active low, is Drive #3 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the MOEN3 bit.
				Miscellaneous
2, 16, 25, 34, 46, 65		VSS		
5, 44, 67		VDD		

TABLE 2-5. PIN DESCRIPTIONS, continued

2.3 CHIP SELECT DECODE

The following codes are qualified by $\overline{CSEN}$ (Logic = 0) and disabled by DACKEN (Logic = 1).

CSL INPUT LINES						
CS#	DPH	DPL	RA10	RA9	RA8	FUNCTION
00H	0	0	0	0	0	Assert $\overline{ROMOE}$ to Output Enable the ROM BIOS[1]
01H	0	0	0	0	1	Assert $\overline{CS8042}$ to Chip Select the Keyboard Control[1]
02H	0	0	0	1	0	Assert $\overline{NPCS}$ to Chip Select the Numerical Processor[1]
03H	0	0	0	1	1	Assert PCUW0 to Write Strobe PCU #0
04H	0	0	1	0	0	Assert $\overline{LCLACK}$ to Acknowledge Keyboard Processor[1]
05H	0	0	1	0	1	Assert RTC ALE for RTC I/O[1]
06H	0	0	1	1	0	Assert RTC Write Strobe Gated by $\overline{CSEN}$ & $\overline{IOW}$[1]
07H	0	0	1	1	1	Assert RTC Read Stobe Gated by $\overline{CSEN}$ & $\overline{IOR}$[1]
08H	0	1	0	0	0	Assert FDC $\overline{LDOR}$ Register Select Line[1]
09H	0	1	0	0	1	Assert FDC $\overline{FDCS}$ Chip Select Line[1]
0AH	0	1	0	1	0	Assert FDC $\overline{LDCR}$ Register (Read/Write) Select Line[1]
0BH	0	1	0	1	1	Assert FDC $\overline{LDCR}$ Register (Read/Write) Select Line & assert $\overline{IDEDENL}$ and $\overline{CSIDE1}$ IDE Card Select Lines1
0CH	0	1	1	0	0	Assert $\overline{IDEDENL}$ and $\overline{CSIDE0}$ IDE Card Select Line & assert IDEDENH if A0 = 0[1]
0DH	0	1	1	0	1	Assert $\overline{IDEDENL}$ and $\overline{CSIDE1}$ IDE Card Select Line[1]
0EH	0	1	1	1	0	Assert $\overline{CSSERA}$ to Chip Select Serial Port A[1]
0FH	0	1	1	1	1	Assert $\overline{CSPAR0}$ to Chip Select Parallel Port 0[1]
10H	1	0	0	0	0	Assert $\overline{CSSERB}$ to Chip Select Serial Port B[1]
11H	1	0	0	0	1	Assert $\overline{PROGCS}$[1]
14H	1	0	1	0	0	Assert $\overline{EMS}$ to signify external EMS memory access[1]
15H	1	0	1	0	1	WD76C30 48 MHz Clk Disable , CSL Latches Code, In, so $\overline{CSSERA}$, $\overline{CSSERB}$ & $\overline{CSPAR0}$ stay asserted[2]
16H	1	0	1	1	0	48 MHz Clk Enable for WD76C30, CSL Un-Latches code, so $\overline{CSSERA}$, $\overline{CSSERB}$ & $\overline{CSPAR0}$ De-Assert[3]
17H	1	0	1	1	1	Assert PCUW1 to Write Strobe PCU #1

TABLE 2-6. CSL INPUT LINE DECODER

[1] These signals are generated using latched CSL inputs if BALE is used.
[2] Suspend Mode is entered by asserting code 15H on the CSL inputs, while qualifying it by $\overline{CSEN}$=0, $\overline{IOW}$=0, and the falling edge of OSC.
[3] Suspend Mode is left by asserting code 16H on the CSL inputs, while qualifying it by an OSC falling edge.

17

2.4 PIN STATES DURING POWER DOWN MODE

PIN NO.	SIGNAL NAME	INPUT/ OUTPUT	PD OPT1 IN	PD OPT1 OUT	PD OPT2 IN	PD OPT2 OUT	SUSPEND MODE IN	SUSPEND MODE OUT
1	$\overline{\text{IDEDENH}}$	OUTPUT		O		O		Z
2	VSS	VSS						
3	$\overline{\text{FX1}}$	OUTPUT		Z		Z		Z
4	FX1	INPUT	IH		IH		IH	
5	VDD	VDD						
6	FCLK2	INPUT	IH		IH		IH	
7	$\overline{\text{RDD}}$	SCH INPUT	IH		IH		IH	
8	DMA	BIDIRECT (input unused)	IH	Z***	IH	Z***	IH	Z
9	$\overline{\text{FIRQ}}$	BIDIRECT	IH	Z***	IH	Z***	IH	Z
10	$\overline{\text{DCHG}}$	SCH W/PULLUP	IH		IH		IH	
11	PCVAL	SCH INPUT	IH		IH		IH	
12	DRV	BIDIRECT SCH (W/PULLUP)	IH	Z	IH	Z	IH	Z
13	$\overline{\text{HS}}$	OUTPUT		Z		Z		Z
14	$\overline{\text{WE}}$	OUTPUT		Z		Z		Z
15	$\overline{\text{WD}}$	OUTPUT		Z		Z		Z
16	VSS	VSS						
17	$\overline{\text{DIRC}}$	OUTPUT		Z		Z		Z
18	$\overline{\text{STEP}}$	OUTPUT		Z		Z		Z
19	$\overline{\text{DS0}}$	OUTPUT		Z		Z		Z
20	$\overline{\text{DS1}}$	OUTPUT		Z		Z		Z
21	$\overline{\text{DS2}}$	OUTPUT		Z		Z		Z
22	$\overline{\text{DS3}}$	OUTPUT		Z		Z		Z
23	$\overline{\text{MO0}}$	OUTPUT		Z		Z		Z
24	$\overline{\text{MO1}}$	OUTPUT		Z		Z		Z
25	VSS	VSS						
26	$\overline{\text{MO2}}$	OUTPUT		Z		Z		Z
27	$\overline{\text{MO3}}$	OUTPUT		Z		Z		Z
28	$\overline{\text{HDL}}$	OUTPUT		Z		Z		Z
29	$\overline{\text{RWC}}$	OUTPUT		Z		Z		Z
30	PWRDN	OUTPUT		OH		OH		OH
31	$\overline{\text{WP}}$	INPUT	IH		IH		IH	

TABLE 2-7. PIN STATES DURING POWER DOWN MODES

PIN NO.	SIGNAL NAME	INPUT/ OUTPUT	PD OPT1 IN	PD OPT1 OUT	PD OPT2 IN	PD OPT2 OUT	SUSPEND MODE IN	SUSPEND MODE OUT
32	$\overline{TR00}$	INPUT	IH		IH		IH	
33	$\overline{IDX}$	INPUT	IH		IH		IH	
34	VSS	VSS						
35	*DB0	BIDIRECT	I	O	I	O	IH	Z
36	*DB1	BIDIRECT	I	O	I	O	IH	Z
37	*DB2	BIDIRECT	I	O	I	O	IH	Z
38	*DB3	BIDIRECT	I	O	I	O	IH	Z
39	*DB4	BIDIRECT	I	O	I	O	IH	Z
40	*DB5	BIDIRECT	I	O	I	O	IH	Z
41	*DB6	BIDIRECT	I	O	I	O	IH	Z
42	*DB7	BIDIRECT	I	O	I	O	IH	Z
43	IDED7	BIDIRECT	I	O	I	O	IH	Z
44	VDD	VDD						
45	A0	INPUT	I		I		IH	
46	VSS	VSS						
47	$\overline{DACK}$	INPUT	I		I		IH	
48	$\overline{IOR}$	INPUT	I		I		IH	
49	$\overline{IOW}$	INPUT	I		I		IH	
50	$\overline{CSEN}$	INPUT	I		I		I	
51	DACKEN	INPUT	I		I		I	
52	DPH	INPUT	I		I		I	
53	DPL	INPUT	I		I		I	
54	RA10	INPUT	I		I		I	
55	RA9	INPUT	I		I		I	
56	RA8	INPUT	I		I		I	
57	RESET	INPUT	I		I		I	
58	$\overline{RCLR}$	INPUT	I		I		IH	
59	BALE	INPUT W/PULLUP	I		I		IH	
60	$\overline{RTCX}$	OUTPUT		O		O		O
61	RTCX	INPUT	I		I		I	
62	VBAT	VDD						
63	MX14	INPUT	I		I		IH	
64	$\overline{MX14}$	OUTPUT		O		O		Z
65	VSS	VSS						

TABLE 2-7. PIN STATES DURING POWER DOWN MODES (Continued)

PIN NO.	SIGNAL NAME	INPUT/ OUTPUT	PD OPT1 IN	PD OPT1 OUT	PD OPT2 IN	PD OPT2 OUT	SUSPEND IN	MODE OUT
66	PDREF	OUTPUT		O		O		O
67	VDD	VDD						
68	OSC	OUTPUT		O		O		O
69	RTCIRQ	OUTPUT		O		O		O
70	TC	OUTPUT		O		O		O
71	PRDY	INPUT	I		I		IH	
72	$\overline{EMS}$	OUTPUT		O		O		Z
73	$\overline{PROGCS}$	OUTPUT		O		O		Z
74	PCUW1	OUTPUT		O		O		O
75	PCUW0	OUTPUT		O		O		O
76	$\overline{NPCS}$	OUTPUT		O		O		Z
77	$\overline{CS8042}$	OUTPUT		O		O		Z
78	$\overline{ROMOE}$	OUTPUT		O		O		Z
79	$\overline{CSPAR0}$	OUTPUT		O		O		O
80	$\overline{CSSERB}$	OUTPUT		O		O		O
81	$\overline{CSSERA}$	OUTPUT		O		O		O
82	$\overline{CSIDE1}$	OUTPUT		O		O		Z
83	$\overline{CSIDE0}$	OUTPUT		O		O		Z
84	$\overline{IDEDENL}$	OUTPUT		O		O		Z

TABLE 2-7. PIN STATES DURING POWER DOWN MODES (Continued)

NOTES:

IH = Input High, internally forced high

IL = Input Low, internally forced low

OH = Output High, internally forced high

Z = Output tri-stated; 1 = Input active; 0 = Output active

* DB is always powered down and Z-state unless chip access is in progress

** Bond option pad, not an additional pin

*** Z only if DMAEN = 0; 0 if DMAEN = 1

3.0 FUNCTIONAL DESCRIPTIONS

3.1 CONTROL REGISTER

($\overline{\text{LDCR}}$=0, $\overline{\text{IOW}}$=0) is a write only register used to set the transfer data rate and disable write precomp. The support logic latches the 3 LSB's of the data bus upon receiving $\overline{\text{LDCR}}$ and $\overline{\text{IOW}}$. These bits are used to select the desired data rate, which in turn controls the internal clock generation. Clock switchover is internally deglitched, allowing continuous operation after changing data rates. If the Control Register is not used, the data rate is governed by the supplied clock, or crystal, frequency and must be 64 times the desired MFM data rate. This implies a maximum frequency of 16 MHz for the data rate of 250 Kb/s and a maximum frequency of 32 MHz for the data rate of 500 Kb/sec, unless the Control Register is used as shown in Table 3-1 and 3-2. Switching this clock must be glitchless, or the device will need to be reset. For all non-standard transfer data rates, Table 3-3 should be used.

As an option, FDC also supports 150 Kb/sec FM data transfer rate. The Control Register is used to set the transfer data rate as shown in Table 3-3. FX1 (pin 10) of the part may be driven with a TTL level 9.6 MHz signal. With this setup, only 150 Kb/sec (FM) and 300 Kb/s (MFM) data transfer rates can be selected.

In PC/AT mode, precomp can be disabled by the use of the No Write Precomp (NWP) bit of the Control Register.

CR1	CR0	DRV	DATA RATE	COMMENTS	PC/ATRPM
0	0	X	500 K	MFM	1
0	0	X	250 K	FM	1
0	1	0	250 K	MFM	0
0	1	1	300 K	MFM (9.6 MHz)	0
1	0	X	250 K	MFM, RESET DEFAULT	0
1	0	X	125 K	FM, RESET DEFAULT	0
1	1	X	125 K	FM	0

TABLE 3-1. 16 MHZ FCLK1 CR1, CR0, DRV DATA RATE DECODER

CR1	CR0	DRV	DATA RATE	COMMENTS	PC/ATRPM
0	0	X	1 M	MFM	1
0	0	X	500 K	FM	1
0	1	0	500 K	MFM	0
0	1	1	300 K	MFM (9.6 MHz)	0
1	0	X	500 K	MFM, RESET DEFAULT	0
1	0	X	250 K	FM, RESET DEFAULT	0
1	1	X	250 K	FM	0

TABLE 3-2. 32 MHZ FX1/FCLK1 CR1,CR0,DRV DATA RATE DECODER

CR1	CR0	DRV	DATA RATE	COMMENTS	PC/AT RPM
0	0	X	300 K	MFM	1
0	0	X	150 K	FM	1

TABLE 3-3. 9.6 MHZ FCLK1 CR1, CR0, DRV DATA RATE DECODER

BiIT	SIGNAL NAME & FUNCTION	RESET CONDITION
0	DATA RATE 0 (CR0)	0
1	DATA RATE 1 (CR1)	0
2	NO WRITE PRECOMP (NWP)	0
3-7	RESERVED	NONE

TABLE 3-4. FDC CONTROL REGISTER, ADDR=3F7, PCAT MODE

3.2 OPERATIONS REGISTER

This register includes support logic that latches the data bus upon receiving $\overline{LDOR}$ and $\overline{IOW}$. It replaces the typical latched port seen in floppy subsystems used to control disk drive spindle motors and select desired drive.

DSEL1, DSEL0 - Encoded drive select bits are decoded in Table 3-5 and are valid only if in PC/AT mode.

DS1	DS0	DRIVE SELECT
0	0	$\overline{DS0}$ ACTIVE
0	1	$\overline{DS1}$ ACTIVE
1	0	$\overline{DS2}$ ACTIVE
1	1	$\overline{DS3}$ ACTIVE

TABLE 3-5. DRIVE SELECT DECODER

$\overline{SRST}$ - This is the Soft Reset bit which will reset the FDC when set to a logic level 0. After the Soft Reset has occurred, the bit itself will be reset to a logic 1.

DMAEN - Active in the PC/AT mode, this DMA Enable bit qualifies DMA and FIRQ outputs and $\overline{DACK}$ input.

MOEN3, MOEN2, MOEN1, MOEN0 - These Motor On Enable bits produce the inverted outputs $\overline{MO3}$, $\overline{MO2}$, $\overline{MO1}$ and $\overline{MO0}$ in PC/AT mode.

BIT	SIGNAL NAME & FUNCTION	RESET CONDITION
0	DRIVE SELECT (DSEL0)	0
1	DRIVE SELECT (DSEL1)	0
2	SOFT RESET ($\overline{SRST}$)	1
3	DMA ENABLE (DMAEN)	0
4	MOTOR ON ENABLE (MOEN0)	0
5	MOTOR ON ENABLE (MOEN1)	0
6	MOTOR ON ENABLE (MOEN2)	0
7	MOTOR ON ENABLE (MOEN3)	0

TABLE 3-6. OPERATIONS REGISTER, ADDR=3F2

3.3 MASTER STATUS REGISTER

In the WD76C20, the Master Status Register is a read/write register, where the read only register in the X765 FDC core is an 8-bit register that contains the status information of the FDC and may be accessed at any time. The new write register is called MSR1 and contains support for the power down mode 1 and the PS/2 drive type select. The user may write to this register to enable the power down mode (option 1), to disable user transparent power down mode (option 2), and to set up the PS/2 type drive configuration.

BIT	SIGNAL NAME & FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	POWER DOWN MODE1 (OPTION 1)	FF	0 (RSTB)	MSRCK
1	PD2ENAB2 DISABLE PDM (OPTION 2)	FF	1 (RSTB)	MSRCK
2	PSSEL0 PS2 DRIVE 0	FF	0 (RSTB)	MSRCK
3	PSSEL1 PS2 DRIVE 1	FF	0 (RSTB)	MSRCK
4-	PSSEL2 PS2 DRIVE 2	FF	0 (RSTB)	MSRCK
5	PSSEL3 PS2 DRIVE 3	FF	0 (RSTB)	MSRCK
6	CTST0 PDM3 OPTION 2 (Reserved)	FF	0 (RSTN)	MSRCK
7	CTST1 PDM3 OPTION 2 (Reserved)	FF	0 (RSTN)	MSRCK

TABLE 3-7A. MASTER STATUS REGISTER, ADDR=3F4, WRITE ONLY

Notes:
. PDM (Power Down Mode). If Option 1 set to PD2ENAB = Disable Power Down Mode 2.
[1] If DB0 is set to logic 1, the FDC will enter into user initiated PDM (Power Down Mode) immediately.
[2] If DB1 is set to logic 0, the FDC will disable the user transparent PDM Option 2; the hard reset enable enables
. the PDM Option 2.
[3] User transparent power down mode counter test.

BIT	NAME	SYMBOL	DESCRIPTION
DB0	FDD 0 BUSY	D0B	FDD number 0 is in Seek Mode. If any bit is set, FDC will not accept READ or WRITE commands.
DB1	FDD 1 BUSY	D1B	FDD number 1 is in Seek Mode. If any bit is set, FDC will not accept READ or WRITE commands.
DB2	FDD 2 BUSY	D2B	FDD number 2 is in Seek Mode. If any bit is set, FDC will not accept READ or WRITE commands.
DB3	FDD 3 BUSY	D3B	FDD number 3 is in Seek Mode. If any bit is set, FDC will not accept READ or WRITE commands.
DB4	FDC BUSY	CB	A READ or WRITE command is in progress. FDC will not accept any other command.
DB5	EXECUTION MODE	EXM	This bit is set only during Execution phase in non-DMA mode. When DB5 goes low, Execution phase has ended and Results Phase has started. It operates only during non-DMA mode of operation.
DB6	DATA INPUT	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO=1, then transfer is from Data Register to processor. If DIO=0, then transfer is from processor to Data Register.
DB7	REQUEST FOR MASTER	RQM	Indicates Data Register is ready to send or receive data to or from processor. Both DIO and RQM should be used to perform "handshaking" functions of "ready" and "direction" to the processor.

TABLE 3-7B. MASTER STATUS REGISTER, ADDR=3F4, READ ONLY

17

3.4 PS/2 SUPPORT

The WD76C20 supports up to four PS/2 type drives, and Table 3-8 summarizes the sequence details for PS/2 drive configuration setup by the FDC.

The Master Status Register (MSR) is used in a write mode to set the conditions for drive select and motor enable signals and also to have correct polarity on DRV/PS2 pin for PS/2 type of drives.

Table 3-8 shows the sequence to select the PS/2 type of drives and the polarity on DRV/PS2 pin which is tied to pin 2 on the floppy disk drive connector. Otherwise, if this register is not programmed for PS/2 configuration, the RWC/output from FDC should go to pin 2 of the floppy disk drive connector. The default is AT mode.

3.5 OVERRUN ERROR STATUS REPORTING

The WD76C20 has the capability to detect and flag data overruns during DMA operations. This situation may occur, as an example, when a floppy operation, DRAM refresh, and DMA channel 2 transfer occur simultaneously. Should a data overrun occur, D4 (OR) in Status Register 1 will be set.

Versions of the WD76C20 which contain this feature can be distinguished easily by reading RTC RAM location 66H after reset. If the device contains the overrun flag feature, the LSB location 66H will be a logic level 1. In these devices, 66H is read only.

SEQUENCE	CODE	REGISTER VALUE	DESCRIPTION	RWC	DRV
Step 1	3F4	00	Disable FDC sleep mode	X	X
Step 2	3F7	00	Select 500 Kb/s data rate and 3 1/2" 1.44 MB in AT mode	1	1[1]
Step 3	3F2	1C	Disable $\overline{SRST}$, enable $\overline{DS0}$, $\overline{MO0}$ and DMAEN bit of OP register	1	1
Step 4	3F4	04	Enable bit 2 of MSR and select PS2 drive0 (1.44 MB)	1	1[2]
Step 5	3F2	1C	Disable SRST, enable DS0, MO0 and DMAEN bit of OP register	1	0[3]
Step 6	3F4	08	Enable bit 3 of MSR and select	X	X[4]
Step 7	3F7	02	Select 250 Kb/s data rate and 3 1/2" 720 KB drive	0	0
Step 8	3F2	2D	Disable SRST, enable DS1, MO1 and DMAEN bit of OP register PSSEL1 (3 1/2" 720 KB)	0	1[5]

TABLE 3-8. PS/2 SUPPORT

Notes:

1 Default for $\overline{RWC}$ and DRV/PS2 is AT mode.

2 Since 500K data rate is selected, the PSSEL0 will select drive 0, and the system configuration for this should be set up for 3 1/2" and 1.44M PS/2 type of drive.

3 Operation Register will select drive 0 and motor 0.

4 Master Status Register will select PSSEL1.

5 Step 5 and 6 will select 250K data rate, the PSSEL1 will select drive 1, and the system configuration for this should be set up for 3 1/2" and 720 KB PS/2 type of drive.

3.6 REAL TIME CLOCK REGISTERS

Shown in Figure 3-1 is a memory map of the RTC SRAM and operational registers. Under normal operating conditions all of the registers may be written to or read from except the following:

- Registers C and D are Read Only.
- Bit 7 of register A is Read Only.
- The high order bit of the seconds byte is Read Only.

0	14 BYTES	00H
13		0DH
14	114 BYTES GENERAL PURPOSE RAM	0EH
102	VERSION NUMBER	66H
127		7FH

0	SECONDS	00H
1	SECONDS ALARM	01H
2	MINUTES	02H
3	MINUTES ALARM	03H
4	HOURS	04H
5	HOURS ALARM	05H
6	DAY OF THE WEEK	06H
7	DAY OF THE MONTH	07H
8	MONTH	08H
9	YEAR	09H
10	REGISTER A	0AH
11	REGISTER B	0BH
12	REGISTER C	0CH
13	REGISTER D/ID	0DH

FIGURE 3-1. RTC ADDRESS MAP

17

Writing the correct time to the RTC is accomplished by first programming the SET bit in register B to a logic 1, and the Data Mode bit (DM) of Register B to the appropriate level. Then the ten bytes representing the current time and alarm status can be loaded from the host into the RTC without a chance of internal bus contention by simply addressing the appropriate memory locations and performing a normal I/O write operation. After all ten timing bytes and the DM bit have been written to the RTC, the SET bit should be cleared. After this, the DM bit cannot be changed without re-initializing all ten registers. Table 3-9 shows the Binary and BCD formats of the time, calendar and alarm locations. When the 12 hour format is selected, the high order bit of the hours byte represents AM when it is a logic 0, and PM when it is a logic 1. Once a second, the ten bytes are updated and checked for alarm conditions. If a Host read of the time occurs during an update, the hours, minutes and seconds may not agree. Methods to avoid this possibility are covered later.

Alarms can be set to interrupt the Host in a variety of different ways, including intervals ranging from once a day to once a second. The method used to set the periodicity is to write don't care bytes (any value from C0 to FF) into the appropriate alarm registers. Therefore an alarm scheduled to interrupt the Host only once a day would have all alarm registers programmed to the proper values. An alarm scheduled to go off once an hour would have a don't care value in the hour register. One scheduled to go off every minute would have don't care values programmed into hours and minutes. And finally, an alarm will go off every second if all three registers are programmed to don't cares.

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE BINARY DATA MODE	BCD DATA MODE
00	SECONDS	0-59	00-3B	00-59
01	SECONDS ALARM	0-59	00-3B	00-59
02	MINUTES	0-59	00-3B	00-59
03	MINUTES ALARM	0-59	00-3B	00-59
04	HOURS - 12 HR MODE	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	HOURS - 24 HR MODE	0-23	00-17	00-23
05	HRS ALARM - 12 HR MODE	1-12	01-0C AM, 81-8C PM	01-12 AM 81-92 PM
	HRS ALARM - 24 HR MODE	0-23	00-17	00-23
06	DAY OF WEEK (SUNDAY=1)	1-7	01-17	01-17
07	DATE OF MONTH	1-31	01-1F	01-31
08	MONTH	1-12	01-0C	01-12
09	YEAR	0-99	00-63	00-99

TABLE 3-9. RTC DATA MODES

REGISTER A SELECT BITS RS3	RS2	RS1	RS0	PERIODIC INTERRUPT RATE
0	0	0	0	NONE
0	0	0	1	3.90625 mS
0	0	1	0	7.8125 mS
0	0	1	1	122.070 uS
0	1	0	0	244.141 uS
0	1	0	1	488.281 uS
0	1	1	0	976.5625 uS
0	1	1	1	1.953125 mS
1	0	0	0	3.90625 mS
1	0	0	1	7.8125 mS
1	0	1	0	15.625 mS
1	0	1	1	31.25 mS
1	1	0	0	62.5 mS
1	1	0	1	125 mS
1	1	1	0	250 mS
1	1	1	1	500 mS

TABLE 3-10. RTC PERIODIC INTERRUPT RATE DECODER

RS3, RS2, RS1 and RS0 are used to select the periodic interrupt rate as seen in the table above. Once the rate is selected, use the PIE bit to enable the interrupt. Functionally, these pins are decoded to choose which spot to tap on the divider chain to generate the interrupts.

DV2, DV1 and DV0 enable and disable the oscillator for use during product shipping. The code 010 will turn the oscillator on and start dividing.

UIP is the Update In Progress bit, which can be used by the Host to determine when updates are not going to occur. If the UIP bit is low, the Host can assume that a transfer is not going to happen for at least another 244 µS, during which time registers 0-9 are fully available. Writing a logic 1 to the SET bit inhibits any further updates and clears the UIP bit.

BIT	SIGNAL NAME & FUNCTION	RESET CONDITION
0	PERIODIC INTERRUPT RATE SELECT BIT 0 (RS0)	UNAFFECTED
1	PERIODIC INTERRUPT RATE SELECT BIT 1 (RS1)	UNAFFECTED
2	PERIODIC INTERRUPT RATE SELECT BIT 2 (RS2)	UNAFFECTED
3	PERIODIC INTERRUPT RATE SELECT BIT 3 (RS3)	UNAFFECTED
4	OSCILLATOR CONTROL BIT 0 (DV0)	UNAFFECTED
5	OSCILLATOR CONTROL BIT 1 (DV1)	UNAFFECTED
6	OSCILLATOR CONTROL BIT 2 (DV2)	UNAFFECTED
7	UPDATE IN PROGRESS (UIP)	UNAFFECTED

TABLE 3-11. RTC REGISTER A, BIT 7 IS READ ONLY

BIT	SIGNAL NAME & FUNCTION	RESET CONDITION
0	DAYLIGHT SAVINGS ENABLE (DSE)	UNAFFECTED
1	HOURS FORMAT (24/12)	UNAFFECTED
2	DATA MODE (DM)	UNAFFECTED
3	RESERVED	NONE
4	UPDATE ENDED INTERRUPT ENABLE (UIE)	0
5	ALARM INTERRUPT ENABLE (AIE)	0
6	PERIODIC INTERRUPT ENABLE (PIE)	0
7	WRITE TO REGISTERS 0-9 IN PROGRESS (SET)	UNAFFECTED

TABLE 3-12. RTC REGISTER B

DSE - This Daylight Savings Enable bit allows the RTC to perform the adjustments required to maintain daylight savings. On the first Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM, and on the last Sunday in October at 1:59:59 AM, it changes to 1:00:00 AM

24/12 - This control bit sets the time to a 24 hour format if set to a logic 1, and to a 12 hour AM, PM format if reset to 0.

DM - This DATA Mode control bit sets and indicates whether the time is stored in binary or BCD format. A logic 1 in the DM bit indicates binary, and a logic 0 indicates binary coded decimal data.

UIE - When the Update Interrupt Enable bit is set to logic 1, it enables a function that interrupts the Host whenever the Update Flag (UF) is set to 1.

AIE - When the Alarm Interrupt Enable bit is set to logic 1, it enables a function that interrupts the Host whenever the Alarm Flag (AF) is set to 1.

PIE - When the Periodic Interrupt Enable bit is set to logic 1, it enables a function that interrupts the Host whenever the Periodic Interrupt Flag (PF) is set to 1.

SET - When the SET bit is written to a logic 1, a write to registers 0-9 can proceed without the possibility of an update cycle occurring part way through.

UF - The Update Ended Interrupt Flag is set to logic 1 after, and reset to logic 0 during, each update cycle.

AF - The Alarm Interrupt Flag is set to logic 1 whenever an alarm condition is met, either through a timing match or don't care conditions. It is cleared by reading Register C or resetting the part.

PF - A read only bit, this Periodic Interrupt Flag is a logic 1 when the divider tap determined by the decoded RSX lines changes state. The bit is independent of the PIE bit, but the PIE bit still controls whether or not an $\overline{\text{RTCIRQ}}$ pulse is generated. The

BIT	SIGNAL NAME & FUNCTION	RESET CONDITION
0-3	RESERVED	NONE
4	UPDATE ENDED INTERRUPT FLAG (UF)	0
5	ALARM INTERRUPT FLAG (AF)	0
6	PERIODIC INTERRUPT FLAG (PF)	0
7	INTERRUPT REQUEST FLAG (IRQF)	0

TABLE 3-13. RTC REGISTER C, READ ONLY

BIT	SIGNAL NAME & FUNCTION	RESET CONDITION
0-3	REVISION ID CODE (ID0, ID1, ID2, ID3)	UNAFFECTED
4-6	RESERVED	NONE
7	VALID RAM AND TIME (VRT)	UNAFFECTED

TABLE 3-14. RTC REGISTER D, READ ONLY

bit is cleared by reading Register C or resetting the part.

IRQF -The Interrupt Request Flag is set to logic 1 whenever the RTC is issuing a Host service interrupt request. The Boolean equation for the flag is IRQF = PF·PIE + AF·AIE + UF·UIE.

ID3, ID2, ID1 and ID0 - used to indicate the device ID code, which exists to identify the chip during board level testing.

VRT - Valid RAM and Time is a read only bit used by the RTC to indicate the possibility of a corruption of the SRAM memory locations. A logic 0 would indicate an interrupt in the power, during which sufficient voltage was not provided by either VBAT or VDD.

3.7 FDC FUNCTIONAL MODE SELECT

PCAT and Test Modes - Each of these modes allow subtle differences which the user may find desirable. Note, the Control Register may be used in any mode without altering functionality.

PCAT Mode

For PCAT compatibility, users will write to the Operations Register after a hardware reset.

FDC Power Down Mode Option 1 - The WD76C20 should enter in Power Down Mode Option 1 when bit 0 of MSR1 register (OPT1) is set to logical 1 and the following conditions are met:

- The PD bit of the MSR1 write only register is set to logic 1
- The RST pin to FDC is inactive
- The bit 2 of Operations Register $\overline{\text{SRST}}$=1
- FDC is waiting command from Host

The FDC will return from Power Down Mode Option 1 when the WD76C20 RESET is active and the FDC is reset. This will also reset bit 0 of MSR1 register to logic 0. The XTAL oscillator will turn on automatically once the chip is reset, but may need 20 mSecs to stabilize. The FDC standby current during the mode is maximum 100 uA. During this time through the normal Master Status register protocol the "request for master" (RQM) bit 7 in the MSR will be inactive. (ROM bit indicates that data register is ready to send or receive data to or from the processor). The FDC can also be brought out from Power Down Mode.

When exiting power down mode option 1, a soft reset assures that an internal reset is generated and the reset is active long enough for the internal clocks and oscillator to start cleanly. If the mode is ever exited by merely writing to the MSR, then it is recommended that a soft reset be issued and a timeout be instituted to allow the oscillator to stabilize (20 msec). The soft reset can be released after this stabilization wait period.

17

FDC Power Down Mode Option 2 - This is a user transparent power down mode. The FDC has been designed to enter in Power Down Mode automatically 500 ms after the beginning of IDLE state (based on the 500 Kb/s data rate). During this time the XTAL oscillator, all the internal clocks, drive interface signals and all the interface signals to FDC will be shut off. The Host interface path to FDC will be active during this time. For low power consumption, the Host interface signals should be held to DC logic levels 1 or 0.

The FDC will come out from PDM by any Host access to FDC. The XTAL oscillator will turn on automatically and need at least 20 ms for oscillator to stabilize and during this time bit 7 of Master Status Register will be logic = 0. Once the Bit 7 of the MSR is set to logic 1, the FDC will be ready to receive any command from Host. During power down mode, the contents of FDC registers will not be affected, and FDC will come up in the same mode as it was before it entered into PDM. The power down mode can be disabled by writing a logic 0 in Bit 1 of the MSR. The default is power down mode enabled all the time after hard reset or chip power up.

Chip Set Power Down

The following denotes I/O status during three different power down options:

- **#1 - FDC Core and Disk Interface I/O Only**
  - During this power down mode, all the input signals to floppy core, except RESET, are shut off. All the floppy disk interface input and output pins are either disabled or tristated.
  - The WD76C20 Host interface input and output pins not related to FDC core are left unaffected by this mode.
  - All the analog circuitry, the XTAL oscillator and clock internal to FDC are shut off.
- **#2 - FDC Core and Disk Interface I/O Only**
  - This is a user transparent power down mode for FDC core and all the FDC disk interface pins. The Host interface to and from FDC core and WD76C20 pins is not affected by this power down mode.
  - All the analog circuitry, the XTAL oscillator and clock internal to FDC are shut off.
- **#3 - WD7600 Core Chip Set Power Down Mode**
  - For FDC core, this mode is exactly the same as Option #2.
  - Only signals which must be active in suspend mode remain active. All other pins are shut off, disabled or tristated.

Device Reset

When asserted, the $\overline{\text{RESET}}$ pin causes the WD76C20 to perform a a hardware reset on the entire chip, including all the subsystems. The FDC supports both a hardware reset pin, $\overline{\text{RESET}}$, and software reset, SRST, through use of the Operations Register. The $\overline{\text{RESET}}$ pin will cause a device reset for the active duration. Default selects 500K MFM (or 250 K FM code dependent) as the data rate (32 MHz input clock). SRST also causes a reset condition for the active duration which will reset the microcontroller as did the $\overline{\text{RESET}}$, but will NOT affect the current data rate selection or the Mode. When both $\overline{\text{RESET}}$ and SRST are active, the high current driver outputs to the disk drive will be disabled.

If the XTAL oscillator is used, instead of the TTL driven clock inputs, the hardware $\overline{\text{RESET}}$ active time requirement will be extended. The oscillator circuit is designed so $\overline{\text{RESET}}$ will bootstrap the circuit into guaranteed oscillation in a fixed amount of time. The extended reset time allows the growth of the oscillation to produce stable internal clock timing.

Within the RTC, neither the clock, calendar, nor SRAM are affected by the hardware reset function. On powerup, the $\overline{\text{RESET}}$ pin must be held low for at least 200 ms to allow the power supply to stabilize. Some Control Register bits have affected reset conditions as shown in Tables 3-10 to 3-13.

4.0 SPECIFICATIONS

4.1 OPERATIONAL

Absolute Maximum Ratings - All voltages referenced to VSS

VCC . . . . . 7.0 Vol

Voltage at any pin . . . . . + 0.3 Volts

Storage Temperature . . -55 ° to +150 ° C

Operating Temperature . 0° to +70° C

TA = 0°C (32°F) to 70°C (158°F)

VCC = 5V = ± 10%

CL = 100 pf

VIL/VOL referenced to 0.8V

VIH/VOH referenced to 2.0V

CY specifies FX1 period

MCY specifies MCLK period, dependent on selected data rate

WCY specifies WCLK period, dependent on selected data rate.

4.2 INTERFACE TIMING

AC Chacteristics

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
VCC	+5V Supply	4.5	5.5	V
VBAT	Battery Backup Voltage	2.6	VDD	V
VIL	Input Low Voltage - Data Bus & XTOCS		0.8	V
VIH	Input High Voltage - Data Bus & XTOCS	2.0		V
VILT	Input Low Threshold - Schmitt Trigger	0.8	1.1	V
VIHT	Input High Threshold - Schmitt Trigger	1.7	2.0	V
VHYS	Schmitt Trigger Hysteresis	0.45		V
VOLAT	Output Low - DBus, FIRQ, DMA; IO=12.0 mA		0.4	V
VOHAT	Output High - DBus, FIRQ, DMA; IO= -5.0 mA	2.8		V
VOLHC	Output Low - Drive Interface IO=48 mA		0.4	V
VOL	Output Low - All Others; IO=4.0 mA		0.4	V
VOH	Output High - All Others; IO=400 uA	2.8		V
ILUL	Latch Up Current Low	40		mA
ILUH	Latch Up Current High	-40		mA
ILL	Leakage Current Low		10	uA
ILH	Leakage Current High		-10	uA
ICC	Supply Current - 100 uA source loads		70	mA
ICC	Supply Current - 5 mA source loads		140	mA
ICCPDM1	Supply current in power down mode[1] (Option 1)		200	uA
ICCPDM2	Supply current in power down mode[1] (Option 2)		2	mA
ICCPDM3	Supply current in chip set power down mode		200	uA
ICCBAT	Supply current in battery backup mode[1]		50	uA
PD	Power Dissipation - ICC max[3]		700	mW
PDHL	Power Dissipation - ICCHL max[2 3]		850	mW

TABLE 4-A. DC CHARACTERISTICS

[1] Vin = VCC or GND, IO=0 mA
[2] Includes DBx; IO=-5.0 mA source loads
[3] Includes open drain high current drivers at Vol=0.4V

17

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSS	CSL Input Address[1] Set Up to $\overline{IOR}$ Low	35		ns
pwRR	$\overline{IOR}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOR}$ High	10		ns
tRD	Data Access Time from $\overline{IOR}$ Low		175	ns
tDF	DB to Float Delay from $\overline{IOR}$ High	10	80	ns
tRI	FIRQ Reset Delay Time from $\overline{IOR}$ High		1MCY	+150 ns

TABLE 4-1. FDC READ TIMING SPECFICIATION

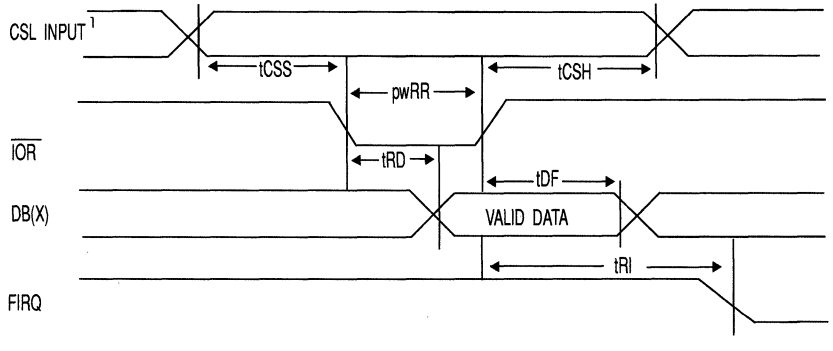


FIGURE 4-1. FDC READ TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOR}$ Low	35		ns
pwRR	$\overline{IOR}$ Pulse Width	180		ns
tRHAH	$\overline{IOR}$ High to BALE High	10		ns
tRD	Data Access Time from $\overline{IOR}$ Low		175	ns
tDF	DB(x) to Float Delay from $\overline{IOR}$ High	10	80	ns
tRI	FIRQ Reset Delay Time from $\overline{IOR}$ High		1 MCY+150	ns

TABLE 4-2. FDC READ W/BALE TIMING SPECIFICATION

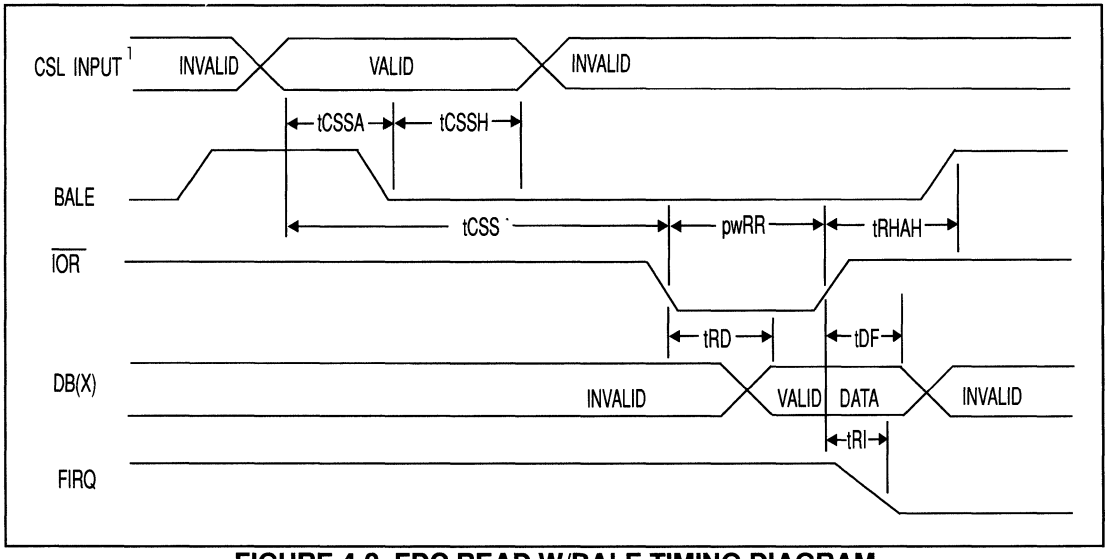


FIGURE 4-2. FDC READ W/BALE TIMING DIAGRAM

17

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSS	CSL Input Address[1] Set Up to $\overline{IOW}$ Low	35		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOW}$ High	10		ns
tDW	Data Set Up Time to $\overline{IOW}$ High	100		ns
tWD	Data Hold Time from $\overline{IOW}$ High	10		ns
tWI	FIRQ Reset Delay from $\overline{IOW}$ High		1MCY + 150ns	

TABLE 4-3. FDC WRITE TIMING SPECIFICATION

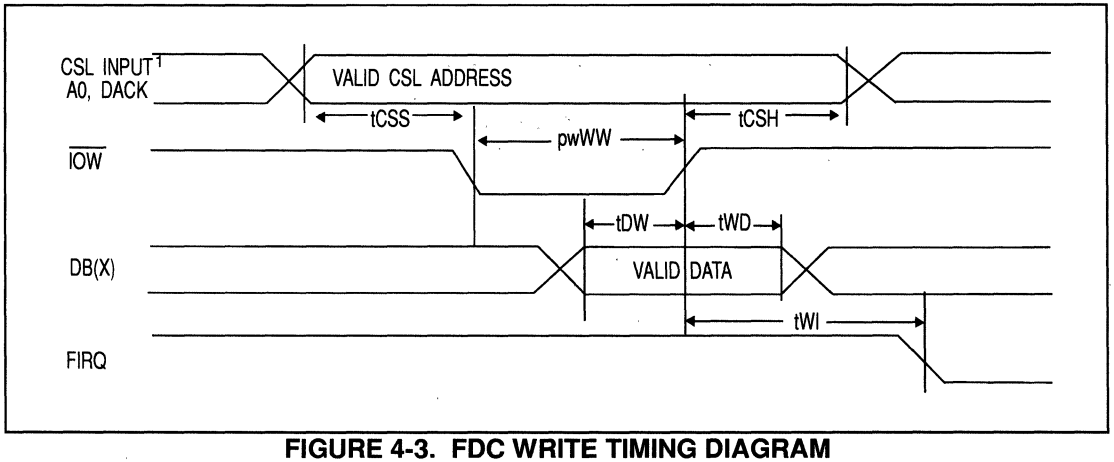


FIGURE 4-3. FDC WRITE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IO}$ Low	35		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tWHAH	$\overline{IOW}$ High to BALE High	10		ns
tDW	Data Set Up Time to $\overline{IOW}$ High	100		ns
tWD	Data Hold Time from $\overline{IOW}$ High	10		ns
tWI	FIRQ Reset Delay from $\overline{IOW}$ High		1 MCY+150ns	

TABLE 4-4. FDC WRITE W/BALE TIMING SPECIFICATION

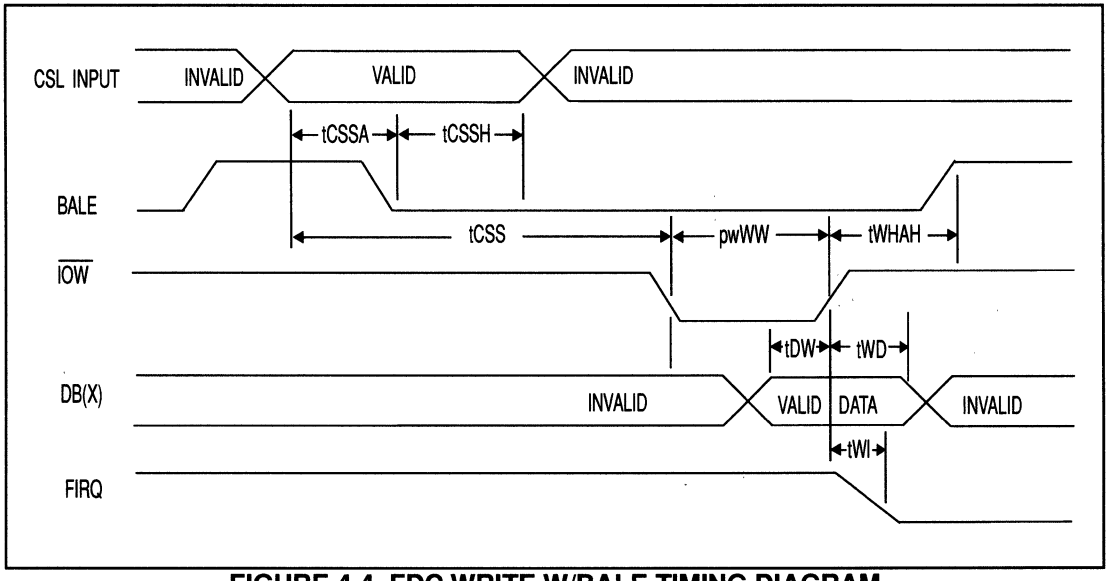


FIGURE 4-4. FDC WRITE W/BALE TIMING DIAGRAM

17

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tMCY	DMA Cycle Time	52		MCY
tMA	$\overline{DACK}$ Delay Time from DMA High	0		ns
tAM	DMA Reset Delay Time from $\overline{DACK}$ Low		140	ns
tAA	$\overline{DACK}$ Width	125		ns
tMRW	$\overline{IOR}$ or $\overline{IOW}$ Response from DMA High		48	MCY
tMtMR	$\overline{IOR}$ Delay from DMA	0		ns
tMW	$\overline{IOW}$ Delay from DMA	0		ns
tRD	Data Access Time from $\overline{IOR}$ Low		120	ns
tDW	Data Set Up Time to $\overline{IOW}$ High	100		ns
tDF	DB to Float Delay from $\overline{IOR}$ High	10	80	ns
tWD	Data Hold Time from $\overline{IOW}$ High	10		ns

TABLE 4-5. FDC DMA TIMING SPECIFICATION

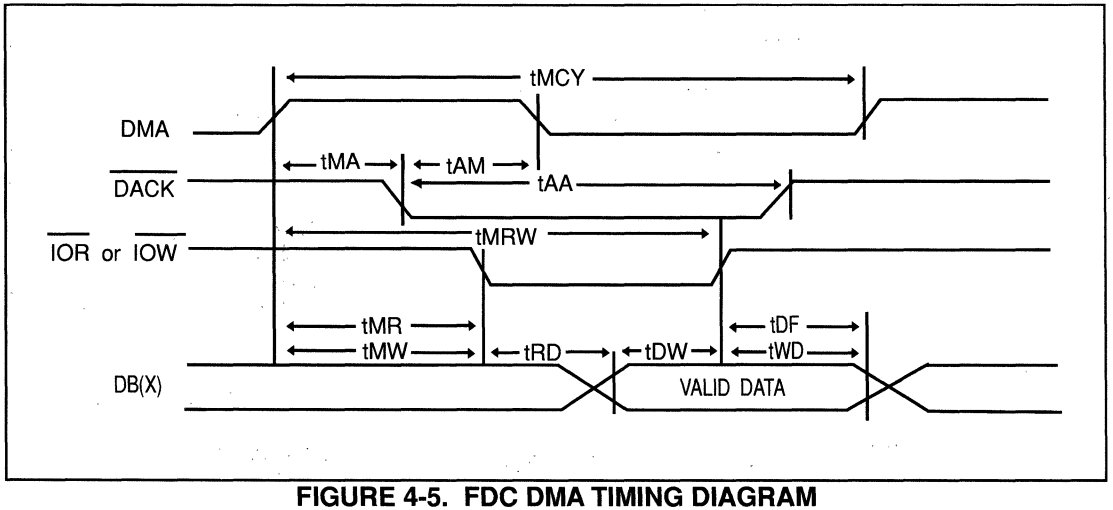


FIGURE 4-5. FDC DMA TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tTCR	DACKEN, $\overline{CSEN}$ Delay from Last DMA or FIRQ, $\overline{IOR}$	0	192	MCY
tTCW	DACKEN, $\overline{CSEN}$ Delay from Last DMA or FIRQ, $\overline{IOW}$	0	384	MCY
tTC	DACKEN High, $\overline{CSEN}$ Low Pulse Width	60		ns
tTCA	DACKEN High, $\overline{CSEN}$ Low to TC Asserted	0	30	ns
tTCD	DACKEN Low, $\overline{CSEN}$ High to TC De-Asserted	0	30	ns

TABLE 4-6. FDC TERMINAL COUNT TIMING SPECIFICATION

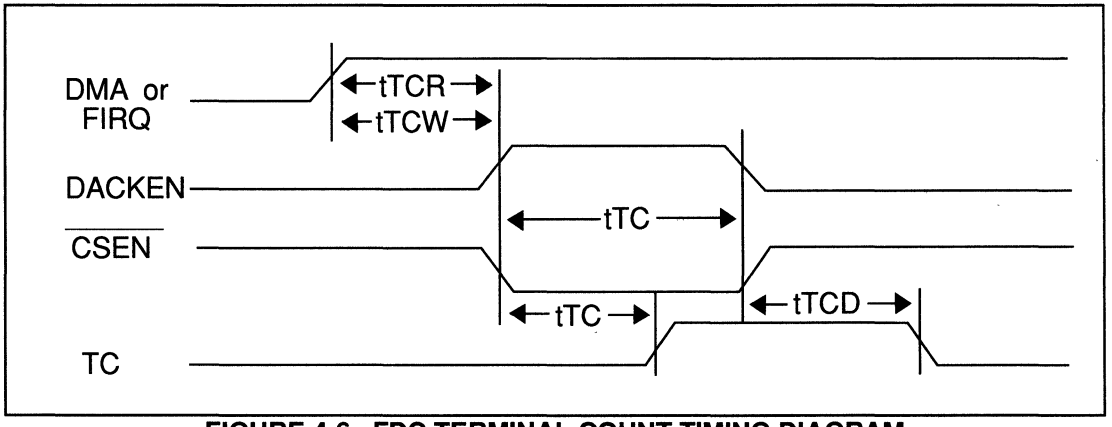


FIGURE 4-6. FDC TERMINAL COUNT TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCY	Clock Period	31		ns
tR	Clock Rise Time		2	ns
tF	Clock Fall Time		2	ns
tPH	Clock Active (High or Low)	13		ns

TABLE 4-7. FDC 32 MHZ CLOCK TIMING SPECIFICATION

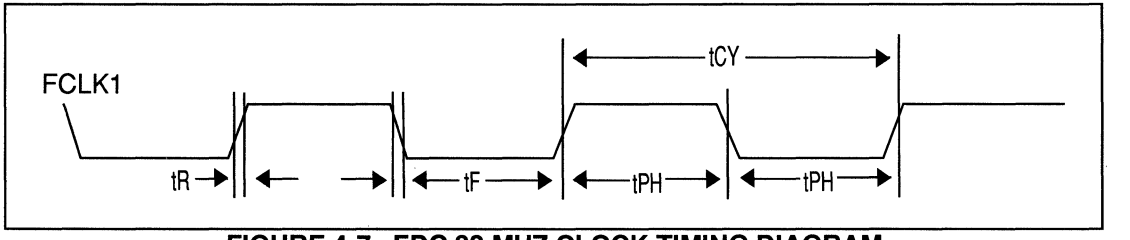


FIGURE 4-7. FDC 32 MHZ CLOCK TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tDST	$\overline{\text{DIRC}}$ Set Up to $\overline{\text{STEP}}$ Low	4		MCY
tSTP	STEP Active Time Low	24		MCY
tSTD	DIRC Hold Time from STEP High	96		MCY
tSC	STEP Cycle Time	132		MCY
tSTU	DS(x) Hold Time from STEP Low	20		MCY
tIDX	IDX Index Pulse Width	1		MCY
tRDD	RDD Active Time Low	40		ns
tWDD	WD Write Data Width Low	1/2		WCY

TABLE 4-8. FDC DISK DRIVE TIMING SPECIFICATION

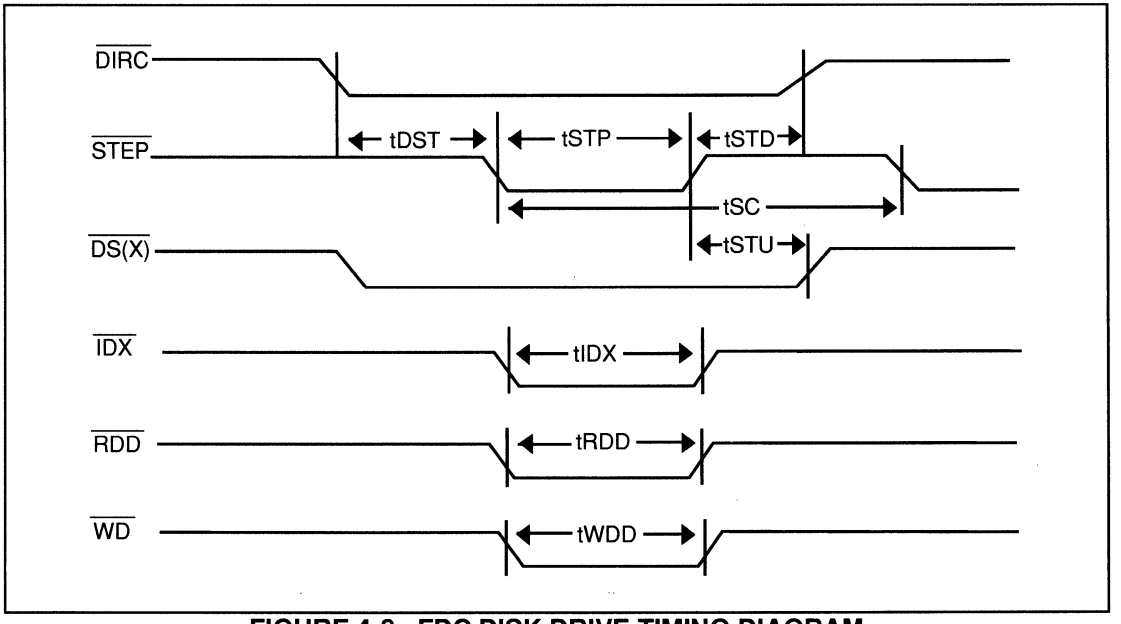


FIGURE 4-8. FDC DISK DRIVE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle $\overline{IOW}$ Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle $\overline{IOW}$ or $\overline{IOR}$ Low (not shown)	100		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOR}$ Low	35		ns
pwRS	$\overline{IOR}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOR}$ High	10		ns
tDDR	Data Access Time from $\overline{IOR}$ Low		175	ns
tDHR	DB to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 4-9. RTC AND RAM READ TIMING SPECIFICATION

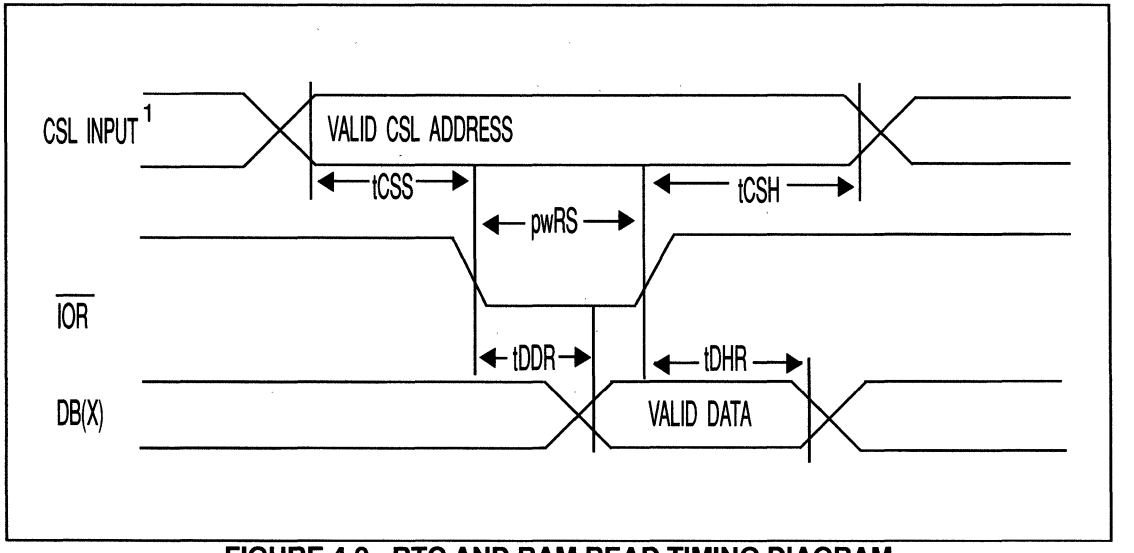


FIGURE 4-9. RTC AND RAM READ TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle $\overline{IOW}$ Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle $\overline{IOW}$ or $\overline{IOR}$ Low (not shown)	100		ns
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tcSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOW}$ Low	35		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tWHAH	$\overline{IOW}$ High to BALE High	10		ns
tDSW	Address or Data Setup Time to $\overline{IOW}$ High	100		ns
tDHW	Address or Data Hold Time from $\overline{IOW}$ High	10		ns

TABLE 4-10. RTC AND RAM WRITE W/BALE TIMING SPECIFICATION

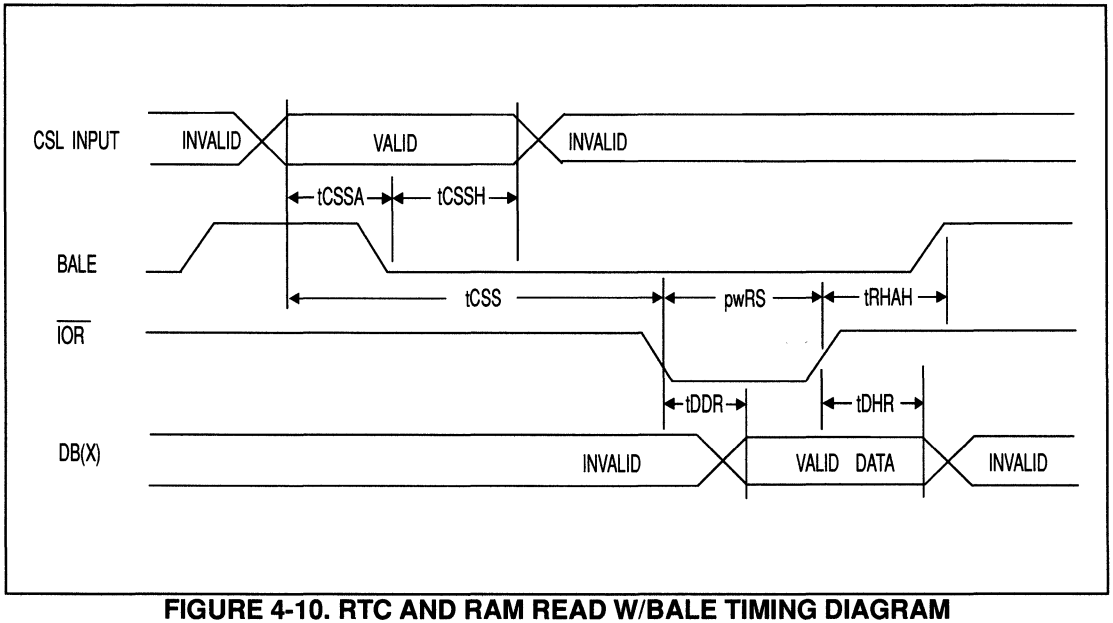


FIGURE 4-10. RTC AND RAM READ W/BALE TIMING DIAGRAM

17

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle $\overline{IOW}$ Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle $\overline{IOW}$ or $\overline{IOR}$ Low (not shown)	100		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOW}$ Low	30		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOW}$ High	10		ns
tDSW	Address or Data Set Up Time to $\overline{IOW}$ High	100		ns
tDHW	Address or Data Hold Time from $\overline{IOW}$ High	10		ns

TABLE 4-11. RTC AND RAM WRITE TIMING SPECIFICATION

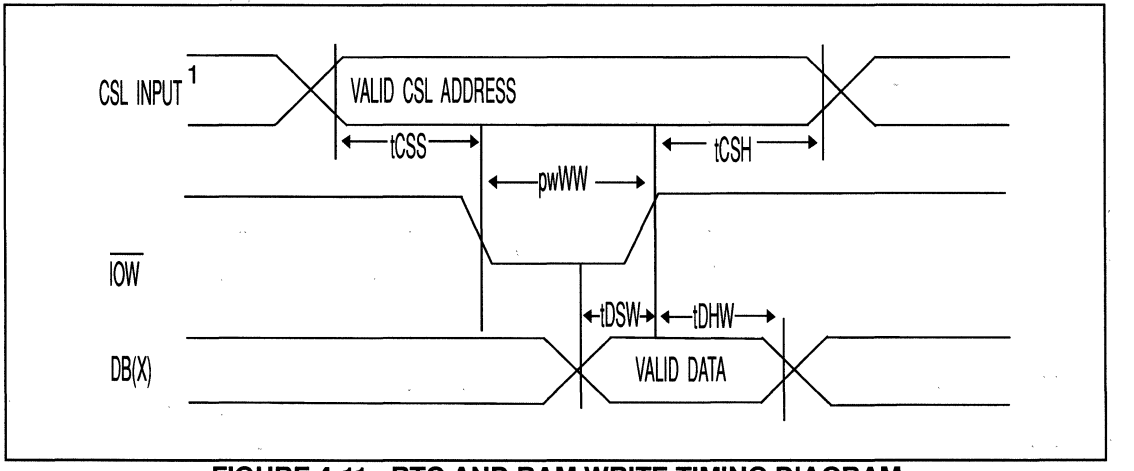


FIGURE 4-11. RTC AND RAM WRITE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle $\overline{IOW}$ Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle $\overline{IOW}$ or $\overline{IOR}$ Low (not shown)	100		ns
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tcSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IO}$ Low	30		ns
pwRS	$\overline{IOR}$ Pulse Width	180		ns
tRHAH	$\overline{IOR}$ High to BALE High	10		ns
tDDR	Data Access Time from $\overline{IOR}$ Low		175	ns
tDHR	DB(x) to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 4-12. RTC AND RAM READ W/BALE TIMING SPECIFICATION

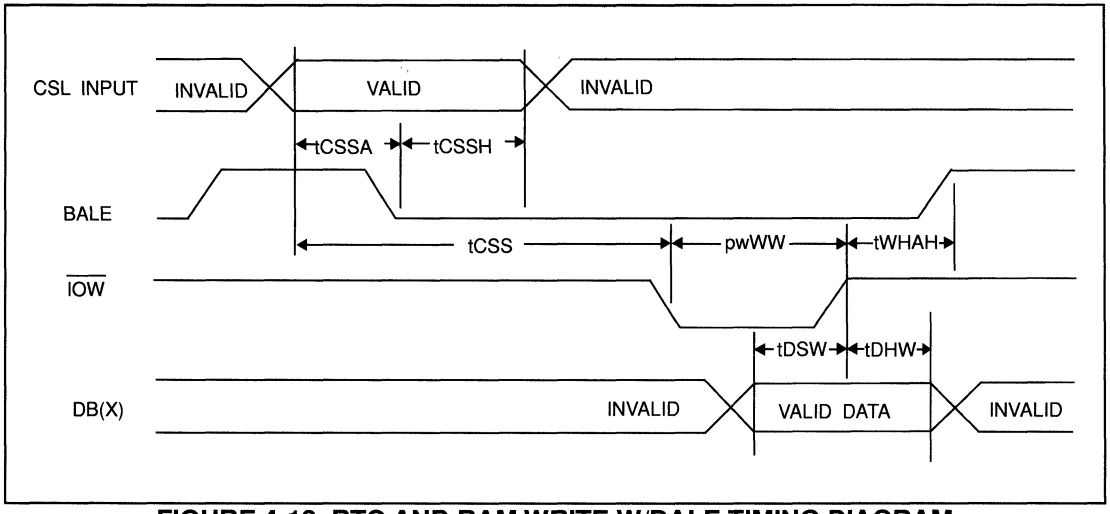


FIGURE 4-12. RTC AND RAM WRITE W/BALE TIMING DIAGRAM

17

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tRLIQ	$\overline{\text{RTCIRQ}}$ Release from $\overline{\text{IOR}}$ (Qualified by RECS)		2	µS
tRLIH	$\overline{\text{RTCIRQ}}$ Release from $\overline{\text{RESET}}$		2	µS

TABLE 4-13. RTCIRQ RELEASE TIMING SPECIFICATION

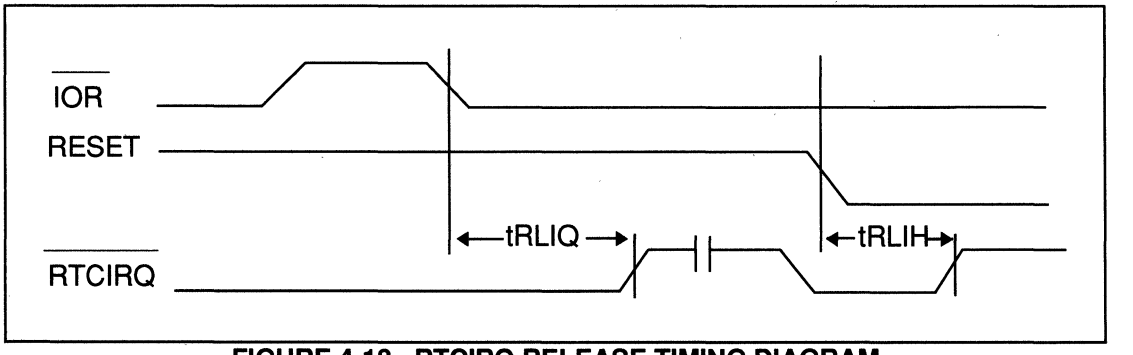


FIGURE 4-13. RTCIRQ RELEASE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tPRST	Power on Reset Width	200		ns
tRST	Reset Width	5		µS
tCA	Chip Access Delay from $\overline{\text{RESET}}$ High	32		MCY

TABLE 4-14. RESET TIMING SPECIFICATION

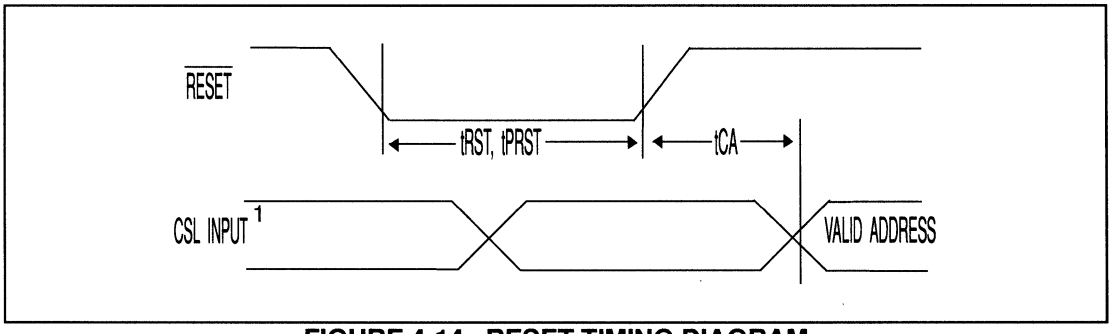


FIGURE 4-14. RESET TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSA	CSL Input Valid to CSL Output Asserted		35	ns
tCSD	CSL Input Invalid to CSL Output De-Asserted		35	ns
tD7DR	D7 Access time from $\overline{IOR}$ low	0	20	ns
tD7D	Propagation Delay from IDED7 to DB7	0	20	ns
tD7HR	DB7 to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 4-15. IDE INTERFACE TIMING (IDED7 TO DB7)

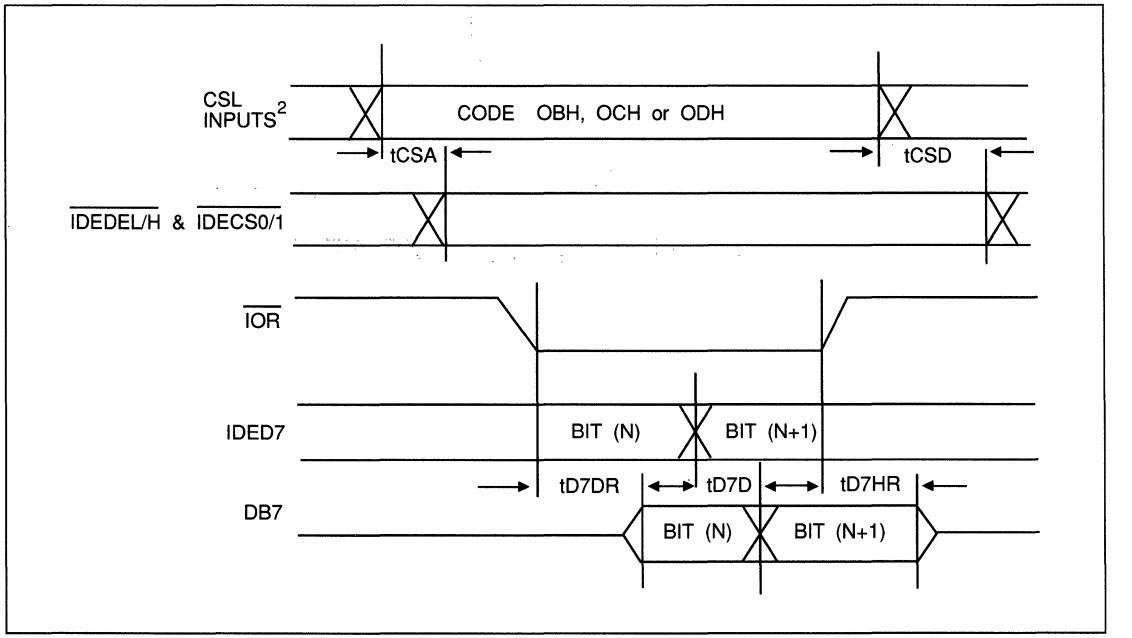


FIGURE 4-15. IDE INTERFACE TIMING DIAGRAM (IDED7 TO DB7)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IO}$ Low	30		ns
tRHAH	$\overline{IOR}$ High to BALE High	10		ns
tD7DR	D7 Access Time from $\overline{IOR}$ Low	0	20	ns
tD7D	Propagation Delay from IDED7 to DB7	0	20	ns
tD7HR	DB7 to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 4-16. IDE INTERFACE W/BALE TIMING (IDED7 TO DB7)

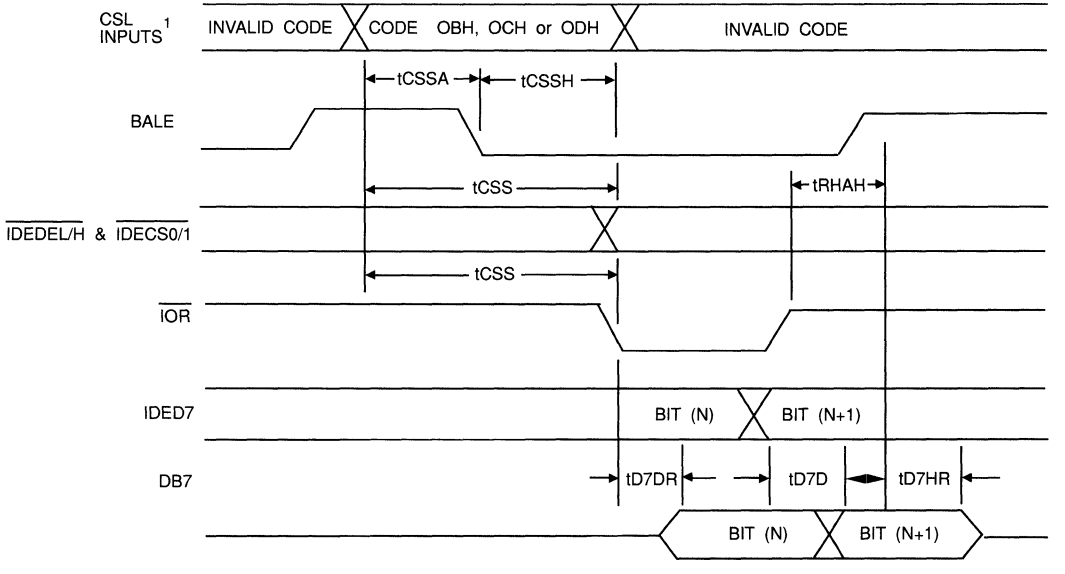


FIGURE 4-16. IDE INTERFACE W/BALE TIMING (IDED7 to DB7)

17

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSA	CSL Input Valid to CSL Output Asserted		35	ns
tCSD	CSL Input Invalid to CSL Output De-Asserted		35	ns
tIDDR	IDED7 Access time from $\overline{IOW}$ low	0	20	ns
tIDD	Propagation Delay from DB7 to IDED7	0	40	ns
tIDHR	IDED7 to Float Delay from $\overline{IOR}$ high	20	160	ns

TABLE 4-17. IDE INTERFACE TIMING (DB7 TO IDED7)

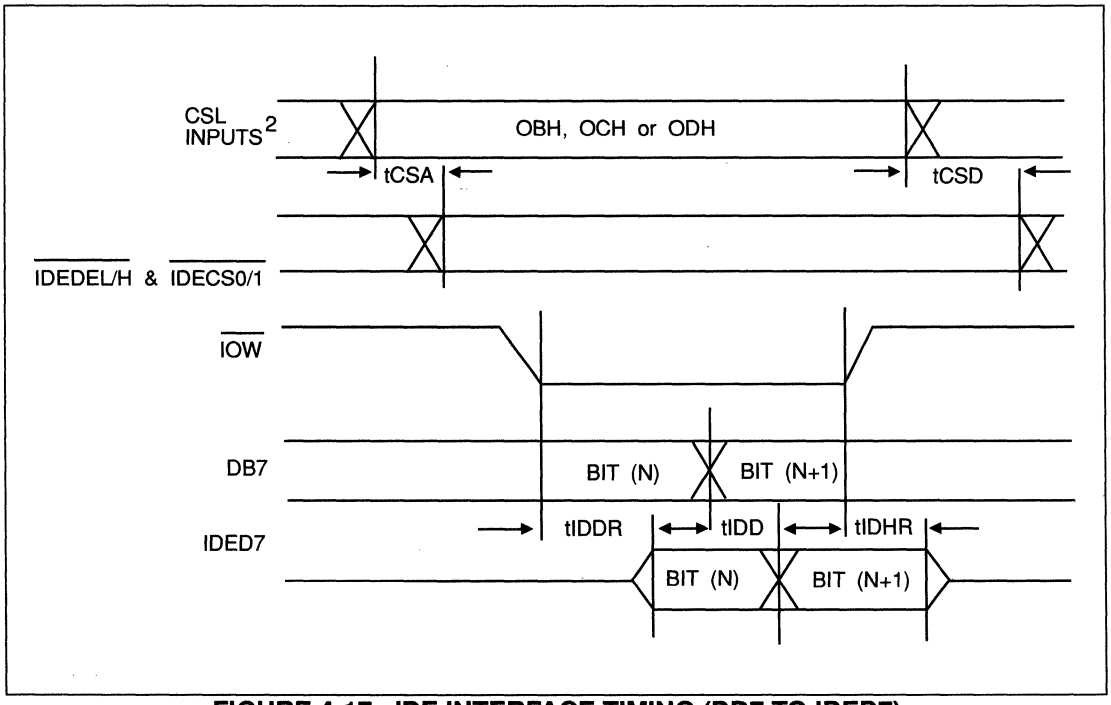


FIGURE 4-17. IDE INTERFACE TIMING (DB7 TO IDED7)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time From BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IO}$ Low	30		ns
tWHAH	$\overline{IOW}$ High to BALE High	10		ns
tIDDR	IDED7 Access time from $\overline{IOW}$ Low	0	20	ns
tIDHR	IDED7 to Float Delay from $\overline{IOR}$ High	20	160	ns

TABLE 4-18. IDE INTERFACE W/BALE TIMING (DB7 TO IDED7)

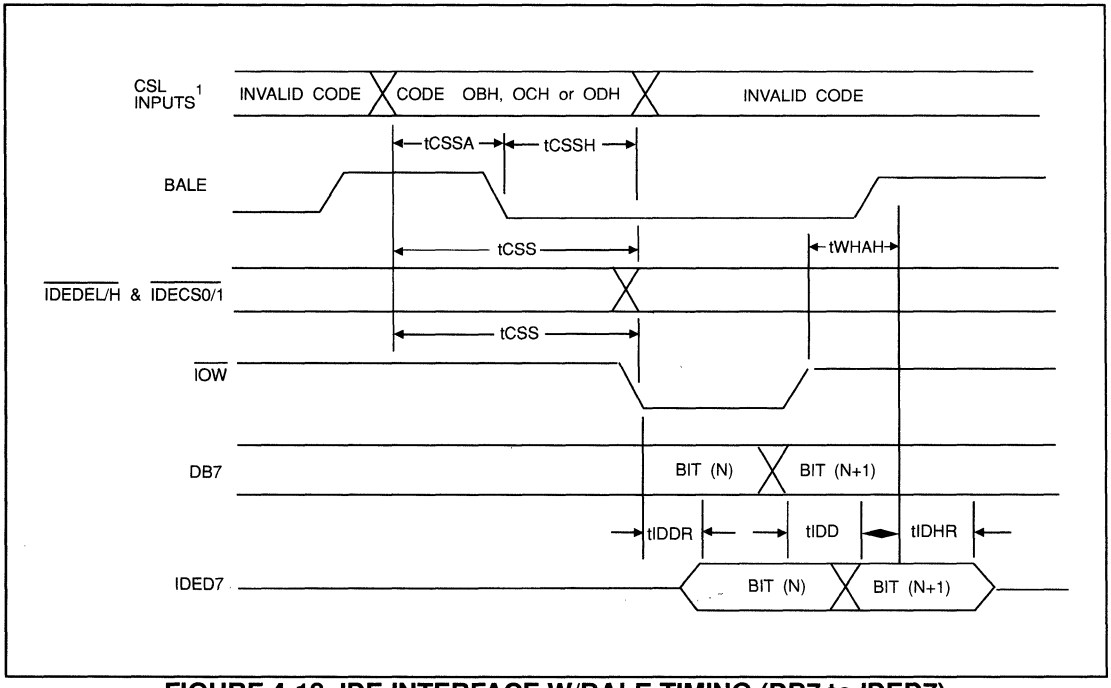


FIGURE 4-18. IDE INTERFACE W/BALE TIMING (DB7 to IDED7)

17

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCWSS	CSL Input Valid and $\overline{IOW}$ Low to OSC Transition to Low	30		ns
tCWSR	CSL Input Invalid and $\overline{IOW}$ Low to OSC Transition to Low	30		ns
tOSD	OSC Suspend Initiated to OSC Low Gap	60		µS
tOSL	OSC Low Gap	60		µS

TABLE 4-19. RESUME TO SUSPEND SUPPORT TIMING*

* Note: Code 15H can also be latched in with BALE as previously shown.

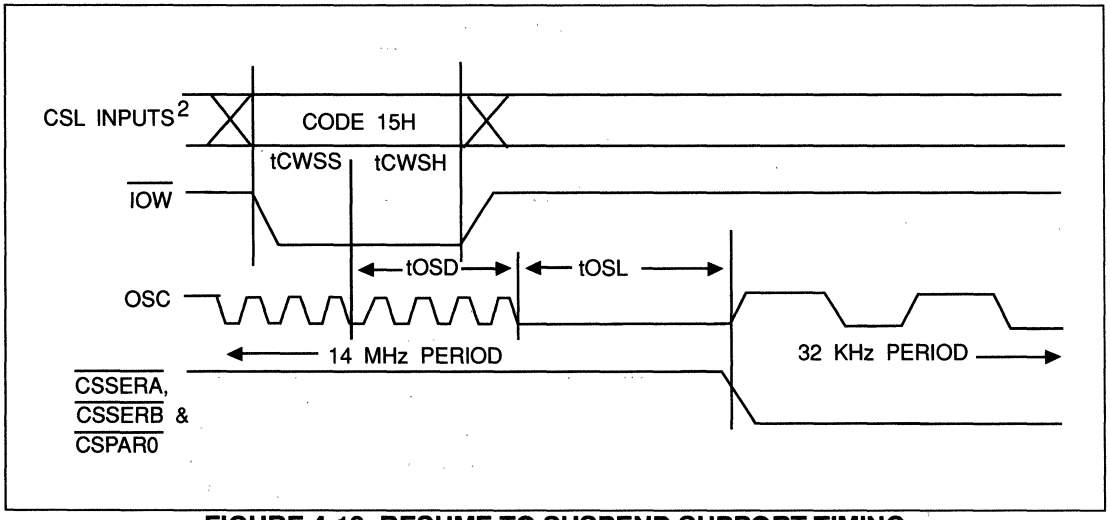


FIGURE 4-19. RESUME TO SUSPEND SUPPORT TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCRS	CSL Input Valid to OSC Transition to Low	30		ns
tCRH	CSL Input Invalid to OSC Transition to Low	30		ns
tCOR	CSL Output De-Assert to Resume WD76C30*	60	91	µS
tOTD	OSC Transition Delay (for XTAL warmup)*	500	501	ms

* CSL Code 16H is latched on the falling edge of OSC.

TABLE 4-20. SUSPEND TO RESUME SUPPORT TIMING

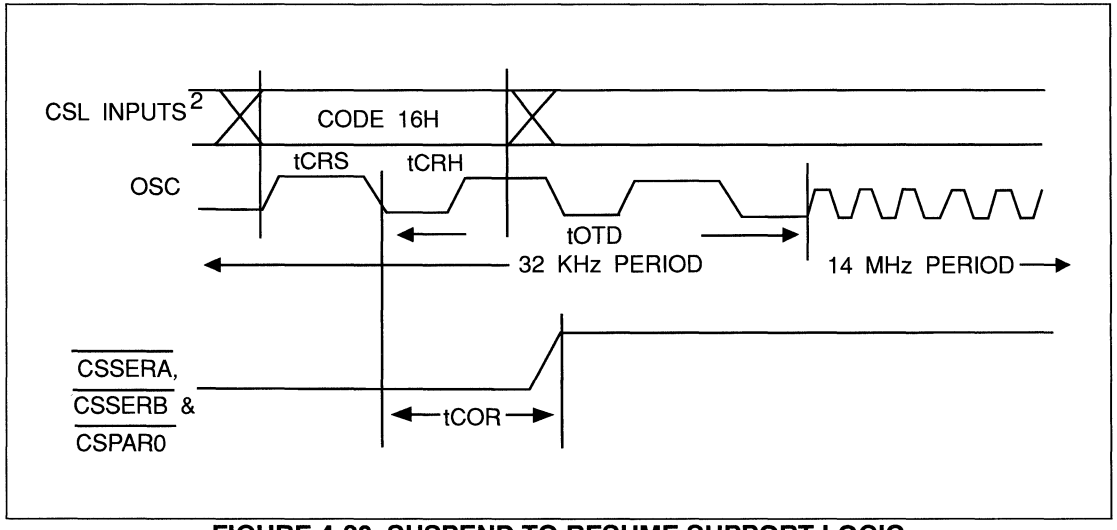


FIGURE 4-20. SUSPEND TO RESUME SUPPORT LOGIC

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSA	CSL Input[2] Valid to CSL Asserted		35	ns
tCSD	CSL Input[2] Invalid to CSL Output De-Asserted		35	ns
tCSH	CSL Input Address[2] Hold Time from $\overline{IOW}$ High	10		ns
tWLPH	$\overline{IOW}$ Low to PCUW0/1 High		35	ns
tWHPH	$\overline{IOW}$ High to PCUW0/1 Low		35	ns

TABLE 4-21. CHIP SELECT LOGIC DECODE TIMING SPECIFICATION

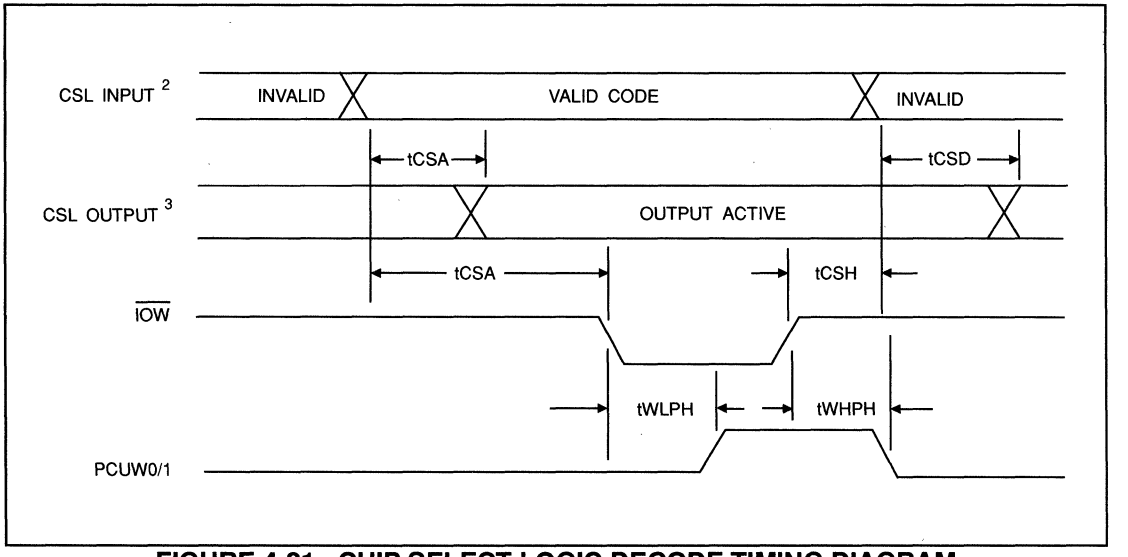


FIGURE 4-21. CHIP SELECT LOGIC DECODE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[2] Set Up to BALE Low	10		ns
tCSSH	CSL Inpu Addresst[2] Hold Time from BALE Low	5		ns
tCSA	CSL Input Valid to Output[3]Asserted	35		ns

TABLE 4-22. CSL DECODE W/BALE TIMING SPECIFICATION

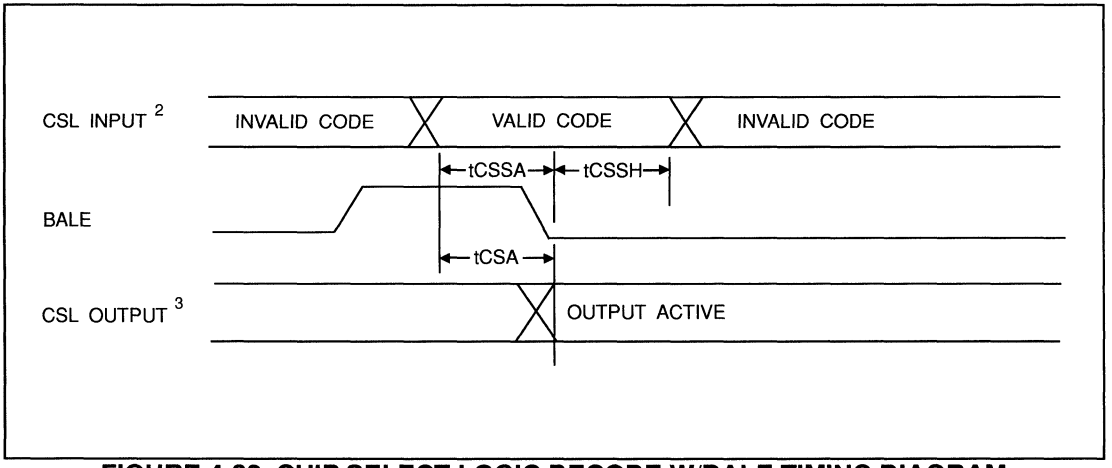


FIGURE 4-22. CHIP SELECT LOGIC DECODE W/BALE TIMING DIAGRAM

Notes

[1] The RTCALE and RTCCS are internal to the WD76C20 and are used by the RTC during I/O operations. The CS, LDCR and LDOR are also internal to the WD76C20 and used by the FDC during I/O operations. CSL Inputs are decoded in Table 2-6 are comprised of DPH, DPL, RA10, RA9 and RA8. All CSL Input Addresses are qualified by the CSEN signal. The general specification for generating the internal and external signals is presented in Table 4-21 and 4-22.

[2] CSL Inputs are decoded in Table 2-6 and are comprised of DPH, DPL, RA10, RA9 and RA8. All CSL Input Addresses are qualified by the CSEN signal as shown in Figure 4-21 and 4-22. Also included in this group is DACKEN which must be deasserted (logic=0) in order to allow the decoder to activate any signal other than TC, which is asserted (logic=1) when both DACKEN and CSEN are active.

[3] CSL outputs are control lines used both internally by the WD76C20 (FDCCS, FDC LDCR, FDC LDOR, RTC CS, and RTC AEN) and externally by other chips (IDEDENL, IDEDENH, CSIDE0, CSIDE1, CSSERA, CSSERB, CSPAR0, ROMOE, 8042CS, NPCS, PCUW0, PCUW1, PROGCS, EMS and TC). For all but one case, only a single, decoded output is asserted at any given time and is unique as decoded in Table 2-6. Although not mentioned in Table 2-6, TC is asserted when both DACKEN and CSEN are active, as specified in Table 4-6.

17

WD76C30

Peripheral Controller, Interrupt Multiplexer, and Clock Generator Device

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 DESCRIPTION

1.1 FEATURES

- Two fully programmable and independent serial I/O ports configurable as PC/AT compatible (WD16C452) or PS/2 compatible (WD16C552)
  - ° Loopback controls for communications link fault isolation for each ACE
  - ° Line break generation and detection for each ACE
  - ° Complete status reporting capabilities
  - ° Generation and stripping of serial asynchronous data control bits (start, stop, parity)
  - ° Programmable baud rate generator and MODEM control signals for each port
  - ° Programmable baud rate generator input clock
  - ° Optional 16 byte FIFO buffers on both transmit and receive of each port for CPU relief during high speed data transfer
  - ° Programmable FIFO threshold levels of 1, 4, 8, or 14 bytes on each port
- Parallel port configurable as a fully Centronics or PS/2 compatible, bidirectional parallel port
- Independently programmable parallel port
- Interrupt multiplexing logic
  - ° Selectable multiplexing logic for connecting PC/AT interrupt request lines to the WD76C10 single chip AT controller
- Clock generation circuitry
  - ° 80287 coprocessor clock generation
  - ° WD76C10 and floppy controller clock generation
  - ° 8042 keyboard clock generation
- Built-in testability features
- Hardware or software controllable sleep mode
- CMOS implementation for high speed and low power requirements
- Pulse extension on IRQ inputs
- 84-pin PLCC and PQFP packages

1.2 GENERAL

The WD76C30 device provides three functional groups. It is a Peripheral Controller, Interrupt Multiplexer, and Clock Generator.

The low power CMOS WD76C30 is a single device solution which provides interrupt multiplexing logic, clock generation, two serial ports, and one bidirectional parallel port.

Interrupt multiplexing logic interfaces the PC/AT interrupt request lines with the WD76C10 Single Chip AT Controller.

Integrated clock generation circuitry uses the 48 MHz input signal to generate the 1.8462, 3.072, and 8.0 MHz clocks used internally for the two serial ports, a 9.6 MHz signal used for the keyboard controller and floppy controller, a programmable duty/frequency clock for the 80287 coprocessor, and a 16 MHz clock for driving the WD76C10 Single Chip AT Controller, and floppy controller.

For low power implementations such as laptops, oscillator disable and sleep modes are available to power down unused logic.

The bidirectional parallel port is software configurable as either a PC/AT or a PS/2 compatible port. The parallel port data lines and open drain printer signals have high current drive capabilities.

Each ACE is programmable as either a WD16C550 or WD16C450 compatible device. Each WD16C550 configured ACE is capable of buffering up to 16 bytes of data upon reception, relieving the CPU of interrupt overhead. Buffering of data also allows greater latency time in interrupt servicing which is vital in a multitasking environment. Each ACE has a maximum recommended data rate of 512K.

1.3 PERIPHERAL CONTROLLER

The peripheral controller is functionally equivalent to the WD16C452/552. The mode of operation of the serial ports and parallel port is selectable via the Mode Select Register. Each serial port is configurable as either a FIFO enhanced ACE (WD16C550 compatible) or a standard ACE (WD16C450). The parallel port is configurable as either a PS/2 bidirectional parallel port or a PC/AT compatible parallel port. A detailed description of the Mode Selection Register is described in the parallel port section.

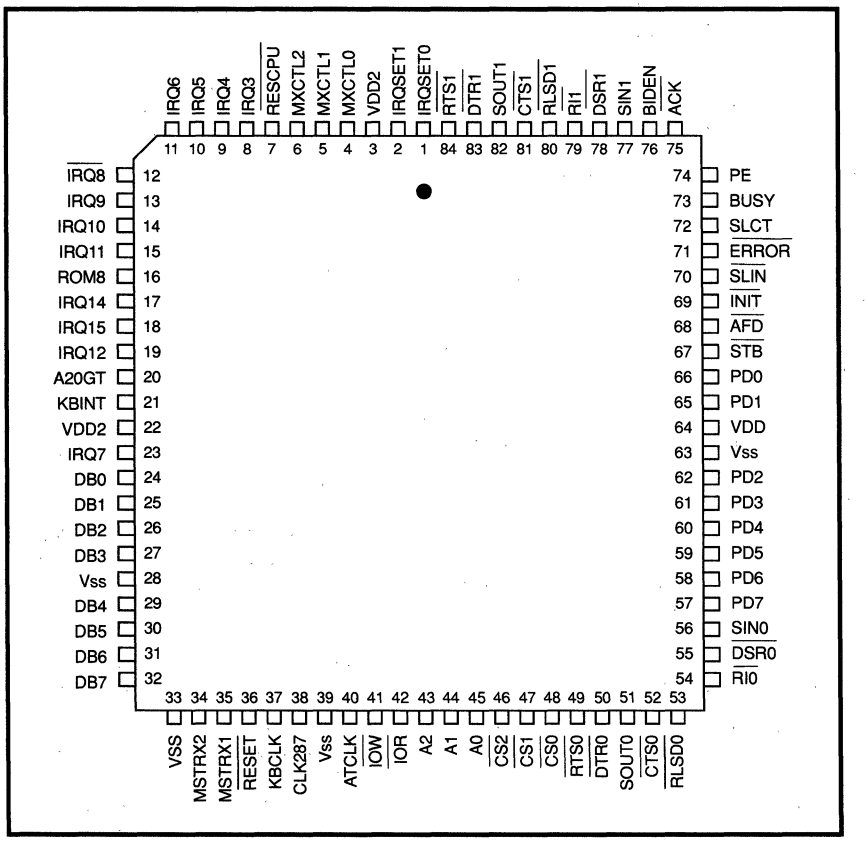


FIGURE 1-1. 84-PIN PLCC - SIGNAL/PIN ASSIGNMENT

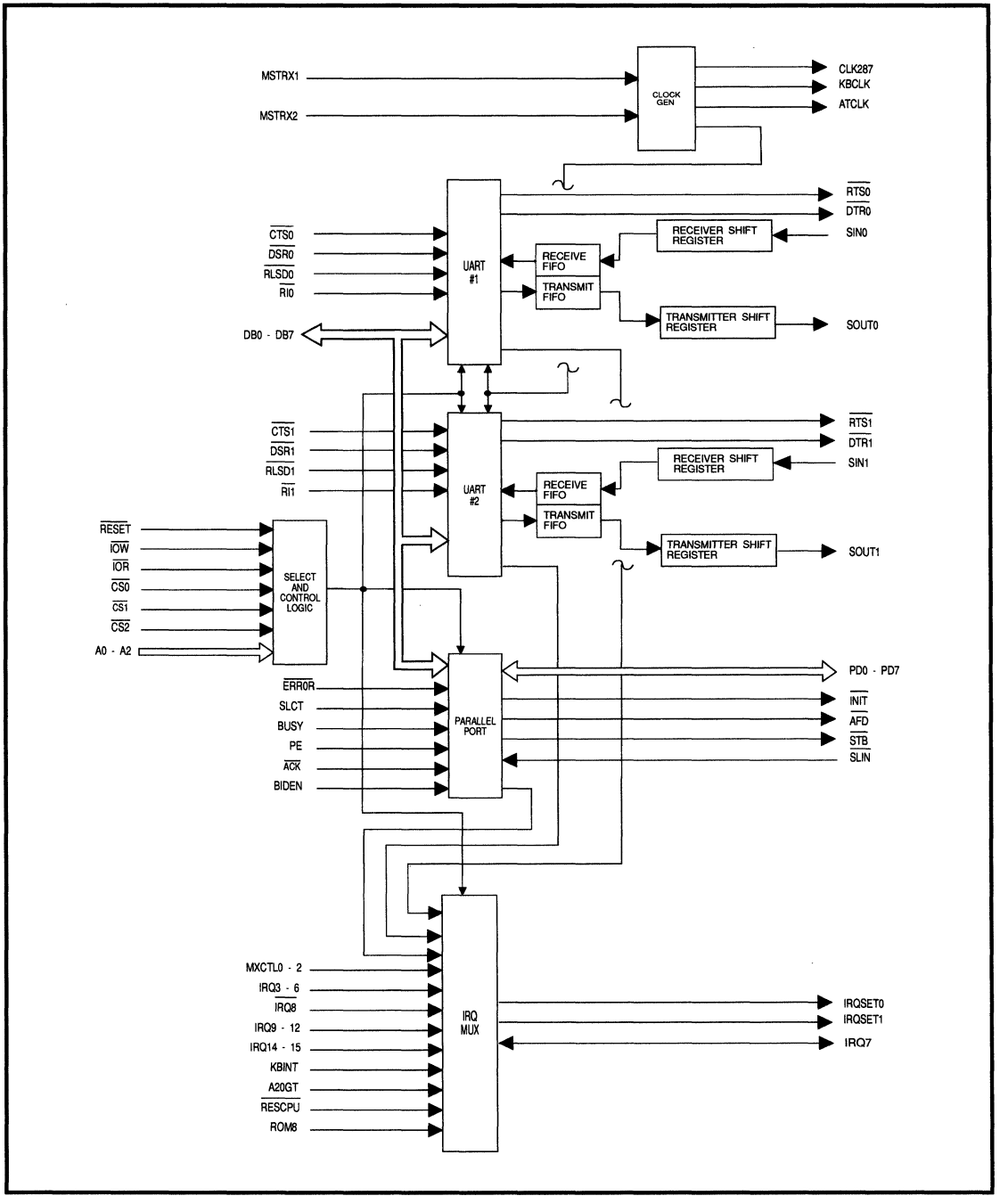


FIGURE 1-2. WD76C30 BLOCK DIAGRAM

18

2.0 PIN DESCRIPTION

Table 2-1 provides a description of the signals serviced by the WD76C30. A drawing of the 84-pin QUAD package, showing the pin and signal locations, is provided on the front cover. The DC operating characteristics and timing is presented in Section 6.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
76	BIDEN	Bidirectional Enable	I	When de-asserted, the BIDEN enables the parallel port data lines as outputs. When asserted, BIDEN works in conjunction with the DIR bit (see Table 4-3) to control the direction of the parallel port data bit.
78, 55	$\overline{DSR1}$, $\overline{DSR0}$	Data Set Ready	I	The communication link asserts these signals to indicate that it is ready to exchange data with the associated Asynchronous Communications Element (ACE). Bit 5 of the associated MODEM Status Register reflects the logical state of $\overline{DSR}$.
79, 54	$\overline{RI1}$, $\overline{RI0}$	Ring Indicator	I	When asserted, these signals indicate that a ringing signal for the associated ACE is being received by the MODEM or data set. This logical value is reflected in bit 6 of the associated MODEM Status Register.
80 53	$\overline{RLSD1}$ $\overline{RLSD0}$	Received Line Signal Detect	I	The Data Circuit-terminating Equipment (DCE) asserts these signals when the associated ACE is receiving a signal that meets its signal quality conditions. Bit 3 of the associated MODEM Status Register reflects this value.
82 51	SOUT1 SOUT0	Serial Data Output	O	SOUT1 is the transmitted Serial Data Output from ACE#1 to the communication link. SOUT0 is the transmitted Serial Data Output from ACE#0 to the communication link. The SOUT signals are set to a marking condition (logical 1) upon a Master Reset.
77, 56	SIN1, SIN0	Serial Data Inputs	I	SIN1 is the received Serial Data Input from the communication link to ACE#1. SIN0 is the received Serial Data Input from the communication link to ACE#0. Data on the serial data inputs are disabled when exercising loop back mode and internally connected to their respective SOUT lines.

TABLE 2-1. PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
83, 50	DTR1, DTR0	Data Terminal Ready	O	When asserted, the Data Terminal Ready informs the MODEM or data set that the associated ACE is ready to receive. This value is reflected in bit 0 of the MODEM Control Register.
84, 49	RTS1, RTS0	Request To Send	O	When asserted, the Request To Send informs the MODEM or data set that the associated ACE is ready to transmit data. This value is reflected in bit 1 of the MODEM Control Register.
81, 52	CTS1, CTS0	Clear to Send	I	The DCE asserts the Clear To Send to signal the associated ACE that a remote device is ready to transmit. This value is reflected in bit 4 of the MODEM Status Register.
32 - 29, 27 - 24	DB7 - DB0	Data Bits	I/O	The Data Bits are tri-state, bidirectional communication lines between the WD76C30 and Data Bus. DB0 is the least significant bit and the first serial bit to be transmitted or received.
43 - 45	A2, A1, A0	Address lines A2-A0	I	Address Lines A2 - A0 are used to select the registers internal to the WD76C30.
41	IOW	Input/Output Write Strobe	I	When Input/Output Write Strobe is asserted, data is written to the Port's addressed register from the Data Bus (DB7 - DB0). The register is addressed by Address Lines A2 - A0. ACE#0, ACE#1, or the Parallel Port is selected by CS0, CS1, or CS2 respectively.
42	IOR	Input/Output Read Strobe	I	When Input/Output Read Strobe is asserted, data is read from the Port's addressed register and placed on the Data Bus (DB7 - DB0). The register is addressed by Address Lines A2 - A0. ACE#0, ACE#1, or the Parallel Port is selected by CS0, CS1, or CS2 respectively.
48	CS0	Chip Select 0	I	Chip Select 0 when asserted, selects serial port 0.
47	CS1	Chip Select 1	I	Chip Select 1 when asserted, selects serial port 1.
46	CS2	Chip Select 2	I	Chip Select 2 when asserted, enables the parallel port.

TABLE 2-1. PIN DESCRIPTIONS Cont.

18

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
36	RESET	Reset	I	When asserted, RESET forces the WD76C30 into an idle mode in which all serial data activities are terminated. The IRQ MUX is forced into a non-compatible mode. The WD76C30 remains in the idle state until programmed to begin data activities.
57 - 62, 65 - 66	PD7 - PD0	Parallel Data Bits	I/O	Bidirectional data port, providing parallel input and output to the parallel port.
67	STB ①	Line Printer Strobe	O	When asserted, the Line Printer Strobe signals the line printer to latch the data currently on the parallel port (PD7 - PD0).
68	AFD ①	Line Printer Autofeed	O	When asserted, the Line Printer Autofeed signals the line printer to autofeed continuous form paper.
69	INIT ①	Line Printer Initialize	O	When asserted, Line Printer Initialize signals the line printer to begin an initialization routine.
70	SLIN ①	Line Printer Select	O	When asserted, Line Printer Select selects the printer.
23	IRQ7/IRQ7	Interrupt Request 7	I/O	IRQ7/IRQ7 is an input to the IRQ MUX when the WD76C30 is not in the Stand Alone Mode. IRQ7/IRQ7 is output as the Parallel Port Interrupt when the WD76C30 is in the Stand Alone Mode (refer to Section 5.6, 5.7). When operating as the Parallel Port Interrupt, IRQ7/IRQ7 is a tri-state signal and must be enabled by bit 4 in the Write Control Register (refer to Section 4.0). When the Parallel Port Interrupt is PC/AT compatible, this signal is IRQ7 and is asserted at the rising edge of ACK and de-asserted at the falling edge of ACK. When the Parallel Port is PS/2 compatible, this signal is IRQ7 and is asserted at the rising edge of ACK and de-asserted at the rising edge of IOR, when reading the Parallel Port Status Register.
71	ERROR	Line Printer Error	I	The printer asserts this signal to inform the parallel port of a deselect condition, PE, or other error condition.

① These outputs are open drain with internal pull-ups.

TABLE 2-1. PIN DECSRIPTION Cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
72	SLCT	Line Printer Select	I	The line printer asserts the Line Printer Select signal when it has been selected.
73	BUSY	Line Printer Busy	I	The line printer asserts the Line Printer Busy signal when it has an operation in progress.
74	PE	Line Printer Paper Empty	I	The line printer asserts the Line Printer Paper Empty signal when it is out of paper.
75	$\overline{ACK}$	$\overline{\text{Line Printer Acknowledge}}$	I	The line printer asserts the $\overline{\text{Line Printer Acknowledge}}$ signal to confirm that the data transfer from the WD76C30 to the printer was successful.
4 - 6	MXCTL0 - MXCTL2	IRQ MUX Control	I	MXCTL0 - MXCTL2 are encoded select signals generated by the WD76C10 for sampling the IRQ inputs.
8 - 15, 17-19	$\overline{IRQ3}$ - 6 $\overline{IRQ8}$ IRQ9-11 IRQ14, 15, 12	IRQ MUX Inputs	I	These 11 interrupt signals, along with $\overline{IRQ7}$, $\overline{RESCPU}$, ROM8, KBINT, and A20GT are multiplexed into IRQSET0 and IRQSET1 at a period rate defined by MXCTL0 - MXCTL2.
7	$\overline{RESCPU}$	$\overline{\text{Reset CPU}}$	I	The keyboard controller asserts $\overline{\text{Reset CPU}}$ when the CPU should be reset.
16	ROM8	8-bit ROM	I	ROM8 is multiplexed into the IRQSET1 signal and, when asserted, indicates to the WD76C10 that the system ROM is eight bits, when de-asserted it is 16 bits.
21	KBINT	Keyboard Interrupt	I	KBINT is multiplexed into the IRQSET1 signal and indicates to the WD76C10 that a keyboard interrupt is pending.
20	A20GT	Address 20 Signal	I	A20GT is multiplexed into the IRQSET1 signal and reflects the state of the address 20 signal. This allows compatibility with the 8086 and 80286 processors when addressing memory in the 64 Kbyte boundary above 1 Mbyte.
35	MSTRX1 ①	Master Clock 1	I	The Master Clock 1 signal can be driven by either a 16 MHz crystal or 48 MHz TTL oscillator.
34	MSTRX2 ①	Master Clock 2	O	Master Clock 2 is connected to the 16 MHz crystal to generate Master Clock 1 for the clock generation circuitry. This pin is left disconnected if Master Clock 1 is being driven by a 48 MHz TTL oscillator.

① Third overtone of 16 MHz crystal is used to generate the 48 MHz clock.

TABLE 2-1. PIN DESCRIPTION Cont.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
38	CLK287	80287 Clock	O	CLK287 clock drives the 80287 coprocessor. CLK287 is programmable via the Clock Selection Register. A variety of clock frequencies and duty cycles provide compatibility with a variety of 80287 or 80287 compatible coprocessors.
37	KBCLK	Keyboard Clock	O	Keyboard Clock is a 9.6 MHz clock used to drive the keyboard controller. This signal can be used to drive the WD37C65 Floppy Disk Controller for systems not using the WD76C20 Storage Controller.
40	ATCLK	AT Clock	O	AT Clock is a 16 MHz clock used to drive the ATCLK input to the WD76C10. AT Clock provides a fixed reference that allows the PC/AT bus state machine to run with 8 MHz compatible timing. This signal can be used to drive the Floppy Disk Controller in the WD76C20 Storage Controller.
1 2	IRQSET0 IRQSET1	Interrupt Request Set 0, 1	O	These signals are outputs of the IRQ multiplexing logic. When in the Stand Alone Mode IRQSET0 and IRQSET1 become the tri-state interrupt outputs from Serial Port 0 and 1 respectively. (Refer to Section 5.6)
64	V_{DD}	Power Supply		+5V power supply to the serial and parallel port logic. This supply can be turned off.
3, 22	$V_{DD}2$	Power Supply		+5V power supply to the WD76C30 with the exclusion of serial and parallel port logic.
28, 39, 63, 33	Vss	Ground		System signal ground.

TABLE 2-1. PIN DESCRIPTION Cont.

3.0 SERIAL PORT REGISTERS

The WD76C30 contains two serial ports, therefore, the following registers exist in duplicate, one per port.

3.1 SERIAL PORT REGISTER ADDRESSING

3.1.1 Chip Select ($\overline{CS0}$, $\overline{CS1}$)

When $\overline{CS0}$ is low, registers for serial port 0 can be accessed, and when $\overline{CS1}$ is low, registers for serial port 1 can be accessed. No more than one $\overline{CS}$ ($\overline{CS0}$, $\overline{CS1}$, or $\overline{CS2}$) should ever be low at any time, unless all three are low for Sleep Mode.

Power Down Reset:
In the Parallel Port, asserting Mode Selection Register bit 3 causes the ACE to reset to the condition listed in Table 3-2.

Software Reset:
A software reset is performed by writing to the Divisor Latches, forcing the transmitter and receiver to an idle mode. Registers are not reset by this operation. Prior to enabling interrupts, the LSR and RBR registers should be read to clear out any data, returning them to a known state without resetting the system.

Chip Select ($\overline{CS0}$, $\overline{CS1}$) and register select (A0, A1, A2) signals must be stable for the duration of a read or write operation.

3.1.2 Register Select (A0, A1, A2)

To select a register for read or write operation, see Table 3-1.

NOTE

Divisor Latch Access Bit (DLAB) is the MSB of the Line Control Register. DLAB must be programmed high (logic 1) by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer Register (read),
0	0	0	0	Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable Register
X	0	1	0	Interrupt Identification Register (read only)
X	0	1	0	FIFO Control Register (write only)
X	0	1	1	Line Control Register
X	1	0	0	MODEM Control Register
X	1	0	1	Line Status Register (read only)
X	1	1	0	MODEM Status Register
X	1	1	1	Scratch Pad Register
1	0	0	0	Divisor Latch Register (least significant byte)
1	0	0	1	Divisor Latch Register (most significant byte)

TABLE 3-1. REGISTER ADDRESSING

3.2 ACE OPERATIONAL DESCRIPTION

3.2.1 Master Reset

Asserting $\overline{\text{RESET}}$ on pin 36 causes the ACE to reset to the condition listed in Table 3-2.

3.2.2 ACE Accessible Registers

The system programmer has access to any of the registers as summarized in Table 3-3. For individual register descriptions, refer to the following pages under register heading.

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-3; 6 and 7 are forced Low. Bits 4 and 5 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, except Bits 5 and 6 are High
MODEM Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low, Bits 4-7 at Input Signal
Divisor Latch (low order byte)	Writing into the Latch	Data
Divisor Latch (high order byte)	Writing into the Latch	Data
$\overline{\text{SOUT}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
RCVR FIFO Counter	MR or FCR1• FCR0 or ΔFCR0	All Bits Low
XMIT FIFO Counter	MR or FCR2 • FCR0 or ΔFCR0	All Bits Low
FIFO CONTROL	Master Reset	All Bits Low
D7 - D0 Data Bus Lines	In Tri-State Mode, Unless $\overline{\text{IOR}}$ = Low	Tri-State Data (ACE to CPU)
Address Selection Register	Master Reset	All Bits Low
Clock Selection Register	Master Reset	All Bits Low
CLK Disable Register	Master Reset	All Bits Low
Serial Port Interrupt Selection Register	Master Reset	All Bits Low
Serial Port Interrupt Selection Register	Master Reset	All Bits Low
Parallel Port Interrupt Selection Register	Master Reset	All Bits Low
Mode Selection Register	Master Reset	All Bits Low
Parallel Port Control	Master Reset	Bits 7 - 6 High, Bits 5 - 0 Low
Parallel Port Data	Master Reset	All Bits Low
Parallel Port StatusNone $\overline{\text{SLIN}}$, $\overline{\text{INIT}}$, $\overline{\text{AFD}}$, $\overline{\text{STB}}$,	Master Reset	High, Low, High, High

* Reset disables the Stand Alone Mode *

TABLE 3-2. RESET CONTROL OF REGISTERS AND PINOUT SIGNALS

	REGISTER ADDRESS ②					
	DLAB = 0 A2-A0 = 0 Read Only	DLAB = 0 A2-A0 = 0 Write Only	DLAB = 0 A2-A0 = 1	DLAB = X A2-A0 = 2 Read Only	DLAB = X A2 - A0 = 2 Write Only	DLAB = X A2 - A0 = 3
	REGISTER TITLE					
Bit No.	Receiver Buffer Register	Transmitter Holding Register	Interrupt Enable Register	Interrupt Identification Register	FIFO Control Register	Line Control Register
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending (IP)	FIFO Enable (FEWO)	Word Length Select Bit 0 (WLS0)
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 1 (IID)	Rcvr FIFO Reset (RFR)	Word Length Select Bit 1 (WLS1)
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ERLSI)	Interrupt ID Bit 2 (IID)	Transmitter FIFO Reset (TFR)	Number of Stop Bits (STB)
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit 3 (IID) ①	Not Used	Parity Enable (PEN)
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity (STP)
6	Data Bit 6	Data Bit 6	0	FIFO Enabled ① (FERO)	Rcvr FIFO Trigger Level (LSB)(RFTL)	Set Break Control (SBR)
7	Data Bit 7	Data Bit 7	0	FIFO Enabled ① (FERO)	Rcvr FIFO Trigger Level (MSB) (RFTL)	Divisor Latch Access Bit (DLAB)

① These bits are 0 in Character Mode. ② See Table 3-1

TABLE 3-3. ACCESSIBLE WD76C30 SERIAL PORT REGISTERS

18

	REGISTER ADDRESS ②					
	DLAB = X A2-A0 = 4	DLAB = X A2-A0 = 5	DLAB = X A2-A0 = 6	DLAB = X A2-A0 = 7	DLAB = 1 A2-A0 = 0	DLAB = 1 A2-A0 = 1
	REGISTER TITLE					
Bit No.	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Pad Register	Divisor Latch (LSB)	Divisor Latch (MSB)
0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Not Connected (NC)	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Interrupt (Int)	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO ① (EIRF)	Received Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

① This bit is 0 in Character Mode. ② See Table 3-1

TABLE 3-3. ACCESSIBLE WD76C30 SERIAL PORT REGISTERS (Cont.)

3.3 LINE CONTROL REGISTER

The Line Control Register provides control over the word length, number of Stop Bits, Parity, Break Control and selection of the Receiver Buffer, Transmitter Holding Register and Interrupt Enable Register.

Address A2-A0 = 3, DLAB = X - Read and Write

7	6	5	4	3	2	1	0
DLAB	SBR	STP	EPS	PEN	STB	WLS1	WLS0

Bit 7 - DLAB, Divisor Latch Access

DLAB = 0 -
Access the Receiver Buffer, Transmitter Holding Register or Interrupt Enable Register.

DLAB = 1 -
Access the Divisor Latches of the Baud Rate Generator during a Read or Write operation.

Bit 6 - SBR, Set Break Control

The SBR feature enables the CPU to alert a terminal in a computer communications system.

SBR = 0 -
Resets the Serial Output (SOUT) from the Spacing State.

SBR = 1 -
The Serial Output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level SBR) regardless of other transmitter activity.

Bit 5 - STP, Stick Parity

STP = 0 -
When parity is enabled by PEN (bit 3), it is represented as indicated by the state of EPS (bit 4).

STP = 1 -
When parity is enabled by PEN, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by EPS.

Bit 4 - EPS, Even Parity Select

EPS = 0 -
When PEN (bit 3) equals 1, an odd number of logic 1's are transmitted or checked in the data word bits and Parity bit.

EPS = 1 -
When PEN equals 1, an even number of bits are transmitted or checked.

Bit 3 - PEN, Parity Enable

PEN = 0 -
No parity is generated or checked.

PEN = 1 -
Parity is generated on transmitted data or checked on received data between the last data word bit and Stop bit of the serial data. The Parity bit is used to produce an even or odd number of 1's when the data word bits and the Parity bit are summed.

Bit 2 - STB, Number Of Stop Bits

This bit specifies the number of Stop Bits in each transmitted serial character.

STB = 0 -
One Stop Bit is generated in the transmit data.

STB = 1 -
When WLS1 and WLS0 (bits 1 and 0) select a 5-bit word length, 1-1/2 Stop bits are generated.

When WLS1 and WLS0 select a 6, 7 or 8-bit word length, two Stop bits are generated.

Bits 1, 0 - WLS1, WLS0, Word Length Select

WLS1 and WLS0 specify the number of bits in each transmitted or received serial character.

WLS1	WLS0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

18

3.4 ACE PROGRAMMABLE BAUD RATE GENERATOR

The ACE contains a programmable Baud Rate Generator with a programmable input clock of 1.843 MHz, 3.0 MHz or 8 MHz clocks, as well as a 48 MHz input for test purposes. The output frequency of the Baud Generator is 16 times the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load. Loading of either divisor Latch forces the Transmitter and Receiver into the Idle Mode.

Tables 3-3, 3-4 and 3-5 illustrate the use of the Baud Generator with three different driving frequencies. One is referenced to a 1.8432 MHz clock, another is a 3.072 MHz clock and the third is an 8.0 MHz clock.

NOTE

The maximum operating frequency of the Baud Rate Generator is 8.0 MHz.

The data rate should never be greater than 512K baud.

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 TIMES CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.690
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.860

TABLE 3-4. BAUD RATES USING 1.8432 MHz CLOCK

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 TIMES CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	—
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.230
9600	20	—
19200	10	—
38400	5	—

TABLE 3-5. BAUD RATES USING 3.072 MHz CLOCK

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 TIMES CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	10000	—
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	—
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.344

TABLE 3-6. BAUD RATE USING 8.0 MHz CLOCK

3.5 LINE STATUS REGISTER

The Line Status Register provides status information to the CPU concerning the data transfer.

Address A2-A0 = 5, DLAB = X - Read and Write

7	6	5	4	3	2	1	0
EIRF	TEMT	THRE	BI	FE	PE	OE	DR

Bit 7 - EIRF, Error in RCVR FIFO

EIRF = 0 -
When in Character Mode, EIRF is always 0.

When in FIFO Mode, a 0 indicates no error in the RCVR.

EIRF = 1 -
There is at least one parity error, framing error or break indication in the FIFO. EIRF is set to 0 when the Line Status Register is read and there are no additional errors in the FIFO.

Bit 6 - TEMT, Transmitter Empty

TEMT = 0 -
When in the Character Mode, at least one byte has been written into the Transmitter Holding Register.

When in the FIFO Mode, at least one byte has been written into the XMIT FIFO.

TEMT = 1 -
When in the Character Mode, the Transmitter Holding Register and Transmitter Shift Register are idle (empty).

In the FIFO Mode, the XMIT FIFO and XMIT Shift Registers are empty.

Bit 5 - THRE, Transmitter Holding Register Empty

Character Mode:

THRE indicates that the ACE is ready to accept a new character for transmission. THRE also causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty interrupt enable is set high.

THRE = 0 -
The CPU has loaded the Transmitter Holding Register.

THRE = 1 -
A character has been transferred from the Transmitter Holding Register into the Transmitter Shift Register.

FIFO Mode:

Normally

THRE responds immediately when the XMIT FIFO is emptied or when the first character is written into the XMIT FIFO.

The first transmitter interrupt after changing the first bit of FIFO Control Register will be immediate if the FIFO Control Register is enabled.

Exception

The Transmitter FIFO empty indications are delayed one character time, minus the last Stop Bit time, whenever the Transmitter FIFO is empty and there have not been at least two characters in Transmitter FIFO at the same time since the last time that Transmitter FIFO was empty.

THRE = 0 -
At least one character has been written into the XMIT FIFO.

THRE = 1 -
The XMIT FIFO is empty.

Bit 4 - BI, Break Interrupt

BI indicates that the received character is a Break.

BI = 0 -
The CPU read the contents of the Line Status Register. Restarting after a break is received requires the SIN pin to be high for at least one half bit time.

BI = 1 -
When in the Character Mode, the received data input has been held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + data bits + Parity + Stop Bits).

When in FIFO Mode, BI is associated to the particular character in the FIFO, and

is set when the associated character is in the top of the FIFO.

Bit 3 - FE, Framing Error

FE indicates that the received character did not have a valid Stop Bit.

FE = 0 -
The CPU read the contents of the Line Status Register.

FE = 1 -
In the Character Mode, the Stop Bit following the last data bit or parity bit was detected as a zero bit (Spacing Level).

In the FIFO Mode, an FE is associated with a particular character in the FIFO, and is set when the associated character is at the top of the FIFO.

Bit 2 - PE, Parity Error

PE indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit.

PE = 0 -
The CPU read the contents of the Line Status Register.

PE = 1 -
In the Character Mode, a parity error has been detected.

In the FIFO Mode, a parity error is associated with a particular character in the FIFO, and PE is set when the associated character is at the top of the FIFO.

Bit 1 - OE, Overrun Error

OE indicates that an Overrun Error occured.

OE = 0 -
The CPU read the contents of the Line Status Register.

OE = 1 -
In the Character Mode, the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register. This destroyed the previous character.

When in FIFO Mode, an OE occurs after the RCVR FIFO is full and the Receiver Shift Register has completely received the next character. An OE is indicated to the CPU as soon as it happens. The character in the shift register will be written over but nothing will be transferred to the FIFO.

Bit 0 - DR, Receiver Data Ready

DR = 0 -
In the Character Mode, the CPU read the data in the Receiver Buffer Register.

In the FIFO Mode, the receiver FIFO is empty.

DR = 1 -
In the Character Mode, a complete incoming character has been received and transferred into the Receiver Buffer Register.

In the FIFO Mode, a complete incoming character has been received and transferred into the RCVR FIFO.

NOTE

Bits 4 through 1 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and Receiver Line Status interrupt is enabled. All bits of the Line Status Register, except bit 7, can be set or reset by writing to the register.

18

3.6 INTERRUPT IDENTIFICATION REGISTER

The ACE has an interrupt capability that allows for complete flexibility in interfacing with all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. Listed according to their priority the four levels of interrupt conditions are:

Receiver Line Status
Received Data Ready
Transmitter Holding Register Empty
MODEM Status

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the Interrupt Identification Register (IIR).

The IIR, when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Bits 3-0 are further described in Table 3-7.

Address A2-A0 = 2, DLAB = X - Read only

7	6	5	4	3	2	1	0
FERO		0	0	IID			IP

Bits 7, 6 - FERO, FIFO Enable

The FE bits identify whether the FIFO Control Register bit 0, has placed the device in the Character Mode or FIFO Mode.

FERO = 0, 0 -
The device is in the Character Mode

FERO = 1, 1 -
The device is in the FIFO Mode.

Bits 5, 4 - These bits are always logic 0.

Bits 3-1 - IID, Interrupt ID

The IID bits identify the highest priority interrupt pending (see Table 3-7).

Bit 0 - IP, Interrupt Pending

The IP bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending.

IP = 0 -
An interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.

IP = 1 -
No interrupt is pending and polling (if used) continues.

INTERRUPT IDENTIFICATION REGISTER				INTERRUPT SET AND RESET FUNCTIONS			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
1	1	0	0	Second	Character Timeout Identification	No Characters have been input or removed from RCVR FIFO during the last 4 character times, and at least one character occupies it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

TABLE 3-7. INTERRUPT CONTROL FUNCTIONS

18

3.7 INTERRUPT ENABLE REGISTER

When INT (bit 3 of Modem Control Register) is a logic 1, the Interrupt Enable Register controls the selection of the four interrupt sources of the ACE, making it possible to separately activate the device's internal Interrupt signals.

It is possible to disable the entire interrupt system, or selected interrupts by configuring bits three though zero of the Interrupt Enable Register.

Disabling the interrupt system inhibits the Interrupt Identification Register and the active internal interrupt signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers.

Address A2-A0 = 1, DLAB = 0 - Read and Write

7	6	5	4	3	2	1	0
0	0	0	0	EDSSI	ERLSI	ETBEI	ERBFI

Bits 7-4 - These four bits are always set to 0 by the hardware.

Bit 3 - EDSSI, Enable MODEM Status Interrupt

EDSSI = 0 -
Disables the MODEM Status Interrupt.

EDSSI = 1 -
Enables the MODEM Status Interrupt.

Bit 2 - ERLSI, Enable Receiver Line Status Interrupt

ERLSI = 0 -
Disables the Receiver Line Status Interrupt.

ERLSI = 1 -
Enables the Receiver Line Status Interrupt.

Bit 1 - ETBEI, Enable Transmitter Holding Register Empty Interrupt

ETBEI = 0 -
Disables the Transmitter Holding Register Empty Interrupt.

ETBEI = 1 -
Enables the Transmitter Holding Register Empty Interrupt.

Bit 0 - ERBFI, Enable Received Data Available Interrupt

ERBFI = 0 -
Disables the Received Data Available Interrupt.

ERBFI = 1 -
Enables the Received Data Available Interrupt.

3.8 SCRATCH PAD REGISTER

This 8-bit register does not control or report status on any part of the ACE. It can be used by the programmer as a general purpose register.

Address A2-A0 = 7, DLAB = X - Read and Write

7	6	5	4	3	2	1	0

3.9 FIFO CONTROL REGISTER

The FIFO Control Register is used to enable the FIFO Mode, clear FIFOs, set the RCVR FIFO trigger levels and select the mode of DMA signaling.

Address A2-A0 = 2, DLAB = X, Write only

7	6	5	4	3	2	1	0
RFTL		Reserved		Not Used	TFR	RFR	FEWO

Bits 7, 6 - RFTL, RCVR FIFO Trigger Level

RFTL controls the trigger level of the Received Data Available Interrupt.

RFTL 7	6	Trigger Level (bytes)
0	0	- 01
0	1	- 04
1	0	- 08
1	1	- 14

Bits 5, 4 - Reserved for future use and should be programmed to zeros.

Bit 3 - Not Used

In the WD16C550 this is the DMS bit.

Bit 2 - TFR, Transmitter FIFO Reset

Writing a one to TFR clears all characters from the XMIT Error FIFO and resets its counters and this bit to 0. The shift register and XMIT FIFO are not cleared.

Bit 1 - RFR, Reciver FIFO Reset

Writing a one to RFR clears all characters from the RCVR Error FIFO and resets its counters and this bit to 0. The shift register and RCVR FIFO are not cleared.

Bit 0 - FEWO, FIFO Enable

FEWO = 0 -
XMIT and RCVR FIFOs are disabled

FEWO = 1 -
XMIT and RCVR FIFOs are enabled. When changing from Character Mode to FIFO Mode, data in the FIFOs does not automatically clear. Setting or resetting FEWO clears all characters from the RCVR Error FIFO and resets the XMIT and RCVR FIFO counters to 0. FEWO must be set to 1 before setting TFR and RFR or they will not be programmed.

3.10 MODEM CONTROL REGISTER

The MODEM Control Register controls the interface with the MODEM, data set or a peripheral device emulating a MODEM.

Address A2-A0 = 4, DLAB = X - Read and Write

7	6	5	4	3	2	1	0
0	0	0	LOOP	INT	NC	RTS	DTR

Bits 7-5 - These three bits are always set to 0 by the hardware.

Bit 4 - LOOP, Loopback Mode

This bit provides a loopback feature for diagnostic testing of the ACE. Selecting the Loopback Mode results in the following setup (Refer to Figure 3-1):

- The transmitter Serial Output (SOUT) is set to a logic 1 (high) state.
- The receiver Serial Input (SIN) is disconnected.
- The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
- The four MODEM Control Inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$ and $\overline{RI}$) are disconnected, and the MODEM Control Register bits 3-0 are internally connected to the four MODEM Control inputs.

If, while in the Standalone Mode Loopback is enabled, the IRQSET output is tri-stated. In the Loopback Mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and receive data paths of the ACE.

In the Loopback Mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

18

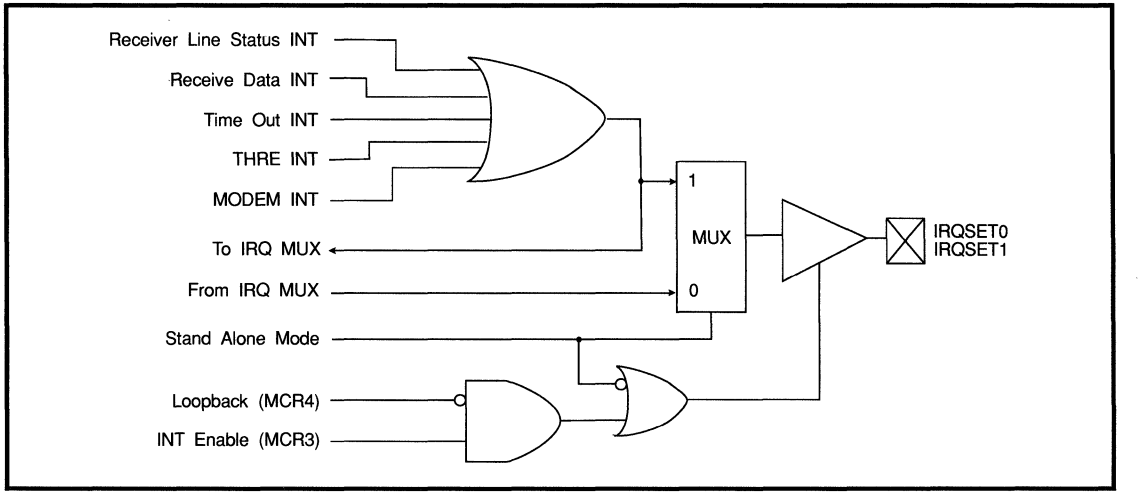


FIGURE 3-1. INTERRUPT SIGNAL LOGIC

The ACE MODEM interrupt system can be tested by writing into the lower four bits of the MODEM Status Register.

To return to normal operation, the registers must be reprogrammed for normal operation and then LOOP (bit 4) reset to a logic 0.

LOOP = 0 -
Normal Mode.

LOOP = 1 -
Loopback Mode.

Bit 3 - INT, Interrupt

INT enables the IRQSET output when in the Stand Alone Mode. In Loopback Mode this bit is connected internally to bit 7 of the MODEM Status Register (Refer to Figure 3-1).

INT = 0 -
The IRQSET output is tri-stated.

INT = 1 -
The IRQSET output is enabled in the Stand Alone Mode.

Bit 2 - NC, No external connection.

In the Loopback Mode, this bit is connected internally to bit 6 of the MODEM Status Register.

Bit 1 - RTS, Request To Send

Bit 1 controls the $\overline{RTS}$ signal. In the Loopback Mode, this bit is connected internally to bit 4 of the MODEM Status Register.

RTS = 0 -
$\overline{RTS}$ is set to a logic one.

RTS = 1 -
$\overline{RTS}$ is set to a logic zero.

Bit 0 - DTR, Data Terminal Ready

Bit 0 controls the $\overline{DTR}$ signal. In the Loopback Mode, this bit is connected internally to bit 5 of the MODEM Status Register.

DTR = 0 -
$\overline{DTR}$ is set to a logic one.

DTR = 1 -
$\overline{DTR}$ is set to a logic zero.

NOTE

The $\overline{DTR}$ output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

3.11 MODEM STATUS REGISTER

The MODEM Status Register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, bits 3 through 0 of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

Address A2-A0 = 6, DLAB = X - Read and Write

7	6	5	4	3	2	1	0
RLSD	RI	DSR	CTS	DRLSD	TERI	DDSR	DCTS

Bit 7 - RLSD, Received Line Signal Detect

RLSD is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input.

In the Loopback Mode (bit 4 of the MODEM Control Register set to 1) this bit is connected internally to bit 3 of the MODEM Control Register (INT).

Bit 6 - RI, Ring Indicator

RI is the complement of the Ring Indicator ($\overline{RI}$) input. In the Loopback Mode (bit 4 of the MODEM Control Register set to 1) this bit is connected internally to bit 2 of the MODEM Control Register.

Bit 5 - DSR, Data Set Ready

DSR is the complement of the Data Set Ready ($\overline{DSR}$) input. In the Loopback Mode (bit 4 of the MODEM Control Register set to 1) this bit is connected internally to bit 0 of the MODEM Control Register (DTR).

Bit 4 - CTS, Clear To Send

CTS is the complement of the Clear to Send ($\overline{CTS}$) input. In the Loopback Mode (bit 4 of the MODEM Control Register set to 1) this bit is connected internally to bit 1 of the MODEM Control Register (RTS).

Bit 3 - DRLSD, Delta Received Line Signal Detector

DRLSD is the Delta Received Line Signal Detector (DRLSD) indicator.

DRLSD = 0 -
The $\overline{RLSD}$ input to the WD76C30 has not changed state since the last time it was read by the CPU.

DRLSD = 1 -
The $\overline{RLSD}$ input to the WD76C30 has changed state since the last time it was read by the CPU.

Bit 2 - TERI, Trailing Edge of Ring Indicator

TERI is the Trailing Edge of Ring Indicator (TERI) detector.

TERI = 0 -
The $\overline{RI}$ input to the WD76C30 has not changed from an On (logic 1) to an Off (logic 0) condition.

TERI = 1 -
The $\overline{RI}$ input to the WD76C30 has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 1 - DDSR, Delta Data Set Ready

DDSR is the Delta Data Set Ready (DDSR) indicator.

DDSR = 0 -
The $\overline{DSR}$ input to the WD76C30 has not changed state since the last time it was read by the CPU.

DDSR = 1 -
The $\overline{DSR}$ input to the WD76C30 has changed state since the last time it was read by the CPU.

Bit 0 - DCTS, Delta Clear to Send

DCTS is the Delta Clear to Send (DCTS) indicator.

DCTS = 0 -
The CTS input to the WD76C30 has not changed state since the last time it was read by the CPU.

DCTS = 1 -
The CTS input to the WD76C30 has changed state since the last time it was read by the CPU.

18

NOTE

Setting bits 3, 2, 1, or 0 to a logic 1 generates a MODEM Status Interrupt.

3.12 FIFO OPERATION NOTES

3.12.1 FIFO Interrupt Mode Operation

When FEWO and ERBFI are 1 (bit 0 of the FIFO Control Register and bit 1 of the Interrupt Enable Register), the following RCVR interrupts will occur.

1. A FIFO timeout interrupt occurs when the following is true:

   a. There is at least one byte in the RCVR FIFO.

   b. No character has been received in four continuous character times (if two stop bits are being used, the second one is included in this time delay).

   c. The most recent CPU read from the FIFO has exceeded four continuous character times.

   The timeout counter is proportional to the baud rate. After a timeout interrupt, the interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

2. When the RCVR FIFO reaches its programmed trigger level, the receive data interrupt is set. This interrupt is cleared as soon as the FIFO level falls below the trigger level.

3. When the XMIT FIFO is empty, the THRE interrupt is set and is reset when one character is written to the XMIT FIFO.

3.12.2 FIFO Polling Mode Operation

The FIFO Polling Mode is initialized when FEWO is 1 and EDSSI, ERLSI, ETBEI and ERBFI are 0 (bit 1 of the FIFO Control Register and bits 3 through 0 of the Interrupt Enable Register). In polling mode, the user can poll the LSR directly to check the transmitter and receiver status. Since the receiver and transmitter are controlled separately, either one or both can be in polling mode.

There is no trigger level reached or timeout condition indicated on the interrupt pin in the FIFO Polling Mode. However, the RCVR and XMIT FIFOs are still fully capable of holding characters.

3.12.3 FIFO Pointer

The RCVR FIFO has an internal pointer that automatically points to the RCVR Data byte and associated Status byte to be read. Reading the RCVR Data byte increments the internal counter, while reading the Status byte does not, therefore, the Status byte should always be read prior to reading the Data byte associated with it.

4.0 PARALLEL PORT DESCRIPTION

The parallel port supports Centronics type printers. When $\overline{CS2}$ is asserted, the parallel port is selected, allowing access to all parallel port control and status registers. (Refer to Tables 4-1 and 4-2.)

A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	REGISTER
X	0	0	0	1	Read Data
X	0	1	0	1	Read Status
X	1	0	0	1	Read Control
0	1	1	0	1	Address Select Register Read
1	1	1	0	1	Data Access Register Read
X	0	0	1	0	Write Data
X	0	1	1	0	Invalid
X	1	0	1	0	Write Control
0	1	1	1	0	Address Select Register Write
1	1	1	1	0	Data Access Register Write

TABLE 4-1. PARALLEL PORT ($\overline{CS2}$ = 0) REGISTER ADDRESS

BIT NO.	READ PORT 0	READ STATUS 1	READ CONTROL 2	WRITE CONTROL 2	WRITE DATA 0
0	Data Bit 0	1	STB	STB	Data Bit 0
1	Data Bit 1	1	AFD	AFD	Data Bit 1
2	Data Bit 2	$\overline{INT}$ ①	$\overline{INIT}$	$\overline{INIT}$	Data Bit 2
3	Data Bit 3	$\overline{ERROR}$	SLIN	SLIN	Data Bit 3
4	Data Bit 4	SLCT	IRQ ENB	IRQ ENB	Data Bit 4
5	Data Bit 5	PE	1	DIR ②	Data Bit 5
6	Data Bit 6	$\overline{ACK}$	1	NC	Data Bit 6
7	Data Bit 7	BUSY	1	NC	Data Bit 7

① This bit is only available when the parallel port interrupt is PS/2 compatible (Mode Selection Register bit 2 is a 1), Otherwise the bit is always a 1.

② This bit is only available when the parallel port bus is PS/2 compatible (Mode Selection Register bit 1 is a 1).

TABLE 4-2. ACCESSIBLE PARALLEL PORT REGISTERS

18

4.1 READ PORT REGISTER

This register is used to read the data from the parallel bus.

Register select:
$\overline{CS2}$ asserted - $\overline{IOR}$ asserted - $\overline{IOW}$ de-asserted
Address A2 = X, A1-A0 = 0

7	6	5	4	3	2	1	0
Parallel Bus Data							

Bits 7-0

These bits correspond to the data on the parallel bus.

4.2 READ STATUS REGISTER

The contents of this register represents the status of the Parallel Port (refer to Table 4-2).

Register select:
$\overline{CS2}$ asserted - $\overline{IOR}$ asserted - $\overline{IOW}$ de-asserted
Address A2 = X, A1-A0 = 1

7	6	5	4	3	2	1	0
BUSY	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	$\overline{INT}$	1	1

Bit 7 - BUSY

Bit 6 - $\overline{ACK}$, Acknowledge

Bit 5 - PE, Parity Error

Bit 4 - SLCT, Select

Bit 3 - $\overline{ERROR}$

Bit 2 - $\overline{INT}$, Interrupt

$\overline{INT}$ represents the status of the Parallel Port's internal interrupt signal. This bit is only available when the parallel port interrupt is PS/2 compatible (Mode Selection Register bit 2 equals 1) otherwise it is a 1.

Bits 1, 0

These bits are set to one by the hardware.

4.3 READ CONTROL REGISTER

With the exception of DIR (bit 5), the contents of this read only register represents the status of the control signals capable of being set/reset by writing to the Write Control Register (refer to Table 4-2).

Register select:
$\overline{CS2}$ asserted - $\overline{IOR}$ asserted - $\overline{IOW}$ de-asserted
Address A2 = X, A1-A0 = 2

7	6	5	4	3	2	1	0
1	1	1	IRQ_ ENB	SLIN	$\overline{INIT}$	AFD	STB

Bits 7-5

These bits are set to one by the hardware.

Bit 4 - IRQ_ENB, Interrupt Request

IRQ represents the status of the Parallel Port Interrupt prior to the IRQ7 I/O Buffer.

Bit 3 - SLIN, Line Printer Select

Bit 2 - $\overline{INIT}$, Line Printer Initialize

Bit 1 - AFD, Line Printer Autofeed

Bit 0 - STB, Line Printer Strobe

4.4 WRITE PORT REGISTER

This register is used to write data to the parallel bus.

Register select:
$\overline{CS2}$ asserted - $\overline{IOR}$ de-asserted - $\overline{IOW}$ asserted
Address A2 = X, A1-A0 = 0

7	6	5	4	3	2	1	0
Parallel Bus Data							

Bits 7-0

These bits represent the data being written to the parallel bus.

4.5 WRITE CONTROL REGISTER

The Write Control Register is used to write to the associated lines and, with the exception of bit 5, is a duplicate of the Read Control Register (refer to Table 4-2).

Register select:
$\overline{CS2}$ asserted - $\overline{IOR}$ de-asserted - $\overline{IOW}$ asserted
Address A2 = X, A1-A0 = 2

7	6	5	4	3	2	1	0
NC	NC	DIR	IRQ_ ENB	SLIN	$\overline{INIT}$	AFD	STB

Bits 7, 6 - Not connected

Bit 5 - DIR, Direction

DIR works in conjunction with the BIDEN pin to determine the direction of the parallel port data bus (refer to Table 4-3). This bit is only available when the parallel port bus is PS/2 compatible (Mode Selection Register bit 1 is a 1).

Port Mode	Port Direction	Biden Pin 76	Direction Bit - 5	Compat-ability
Extended	Write *	1	0	PS/2
Extended	Write *	0	X	PS/2
Extended	Read *	1	1	PS/2
Compatible	Read *	1	N/A	PC/AT
Compatible	Write *	0	N/A	PC/AT

* Read and write refer to internal WD76C30 reading and writing the Parallel Port.

TABLE 4-3. PARALLEL PORT OPERATION MODES

Bit 4 - IRQ_ENB, Interrupt Request

IRQ represents the status of the Parallel Port Interrupt prior to the IRQ7 I/O Buffer.

Bit 3 - SLIN, Line Printer Select

Bit 2 - $\overline{INIT}$, Line Printer Initialize

Bit 1 - AFD, Line Printer Autofeed

Bit 0 - STB, Line Printer Strobe

18

5.0 INTERRUPT, CLOCK AND MODE SELECTION REGISTERS

The internal registers used for the interrupt multiplexing, clock selection and mode selection are accessed in a two step process, using two address locations in the Parallel Port Register. First, the address for the desired register to be accessed is written into the Address Select Register located at address three of the Parallel Port. Then the data to be read from or written to the selected register is accessed through the Data Access Register, located at address seven in the Parallel Port. It is not necessary for these write operations to follow each other.

5.1 ADDRESS SELECTION REGISTER

Register select - Read:
$\overline{CS2}$ asserted - $\overline{IOR}$ asserted - $\overline{IOW}$ de-asserted
Address A2-A0 = 3

Register select - Write:
$\overline{CS2}$ asserted - $\overline{IOR}$ de-asserted - $\overline{IOW}$ asserted
Address A2-A0 = 3

7	6	5	4	3	2	1	0
TEST BIT	SER_PRT_1 CLK		SER_PRT_0 CLK		DAT_ACC_REG		

Bit 7 - Testbit

The Testbit replaces the Serial 1, Serial 0 and Parallel Port interrupt signals to the internal interrupt multiplexer with the SLCT, BUSY and PE signals, respectively.

Bits 6, 5 - SER_PRT_1 CLK, Serial Port 1 Clock

These bits select the input clock used by serial port 1.

SER_PRT_1 CLK

6	5	Serial Port 1 Clock
0	0	1.8432 MHz
0	1	3.072 MHz
1	0	MSTRX1
1	1	8.0 MHz

Bits 4, 3 - SER_PRT_0 CLK, Serial Port 0 Clock

These bits select the input clock used for serial port 0.

SER_PRT_0 CLK

4	3	Serial Port 0 Clock
0	0	1.8432 MHz
0	1	3.072 MHz
1	0	MSTRX1
1	1	8.0 MHz

Bits 2-0 - DAT_ACC_REG, Data access register name

These bits select the address of the register to be accessed by the Data Access Register.

DAT_ACC_REG

2	1	0	Data Access Register Name	Reset Mode
0	0	0	Clock Select Reg.	00H
0	0	1	Clock Disable Reg.	00H
0	1	0	Serial Port 0 Int. Selection Reg.	00H
0	1	1	Serial Port 1 Int. Selection Reg.	00H
1	0	0	Parallel Port Int. Selection Reg.	00H
1	0	1	Mode Selection Reg.	00H

5.2 CLOCK SELECTION REGISTER

The Clock Selection Register is addressed by bits 2-0 of the Address Selection Register described in Section 5.1.

7	6	5	4	3	2	1	0
RESERVED					CLOCK CO-CPU		

Bits 7-3 - Reserved for future use and should be programmed to 0.

Bits 2-0 - CLOCK C0-CPU

These bits are used to select the desired frequency and duty cycle for supporting the 80287 coprocessor. Refer to Table 5-1 for the bit configurations.

B2	B1	B0	CLK287 FREQUENCY	COPROCESSOR SUPPORTED
0	0	0	8 MHz, 33% Duty Cycle	8 MHz Intel 80287 8 MHz AMD 80C287
0	0	1	9.6 MHz, 33% Duty Cycle	10 MHz Intel 80287 10 MHz AMD 80C287 10 MHz AMD 80EC287
0	1	0	12 MHz, 33% Duty Cycle	12 MHz AMD 80C287 12 MHz AMD 80EC287
0	1	1	12 MHz, 50% Duty Cycle	12 MHz Intel 80C287A
1	0	0	16 MHz, 33% Duty Cycle	16 MHz AMD 80C287 16 MHz AMD 80EC287
1	0	1	16 MHz, 50% Duty Cycle	Future Expansion
1	1	0	Logic Low	CLK287 Stopped low
1	1	1	Logic High	CLK287 Stopped high

TABLE 5-1. CLOCK SELECTION REGISTER

5.3 SLEEP MODE

For low power consumption, the internal oscillators may be individually disabled via the Clock Disable Register described in Section 5.4. For minimum power consumption, a sleep mode is offered which disables the 48 MHz clock, KBCLK, CLK287, ATCLK, Parallel Port (PD0 - 7), Data Bus (D0-7), all outputs, all pullups and, except for $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$ and $\overline{RESET}$, all inputs. Although KBCLK, CLK287, and ATCLK are disabled during sleep mode, their outputs are held low with small pulldown transistors.

Sleep Mode is activated by hardware asserting all three Selects ($\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$) simultaneously. All registers are preserved in the sleep mode. Sleep Mode is deactivated when one or more of the Select signals are de-asserted.

5.4 CLOCK DISABLE REGISTER

The Clock Disable Register is addressed by bits 2-0 of the Address Selection Register described in Section 5.1.

7	6	5	4	3	2	1	0
ISP1 CLK	ISP0 CLK			AT_ CLK	KB_ CLK	OSC_ DIS	

Bit 7 - ISP1 CLK, Internal Serial Port 1 Clock

ISP1 CLK = 0 -
Internal Serial Port 1 clock is not disabled.

ISP1 CLK = 1 -
Internal Serial Port 1 clock is disabled.

Bit 6 - ISP0 CLK, Internal Serial Port 0 Clock

ISP0 CLK = 0 -
Internal Serial Port 0 clock is not disabled.

ISP0 CLK = 1 -
Internal Serial Port 0 clock is disabled.

Bit 5, 4 - Reserved and should be programmed to 0.

Bit 3 - ATCLK

ATCLK = 0 -
ATCLK is not disabled.

ATCLK = 1 -
ATCLK signal is held at a logic low.

Bit 2 - KBCLK

KBCLK = 0 -
KBCLK is not disabled.

KBCLK = 1 -
KBCLK signal is held at a logic low.

18

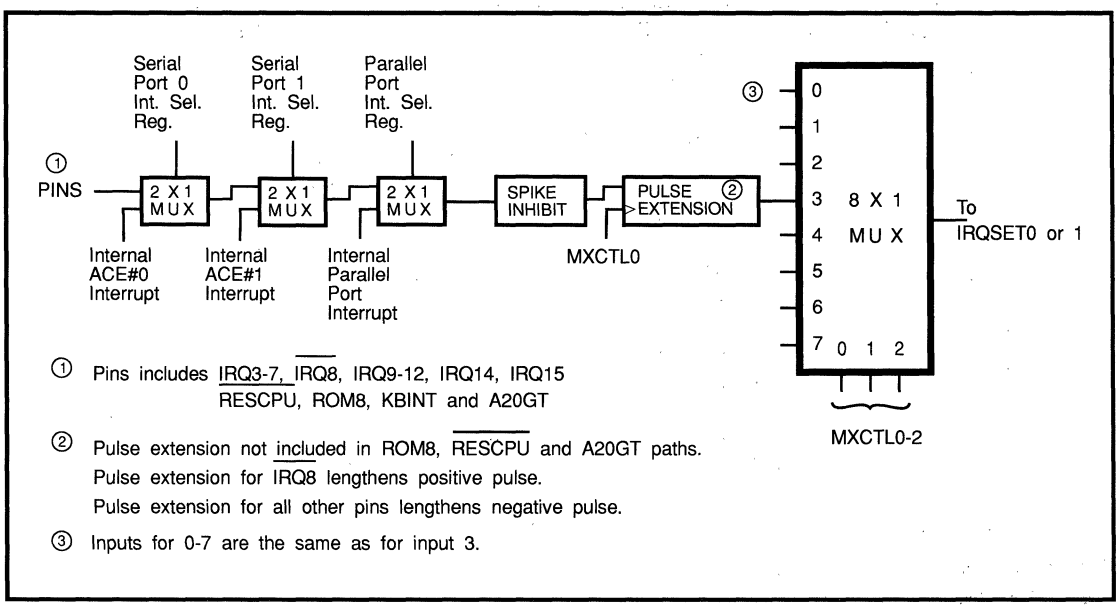


FIGURE 5-1. INTERRUPT MUX BLOCK DIAGRAM

Bit 1 - OSC_DIS, Oscillator Disable

OSC_DIS = 0 -
The 48 MHz oscillator is not disabled and, KBCLK, CLK287 and ATCLK are not frozen.

OSC_DIS = 0 -
The 48 MHz oscillator is disabled and, KBCLK, CLK287 and ATCLK are frozen.

Bit 0 - Reserved and should be programmed to 0.

NOTE

Asserting $\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$ simultaneously disables the 48 MHz oscillator. Upon removing the disabling of the 48 MHz oscillator, it restarts itself within 30 ms. Logic prevents the internal OSC Clock from starting again until the 48 MHz oscillator is running at full amplitude.

5.5 MODE SELECTION REGISTER

The Mode Selection Register is addressed by bits 2-0 of the Address Selection Register described in Section 5.1.

7	6	5	4	3	2	1	0
				PUD	ATPS2 INT	ATPS2 PP	SP FIFO

Bits 7-4 - Reserved and should be programmed to 0.

Bit 3 - PUD, Power-up Power-down

PUD must always be high when powering down the ports by turning off V_{DD}.

PUD = 0 -
The serial and parallel ports are in the power-up mode.

PUD = 1 -
The serial and parallel ports are in the power-down mode.

With the exception of addresses 011 and 111 of the parallel port, all registers are reset. Also the following signals are disabled: $\overline{DTR0}$, $\overline{DTR1}$, $\overline{RST0}$, $\overline{RST1}$, $\overline{SOUT0}$, $\overline{SOUT1}$, $\overline{PD0-7}$, $\overline{BIDEN}$, $\overline{ERROR}$, $\overline{SLCT}$, $\overline{PE}$, $\overline{ACK}$, BUSY, $\overline{INIT}$, $\overline{SLIN}$, $\overline{STB}$ AND $\overline{AFD}$.

Bit 2 - ATPS2_INT, PC/AT PS/2 Parallel Port Interrupt

ATPS2_INT = 0 -
The Parallel Port interrupt signal is compatible to a PC/AT compatible Parallel Port.

ATPS2_INT = 1 -
The Parallel Port interrupt signal is compatible to a PS/2 compatible Parallel Port.

Bit 1 - ATPS2_PP, PC/AT PS/2 Parallel Port

ATPS2_PP = 0 -
The Parallel Port Bus is configured as a PC/AT compatible Parallel Port.

ATPS2_PP = 1 -
The Parallel Port Bus is configured as a PS/2 compatible Parallel Port.

Bit 0 - SP_FIFO, Serial Port FIFO

SP_FIFO = 0 -
Both Serial Ports are configured to operate in non-FIFO mode.

SP_FIFO = 1 -
Both Serial Ports can operate in the FIFO mode if the applicable FEWO is set to 1.

5.6 INTERRUPT MULTIPLEXER

The WD76C30 provides the logic required to interface the PC/AT interrupt request lines with the WD76C10 Single Chip AT Controller. The WD76C10 generates input signals MXCTL2 - 0 and the WD76C30 uses these signals to select the IRQ inputs. Table 5-3 identifies the multiplexing sequence for the IRQSET0 and IRQSET1 signals. The output of the sampled IRQ inputs are provided on the IRQSET0 and IRQSET1 outputs (see Figure 5-1 IRQSET).

Negative pulse extension logic widens negative pulses on twelve of the sixteen MUX inputs. They are IRQ3-7, IRQ9-12, IRQ14,15 and KBINT. Positive pulse extension logic widens a positive pulse on IRQ8. The pulse width is extended by five positive going edges on MXCTL0 from the leading edge of the pulse or three positive going edges on MXCTL0 from the trailing edge of the pulse, whichever lasts longer. Note that pulses in the opposite direction that don't include three rising MXCTL0 edges are never seen on IRQSET0 or IRQSET1. None of this pulse extension logic applies to RESCPU, ROM8 or A20GT.

When the appropriate bits in the Serial Port 0 Interrupt Selection Register (see Section 5.7) are set to the Stand Alone Mode, the interrupt multiplexing logic is disabled. IRQSET0 and IRQSET1 are defined in Table 5-2. The Serial Port 0 Interrupt Selection Register and Serial Port 1 Interrupt Selection Register are used to assign Serial Port Interrupts to IRQ MUX inputs. The Parallel Port Interrupt Selection Register is used to assign the Parallel Port Interrupt to one IRQ MUX input.

IRQSET0 = Serial Port 0 Interrupt (tri-state enabled by Modem Control Register)

IRQSET1 = Serial Port 1 Interrupt (tri-state enabled by Modem Control Register)

IRQ7 = Parallel Port Interrupt (tri-state enabled by bit 4 of the parallel port Write Control Register)

TABLE 5-2. STAND ALONE MODE

MXCTL 2	1	0	IRQSET0
0	0	0	$\overline{\text{IRQ8}}$
0	0	1	IRQ9
0	1	0	IRQ10
0	1	1	IRQ11
1	0	0	ROM8
1	0	1	$\overline{\text{RESCPU}}$
1	1	0	IRQ14
1	1	1	IRQ15
MXCTL 2	**1**	**0**	**IRQSET1**
0	0	0	IRQ12
0	0	1	KBINT
0	1	0	A20GT
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

TABLE 5-3. MXCTL2 - 0 IRQSET0 - 1 MULTIPLEXING

18

5.7 SERIAL PORT 0 INTERRUPT SELECTION REGISTER

The Serial Port 0 Interrupt Selection Register is addressed by bits 2-0 of the Address Selection Register described in Section 5.1.

7	6	5	4	3	2	1	0
				SP0_INT_SEL			

Bits 7-4 - Reserved and should be programmed to 0.

Bits 3-0 - SP0_INT_SEL, Serial Port 0 Interrupt Select

These bits determine which IRQ MUX input is to be replaced by the internal Serial Port 0 Interrupt. The Stand Alone Mode may also be selected by these bits and applies to all ports.

Bits 4 and 3 of the Modem Control Register (refer to Section 3.10) must be set as follows:

EN = (MCR bit 4 = 0 • bit 3 = 1)

EN	B3	B2	B1	B0	Serial Port 0 Interrupt Selection
X	0	0	0	0	Disabled
1	0	0	0	1	IRQ3
1	0	0	1	0	IRQ4
1	0	0	1	1	IRQ5
1	0	1	0	0	IRQ6
1	0	1	0	1	IRQ7
1	0	1	1	0	IRQ10
1	0	1	1	1	IRQ11
1	1	0	0	0	ROM8
1	1	0	0	1	IRQ15
X	1	1	1	1	Stand Alone Mode

All other combinations are reserved.

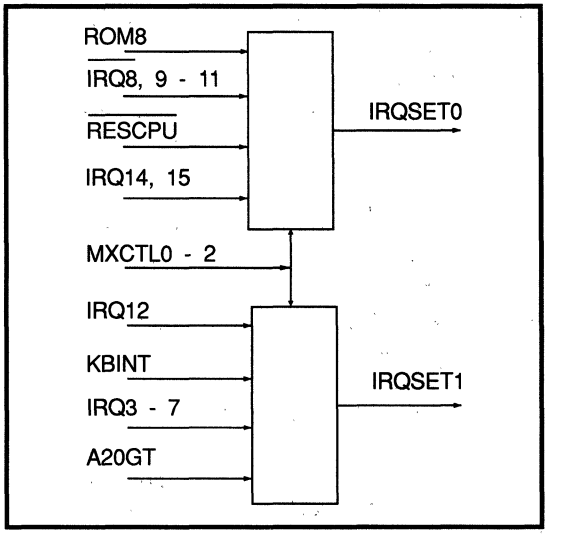


FIGURE 5-2. IRQSET - WHEN NOT IN STAND ALONE MODE

5.8 SERIAL PORT 1 INTERRUPT SELECTION REGISTER

The Serial Port 1 Interrupt Selection Register is addressed by bits 2-0 of the Address Selection Register described in Section 5.1.

7	6	5	4	3	2	1	0
				SP1_INT_SEL			

Bits 7-4 - Reserved and should be programmed to 0.

Bits 3-0 - SP1_INT_SEL, Serial Port 1 Interrupt Select

These bits determine which IRQ MUX input is to be replaced by the internal Serial Port 1 Interrupt.

Bits 4 and 3 of the Modem Control Register (refer to Section 3.10) must be set as follows:

EN = (MCR bit 4 = 0 • bit 3 = 1)

EN	B3	B2	B1	B0	Serial Port 1 Interrupt Selection
X	0	0	0	0	Disabled
1	0	0	0	1	IRQ3
1	0	0	1	0	IRQ4
1	0	0	1	1	IRQ5
1	0	1	0	0	IRQ6
1	0	1	0	1	IRQ7
1	0	1	1	0	IRQ10
1	0	1	1	1	IRQ11
1	1	0	0	0	ROM8
1	1	0	0	1	IRQ15

All other combinations are reserved.

NOTE

The Serial Port 1 Interrupt Selection Register has priority over the Serial Port 0 Interrupt Selection Register. That is, Serial Port 1 interrupt replaces the Serial Port 0 interrupt when both registers select the same interrupt. The interrupts are not ORed.

5.9 PARALLEL PORT INTERRUPT SELECTION REGISTER

The Parallel Port Interrupt Selection Register is addressed by bits 2-0 of the Address Selection Register described in Section 5.1.

7	6	5	4	3	2	1	0
				PP_INT_SEL			

Bits 7-4 - Reserved and should be programmed to 0.

Bits 3-0 - PP_INT_SEL, Parallel Port Interrupt Select

These bits determine which IRQ MUX input is to be replaced by the internal Parallel Port Interrupt.

Bit 4 of the Parallel Port Write Control Register (refer to Section 4.5) must be set as follows:

EN = (WCR bit 4 = 1)

EN	B3	B2	B1	B0	Parallel Port Interrupt Selection
X	0	0	0	0	Disabled
1	0	0	0	1	IRQ3
1	0	0	1	0	IRQ4
1	0	0	1	1	IRQ5
1	0	1	0	0	IRQ6
1	0	1	0	1	IRQ7
1	0	1	1	0	IRQ10
1	0	1	1	1	IRQ11
1	1	0	0	0	ROM8
1	1	0	0	1	IRQ15

All other combinations are reserved.

NOTE

The Parallel Port Interrupt Selection Register has priority over both of the Serial Port Interrupt Selection Registers. That is, the Parallel Port interrupt replaces the Serial Port 0 or 1 interrupt when the registers select the same interrupt. The interrupts are not ORed.

18

6.0 ELECTRICAL SPECIFICATIONS

6.1 MAXIMUM RATINGS

Temperature Under Bias ..... 0°C (32°F) to 70°C (158°F)

Storage Temperature ..... -65°C (-85°F) to +150°C (302°F)

All Input or Output Voltages with respect to Vss ..... -0.5V to +7.0V

Power Dissipation ..... 300 mW

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Operating Characteristics.

6.2 CAPACITANCE

Ta = 25°C (77°F), f = 1.0 MHz, VccA = 5.0V, VccB = 5.0V, Vss = 0V

SYMBOL	CHARACTERISTIC	TYP.	MAX.	UNITS	TEST CONDITIONS
Cxin	Clock Input Capacitance	15	20	pF	fc = 1 MHz
Cxout	Clock Output Capacitance	20	30	pF	
Cin	Input Capacitance	6	10	pF	Unmeasured Pins Returned to Vss
Cout	Output Capacitance	10	20	pF	Unmeasured Pins Returned to Vss

TABLE 6-1 CAPACITANCE

6.3 DC OPERATING CHARACTERISTICS

Ta = 0°C (32°F) to =70°C (158°F), V_{DD} = +5V ± 10%, $V_{DD}2$ = +5V ±10%,
Vss = 0V, unless otherwise specified.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
Vilx	Clock Input Low Voltage			V	
Vihx	Clock Input High Voltage			V	
Vil	Input Low Voltage	-0.5	0.8	V	
Vih	Input High Voltage	2.0	Vcc	V	
Vol	Output Low Voltage		0.4	V	Iol = 4.0 mA on DB0-DB7. Iol = 24 mA on PD0-PD7. Iol = 20 mA on INIT, STB ,SLIN, AFD ① Iol = 2.0 mA on other outputs.
Voh	Output High Voltage	2.4		V	Ioh = -0.4 mA on DB0-DB7. Ioh = -15.0 mA on PD0-PD7. Ioh = -0.55 mA on INIT, AFD, STB, SLIN. Ioh = -0.2 mA on other outputs.
Icc	Power Supply Current		60	mA	Vcc = 5.5V MSTRX1 = 48 MHz All other inputs = 5.5V. All outputs floating Baud Rate = 512K. Serial Port CLK = 8 MHz.
Iil ②	Input Leakage		æ15	µA	Vcc = 5.5V, Vss = 0.0V. All other pins float.
Icl	Clock Leakage				Vin = 0.0V, 5.5V.
Idl	Data Bus Leakage (DB and PD)		±10	µA	Vout = 0.4V, Vout = 4.5V Data Bus in High Impedance State.
Ioz	Tri-State Leakage		± 20	µA	Vcc = 5.5V, GND = 0V, Vout = 0.0V, 5.5V.
Vil (RES)	Reset Schmitt Vil		0.8	V	
Vih (RES)	Reset Schmitt Vih	2.0		V	

TABLE 6-2. DC OPERATING CHARACTERISTICS

① The SLIN, AFD, STB and INIT outputs are all open collector with 2.5K to 3.5K Ohms internal pull-up resistors. In PS/2 mode IRQ7 is also an open collector. When in Vol state, each input sinks a minimum of 10 mA.

② RESCPU, IRQ3 - 7, IRQ8, IRQ9 - 12, IRQ14 - 15, ROM8, A20GT, KBINT, AND CS1 have nominally 300 µA pullups. These pullups, along with all others, are disabled when the 48 MHz oscillator is disabled by asserting CS0, CS1, and CS2 simultaneously. The pulldowns on KBCLK, ATCLK, and CLK287 are enabled when the three chip selects are low and nominally sink 300 µA.

18

6.4 AC OPERATING CHARACTERISTICS AND TIMING

Ta = 0°C (32°F) to +70°C (158°F), Vss = +5V ± 10%, $V_{DD}2$ = +5V ±10%,
Table 6-1 lists the timing categories and their Figure and Table number.

FIGURE NUMBER	TABLE NUMBER	FIGURE TITLE
6-1	6-4	Receiver Timing
6-2	6-5	Transmitter Timing
6-3	6-6	MODEM Control Timing
6-4	6-7	Read Cycle Timing
6-5	6-7	Write Cycle Timing
6-6	6-4	RCVR FIFO Signaling Timing for First Byte
6-7	6-4	RCVR FIFO Signaling Timing after First Byte (RBR already set)
6-8	6-8	Parallel Port Timing
6-9	6-8	Parallel Port Interrupt Timing
6-10	6-9	Clock Generation Timing
6-11	6-10	Interrupt MUX Timing (A)
6-12	6-10	Interrupt MUX Timing (B)

TABLE 6-3. TIMING FIGURE/TABLE NUMBERS

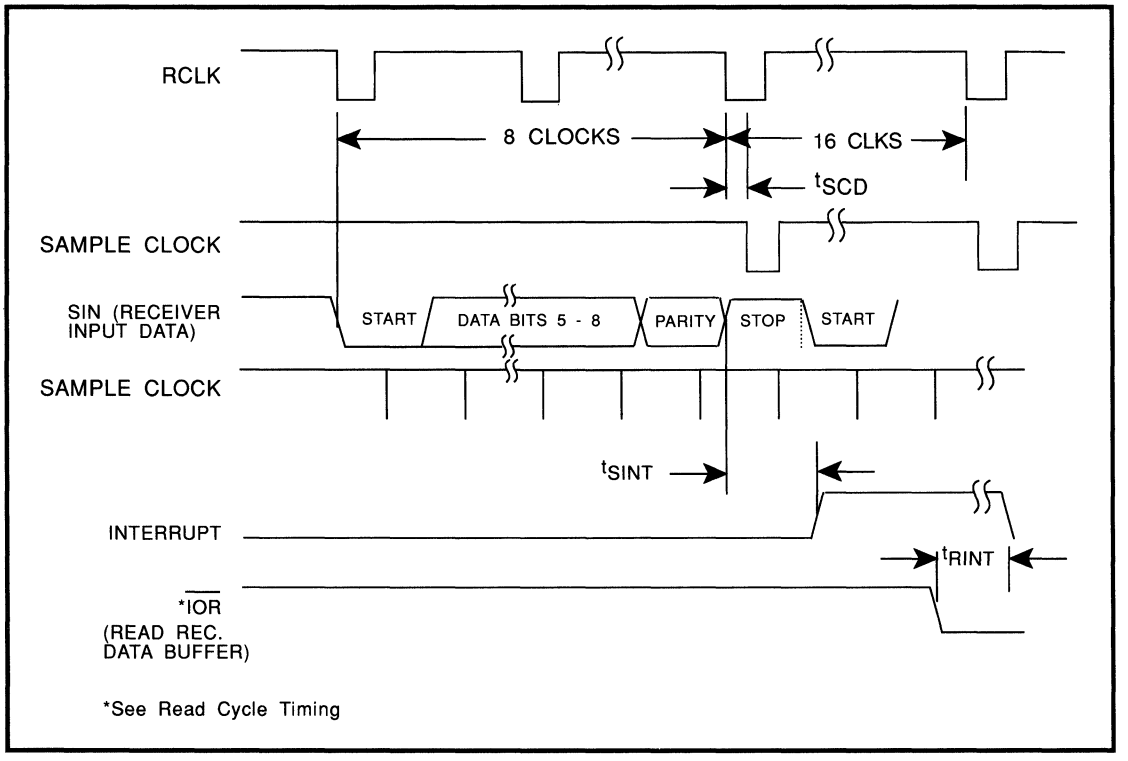


FIGURE 6-1. RECEIVER TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
tSCD	Delay from RCLK† to Sample Time		2	µs	
tSINT	Delay from Stop to Set Interrupt		17 ①	RCLK ② Cycles	100 pF Load
tRINT	Delay from $\overline{IOR}$ (RD RBR) Reset Interrupt	250	1000	ns	100 pF Load

TABLE 6-4. RECEIVER TIMING

18

① When receiving the first byte in FIFO Mode, tSINT (only for timeout or trigger level interrupt) will be delayed 19 RCLK cycles, except for a timeout interrupt where tSINT will be delayed 24 RCLK cycles.

② RCLK is an internal clock used for sampling serial in data. RCLK is equivalent to 16 times the baud rate clock.

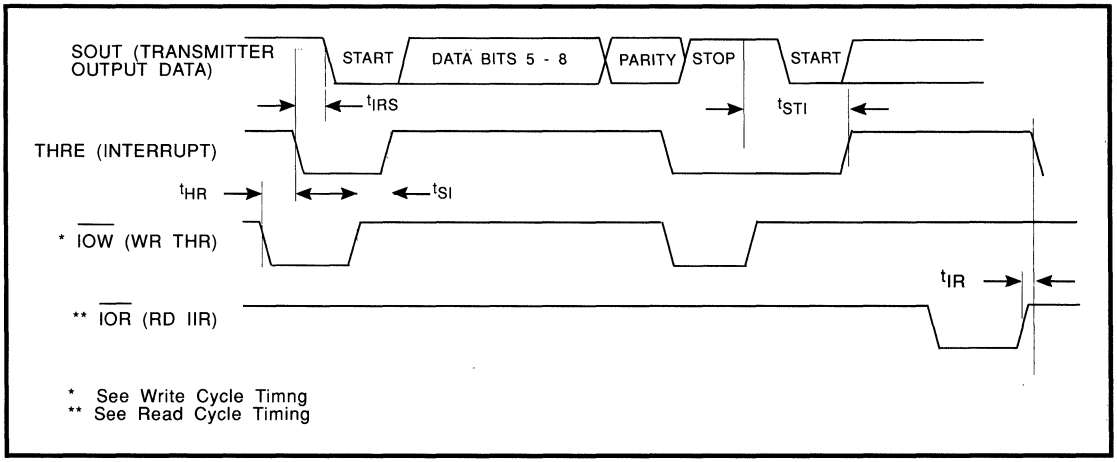


FIGURE 6-2. TRANSMITTER TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
tHR	Delay from IOW (WR THR) to Reset Interrupt		175	ns	100 pF Load
tIRS	Delay from initial INTR Reset to Transmit start	8	24	TCLK ① Clock Cycles	
tSI ②	Delay from Initial Write to Interrupt	16	24	TCLK ① Clock Cycles	
tSTI	Delay from Stop to Interrupt (THRE)	8	8	TCLK ① Clock Cycles	
tIR	Delay from IOR (RD IIR to Reset Interrupt (THRE)		250	ns	100 pF Load
tSXA	Delay from Start to TXRDY Active	0	8	TCLK ① Clock Cycles	
tWXI	Delay from Write to TXRDY Inactive	0	300	ns	

TABLE 6-5. TRANSMITTER TIMING

① TCLK is an internal clock used for sending serial out data. TCLK is equivalent to 16 times the baud rate clock.

② In FIFO mode tSI might extend to beginning of Stop Bit. See Line Status Register for details.

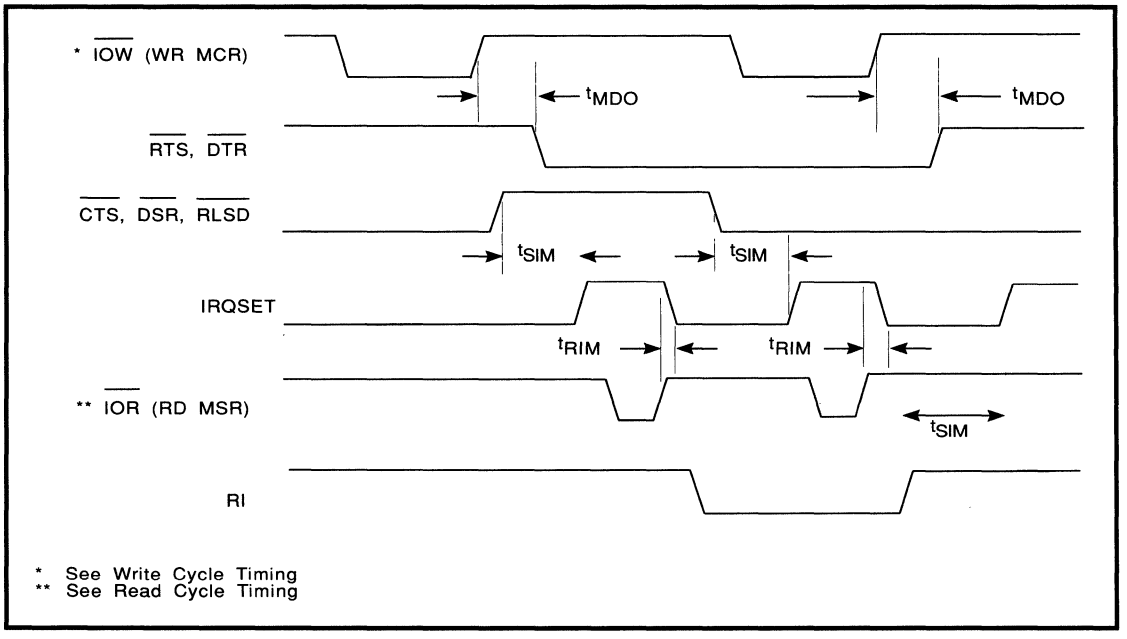


FIGURE 6-3. MODEM CONTROL TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
tMDO	Delay from IOW (WR MCR) to Output		200	ns	100 pF Load
tSIM	Delay to Set Interrupt from MODEM Input		250	ns	100 pF Load
tRIM	Delay to Reset Interrupt from IOR (RD MSR)		250	ns	100 pF Load

TABLE 6-6. MODEM CONTROL TIMING

18

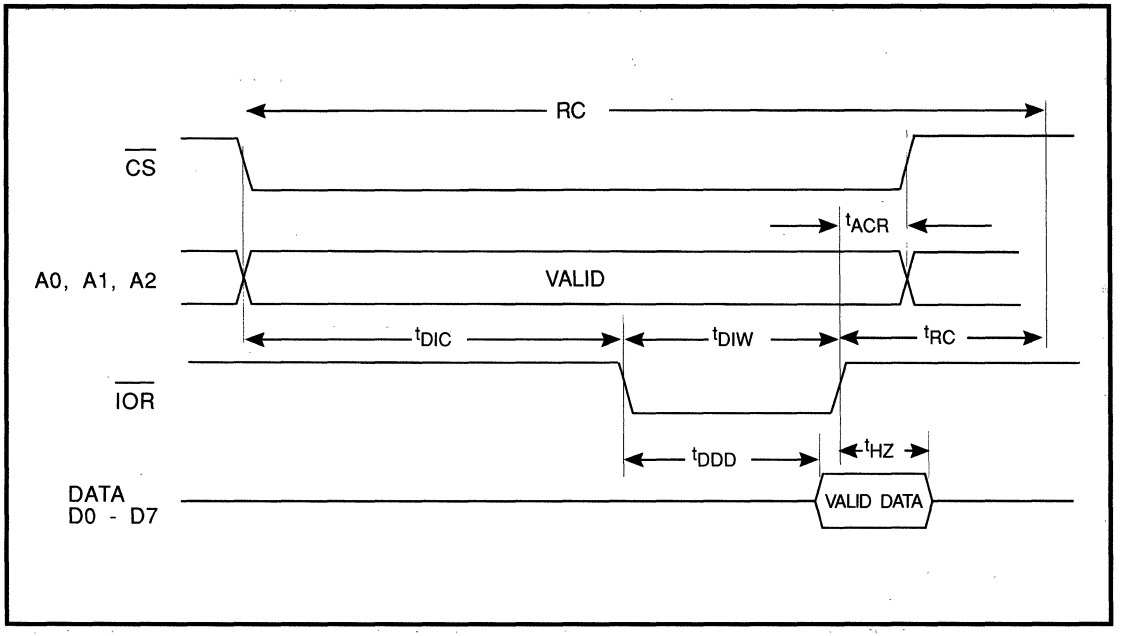


FIGURE 6-4. READ CYCLE TIMING

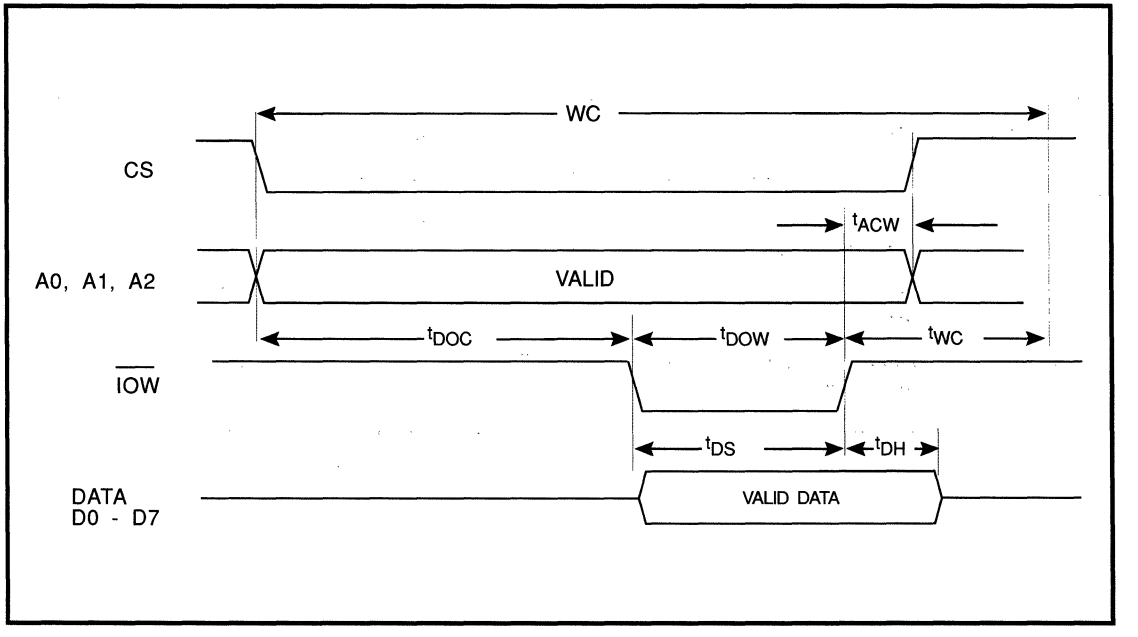


FIGURE 6-5. WRITE CYCLE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
t_{DIW}	$\overline{IOR}$ Strobe Width	125		ns	1TTL Load
t_{RC}	Read Cycle Delay	125		ns	1TTL Load
RC	Read Cycle = $t_{DIC} + t_{DIW} + t_{RC}$ + 20 ns	300		ns	1TTL Load
t_{HZ}	$\overline{IOR}$ to Floating Data Delay	0	100	ns	1TTL Load
t_{DOW}	$\overline{IOW}$ Strobe Width	100		ns	1TTL Load
t_{WC}	Write Cycle Delay	150		ns	1TTL Load
WC	Write Cycle = + t_{DOC} + t_{DOW} + t_{WC} + 20 ns	300		ns	1TTL Load
t_{DS}	Data Setup Time	30		ns	1TTL Load
t_{DH}	Data Hold Time	30		ns	1TTL Load
t_{DIC}	$\overline{IOR}$ DELAY from Select or Address	30		ns	1TTL Load
t_{DOC}	$\overline{IOW}$ Delay from Select or Address	30		ns	1TTL Load
t_{ACR}	Address and Chip Select Hold Time from $\overline{IOR}$	20		ns	1TTL Load
t_{ACW}	Address and Chip Select Hold Time from $\overline{IOW}$	20		ns	1TTL Load
t_{DDD}	Delay from $\overline{IOR}$ to data		100	ns	1 TTL Load
t_{MR}	Master Reset Pulse Width	1.0		µs	1 TTL Load
t_{PWRUP}	Delay from TTL Clock in to internal clock on power up.		30	µs	
t_{OSCUP}	Delay from OSC clock in to internal clock on power up.		30	ms	

TABLE 6-7. READ/WRITE CYCLE TIMING

18

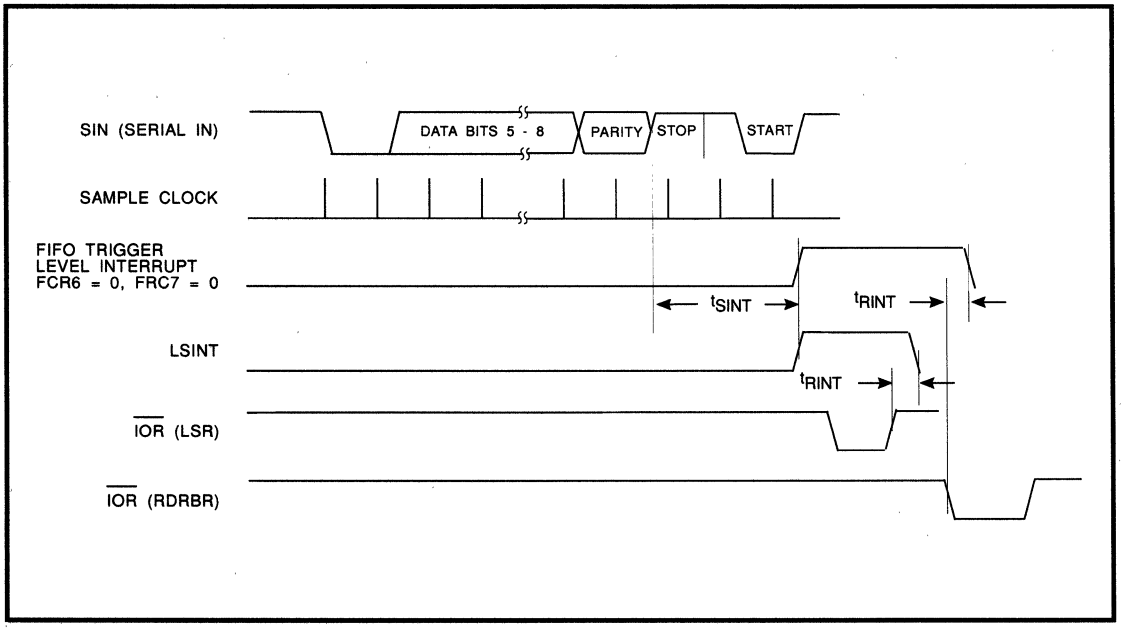


FIGURE 6-6. RCVR FIFO SIGNAL TIMING FOR FIRST BYTE

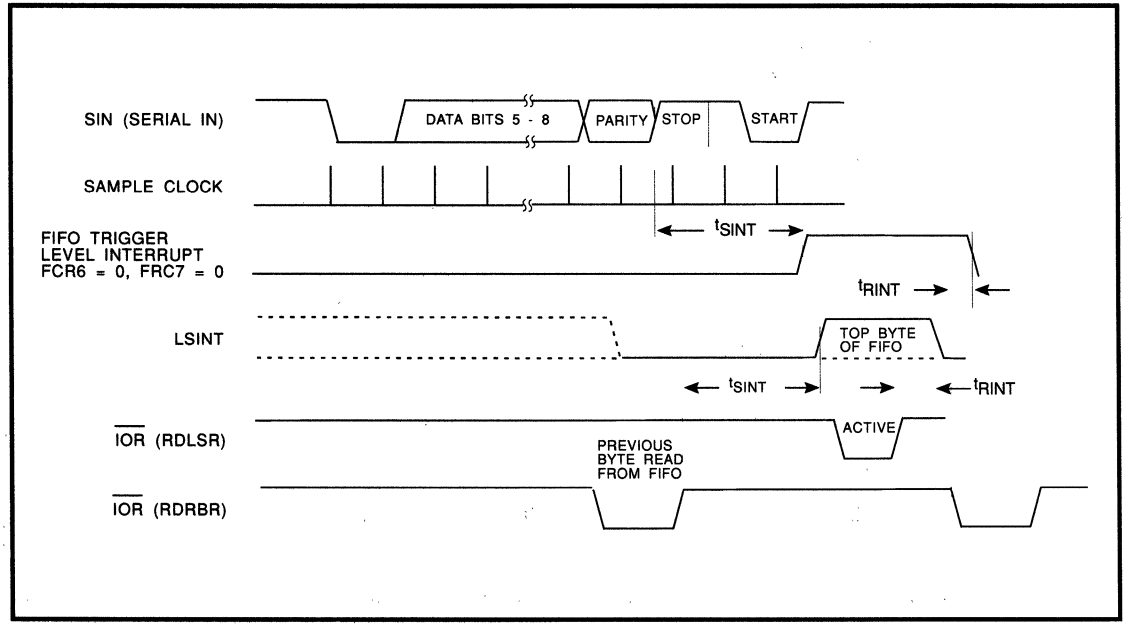


FIGURE 6-7. RCVR FIFO SIGNAL TIMING AFTER FIRST BYTE (RBR ALREADY SET)

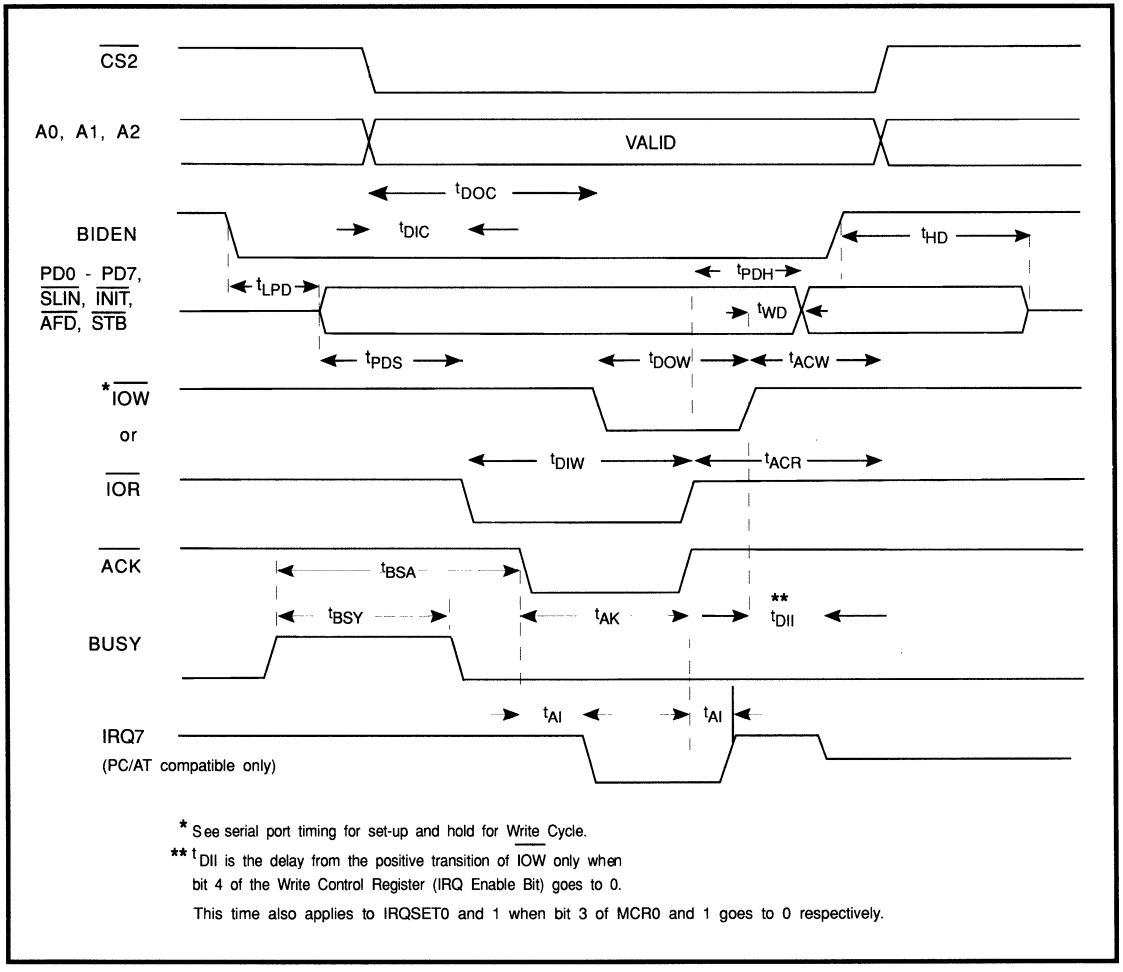


FIGURE 6-8. PARALLEL PORT TIMING

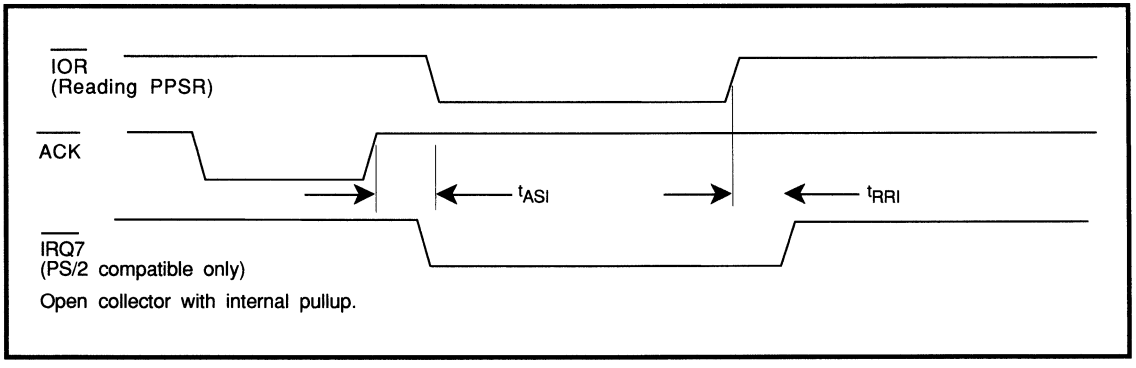


FIGURE 6-9. PARALLEL PORT INTERRUPT TIMING

18

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
t_{DOC}	$\overline{IOW}$ Delay from Chip Select and Address	30		ns	
t_{DIC}	$\overline{IOR}$ Delay from Chip Select and Address	30		ns	
t_{WD}	$\overline{IOW}$ High to PD0-PD7, $\overline{SLIN}$, $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$		1	µs	No External Pull-up Resistor and 50 pF Load
t_{HD}	BIDEN High to PD0-PD7 Tri-State		120	ns	50 pF Load
t_{LPD}	BIDEN Low to PD0-PD7 Delay		100	ns	50 pF Load
t_{PDH}	PD0-PD7 Hold Time from $\overline{IOR}$	100		ns	
t_{PDS}	PD0-PD7 Set-up Time from $\overline{IOR}$	100		ns	
t_{DOW}	$\overline{IOW}$ Strobe Width	100		ns	
t_{DIW}	$\overline{IOR}$ Strobe Width	125		ns	
t_{ACW}	Chip Select and Address Hold Time from $\overline{IOW}$	20		ns	
t_{ACR}	Chip Select and Address Hold Time from $\overline{IOR}$	20		ns	
t_{BSA}	BUSY Start to $\overline{ACK}$	0		ns	
t_{BSY}	BUSY Width	100		ns	
t_{AK}	$\overline{ACK}$ Width	100		ns	
t_{AI}	IRQ7 Delay from $\overline{ACK}$		60	ns	50 pF Load
tASI	$\overline{ACK}$ to set interrupt		60	ns	50 pF Load
t_{RRI}	Read Parallel Port Status Register (PPSR)		60	ns	50 pF Load
t_{DII}	$\overline{IOW}$ to Tri-State	0	100	ns	50 pF Load

TABLE 6-8. PARALLEL PORT TIMING

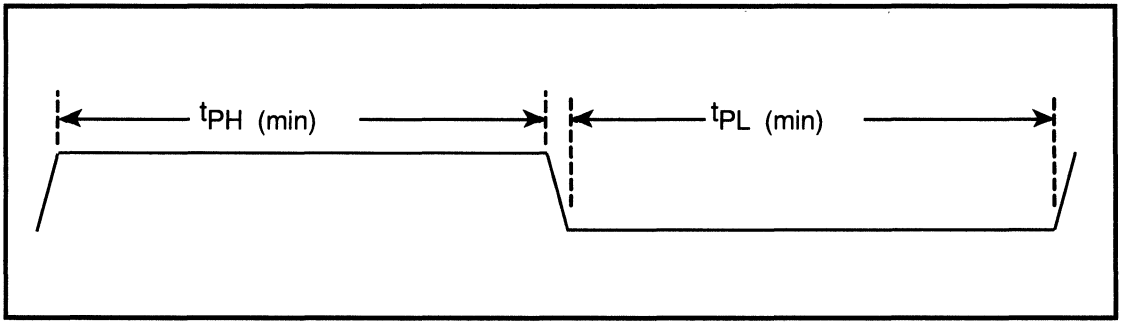


FIGURE 6-10. CLOCK GENERATION TIMING

CLOCK TYPE	tPH min. ns.	tPL min. ns.	FREQUENCY MHz	MAX. EDGE DELAY ① FROM MSTRX1 EDGE
CLK287 SEL				
0	43	68	8	100 ns
1	28	62	9.6	100 ns
2	22	50	12	100 ns
3	35	35	12	100 ns
4	17	37	16	100 ns
5	25	25	16	100 ns
KBCLK	50	33	9.6	100 ns
ATCLK	28	28	16	100 ns
MSTRX1	8	8	48	N/A

TABLE 6-9. CLOCK GENERATION TIMING

① All 50 pF loads

18

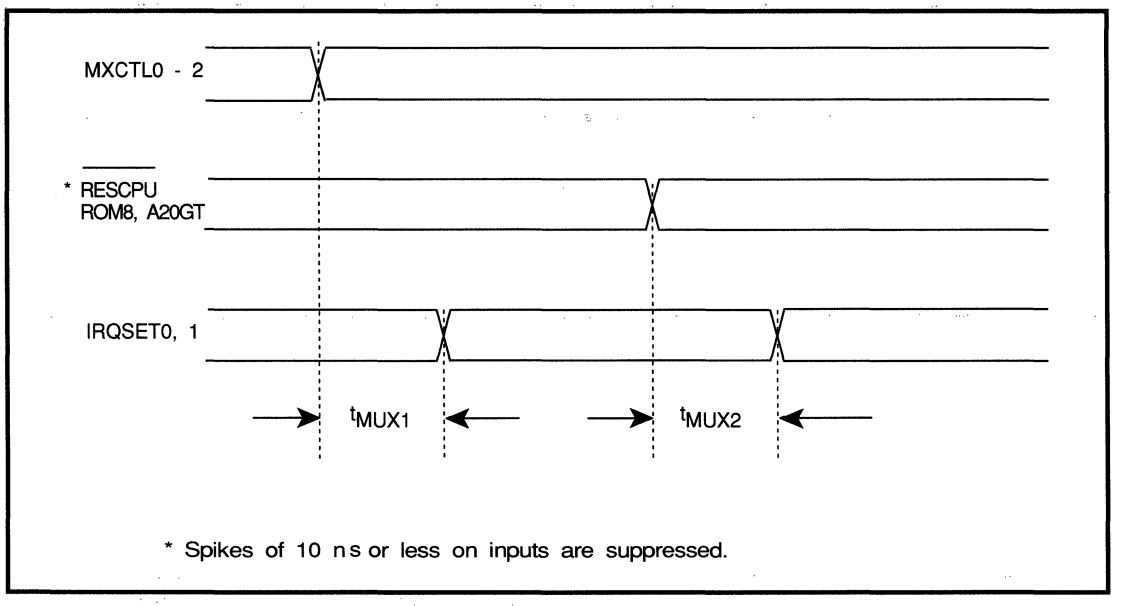


FIGURE 6-11. INTERRUPT MUX TIMING - A

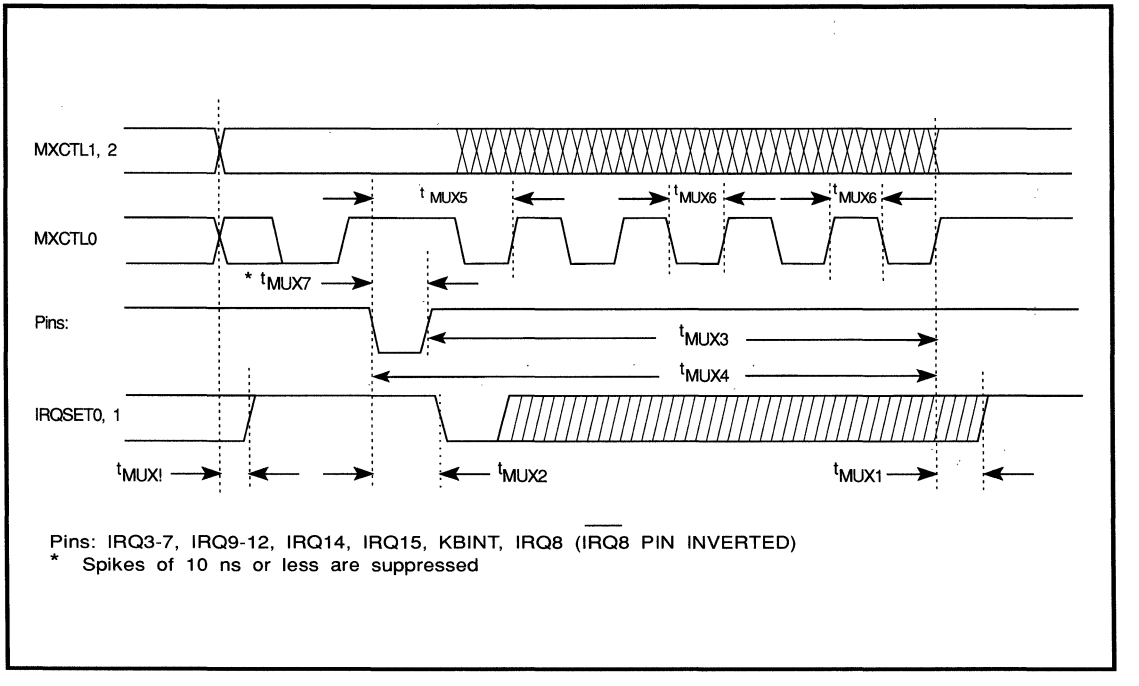


FIGURE 6-12. INTERRUPT MUX TIMING - B

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
$^tMUX1$	Delay from MUX control change		25	ns	50 pF load
$^tMUX2$	Delay from MUX input going low		125	ns	50 pF load
$^tMUX3$	Rising MXCTL0 clock edges required	3	5		
$^tMUX4$	Rising MXCTL0 clock edges required	5			
$^tMUX5$	MUX input setup time	100		ns	
$^tMUX6$	MXCTL0-2 pulse width	40		ns	
$^tMUX7$	Pins pulse width	75		ns	

TABLE 6-10. INTERRUPT MUX TIMING

7.0 PACKAGE DIMENSIONS

Figure 7-1. Illustrates the 84-Pin PLCC package showing the dimensions in inches.
Figure 7-2. Illustrates the 84-Pin PQFP package showing the dimensions in inches.

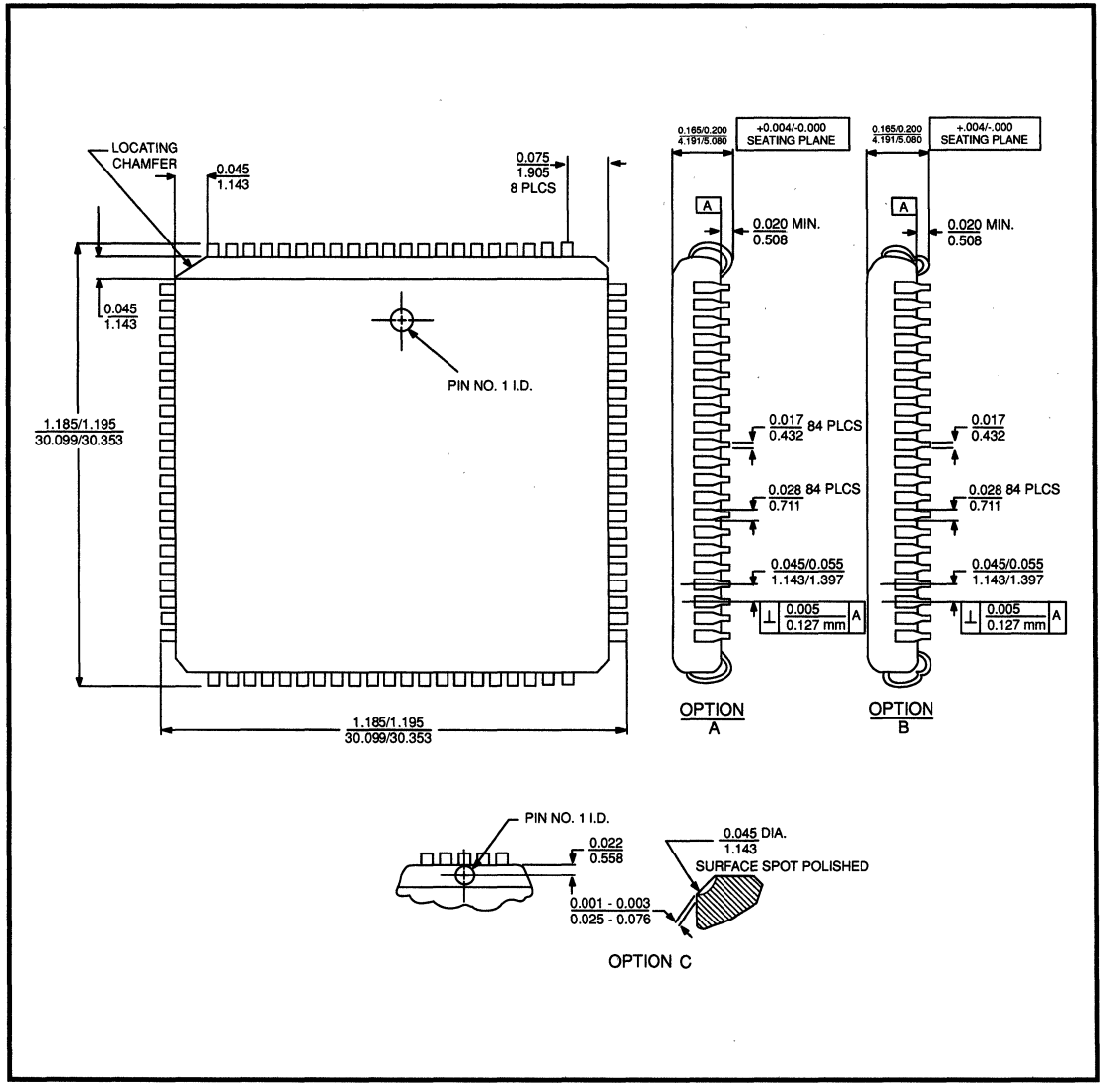


FIGURE 7-1. 84-PIN PLCC PACKAGE

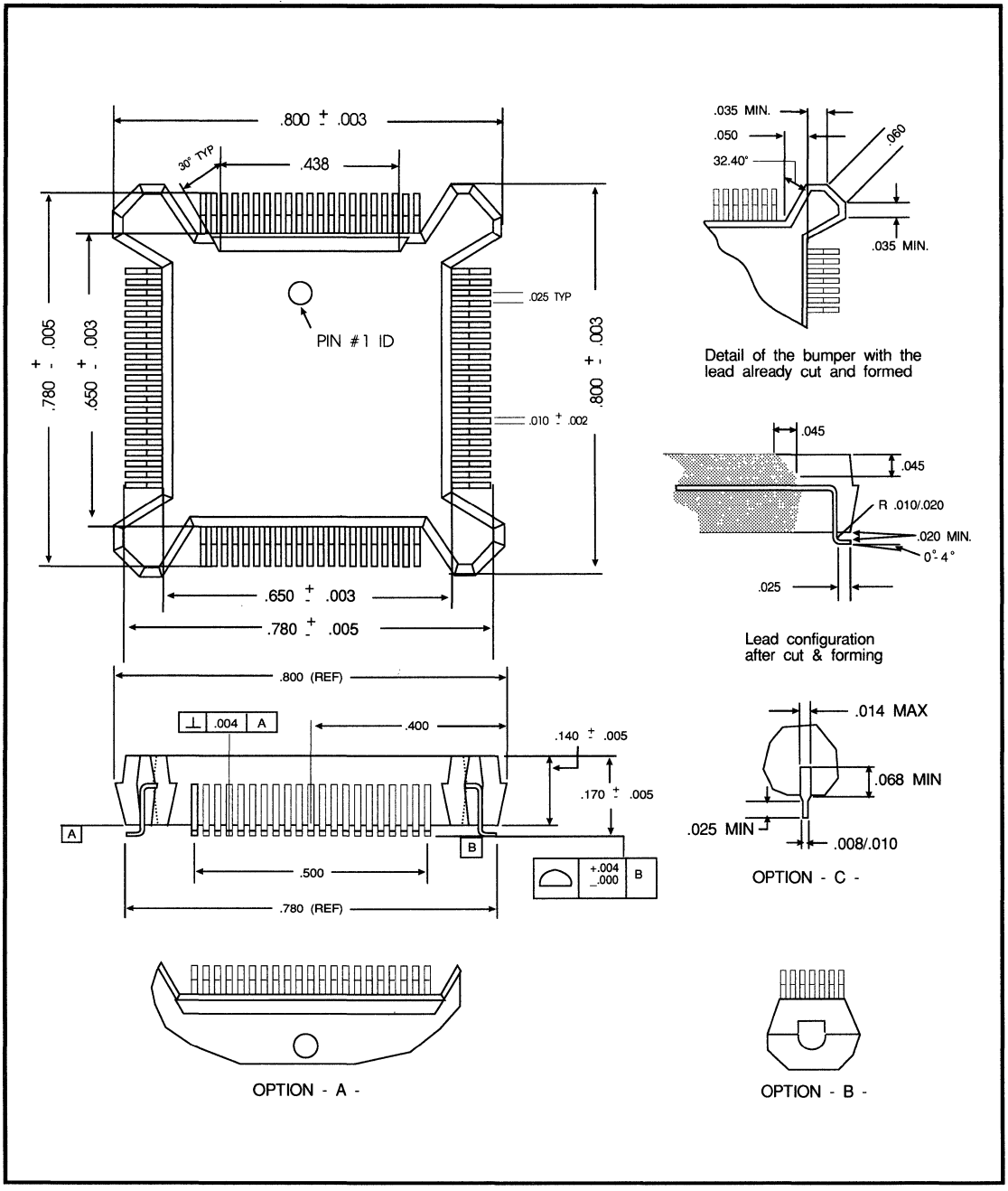


FIGURE 7-2. 84-PIN PQFP PACKAGE

8.0 CRYSTAL MANUFACTURES (Partial List)

American Time Products Division
Frequency Control Products, Inc.
Woodside, New York 11377

Bliley Electric Company
Eire, Pennsylvania 16508

Cryster Crystals
Whitby, Ontario

Erie Frequency Control
Carlisle, Pennsylvania 17013

Q-Matic Corporation
Costa Mesa, California 92626

8.1 CRYSTAL SPECIFICATIONS

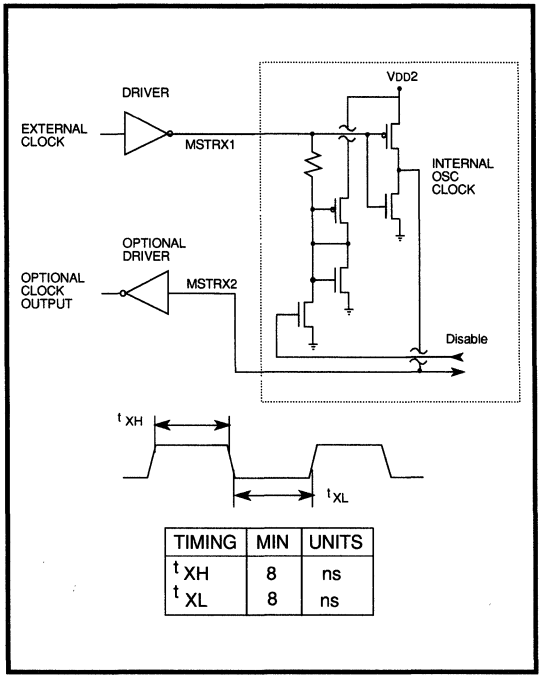
Frequency: 16.0 MHz (third overtone = 48 MHz)

Type: Microprocessor Crystal

Temperature Range: 0°C (32°F) to 70°C (158°F)

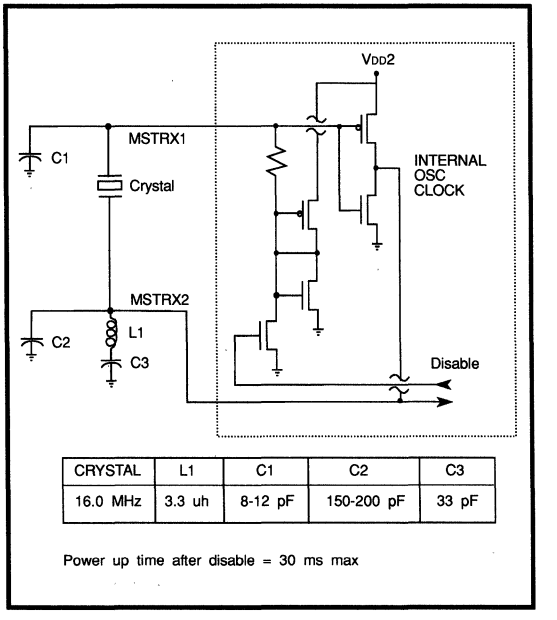
Series Resistance: 50 Ohms to 75 Ohms
(16.0 MHz)

Series Resonant
Overall Tolerance: ±0.01%



TIMING	MIN	UNITS
tXH	8	ns
tXL	8	ns

FIGURE 8-1. EXTERNAL CLOCK INPUT (48 MHz MAX.)



CRYSTAL	L1	C1	C2	C3
16.0 MHz	3.3 uh	8-12 pF	150-200 pF	33 pF

Power up time after disable = 30 ms max

FIGURE 8-2. TYPICAL CRYSTAL OSCILLATOR NETWORK

PVGA1A

Video Graphics Array Device

WESTERN DIGITAL

TABLE OF CONTENTS

19

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

1.1 DESCRIPTION

The Paradise Video Graphics Array (PVGA1A) is designed to enhance the VGA subsystem in IBM PC AT Bus or Personal System 2 (PS/2) Micro Channel compatible applications. The AT or Micro Channel Bus interface switch is set through the Configuration Register after power up.

Other improvements, such as an 8/16 bit wide CPU data path, a DRAM controller for up to 1 MB of video memory space, support for an 8/16 bit wide BIOS ROM data path, auto monitor detect input, and a CRT controller for fixed or variable scan analog monitors, are offered as standard features.

1.2 FEATURES

- Provides single Chip Video Graphics Solution for IBM PC / XT / AT and Personal System/2 compatible systems
- 100% hardware compatible with IBM's VGA card in all modes
- 100% IBM VGA and EGA BIOS compatible
- 100% CGA, MDA, Hercules Graphics, AT&T Model 6300 compatible
- Integrated bus interface for PC / XT / AT, Micro Channel
- High performance FIFO memory architecture
- Includes 8- or 16-bit wide CPU data bus
- 800 by 600 by 16 colors, 640 x 400 x 256 colors
- 640 by 480 by 256 colors (512K DRAM)
- 132 column text modes, with 25, 43, or 50 rows
- Support for external Color Lookup Table (Palette Chip) with 256 Kbyte available colors
- Up to 40 MHz maximum video clock rate
- 1.25 Micron CMOS VLSI technology
- 100 pin Plastic Leadless Chip Carrier (PLCC), or 100 pin Plastic Flat Pack (PFP) JEDEC package
- Minimizes circuit board space requirements.

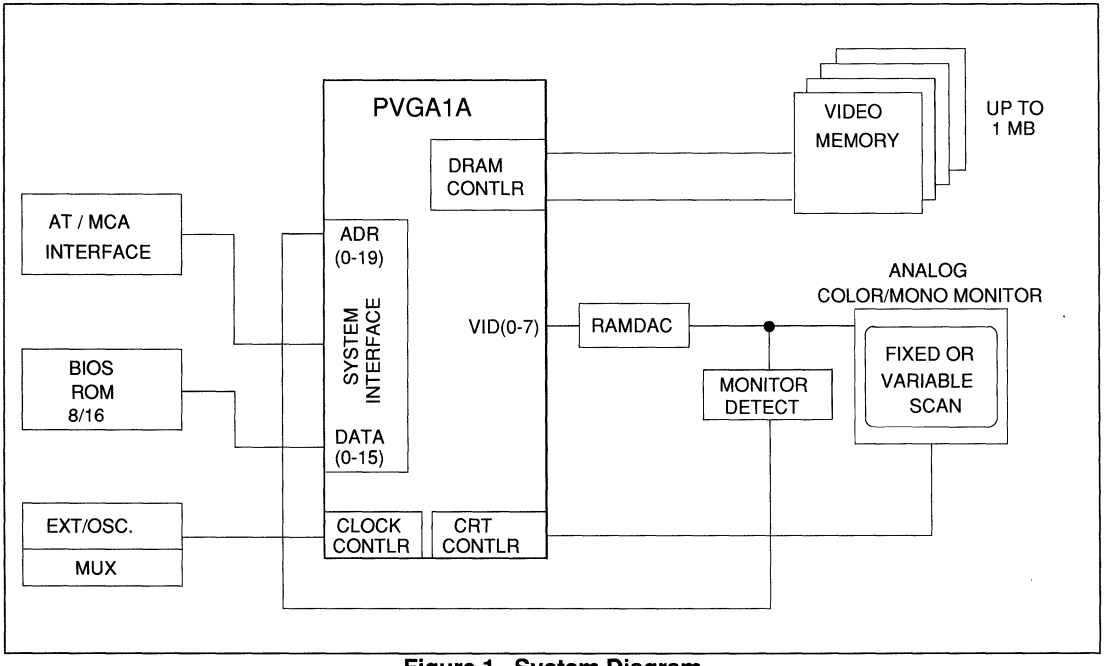
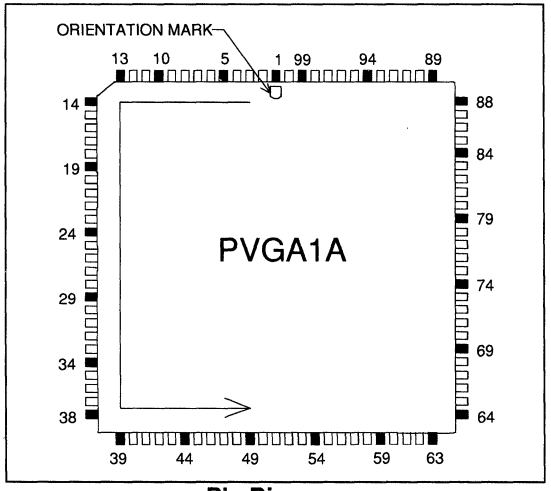
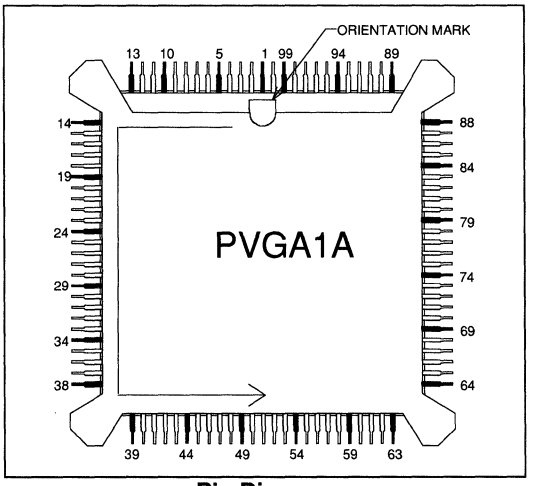


Figure 1. System Diagram

19



Pin Diagram



Pin Diagram

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	GND	26	GND	51	GND	76	MCLK
2	MD4	27	A18	52	VCC	77	GND
3	MD3	28	A19	53	VID4	78	VCC
4	MD2	29	IORN	54	VID3	79	RAS10N
5	MD1	30	IOWN	55	VID2	80	CAS10N
6	MD0	31	MRDN	56	VID1	81	OE10N
7	EBROMN	32	MWRN	57	VID0	82	RAS32N
8	DS16N	33	EION	58	WPLTN	83	CAS32N
9	BHEN	34	RDY	59	PCLK	84	OE32N
10	SFDBKN	35	IRQ	60	HSYNC	85	WE0N
11	EABUFN	36	RSET	61	VSYNC	86	WE1N
12	DA8	37	DIR	62	BLNKN	87	WE2N
13	DA9	38	EDBUFN	63	MA8	88	WE3N
14	DA10	39	DA0	64	GND	89	MD15
15	GND	40	DA1	65	MA7	90	MD14
16	DA11	41	DA2	66	MA6	91	MD13
17	DA12	42	DA3	67	MA5	92	MD12
18	DA13	43	DA4	68	MA4	93	MD11
19	DA14	44	DA5	69	MA3	94	MD10
20	DA15	45	DA6	70	MA2	95	MD9
21	EMEM	46	DA7	71	MA1	96	MD8
22	A15	47	RPLTN	72	MA0	97	MD7
23	A16	48	VID7	73	VCLK2	98	MD6
24	A17	49	VID6	74	VCLK1	99	MD5
25	VCC	50	VID5	75	VCLK0 1	00	VCC

PVGA1A Pin Descriptions

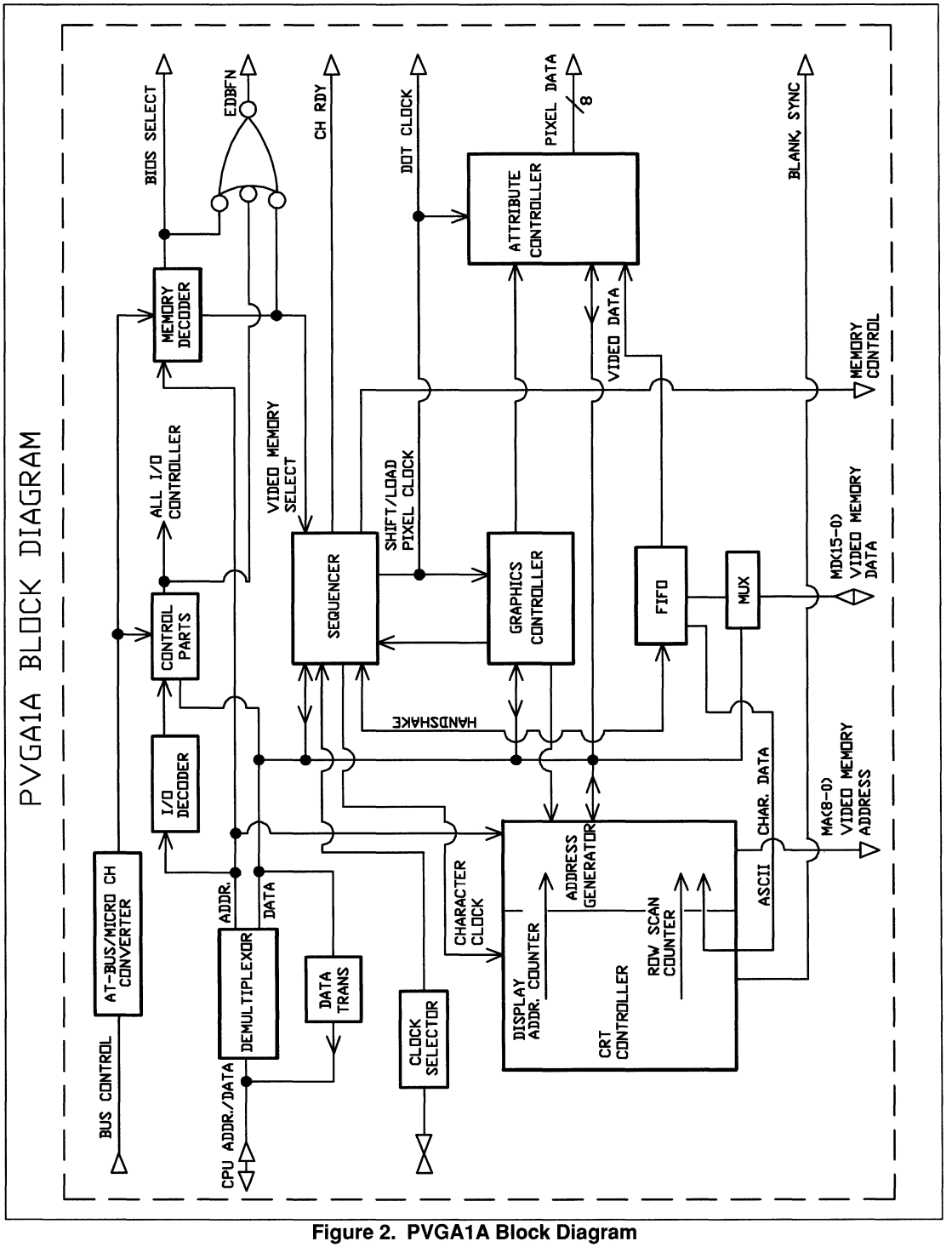


Figure 2. PVGA1A Block Diagram

2.0 SCOPE

Many applications require greater graphics capability than is available through the IBM Monochrome Display Adapter (MDA), Color Graphics Adapter (CGA), Enhanced Graphics Adapter (EGA), Multicolor Graphics Array (MCGA), and the Video Graphics Array (VGA). The Paradise PVGA1A is a 1.25 micron, 12,000 gate CMOS VLSI device that allows the design of a very high performance VGA graphics subsystem able to interface with the PC/XT/AT Bus, as well as the IBM Micro Channel Bus, while maintaining backwards compatibility with previous video standards. A major advantage of the PVGA1A is that designs implementing this graphics controller will be able to run applications requiring MDA, CGA, Hercules, AT&T 6300, and VGA hardware and BIOS compatibility, and also EGA BIOS compatibility, on analog or multifrequency monitors.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, internal register descriptions, AC/DC characteristics, timing diagrams, VLSI package mechanical information, and a list of associated references.

2.1 PVGA1A DESCRIPTION

The PVGA1A internally contains four major modules. These are the CRT Controller, the Sequencer, the Graphics Controller and the Attribute Controller. The PVGA1A has 4 major interfaces: the CPU and BIOS ROM interface, the Clock interface, the DRAM Display Buffer interface, and the Video and RAMDAC interface.

The PVGA1A internally contains four major modules. These are the CRT Controller, the Sequencer, the Graphics Controller and the Attribute Controller. The PVGA1A has 4 major interfaces: the CPU and BIOS ROM interface, the Clock interface, the DRAM Display Buffer interface, and the Video and RAMDAC interface.The PVGA1A controls the interfacing between the system microprocessor and video memory. Because PVGA1A controls arbitration for video memory between the system microprocessor and the CRT Controller function contained within the PVGA1A, all data passes through PVGA1A when the system microprocessor writes to or reads from video memory.

A FIFO is used internally to achieve the video display bandwidth necessary between CPU accesses and display refresh cycles, using standard DRAMs.

2.2 PVGA1A MODULES

The CRT Controller section within the PVGA1A maintains screen refresh functions for the various display modes defined by the BIOS ROM resident firmware. The PVGA1A CRT Controller also generates horizontal sync (HSYNC), vertical sync (HSYNC), and blank pulses for the display monitor.

The Sequencer functions as a timing generator for the AT bus or Micro Channel interface, in I/O or memory cycles. It also provides the character clock in the alphanumeric mode, and the dot clock in the graphics mode, for the CRT, Graphics, and Attribute Controllers.

The Graphics Controller manages data flow between video memory and the Attribute Controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the Sequencer.

The Attribute Controller modifies the CRT display data stream in graphics and character modes. It controls display attributes such as blinking, underlining, cursor, scrolling, reverse video, and background or foreground video, in VGA and enhanced VGA BIOS modes.

3.0 PVGA1A INTERFACES

3.1 CPU AND BIOS ROM INTERFACE

The PVGA1A is designed to operate in two different bus architecture configurations. These are the PC/XT/AT Bus and the PS/2 Micro Channel Bus. The selection of the mode is dependant on the setting of a configuration register bit CNF(2), which is determined upon power-up/reset, and is described in the PVGA1A Paradise Register section of this data sheet.

The I/O data path is eight bit. The DRAM display buffer data path can be 8- or 16-bit. EGA Planar modes have an eight bit data path with the CPU. Text modes and 256 color extended modes (packed pixel modes) can have a 16-bit data path if the video subsystem supports a 16-bit bus.

The PVGA1A will provide the necessary waitstates for CPU accesses to the video memory. Wait states for I/O accesses and BIOS ROM accesses are not generated.

Special I/O ports, such as 46E8H(AT) for setup, and 102H for VGA enable, have been implemented internally in the PVGA1A.

When configured for AT or Micro Channel operation, the PVGA1A operates functionally in a manner that is conducive to PC/XT/AT or Micro Channel interfacing respectively. The signal pins, memory maps and I/O ports all operate to optimize this interface with minimal external circuitry.

The PVGA1A provides all the signals, and decodes all the necessary memory and I/O addresses to interface with the AT bus or the Micro Channel bus, in 8- or 16-bit data path modes. PVGA1A also provides the necessary decoding of the adapter video BIOS ROM, and has additional signals and registers to help with BIOS ROM page mapping as done on the IBM PS/2 display adapter. Using the provided signals, the user can implement designs able to multiplex the address/data signals to the PVGA1A in 8- or 16-bit mode, control an 8- or 16-bit BIOS ROM, and generate the desired control/handshake signals (such as -MEMCS16 in AT mode).

3.2 DRAM INTERFACE

The PVGA1A optimizes its interface to the video memory display buffer. The video memory DRAMs are organized as 4 planes and the PVGA1A is designed for 3 configurations of DRAMs. Each plane can be configured as 64 Kbytes (256 Kbyte total), 128 Kbytes (512 Kbyte total), or 256 Kbytes (1 Mbyte total). cycles. PVGA1A will also refresh the DRAMs with 3 or 5 refresh cycles (page mode in graphics or RAS refresh in alpha) after every horizontal scan line.

The PVGA1A supports 256 Kbytes of DRAM by using eight 64 Kbyte by 4 page mode DRAM chips; 512 Kbytes of DRAM by using sixteen 64 Kbyte by 4 page mode DRAM chips; or 1 Mbyte of DRAM using eight 256 Kbyte by 4 page mode DRAM chips. Usually a 36 MHz MCLK and 120ns DRAMs are used. A 640 by 400 by 256 color mode is supported when 100 ns DRAMs and a 42 MHz MCLK is used. 640 by 480 by 256 color mode is supported when the 512 Kbyte DRAM configuration along with 100ns DRAMs and a 42 MHz MCLK are used. The PVGA1A Paradise registers provide support for accesses of up to 1 Mbyte of video memory.

The PVGA1A provides the necessary control signals and address/data lines to access the video memory as two 16-bit data interleaved banks. For display refresh cycles, the PVGA1A will perform page mode Read operations on the video memory in graphics modes, and in alpha modes it will generate standard RAS/CAS.

3.3 VIDEO INTERFACE

The PVGA1A is optimized to connect to an analog CRT monitor through a RAMDAC, but it may also be used to drive other types of displays, such as TTL monitors. In interfacing to an analog monitor through an external RAMDAC, the PVGA1A provides all the necessary signals to interface to the video RAMDAC.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and depth (bits/pixels) of the image desired. New monitors, such as multifrequency monitors, are less stringent because of the many sync frequencies available. The PVGA1A can be programmed to directly generate all the CRT signals for up to 8 bits/pixel (256 color) displays. In addition, external hardware can be added to allow higher display resolutions by trading off the number of bits/pixel.

The Micro Channel Auxiliary Video Connector and the AT Feature Connector can be connected to PVGA1A. PVGA1A also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

3.4 CLOCK INTERFACE

The PVGA1A has four clock input signal pins. These are: the separate memory clock, MCLK, which drives the DRAM timing in graphics modes; and the three video clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing and DRAM timing in alphanumeric modes. PVGA1A also provides the option to externally control a multiplexer that supplies the video clock.

3.5 PVGA1A POWER-UP CONFIGURATION

The PVGA1A uses the memory data pins to configure an internal configuration register upon power-up/reset. CNF(2) will determine whether the PVGA1A will operate in AT or Micro Channel bus mode.

Other CNF bits configured by PVGA1A at power-up/reset are used as status bits, or for clock source control. For more information on PVGA1A power-up configuration, refer to the Paradise Register section of this data sheet.

4.0 PIN DESCRIPTION

The table below provides PVGA1A pin definitions for the 100 Pin Plastic Leadless Chip Carrier (PLCC)and Plastic Flat Pack (PFP) package. The PVGA1A mnemonics are used. For more design details in AT or Micro Channel modes refer to the application notes and reference section of this document.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
			POWER ON
36	RSET	I	RESET: This signal input will reset the PVGA1A. MCLK and VCLK0 should be connected to PVGA1A in order for the PVGA1A to initialize during Reset. Paradise registers PR1, and CNF are initialized at power-up reset based on the logic level on the MD7-0 bus as determined by pull-up/ pull-down resistors. Outputs EABUFN and EDBUFN are 3-stated during reset. The reset pulse width should be at least **ten** MCLK clock periods.
			CLOCK SELECTION
76	MCLK	I	MEMORY CLOCK: This clock signal determines the VGA graphics mode video DRAM read/write access timing as well as system microprocessor I/O and memory timing. MCLK should be approximately 36 MHz for 120 ns DRAMS, and 42.0 MHz for 100 ns DRAMS.
75	VCLK0	I	VIDEO CLOCK 0: This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK0 is 25.175 MHz to display 640 pixels per horizontal display line. MCLK should be greater than or equal to VCLK0. The Miscellaneous Output Register bits 2 and 3, both set to 0, will select this clock if VCLK1 and VCLK2 are used as inputs.
74	VCLK1	I/O	VIDEO CLOCK 1: This pin can be a second video display clock input or an output to external clock selection module. Pin direction is determined on Reset by a pull-up/down resistor on pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 is an active low pulse during I/O writes to port 3C2H. Refer to the Configuration Register description. MCLK should be greater than or equal to VCLK1.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
73	VCLK2	I/O	VIDEO CLOCK 2: This pin can be a third video display clock input or an output to external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. It acts as either a user-defined external clock input, or as an output reflecting the content of bit PR2(1) if CNF (3) is set to 1. Refer to the Configuration Register description. MCLK should be greater than or equal to VCLK2.
			CPU ADDRESS AND DATA BUS
28	A19	I	ADDRESS-ONLY BUS (A15-A19): These active high inputs form the high-order five bits of video memory address. These addresses are not decoded during I/O accesses in AT or Micro Channel modes. These inputs are directly connected to the system bus.
27	A18	I	
24	A17	I	
23	A16	I	
22	A15	I	
20	DA15(*)	I/O	DATA/ADDRESS BUS (DA0-DA15): These signals comprise an active high multiplexed data/address bus for I/O and memory accesses. Only the low eight bits are used for data during I/O read and write cycles. During every I/O read and write, the voltage level on DA15 is used to help determine the monitor type, and can be read at port 3C2H bit 4. A logic 0 or logic 1 on DA15 places a logic 0 or a logic 1 into bit 4 of the Input Status Register 0, respectively. Refer to the general register description for more information.
19	DA14	I/O	
18	DA13	I/O	
17	DA12	I/O	
16	DA11	I/O	
14	DA10	I/O	
13	DA9	I/O	
2	DA8	I/O	
46	DA7	I/O	
45	DA6	I/O	
44	DA5	I/O	
43	DA4	I/O	
42	DA3	I/O	
41	DA2	I/O	NOTE : " * "DA15 signal is multiplexed with data bit 15and CRT
40	DA1	I/O	monitor sense input for auto monitor detection. Refer to
39	DA0	I/O	technical brief on auto monitor detection circuit.
			CPU CONTROL BUS
21	EMEM	I	ENABLE DISPLAY MEMORY: This signal is active high in both Micro Channel and AT modes. In AT Mode, EMEM enables video memory accesses. BIOS ROM accesses are not controlled by EMEM. If the video memory is within the lowest 1MB of the processor address space, EMEM signal must be active during video memory access. Otherwise, EMEM should be generated by external logic when the PVGA1A video memory is accessed. During AT Bus refresh time, EMEM can be connected to REFRESH to disable the PVGA1A. In Micro Channel mode this signal enables I/O and video memory access. External logic is required to implement the function EMEM.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
10	SFDBKN	O	16-BIT WIDE BIOS ROM: In AT mode this active low signal is the inverted value of register PR1(1), which determines BIOS ROM data path width selection. It may be used to control data buffers for a 16 bit data path BIOS ROM and to generate the BIOS ROM chip enable signal MEMCS16 in AT mode. In Micro Channel mode, its mnemonic is -CD SFDBK. -CD SFDBK is the unlatched decode (active low) when a memory, I/O, or BIOS ROM access is done from the system bus and may be considered as adapter or VGA feedback. For further details, refer to the reference literature.
34	RDY	O	READY: An active high output which signals to the system processor that a memory access is completed and is only used to add wait states to the MCA or CPU bus cycles during video memory accesses. It is pulled inactive by PVGA1A to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM. For further details, refer to the reference literature.
35	IRQ	O	INTERRUPT REQUEST: Programmable processor interrupt request. It is enabled via bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of Vertical Display occurs, this signal will transition active, causing the interrupt. It will stay latched until CRTC11 bit 4 clears it. In an AT system IRQ is not connected, but may be connected if desired. -IRQ9 is used to generate interrupt in the Micro Channel mode. For further details, refer to the reference literature and the CPU section in the introduction.
8	DS16N	O	DATA SIZE 16: Active low enable for 16-bit video memory word transfers. It is a mode dependent signal. In AT mode, the signal level is as programmed in bit PR1(2) and may be used to control 16 bit external data buffers. See the Paradise Register (PR1) description for further details. This signal is used to generate -MEMCS16 using external logic for AT mode designs. In Micro Channel mode, the signal is active only during BIOS ROM accesses (if enabled) by PR1(1)) and/or during memory 16-bit data path access (if enabled by PR1(2)). See the section on Paradise Registers or consult the reference literature for more information.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
33	EION	I	ENABLE I/O: In AT mode, this active low signal enables I/O accesses to the PVGA1A. In Micro Channel mode, this signal is the set up input pin and is connected to the card set up or the VGA setup. The externally designed system I/O (96H for Adapter card or 94H bit 5 for system board design) is connected to the EION pin. When this signal is high, the PVGA1A is enabled or in the operating state. An active low signal on this pin puts the PVGA1A into set up mode. During the set up mode, write logic 1 to PVGA1A internal port 102H to awaken the PVGA1A after power on. Refer to application note for more information. When in set up mode, the PVGA1A will only respond to the internal I/O register located at 102H. Accesses to port 3C3H (external) and BIOS ROM addresses are not affected by setup mode, so they can be accessed.
9	BHEN	I	BUS HIGH ENABLE: In both AT and MCA mode, this active low signal enables and indicates transfer of data on the high byte of the data bus (DA8-D15) when PVGA1A is in 16-bit mode. With address A0, it distinguishes between high byte (DA15-8) and low byte (DA0-7) data transfers. It is not used for I/O transfers in either AT mode or Micro Channel mode.
31	MRDN	I	MEMORY READ: In AT mode, this signal is called -SMEMR and is an active low memory read strobe. It is asserted in 8/16 bit memory read cycles. In Micro Channel mode, the signal is called M/-IO. It distinguishes between memory and I/O cycles. When (M/-IO) is high, a memory cycle is in process. A low on (M/-IO) shows that an I/O cycle is in process. For further details, refer to the reference literature.
32	MWRN	I	MEMORY WRITE: The Active low memory write strobe in AT mode for 8/16 bit data transfers. In Micro Channel mode, it becomes -S0 and is the channel status signal which indicates the start and type of a channel cycle. Along with -S1, M/-IO, and -CMD signals, it is decoded to interpret I/O and memory commands. For further details, refer to the reference literature.
29	IORN	I	I/O READ: Active low I/O read strobe in AT mode. It is asserted in 8/16 bit I/O read bus cycles. -S1 is the alternate mnemonic used in Micro Channel mode to indicate the start and type of a channel cycle. For further details, refer to the reference literature.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
30	IOWN	I	I/O WRITE: Active low strobe. In AT mode, the strobe signals an I/O write for 8/16 bit I/O write cycles. In Micro Channel mode it is synonymous with -CMD; address bus validity is signaled by -CMD going low while the rising edge of -CMD indicates the end of a Micro Channel bus cycle. For further details, refer to the reference literature.
			VIDEO MEMORY DATA
89 90 91 92 93 94 95 96 97 98 99 2 3 4 5 6	MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8 MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0	I/O	DISPLAY MEMORY DATA (D0-D15): These lines are the data bus to the video display DRAMS. Data lines MD0-7 are pulled up or down with resistors to provide set up information on power-up (reset) as follows: MD — Power-Up Function — Affected Register (bit) 7 — General Purpose — CNF(7) * 6 — General Purpose — CNF(6) * 5 — General Purpose — CNF(5) * 4 — General Purpose — CNF(4) * 3 — VCLK1,2 Input/Output — CNF(3) + 2 — AT/Micro Channel Mode — CNF(2) + 1 — BIOS ROM Data Path — PR1(1) * 0 — BIOS ROM Mapping — PR1(0) * NOTE : " * " Pulldown resistor sets these bits to logic 1. " + " Pullup resistor sets these bits to logic 1. For more details refer to the section on Paradise Registers.
			VIDEO MEMORY ADDRESS
63 65 66 67 68 69 70 71 72	MA8 † MA7 † MA6 † MA5 † MA4 † MA3 † MA2 † MA1 † MA0 †	O	MEMORY ADDRESS (MA0-MA8): Display memory DRAM address.

Note: "†" For testing purposes, these pins can be tri-stated by setting Paradise Register PR4(4)=1.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
			VIDEO MEMORY CONTROL SIGNALS
80	CAS10N †	O	COLUMN ADDRESS STROBE: Active low Memory Maps 1 & 0 CAS output signal.
83	CAS32N †	O	COLUMN ADDRESS STROBE: Active low Memory Maps 3 & 2 CAS output signal.
79	RAS10N †	O	ROW ADDRESS STROBE: Active low Memory Maps 1 & 0 RAS output signal.
82	RAS32N †	O	ROW ADDRESS STROBE: Active low Memory Maps 3 & 2 RAS output signal.
81	OE10N †	O	OUTPUT ENABLE: Active low Memory Maps 1 & 0 DRAM output enable.
84	OE32N †	O	OUTPUT ENABLE: Active low Memory Maps 3 & 2 DRAM output enable.
85	WE0N †	O	WRITE ENABLE: Active low Write Enable to DRAM bank 0, lower byte (Memory map 0).
86	WE1N †	O	WRITE ENABLE: Active low Write Enable for DRAM bank 0, upper byte (Memory map 1).
87	WE2N †	O	WRITE ENABLE: Active low Write Enable for DRAM bank 1, lower byte (Memory map 2).
88	WE3N †	O	WRITE ENABLE: Active low Write Enable for DRAM bank 1, upper byte (Memory map 3).

Note: "†" For testing purposes, these pins can be tri-stated by setting Paradise Register PR4(4)=1.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
			RAMDAC INTERFACE
48 49 50 53 54 55 56 57	VID7 § VID6 § VID5 § VID4 § VID3 § VID2 § VID1 § VID0 §	O	VIDEO (VD0-VD7): Pixel video output to DAC and color palette.
47	RPLTN	O	READ PALETTE: Video DAC register and color palette read signal. Active low during I/O read to addresses 3C6H, 3C8H, and 3C9H.
58	WPLTN	O	WRITE PALETTE: Video DAC register and color palette write signal. Active low during I/O write to addresses 3C6H-3C9H.
59	PCLK	O	PIXEL CLOCK: Video pixel clock output used by the DAC to latch video signals VID0-7. Its source is one of the video clock inputs: VCLK0, VCLK1, or VCLK2 as determined by the Miscellaneous Output register. Note that VCLK0, 1 or 2 is divided by two in 320/360 pixel display mode to derive PCLK.
62	BLNKN ‡	O	BLANK: Active low display monitor blank pulse.
			CRT CONTROL
60	HSYNC ‡	O	HORIZONTAL SYNC: Display monitor horizontal synchronization pulse. Active high or low depending on the Miscellaneous register programming.
61	VSYNC ‡	O	VERTICAL SYNC: Active high display monitor vertical synchronization pulse. It is active high or low, depending on the Miscellaneous Output Register.

Notes: "§" For testing purposes, these pins can be tri-stated by setting Paradise Register PR4(5)=1.
"‡" For testing purposes, these pins can be tri-stated by setting Paradise Register PR4(6)=1.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
			BIOS ROM CONTROL
7	EBROMN	O	ENABLE BIOS ROM ACCESS: In both AT and Micro Channel modes this signal is active (low) during memory reads in the address range (C0000H-C7FFFH) if enabled by bit PR1(0). It is not active for accesses to addresses in the range C6000H-C67FFH. In AT mode only, a write to the PVGA1A internal I/O port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
			BUFFER CONTROL
11	EABUFN	O	ENABLE ADDRESS BUFFER: This active low signal permits control of an external address buffer for multiplexing address and data to PVGA1A. It is 3-stated while Reset is active.
38	EDBUFN	O	ENABLE DATA BUFFER: Allows control of an external data buffer for multiplexing address and data to PVGA1A. It is 3-stated while Reset is active.
37	DIR	O	DIRECTION CONTROL: Active high Direction Control for reads of the MD0-15 data bus in AT and Micro Channel modes. The default state is low until a read/write cycle occurs. Then the PVGA1A will drive DIR high to change the direction of the data buffers.
			POWER AND GROUND
25	VCC	-----	+5VDC
52	VCC	-----	+5VDC
78	VCC	-----	+5VDC
100	VCC	-----	+5VDC
1	GND	-----	Ground
15	GND	-----	Ground
26	GND	-----	Ground
51	GND	-----	Ground
64	GND	-----	Ground
77	GND	-----	Ground

5.0 ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	$0^{o}C$ to $70^{o}C$
Storage temperature	$-40^{o}C$ to $125^{o}C$
Voltage on all inputs and outputs with respect to V_{SS}	-0.3 to 7 Volts
Power dissipation	1.0 Watt

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating temperature range	0^{o} to $70^{o}C$
Power supply voltage	4.75 to 5.25 Volts

NOTE :

5.1 D.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX	UNITS	CONDITIONS	NOTE
VIL	Input Low Voltage	-0.3	0.8	V	VCC = 5V +/-5%	
VIH	Input High Voltage	2.0	VCC+0.3	V	VCC = 5V +/-5%	
IIL	Input Low Current	-----	+/-10	uA	VIN = 0.0V	
IIH	Input High Current	-----	+/-10	uA	VIN = VCC	
VOL	Output Low Voltage	-----	0.4	V	IOL +4.0 mA	1
VOH	Output High Voltage	2.4	-----	V	IOH = 4.0 mA	1
IOZ	High Impedance Leakage Current	-10.0	10.0	uA	OV<VOUT<VCC	
ICC	Stand By Current (All Inputs at TTL Levels)	-----	22	mA	VCC = 5.25 VDC TA = $0^{o}C$, Static	
CIN	Input Capacitance	-----	10	pF	FC = 1MHZ	
COUT	Output Capacitance	-----	10	pF	FC = 1MHZ	

1. PVGA1A outputs have 4.0 mA maximum source and sink capability except as follows: RDY = 12.0 mA sink and 4.0 mA source.

19

5.2 AC CHARACTERISTICS

I/O READ - AT MODE TIMING DIAGRAM (See Figure 4)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, EION Setup to IORN	13	--	
2	Address Hold from IORN Active	4	--	
3	Read Data Valid from IORN Active	--	2Tp+20	1
4	IORN Pulse Width	2Tp+50	--	1
5	Read Data Hold from IORN Inactive	16	--	
6	EABUFN Inactive from IORN Active	--	29	
7	EDBUFN Active from EABUFN Inactive	--	31	
8	EDBUFN Inactive from IORN Inactive	--	30	
9	EABUFN Active from EDBUFN Inactive	--	31	
10	DIR Active to IORN Active	--	25	
11	DIR Inactive from IORN Inactive	--	26	
12	RPLTN Active from IORN Active	--	2Tp+34	1,2
13	RPLTN Inactive from IORN Inactive	13	--	2
14	EION Hold from IORN Inactive	5	--	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes.
2. RPLTN signal active only with I/O addresses 03C6H-03C9H, except 03C7H.
3. For the signals that change between AT and Micro Channel modes, based upon CNF(2), the PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the AT mode timing diagrams.

** For reference only. RPLTN is in synchronization with MCLK.

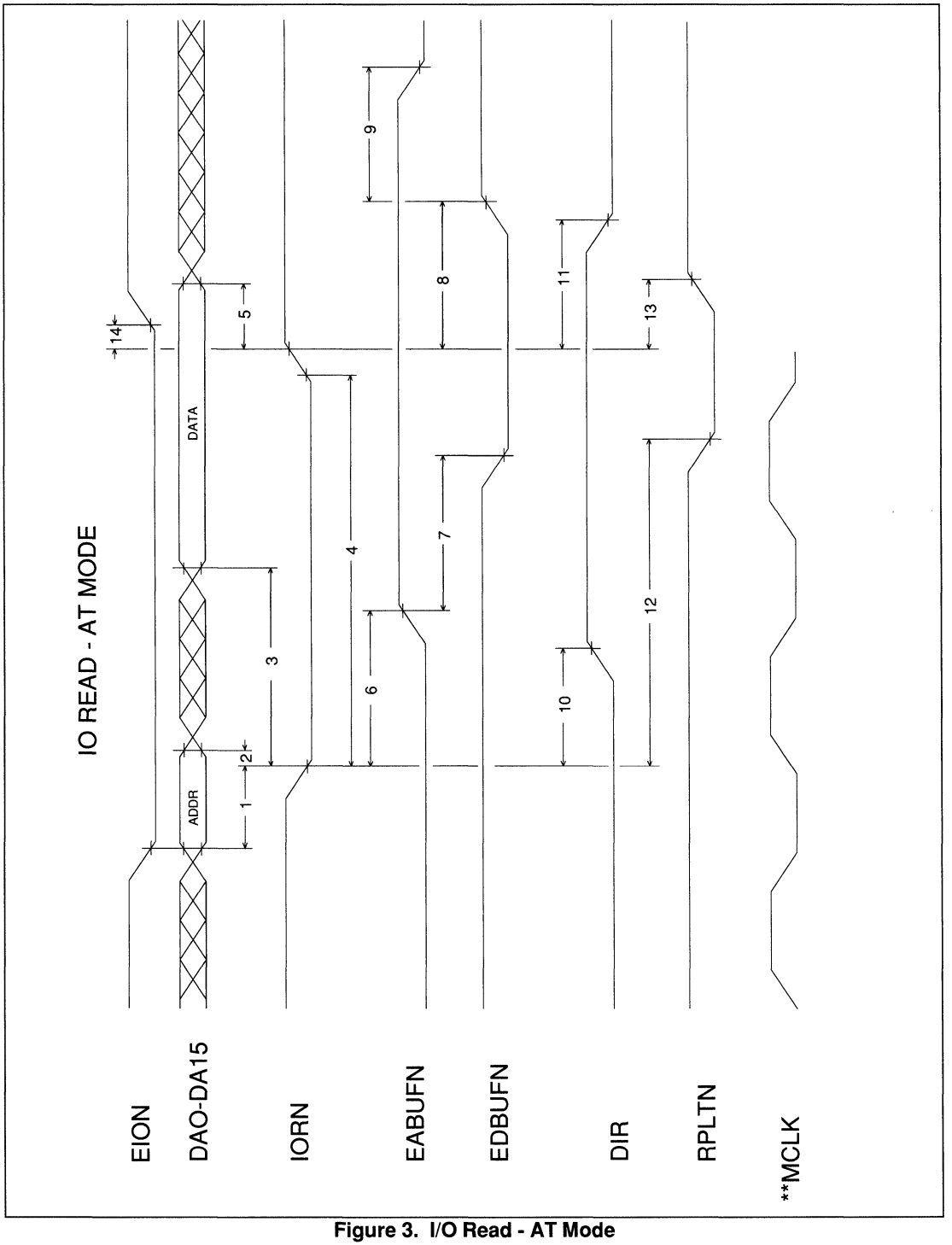


Figure 3. I/O Read - AT Mode

6.0 TIMING DIAGRAMS

6.1 I/O WRITE - AT MODE TIMING DIAGRAM (See Figure 5)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, EION Setup to IOWN	13	--	
2	Address Hold From IOWN Active	4	--	
3	Write Data Valid from IOWN Active	--	3Tp-8	1
4	IOWN Pulse Width	3Tp+50	--	1
5	Write Data Hold from IOWN Inactive	16	--	
6	EABUFN Inactive from IOWN Active	--	29	
7	EDBUFN Active from EABUFN Inactive	--	31	
8	EDBUFN Inactive from IOWN Inactive	--	30	
9	EABUFN Active from EDBUFN Inactive	--	31	
10	WPLTN Active from IOWN Active	--	3Tp+Tv+15	1,2
11	WPLTN Inactive from IOWN Inactive	16	--	2
12	EION Hold from IOWN Inactive	5	--	
13	EBROMN Active from IOWN Active	--	29	3
14	EBROMN Inactive from IOWN Inactive	--	27	3

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes. Tv = 2/VCLK0 or 2/VCLK1 or 2/VCLK2 depending on selected video clock.
2. WPLTN signal active only with I/O addresses 03C6H-03C9H.
3. EBROMN signal is active only during I/O port 46E8H write operation.
4. For the signals that change between AT and Micro Channel modes, based upon CNF(2), the PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the AT mode timing diagrams.

** For reference only. WPLTN is in synchronization with PCLK.

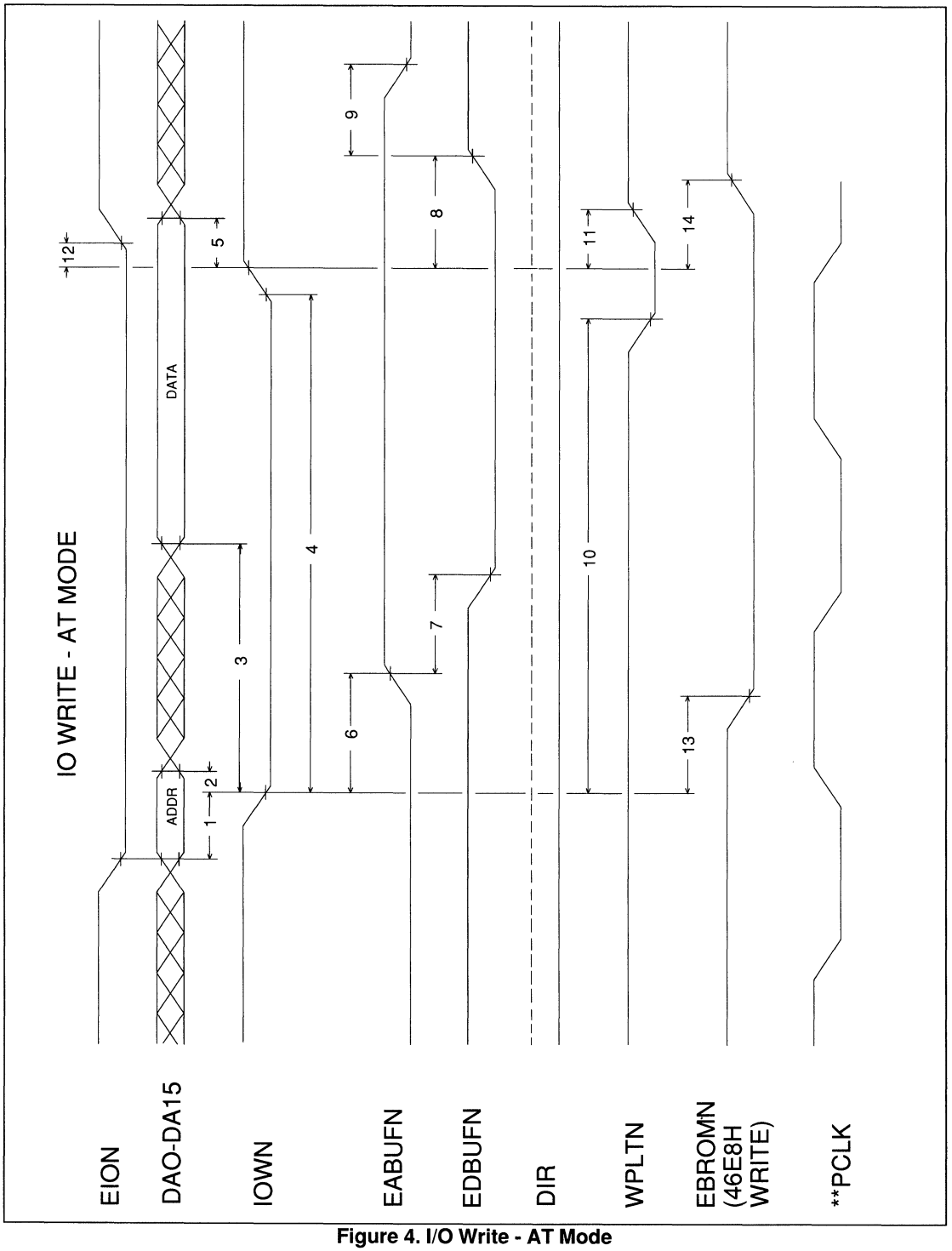


Figure 4. I/O Write - AT Mode

MEMORY READ - AT MODE TIMING DIAGRAM **(See Figure 6)**

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, BHEN, EMEM Setup to MRDN	13	--	
2	Address, BHEN Hold from MRDN Active	4	--	
3	Data Valid Setup to RDY	Tp+25	--	5
4	Data Hold from MRDN Inactive	10	--	
5	EABUFN Inactive from MRDN Active	--	29	
6	EDBUFN Active from EABUFN Inactive	--	31	
7	EDBUFN Inactive from MRDN Inactive	--	30	
8	EABUFN Active from EDBUFN Inactive	--	31	
9	DIR Active to MRDN Active	--	25	
10	DIR Inactive from MRDN Inactive	--	26	
11	RDY Inactive from MRDN Active	--	18	
12	RDY Active High from MRDN Active	--	2000	
13	RDY Inactive (Tri-state) from MRDN Inactive	--	180	4
14	EBROMN Active from MRDN Active	--	29	2
15	EBROMN Inactive from MRDN Inactive -	-	27	2
16	EMEM Hold from MRDN Inactive	4	--	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Duration of RDY signal inactive is dependent on video memory access contention and phase of clock.
   The Clock is MCLK, VCLK0, VCLK1, or VCLK2 depending on clock selection.
2. EBROMN signal active for addresses C0000-C7FFFH excluding addresses C6000-C67FFH.
3. For the signals that change between AT and Micro Channel modes, based upon CNF(2), the PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the AT mode timing diagrams.
4. On AT bus, this signal is tri-state and pulled up to +5V externally.
5. Tp = 1 / MCLK

** For reference only. WPLTN is in synchronization with PCLK

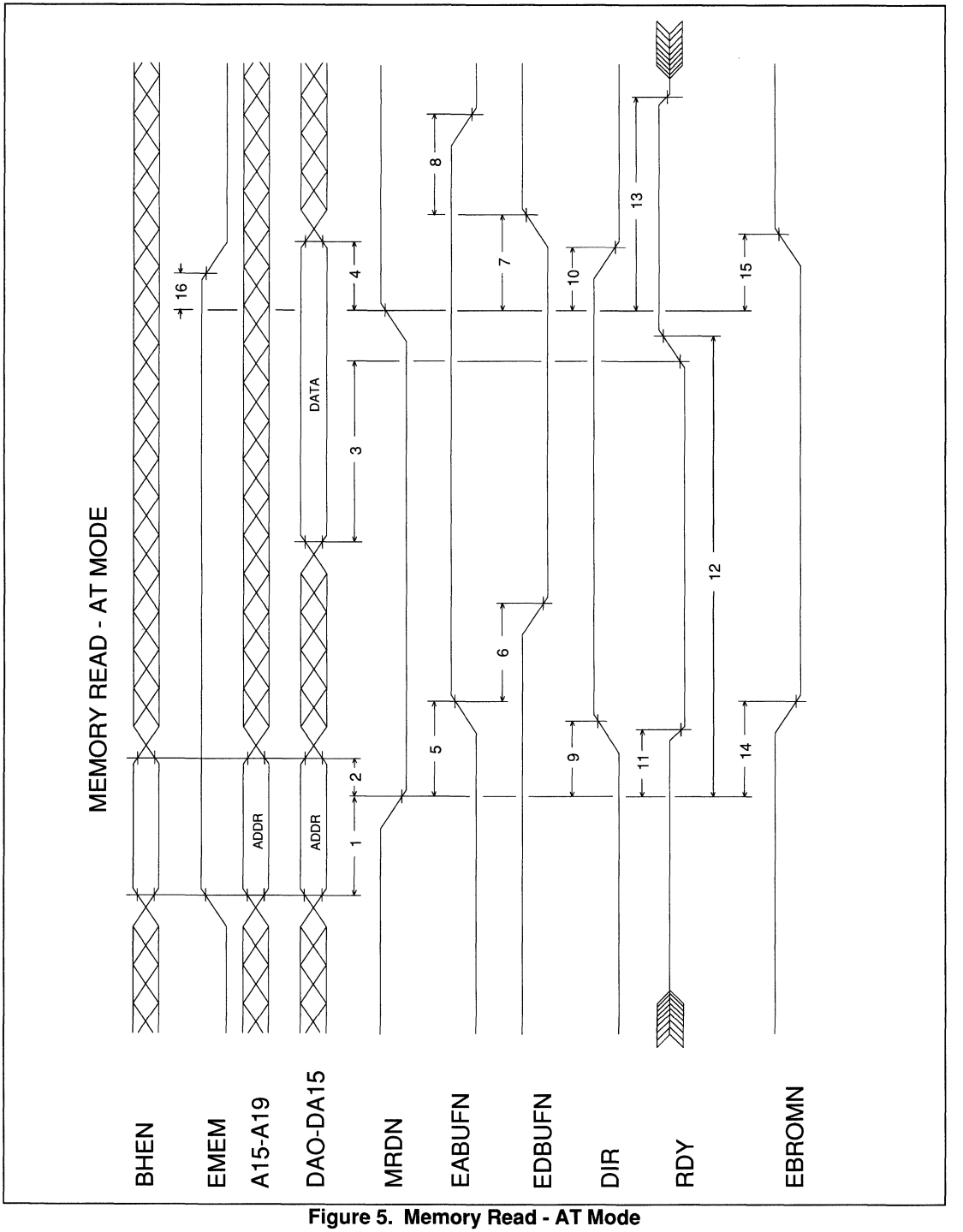


Figure 5. Memory Read - AT Mode

MEMORY WRITE- AT MODE TIMING DIAGRAM **(See Figure 7)**

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, BHEN, EMEM Setup to MWRN	13	--	
2	Address, BHEN Hold from MWRN Active	4	--	
3	Data Valid from MWRN Active --		3.5Tp-23	1
4	Data Hold from MWRN Inactive	0	--	
5	EABUFN Inactive from MWRN Active	--	29	
6	EDBUFN Active from EABUFN Inactive	--	31	
7	EDBUFN Inactive from MWRN Inactive	--	30	
8	EABUFN Active from EDBUFN Inactive	--	31	
9	RDY Inactive from MWRN Active	--	18	
10	RDY Active High from MWRN Active	--	2000	2
11	RDY Inactive (Tri-state) from MWRN Inactive	--	180	4
12	EMEM Hold from MWRN Inactive	4	--	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes.
2. Duration of RDY signal inactive is dependent on video memory access contention and phase of clock.
   The Clock is MCLK, VCLK0, VCLK1, or VCLK2 depending on clock selection.
3. For the signals that change between AT and Micro Channel modes, based upon CNF(2), the PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the AT mode timing diagrams.
4. On AT bus, this signal is tri-state and pulled up to +5V externally.

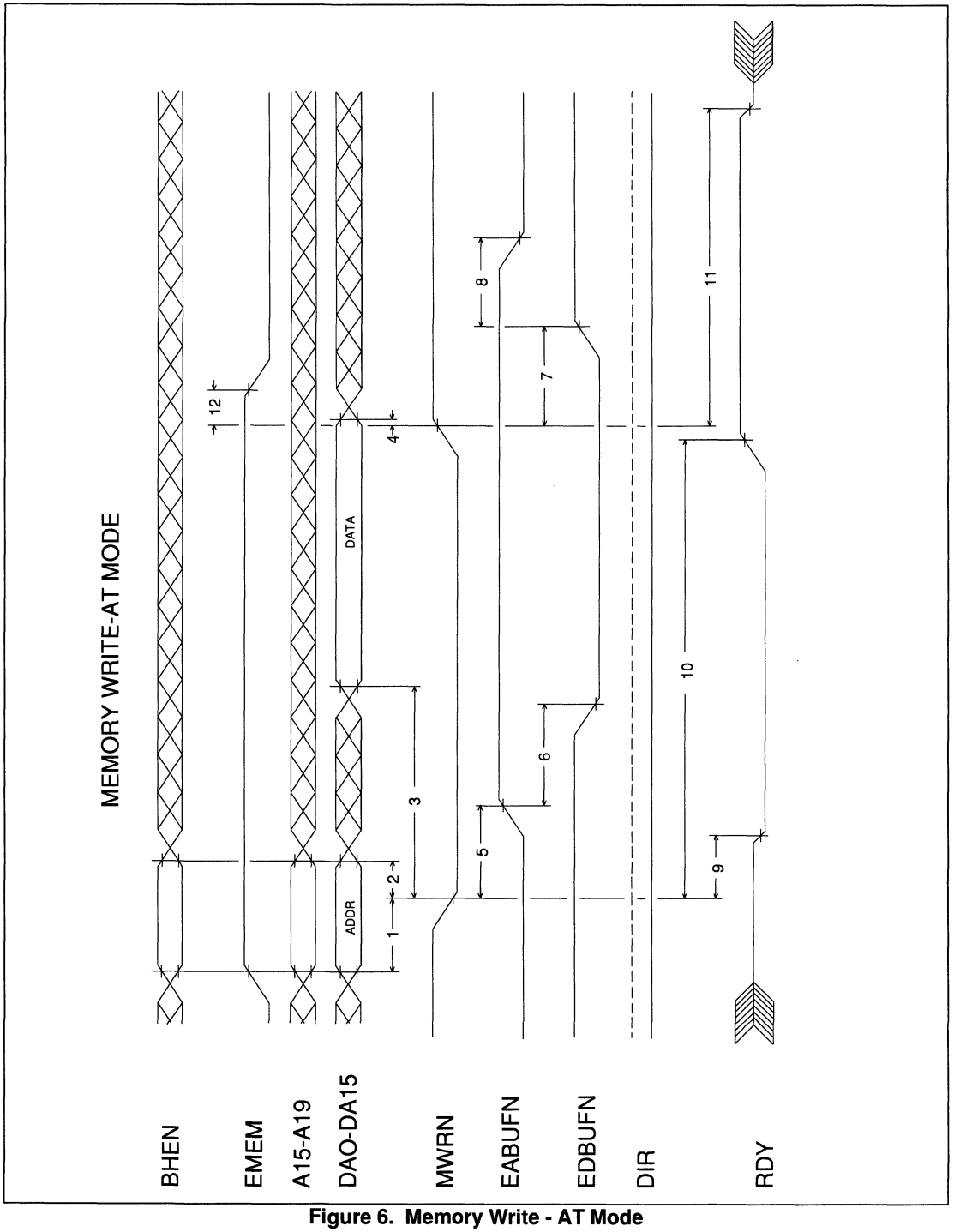


Figure 6. Memory Write - AT Mode

6.2 I/O READ - MICRO CHANNEL MODE TIMING DIAGRAM(See Figure 8)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, M/IO Setup to -CMD	13	--	
2	Address Hold from -CMD	4	--	
3	EMEM Active to -CMD Active	13	--	
4	EMEM Hold from -CMD Active	4	--	
5	-S1 Active to -CMD Active	3	--	
6	-S1 and M/IO Inactive from -CMD Active	5	--	
7	Read Data Valid from -CMD Active	--	2Tp+22	1
8	Read Data Hold from -CMD Inactive	18	--	
9	-CMD Pulsewidth	2Tp+50	--	1,5
10	-CMD Inactive to next -CMD Active	80	--	
11	EABUFN Iactive from -CMD Active	--	30	
12	EDBUFN Active from EABUFN Inactive	--	31	
13	EDBUFN Inactive from -CMD Inactive	--	31	
14	EABUFN Active from EDBUFN Inactive	--	30	
15	DIR Active to -CMD Active	--	27	
16	DIR Inactive from -CMD Inactive	--	26	
17	RPLTN Active from -CMD Active	--	2Tp+36	1,2
18	RPLTN Inactive from -CMD Inactive	13	--	2
19	SFDBKN Active from Address Valid, EMEM, and M/IO	--	34	4
20	SFDBKN Inactive from -CMD Inactive	--	32	4
21	-CD SETUP Active to -CMD Active	13	--	3
22	-CD SETUP Inactive from -CMD Inactive	4	--	3

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes.
2. RPLTN signal active only with I/O addresses 03C6H-03C9H, except 03C7H.
3. EION signal active as -CD SETUP for I/O access to port 102H only, otherwise its level is high.
4. If -CD SETUP (EION) signal is low, this output stays inactive.
5. Read operation is internally delayed by two Tp clocks.
6 For the signals that change between AT and Micro Channel modes, based upon CNF(2), the Micro Channel names and PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the Micro Channel mode timing diagrams.

** For reference only. RPLTN is in synchronization with MCLK.

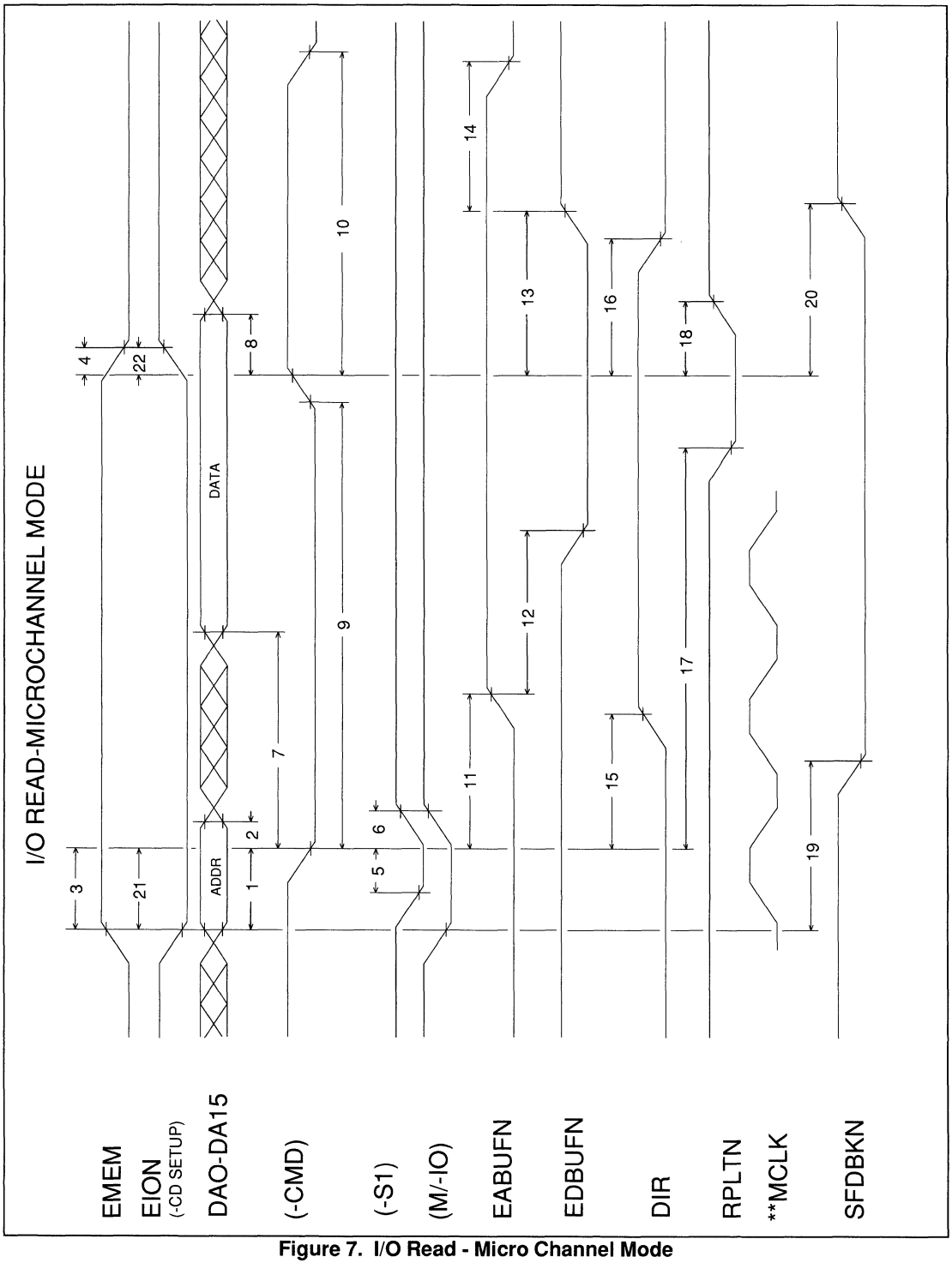


Figure 7. I/O Read - Micro Channel Mode

19

I/O WRITE - MICRO CHANNEL MODE TIMING DIAGRAM(See Figure 9)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, M/IO Setup to -CMD	13	--	
2	Address Hold from -CMD	4	--	
3	EMEM Active to -CMD Active	13	--	
4	EMEM Hold from -CMD Inactive	4	--	
5	-S0 Active to -CMD Active	3	--	
6	-S0 and M/IO Inactive from -CMD Active	5	--	
7	Write Data from -CMD Active	--	3Tp-10	1
8	Write Data Hold from -CMD Inactive	18	--	
9	-CMD Pulsewidth	3Tp+50	--	1,5
10	-CMD Inactive to next -CMD Active	80	--	
11	EABUFN Inactive from -CMD Active	--	30	
12	EDBUFN Active from EABUFN Inactive	--	31	
13	EDBUFN Inactive from -CMD Inactive	--	31	
14	EABUFN Active from EDBUFN Inactive	--	30	
15	WPLTN Active from -CMD Active	--	3Tp+Tv+17	1,2
16	WPLTN Inactive from -CMD Inactive	18	--	2
17	SFDBKN Active from Address Valid, EMEM, and M/IO	--	34	4
18	SFDBKN Inactive from -CMD Inactive	--	32	4
19	-CD SETUP Active to -CMD Active	13	--	3
20	-CD SETUP Inactive from -CMD Active	4	--	3

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes. Tv = 2/VCLK0 or 2/VCLK1 or 2/VCLK2 depending on selected video clock.
2. WPLTN signal active only with I/O addresses 03C6H-03C9H.
3. EION signal active as -CD SETUP for I/O access to port 102H only, otherwise its level is high.
4. If -CD SETUP (EION) signal is low, this output stays inactive.
5. Write operation is internally delayed three Tp clocks.
6 For the signals that change between AT and Micro Channel modes, based upon CNF(2), the Micro Channel names and PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the Micro Channel mode timing diagrams.

** For reference only. WPLTN is in synchronization with PCLK.

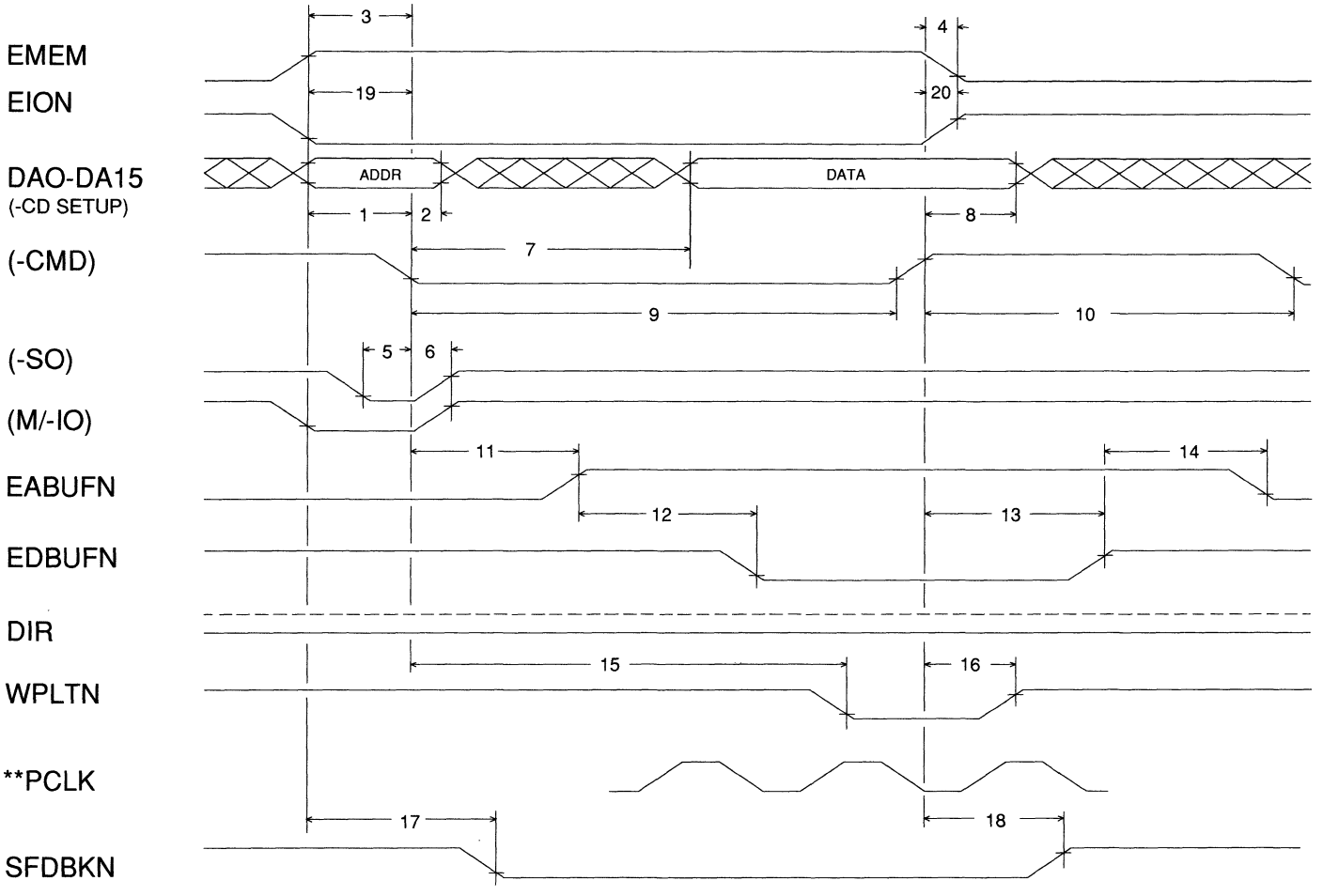


Figure 8. I/O Write - Micro Channel Mode

MEMORY READ - MICRO CHANNEL MODE TIMING DIAGRAM (See Figure 10)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address Setup to -CMD	13	--	
2	Address, BHEN Hold from -CMD Active	4	--	
3	BHEN, EMEM, M/IO Setup to -CMD Active	13	--	
4	DS16N Inactive from EMEM, M/IO, Address Invalid	--	30	3
5	-S1 Active to -CMD Active	3	--	
6	-S1 Hold from -CMD Active	5	--	
7	Read Data Valid Setup to RDY	Tp+25	--	5
8	Read Data Hold from -CMD Inactive	11	--	
9	-CMD Pulsewidth	2Tp+50	--	5
10	-CMD Inactive to next -CMD Active	80	--	
11	EABUFN Inactive from -CMD Active	--	30	
12	EDBUFN Active from EABUFN Inactive	--	31	
13	EDBUFN Inactive from -CMD Inactive	--	31	
14	EABUFN Active from EDBUFN Inactive	--	30	
15	DIR Active to -CMD Active	--	27	
16	DIR Inactive from -CMD Inactive	--	26	
17	RDY Inactive from Active Status	--	27	
18	RDY Active High from -CMD Active	--	2000	1
19	RDY Inactive (Tri-state) from -CMD Inactive	--	180	7
20	EBROMN Active from -CMD Active	--	31	2
21	EBROMN Inactive from -CMD Inactive	--	29	2
22	DS16N Active from Address Valid, EMEM, and M/IO	--	32	3
23	SFDBKN Active from Address Valid, EMEM, and M/IO	--	34	
24	SFDBKN Inactive from Address, M/IO, EMEM Invalid	--	32	
25	EMEM and M/IO Inactive from -CMD Inactive	5	--	4
26	Address, Hold from -CMD Inactive	4	--	

NOTES: * Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1 Duration of RDY signal inactive is dependent on video memory access contention and phase of clock. The Clock is MCLK, VCLK0, VCLK1, or VCLK2 depending on clock selection.

2 EBROMN signal active for addresses C0000-C7FFFH excluding addresses C6000-C67FFH.

3 DS16N signal active only for 16-bit access to memory and ROM addresses.

4 M/-IO, EMEM, & A15-A19 have to be latched during the command active period for the PVGA1A in 16 bit interface mode.

5 Tp = 1 / MCLK

6 For the signals that change between AT and Micro Channel modes, based upon CNF(2), the Micro Channel names and PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the Micro Channel mode timing diagrams.

7 For Micro Channel mode, this signal is tri-state. It is pulled up externally through a resistor to +5V.

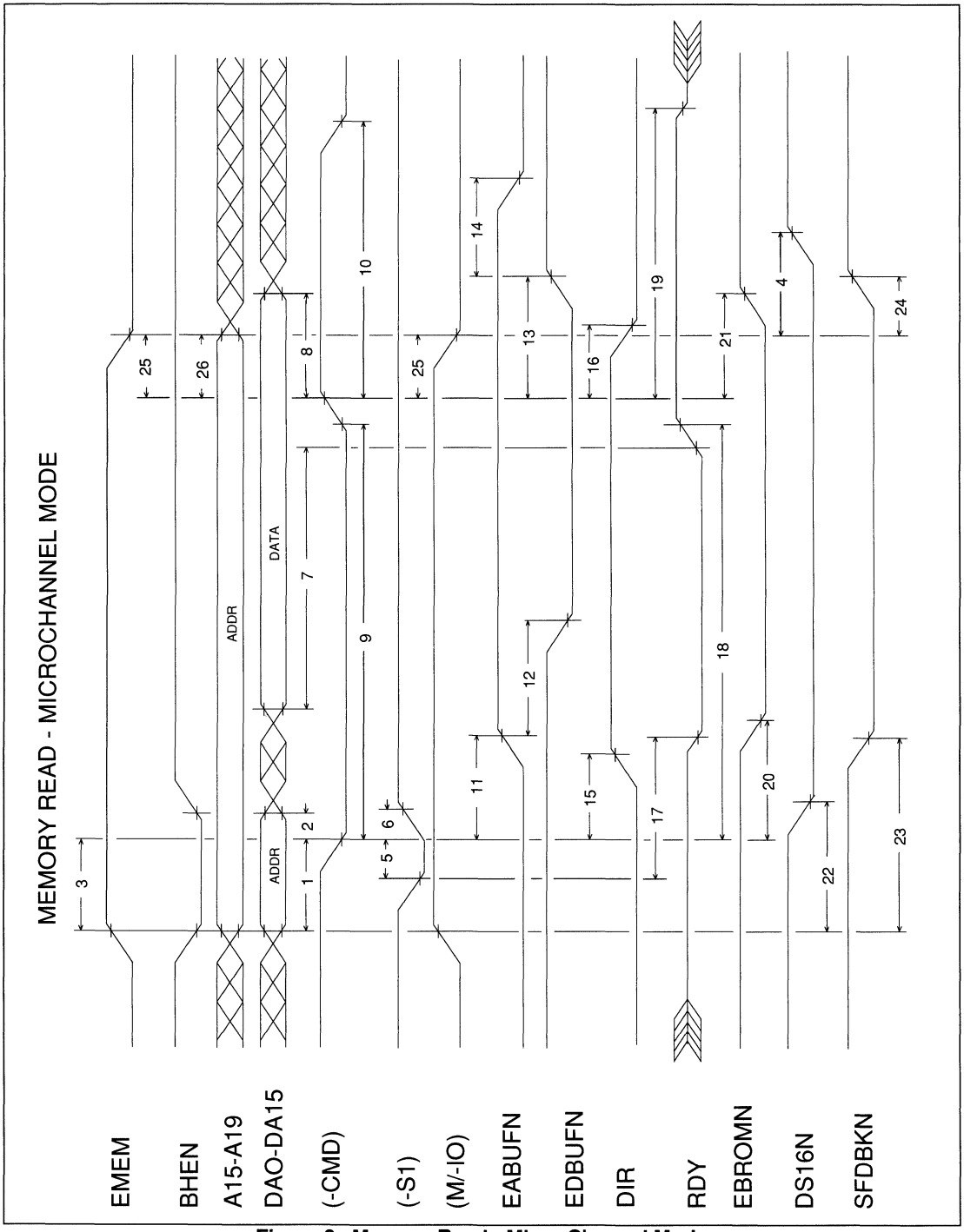


Figure 9. Memory Read - Micro Channel Mode

MEMORY WRITE - MICRO CHANNEL MODE TIMING DIAGRAM (See Figure 11)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address Setup to -CMD	13	--	
2	Address, BHEN Hold from -CMD Active	4	--	
3	BHEN,EMEM, M/IO Setup to -CMD Active	13	--	
4	DS16N Inactive from EMEM, M/IO, Address Invalid	--	30	3
5	-S0 Active to -CMD Active	3	--	
6	-S0 Hold from -CMD Active	5	--	
7	Write Data Valid from -CMD Active	--	3.5Tp-23	1
8	Write Data Hold from -CMD Inactive	0	--	
9	-CMD Pulsewidth	3Tp+50	--	1
10	-CMD Inactive to next -CMD Active	80	--	
11	EABUFN Inactive from -CMD Active	--	30	
12	EDBUFN Active from EABUFN Inactive	--	31	
13	EDBUFN Inactive from -CMD Inactive	--	31	
14	EABUFN Active from EDBUFN Inactive	--	30	
15	RDY Inactive from Active Status	--	27	
16	RDY Active High from -CMD Active	--	2000	2
17	RDY Inactive (Tri-state) from -CMD Inactive	--	180	6
18	DS16N Active from Address Valid, EMEM, and M/IO	--	32	3
19	SFDBKN Active from Address Valid, EMEM, and M/IO	--	34	
20	SFDBKN Inactive from, Address, M/IO, EMEM Invalid	--	32	
21	EMEM, and M/IO Inactive from -CMD Inactive	5	--	4
22	Address, Hold from -CMD Inactive	4	--	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes.
2. Duration of RDY signal inactive is dependent on video memory access contention and phase of clock.
   The Clock is MCLK, VCLK0, VCLK1, or VCLK2 depending on clock selection.
3. DS16N signal active only for 16-bit access to memory and ROM addresses.
4. M/-IO, EMEM, & A15-A19 have to be latched during the command active period for the PVGA1A in 16 bit interface mode.
5. For the signals that change between AT and Micro Channel modes, based upon CNF(2), the Micro Channel names and PVGA1A pnemonics (Refer to equivalence table in the pin description section) are used in the Micro Channel mode timing diagrams.
6. For Micro Channel mode, this signal is (tri-state). It is pulled up externally through a resistor to +5V.

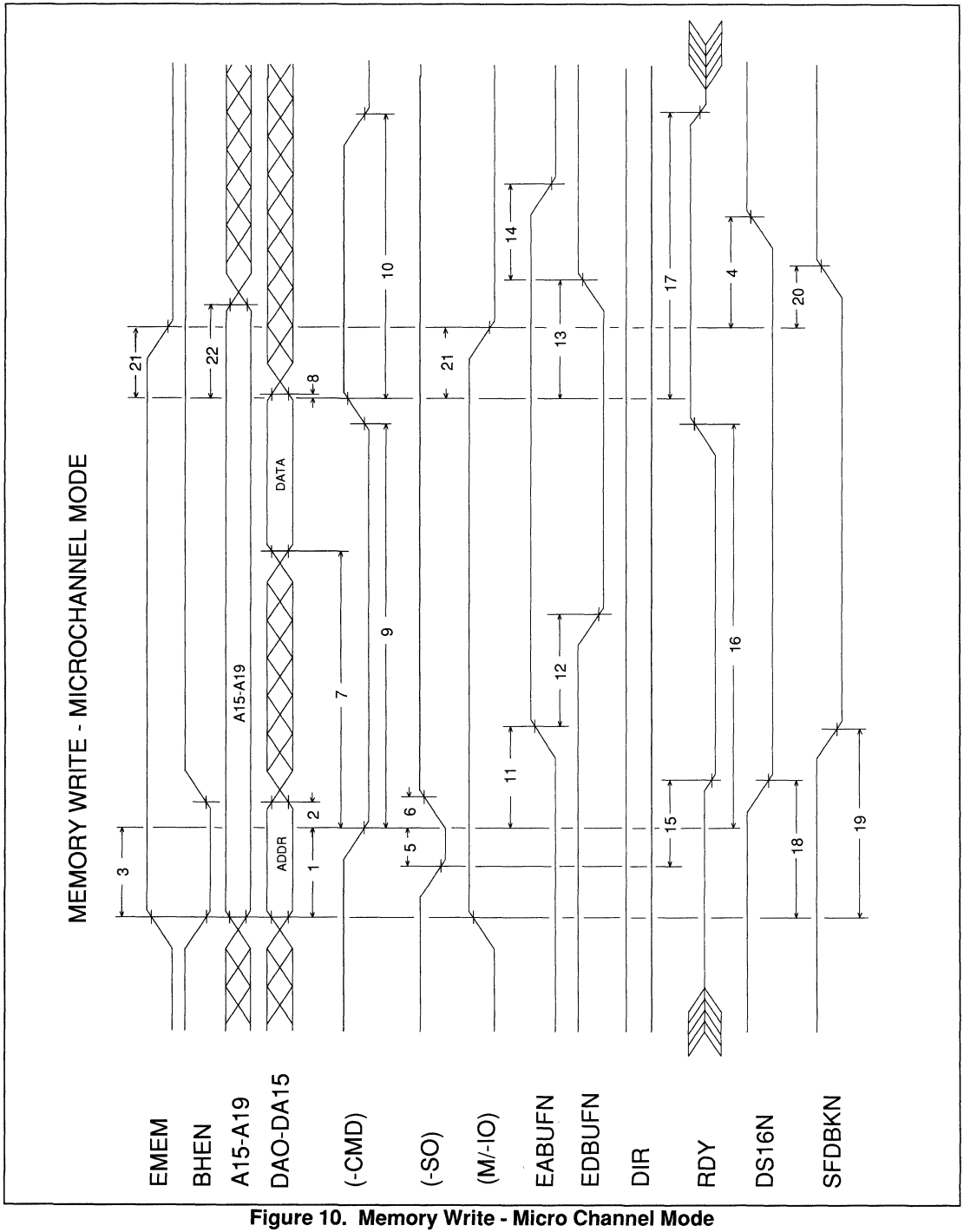


Figure 10. Memory Write - Micro Channel Mode

6.3 VIDEO MEMORY READ - ALPHA MODE TIMING DIAGRAM (See Figure 12)

SYMBOL	PARAMETER	MIN		MAX	NOTES*+
1	Row Address Valid from Clock Low	--		34	1
2	Column Address Valid from Clock High	--		34	1
3	RAS Active from Clock High	--		39	1
4	RAS Inactive from Clock high	--		37	1
5	CAS Active from Clock Low	--		41	1
6	CAS Inactive from Clock Low	--		37	1
7	Read Data Setup to CAS	20	--		
8	Read Data Hold from CAS	0	--		
9	Output Enable Active from Clock Low	--		54	1
10	Output Enable Inactive from Clock Low	--		39	1
11	RAS Refresh Cycle Period	--		7Tp	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Clock is MCLK in any VGA graphics mode, and VCLK0, VCLK1, or VCLK2 in alphanumeric modes depending on clock selection.
2. In refresh cycle, RAS period is 4 clocks active and 3 clocks for precharge.
3. The CAS precharge time is 4 clocks and CAS active time is 3 clocks.
4. Tp = 1 / CLOCK (See note 1.)

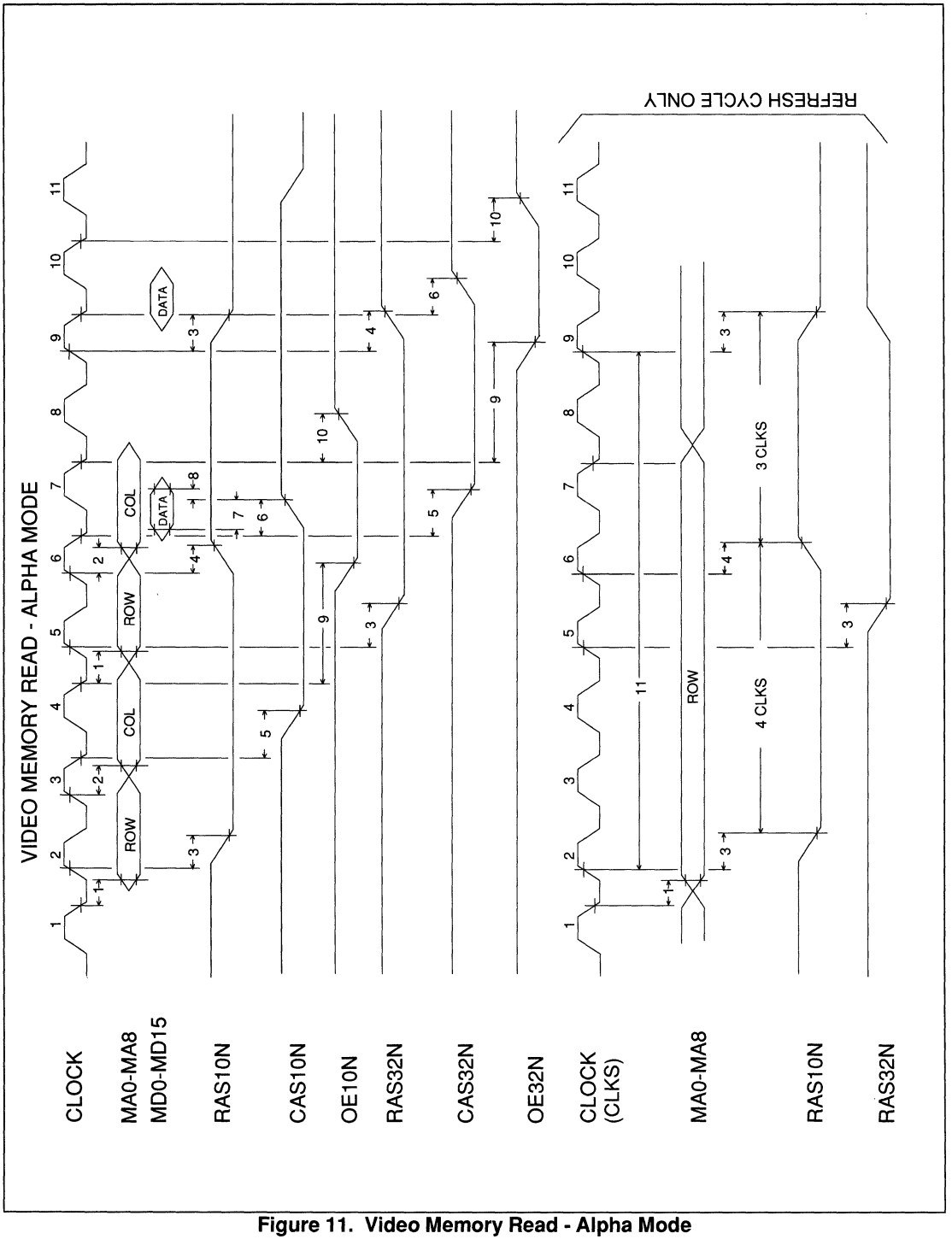


Figure 11. Video Memory Read - Alpha Mode

VIDEO MEMORY WRITE - ALPHA MODE TIMING DIAGRAM (See Figure 13)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Row Address Valid from Clock Low	--	34	1
2	Column Address Valid from Clock High	--	34	1
3	RAS Active from Clock High	--	39	1
4	RAS Inactive from Clock High	--	37	1
5	CAS Active from Clock Low	--	41	1
6	CAS Inactive from Clock Low	--	37	1
7	Write Data Setup to Write Enable	1.5Tp-5	--	1,2
8	Write Data Hold from Write Enable	2Tp	--	1,2
9	Write Enable Active from Clock Low	--	54	1
10	Write Enable Inactive from Clock Low	--	57	1

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Clock is MCLK in any VGA graphics mode, and VCLK0, VCLK1, or VCLK2 in alphanumeric modes depending on clock selection.
2. Tp = 1/CLOCK (See Note 1.)
3. The CAS precharge time is 4 clocks and CAS active time is 3 clocks.

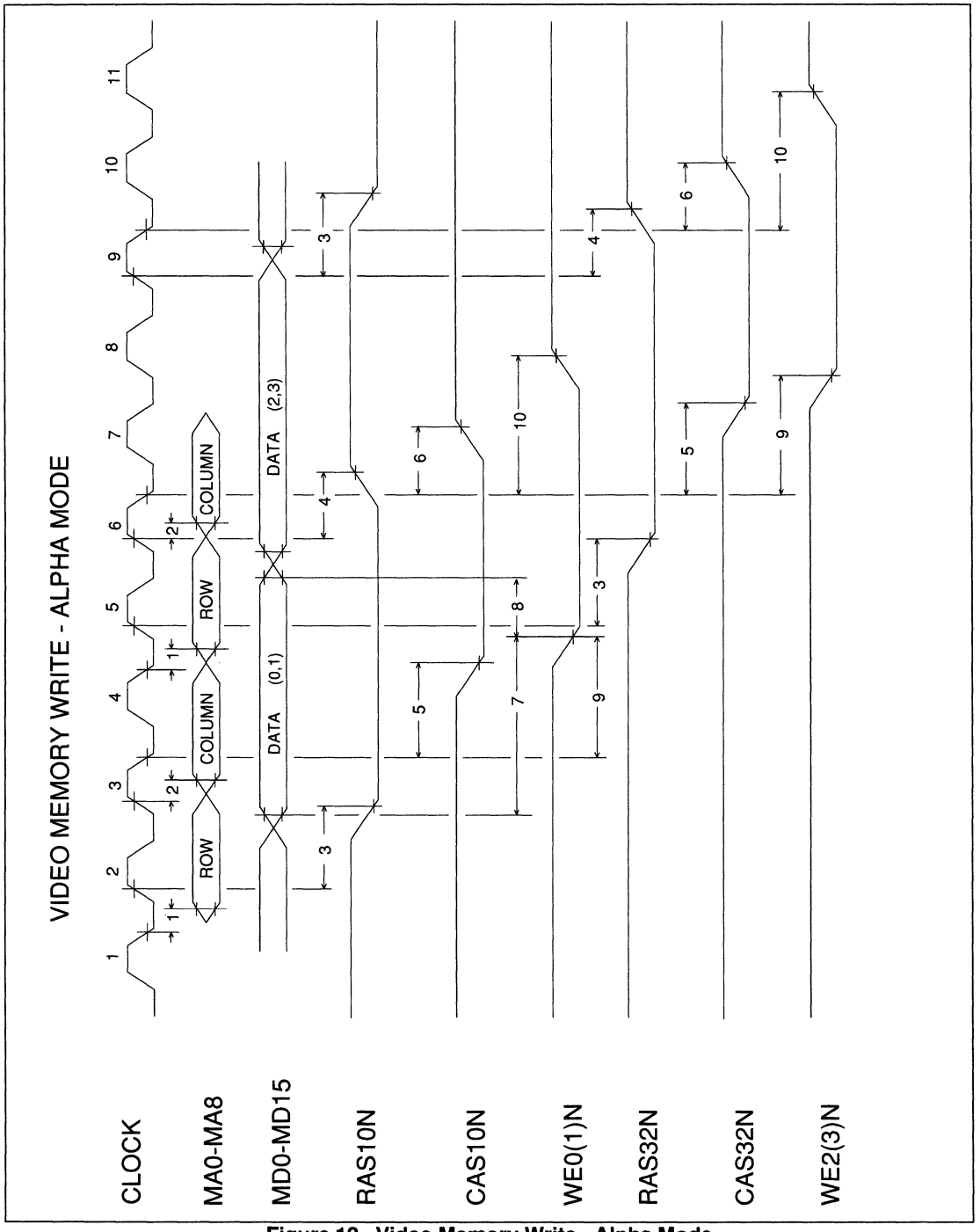


Figure 12. Video Memory Write - Alpha Mode

VIDEO MEMORY READ - GRAPHICS MODE TIMING DIAGRAM (See Figure 14)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Row Address Valid from Clock Low	--	35	1
2	Column Address Valid from Clock High	--	35	1
3	RAS Active from Clock High	--	36	1
4	RAS Inactive from Clock Low	--	34	1
5	CAS Active from Clock	--	36	1,3
6	CAS Inactive from Clock	--	34	1,3
7	Read Data Setup to CAS	20	--	
8	Read Data Hold from CAS	0	--	
9	Output Enable Active from Clock	--	36	1
10	Output Enable Inactive from Clock	--	34	1
11	RAS Refresh Cycle Period	--	10Tp	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Clock is MCLK in any VGA graphics mode, and VCLK0, VCLK1, or VCLK2 in alphanumeric modes depending on clock selection.
2. In refresh cycle, RAS period is 6.5 clocks active and 3.5 clocks for precharge.
3. CAS10N is referenced to Clock Low and CAS32N to Clock High.
4. The CAS precharge time is 4 clocks and CAS active time is 3 clocks.

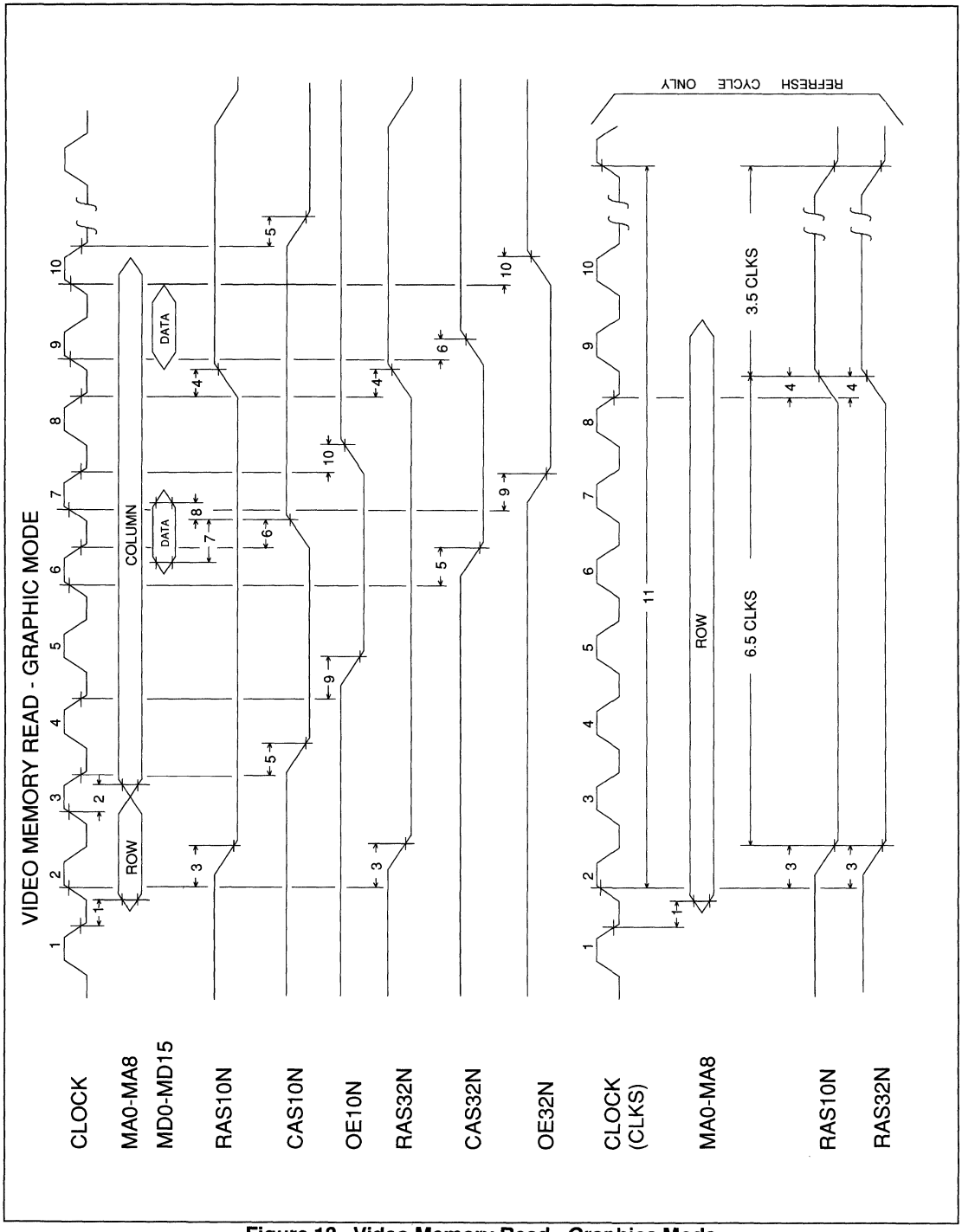


Figure 13. Video Memory Read - Graphics Mode

VIDEO MEMORY WRITE - GRAPHICS MODE TIMING DIAGRAM (See Figure 15)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Row Address Valid from Clock Low	--	35	1
2	Column Address Valid from Clock High	--	35	1
3	RAS Active from Clock High	--	36	1
4	RAS Inactive from Clock Low	--	34	1
5	CAS Active from Clock	--	36	1,3
6	CAS Inactive from Clock	--	34	1,3
7	Write Data Setup to Write Enable	1.5Tp-5	--	1,2
8	Write Data Hold from Write Enable	1.5Tp	--	1,2
9	Write Enable Active from Clock	--	50	
10	Write Enable Inactive from Clock	--	48	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Clock is MCLK in any VGA graphics mode, and VCLK0, VCLK1, or VCLK2 in alphanumeric modes depending on clock selection.
2. Tp = 1/CLOCK (See Note 1.)
3. CAS10N is referenced to Clock Low and CAS32N to Clock High.

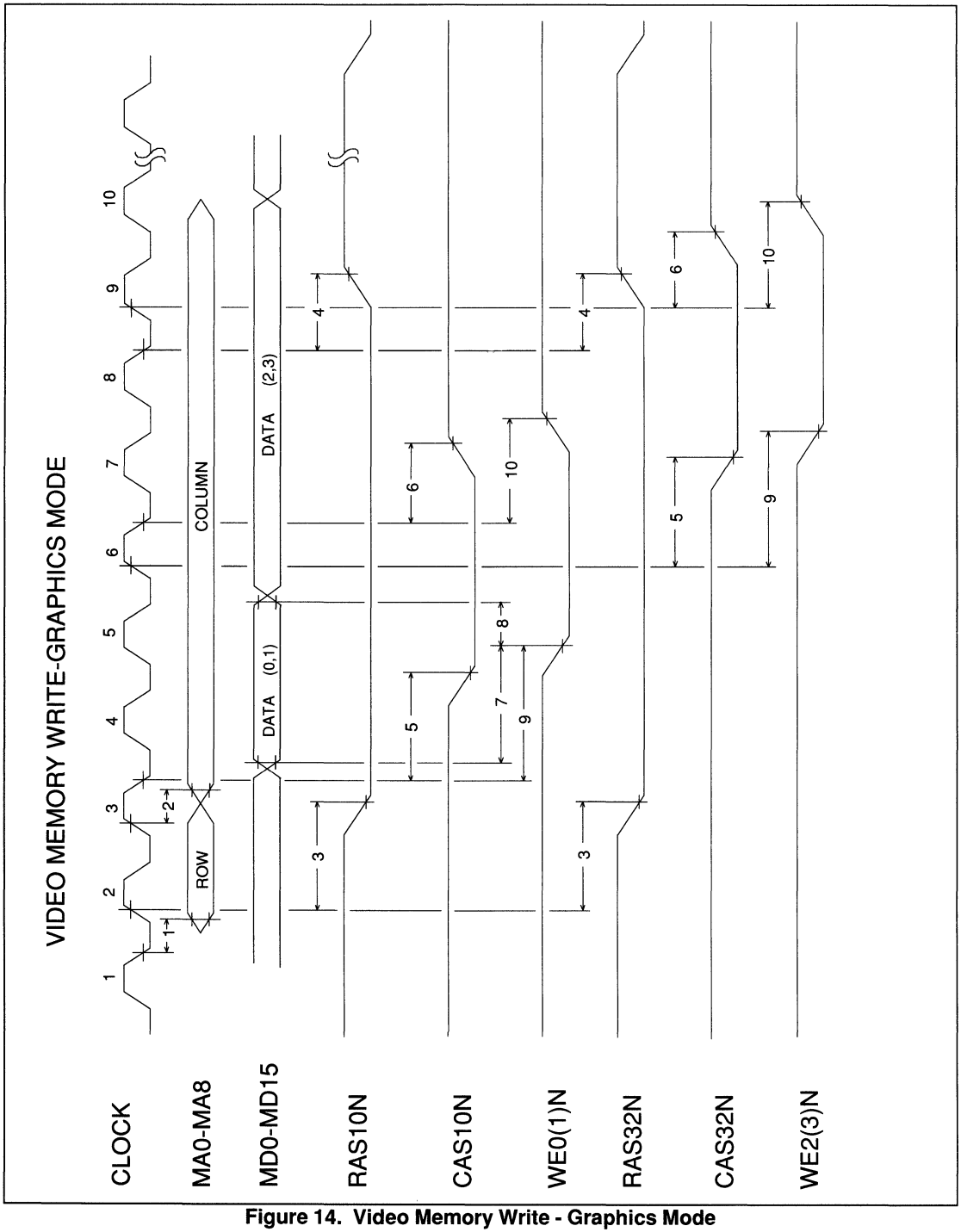


Figure 14. Video Memory Write - Graphics Mode

VIDEO MEMORY PAGE READ - GRAPHICS MODE TIMING DIAGRAM (See Figure 16)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Row Address Valid from Clock Low	--	35	1,2
2	Column Address Valid from Clock High	--	35	1,2
3	RAS Active from Clock High	--	36	1,2
4	RAS Hold from Clock Low	--	34	1,2
5	CAS Active from Clock Low	--	36	2
6	CAS Hold from Clock High	--	34	2
7	Output Enable Active from Clock Low	--	36	2
8	Data Hold from CAS	0	--	
9	Data setup from CAS	22	--	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Clock is MCLK in any VGA graphics mode.
2. See Video Memory Read - Graphics Timing Diagram.
3. The CAS precharge time is 4 clocks and CAS active time is 3 clocks.

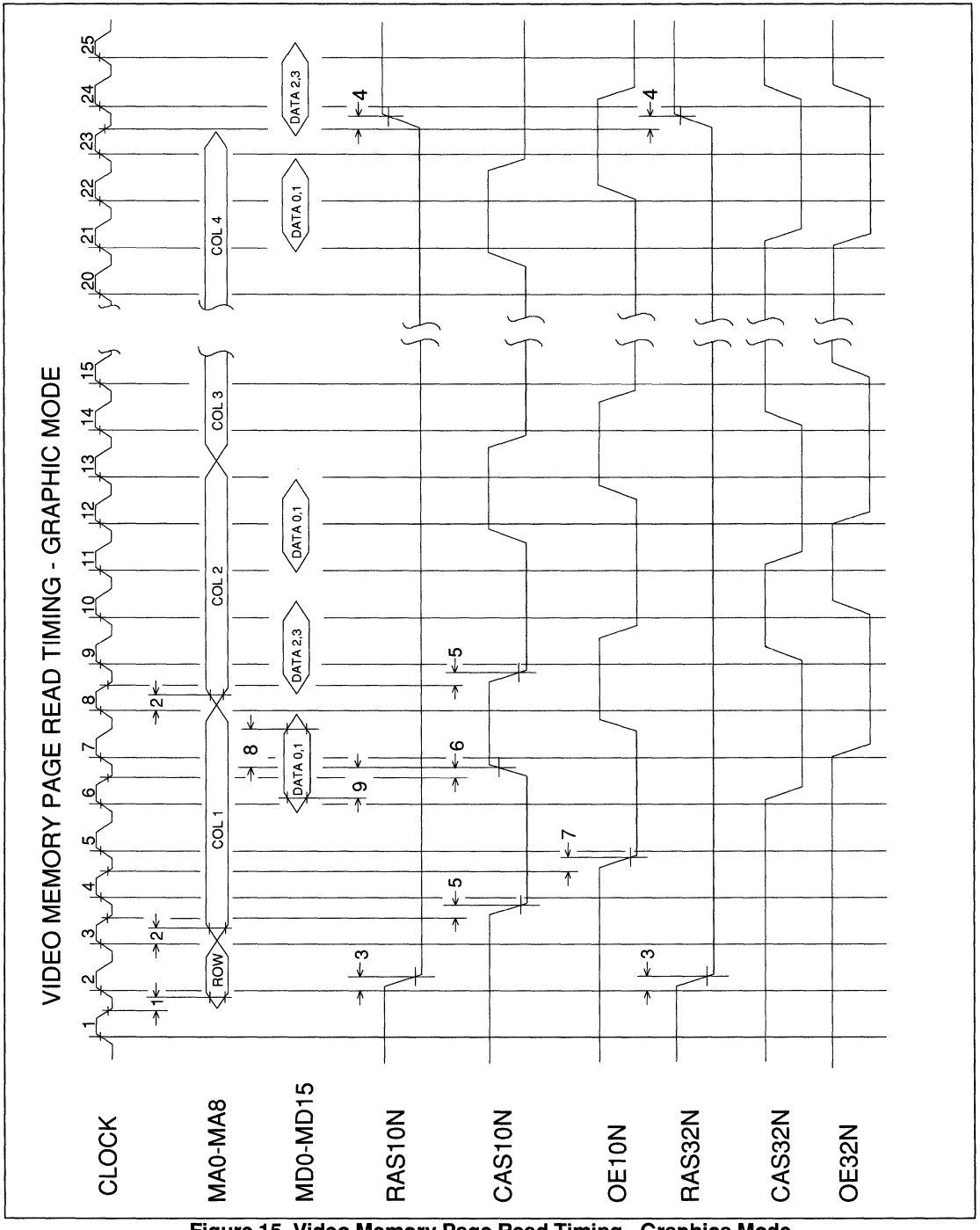


Figure 15. Video Memory Page Read Timing - Graphics Mode

6.4 CLOCK AND VIDEO SIGNALS TIMING DIAGRAM(See Figure 17)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	MCLK Clock Period	23.8	--	1
2	MCLK Clock High Time	10.7	--	
3	MCLK Clock Low Time	10.7	--	
4	VCLK0, VLCK1, VCLK2 Clock Period	25	--	1
5	VCLK0, VLCK1, VCLK2 Clock Low Time	11.2	--	
6	VCLK0, VLCK1, VCLK2 Clock High Time	11.2	--	
7	PCLK Low from VCLK High	--	30	5
8	BLNKN Active Delay from VCLK	--	37	
9	BLNKN Inactive Delay from VCLK	--	38	
10	VSYNC Active Delay from VCLK	--	37	2
11	VSYNC Inactive Delay from VCLK	--	37	2
12	HSYNC Active Delay from VCLK	--	34	2
13	HSYNC Inactive Delay from VCLK	--	38	2
14	VID(7:0) Data from VCLK	--	30	5

NOTES:

* Units are in nanoseconds (ns)

1. Input clocks require a 50% duty cycle with a tolerance of 10 %.
2. VSYNC and HSYNC polarity is positive or negative depending on video mode.
3. PCLK / 2 is for 40 x 25 alpha modes or 320 x 200 x 256 color graphics modes.
4. C_L for VID(0:7) and PCLK is 30 pF.
5. There is a limit on the maximum skew between video clock and data outputs. With respect to the falling edge of PCLK, the delay of VID(0:7) output will not exeed + / - 5ns at 1.4V output level.
6. Duty cycle variations from VCLK to PCLK:
   Values are referenced to a input 50% waveform from 0.8V to 2.0V, 30pF load, and 1.3V threshold.
   High pulse width = Input width - 1.5ns Min
   Input width + 3.2ns Max
   Low pulse width = Input width - 3.2ns Min
   Input width + 1.5ns Max

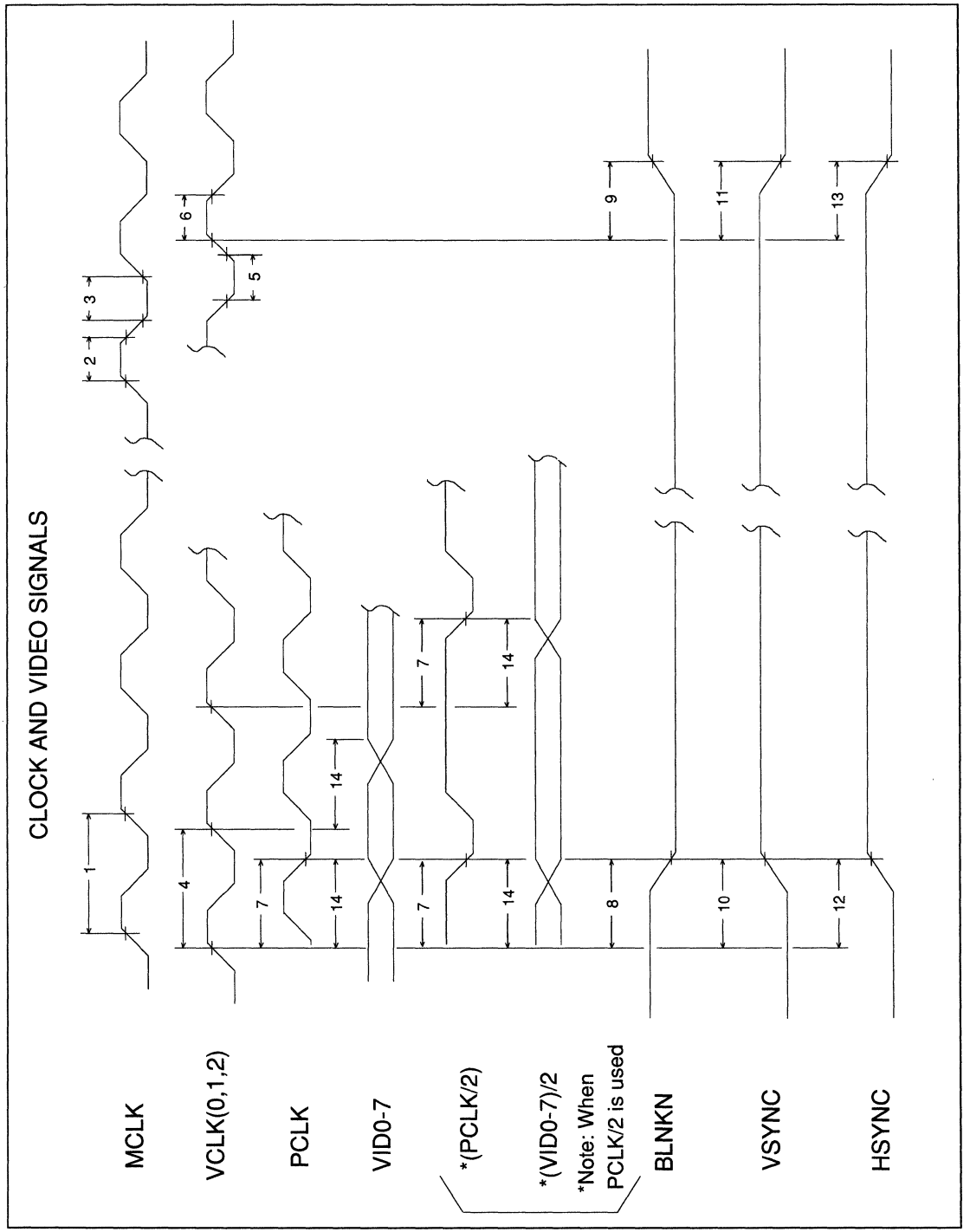


Figure 16. Clock and Video Signals

7.0 PVGA1A REGISTERS

All the standard IBM registers incorporated inside the PVGA1A are functionally equivalent to the VGA implementation while additional Paradise registers enhance the VGA video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards defined earlier using the 6845 CRT Controller. This section describes the VGA registers in greater detail followed by the Paradise register description. For more information, refer to the reference literature.

VGA REGISTERS SUMMARY

	R/W	Monochrome	Color	Either
General Registers:				
Miscellaneous Output Reg	W			03C2
	R			03CC
Input Status Reg 0	RO			03C2
Input Status Reg 1	RO	03BA	03DA	
Feature Control Reg	W	03BA	03DA	
	R			03CA
‡Video Subsystem Enable	RW			03C3
Sequencer Registers:				
Sequencer Index Reg	RW			03C4
Sequencer Data Reg	RW			03C5
CRT Controller Registers:				
Index Reg	RW	03B4	03D4	
CRT Controller Data Reg	RW	03B5	03D5	
Graphics Controller Registers:				
Index Reg	RW			03CE
Other Graphics Reg	RW			03CF
Attribute Controller Registers:				
Index Reg	RW			03C0
Attribute Controller Data Reg	W			03C0
	R			03C1

NOTES: 1. **RO** = Read-Only, **RW** = Read/Write, **WO** = Write-Only. All Register addresses are in hex.
2. ‡ = Video Subsystem Enable Register 03C3 is to be implemented externally since it is not present inside the PVGA1A for Microchannel implementations.

PARADISE REGISTERS SUMMARY

	R/W	Monochrome	Color
Paradise Register Index	R/W	-----	03CE
PR0(A) Address Offset A	R/W	-----	03CF.09
PR0(B) Address Offset B	R/W	-----	03CF.0A
PR1 Memory Size	R/W	-----	03CF.0B
PR2 Video Select	R/W	-----	03CF.0C
PR3 CRT Control	R/W	-----	03CF.0D
PR4 Video Control	R/W	-----	03CF.0E
PR5 Lock/Status	R/W	-----	03CF.0F
** CNF Configuration	-----	-----	-----

COMPATIBILITY REGISTERS SUMMARY

	R/W	MDA	CGA	AT&T	Hercules
Mode Control Reg	WO	03B8	03D8	03D8	03B8
Color Select Reg	WO	-----	03D9	03D9	-----
Status Reg	RO	03BA	03DA	03DA	03BA
Preset Light Pen Latch	WO	03B9	03DC	03DC	-----
Clear Light Pen Latch	WO	03BB	03DB	03DB	-----
AT&T / M24 Reg	WO	-----	-----	03DE	-----
Hercules Reg	WO	-----	-----	-----	03BF
+ CRTC	RW	03B0-03B7	03D0-03D7	03D0-03D7	03B0-03B7

NOTES:
1. **RO** = Read-Only, **RW** = Read/Write, **WO** = Write-Only. All Register addresses are in hex.
2. **+** = 6845 Mode Registers
3. ** = This register is loaded during power on.

19

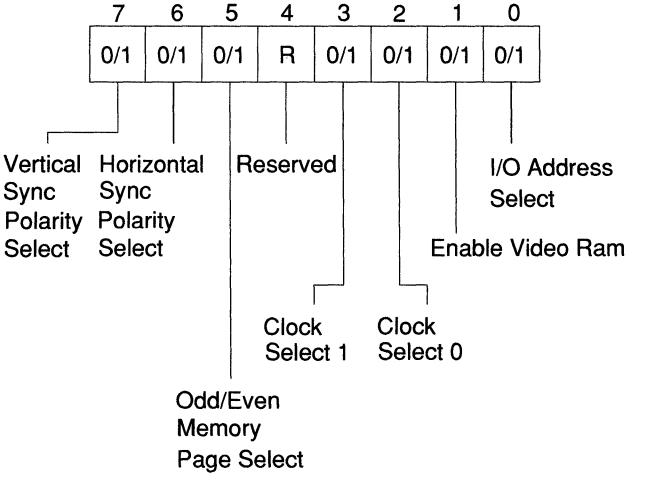
7.1 GENERAL REGISTERS

Name	Read Port	Write Port
Miscellaneous Output	03CC	03C2
Input Status Register 0	03C2	----
Input Status Register 1	03?A	03?A
Feature Control	03CA	03?A

NOTES:

1. Reserved bits should be set to zero.
2. " ? " Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below :
   ? = B in Monochrome Emulation Modes
   ? = D in Color Emulation Modes

Miscellaneous Output Register: Read Port = 03CC Write Port = 03C2



* Bit 7 Vertical Sync Polarity Selection.
  0 = Positive vertical sync polarity.
  1 = Negative vertical sync polarity.

* Bit 6 Horizontal Sync Polarity Selection.
  0 = Positive horizontal sync polarity
  1 = Negative vertical sync polarity.

Note: * These bits are determined by the monitor type. Their encoding is shown below:

Bit 7	Bit 6	Vertical Frame
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

MISCELLANEOUS OUTPUT REGISTER (contd)

Bit 5 Odd or Even Memory Page Select. When in modes 0 - 5 the page size is 64KB. One memory page is selected from the two 64 Kbyte pages. This bit is used for diagnostic purposes and has no effect if PR1(7) = 1 or PR1(6) = 1.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4 Reserved.

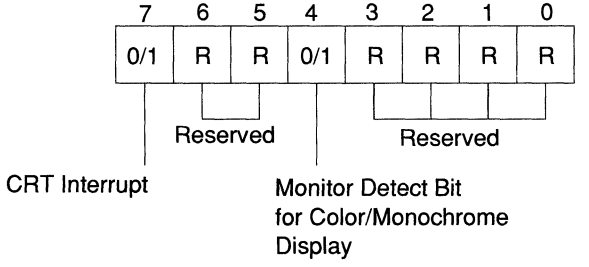
Bit 3, Bit 2 Clock Select 1, 0.

Bit 3	Bit 2	Function
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175MHz).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration
1	1	Register bit 3 = 0. Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

Bit 1 System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0 CRT Controller I/O Address Range Selection.
Selection for MDA (03B4 and 03B5), or CGA (03D4 and 03D5) mode. Bit 0 also maps Input Status Register 1 at MDA (03BA) or CGA (03DA).
0 = CRTC addresses for MDA emulation mode.
1 = CRTC addresses for CGA emulation mode.

INPUT STATUS REGISTER 0 : READ ONLY PORT = 03C2



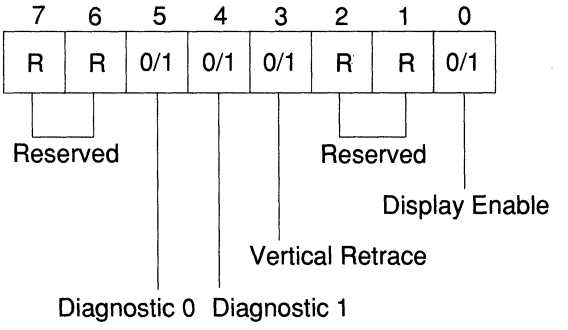
Bit 7 CRT Interrupt Pen ding or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit 6, Bit 5 Reserved.

Bit 4 Monitor Detection.
DA15 monitor status (pin 20) is sampled and can be read from this bit.

Bit 3-Bit 0 Reserved

INPUT STATUS REGISTER 1 : READ ONLY PORT = 03?A



Bit 7, Bit 6 Reserved.

Bit 5, Bit 4 Color Plane Diagnostics.
These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register bits 4 and 5. Their status is defined below:

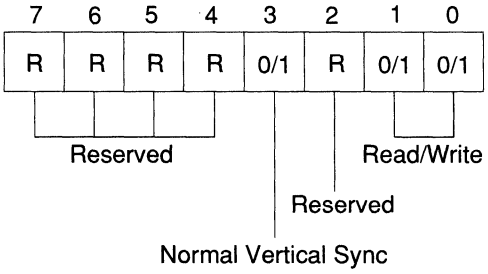
Color Plane Enable Register		Input Status Register 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

Bit 3 Vertical Retrace Status.
0 = Vertical frame is displayed.
1 = Vertical retrace is active.

Bit 2, Bit 1 Reserved.

Bit 0 Display Enable Status.
0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

FEATURE CONTROL REGISTER READ PORT = 03CA WRITE PORT = 03?A



Bit 7 - Bit 4 Reserved.

Bit 3 Normal Vertical Sync.
This bit should always be zero.
0 = Normal vertical sync enabled.
1 = Vertical sync output is the logical OR of vertical sync and vertical display enable.

Bit 2 Reserved.

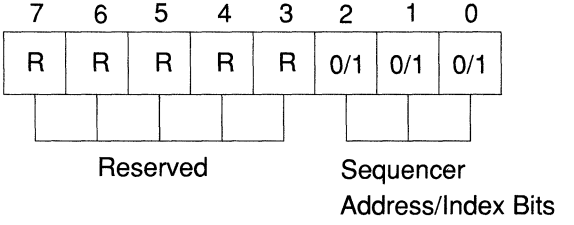
Bit1, Bit 0 Read and write bits.

7.2 SEQUENCER REGISTERS

Name	Port (hex)	Index (hex)
Sequencer Index	03C4	---
Reset	03C5	00
Clocking Mode	03C5	01
Map Mask	03C5	02
Character Map Select	03C5	03
Memory Mode	03C5	04

NOTE: 1. Reserved bits should be set to zero.

SEQUENCER INDEX REGISTER - READ/WRITE PORT = 03C4

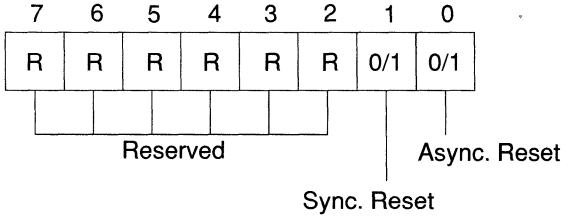


Bit 7 - Bit 3 Reserved.

Bit 2 - Bit 0 Sequencer Address/Index.

The Sequencer Address Register is written with the index value (00H-04H) of the Seqencer register to be accessed.

RESET REGISTER - READ/WRITE PORT = 03C5 AND INDEX REGISTER = 00



Bit 7 - Bit 2 Reserved.

Bit 1 Synchronous Reset.

To prevent loss of data, bit 1 must be set to 0 during active display interval before changing clock selection through clocking mode, or Miscellaneous Output Register.

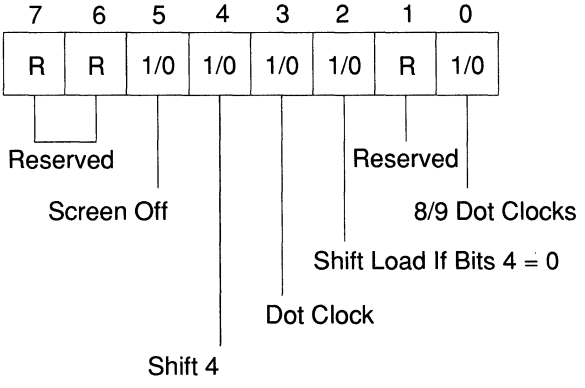
0 = Sequencer is cleared and halted synchronously.

1 = Operational mode (Bit 0 = 1).

RESET REGISTER (contd)

Bit 0 Asynchronous Reset.
Video data can be lost if Sequencer is reset with this bit.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

CLOCKING MODE REGISTER - READ/WRITE PORT 03C5 AND INDEX REGISTER = 01



Bit 7, Bit 6 Reserved.

Bit 5 Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4 Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character clock.
1 = Serial shift registers loaded every 4th character clock (32 bit fetches).

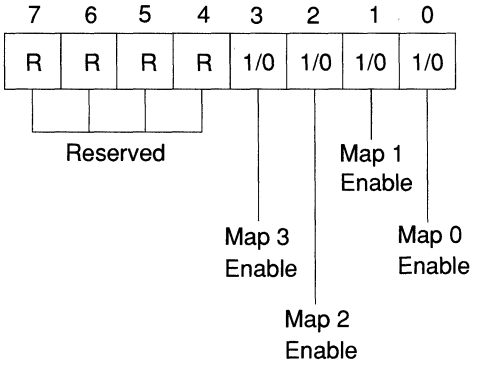
Bit 3 Dot Clock Selection
0 = Normal dot clock selected by VCLK0 input frequency (640 pixels).
1 = Dot Clock divided by 2 (320/360 pixels).

Bit 2 Shift Load.
0 = If bit 4 of this register also equals 0, then video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

Bit 1 Reserved.

Bit 0 8/9 Dot Clock.
Commands Sequencer to generate 8 or 9 dot wide character clock.
0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

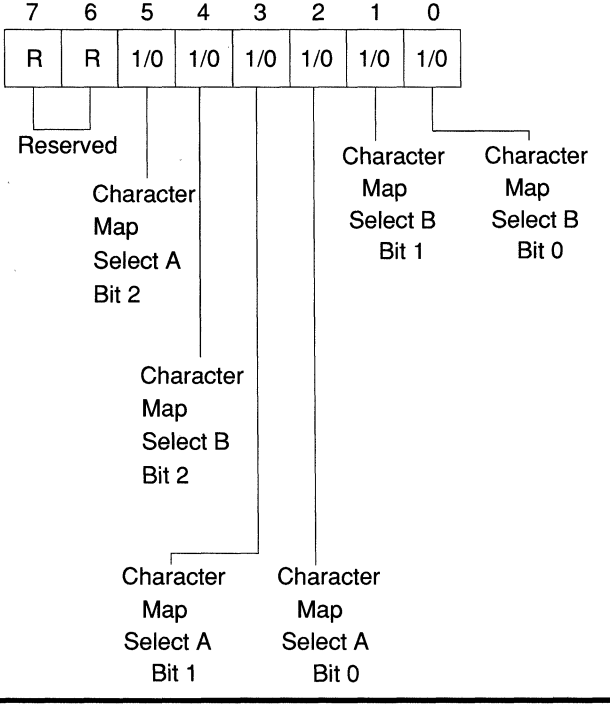
MAP MASK REGISTER - READ/WRITE PORT = 03C5 AND INDEX REGISTER = 02



Bit 7 - Bit 4 Reserved.

Bit 3 - Bit 0 Prohibit Access To Memory Maps (0 - 3).
0 = Access to maps (0 - 3) disallowed.
1 = Maps (0 - 3) accessible.

CHARACTER MAP SELECT REGISTER
READ/WRITE PORT 03C5 AND INDEX REGISTER = 03



CHARACTER MAP SELECT REGISTER (contd)

Bit 7, Bit 6 Reserved.

Bit 5 Character Map A MSB Select.
The Most Significant Bit (MSB) of character map A is defined by bits 3 and 2, containing the character font table shown below:

Bits 5	3	2	Map Selected	Font Table/Plane 2 or 3 Location
0	0	0	0	1st 8KB
0	0	1	1	3rd 8KB
0	1	0	2	5th 8KB
0	1	1	3	7th 8KB
1	0	0	4	2nd 8KB
1	0	1	5	4th 8KB
1	1	0	6	6th 8KB
1	1	1	7	8th 8KB

Bit 4 Character Map B MSB Select.
MSB of character map B is defined by bits 1 and 0, containing the font table described below:

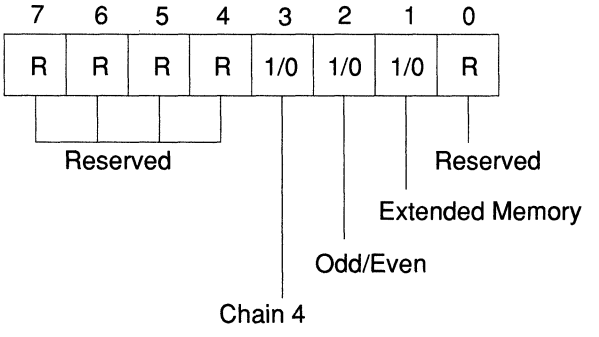
Bits 4	1	0	Map Selected	Font Table/Plane 2 or 3 Location
0	0	0	0	1st 8KB
0	0	1	1	3rd 8KB
0	1	0	2	5th 8KB
0	1	1	3	7th 8KB
1	0	0	4	2nd 8KB
1	0	1	5	4th 8KB
1	1	0	6	6th 8KB
1	1	1	7	8th 8KB

Bit 3, Bit 2 Characer Map Select A.
Refer to bit 5 table.

Bit 1, Bit 0 Character Map Select B.
Refer to bit 4 table.

NOTE: 1. Character Map selection from either Plane 2 or Plane 3 is determined by PR2(2), PR2(5) and bit 4 of the attribute code.

MEMORY MODE REGISTER - READ/WRITE PORT = 03C5 AND INDEX REGISTER = 04



Bit 7 - Bit 4 Reserved.

Bit 3 Chains 4 Maps.
0 = Processor sequentially accesses data using map mask register.
1 = Directs the two lower order video memory address pins (MA0, MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	Map Enabled
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2 Odd/Even Map Selection.
0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.
1 = Sequential processor access as defined by map mask register.

Bit 1 Extended Video Memory.
0 = 64 Kbyte of video memory.
1 = Greater than 64 Kbyte of memory for VGA/EGA modes.

Bit 0 Reserved.

7.3 CRT CONTROLLER REGISTERS

VGA Register Name	*6845 Register Name	Port (hex)	Index (hex)
CRT Controller Address Register	CRT Controller Address Register	03?4	---
Horizontal Total	Horizontal Total	03?5	00
Horizontal Display Enable End	Horizontal Displayed	03?5	01
Start Horizontal Blanking	†-----	03?5	02
End Horizontal Blanking	†-----	03?5	03
Start Horizontal Retrace Pulse	†-----	03?5	04
End Horizontal Retrace	†-----	03?5	05
Vertical Total	Vertical Displayed	03?5	06
Overflow	†-----	03?5	07
Preset Row Scan	†-----	03?5	08
Maximum Scan Line/Others	Maximum Scan Line Address	03?5	09
Cursor Start	Cursor Start	03?5	0A
Cursor End	Cursor End	03?5	0B
Start Address High	Start Address High	03?5	0C
Start Address Low	Start Address Low	03?5	0D
Cursor Location High	Cursor Location High	03?5	0E
Cursor Location Low	Cursor Location Low	03?5	0F
Vertical Retrace Start	Light Pen High	03?5	10
Vertical Retrace End	Light Pen Low	03?5	11
Vertical Display Enable End		03?5	12
Offset		03?5	13
Underline Location		03?5	14
Start Vertical Blank		03?5	15
End Vertical Blank		03?5	16
CRTC Mode Control		03?5	17
Line Compare		03?5	18

NOTES :

1. " ? " Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below :
   ? = B in Monochrome Emulation Modes and
   ? = D in Color Emulation Modes
2. "*" 6845 Mode Registers are defined and explained in greater detail in the reference literature.
3. "†" This register can be programmed in VGA mode only. It is not applicable in 6845 mode.
4. Reserved bits should be set to zero.

CRT CONTROLLER REGISTERS DESCRIPTION

CRT Address Register (Port = 03?4)

Bit 7 - Bit 5 Reserved.

Bit 4 - Bit 0 Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed hex.

†Horizontal Total Register (Port = 03?5, Index = 00H)

Bit 7 - Bit 0 Count Plus Retrace Less 5.
In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line. In 6845 mode the character count is less 1.

†Horizontal Display Enable End Register (Port = 03?5, Index = 01H)

Bit 7 - Bit 0 Displayed Characters Less 1.
Program count of the displayed number of characters less 1 in VGA mode. For 6845 mode, load count of the number of characters to be displayed. Left or right borders and blanking time is excluded.

†Start Horizontal Blanking (Port = 03?5, Index = 02H)

Bit 7 - Bit 0 Character Clock Value.
Horizontal blanking begins when the horizontal character counter reaches this character clock value.

†End Horizontal Blanking (Port = 03?5, Index = 03H)

Bit 7 Reserved.

Bit 6, Bit 5 Display Enable Signal Skew Time.
They define the display enable signal skew time in relation to horizontal or vertical synchronization pulses. The skew table is shown below:

Bit 6	Bit 5	Skew in Character Clocks
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4 - Bit 0 End Horizontal Blank Signal Width.
End horizontal blank signal width "W" is determined as the value of start blanking register plus "W" in character clocks. The least significant five bits are programmed in this register, while the sixth bit is the Retrace Register (index 05H) programmed as bit 7 of the End Horizontal Register.

NOTE: † This register is locked if the Paradise Register PR3(5) = 1 OR the Vertical Retrace End. Register bit 7 = 1.

CRT CONTROLLER REGISTERS DESCRIPTION (contd)

†Start Horizontal Retrace Pulse Register (Port = 03?5, Index = 04H)

Bit 7 - Bit 0 Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active.

†End Horizontal Retrace Register (Port = 03?5, Index = 05H)

Bit 7 MSB (Sixth Bit) Of End Horizontal Blanking Register.

Bit 6, Bit 5 Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

Bit 6	Bit 5	Character Clock Delay
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4 - Bit 0 End Horizontal Retrace Pulse Width "W".
Start retrace register value is added to the character count for width "W". The least significant five bits are programmed in this register. When the Start Horizontal Retrace Register value matches these five bits, the horizontal retrace signal is turned off.

‡Vertical Total Register (Port = 03?5, Index = 06H)

Bit 7 - Bit 0 Raster Scan Line Total Less 2.
The least significant eight bits of a ten bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync is also included. The ninth and tenth bits of this count are loaded into the Vertical Overflow Register (index = 07H) bit 0 and bit 5 respectively. In 6845 modes, total vertical display time in rows is programmed into bit 6 - bit 0, while bit 7 is reserved. Scan count reduction is not necessary. (The number of scan lines in a row is determined by the Maximum Scan Line Register (index 09H) bits 0 thru 4).

Overflow Vertical Register (Port = 03?5, Index = 07H)

‡Bit 7 Vertical Retrace Start Bit 9 (index = 10H).
**Bit 6 Vertical Display Enable End Bit 9 (index = 12H).
‡Bit 5 Vertical Total Bit 9 (index = 06H).
Bit 4 Line Compare Bit 8 (index = 18H).

‡Bit 3 Start Vertical Blank Bit 8 (index = 15H).
‡Bit 2 Vertical Retrace Start Bit 8 (index = 10H).
**Bit 1 Vertical Display Enable End Bit 8 (index = 12H).
‡Bit 0 Vertical Total Bit 8 (index = 06H).

NOTES: † This register is locked if the Paradise Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

** This register is locked if the Paradise Register PR3(1) = 0 AND the Vertical Retrace End Register bit 7 = 1.

‡ This register is locked if the Paradise Register PR3(0) = 1 OR the Vertical Retrace End

19

CRT CONTROLLER REGISTERS DESCRIPTION (contd)

Preset Row Scan Register (Port = 03?5, Index = 08H)

Bit 7 Reserved.

Bit 6, Bit 5 Byte Panning Control.
These bits allow up to 3 bytes to be panned in modes progammed as multiple shift modes.

Bit 6	Bit 5	Operation
0	0	Normal
0	1	1 byte left shift
1	0	2 bytes left shift
1	1	3 bytes left shift

Bit 4 - Bit 0 Preset Row Scan Count.
These bits preset the vertical row scan count once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scroll of text.

Maximum Scan Line Register/ (Port = 03?5, Index = 09H)

Bit 7 200 To 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes to display 400 scan lines (each line is double scanned).

Bit 6 Line Compare.
This is bit 9 of the Line Compare Register (index = 18H).

§ Bit 5 Start Vertical Blank.
This is bit 9 of the Start Vertical Blank Register (index = 15H).

Bit 4 - Bit 0 Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, bits 5-7 are reserved, and bits 4-0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported.

Cursor Start Register (Port = 03?5, Index = 0AH)

Bit 7, Bit 6 Reserved.

Bit 5 Cursor Control.
0 = Cursor on.
1 = Cursor off.

Bit 4 - Bit 0 These bits specify the row within the character box where the cursor begins.
These bits contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0BH), no cursor is generated. For 6845 modes, bit 7 is reserved. Bit 5 controls the cursor operation and bits 4-0 contain the cursor start value. Bit 6 is not used.

NOTE: § This register is locked if the Paradise Register PR3(0) = 1.

CRT CONTROLLER REGISTERS DESCRIPTION (contd)

Cursor End Register (Port = 03?5, Index = 0BH)

Bit 7 Reserved.

Bit 6, Bit 5 Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the table below:

Bit 6	Bit 5	Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4 - Bit 0 These bits specify the row within the character box where the cursor ends.
These bits contain the value of character row less 1. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, bits 7-5 are reserved and bits 4-0 contain row value of the cursor end.

Start Address High Register (Port 03?5H, Index = 0CH)

Bit 7 - Bit 0 Display Screen Start Address Upper Byte Bits.
Eight high order bits of the 16 bit video memory address, used for screen refresh. The low order eight bit register is at index 0DH. The Paradise Register PR3 bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes bits 6 and 7 are forced to 0 regardless of this register's contents, while the lower order 8 bits are at index register 0DH.

Start Address Low Register (Port = 03?5H, Index = 0DH)

Bit 7 - Bit 0 Display Screen Start Address Lower Byte Bits.
The lower order eight bits of the 16 bit video memory address in VGA or 6845 modes.

Cursor Location High Register (Port = 03?5, Index = 0EH)

Bit 7 - Bit 0 Cursor Address Upper Byte Bits.
The eight higher order bits of 16-bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0F. In VGA mode, the Paradise Register PR3 bits 3 and 4 extend the Cursor Location High Register to 18 bits. For 6845 modes, bits 6 and 7 are reserved, while bits 5 - 0 are the high order bits of the cursor.

Cursor Location Low Register (Port = 03?5, Index = 0FH)

Bit 7 - Bit 0 Cursor Address Lower Byte Bits.
The lower order eight bits of the 16-bit video memory address in VGA or 6845 modes.

CRT CONTROLLER REGISTERS DESCRIPTION (contd)

§Vertical Retrace Start Register (Port = 03?5, Index = 10H)

Bit 7 - Bit 0 Vertical Retrace Start Pulse Lower Eight Bits.
The lower eight bits of the ten bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07H). In 6845 or EGA compatible mode, this register shows the high order six bits in positions 5-0 as the **light pen** read back value, and bits 6 and 7 are reserved. The lower order eight bits of the **light pen** read back register are at index 11H.

§Vertical Retrace End Register (Port = 03?5, Index = 11H)

Bit 7 CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller index registers in the range of 00H-07H. The line compare bit 4 in the Overflow Register (07H) is not protected.

Bit 6 DRAM Refresh /Horizontal Scan Line.
Selects 5 DRAM refresh cycles per horizontal scan line.
0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan lines for 15.75 KHZ display monitors.

Bit 5 Enable Vertical Retrace Interrupt.
0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4 Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by reseting (writing a 0 to) an internal flip-flop.
1 = Vertical retrace interrupt. Sets (writes a 1 to) an internal flip-flop after clearing interrupt, to prepare for next interrupt. The flip-flop must be set or it will hold interrupts inactive.

Bit 3 - Bit 0 Vertical Retrace End.
They specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan count for "W" to the value of the Vertical Retrace Start Register. The 4 bit result is written in the Vertical Retrace End Register. In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of the **Light Pen Register**.

Vertical Display Enable End Register (Port = 03?5, Index = 12H)

Bit 7 - Bit 0 Vertical Display Enable End Lower Eight Bits.
The eight lower bits of ten bit register that defines where the active display frame ends. The programmed count is in scan lines minus 1. Bits 8 and 9 are in the Overflow Register (index 07H) at positions 1 and 6, respectively.

NOTE: § This register is locked if the Paradise Register PR3(0) = 1.

CRT CONTROLLER REGISTERS DESCRIPTION (contd)

Offset Register (Port = 03?5, Index = 13H)

Bit 7 - Bit 0 Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:
Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K = 2 in byte mode and K = 4 in word mode.

Underline Location Register (Port = 03?5, Index = 14H)

Bit 7 Reserved.

Bit 6 Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5 Count By 4 For Doubleword Access.
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit 4 - Bit 0 Underline Location.
These bits specify the scan line within a character matrix where underline is to be displayed. Load a value 1 less than the desired scan line number.

§Start Vertical Blank Register (Port = 03?5, Index = 15H).

Bit 7 - Bit 0 Start Vertical Blank Lower Eight Bits.
The lower eight bits of the ten bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). The ten bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

§End Vertical Blank Register (Port = 03?5, Index = 16H)

Bit 7 - Bit 0 Vertical Blank Inactive Count.
End Vertical Blank is an 8 bit value calculated as follows:

8-Bit End Vertical Blank value =
(value of Start Vertical Blank minus 1) + (value of Vertical Blank signal in scan lines).

NOTE: § This register is locked if the Paradise Register PR3(0) = 1.

CRT CONTROLLER REGISTERS DESCRIPTION (contd)

CRT Mode Control Register (Port = 03?5, Index = 17H)
This register is locked if Paradise Register PR3(5) = 1.

Bit 7 Hardware Reset.
0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6 Word Or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by 1 bit and the MSB of the address counter appears on the LSB. See the table below.
1 = Byte address mode.

Memory Address	Byte Address Mode	Word Address Mode	Doubleword Address Mode
MA0/RF0	MA0	* MA15 or MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE: * See bit 5, defining address wrap. This table is only applicable when Paradise Register PR1 bits 7 and 6 are zero.

The CRT Underline Location Register (index = 14H) bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) bit 6 controls addressing. See the table below:

CRT14H Bit 6	CRT17H Bit 6	Address Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5 Address Wrap.
0 = In word address mode, this bit enables bit 13 or bit 15 to appear at MA0, otherwise bit 0 appears on MA0.
1 = Select MA15 for odd/even mode when 256KB of video memory is used on the system board. Bit MA13 is used in applications which do not use system board memory for CGA compatibility.

CRT CONTROLLER REGISTERS DESCRIPTION (contd)

CRT Mode Control Register (contd)

Bit 4 Reserved.

Bit 3 Count By Two
0 = Character clock increments memory address counter.
1 = Character clock divided by 2 increments address counter. Selects byte or word refresh address of the display memory.

Bit 2 Horizontal Retrace Clock Rate Select For Vertical Timing Counter.
0 = Selects horizontal retrace clock rate.
1 = Selects horizontal retrace clock rate divided by 2.

Bit 1 Select Row Scan Counter.
0 = Selects row scan counter bit 1 as output at MA14 address pin.
1 = Selects bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0 6845 CRT Controller compatibility mode support for CGA operation.
0 = Row scan address bit 0 is substituted for memory address bit 13 at MA13 output pin during active display time.
1 = Enable memory address pin 13 to be output at MA13 address pin.

Line Compare Register (Port = 03?5, Index = 18H)

Bit 7 - Bit 0 Line Compare Lower Eight Bits.

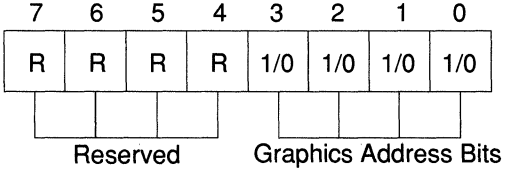
Lower eight bits of the ten bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared.

7.4 GRAPHICS CONTROLLER REGISTERS

Name	Port (Hex)	Index (Hex)
Graphics Index Register	03CE	---
Set / Reset	03CF	00
Enable Set/ Reset	03CF	01
Color Compare	03CF	02
Data Rotate	03CF	03
Read Map Select	03CF	04
Graphics Mode Register	03CF	05
Miscellaneous Register	03CF	06
Color Don't Care	03CF	07
Bit Mask Register	03CF	08

NOTE: 1. Reserved bits should be set to zero.

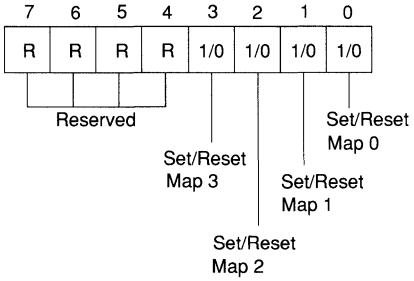
GRAPHICS INDEX REGISTER - READ/WRITE PORT = 03CE



Bit 7 - Bit 4 Reserved.

Bit 3 -Bit 0 Graphics Controller Register Index Pointer Bits.
Note that all the Paradise registers reside with the index pointer extension beyond graphics Controller registers.

SET / RESET REGISTER - READ / WRITE PORT 03CF AND INDEX REGISTER = 00



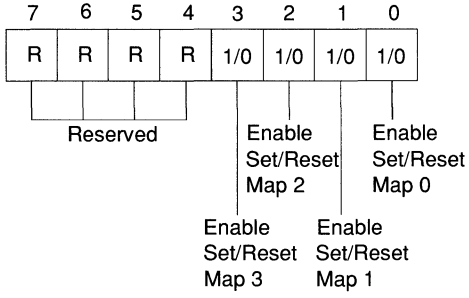
Bit 7 - Bit 4 Reserved.

Bit 3 - Bit 0 Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined below:
0 = Reset.
1 = Set.

Bit	Set/Reset
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE: *The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05H) bit 1 and bit 0.

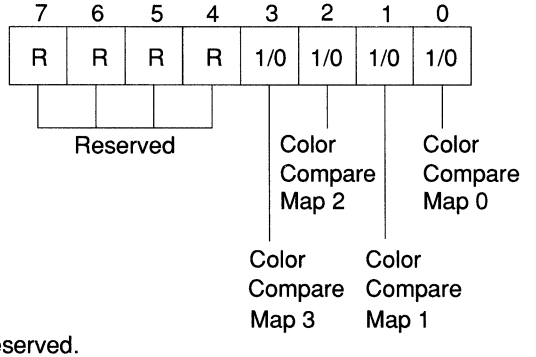
ENABLE SET / RESET REGISTER - READ/WRITE PORT = 03CF AND INDEX REGISTER = 01



Bit 7 - Bit 4 Reserved.

Bit 3 - Bit 0 Enable The Set/Reset Register (Index = 00H).
0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00H) memory map access and the map is written with the rotated 8-bit data value of the system microprocessor.
1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00H), and the respective memory map is written with the Set/Reset Register value.

COLOR COMPARE REGISTER - READ/WRITE PORT 03CF AND INDEX REGISTER = 02

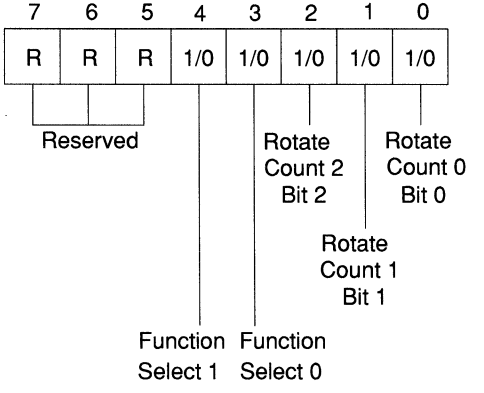


Bit 7 - Bit 4 Reserved.

Bit 3 - Bit 0 Color Compare.
The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a 1 is returned for the map positions where the bits of all four maps equal their corresponding color compare value.
When read mode bit 3 in the Graphics Mode Register (index = 05H) is set to 1 and the system does a memory read, a 1 will be returned for each bit where the four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05H), data is returned without comparison. Color compare map coding is shown below:

Bit	Color Compare
3	Map 3
2	Map 2
1	Map 1
0	Map 0

DATA ROTATE REGISTER - READ/WRITE PORT = 03CF AND INDEX REGISTER = 03



Bit 7 - Bit 5 Reserved.

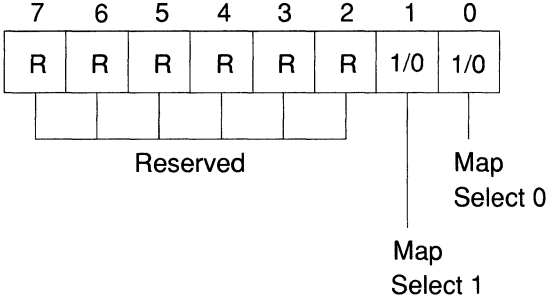
Bit 4, Bit 3 Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05H) is defined as follows:

DATA ROTATE REGISTER (contd)

Bit 4	Bit 3	Function
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches

Bit 2 - Bit 0 Rotate Count.
It specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05H).

READ MAP SELECT REGISTER - READ/WRITE PORT = 03CF AND INDEX REGISTER = 04



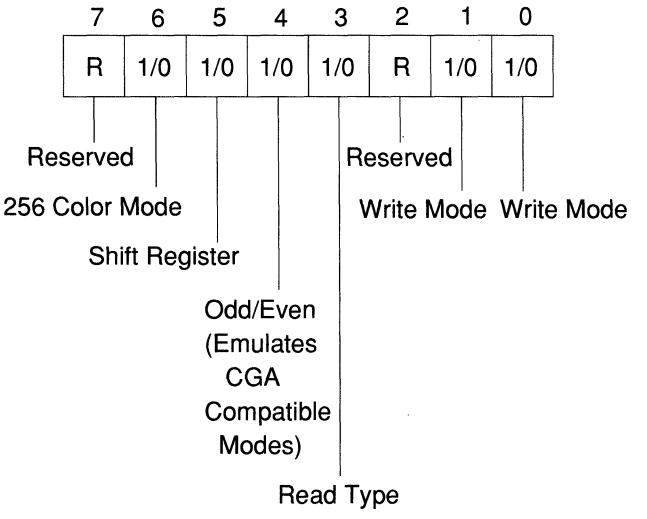
Bit 7 - Bit 2 Reserved.

Bit1, Bit 0 Map Select.
These bits select memory map in system read operations. It has no effect on color compare read mode. Map read is defined as shown under:

Bit 1	Bit 0	Read Map
0	0	0
0	1	1
1	0	2
1	1	3

19

GRAPHICS MODE REGISTER - READ/WRITE PORT = 03CF AND INDEX REGISTER = 05



Bit 7 Reserved.

Bit 6 256 Color Mode.
0 = Enables bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID6, VID7) are determined by bits 2 and 3 of the Color Select Register located at index = 14H within the Attribute Controller.
1 = Load video shift registers to support 256 color mode.

Bit 5 Shift Register.
Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.
0 = Map 0 - Map 3 data is placed into shift registers for normal operations.
1 = For CGA graphics mode compatibility, even numbered bits from all the maps are shifted out of the even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4 Odd/Even Mode.
0 = normal
1 = CGA compatible odd/even system access mode. Sequential addressing as defined by bit 2 of the memory mode register (index = 04H) in the Sequencer Register. Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3 Read Mode.
0 = System reads data from memory maps selected by Read Map Select Register (index 04H). This setting will have no effect if bit 3 of the Sequencer Memory Mode Register = 1.
1 = System reads the comparison of the memory maps and the Color Compare Register.

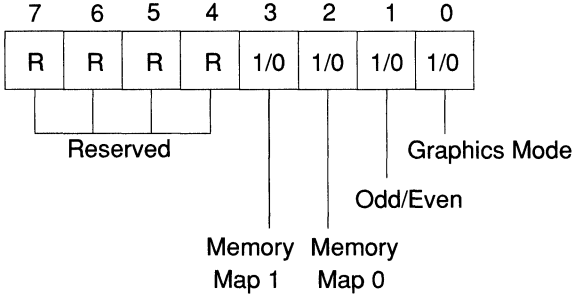
Bit 2 Reserved.

GRAPHICS MODE REGISTER (contd)

Bit 1, Bit 0 Write Mode.
The following table defines the four write modes.

Bit 0	Bit 1	Write Mode
0	0	Write Mode 0. If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	Write Mode 1. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	Write Mode 2. Memory maps (3 : 0) are filled with the 8-bit value of the corresponding CPU data bits (3 : 0). The 32 bit output of the four memory maps is operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	Write Mode 3. Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

MISCELLANEOUS REGISTER - READ/WRITE PORT = 03CF AND INDEX REGISTER = 06



Bit 7 - Bit 4 Reserved.

MISCELLANEOUS REGISTER (contd)

Bit3, Bit 2 Memory Map 1, 0
Display memory map control into the CPU address space is shown below:

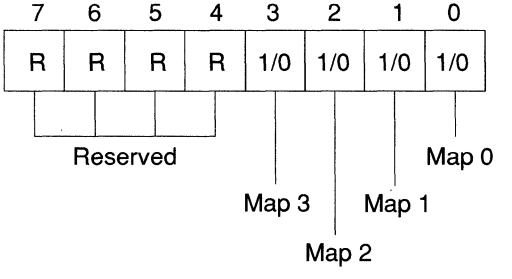
Bit 3	Bit 2	CPU Address Range	Length
0	0	A0000 - BFFFFH	128KB
0	1	A0000 - AFFFFH	64KB
1	0	B0000 - B7FFFH	32KB
1	1	B8000 - BFFFFH	32KB

Bit 1 Odd/Even Mode.
0 = CPU address bit A0 is output on PVGA1A memory pin MA0.

1 = CPU address bit A0 is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0 Graphics/Alphanumeric Mode
This bit is programmed the same way as bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selected.
1 = Graphics mode selected.

COLOR DON'T CARE REGISTER - READ/ WRITE PORT 03CF AND INDEX REGISTER = 07

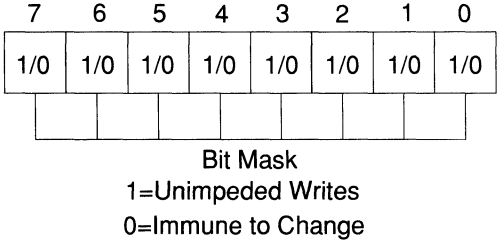


Bit 7 - Bit 4 Reserved.
Bit 3 - Bit 0 Memory Map Color Compare Operation.
Map coding is shown below:

	Bit 3	Bit 2	Bit 1	Bit 0
Map #	3	2	1	0

0 = Disable color compare operation.
1 = Enable color compare operation.

BIT MASK REGISTER - READ/WRITE PORT = 03CF AND INDEX REGISTER = 08



Bit 7 - Bit 0 Bit mask.
Bit mask operation applies simultaneously to all the four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable.

1 = Bit position value is unmasked and can be changed in the corresponding map.

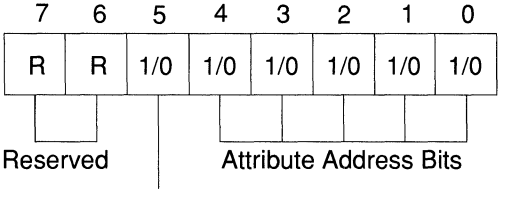
7.5 ATTRIBUTE CONTROLLER REGISTERS

Name	Port (Hex)	Index (Hex)
Index Register	03C0	---
Palette Registers	03C0	00---0F
Attribute Mode Control Register	03C0	10
Overscan Control Register	03C0	11
Color Plane Enable Register	03C0	12
Horizontal PEL Panning Register	03C0	13
Color Select Register	03C0	14

NOTES: 1. Each attribute data register is written at 03C0 and register data is read from address 03C1.
2. Reserved bits should be set to zero.
3. ? " Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below :

? = B in Monochrome Emulation Modes and
? = D in Color Emulation Modes

ATTRIBUTE INDEX REGISTER - READ/WRITE PORT = 03C0



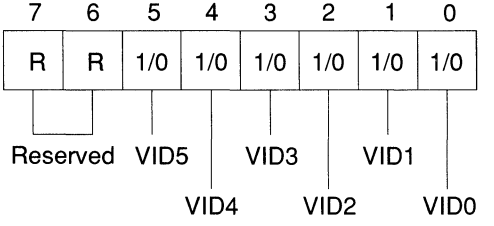
Bit 7 , Bit 6 Reserved.

Bit 5 Palette Address Source.
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 - 0FH).
1 = Enable internal color palette and normal video translation.

Bit 4 - Bit 0 Attribute Controller Index Register Address Bits.

NOTE: The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 03?A) clears the flip-flop and selects the Address Register, which is read thru address 03C1 and written at address 03C0. Once the Address Register has been loaded with an index, the next write operation to 03C0 will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address hex 03C0, but does not toggle for reads to address 03C1.

PALETTE REGISTERS (00-0F Hex) - READ PORT 03C1/WRITE PORT 03C0



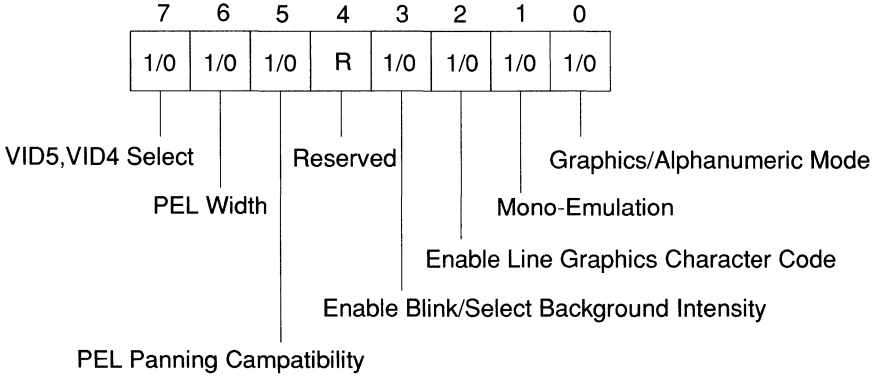
Bit 7, Bit 6 Reserved.

Bit 5 - Bit 0 Palette Pixel Colors.
They are defined as follows:
0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the table below:

Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

ATTRIBUTE MODE CONTROL REGISTER

READ PORT 03C1/WRITE PORT 03C0 AND INDEX REGISTER = 10



Bit 7 VID5, VID4 Select.
0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14H) bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6 Pixel Width.
0 = Disable 256 color mode pulse width.
1 = Enable pulse width for 256 color mode.

19

ATTRIBUTE MODE CONTROL REGISTER (contd)

Bit 5 PEL Panning Compatibility.
Line Compare in the CRT Controller.
0 = A Line compare will have no effect on the PEL Panning Register.

1 = Allows a successful line compare to disable the PEL Panning Register until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4 Reserved.

Bit 3 Back Ground Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

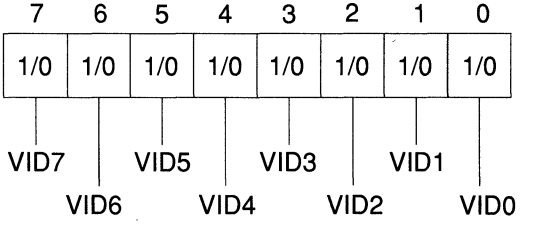
Bit 2 Enable Line Graphics Character Code.
Set this bit to zero for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1 Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes.

Bit 0 Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

OVERSCAN COLOR REGISTER

READ PORT 03C1/WRITE PORT 03C0 AND INDEX REGISTER = 11

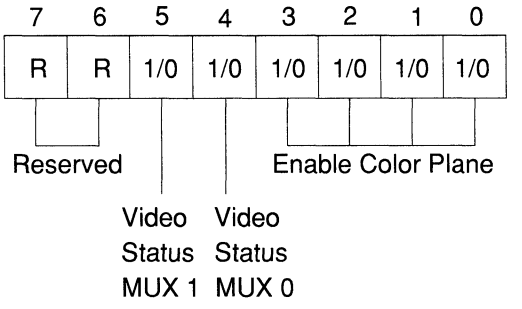


Bit 7 - Bit 0 Overscan/Border Color.
They determine the overscan or border color. For monochrome display, this register is set to 0. Border colors are set as shown below:

Bit 7 VID7
Bit 6 VID6
Bit 5 VID5
Bit 4 VID4
Bit 3 VID3
Bit 2 VID2
Bit 1 VID1
Bit 0 VID0

COLOR PLANE ENABLE REGISTER

READ PORT 03C1/WRITE PORT 03C0 AND INDEX REGISTER = 12



Bit7, Bit 6 Reserved.

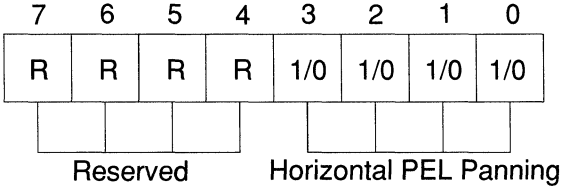
Bit 5, Bit 4 Video Status Control.
These bits select 2 out of 8 color outputs which can be read by the Input Status Register 1 (port = 03?A) bits 4 and 5.

Color Plane		Input Status Register	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3 - Bit 0 Color Plane Enable.
0 = Disables respective color planes.
1 = Enables the respective display memory color plane.

HORIZONTAL PEL PANING REGISTER

READ PORT 03C1/WRITE PORT 03C0 AND INDEX REGISTER = 13



Bit 7 - Bit 4 Reserved.

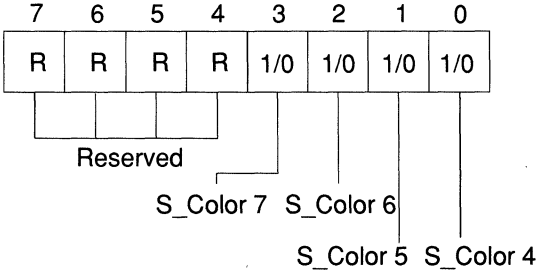
Bit 3 - Bit 0 Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to 3 position pixel shift can occur. The following table defines the shift in different modes:

HORIZONTAL PEL PANNING REGISTER (contd)

Register Value	Left Shift Pixel Value 9 Dots/Character	8 Dots/Character	256 color Mode
0	1	0	0
1	2	1	-
2	3	2	1
3	4	3	-
4	5	4	2
5	6	5	-
6	7	6	3
7	8	7	-
8	0	-	-

COLOR SELECT REGISTER

READ PORT 03C1/WRITE PORT 03C0 AND INDEX REGISTER = 14



Bit 7 - Bit 4 Reserved.

Bit 3, Bit 2 Color Value MSB.
Two most significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 250 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6.

Bit 1, Bit 0 Substituted Color Value Bits.
These bits can be substituted for VID5 and VID4 output by the Attribute Controller palette registers, to create eight bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10H).

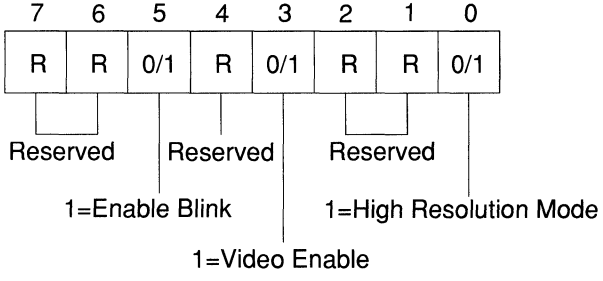
7.6 COMPATIBILITY REGISTERS

Name	Port (Hex)
Mode Control Register	03?8
Color Select Register	03D9
Status Register	03?A
AT&T/M24 Register	03DE
Hercules Register	03BF
Preset Light Pen Latch	03B9 (Mono) & 03DC (CGA)
Clear Light Pen Latch	03?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting Paradise Register PR2(6) = 1.
2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting Paradise Register PR2(7) = 1.
3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
   ? = B in Monochrome Emulation Modes
   ? = D in Color Emulation Modes

MODE CONTROL REGISTER
MONOCHROME (HIGH RESOLUTION) MDA OPERATION - WRITE ONLY PORT = 03B8



Bit 7, Bit 6 Reserved.

Bit 5 Enable Blink.
0 = Disable blink.
1 = Enable blink.

Bit 4 Reserved.

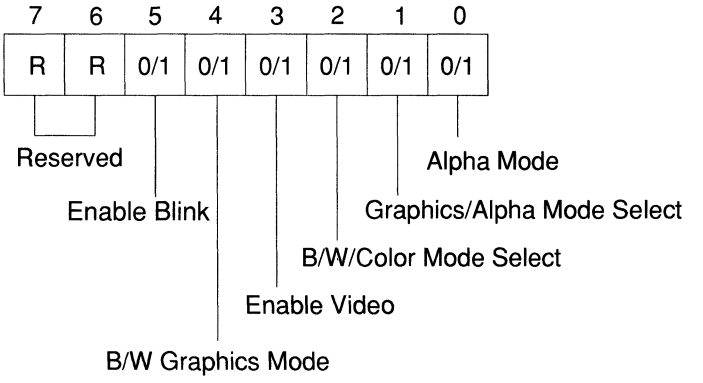
Bit 3 Video Enable.
0 = Video disable.
1= Video activated.

Bit 2, Bit 1 Reserved.

Bit 0 High Resolution Mode.
0 = High resolution disabled. This is not allowed in MDA designs.
1 = High resolution is enabled.

MODE CONTROL REGISTER (contd)

COLOR CGA OPERATION - WRITE ONLY PORT = 03D8



Bit 7, Bit 6 Reserved.

Bit 5 Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4 B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

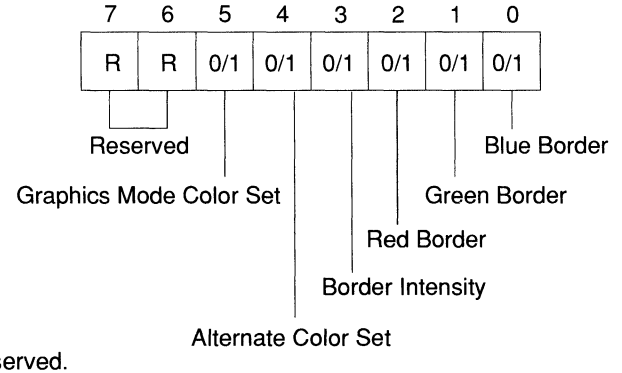
Bit 3 Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = Enable video signal.

Bit 2 B/W or Color Display Mode.
0 = Color mode selected.
1 = B/W mode enabled.

Bit 1 Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = Graphics mode (320 by 200) activated.

Bit 0 (40 by 25) or (80 by 25) Text Mode Selection.
0 = (40 by 25) alpha mode enabled.
1 = (80 by 25) alpha mode activated.

CGA COLOR SELECT REGISTER - WRITE ONLY PORT = 03D9



Bit 7, Bit 6 Reserved.

Bit 5 320 by 200 Color Set Select.
0 = Disable 320 by 200 color mode.
1 = Color set selection for 320 by 200 color mode.

Bit 4 Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = Enable alternate color set in graphics mode.

Bit 3 Border Intensity.
Border color select in text modes, and screen background color in (320 by 200) and (640 by 400) graphics mode.
Alphanumeric Mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0-C1).
640 by 200 Graphics Mode.
1 = Selects intensified foreground color.

Bit 2 Red Border/Background.
Border color select in text modes, and screen background color in (320 by 200) and (640 by 400) graphics mode.
Alphanumeric Mode.
1 = Selects red border color.
320 by 200 Graphics Mode.
1 = Selects red background and border color (C0-C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

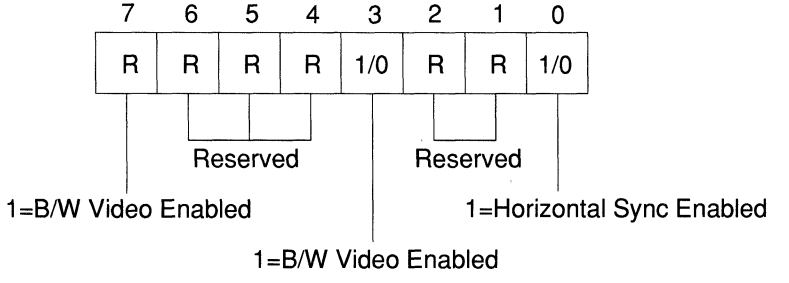
Bit 1 Green Border/Background.
Border color select in text modes, and screen background color in (320 by 200) and (640 by 400) graphics mode.
Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0-C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

CGA COLOR SELECT REGISTER CONTD

Bit 0 Blue Border/Background.
Border color select in text modes, and screen background color in (320 by 200) and (640 by 400) graphics mode.
Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Selects blue background and border color (C0-C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

CRT STATUS REGISTER

MDA OPERATION - READ ONLY PORT = 03BA



Bit 7 B/W Video Status.
0 = B/W Video disabled.
1 = B/W video enabled.

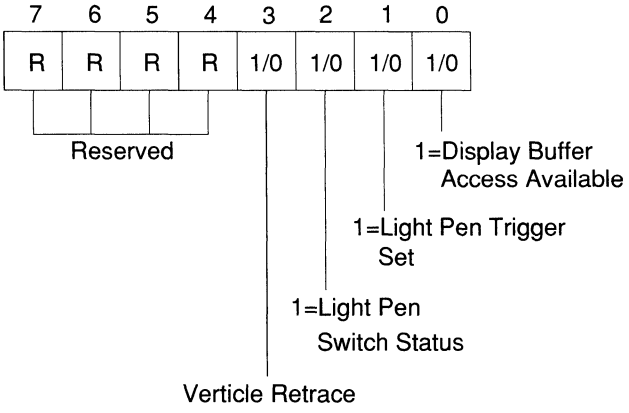
Bit 6 - Bit 4 Reserved.

Bit 3 B/W Video Status.
0 = B/W Video disabled.
1 = B/W video enabled.

Bit 2 - Bit 1 Reserved.

Bit 0 Horizontal Sync Status.
0 = Horizontal sync not active.
1 = Horizontal sync enabled.

CGA OPERATION - READ ONLY PORT = 03DA



Bit 7 - Bit 4 Reserved.

Bit 3 Video Signal Output Status.
0 = Video signal enabled.
1 = Video signal disabled.

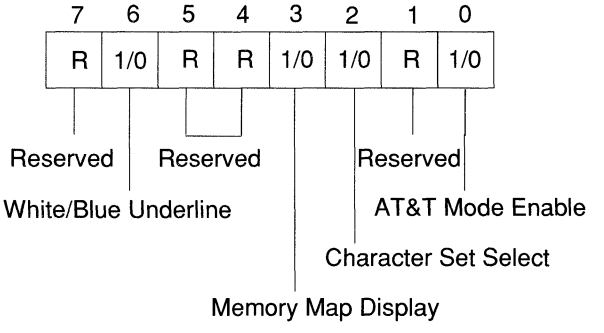
Bit 2 Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open.

Bit 1 Light Pen Trigger Set.
0 = Light pen not triggered.
2 = Positive going edge from the light pen input has triggered its latch.

Bit 0 Display Buffer Access Status.
0 = Display buffer access is not allowed.
1 = Display buffer access is permitted without interfering with the display.

AT&T / M24 REGISTER - WRITE ONLY PORT = 03DE

This is a write only, 8-bit register located at address 03DE. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting bit 7 in Paradise Register 2 (PR2).



Bit 7 Reserved.

Bit 6 White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in color text modes.
1 = Underline attribute selects white underlined foreground.

Bit 5, Bit 4 Reserved.

Bit 3 Page Select.
Selects between one or two 16KB RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B8000H (16 Kbyte length).
1 = Display memory address starts at BC000H (16 Kbyte length).

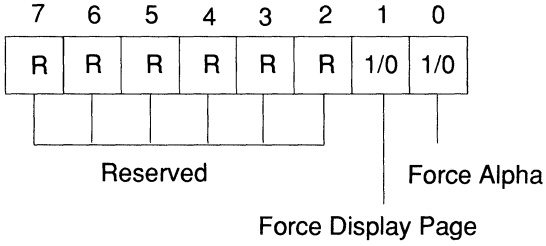
Bit 2 Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1 Reserved.

Bit 0 M24 or Non-IBM Graphics Mode.
A 400 line monitor is required for this mode.
0 = 200 line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400 line graphics.

HERCULES REGISTER - WRITE ONLY PORT = 03BF

The Hercules Mode Register is a 2-bit write only register located at I/O port address 03BF hex. Its bits only effect device operation in 6845 mode. Both of the bits are set to low (0) by reset, or when the device is put into a color mode.



Bit7 - Bit 2 Reserved.

Bit 1 Force Display Page.
Enables Mode Register bit 7 of the Hercules Graphics Card to select displayed memory page in graphics mode. When reset, bit 1 also prevents access of display of second memory page.
0 = Bit 7 of the Mode Register can't be set, and the upper memory page is mapped out.
1 = Bit 7 of the Mode Register can be set, and the upper memory page is accessible.

Bit 0 Force Alpha.
Enables Mode Register Bit 1. This bit forces alpha mode.
0 = Bit 1 of the Mode Register can't be set forcing alpha mode.
1 = Bit 1 of the Mode Register may be changed. Therefore, text or graphics modes may be displayed.

8.0 PVGA1A PARADISE REGISTERS (PR)

The PVGA1A incorporates six additional I/O registers to enhance the functions of the basic VGA. The registers are lock protected and located in the graphics controller I/O section at register locations which have not been used by IBM. All PR registers listed below are read or write able.

NAME	DESIGNATION	I/O LOCATION
Address Offset A	PR0A (6:0)	3CF.09
Address Offset B	PR0B (6:0)	3CF.0A
Memory Size	PR1 (7:0)	3CF.0B
Video Select	PR2 (7:0)	3CF.0C
CRT Control	PR3 (7:0)	3CF.0D
Video Control	PR4 (7:0)	3CF.0E
Lock/Status	PR5 (7:0)	3CF.0F
Configuration	CNF (7:2)	---------

Paradise Register Notation: XXX.YY where XXX is the data port address and YY is the register index e.g. 3CF.0F implies 0F --> 3CE (select index register) followed by (data byte) --> 3CF (data port).

Registers PR0 through PR4 are normally locked after power up. In order to access registers (PR0-PR4), the PR5 register has to be loaded with the value 05H. These registers stay unlocked until the PR5 register is loaded with another value.

All PR registers, except for PR1 (1:0), are set to 0 at power on reset. The PR1 (1:0) bits are latched internally at power on reset from the corresponding video memory data bus pins MD (1:0), connected to the pullup or pulldown external resistors. Pullup resistors on MD(1:0) causes PR(1:0) to be latched low.

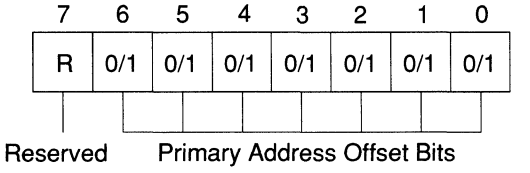
8.1 PR0 A,B Address Offset Registers A & B.

The PVGA1A can control up to one megabyte of video RAM. However, the memory map for IBM PC and compatible product assigns 128 Kbytes of the available 1MB total system space to the video controller. Therefore, the video memory space starts at A0000H and ends at BFFFFH. To allow a second video card to co-exist, this space is furthur limited to a 64 Kbyte video memory partition. Primary offset register (PR0A), is always enabled if PR1 bit3 is 0. PR0A is normally used to control 64KB of the available video address space.

Alternatively, Paradise address offset register (PR0A) and address offset register (PR0B) may be used to access two 32KB video RAM windows. PR0A window is mapped from A8000H-AFFFF while PR0B is mapped from A0000H-7FFFFH if PR1 bit 3 is set to 1 (Alternate address register PR0B is enabled).

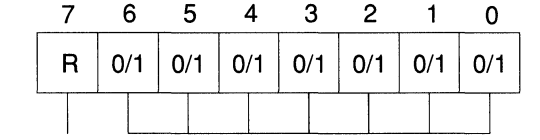
These registers contain an offset which gets added to the system address when accessing 1MB of video memory. Address offset register A is the primary address offset register and is always enabled. On the other hand, alternate address offset register B is enabled only if PR1 bit3 is set to 1. PR0A,B register six bit offset is added to address bits (12:18) of the system address bus SA(0:19) to form a 20-bit address. It can be thought of as being segment registers DS and ES of the 8088 architecture. PR0A,B will have 4KB segments.

PR0 A - ADDRESS OFFSET REGISTER A - READ/WRITE PORT= 3CF & INDEX REGISTER=09



Address Offset Register A
Added to the System Address
Selected When Address Bit A15=1
it is the Default Address
Offset Register

PR0 B - ADDRESS OFFSET REGISTER B - READ/WRITE PORT=3CF & INDEX REGISTER=0A



Address Offset Register B
Selected by System Address
only if PR1(bit 3)=1

8.2 PR1 Memory Size

This register is 8 bits wide. Bits PR1 (1:0) are latched internally at power on reset from the corresponding memory data bus pins MD (1:0), using either pullup or pulldown external resistors. Pullup resistors on MD(1:0) causes PR1(1:0) bits to be latched low. According to the VGA video memory organization, 256 Kbyte of the available memory space is divided into four 64 Kbyte maps (0-3) each defining bit planes (0-3). In mode 13, the four bit planes are chained to form one large bit plane.

The starting address of the 256 Kbyte video memory buffer can be configured to match other video adapters, and, or, application programs. For example, 256 Kbyte video display buffer with 128 Kbyte or 64 Kbyte segments can start at address A0000 (Hex) while 32 Kbyte segments start at address B0000 (Hex) or B8000 (Hex). PVGA1A enhances memory size capability when bits 6 and 7 are programmed to extend video buffer size to 512 Kbyte or 1024 Kbyte. The DRAM organizations supported by the PVGA1A and its associated video space table are shown below:

DRAMS	MA8 Pin	Video Space	Memory Planes
64Kx4	N/U	256KB	4 (64KB per plane)
64Kx4	Bank Select	512KB	4 (128KB per plane)
256Kx4	DRAM Pin A8	1024KB	4 (256KB per plane)

When video memory size is 512 Kbyte, and 64 Kbyte by 4 DRAMS are used, two banks of 64 Kbyte form 128 Kbyte per plane. MA8 provides the bank selection using an external multiplexer to access the appropriate bank in a plane. Four planes form the desired 512 Kbyte video memory space. For 1024 Kbyte video memory size, MA8 is directly connected to the A8 address pin of the 256 Kbyte by 4 DRAMS, and two DRAMS form a 256 Kbyte per plane. Four planes make the desired 1024 Kbyte video memory space. For more details, refer to the programming section listed on the next page:

MEMORY SIZE REGISTER

GRAPHICS MODE RAM ADDRESSING:

PR1(7) **PR1(6)**

0 0 256 K TOTAL; 64K/PLANE; IBM VGA MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
.....	.....	.....	.....	.....	.....	.....
.....	.....	.....	.....	.....	.....	.....
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(0)	A(0)	CA(0)	A(16) or XRN(5)	CA(15) or CA(13)	A(14)	CA(12)

PR1(7) **PR1(6)**

0 1 256K TOTAL; 64K/PLANE; PVGA1A MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12
.....	.....	.....	.....	.....	.....	.....
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

PR1(7) **PR1(6)**
1 0 512 KBYTE TOTAL IN FOUR PLANES ; 128KB / PLANE IN PVGA1A MEMORY ORGANIZATION (EACH PLANE IS 2 BANKS OF 64 KBYTE BY 8)

VIDEO RAM ADDR BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	------	-----	-----	------	-----	-----
MA(16)*	A(16)*	CA(16)*	A(17)*	CA(16)*	A(18)*	CA(16)*
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
.....	.....	.....	.....	.....	.....	.....
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

NOTE: "*" Controls CAS external to PVGA1A

PR1(7) **PR1(6)**
1 1 1024 KBYTE TOTAL IN FOUR PLANES ; 256K/PLANE IN PVGA1A MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)
MA(16)	A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
.....	.....	.....	.....	.....	.....	.....
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)
MA(0)	A(0)	CA(0)	A(18)	CA(17)	A(18)	CA(16)

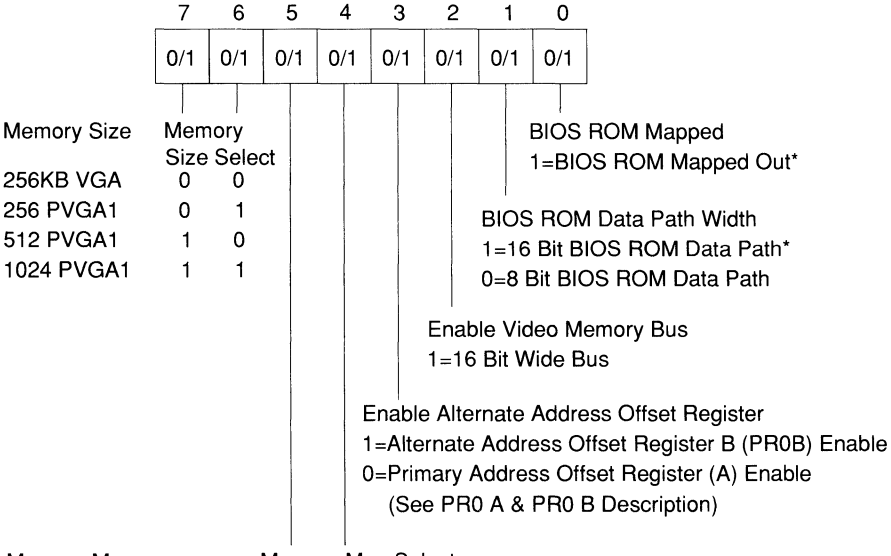
NOTES: 1. A(19)-A(0) are modified System Addresses through PR0A or PR0B.

2. CA(17)-CA(0) are CRT Controller Character Address Counter bits.

3. XRN(5) is Miscellaneous Output Register 3C2, inverted bit 5. This bit selects the displayed page in chained modes. XRN(5)is selected as MA(0) if GR6(3) OR GR6(2) = 1.

4. CA(13) is selected as MA(0) if CRTC Mode Register R17(5) = 0.

PR1 - MEMORY SIZE REGISTER - READ/WRITE PORT=3CF & INDEX REGISTER=0B



NOTE: * = A Pull Up Resister On MD(0) Or MD(1) Line Sets These Bits To 0 At Power On Reset

Bit7	Bit6	MEMORY SIZE
0	0	256KB VGA
0	1	256KB PVGA
1	0	512KB PVGA
1	1	1024KB PVGA

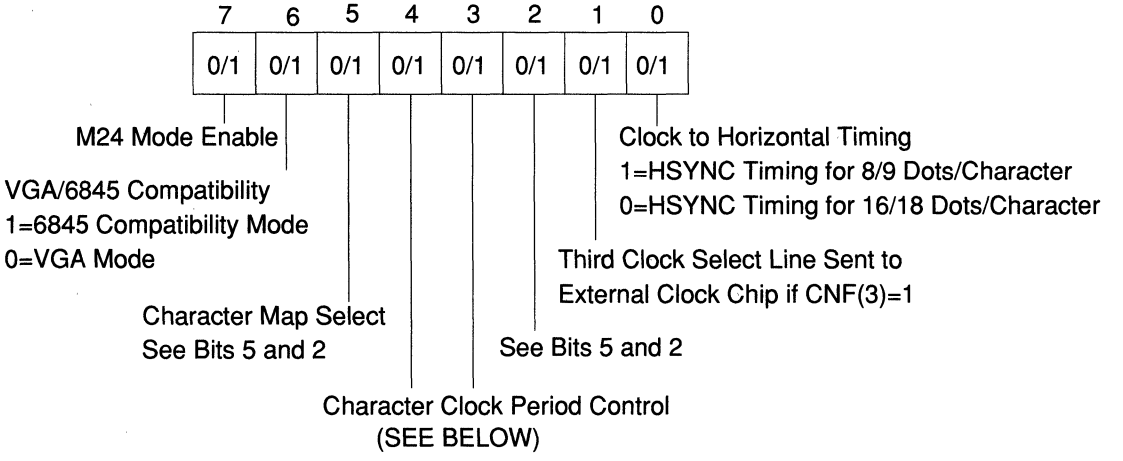
Bit5	Bit4	MEMORY MAP
0	0	VGA Mapping
0	1	1st 256KB in 1MB space
1	0	1st 512KB in 1MB space
1	1	1st 1024KB in larger space

Bit3 Enable Alternate Address Offset Register
(Refer to PR0A and PR0B descriptions)

Bit2
Bit1 Enable 16 bit bus for Video Memory
When set to 1, the BIOS ROM has 16 bits data path.
If set to 0, the BIOS ROM data path is 8 bits wide.
A pullup on MD (1) sets this bit to 0 at power on reset.

19

8.3 PR2 - VIDEO SELECT REGISTER - READ/WRITE PORT=3CF & INDEX REGISTER=0C



Bit 7 It enables M24 mode.

Bit 6 0 = VGA mode.
1 = 6845 Compatibility Mode

Bit 5 Character Map Select. This bit in conjunction with PR2(2) and bit 4 of the attribute code, enables character maps from planes 2 or 3 to be selected per the table below:

PR2(5)	PR2(2)	ATT(4)	Plane Select
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

Bit4	Bit3	Character Clock Period Control
0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132 character mode)
1	0	9 dots
1	1	10 dots

Bit 2 Enable special color underline using all odd numbered attributes (e.g. Programming 1 gives blue colored underline). In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1 This bit is the third clock select line sent to the external clock chip if CNF (3) is set to 1. If CNF register(Bit3) is set to 0, the internal clock select multiplexor is locked.

Bit 0 1 = Set horizontal sync timing for 8/9 dots/character
0 = Set horizontal sync timing for 16/18 dots/character

8.4 PR3 - CRT CONTROL AND GROUP LOCKING

The CRT control register description and software notation are summarized. For example, 3?5.11(7) refers to bit 7 of the CRTC data register 11 (Hex). To read this bit, first write 11 (Hex) to to 3?4, then read 3?5 and test bit 7's value.

PVGA1A CRT CONTROLLER - REGISTER LOCKING

Register locking is controlled by 4 bits. They are PR3 (5,1,0) and 3?5.11(7) (i.e. IBM Vertical Retrace End Register bit 7 controlled by index register 11). When bit 7 is 1, CRT contoller registers (R0-7) are write protected per VGA definition. For more information on the five groups, and their locking schemes, refer to the section below:

GROUP 0

These registers are locked if PR3(5)=1 OR 3?5.11(7)=1
CRT controller register 00 ------ Horizontal Total characters per scan
CRT controller register 01 ------- Horizontal Display Enable End
CRT controller register 02 ------ Start Horizontal Blanking
CRT controller register 03 ------ End Horizontal Blanking
CRT controller register 04 ------ Start Horizontal Retrace
CRT controller register 05 ------ End Horizontal Retrace

GROUP 1

These registers are locked if PR3(1)=0 AND 3?5.11(7)=1
CRT controller register 07(Bit6) ------ Vertical Display Enable End bit 9
CRT controller register 07(Bit1) ------ Vertical Display Enable End bit 8

GROUP 2

These registers are locked if PR3(0)=1 OR 3?5.11(7)=1
CRT controller register 06 -------- Vertical Total
CRT controller register 07(Bit7) ------ Vertical Retrace Start bit 9
CRT controller register 07(Bit5) ------ Vertical Total bit 9
CRT controller register 07(Bit3) ------ Start Vertical Blank bit 8
CRT controller register 07(Bit2) ------ Vertical Retrace Start bit 8
CRT controller register 07(Bit0) ------ Vertical Total bit 8

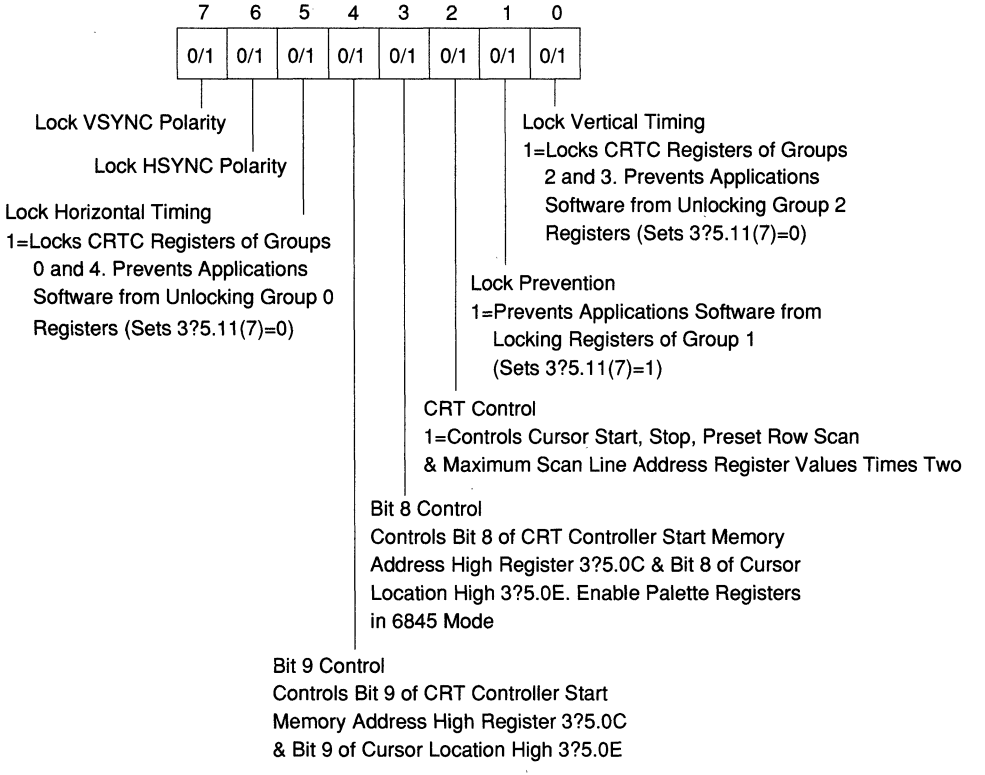
GROUP 3

These registers are locked if PR3(0)=1
CRT controller register 09(Bit5) ------ Start Vertical Blank bit 9
CRT controller register 10 ------ Vertical Retrace Start
CRT controller register 11(Bits 3-0) ------ Vertical Retrace End
CRT controller register 15 ------ Start Vertical Blanking
CRT controller register 16 ------- End Vertical Blanking

GROUP 4

This register is locked if PR3(5)=1
CRTC mode control register 17(Bit2) ----- Selects divide by two vertical timing

PR3 - CRT LOCK CONTROL REGISTER - READ/WRITE PORT=3CF & INDEX REGISTER=0D



Bit0 If set to 1 the BIOS ROM is mapped out. Pullup reisistor latches 0 after power up. A pullup on MD (0) sets this bit to 0 at power on reset.

Bit 7 Lock VSYNC polarity, as programmed in 3C2 bit 7

Bit 6 Lock HSYNC polarity, as programmed in 3C2 bit 6

Bit 5 Lock horizontal timing.
Locks CRTC registers of Groups 0 and 4.
Prevents attempt by applications software to unlock Group 0 registers by setting 3?5.11 bit 7=0.

Bit 4 Bit 9 of CRT Controller Start Memory Address High Register 3?5 .0C, and bit 9 of Cursor Location High 3?5 .0E. This bit corresponds to Character Address CA (17).

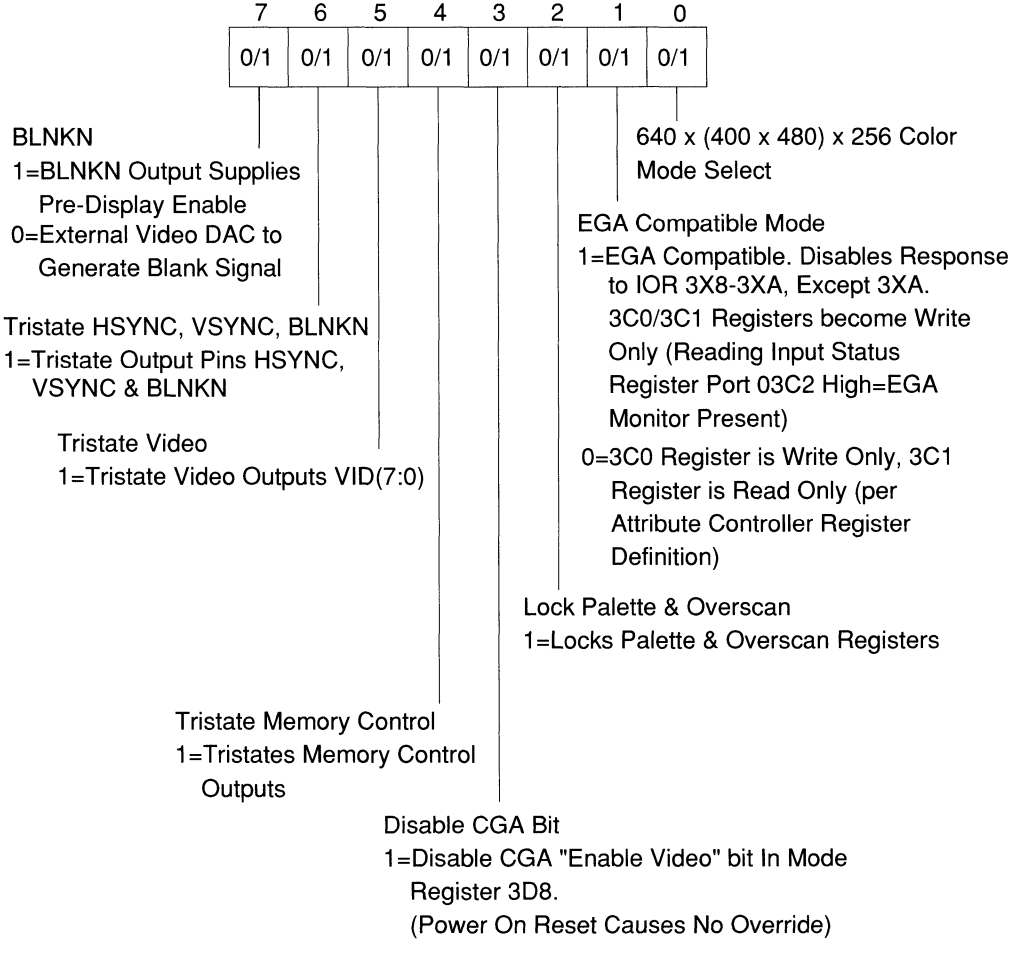
Bit 3 Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (16). This bit is used to enable palette registers in non EGA (6845) mode. In the PVGA1A, the palette will be enabled all of the time.

Bit 2 Cursor start, stop, preset row scan, and maximum scan line address registers values multiplied by two.

Bit 1 1 = Prevents attempt by applications software to lock registers of Group 1 by its setting 3?5 .11 bit 7=1.

8.5 PR4 - VIDEO CONTROL REGISTER - READ/WRITE PORT=3CF & INDEX REGISTER=0E

The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAMDAC, and memory control outputs.



PR4 - VIDEO CONTROL REGISTER (contd)

Bit 7 This bit controls the output signal BLNKN, which normally in the VGA mode, is used by the external video DAC chip to generate blanking.
1 = Display enable.
0 = Blank.

Bit 6 1 = Tristate the output pins HSYNC, VSYNC, and BLNKN.
0 = Normal operation.

Bit 5 1 = Tristate the video outputs VID (7:0).
0 = Normal operation.

Bit 4 1 = Tristates the memory control outputs RAS32N, RAS10N, CAS32N, CAS10N, OE32N, OE10N, WE3N, WE2N, WE1N, WE0N, and MA (0 : 8).
0 = Normal operation.

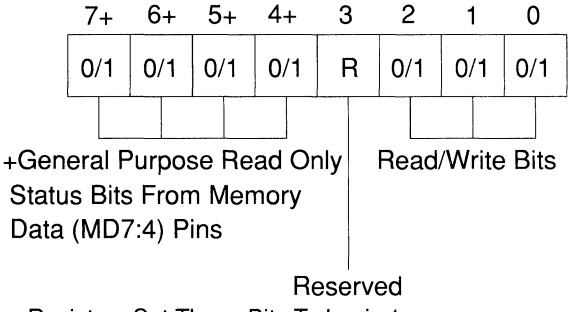
Bit 3 1 = Disables the CGA "enable video" bit in mode register 3D8. Power on reset causes no override.
0 = Normal operation.

Bit 2 1 = Lock palette and overscan registers.
0 = Normal operation.

Bit 1 1 = EGA Compatible Mode. It disables response to IOR 3X8-3XA, to turn off 6845 compatible modes except status register 3XA. Reading Input Status register port 03C2 high implies the presence of EGA monitor in VGA mode.. Also, registers at 3C0/3C1 change to write only mode if EGA compatibility bit is set. In VGA mode (PR(4) bit 1 is zero) 3C0 register is write only, while 3C1 register is read only, per the Attribute Controller registers definition.

Bit 0 Paradise shift register control. It selects 640(400 by 480) by 256 color mode, in addition to the PVGA1A operation by enhancing IBM Mode 13, which has only 320 by 200 dot resolution.

8.6 PR5 - GENERAL PURPOSE STATUS BITS - READ/WRITE PORT=3CF & INDEX REGISTER =0F



NOTE: += Pull Down Resistors Set These Bits To Logic 1

Bit 0 Lock vertical timing. 1 = Locks CRTC registers of Groups 2 and 3. Overrides attempt by applications software to unlock Group 2 registers by its setting 3?5 .11 bit 7=0.

General purpose status bits (7:4) and Paradise register lock/unlock bits (2:0) are stored in the Paradise Register (PR5)

Bits (7:4) These are general purpose status bits. They are latched at power on reset from the corresponding memory data bus pins MD (7:4) connected to the external

INTERNAL I/O PORTS

I / O PORT 46E8H (AT MODE - WRITE ONLY)

IBM has implemented a scheme for mapping the BIOS ROM on the PS/2 VGA display adapter card. This mapping is not done on Micro Channel based VGA implementations. The mapping is controlled through a five bit, write only register located at I/O address 46E8H. The card does not fully decode the address and it also appears at addresses 56E8H, 66E8H and 76E8H. The use of bits within the register are as follows:

D7:D5	Unused
D4	Setup
D3	Enable I/O and memory acceses
D2:D0	BIOS ROM page select (External Implementation)

The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0. The I/O port 46E8H bits (4 : 3) are provided inside the PVGA1A. Bits (2 : 0) are implemented externally. PVGA1A provides EBROMN as the write strobe to external circuitry inplementing BIOS ROM page mapping whenever 46E8H is accessed.

I / O PORT 102H - VIDEO ENABLE (AT AND MICRO CHANNEL MODES)

Power On Self Test (POST) sleep bit 0 is used to awaken the PVGA1A after power on in the MCA mode. Program the I/O port 102H Option Select Byte #1 to enter the set up mode. Port 102H is **internal** to the PVGA1A. If the port 102H bit 0 is set to 1, the PVGA1A is functional. However, if the bit 0 is programmed as 0, the PVGA1A will only respond to setup read and write operations. It will disregard I/O or memory read / write operations and cause no interrupts in the set up mode. To enter the set up mode in AT bus applications, bit 4 of the **partially** decoded **internal** I/O port 46E8H is set to 1 before accessing the I/O port 102H. In MCA mode, when the CDSETUP (EION) signal pin is active low, the PVGA1A is in setup mode and port 102H can be accessed.

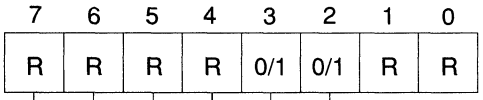
VIDEO RAMDAC PORTS

Video RAMDAC is implemented external to the PVGA1A. However, the WPLTN and RPLTN signals required by the RAMDAC are provided by the PVGA1A. WPLTN and RPLTN signals to the RAMDAC are generated when the following I / O ports are written to or read from :

DAC ADDRESS	DAC OPERATION	DETAILS
3C8H	PEL address port (write)	Read/write port
3C7H	PEL address port (read)	Write only port
* 3C7H	* DAC state (read only)	* If bits 0/1 =1, DAC in read operation When bits 0/1 =0, DAC in write operation. Bits 2-7 are reserved.
3C6H	PEL mask (read/write)	Not to be written by application code or color look up table will be changed.
3C9H	PEL data register (read/write)	Three successive read/write bytes.

*** NOTE : This port is internal to PVGA1A.**

PVGA1A CONFIGURATION BITS CNF (2:3) - NON-READ / NON-WRITE PORT



Read Back As
PR5 Bits (4:7)

Bus Architecture Select
1=IBM PC AT Bus Architecture Signals
0=IBM Microchannel Architecture Signals

Video Clock Source Control
1=Configures PVGA1A Pins VCLK1 & VCLK2 as Outputs
0=Configures PVGA1A Pins VCLK1 & VCLK2 as Inputs

Bits CNF (2:3) are latched internally at power on reset from the corresponding memory data bus pins MD (2:3), connected to the external pullup or pulldown resistors. Pullup resistor sets MD(2:3) to logic 1. Note, that the configuration bits (2:3) are not readable since they are latched after power up. However, the configuration register bits (4:7) are readable after power up as PR5 bits (4:7). They appear as general purpose read only status bits in the PR5 register.

CNF Bit(2) Bus Architecture Select

Pulled low = IBM Microchannel architecture.
Pulled high = IBM PC AT BUS architecture.

CNF Bit(3) Video Clock Source Control.

CNF bit3 configures PVGA1A pins VCLK1 and VCLK2 as inputs or outputs. It is reset to 0 for inputs and set to 1 for outputs.When used as inputs, these pins supply alternate video dot clocks. The selection of dot clocks is done by an internal multiplexer. When used as outputs, VCLK1 becomes an active low load pulse for an external Paradise Clock chip (the PCLK1), active during I/O writes to the port 3C2. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input.
For more details, refer to the PCLK1 data sheet.

9.0 APPLICATION

The PVGA1A applications chapter is divided into various interfaces such as processor (AT or Micro Channel mode), video memory, RAMDAC (INMOS G171), analog monitor, and clock. The description and block diagrams are generic. **No attempt is made to present schematic level details.** Currently available application notes, technical briefs, and referenced literature at the end of the data sheet should supplement the information provided in this chapter. External video subsystem enable I/O port at 3C3H is briefly explained. The Figures 17 through 25 are shown along with their brief description on the subsequent pages.

9.1 I / O PORT 3C3H - VIDEO SUBSYSTEM ENABLE REGISTER

The Paradise PVGA1A does not internally support the 3C3H port in either the AT or Micro Channel mode. In the Micro Channel mode, bit D0 of this port is used to enable the video subsystem per IBM definition. If D0 is 1, the video I / O and memory address decoding is enabled. When D0 is 0, the video I/O and memory address is disabled. This port is set to enable (logic 1) after power on. It is not affected by the VGA sleep bit (I / O port 102H bit 0) of the Programmable Option Select (POS). When, PVGA1A is used in the Micro Channel bus designs, the read or write I/O port at 3C3H is implemented externally

The Figure 17 shows a block diagram of the PVGA1A with 8-bit PC/XT interface using 8-bit BIOS. The system data bus SD(0:7) and address bus SA(0:19) are shown along with associated buffers and BIOS ROM. Auto monitor sense line is also included.

CONVENTION: " * " = Logic **AND** function, " / " = **Inverted** function, and " + " = Logic **OR** function

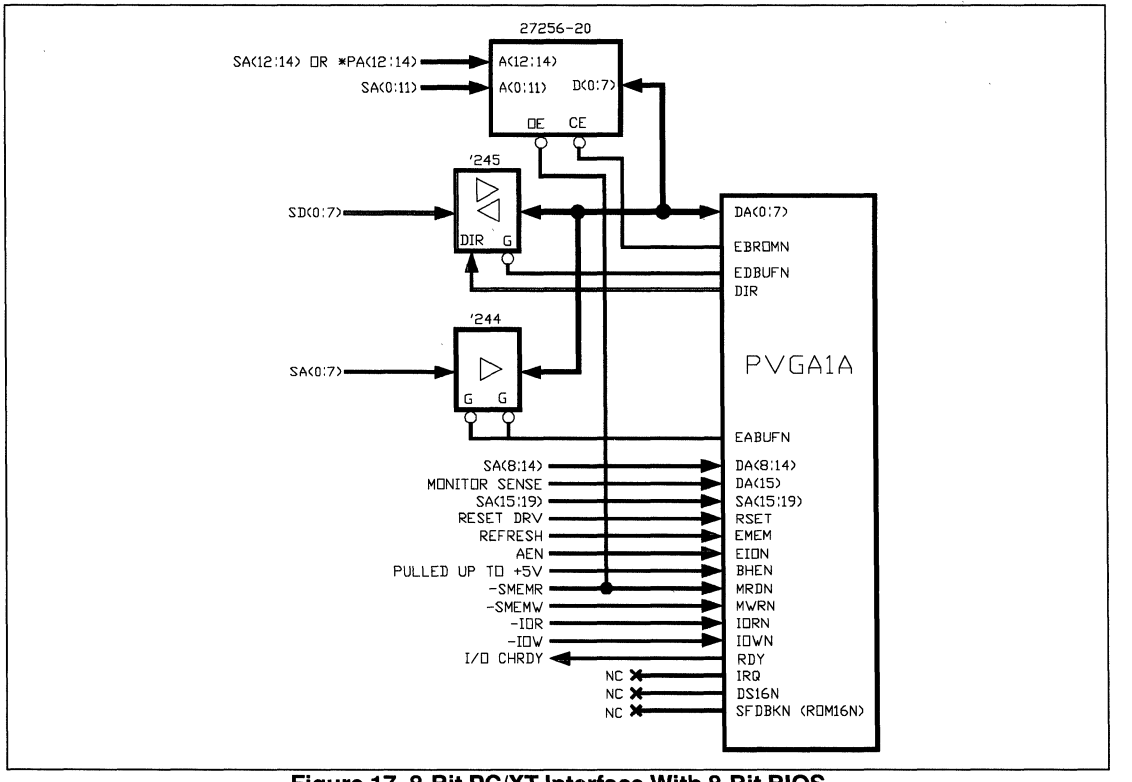


Figure 17. 8-Bit PC/XT Interface With 8-Bit BIOS

Figure 18 illustrates 16-bit PC/AT interface with 8 bit BIOS using PVGA1A. The processor data bus SD(0:15), and the system address bus SA(0:19) are shown. Associated address and data bus buffers, BIOSROM, and auto monitor sense are also shown in it. Note, PA(12:14) to BIOS ROM can be derived from the BIOS page mapping logic if implemented. Logic equations for upper data bus buffer gate EDBF1.

/EDBF1 = /EDBUFN * EBROMN * /SMEMW * /SBHE * /DS16N
+ /EDBUFN * EBROMN * /SMEMR * /SBHE * /DS16N

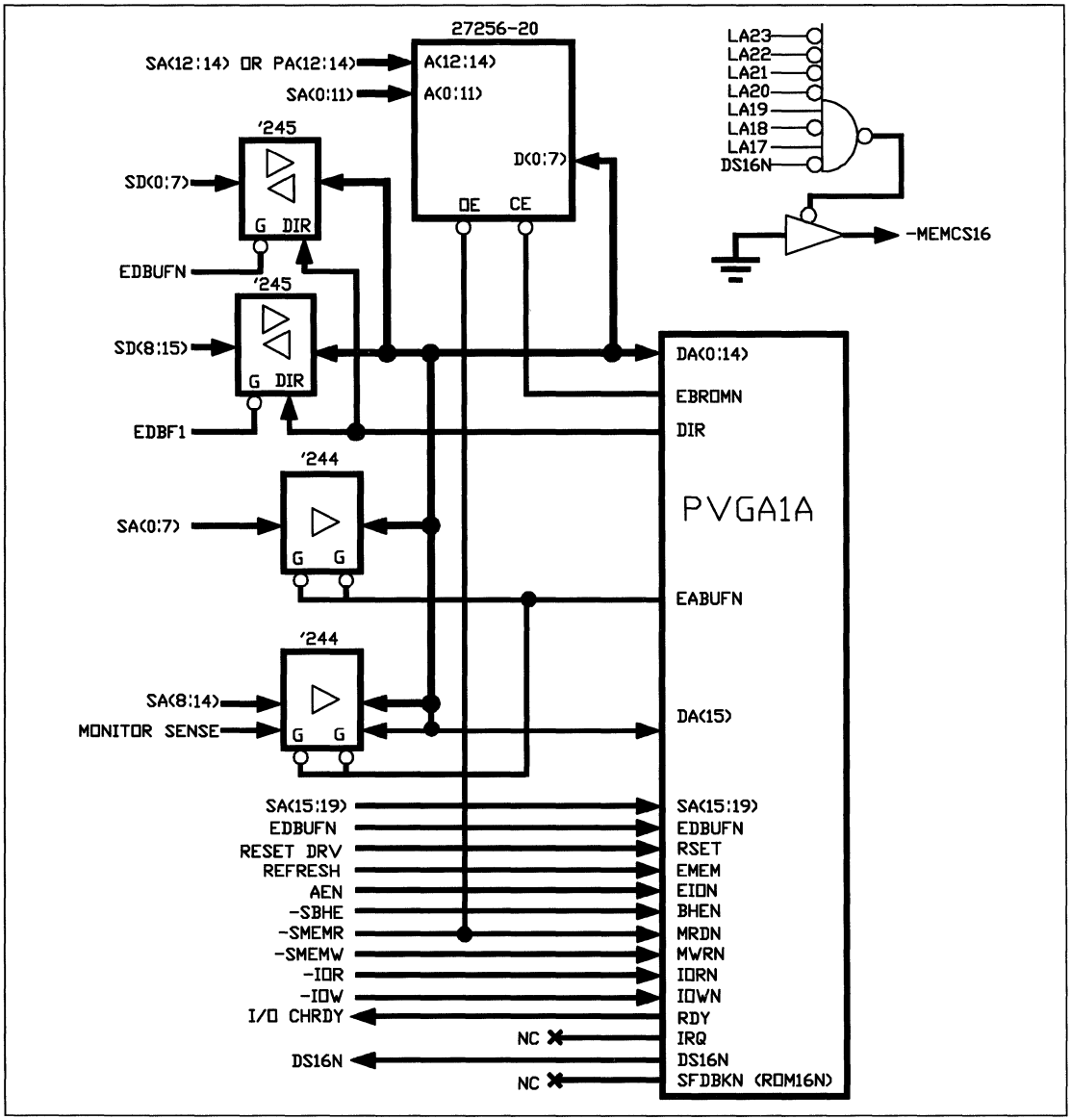


Figure 18. 16-Bit PC/AT Interface With 8-Bit BIOS

Figure 19 describes 16-bit PC/AT interface with 16-bit BIOS ROM implementation using PVGA1A. The system data bus SD(0:15), address bus SA(0:19), address and data bus buffers, and auto monitor sense input is presented. The (16KX8) upper and lower byte EPROMS, output enable lines (EROM0 / EROM1), and EPROM buffer (Gated by EDBFX) are shown. Note that PA(12:14) to BIOS ROM can be derived from the BIOS page mapping logic if it is implemented. Also, -MEMCS16 implementation limits addition of 8 bit cards with memory addresses at the locations of segment C000H for 128 Kbyte memory space. Boolean equations for some of the important signals are listed:

/EROM0 = /EBROMN * /SMEMR * /SA0

/EROM1 = /EBROMN * /SBHE * /SMEMR * /ROM16N + /EBROMN * SA0 * /SMEMR * ROM16N

/EDBFX = /EBROMN * SA0 * /SMEMR * ROM16N

/EDBUF1 = /EDBUFN * /SMEMW * /SBHE * /DS16N + /EBROMN * /SMEMR * /SBHE * /ROM16N
+ /EDBUFN * /SMEMR * /SBHE * /DS16N * EBROMN

Figure 19 is illustrated on the subsequent page.

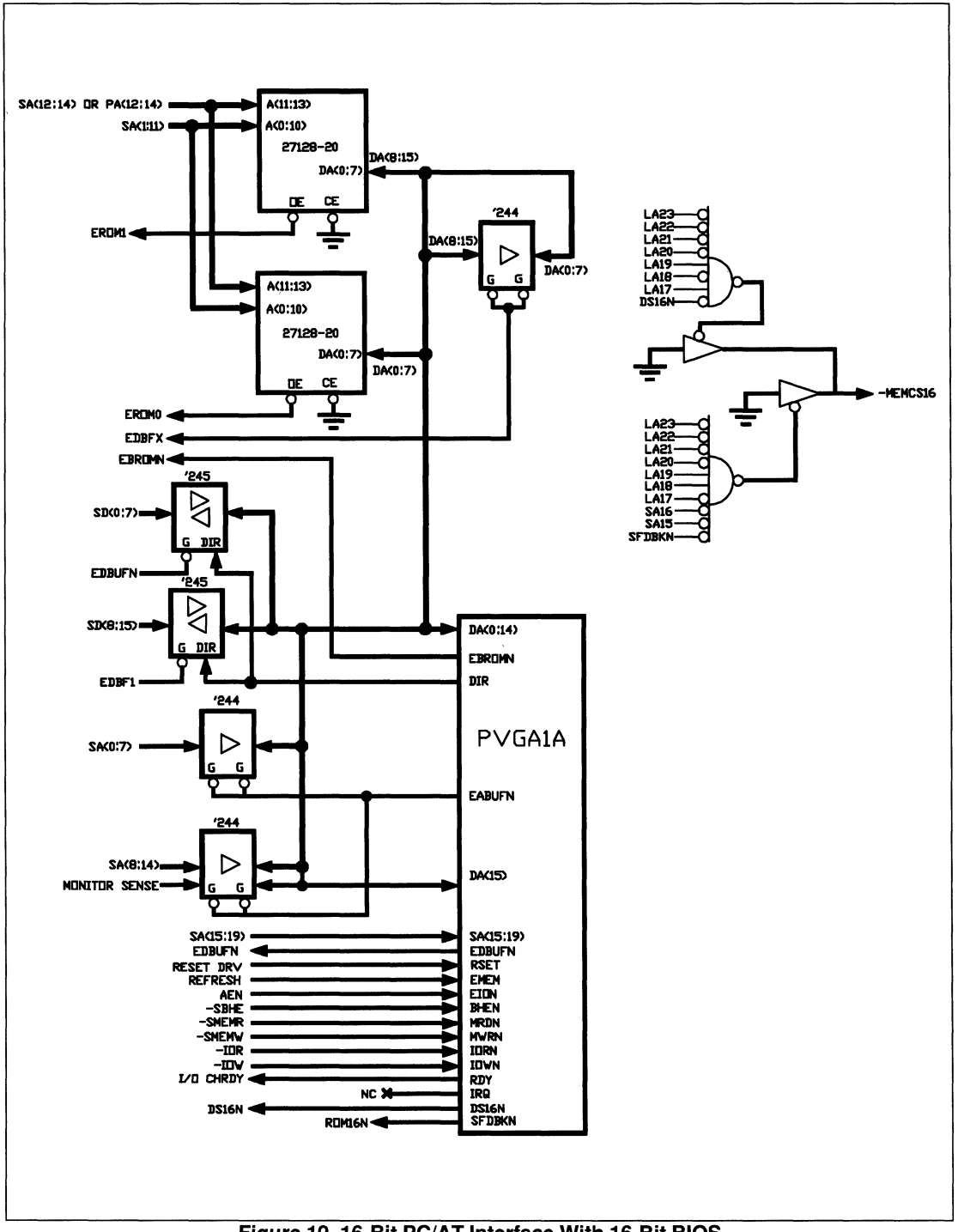


Figure 19. 16-Bit PC/AT Interface With 16-Bit BIOS

Figure 20 indicates PVGA1A and 16-bit Micro Channel interface. The system data bus upper byte bits D(8:14) and lower data bus byte D(0:7) are sampled and buffered for the PVGA1A input pins DA(0:14). Likewise, system address byte upper bits A(8:14) and lower address byte A(0:7) are buffered and gated to the PVGA1A input pins DA(0:14). The most significant system address bits A(15:19) are latched and sent to the PVGA1A. The monitor sense input buffer and D15 are gated into the DA15 input of the PVGA1A. The Micro Channel bus control signals provide the timing and are gated by the appropriate logic blocks to the PVGA1A.

Associated Boolean equations are shown below:

EMEM = (-CMD) * 3C3.D0 * /A23 * /A22 * /A21 * /A20 * (M/-IO) * (MADE24) +
(-CMD) * 3C3.D0 * /(M/-IO) + /(-CMD) * EMEM

NOTE:

1.0 ASYNCHRONOUS EXTENDED CYCLE (300NS) IS REQUIRED IN THIS CONFIGURATION. SIGNAL (-CD SFDBK) MAY NEED TO BE TRANSPARENTLY LATCHED WITH (-CMD). 3C3 IS AN EXTERNAL I/O PORT.

2.0 RPLTN AND WPLTN GO TO THE RAMDAC.

3.0 WPLTN AND RPLTN TO RAMDAC PORTS 3C6H-3C9H WILL NEED ADDITION OF TWO EXTERNAL WAIT STATES OR EXTERNAL SIGNAL GENERATION AS SHOWN BELOW.

/WPLTN = /(M/-IO) * /(-S0) * (-S1) * /A4 * /A3 * A2 * A1 * (-CMD) * /(-CDSFDBK)
+ /(M/-IO) * /(-S0) *(-S1) * /A4 * A3 * /A2 * /A1 * (-CMD) * /(-CDSFDBK)
+ /(-CMD) * /WPLTN

/RPLTN = /(M/-IO) * (-S0) * /(-S1) * /A4 * A3 * /A2 * /A1 * (-CMD) * /(-CDSFDBK)
+ /(M/-IO) * (-S0) * /(-S1) * /A4 * /A3 * A2 * A1 * /A0 * (-CMD) * /(-CDSFDBK)
+ /(-CMD) * /RPLTN

Figure 20 is drawn on the following page.

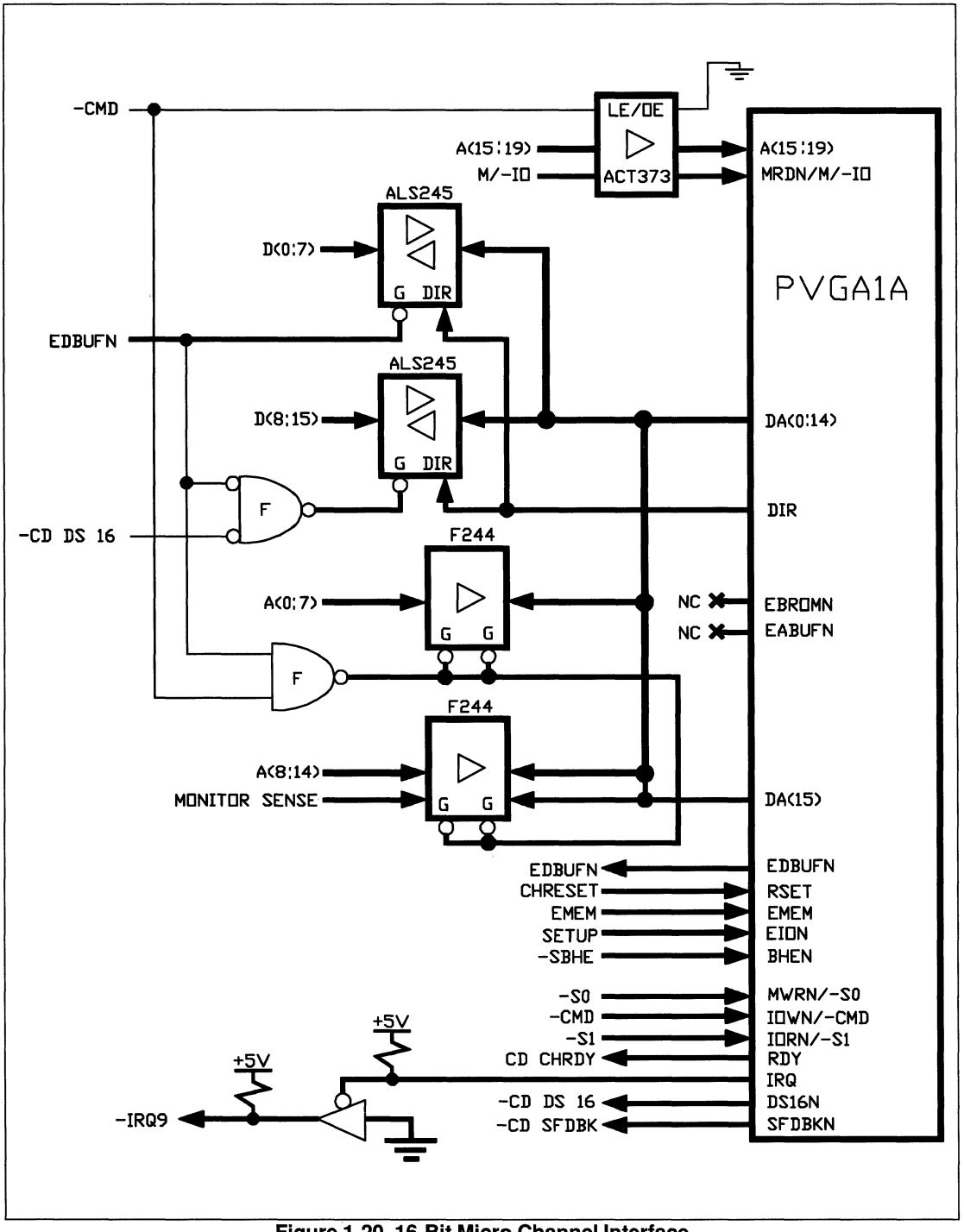


Figure 1-20. 16-Bit Micro Channel Interface

Figure 21 presents PVGA1A with 256 Kbyte video memory organization using four 64 Kbyte maps. Each 64 Kbyte map is made from two (64KX4) DRAMs. The built in DRAM controller provides all the memory control signals and refresh cycles.

The PVGA1A also supports 512 Kbyte, or 1024 Kbyte video memory organization using (64KX4) DRAM modules.

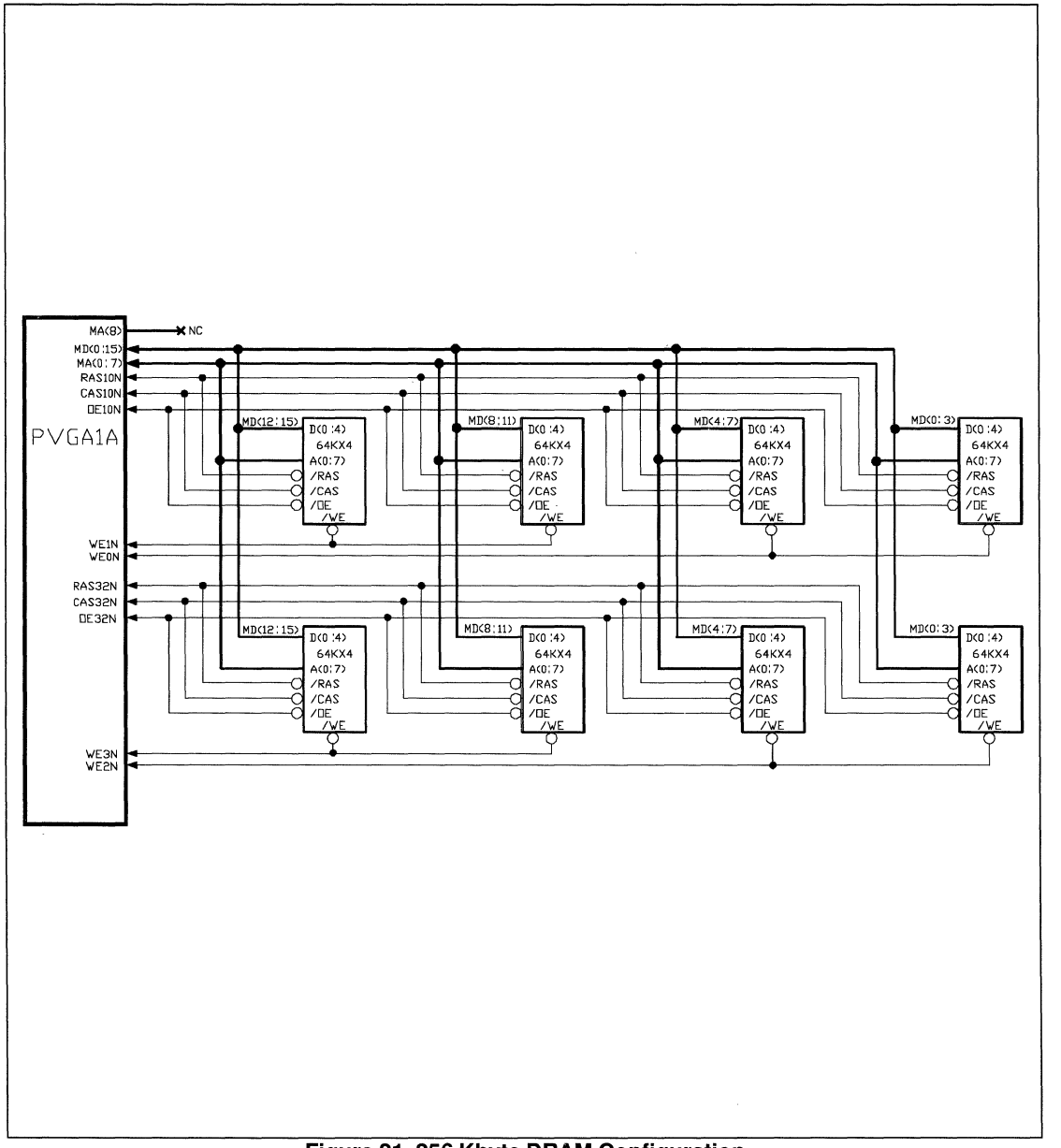


Figure 21. 256 Kbyte DRAM Configuration

Figure 22 illustrates the PVGA1A and RAMDAC (INMOS G171) interface block diagram for analog monitors.

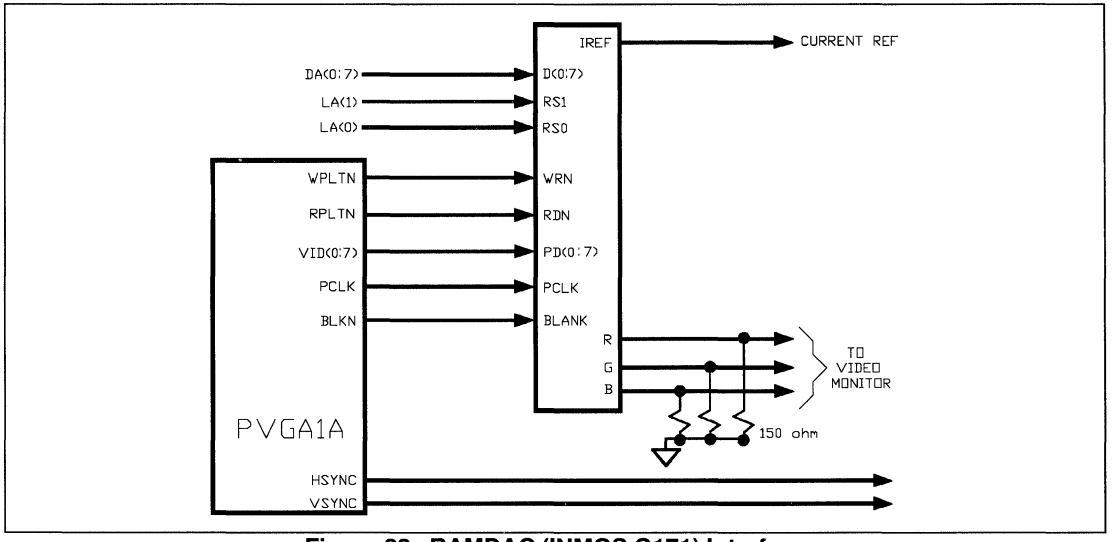


Figure 22. RAMDAC (INMOS G171) Interface

NOTE: LA (1), LA(0) are latched addresses.

Figure 23 shows the PVGA1A and digital monitor connections.

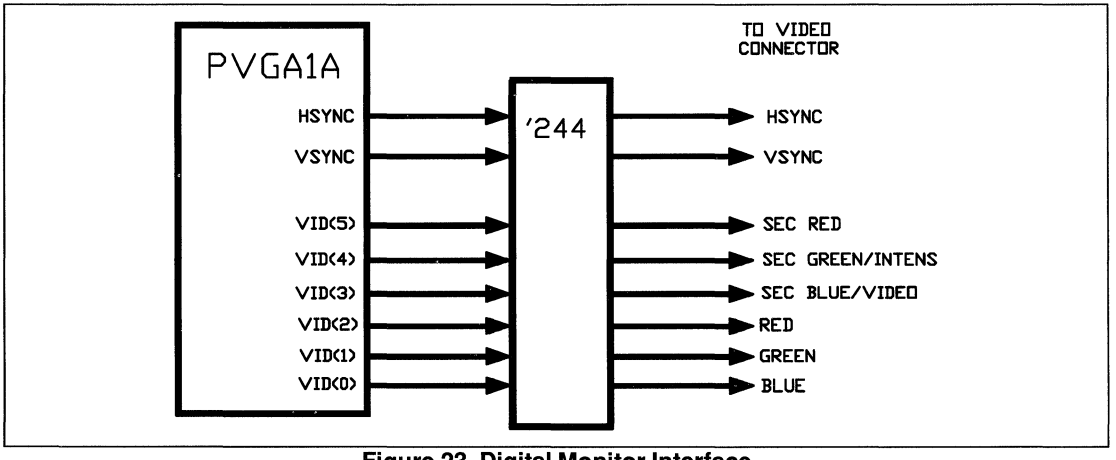


Figure 23. Digital Monitor Interface

Figure 24 presents PVGA1A with external oscillators at the clock pins configured as inputs.. The clock selection is determined by register 3C2H bit 3 and bit 2. It is described by the table below:

3C2H Bit 3	3C2H Bit 2	CLOCK SELECTION
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

The Configuration register Bit 3 (MD3) should be tied low to make the PVGA1A signal pins (VCLK1, VCLK2) inputs.

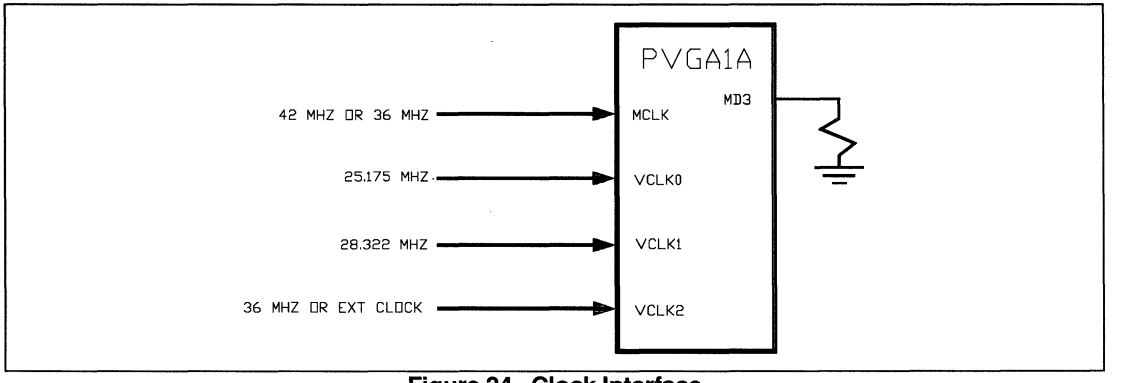


Figure 24. Clock Interface

Figure 25 illustrates PVGA1A pins VCLK1 and VCLK2 configured as outputs. This is done when the Configuration register Bit 3 (MD3) is tied high. The figure also shows how the VCLK1 and VCLK2 signals can be used to control external input clock multiplexor to select 1 of 8 possible clock frequencies.

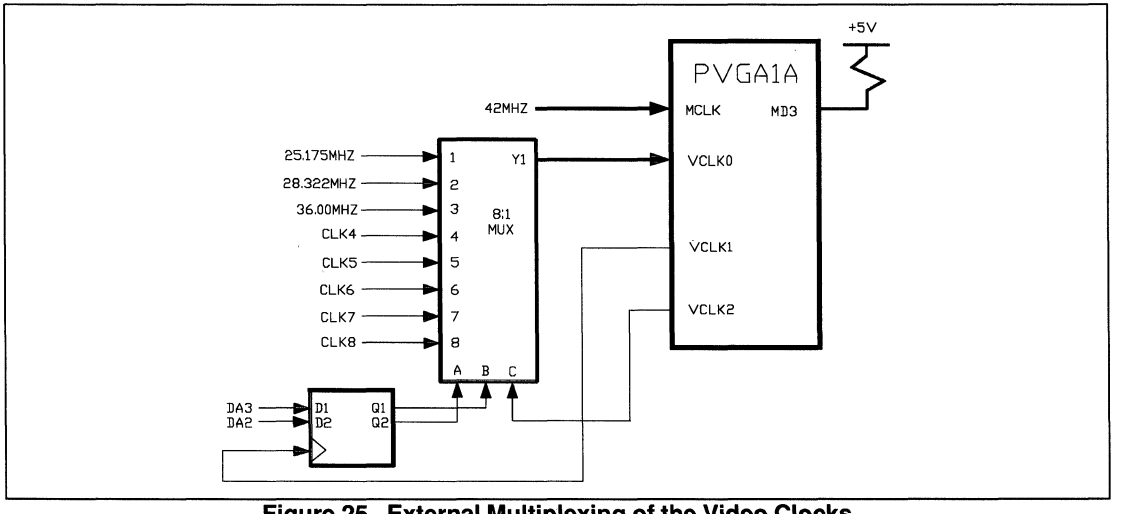


Figure 25. External Multiplexing of the Video Clocks

PVGA1A POWER UP CONFIGURATION

The PVGA1A uses the MD(0:7) input pin to configure itself at power up/reset. These lines will, upon power up/reset, latch logic values depending on whether there is a pull up or a pull down resister on them. PR1(1:0) and CNF(7:2) are the internal registers that are configured on power up. CNF(3:2) will latch a noninverted value (pull up resister = 1) into it and the others will latch an inverted value.

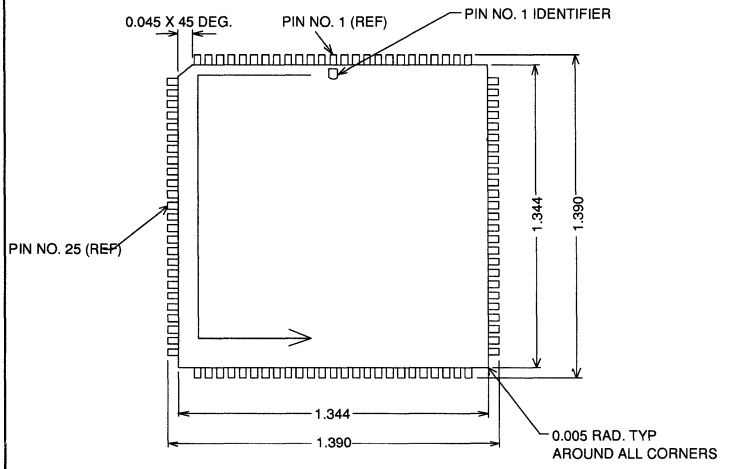
PR1 bit 0 will latch the inverted value of MD(0). A value of 1 (pulled down) will map out the decoding of the BIOS ROM by the PVGA1A. A value of 0 will map it in.

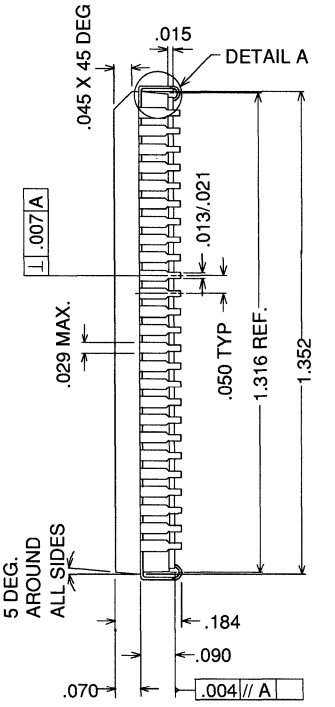
PR1 bit 1 will latch the inverted value of MD(1). A value of 1 (pulled down) will signify to the PVGA1A that the ROM BIOS data path is 16 bits. The PVGA1A will bring SFDBKN active low in AT mode (static signal) and SFDBKN can be used to externally generate -MEMCS16 (off the AT Bus) for 16-bit ROM accesses. In Micro Channel Mode, SFDBKN changes function to be the -CD SFDBK signal output and DS16N is driven active when PR1(1) is set and a valid ROM BIOS address is decoded.

CNF(2) will latch the noninverted value of MD(2). A value of 1 (pulled up) will configure the PVGA1A for IBM PC/XT/AT architecture. A value of 0 will configure the PVGA1A for IBM PS/2 Micro Channel Architecture. VGA1A Signal Pins and the interface will change functions depending on this value.

CNF(3) will latch the noninverted value of MD(3). This bit configures the PVGA1A pins VCLK1 and VCLK2 as inputs or as outputs. A value of 0 (pulled down) will configure these pins as inputs and a value of 1 sets them as outputs. When used as inputs, these pins when connected to clock crystals supply the video dot clock. The selection of these clocks, through an internal multiplexer and along with VCLK0, depends on the value of 3C2H bits 2 and 3. When used as outputs, VCLK1 becomes an active low load pulse when 3C2H is written to with data. VCLK2 becomes the static value determined by the state of PR2 bit 1. When these signal pins are selected as outputs, the internal multiplexer is locked to select the VCLK0 input pin as the video dot clock.

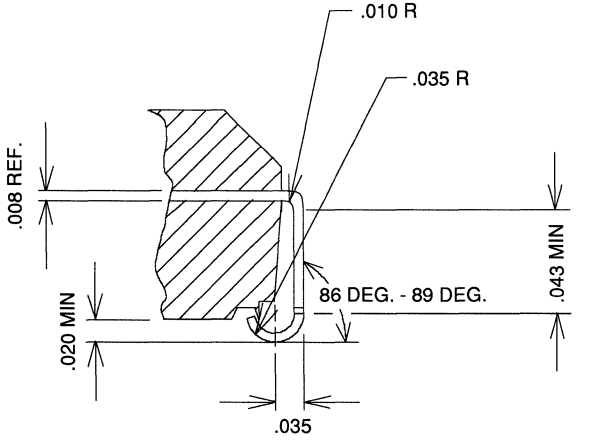
CNF(7:4) will latch the inverted value of MD(7:4). These bits can be read through Paradise Register PR5 bits 7 to 4. These are general purpose bits that may be used by the video BIOS. If reserved or unused by the BIOS, they are available to the application software.





(TOP VIEW)

DETAIL A



NOTE: All dimensions are in millimeters

Figure 26. 100 Pin PLCC Package

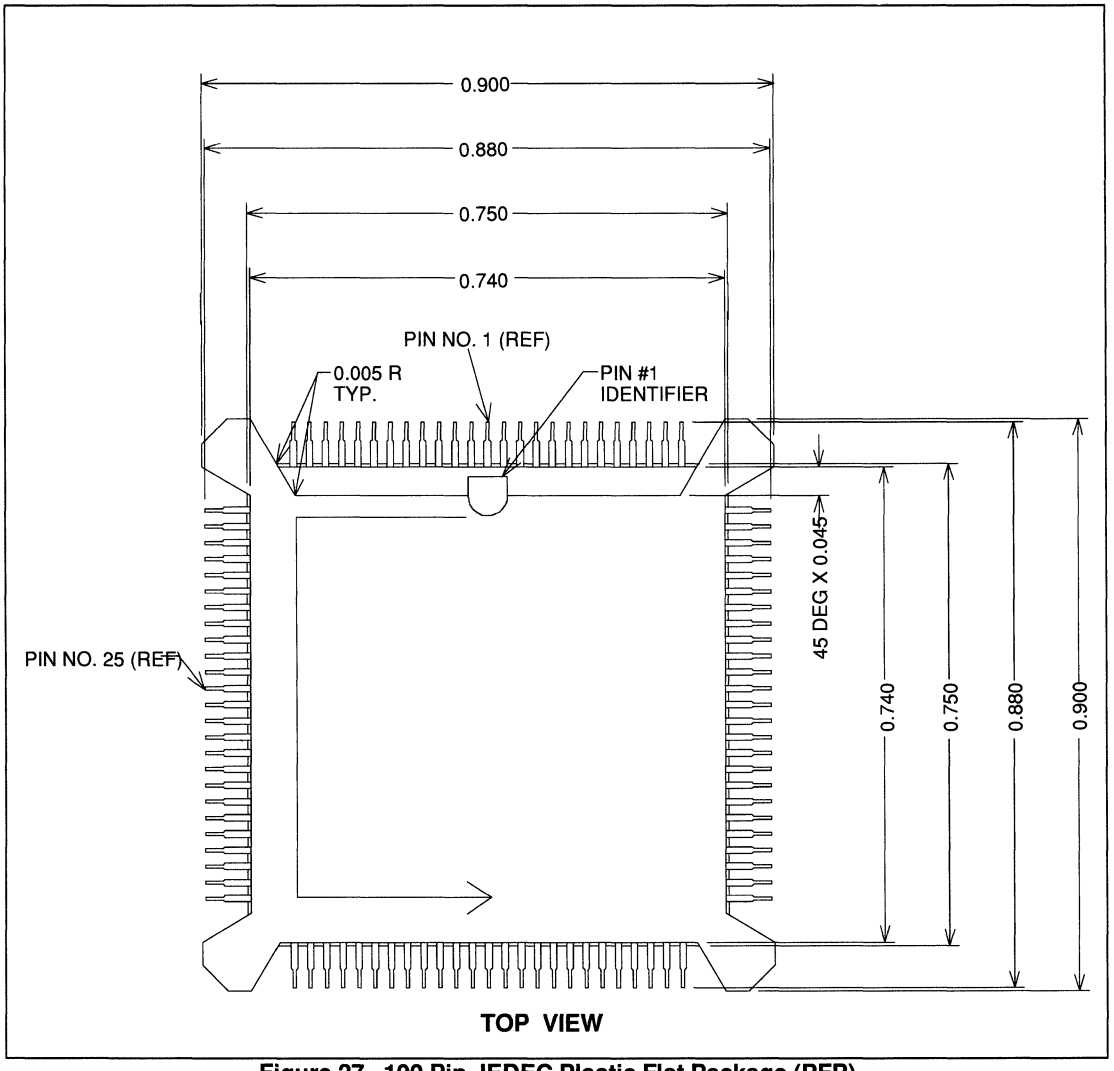


Figure 27. 100 Pin JEDEC Plastic Flat Package (PFP)

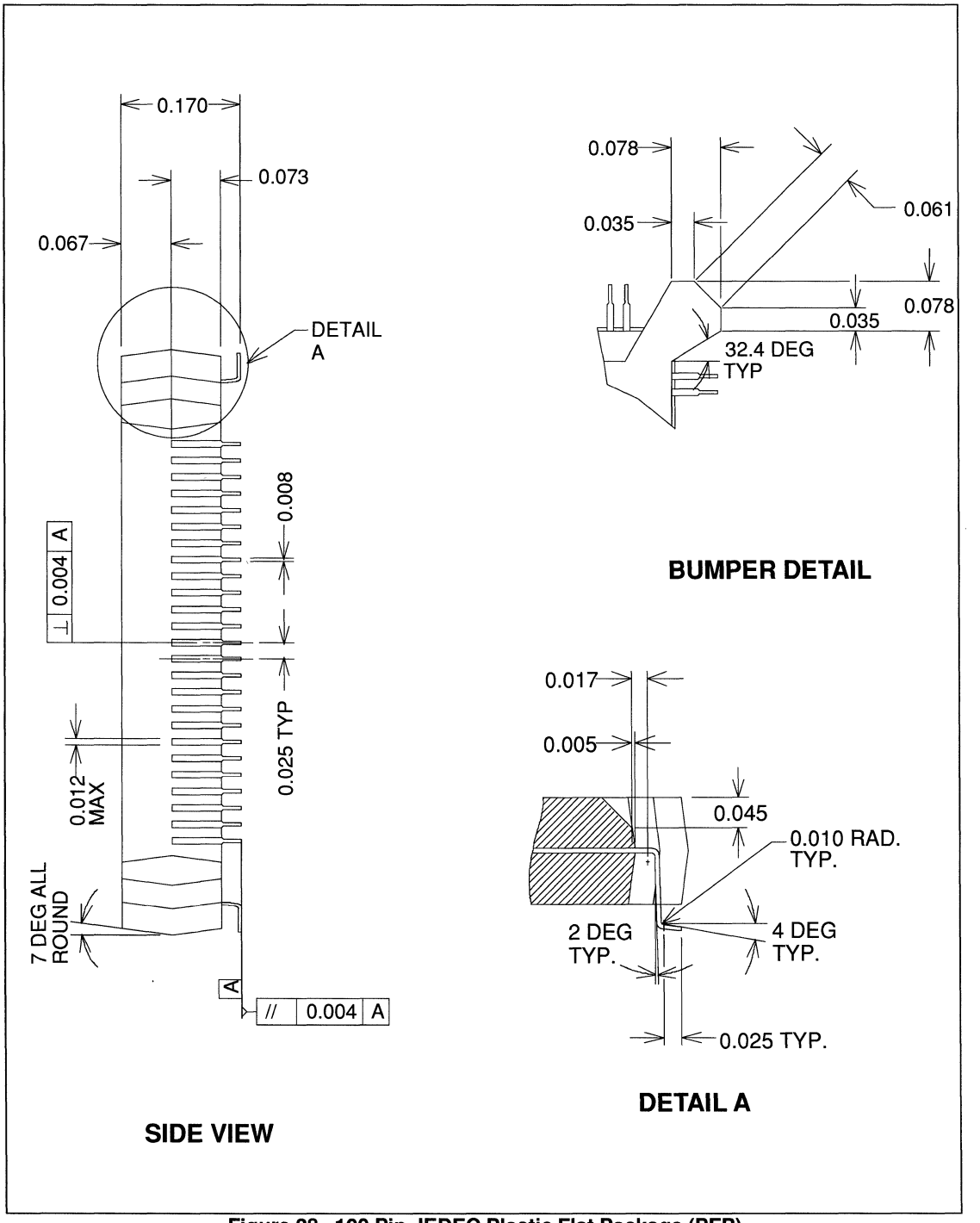


Figure 28. 100 Pin JEDEC Plastic Flat Package (PFP)

REFERENCES

A list of references for generating the PVGA1A data sheet information is shown below:

IBM Personal Computer Hardware User Guide (IBM # 6322510)

IBM Personal Computer XT Hardware User Guide (IBM # 6322511)

IBM Personal Computer AT Hardware User Guide (IBM # 6280066)

IBM Personal System 2 Model 30 Hardware User Guide (IBM # 68x2230)

IBM Personal Computer AT Technical Reference Manual (IBM # 6280070)

IBM Personal System 2 Model 30 Technical Reference Manual (IBM # 68x2201)

IBM PC Options & Adapters Technical Reference Manual (IBM # 6322509)

IBM Personal System 2 BIOS Reference Manual (IBM # 68x2260)

Personal Computer Reference Manual (IBM # 6025005)

AT &T Video Display Controller VDC 750 / VDC 600 Installation Guide

Hercules Graphics Card Owner's Manual

Paradise OEM Technical Publication Manual

The customers are urged to refer to the manuals listed above and supplement their knowledge from **other** books and literature available in the market.

WD90C00

(PVGA1B) VGA

Controller

WESTERN DIGITAL

TABLE OF CONTENTS

APPENDICES

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

Many applications require greater graphics capability than is available through the IBM Monochrome Display Adapter (MDA), Color Graphics Adapter (CGA), Enhanced Graphics Adapter (EGA), Multi Color Graphics Array (MCGA), and the Video Graphics Array (VGA). The WDI WD90C00 is a 1.25 micron, 15,000 gate CMOS VLSI device that fulfills this need and allows for the design of very high performance VGA graphics subsystems that are able to interface with the PC/AT Bus, as well as the IBM Micro Channel Bus, while maintaining backwards compatibility with previous video standards.

A major advantage of using the WD90C00 is that designs implementing this graphics controller will be able to run applications requiring MDA, CGA, EGA, Hercules graphics, AT&T (640 by 400 graphics mode), VGA hardware and BIOS level compatibility on analog and TTL monitors. In addition, it includes full support for running extended high resolution 1024 by 768 by 16 colors interlaced graphics mode on 8514 Color Displays. A Noninterlaced 1024 by 768 by 16 colors graphics mode requires external circuitry along with a 56 MHz MCLK and 80 ns DRAMs.

1.1 FEATURES

- Provides single chip Video Graphics Solution for IBM PC/XT/AT and Personal System/2 compatible systems
- 100% hardware compatible with IBM's VGA card in all modes
- 100% EGA, CGA, MDA, Hercules Graphics, AT&T Model 6300 compatible
- Integrated bus interface for PC/XT/AT, and Micro Channel
- 800 by 600 x 16 colors, 640 by 400 x 256 colors
- 640 by 480 x 256 colors (512 Kbytes DRAM)
- 800 by 600 x 256 colors (512 Kbytes DRAM)
- 1024 by 768 x 16 colors interlaced graphics mode support - 8514 monitor compatible
- 1024 by 768 x 16 colors noninterlaced with external logic
- 132 column text modes, with 25, 43, or 50 rows
- Up to four simultaneous displayable fonts
- Special register locking for flat panel applications
- Lockable palette, RAMDAC, and overscan registers
- Display memory offset registers to control 4 Kbyte windows or 64 Kbyte windows
- Provides adapter video BIOS ROM decoding
- True 7, 8, 9, 10, and 16 pixel wide fonts
- Supports up to 1 Mbyte display memory addressing
- Load up to 16 fonts
- Special underlining in color text mode
- Two additional bits for a total of 18 address bits for cursor location and start address
- Special double scanning
- Special display enable or blanking output signal
- Special border disable
- Page mode addressing for CRTC refresh cycles
- High performance FIFO memory architecture
- Includes 8- or 16-bit wide CPU data bus
- Support for external color lookup table (Palette Chip) with 256K available colors
- Pin for pin compatible with the PVGA1A (AT bus mode)
- Enhanced virtual VGA support
- Up to 45 MHz maximum video clock rate
- Up to 56 MHz maximum memory clock rate
- 1.25 micron CMOS VLSI technology
- 100-pin Plastic Leadless Chip Carrier (PLCC) or Plastic Quad Flat Pack (PQFP) JEDEC package
- Minimizes circuit board space requirements and lowers system cost

1.2 DESCRIPTION

The Western Digital Imaging (WDI) WD90C00 is a 1.25 micron, 15,000 gate CMOS VLSI device designed to implement the IBM Personal System/2 Standard video modes along with all of the popular modes used in the IBM PC/AT family. The WD90C00 is designed to offer more improvements for a wider range of applications. These enhancements include additional extended PR registers for EGA register level compatibility for analog and TTL monitors, high resolution interlaced graphics support, improved bus interface design, and an improved memory and video interface for higher performance.

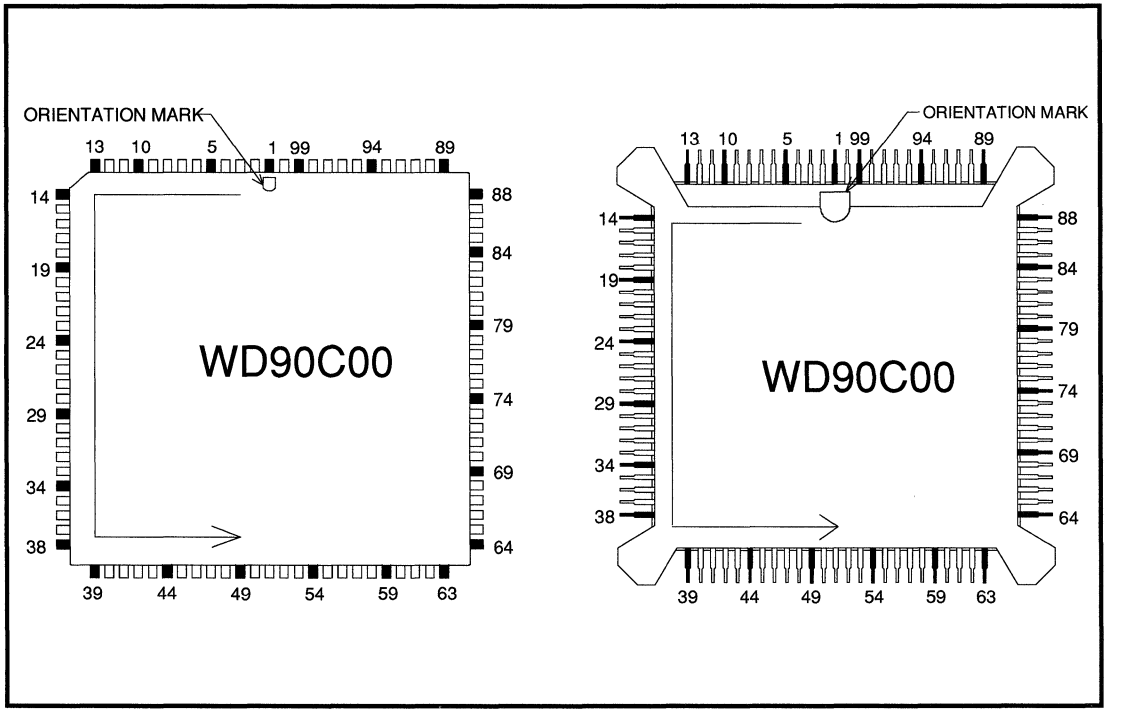


FIGURE 1. PLCC AND PQFP PIN DIAGRAMS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	26	GND	51	GND	76	MCLK
2	MD4	27	A18	52	VCC	77	GND
3	MD3	28	A19	53	VID4	78	VCC
4	MD2	29	$\overline{IOR}$	54	VID3	79	$\overline{RAS10}$
5	MD1	30	$\overline{IOW}$	55	VID2	80	$\overline{CAS10}$
6	MD0	31	$\overline{MRD}$	56	VID1	81	$\overline{OE10}$
7	$\overline{EBROM}$	32	$\overline{MWR}$	57	VID0	82	$\overline{RAS32}$
8	$\overline{DS16}$	33	$\overline{EIO}$	58	$\overline{WPLT}$	83	$\overline{CAS32}$
9	$\overline{BHE}$	34	RDY	59	PCLK	84	$\overline{OE32}$
10	$\overline{SFDBK}$	35	IRQ	60	HSYNC	85	$\overline{WE0}$
11	$\overline{EABUF}$	36	RSET	61	VSYNC	86	$\overline{WE1}$
12	DA8	37	DIR	62	$\overline{BLNK}$	87	$\overline{WE2}$
13	DA9	38	$\overline{EDBUF}$	63	MA8	88	$\overline{WE3}$
14	DA10	39	DA0	64	GND	89	MD15
15	GND	40	DA1	65	MA7	90	MD14
16	DA11	41	DA2	66	MA6	91	MD13
17	DA12	42	DA3	67	MA5	92	MD12
18	DA13	43	DA4	68	MA4	93	MD11
19	DA14	44	DA5	69	MA3	94	MD10
20	DA15	45	DA6	70	MA2	95	MD9
21	EMEM	46	DA7	71	MA1	96	MD8
22	A15	47	$\overline{RPLT}$	72	MA0	97	MD7
23	A16	48	VID7	73	VCLK2	98	MD6
24	A17	49	VID6	74	VCLK1	99	MD5
25	VCC	50	VID5	75	VCLK0	100	VCC

TABLE 1. PIN ASSIGNMENTS

2.0 ARCHITECTURE

The WD90C00 is a highly integrated device that internally contains four major modules. These are the CRT Controller, the Sequencer, the Graphics controller and the Attribute Controller.

- **CRT Controller**

The CRT Controller maintains screen refresh functions for the various display modes defined by the programming of its registers either by the BIOS ROM resident firmware or from the application program. These screen refresh functions include display page control, cursor control, sync generation and resolution.

- **Sequencer**

The Sequencer functions as a timing generator for the AT bus or Micro Channel interface, in I/O or memory cycles. It also provides the character clock and the dot clock for the CRT, Graphics and Attribute controllers.

- **Graphics Controller**

The Graphics Controller manages data flow between video memory and the Attribute Controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the Sequencer.

- **Attribute Controller**

The Attribute Controller modifies the CRT display data stream in graphics and character modes. It controls display attributes such as blinking, underlining, cursor, pixel panning, reverse video, overscan color and background or foreground color.

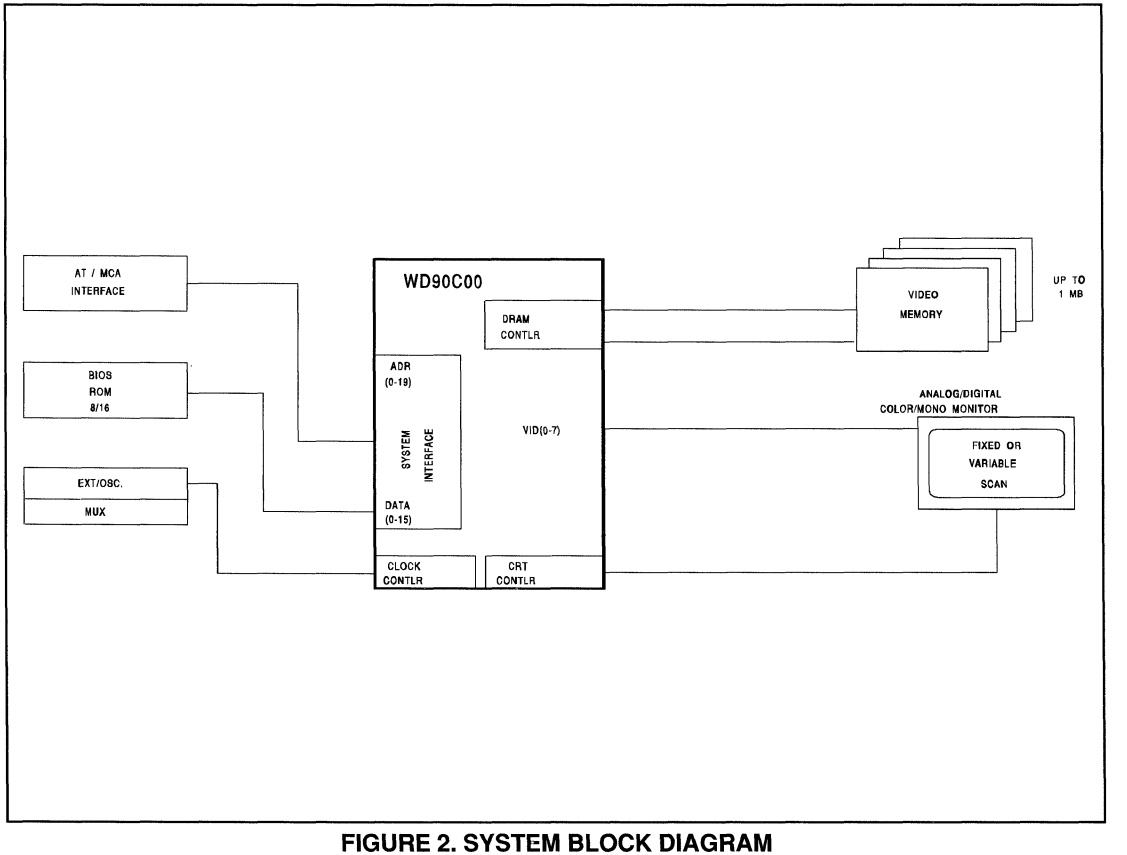


FIGURE 2. SYSTEM BLOCK DIAGRAM

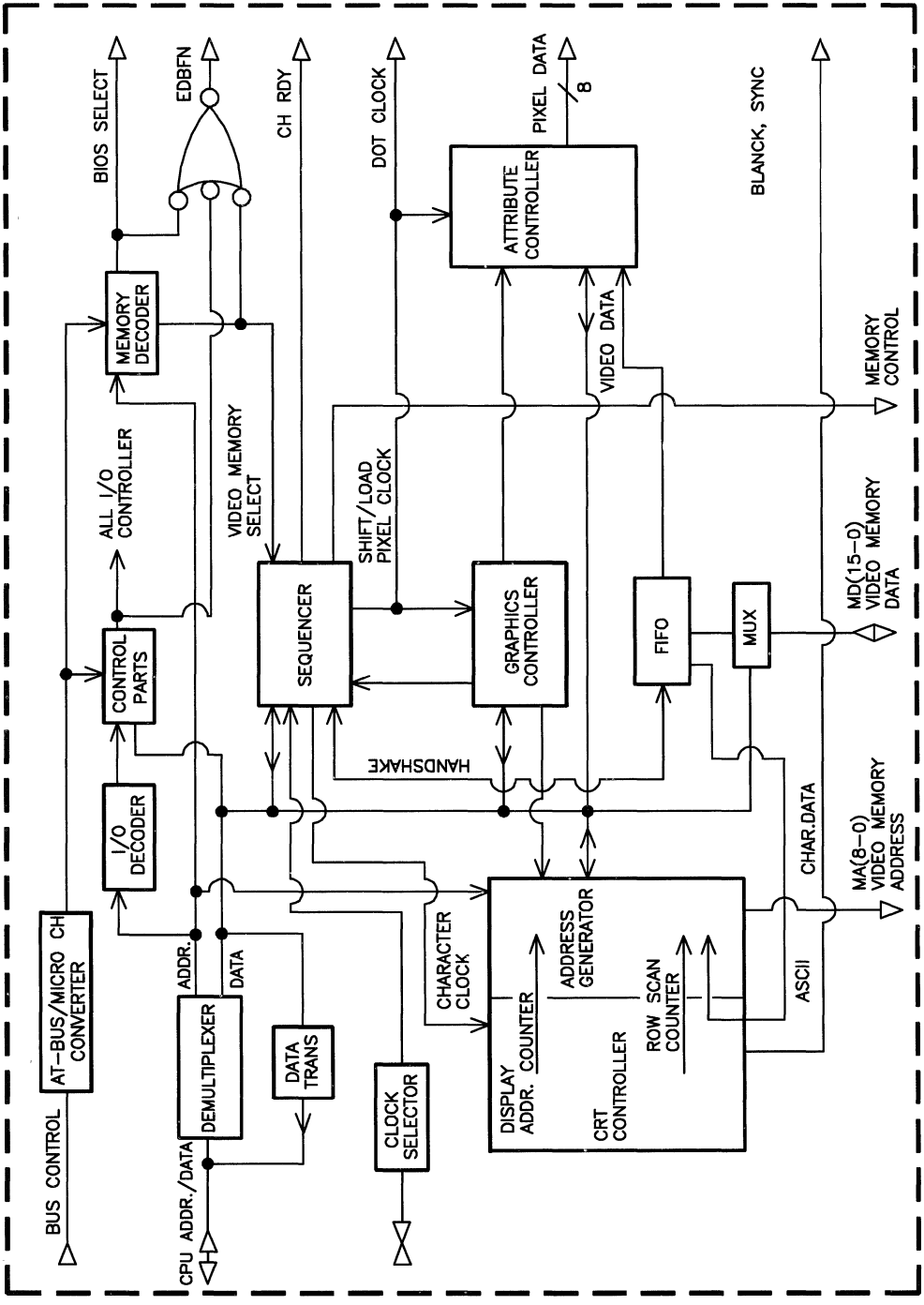


FIGURE 3. WD90C00 BLOCK DIAGRAM

20

3.0 WD90C00 INTERFACES

The WD90C00 has four major interfaces: the CPU and BIOS ROM interface, the DRAM Display Buffer interface, the Video and RAMDAC interface, and the Clock interface.

3.1 CPU AND BIOS ROM INTERFACE

The WD90C00 is designed to operate in two different bus architecture configurations. These are the PC/AT Bus and the PS/2 Micro Channel Bus. The selection of the mode is dependant on the pin strapping upon power up that sets Configuration Register CNF(2).

When configured for AT or Micro Channel operation, the WD90C00 operates functionally in a manner that is conducive to PC/AT or Micro Channel interfacing respectively. The signal pins, memory maps, and I/O ports all operate to optimize this interface with minimal external circuitry.

The WD90C00 provides all the signals and decodes all the necessary memory and I/O addresses for either an 8 or 16 bit data bus. It also provides the necessary decoding of the Adapter Video BIOS ROM and has additional signals and registers to help with BIOS ROM page mapping as done on the IBM PS/2 Display adapter. Using the provided signals, the customer can implement designs which multiplex the address/data signals to the WD90C00 in 8 or 16 bit mode, control an 8 or 16 bit BIOS ROM, and generate the desired control and handshake signals such as -MEMCS16.

The I/O data path is eight bit. The memory display buffer data path can be eight or sixteen bits wide. EGA Planar modes have a mandatory eight bit data path with the CPU. Text modes, odd/even, and 256 color modes can support a sixteen bit data path if the video subsystem supports a 16 bit bus implementation. The WD90C00 will provide the necessary wait states for CPU accesses to the video memory. Wait states for I/O accesses and BIOS ROM accesses are not generated. Special I/O ports such as 46E8H (AT mode) and 102H for VGA Enable have been implemented internally in the WD90C00. VGA Subsystem Enable port 3C3h (MCA mode) needs to be implemented externally.

3.2 DRAM DISPLAY BUFFER INTERFACE

The WD90C00 has an optimized interface to the video memory display buffer. The video memory DRAMS can be considered as being organized as four planes. Three configurations of DRAMs exist for the WD90C00 where each plane can be configured as 64 Kbytes (256 Kbytes total), 128 Kbytes (512 Kbytes total), or 256 Kbytes (1 Mbyte total).

The Video memory address range can be up to 1 Mbyte depending on the configuration. Its range is usually from A000:0H to BFFF:FH. External circuitry can be used to map the video memory in different (up to) 1 Mbyte windows.

Eight 64K by 4 page mode DRAM chips are supported for the default IBM memory size. Sixteen 64K by 4 DRAMs and a multiplexer are needed to have a total of 512 KB DRAM. This configuration is needed to support extended video modes such as 640 by 480 x 256 colors and 1024 by 768 x 16 colors. Eight 256 KB by 4 DRAMs are needed to support 1 Mbyte total memory. The WD90C00 provides the support to access all of the available memory. As the WD90C00 has a separate memory clock, 36 MHz to 40 MHz clocks are needed to drive 120 ns DRAMs. With 100 ns DRAMs, up to a 44.9 MHz clock can be used. The WD90C00 can support up to a 56 MHz MCLK which allows it to support much higher extended resolutions such as an 800 by 600 x 256 color mode.

The combination of video clock and memory clock and DRAM speed will determine the video modes available. Usually, a 44.9 MHz MCLK and 44.9 MHz VCLK will support the 1024 by 768 resolution modes. A 42 MHz MCLK will be needed to support the extended 256 color modes but the 44.9 MHz is recommended. A 36 MHz MCLK and VCLK will support the 800 by 600 x 16 color mode.

3.2.1 DRAM Cycle Types

The WD90C00 will do standard RAS/CAS single cycle accesses to the DRAM during CPU writes and reads in graphics modes and alphanumeric modes. For CRTC display refresh cycles, the WD90C00 will do page mode access reads for all cycles in graphics modes. It will also do page mode reads to the DRAM when selected to do so to increase performance in alphanumeric modes. The default mode of DRAM access in alphanumeric mode is the standard single RAS/CAS cycle. The WD90C00 provides the necessary control signals and address/data lines to access the video memory as two 16 bit data interleaved banks. The WD90C00 will also refresh the DRAMs with 3 or 5 refresh cycles after every horizontal scan line.

3.3 VIDEO AND RAMDAC INTERFACE

3.3.1 RAMDAC

The WD90C00 is designed to connect to an analog CRT monitor through an external RAMDAC, but it may also be used to drive other types of displays such as TTL monitors along with the correct register programming and clocks. All the necessary signals to interface to the video RAMDAC are provided.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and depth (bits/pixels) of the image desired. New monitors, such as multifrequency monitors, are less stringent because of the many sync frequencies available. The WD90C00 can be programmed to directly generate all the CRT signals for up to 8 bits/pixel (256 color). In addition, external hardware can be added to allow higher display resolutions by trading off the number of bits/pixel such as a 1024 by 768 noninterlaced mode.

The Micro Channel Auxiliary Video Connector and the AT Feature Connector can be connected to the WD90C00. The WD90C00 also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

3.4 CLOCK INTERFACE

The WD90C00 has four clock input signal pins. These are: separate memory clock, MCLK, which drives the DRAM timing in graphics and alpha modes; and the three video clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing. WD90C00 also provides the option to externally control a multiplexer that supplies the video clock. The MCLK can also be selected as the video dot clock.

3.5 WD90C00 POWER-UP CONFIGURATION

The WD90C00 uses the memory data pins that are "strapped" to ground or Vcc through resistors to configure an internal configuration register upon powerup/reset. CNF(2) will determine whether the WD90C00 will operate in AT or Micro Channel Architecture (MCA) implementation. Other CNF bits configured by WD90C00 at power-up/reset are used as status bits, or for clock source control. For more information on WD90C00 power-up configuration, refer to the PR Register section of this data sheet.

4.0 PIN DESCRIPTION

The following tables provide WD90C00 pin definitions for the 100-Pin Plastic Leadless Chip Carrier (PLCC) and Plastic Flat Pack (PQFP) package.

The WD90C00 mnemonics are used. For more design details in AT or Micro Channel modes refer to the application notes and reference section of this document.

PIN NO	PIN SYMBOL	TYPE	DESCRIPTION
		POWER ON	
36	RSET	I	RESET: This signal input will reset the WD90C00 in order for the WD90C00 to initialize during Reset. PR registers PR1, PR11, and CNF are initialized at power-up reset based on the logic level on the MD(7:0), MD(15:11) bus as determined by pull-up/pull-down resistors. Outputs $\overline{\text{EABUF}}$ and $\overline{\text{EDBUF}}$ are tri-stated during reset. The active high reset pulse width should be at least ten MCLK clock periods.
		CLOCK SELECTION	
76	MCLK	I	MEMORY CLOCK: This clock signal determines the VGA graphics and alpha mode video DRAM read/write access timing as well as system microprocessor I/O and memory timing. MCLK should be equal to or greater than VCLK. It is 36 to 40 MHz for 120 ns DRAMs, and recommended to be 44.9 MHz for 100 ns DRAMs.
74	VCLK1	I/O	VIDEO CLOCK 1: This pin can be either the second video display clock input or an output selection signal to the external clock selection module. Pin direction is determined on Reset by a pull-up/down register on pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 can be an active low pulse during I/0 writes to port 3C2H or the state of 3C2H bit 2 as per PR15(5). Refer to the Configuration Register description.
73	VCLK2	I/O	VIDEO CLOCK 2: This pin can be a third video display clock input or an output to external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. It acts as either a user defined external clock input, or as an output reflecting the content of bit PR2(1) or the state of 3C2H bit 3 as per PR15(5) if CNF(3) is set to 1 . Refer to the Configuration Register description.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
			CLOCK SELECTION (CONT)
75	VCLK0	I	VIDEO CLOCK 0: This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK0 is 25.175 MHz to display 640 pixels per horizontal display line. The Miscellaneous Output Register (3C2H) bits 3 and 2 when both are set to 0 will select this clock.
			CPU ADDRESS BUS
28 27 24 23 22	A19 A18 A17 A16 A15	I I I I I	ADDRESS ONLY BUS A(19:15): These active high inputs form the high-order five bits of video memory address. These addresses (19:16) are not decoded during I/O accesses in AT or MCA implementation. These inputs are directly connected to the system bus.
			CPU DATA BUS
20 19 18 17 16 14 13 12 46 45 44 43 42 41 40 39	DAI5(*) DA14 DA13 DA12 DA11 DA10 DA9 DA8 DA7 DA6 DA5 DA4 DA3 DA2 DA1 DA0	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	DATA/ADDRESS BUS DA(15:0): These signals comprise an active high multiplexed data/address bus for I/O and memory accesses. Only the low eight bits are used for data during I/O read and write cycles. During every I/O read and write, the voltage level on DA15 is used to help determine the monitor type, and can be read at port 3C2H bit 4. A logic 0 or logic 1 on DA15 places a logic 0 or a logic 1 into bit 4 of the Input Status Register 0, respectively. Refer to the general register description for more information. NOTE: "*" DA15 signal is multiplexed with data bit 15 and CRT monitor sense input for auto monitor detection.
			CPU CONTROL BUS
21	EMEM	I	ENABLE DISPLAY MEMORY: This signal is active high in both Micro Channel and AT modes. In AT Mode, EMEM enables video memory accesses. BIOS ROM accesses are not controlled by EMEM. If the video memory is within the lowest 1MB of the processor address space, EMEM signal must be active during video memory access. Otherwise, EMEM should be generated by external logic when the WD90C00 video memory is accessed. During AT Bus refresh time, EMEM can be connected to REFRESH to disable the WD90C00. In Micro Channel mode this signal enables I/O and video memory access. External logic is required to implement the function EMEM.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
10	$\overline{\text{ROM16}}$ $\overline{\text{SFDBK}}$	O	16 BIT WIDE BIOS ROM: In AT mode this active low status signal is the inverted value of register PR1(1), which determines BIOS ROM data path width selection. It may be used to control data buffers for a 16 bit data path BIOS ROM and to generate the signal -MEMCS16 in AT mode. In Micro Channel mode, $\overline{\text{SFDBK}}$ is the unlatched address decode (active low) when a memory, I/O, or BIOS ROM access is done from the system bus and may be considered as adapter or VGA feedback.
34	RDY	O	READY: An active high output which signals to the system processor that a memory access is completed and is only used to add wait states to the CPU bus cycles during video memory accesses. It is pulled inactive by WD90C00 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM. This is a tri-state signal.
35	IRQ	O	INTERRUPT REQUEST: It is enabled via bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of a Vertical Display occurs, this signal will transition active at the start of vertical retrace, causing the interrupt. It will stay latched until CRTC11 bit 4 clears it. In a AT mode, IRQ is tri-state upon power up reset and may be enabled by PR14(7). In Micro Channel mode, PR14(7) will power up IRQ enabled. This is a tri-state signal.
8	$\overline{\text{DS16}}$	O	DATA SIZE 16: Active low enable for 16 bit video memory word transfers. It is a mode dependent signal. In AT mode, $\overline{\text{DS16}}$ is a status signal as programmed in bit PR1(2) (and other registers) and is used to control the high and low byte 16 bit external data buffers. See the PR Register (PR1) description for further details. This status signal is also used to generate -MEMCS16 using external logic for AT mode designs. In Micro Channel mode, the signal is active only during BIOS ROM accesses (if enabled) by PR(1) and/or during memory 16 bit data path access (if enabled by PR1(2)).

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
33	$\overline{EIO}$ VGASETUP	I	ENABLE I/O: In AT mode, this active low signal enables I/O accesses to the WD90C00. In Micro Channel mode, this signal is the VGASETUP input pin and is connected to the latched card setup or the VGA setup. The externally designed system I/O port signals (96H for Adapter card or 94H bit 5 for system board design) is connected to the $\overline{EIO}$ pin. When this signal is high, the WD90C00 is enabled or in the operating state. An active low signal on this pin puts the WD90C00 into set up mode. During the set up mode, write logic 1H to WD90C00 internal port 102H to awaken the WD90C00 after power on.
9	$\overline{BHE}$	I	BUS HIGH ENABLE: In both AT and MCA mode, this active low signal enables and indicates a 16 bit transfer of data
31	$\overline{MRD}$ M/-I/O	I	MEMORY READ: In AT mode, this is an active low memory read strobe. It is asserted in 8/16 bit memory read cycles. In Micro Channel mode, the signal is called M/-IO. It distinguishes between memory and I/O cycles. When (M/-I/O) is high, a memory cycle is in process. A low on (M/-IO) shows that an I/O cycle is in process.
32	$\overline{MWR}$ -S0	I	MEMORY WRITE: The Active low memory write strobe in AT mode for 8/16 bit data transfers. In Micro Channel mode, it becomes -S0 and is the channel status signal which indicates the start and type of a channel cycle. Along with -S1, M/-IO, and -CMD signals, it is decoded to interpret I/O and memory commands.
29	$\overline{IOR}$ -S1	I	I/O READ: Active low I/O read strobe in AT mode. It is asserted in I/O read bus cycles. -S1 is the alternate mnemonic used in Micro Channel mode to indicate the start and type of a channel cycle.
30	$\overline{IOW}$ -CMD	I	I/O WRITE: Active low strobe. In AT mode, the strobe signals an I/O write cycle. In Micro Channel mode it is synonymous with -CMD; address bus validity is signaled by -CMD going low while the rising edge of -CMD indicates the end of a Micro Channel bus cycle.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
VIDEO MEMORY DATA			
89 90 91 92 93 94 95 96 97 98 99 2 3 4 5 6	MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8 MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0	I/O	DISPLAY MEMORY DATA MD(15:0): These lines are the data bus to the video display DRAMS. Data lines MD(7:0) are pulled up or down with resistors to provide set up information on power-up (reset) as follows: MD 15 Power-Up Function: EGA SW4 — Register (Bit): PR11(7)+ MD 14 Power-Up Function: EGA SW3 — Register (Bit): PR11(6)+ MD 13 Power-Up Function: EGA SW2 — Register (Bit): PR11(5)+ MD 12 Power-Up Function: EGA SW1 — Register (Bit): PR11(4)+ MD 11 Power-Up Function: ANALOG/TTL Display — Register (Bit): CNF(8) * MD 7 Power-Up Function: General Purpose — Register (Bit): CNF(7) * MD 6 Power-Up Function: General Purpose — Register (Bit): CNF(6) * MD 5 Power-Up Function: General Purpose — Register (Bit): CNF(5) * MD 4 Power-Up Function: General Purpose — Register (Bit): CNF(4) * MD 3 Power-Up Function: VCLK1,2 Input/Output — Register (Bit): CNF(3) + MD 2 Power-Up Function: AT/MicroChannel Mode — Register (Bit): CNF(2) + MD 1 Power-Up Function: BIOS ROM Data Path — Register (Bit): PR1(1) * MD 0 Power-Up Function: BIOS ROM Mapout — Register (Bit): PR1(0) * NOTE: "*" Pulldown resistor sets these bits to logic 1. "+" Pullup resistor sets these bits to logic 1. For more details refer to PR Registers.
VIDEO MEMORY ADDRESS			
63 65 66 67 68 69 70 71 72	MA8+ MA7+ MA6+ MA5+ MA4+ MA3+ MA2+ MA1+ MA0+	O	MEMORY ADDRESS MA(8:0): Display memory DRAM address. NOTE: "+" For testing purposes, these pins can be tri-stated by setting PR Register PR4(4) = 1.
VIDEO MEMORY CONTROL SIGNALS			
80	$\overline{\text{CAS10}}$+	O	COLUMN ADDRESS STROBE: Active low Memory Maps 1 & 0 CAS output signal.
83	$\overline{\text{CAS32}}$+	O	COLUMN ADDRESS STROBE: Active low memory maps 3 & 2 CAS output signal.
79	$\overline{\text{RAS10}}$+	O	ROW ADDRESS STROBE: Active low Memory Maps 1 & 0 RAS output signal.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
			VIDEO MEMORY CONTROL SIGNALS
82	$\overline{RAS32+}$	O	ROW ADDRESS STROBE: Active low Memory Maps 3 & 2 RAS output signal.
81	$\overline{OE10+}$	O	OUTPUT ENABLE: Active low Memory Maps 1 & 0 DRAM output enable.
84	$\overline{OE32+}$	O	OUTPUT ENABLE: Active low Memory Maps 3 & 2 DRAM output enable.
85	$\overline{WE0+}$	O	WRITE ENABLE: Active low Write Enable to DRAM bank 0, upper byte (Memory map 0).
86	$\overline{WE1+}$	O	WRITE ENABLE: Active low Write Enable for DRAM bank 0, upper byte (Memory map 1)
87	$\overline{WE2+}$	O	WRITE ENABLE: Active low Write Enable for DRAM bank 1, lower byte (Memory map 2).
88	$\overline{WE3+}$	O	WRITE ENABLE: Active low Write Enable for DRAM bank 1, upper byte (Memory map 3). NOTE: 1. "+" For testing purposes, these pins can be tri-stated by setting PR Register PR4(4) = 1.
			RAMDAC INTERFACE
48 49 50 53 54 55 56 57	VID7* VID6* VID5* VID4* VID3* VID2* VID1* VID0*	O	VIDEO VID(7:0): Pixel video data output to DAC. NOTE: "*" For testing purposes, these pins can be tri-stated by setting PR Register PR4 (5) = 1.
47	$\overline{RPLT}$	O	READ PALETTE: Video DAC register and color palette read signal. Active low during I/O read to addresses at 3C6H, 3C8H, and 3C9H.
58	$\overline{WPLT}$	O	WRITE PALETTE: Video DAC register and color palette write signal. Active low during I/O write to addresses at 3C6H-3C9H.
59	PCLK	O	PIXEL CLOCK: Video pixel clock output used by the RAMDAC to latch video signals VID(7:0). Its source is one of the video clock inputs: VCLK0, VCLK1, or VCLK2 as determined by the Miscellaneous Output register. Note that VCLK0, 1, or 2 is divided by two in 320/360 pixel display mode to derive PCLK. MCLK can be the source of this clock.
62	$\overline{BLNK}$ *	O	BLANK: Active low RAMDAC blank pulse. NOTE: "*" For testing purposes, this pin can be tri-stated by setting PR Register PR4 (5) = 1.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
			CRT CONTROL
60	HSYNC+	O	HORIZONTAL SYNC: Display monitor horizontal synchronization pulse. Active high or low depending on the Miscellaneous register programming. SEE NOTE BELOW.
61	VSYNC+	O	VERTICAL SYNC: Active high display monitor vertical synchronization pulse. It is active high or low, depending on the Miscellaneous Output Register. NOTES: 1. "+" For testing purposes, these pins can be tri-stated by setting PR Register PR4(5)=1.
			BIOS ROM CONTROL
7	$\overline{\text{EBROM}}$	O	ENABLE BIOS ROM ACCESS: In both AT and Micro Channel modes this signal is active (low) during memory reads in the address range (C000:0H-C7FF:FH) if enabled by bit PR1(0). It is not active for accesses to addresses in the range C600:0H-C67F:FH. However, the C600:0H-C67F:FH address range can be mapped in to increase BIOS space by setting PR17(0) = 0. In AT mode only, a write to the WD90C00 internal I/0 port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
			BUFFER CONTROL
11	$\overline{\text{EDBUFH}}$	O	ENABLE ADDRESS BUFFER: This active low signal permits control of an external address buffer for multiplexing aqyddress and data to WD90C00. It is tri-stated while Reset is active. When in MCA implementation, this output becomes the high byte data bus enable signal during the 16 bit data transfers and is referred as $\overline{\text{EDBUFH}}$.
38	$\overline{\text{EDBUF}}$	O	ENABLE DATA BUFFER: Allows control of an external data buffer for multiplexing address and data to WD90C00. It is tri-stated while Reset is active.
37	DIR	O	DIRECTION CONTROL: Active high Direction Control for reads of the DA(15:0) data bus in AT and MCA implementation. The default state is low until a read cycle occurs, and the WD90C00 will drive DIR high to change the direction of the data buffers.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
POWER AND GROUND			
25	VCC	—	+5VDC
52	VCC	—	+5VDC
78	VCC	—	+5VDC
100	VCC	—	+5VDC
1	GND	—	Ground
15	GND	—	Ground
26	GND	—	Ground
51	GND	—	Ground
64	GND	—	Ground
77	GND	—	Ground

5.0 ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0 °C to 70 °C
Storage temperature	- 40 °C to 125 °C
Voltage on all inputs and outputs to Vss	- 0.3 to 7 Volts
Power dissipation	1.0 Watt

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

6.0 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to Vss (0V Ground). Positive current flows into the reference pin.

Operating temperature range	0° C to 7 °C
Power supply voltage	4.75 to 5.25 Volts

7.0 D.C CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX	UNITS	CONDITIONS
V(IL)	Input Low Voltage	--	0.8	V	VCC=5V±5%
V(IH)	Input High Voltage	2.0	--	V	VCC=5V±5%
I(IL)	Input Low Current	--	±10	uA	VIN=0.0V
I(IH)	Input High Current	--	±10	uA	VIN=VCC
V(OL)	Output Low Voltage	--	0.4	V	IOL +4.0mA[1]
V(OH)	Output High Voltage	2.4	--	V	IOH=4.0mA[1]
I(OZ)	High Impedance Leakage Current	-10.0	10.0	uA	0V
I(CC)	Stand By Current (All Inputs at TTL Levels)	--	22	mA	VCC=5.25 VDC TA=0 °C, Static
I(DD)	Operating current	--	130	mA	VCC=5.25V, MCLK=VCLK=45 MHz
C(IN)	Input Capacitance	--	10	pF	FC=1 MHz
C(OUT)	Output Capacitance	--	10	pF	FC=1 MHz

TABLE 2. DC CHARACTERISTICS

NOTES

1. WD90C00 outputs have 4.0 mA maximum source and sink capability except for pin RDY = 24.0 mA sink and 4.0 mA source and pin IRQ = 24.0 mA sink and 4.0 mA source.

2. Pullups on MD(0:15), DA(0:15), $\overline{\text{EDBUF}}$, $\overline{\text{EABUF}}$ = 100 K ohms. Pullup on $\overline{\text{BHE}}$ = 50 K ohms.

8.0 AC TIMING CHARACTERISTICS

C_L = load capacitance = 70 pf unless specified otherwise.

t=1/MCLK in all modes
Units are in nanoseconds (ns).

NUMBER	PARAMETER	MIN	MAX	NOTES
	RESET TIMING			
1	Reset Pulse Width	10t		1
2	MD Setup to RSET low	2t		
3	MD Hold from RSET low	2t		
4	Vcc high to RSET high setup	100		
5	RSET low to first $\overline{MRD}$/ $\overline{IOW}$	10t		
	CLOCK TIMING			
1	Input Clock (MCLK or VCLK) Period	t	t	
2	Clock low	40%t		2
3	Clock high		60%t	2
4	Clock Rise Time		3	3
5	Clock Fall Time		3	3
6	Input VCLK to PCLK Delay		13	
9a	PCLK to Hsync and Vsync Delay		6.5	
9b	PCLK to $\overline{BLNK}$ Delay		6.5	
9c	PCLK to VID(7:0) Delay		3	
	AT MODE I/O & MEMORY READ/WRITE TIMING			
1	$\overline{EIO}$ setup to $\overline{IOR}$ and $\overline{IOW}$ active	8		
2	$\overline{EIO}$ hold from $\overline{IOR}$ and $\overline{IOW}$ inactive	5		
3	EMEM setup to $\overline{MR}$ and $\overline{MW}$ active	4		
4	EMEM hold from $\overline{MR}$ and $\overline{MW}$ inactive	4		
5	$\overline{EABUF}$ inactive from $\overline{IOR}$/ $\overline{W}$, $\overline{MR}$/ $\overline{W}$ active		30	
6a	$\overline{EABUF}$ active from $\overline{EDBUF}$ inactive (I/O R&W)		21	
6b	$\overline{EABUF}$ active from $\overline{EDBUF}$ inactive (M R&W)		15	
7a	$\overline{EDBUF}$ active from $\overline{EABUF}$ inactive (I/O R&W)		13	
7b	$\overline{EDBUF}$ active from $\overline{EABUF}$ inactive (M R&W)		35	

TABLE 3. AC TIMING CHARACTERISTICS

1. The MCLK should be running with the reset applied.
2. Measured at 1.4V.
3. Measured between 0.8V and 2.0V.

20

NUMBER	PARAMETER	MIN	MAX	NOTES
AT MODE I/O & MEMORY READ/WRITE TIMING (CONTINUED)				
8	EDBUF inactive from IOR/ W, MR/ W inactive		21	
9	DIR active from IOR and MR active		24	
10	DIR inactive from IOR and MR inactive		21	
11a	BHE setup to MR and MW active	4		
11b	Address setup to IOR and IOW active	8		
11c	Address setup to MR and MW active	4		
12a	BHE hold to MR and MW active	6		
12b	Address hold to IOR and IOW active	4		
12c	Address hold to MR and MW active	6		
13	DA(15:0) valid address setup to IOR/ W, MR/ W	13		
14	DA(15:0) valid address hold from IOR/ W, MR/ W	4		
15	Data setup to IOW inactive	10		
16	Data hold from IOR/ W, MR/ W inactive	8		
17a	Data valid from IOR active		2t + 42	
17b	Data valid (CAS32 inactive) from MR active	11.5t		
17c	Write data valid from MW active	4.5t-50		4
18	Read data setup to RDY high	3.5t-40		5
19	RDY inactive from MR and MW active		13	
20	RDY active from MW, MR active	15t		
21	RDY tri-state from MW, MR inactive		10	
22	WPLT active from IOW active		2t+35	
23	WPLT inactive from IOW inactive		22	
24	RPLT active from IOR active		31	
25	RPLT inactive from IOR inactive		21	
26	EBROM active from IOW active (46E8)		2t+29	
27	EBROM inactive from IOW inactive		20	
28	EBROM active from valid address		20	
29	EBROM inactive from MRD inactive		23	
30	VCLK1 (as output) delay from IOW		2t+33	

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

4. This spec includes 50 ns worst case delay from DA to MD bus.
5. This spec includes 40 ns worst case delay from MD to DA bus.

NUMBER	PARAMETER	MIN	MAX	NOTES
	MICRO CHANNEL I/O & MEMORY READ AND WRITE TIMING			
1	$\overline{\text{CDSETUP}}$ setup to $\overline{\text{CMD}}$ active	0		
2	$\overline{\text{CDSETUP}}$ hold from $\overline{\text{CMD}}$ inative	4		
3	EMEM, $\overline{\text{BHE}}$, Address setup to $\overline{\text{CMD}}$	10		
4	EMEM, $\overline{\text{BHE}}$, Address hold from $\overline{\text{CMD}}$	6		
5	$\overline{\text{S1}}$, $\overline{\text{S0}}$, M/ $\overline{\text{IO}}$ setup to $\overline{\text{CMD}}$	10		
6	$\overline{\text{S1}}$, $\overline{\text{S0}}$, M/ $\overline{\text{IO}}$ hold from $\overline{\text{CMD}}$	6		
7	$\overline{\text{EABUF}}$, $\overline{\text{EDBUF}}$ active from $\overline{\text{CMD}}$ active		26	
8	$\overline{\text{EABUF}}$, $\overline{\text{EDBUF}}$ inactive from $\overline{\text{CMD}}$ inactive		22	
9	DIR active from $\overline{\text{CMD}}$ active		22	
10	DIR inactive from $\overline{\text{CMD}}$ inactive		22	
11a	$\overline{\text{SFDBK}}$ active from $\overline{\text{CMD}}$ active (IO R&W)		27	
11b	$\overline{\text{SFDBK}}$ active from $\overline{\text{CMD}}$ active (M R&W)		19	
12a	$\overline{\text{SFDBK}}$ inactive from $\overline{\text{CMD}}$ inactive(IO R&W)		25	
12b	$\overline{\text{SFDBK}}$ inactive from $\overline{\text{CMD}}$ inactive(M R&W)		19	
13	$\overline{\text{SFDBK}}$ inactive from invalid address		25	
14	$\overline{\text{DS16}}$ active from valid address (M R&W)		29	
15	$\overline{\text{DS16}}$ inactive from invalid address		20	
16	Address setup to $\overline{\text{CMD}}$ active	7		
17	DA (15:0) valid address hold from $\overline{\text{CMD}}$ active	4		
18	Write data setup to $\overline{\text{CMD}}$ inactive	10		
19	Write data hold from $\overline{\text{CMD}}$ inactive	7		
20a	Read data valid from $\overline{\text{CMD}}$ active	11.5t		
20b	Write data valid from $\overline{\text{CMD}}$ active	4.5t-50		6
21	Read data setup to RDY high	3.5t-40		7
22	RDY inactive from status (MR)		22	
23	RDY active from $\overline{\text{CMD}}$ active	15t		
24	RDY inactive from $\overline{\text{CMD}}$ inactive		41	
25	$\overline{\text{EBROM}}$ active from valid address		22	
26	$\overline{\text{EBROM}}$ inactive from $\overline{\text{CMD}}$ inactive		29	
27	$\overline{\text{WPLT}}$ active from $\overline{\text{CMD}}$ active		41	
28	$\overline{\text{WPLT}}$ inactive from $\overline{\text{CMD}}$ inactive		22	
29	$\overline{\text{RPLT}}$ active from $\overline{\text{CMD}}$ active		31	
30	$\overline{\text{RPLT}}$ inactive from $\overline{\text{CMD}}$ inactive		23	
31, 32	VCLK1 delay from $\overline{\text{CMD}}$		33	

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

6. This spec includes 50 ns worst case delay from DA to MD bus.
7. This spec includes 40 ns worst case delay from MD to DA bus.

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM TIMING, CPU READ AND WRITE			
1	$\overline{RAS10}$, $\overline{RAS32}$ cycle time	9t		
2a	$\overline{RAS10}$, $\overline{RAS32}$ pulse width low	5t-8	5t	
2b	$\overline{RAS10}$, $\overline{RAS32}$ low to $\overline{CAS10}$, $\overline{CAS32}$ high	5t-11	5t-2	
3	$\overline{RAS10}$, $\overline{RAS32}$ precharge	4t+1	4t+8	
4	$\overline{RAS10}$, $\overline{RAS32}$ low to $\overline{CAS10}$, $\overline{CAS32}$ low	2t-11	2t+2	
5a	$\overline{CAS10}$, $\overline{CAS32}$ low to $\overline{RAS10}$, $\overline{RAS32}$ high	3t-8	3t+3	
5b	$\overline{CAS10}$, $\overline{CAS32}$ pulse width low	3t-4	3t	
6	$\overline{CAS10}$, $\overline{CAS32}$ high to $\overline{RAS10}$, $\overline{RAS32}$ low	4t+2	4t+14	
7	Row Address setup to $\overline{RAS10}$, $\overline{RAS32}$ low	1t-10	1t+5	
8	Row Address hold from $\overline{RAS10}$, $\overline{RAS32}$ low	1t-6	1t+8	
9	Column address setup to $\overline{CAS10}$, $\overline{CAS32}$ low	1t-12	1t+1	
10	Column address hold from $\overline{CAS10}$, $\overline{CAS32}$ low	1.5t	1.5t+14	
11	$\overline{CAS10}$, $\overline{CAS32}$ precharge high	6t	6t+4	
12	WE0:1 low setup to $\overline{CAS10}$, $\overline{RAS10}$ high	2.5t-7	2.5t+4	
13a	WE3:2 low setup to $\overline{CAS32}$, $\overline{RAS32}$ high	5t-7	5t+4	
13b	$\overline{WE3}$, $\overline{WE2}$ pulse width low	5t-2	5t+2	
17	$\overline{WE0}$, $\overline{WE1}$ pulse width low	3t-2	3t+2	
18	Data hold from $\overline{WE0}$, $\overline{WE1}$ active	2t-5		
19	Data setup to $\overline{WE0}$, $\overline{WE1}$ active	1t-5		
20	$\overline{WE0}$, $\overline{WE1}$ low from $\overline{CAS10}$ low	.5t-7	.5t+4	
21	$\overline{WE3}$, $\overline{WE2}$ setup to $\overline{CAS32}$ low	2t-4	2t+7	
22	$\overline{OE10}$, $\overline{OE32}$ low after $\overline{CAS10}$, $\overline{CAS32}$ low	1t-6	1t+5	
23	$\overline{OE10}$, $\overline{OE32}$ high after $\overline{CAS10}$, $\overline{CAS32}$ high	1t-5	1t+5	
24	$\overline{OE10}$, $\overline{OE32}$ pulse width low	3t-3	3t+1	
25	Read data setup to CAS inactive	10		
26	Read data hold from CAS inactive	10		
27	$\overline{RAS32}$ low after $\overline{RAS10}$ low	4.5t-7	4.5t+7	
28	Write data setup to $\overline{CAS\ 32}$	2t-5		
29	Write data hold from $\overline{CAS32}$	1t-5		
30	$\overline{CAS10}$, $\overline{CAS32}$ high after $\overline{OE10}$, $\overline{OE32}$ low	2t-8	2t+2	

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM PAGE MODE READ AND WRITE TIMING			
1	RAS10, RAS32 pulse duration	7t		
2	Page mode CAS10 cycle time	5t		8
3	RAS10, RAS32 precharge	4t	4t+8	
4	RAS10 low to first CAS10 high	5t-14	5t-2	
5	RAS10, RAS32 low to CAS10, CAS32 low	2t-11	2t+2	
7	CAS10, CAS32, OE10, OE32 pulse width high	2t	2t+4	9
8	CAS10, low to RAS10 high	3t-8	3t+3	
9	CAS32 low to RAS32 high	5t-8	5t+3	
10, 14	Row address setup to RAS10, RAS32 low	1t-10	1t+5	
11, 15	Row address hold from RAS10, RAS32 low	1t-6	1t+8	
12, 16	Column address setup to CAS10, CAS32 low	1t-12	1t+1	
13, 17	Column address hold from CAS10, CAS32 low	1.5t	1.5t+14	
18	RAS32 low after RAS10 low	4.5t-7	4.5t+7	
19	Read data setup to CAS inactive	10		
20	Read data hold from CAS inactive	10		
21	OE10, OE32 pulse width low	3t-3	3t+1	
22	OE10, OE32 low after CAS10, CAS32 low	1t-6	1t+5	
23	OE10, OE32 high after CAS10, CAS32 high	1t-5	1t+5	
24	CAS10, CAS32 pulse width low	3t-4	3t	
25	CAS10, CAS32 high after OE10, OE32 low	2t-8	2t+2	

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

8. First cycle is two mclocks longer than this spec.
9. CAS10 and OE10 are two mclocks longer for the first cycle.

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM REFRESH TIMING			
1	Address Setup to $\overline{\text{RAS10}}$ active	2t-5		10
2	Address Hold from $\overline{\text{RAS32}}$ active	3t-5		
3	$\overline{\text{RAS10}}$ low time	5t-8		
4	$\overline{\text{RAS10}}$ high time	4t+1		
5	$\overline{\text{RAS32}}$ low time	5t+1		
6	$\overline{\text{RAS32}}$ high time	4t-8		
7	RAS cycle time	9t		

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

10. This spec is shorter by 1 mclock for the first cycle.

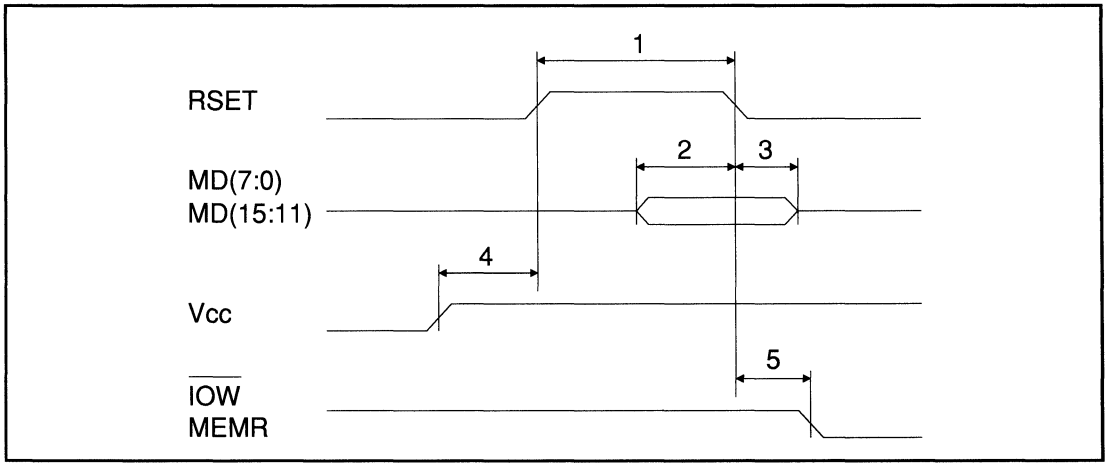


FIGURE 4. RESET TIMING

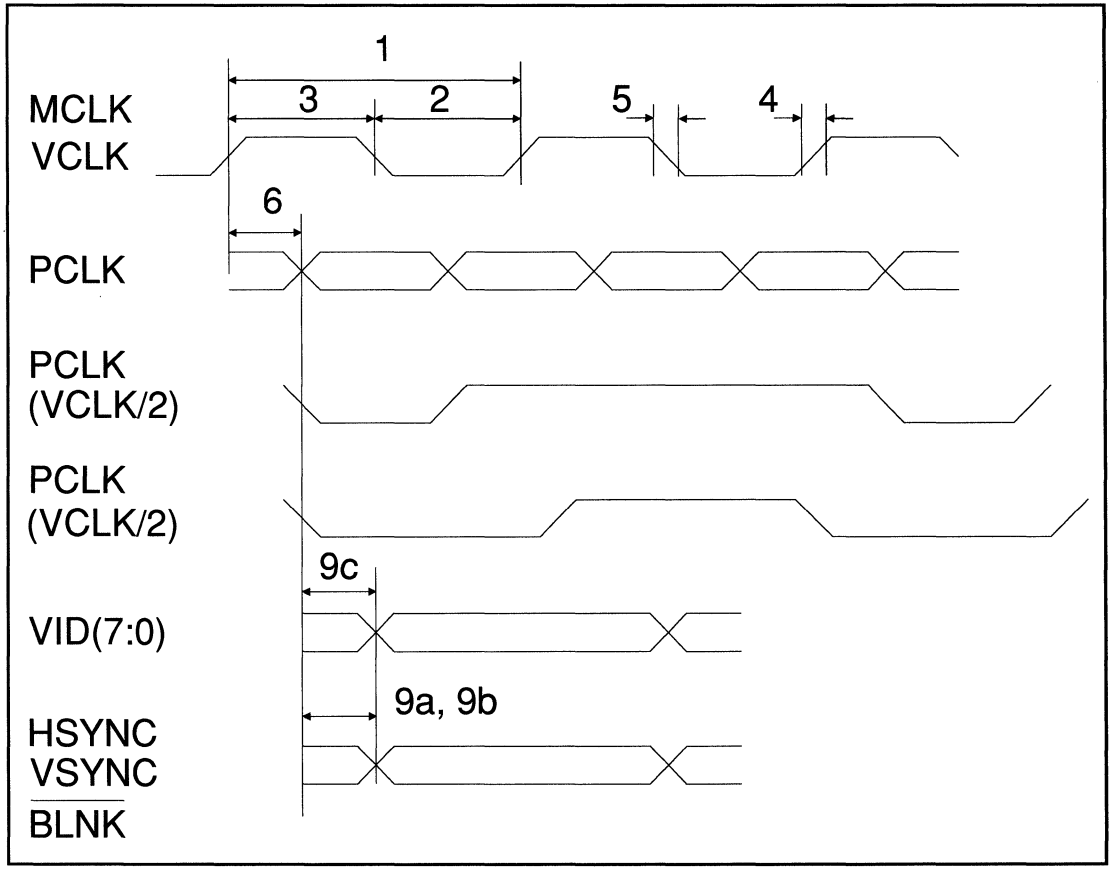


FIGURE 5. CLOCK AND VIDEO TIMING

20

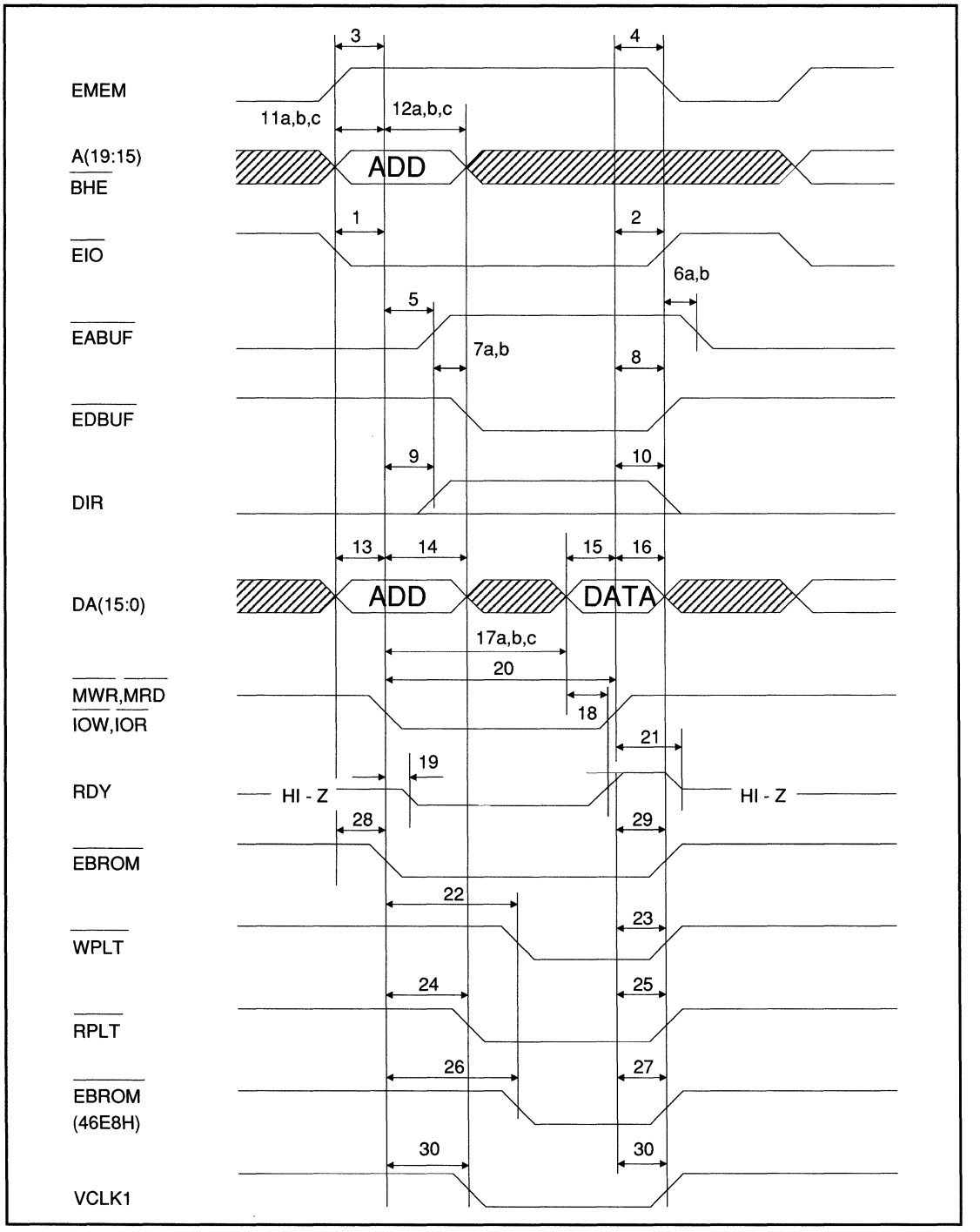


FIGURE 6. AT MODE I/O & MEMORY READ/WRITE TIMING

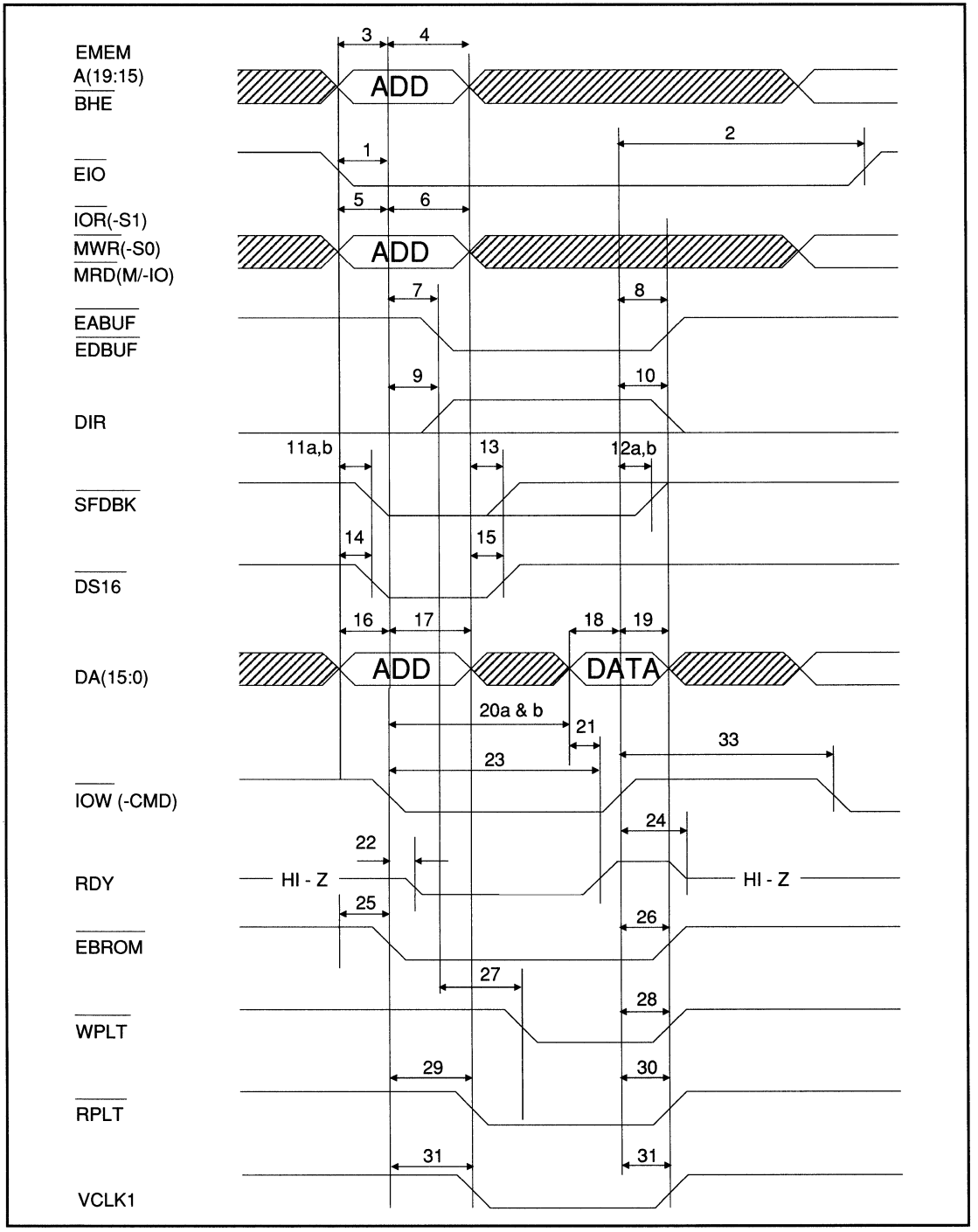


FIGURE 7. MICRO CHANNEL I/O & MEMORY READ & WRITE TIMING

20

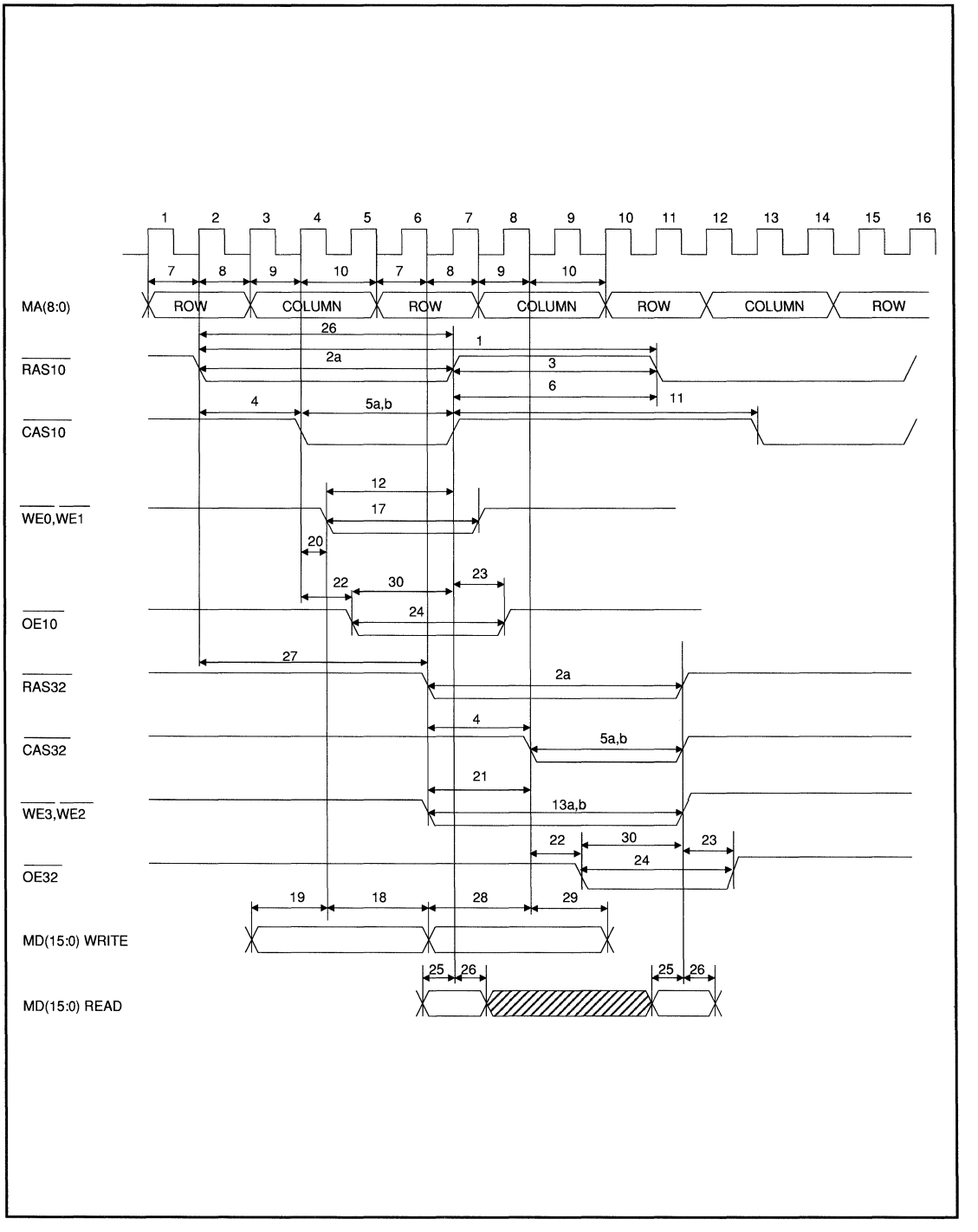


FIGURE 8. CPU READ/WRITE DRAM TIMING

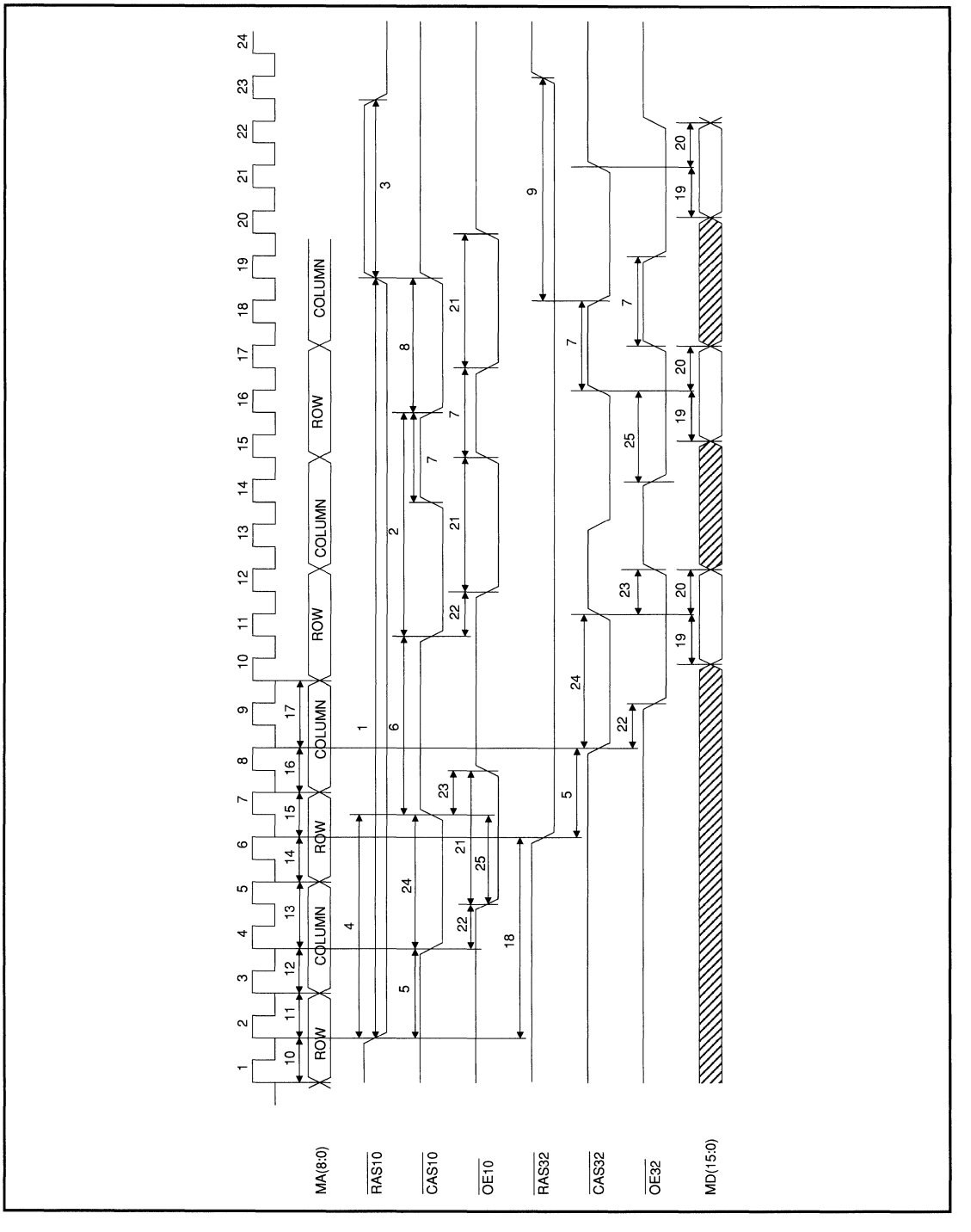


FIGURE 9. DRAM PAGE MODE READ TIMING

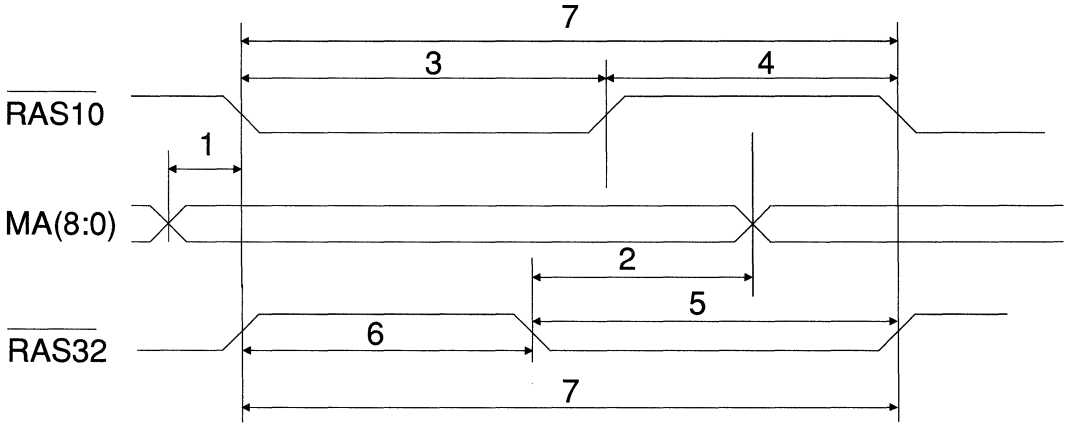


FIGURE 10. DRAM REFRESH TIMING

9.0 WD90C00 REGISTERS

All of the standard IBM registers incorporated inside the WD90C00 are functionally equivalent to the VGA implementation while additional PR registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards defined earlier using the 6845 CRT Controller. This section describes the WD90C00 registers in greater detail.

9.1 VGA REGISTERS SUMMARY

REGISTERS	RW	MONO	COLOR	EITHER
GENERAL REGISTERS				
Miscellaneous Output Reg	W			3C2
	R			3CC
Input Status Reg 0	RO			3C2
Input Status Reg 1	RO	3BA	3DA	
Feature Control Reg	W	3BA	3DA	
	R			3CA
+Video Subsystem Enable	RW			3C3
NOTE: + Video Subsystem Enable Register 3C3H needs to be implemented externally in a Micro Channel configuration.				
SEQUENCER REGISTERS				
Sequencer Index Reg	RW			3C4
Sequencer Data Reg	RW			3C5
CRT CONTROLLER REGISTERS				
Index Reg	RW	3B4	3D4	
CRT Controller Data Reg	RW	3B5	3D5	
GRAPHICS CONTROLLER REGISTERS				
Index Reg	RW			3CE
Other Graphics Reg	RW			3CF
ATTRIBUTE CONTROLLER REGISTERS				
Index Reg	RW			3C0
Attribute Controller Data Reg	W			3C0
	R			3C1
VIDEO DAC PALETTE REGISTERS				
Write Address	RW			3C8
Read Address	W			3C7
DAC State	R			3C7
Data	RW			3C9
Pel Mask	RW			3C6

TABLE 4. VGA REGISTERS SUMMARY

9.2 PR REGISTERS SUMMARY

REGISTERS	RW	MONOCHROME	COLOR
PR Register Index	RW	3CE	3CE
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10-PR17 INDEX	RW	3B4	3D4
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
Reserved 3X5.31- 3X5.3F			

TABLE 5. PR REGISTERS SUMMARY

NOTE: ALL THE PR REGISTERS ARE WRITE PROTECTED. SEE THE PR REGISTERS' DESCRIPTION FOR MORE DETAILS.

9.3 COMPATIBILITY REGISTERS SUMMARY

FUNCTIONS	RW	MDA	CGA	AT&T	HERCULES
Mode Control Reg	WO	3B8	3D8	3D8	3B8
Color Select Reg	WO		3D9	3D9	
Status Reg	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Reg	WO			3DE	
Hercules Reg	WO				3BF
+CRTC	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

TABLE 6. COMPATIBILITY REGISTERS SUMMARY

NOTES:

1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. + = 6845 Mode Registers

9.4 VGA REGISTERS

Throughout this section, all bit graphics and definitions apply to VGA mode followed by their brief description.

9.5 GENERAL REGISTERS

NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES:

1. Reserved bits should be set to zero.

2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes

   1 = D in Color Modes

9.5.1 Miscellaneous Output Register, Read Port = 3CC, Write Port = 3C2

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.
0= Positive vertical sync polarity.
1= Negative vertical sync polarity.

Bit 6 *

Horizontal Sync Polarity Selection.
0= Positive horizontal sync polarity.
1= Negative horizontal sync polarity.

NOTE:

*These bits determined the vertical size of the vertical frame by the monitor. Their encoding is shown below:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.
When in modes 0-5, one memory page is selected from the two 64KB pages.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bit(3:2) Clock Select 1,0.

BIT 3	BIT 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

Bit 1

System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection. Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0= CRTC and status addresses for MDA mode (3BX).
1= CRTC and status addresses for CGA mode (3DX).

9.5.2 Input Status Register 0, Read Only Port = 3C2

BIT	FUNCTION
7	CRT Interrupt
6, 5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3: 0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit(6:5)

Reserved in VGA.

Bit 4

Monitor Detection in VGA mode. DA15 monitor status (pin 20) is sampled and can be read from this bit.

Bit(3:0)

Reserved.

9.5.3 Input Status Register 1, Read Only Port = 3?A

BIT	FUNCTION
7, 6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved
0	Display Enable

Bit(7:6)

Reserved.

Bit(5:4)

Color Plane Diagnostics.
These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.
0= Vertical frame is displayed.
1= Vertical retrace is active.

Bit(2:1)

Reserved.

Bit 0

Display Enable Status.
0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

9.5.4 Feature Control Register, Read Port = 3CA, Write Port = 3?A

BIT	FUNCTION
7 - 4	Reserved
3	Vertical Sync Control
2 - 0	Reserved

Bits(7:4)

Reserved

Bit 3

Vertical Sync Control:
0: Vsync output enabled
1: Vsync output is logical "OR" of Vsync and Vertical Display Enable.

Bit(2:0)

Reserved

9.6 SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE: Reserved bits should be set to zero.

9.6.1 Sequencer Index Register, Read/Write Port = 3C4

BIT	FUNCTION
7 - 3	Reserved
2 - 0	Sequencer Address/Index Bits

Bit(7:3)

Reserved.

Bit(2:0)

Sequencer Address/Index.
The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer register to be accessed.

9.6.2 Reset Register, Read/Write Port = 3C5, Index = 00

BIT	FUNCTION
7 - 2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

NOTE:

Due to the improved design of the WD90C00, the fuction of Bits (1:0) are not required and are instead implemented as shadow registers.

Bit(7:2)

Reserved.

Bit 1

Synchronous Reset.
0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0

Asynchronous Reset.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

9.6.3 Clocking Mode Register, Read/Write Port = 3C5, Index = 01

BIT	FUNCTION
7, 6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load
1	Reserved
0	8/9 Dot Clocks

Bit(7:6)

Reserved.

Bit 5

Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character or every other character clock depending on bit 2.
1 = Serial shift registers loaded every 4th character clock (32-bit fetches).

Bit 3

Dot Clock Selection
0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360 pixels).

Bit 2

Shift Load. Effective only if bit 4=0.
0 = Video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.
Commands Sequencer to generate 8 or 9 dot wide character clock.
0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

9.6.4 Map Mask Register, Read/Write Port = 3C5, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bit(7:4)

Reserved.

Bit(3:0)

Controls Writing To Memory Maps (0-3) respectively.
0 = Writing to maps (0-3) disallowed.
1 = Maps (0-3) accessible.

9.6.5 Character Map Select Register Read/Write Port = 3C5, Index = 03

BIT	FUNCTION
7, 6	Reserved
5	Character Map Select A Bit 2
4	Character Map Select B Bit 2
3	Character Map Select A Bit 1
2	Character Map Select A Bit 0
1	Character Map Select B Bit 1
0	Character Map Select B Bit 0

If Sequencer Register 4 bit 1 is 1, then the attribute byte bit 3 in text modes is redefined to control switching between character sets. A 0 selects character map B. A 1 selects character map A. Character Map selection from either plane 2 or plane 3 is determined by PR2(2), PR2(5) and bit 4 of the attribute code.

Bit(7:6)

Reserved.

Bit 5

Character Map A MSB Select.
The Most Significant Bit (MSB) of character map A along with bits 3 and 2, select the location of character map A as shown below.

BITS 5 3 2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit 4

Character Map B MSB Select.
The MSB of character map B along with bits 1 and 0, select the location of character map B as shown below.

BITS 4 1 0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit(3:2)

Character Map Select A.
Refer to bit 5 table.

Bit(1:0)

Character Map Select B.
Refer to bit 4 table.

9.6.6 Memory Mode Register, Read/Write Port = 3C5, Index = 04

BIT	FUNCTION
7 - 4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bit(7:4)

Reserved.

Bit 3

Chains 4 Maps.
0 = Processor sequentially accesses data using map mask register.
1 = Directs the two lower order video memory address pins (MA0,MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.
0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.
1 = Sequential processor access as defined by map mask register.

Bit 1

Extended Video Memory.
0 = 64 KB of video memory.
1 = Greater than 64KB of memory for VGA/EGA modes.

Bit 0

Reserved.

9.7 CRT CONTROLLER REGISTERS

PORT	INDEX	VGA REGISTER NAME	*6845 REG NAME
3?4	---	CRT Controller Address Reg.	CRTC Address Reg
3?5	00	Horizontal Total	Hor. Total
3?5	01	Horizontal Display Enable End	Hor. Disp
3?5	02	Start Horizontal Blanking	+
3?5	03	End Horizontal Blanking	+
3?5	04	Start Horizontal Retrace	+
3?5	05	End Horizontal Retrace	+
3?5	06	Vertical Total	Vert. Disp.
3?5	07	Overflow	+
3?5	08	Preset Row Scan	+
3?5	09	Maximum Scan Line/Others	Max. Scan Line Add.
3?5	0A	Cursor Start	Cursor Start
3?5	0B	Cursor End	Cursor End
3?5	0C	Start Address High	Start Add. High
3?5	0D	Start Address Low	Start Add. Low
3?5	0E	Cursor Location High	Cursor Loc. High
3?5	0F	Cursor Location Low	Cursor Loc. Low
3?5	10	Vertical Retrace Start	Light Pen High Read
3?5	11	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	+
3?5	13	Offset	+
3?5	14	Underline Location	+
3?5	15	Start Vertical Blank	+
3?5	16	End Vertical Blank	+
3?5	17	CRTC Mode Control	+
3?5	18	Line Compare	+

TABLE 7. CRT CONTROLLER REGISTERS

NOTES:

1. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0=B in Monochrome Modes and
1=D in Color Modes

2. "*" 6845 Mode Registers are defined and explained in greater detail in the reference literature.

3. "+" This register can be programmed in VGA mode only. It is not applicable in 6845 mode.

4. Reserved bits should be set to zero.

9.7.1 CRT Address Register Read/Write Port = 3?4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Index bits

Bit(7:5)

Reserved.

Bit(4:0)

Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed hex.

9.7.2 Horizontal Total Register Read/Write Port = 3?5, Index=00H

BIT	FUNCTION
7 - 0	Horizontal Total Period

This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

Bit(7:0)

Count Plus Retrace Less 5.
In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line.

9.7.3 Horizontal Display Enable End Register Read/Write Port = 3?5, Index 01H

BIT	FUNCTION
7 - 0	Displayed Characters per scan line

Bit(7:0)

Horizontal blanking begins when the horizontal character counter reaches this character clock value.

9.7.4 Start Horizontal Blanking Register Read/Write Port = 3?5, Index = 02H

BIT	FUNCTION
7 - 0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches this character clock value. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

9.7.5 End Horizontal Blanking Register Read/Write Port = 3?5, Index = 03H

BIT	FUNCTION
7	Reserved
6, 5	Display Enable Signal Skew Control
4 - 0	End Horizontal Blanking (lower 5 bits)

This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

Bit 7

Reserved

Bit(6:5)

Display Enable Signal Skew Control.
They define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

BIT 6	BIT 5	SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

End Horizontal Signal Width.
End Horizontal Blank signal width "W" is determined as the value of start blanking register plus "W" in character clocks. The least significant five bits are programmed in this register, while the most significant bit is the End Horizontal Retrace Register (Index 05H) bit 7.

9.7.6 Start Horizontal Retrace Register Read/Write Port = 3?5, Index = 04H

BIT	FUNCTION
7 - 0	Start Horizontal Retrace Character Count

Bit(7:0)

Start Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

9.7.7 End Horizontal Retrace Register Read/Write Port = 3?5, Index = 05H

BIT	FUNCTION
7	End Horizontal Blank bit 6
6, 5	Horizontal Retrace Delay
4 - 0	End Horizontal Retrace

This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

Bit 7

MSB (Sixth Bit) Of End Horizontal Blanking Register.

Bit(6:5)

Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

BIT 6	BIT 5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

Bit(4:0)

End Horizontal Retrace Pulse Width "W".
Start retrace register value is added to the character count for width "W". The least significant five bits are programmed in this register. When the Start Horizontal Retrace Register value matches these five bits, the horizontal retrace signal is turned off.

9.7.8 Vertical Total Register Read/Write Port = 3?5,Index = 06H

BIT	FUNCTION
7 - 0	Vertical Total Scan Lines

Bit(7:0)

Raster Scan Line Total Less 2.
The least significant eight bits of a ten bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync are also included. The ninth and tenth bits of this count are loaded into the Vertical Overflow Register (index = 07H) bit 0 and bit 5 respectively. In 6845 modes, total vertical display time in rows is programmed into bit 6 - bit 0, while bit 7 is reserved. Scan count reduction is not necessary. (The number of scan lines in a row is determined by the maximum Scan Line Register (index 09H bits 0 through 4). This register is locked if the PR Register PR3 (0) = 1 or the Vertical Retrace End Register bit 7 = 1.

9.7.9 Overflow Vertical Register Read/Write Port = 3?5, Index = 07H

BIT	FUNCTION
7	Vert. Ret. Start Bit 9
6	Vert. Display Enable End Bit 9
5	Vert. Total Bit 9
4	Line Compare Bit 8
3	Start Vert. Blank Bit 8
2	Vert. Ret. Start Bit 8
1	Vert. Display Enable End Bit 8
0	Vert. Total Bit 8

++Bit 7

Vertical Retrace Start Bit 9 (index = 10H).

****Bit 6**

Vertical Display Enable End Bit 9 (index = 12H).

++Bit 5

Vertical Total Bit 9 (index = 06H).

Bit 4

Line Compare Bit 8 (index = 18H).

++Bit 3

Start Vertical Blank Bit 8 (index =15H).

++Bit 2

Vertical Retrace Start Bit 8 (index = 10H).

****Bit 1**

Vertical Display Enable End Bit 8 (index = 12H).

++Bit 0

Vertical Total Bit 8 (index = 06H).

NOTES:

** This register is locked if the PR Register PR3(1)=0 AND the Vertical Retrace End Register bit 7 = 1.

++ This register is locked if the PR Register PR3(0) = 1 OR the Vertical Retrace End Register bit 7 = 1.

9.7.10 Preset Row Scan Register Read/Write Port = 3?5, Index = 08H

BIT	FUNCTION
7	Reserved
6, 5	Byte Panning Control
4 - 0	Preset Row Scan Count

Bit 7

Reserved.

Bit(6:5)

Byte Panning Control.
These bits allow up to 3 bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 byte left shift
1	0	2 bytes left shift
1	1	3 bytes left shift

Bit(4:0)

Preset Row Scan Count.
These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

9.7.11 Maximum Scan Line Register Read/Write Port=3?5, Index=09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare bit 9
5	Start Vertical Blank bit 9
4 - 0	Maximum Scan Line

Bit 7

200 To 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.
This is bit 9 of the Line Compare Register (index = 18H).

Bit 5

Start Vertical Blank.
This is bit 9 of the Start Vertical Blank Register (index = 15H). This register is locked if the PR Register PR3 (0) = 1.

Bit(4:0)

Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, bits 5-7 are reserved, and bits 4-0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported.

9.7.12 Cursor Start Register Read/Write Port = 3?5, Index = 0AH

BIT	FUNCTION
7, 6	Reserved
5	Cursor Control
4 - 0	Cursor Start Scan Line

Bit(7:6)

Reserved.

Bit 5

Cursor Control.
0=Cursor on.
1=Cursor off.

Bit(4:0)

These bits specify the row scan counter value within the character box where the cursor begins. These bits contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0BH), no cursor is generated. For 6845 modes, bit 7 is reserved. Bit 5 controls the cursor operation and bits 4-0 contain the cursor start value. Bit 6 is not used.

9.7.13 Cursor End Register Read/Write Port = 3?5h, Index = 0BH

BIT	FUNCTION
7	Reserved
6, 5	Cursor Skew
4 - 0	Cursor End Scan Line

Bit 7

Reserved.

Bit(6:5)

Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the table below.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

These bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, bits 7-5 are reserved and bits 4-0 contain row value of the cursor end.

NOTE: There are three types of cursors generated, depending upon the mode i.e, EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

9.7.14 Start Address High Register Read/Write Port 3?5H, Index = 0CH

BIT	FUNCTION
7 - 0	Start Address High Byte

Bit(7:0)

Display Screen Start Address Upper Byte Bits.
Eight high order bits of the 16 bit video memory address, used for screen refresh. The low order eight bit register is at index 0DH. The PR Register PR3 bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes bits 6 & 7 are forced to 0 regardless of this register's contents, while the lower order 8 bits are at index register 0DH.

9.7.15 Start Address Low Register Read/Write Port = 3?5H, Index = 0DH

BIT	FUNCTION
7 - 0	Start Address Low Byte

Bit(7:0)

The lower order eight bits of the 16 bit video memory address in VGA or 6845 modes.

9.7.16 Cursor Location High Register Read/Write Port = 3?5h, Index = 0Eh

BIT	FUNCTION
7 - 0	Cursor Location High Byte

Bit(7:0)

Cursor Address Upper Byte Bits.
The eight higher order bits of 16 bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0FH. In VGA mode, the PR Register PR3 bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, bits 6 and 7 are reserved, while bits 5 - 0 are the high order bits of the cursor.

9.7.17 Cursor Location Low Register Read/Write Port = 3?5, Index = 0FH

BIT	FUNCTION
7 - 0	Cursor Location Low Byte

Bit(7:0)

Cursor Address Lower Byte Bits.
The lower order eight bits of the 16 bit video memory address in VGA or 6845 mode.

9.7.18 Vertical Retrace Start Register Read/Write Port = 3?5, Index=10H

BIT	FUNCTION
7 - 0	Vertical Retrace Start (Lower eight bits)

Bit(7:0)

Vertical Retrace Start Pulse Lower Eight Bits. The lower eight bits of the ten bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07H). In 6845 compatible mode, this register shows the high order six bits in positions 5 - 0 as the light pen read back value, and bits 6 an 7 are reserved. The lower order eight bits of the light pen read back register are at the index 11H. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3 (0) = 1.

9.7.19 Vertical Retrace End Register Read/Write Port = 3?5, Index = 11H

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3 - 0	Vertical Retrace End

This register is locked if the PR Register PR3(0)=1.

Bit 7

CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller index registers in the range of index 00H-07H. The line compare bit 4 in the Overflow Register (07H) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.
Selects DRAM refresh cycles per horizontal scan line.
0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.
0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4

Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by resetting (writing a 0 to) an internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

Bit(3:0)

Vertical Retrace End.
They specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan counter for "W" to the value of the Vertical Retrace Start Register. The 4 bit result is written in the Vertical Retrace End Register. In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of Light Pen Register.

9.7.20 Vertical Display Enable End Register Read/Write Port = 3?5, Index = 12H

BIT	FUNCTION
7 - 0	Vertical Display Enable End (Lower eight bits)

Bit(7:0)

Vertical Display Enable End Lower Eight Bits.
The eight lower bits of ten bit register that defines where the active display frame ends.
The programmed count is in scan lines minus 1.
Bits 8 and 9 are in the Overflow Register (index 07H) at positions 1 and 6 respectively.

9.7.21 Offset Register Read/Write Port = 3?5, Index = 13H

BIT	FUNCTION
7 - 0	Logical Line Screen width

Bit(7:0)

Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:
Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K=2 in byte mode and K=4 in word mode.

9.7.22 Underline Location Register Read/Write Port = 3?5, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4 - 0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5

Count By 4 For Double word Access
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit(4:0)

Underline Location.
These bits specify the row scan counter value within a character matrix where under line is to be displayed. Load a value 1 less than the desired scan line number.

9.7.23 Start Vertical Blank Register Read/Write Port = 3?5, Index =15H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	Start Vertical Blank (Lower eight bits)

Bit(7:0)

Start Vertical Blank Lower Eight Bits.
The lower eight bits of the ten bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). The ten bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

9.7.24 End Vertical Blank Register Read/Write Port=3?5, Index=16H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	End Vertical Blank

Bit(7:0)

Vertical Blank inactive Count.
End Vertical Blank is an 8 bit value calculated as follows:
8 Bit End Vertical Blank value =
(value of Start Vertical Blank minus 1) + (value of Vertical Blank signal width in scan lines).

9.7.25 CRT Mode Control Register Read/Write Port = 3?5, Index = 17H

This register is locked if PR Register PR3(5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.
0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word Or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by 1 bit and the MSB of the address counter appears on the LSB. See the table below.
1 = Byte address mode.

MEMORY ADDRESS	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLEWORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE:
* See bit 5, defining address wrap. This table is only applicable when PR Register PR1 bits 7 and 6 equal zero, or PR16 bit 1 equals one.
The CRT Underline Location Register (index = 14H) bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) bit 6 controls addressing. See the table below:

CRT14H	CRT17H	ADDRESS
Bit 6	Bit 6	Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.
0 = In word address mode, this bit enables bit 13 to appear at MA0, otherwise bit 0 appears on MAO.
1 = Select MA15 for odd/even mode when 256KB of video memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2
0 = Character clock increments memory address counter.
1 = Character clock divided by 2 increments the address counter.

Bit 2

Horizontal Retrace Clock Rate Select For Vertical Timing Counter.
0 = Selects horizontal retrace clock rate
1 = Selects horizontal retrace clock rate divided by 2.

Bit 1

Select Row Scan Counter.
0 = Selects row scan counter bit 1 as output at MA14 address pin.
1 = Selects bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0

6845 CRT Controller compatibility mode support for CGA operation.
0 = Row scan address bit 0 is substituted for memory address bit 13 at MA13 output pin during active display time.
1 = Enable memory address pin 13 to be output at MA13 address pin.

9.7.26 Line Compare Register Read/Write Port = 3?5, Index = 18H

BIT	FUNCTION
7 - 0	Line Compare (lower eight bits)

Bit(7:0)

Line Compare Lower Eight Bits.
Lower eight bits of the ten bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared. This creates a split screen where the lower screen does not scroll.

9.8 GRAPHICS CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

NOTE:
1. Reserved bits should be set to zero.

9.8.1 Graphics Index Register Read/Write Port = 3CE

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Graphics Address Bits

Bit(7:4)

Reserved.

Bit(3:0)

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

9.8.2 Set/Reset Register, Read/Write Port 3CF, Index = 00H

BIT	FUNCTION
7 - 4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined below:
0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE:
*The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05H) bit 1 and bit 0.

9.8.3 Enable Set/Reset Register, Read/Write Port = 3CF, Index = 01H

BIT	FUNCTION
7 - 4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Enable Set/Reset Register (Index 00H).

0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00H) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.
1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00H), and the respective memory map is written with the Set/Reset Register value.

9.8.4 Color Compare Register, Read/Write Port 3CF, Index = 02H

BIT	FUNCTION
7 - 4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Color Compare.
The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a 1 is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05H), data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

9.8.5 Data Rotate Register, Read/Write Port = 3CF, Index = 03H

BIT	FUNCTION
7 - 5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count 2 Bit 2
1	Rotate Count 1 Bit 1
0	Rotate Count 0 Bit 0

Bit(7:5)

Reserved.

Bit(4:3)

Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05H) is defined as follows.

BIT 4	BIT 3	FUNCTION
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches

Bit(2:0)

Rotate Count.
It specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05H).

9.8.6 Read Map Select Register, Read/Write Port = 3CF, Index = 04H

BIT	FUNCTION
7 - 2	Reserved
1	Map Select 1
0	Map Select 0

Bit(7:2)

Reserved.

Bit(1:0)

Map Select.
These bits select memory map in system read operations. It has no effect on color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained maps 0 & 1 or value 10b or 11b to select the chained maps 2 & 3. Map read is defined as shown below.

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

9.8.7 Graphics Mode Register, Read/Write Port = 3CF, Index = 05H

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7

Reserved.

Bit 6

256 Color Mode.
0 = Enables bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID6, VID7) are determined by bits 2 and 3 of the Color Select Register located at index = 14H within the Attribute Controller.
1 = Load video shift registers to support 256 color mode.

Bit 5

Shift Register.
Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.
0 = Map 0 - Map 3 data is placed into shift registers for normal operations.
1 = For CGA graphics mode compatibility, even numbered bits from all of the maps are shifted out of even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.
0 = normal
1 = CGA compatible odd/even system access mode. Sequential addressing as defined by bit 2 of the memory mode register (index = 04H) in the Sequencer Register. Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3

Read Mode.
0 = System reads data from memory maps selected by Read Map Select Register (index 04H). This setting will have no effect if bit 3 of the Sequencer Memory Mode Register = 1.
1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved.

Bit(1:0)

Write Mode.
The following table defines the four write modes.

BIT 0	BIT 1	WRITE MODE
0	0	Write Mode 0. If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	Write Mode 1. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	Write Mode 2. Memory maps (3:0) are filled with the 8-bit value of the corresponding CPU data bits (3:0). The 32 bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	Write Mode 3. Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

9.8.8 Miscellaneous Register, Read/Write Port = 3CF, Index = 06H

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bit(7:4)

Reserved.

Bit(3:2)

Memory Map 1, 0
Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0H-BFFF:FH	128KB
0	1	A000:0H-AFFF:FH	64KB
1	0	B000:0H-B7FF:FH	32KB
1	1	B800:0H-BFFF:FH	32KB

Bit 1

Odd/Even Mode.
0 = CPU address bit A0 is the memory address bit MA0.
1 = CPU address bit A0 is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode
This bit is programmed the same way as bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selects.
1 = Graphics mode selected.

9.8.9 Color Don't Care Register, Read/Write Port 3CF, Index = 07H

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Memory Map Color Compare Operation.

0 = Disable color compare operation.
1 = Enable color compare operation.

9.8.10 Bit Mask Register, Read/Write Port = 3CF, Index = 08H

BIT	FUNCTION
7 - 0	Bit Mask

Bit(7:0)

Bit mask operation applies simultaneously to all the four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

9.9 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CO	——	Index Register
3CO	00-0F	Palette Registers
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

NOTES:
1. Each attribute data register is written at 3C0 and register data is read from address 3C1.
2. Reserved bits should be set to zero.
3. ? " Value is controlled by Bit 0 of the Miscellaneous Output register and is programmed as shown below.

0 = B in Monochrome Modes and
1 = D in Color Modes

9.9.1 Attribute Index Register, Read/Write Port = 3C0

BIT	FUNCTION
7 - 6	Reserved
5	Palette Address Source
4 - 0	Attribute Address Bits

Bit(7:6)

Reserved.

Bit 5

Palette Address Source.
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 - 0FH).
1 = Enable internal color palette and normal video translation.

Bit(4:0)

Attribute Controller Index Register Address Bits

NOTE:
The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 3?A) clears the flip-flop and selects the Address Register, which is read thru address 3C1 and written at address 3C0. Once the Address Register has been loaded with an index, the next write operation to 3C0 will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address hex 3C0, but does not toggle for reads to address 3C1.

9.9.2 Palette Registers (00-0F Hex), Read Port 3C1/Write Port 3C0

BIT	FUNCTION
7 - 6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:6)

Reserved.

Bit(5:0)

Palette Pixel Colors.
They are defined as follows:
0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the table below.

Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

9.9.3 Attribute Mode Control Register Read Port 3C1/Write Port 3C0, Index = 10H

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7

VID5, VID4 Select
0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14H) bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6

Pixel Width
0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.
1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility
Line Compare in the CRT Controller.
0 = A Line compare will have no effect on the PEL Panning Register.
1 = Allows a successful line compare to disable the PEL Panning Register and also bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4

Reserved.

Bit 3

Background Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code.
Set this bit to zero for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes

Bit 0

Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

9.9.4 Overscan Color Register Read Port 3C1/Write Port 3C0, Index = 11H

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:0)

Overscan/Border Color.

They determine the overscan or border color.
For monochrome display, this register is set to 0.
Border colors are set as shown above.

9.9.5 Color Plane Enable Register Read Port 3C1/Write Port 3C0, Index = 12H

BIT	FUNCTION
7 - 6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3 - 0	Enable Color Plane

Bit(7:6)

Reserved.

Bit(5:4)

Video Status Control.
These bits select 2 out of 8 color outputs which can be read by the Input Status Register 1 (port = 03?A) bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit(3:0)

Color Plane Enable.
0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

9.9.6 Horizontal Pel Panning Register Read Port 3C1/Write Port 3C0, Index = 13H

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Horizontal PEL Panning

Bit(7:4)

Reserved.

Bit(3:0)

Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to 3 position pixel shift can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Character	8 dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

9.9.7 Color Select Register Read Port 3C1/Write Port 3CO, Index = 14H

BIT	FUNCTION
7 - 4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bit(7:4)

Reserved.

Bit(3:2)

Color Value MSB.
Two most two significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6

Bit(1:0)

Substituted Color Value Bits.
These bits can be substituted for VID5 an VID4 output by the Attribute Controller palette registers, to create eight bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10H).

9.10 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting PR Register PR2(6) = 1.

2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting PR Register PR2(7) = 1.

3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0 = B in Monochrome Modes
1 = D in Color Modes

9.10.1 Hercules/MDA Mode Control Register, MDA Operation Write Only Port = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode. If Bit 1=1 and Port 3BFH bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5

Enable Blink.
0 = Disable Blinking
1 = Enable Blinking

Bit 4

Reserved.

Bit 3

Video enable.
0 = Video Disable
1 = Video activated

Bit 2

Reserved.

Bit 1

Port 3BFH enable.
0 = Prevents setting of Port 3BF bit 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFh bit 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode. Should be 1.
0 = High resolution disabled.
1 = High resolution is enabled.

9.10.2 Hercules Compatibility Register Write Only Port = 3BFH

BIT	FUNCTION
7 - 2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)

Reserved.

Bit 1

Upper Memory Page Address.
Enable Mode Control Register (3B8) bit 7 selects the displayed memory page address in the graphics mode. When it is reset, bit 1 prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.
0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics.
Allows the Enable Mode Register (3B8) bit 1 to override.
0 = Alpha mode display.
1 = Graphics modes may be displayed.

9.10.3 Color CGA Operation Register, Write Only Port = 3D8

BIT	FUNCTION
7, 6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bit (7:6)

Reserved.

Bit 5

Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4

B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3

Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = Enable video signal.

Bit 2

B/W or Color Display Mode.
0= Color mode selected.
1= B/W mode selected.

Bit 1

Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = Graphics mode (320 by 200) activated.

Bit 0

(40 by 25) or (80 by 25) Text Mode Selection.
0 = 40 by 25 alpha mode enabled.
1 = 80 by 25 alpha mode activated.

9.10.4 CGA Color Select Register Write Only Port = 3D9

BIT	FUNCTION
7, 6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bit (7:6)

Reserved.

Bit 5

320 by 200 Color Set Select for the CGA 2 bits per pixel.
0 = Background, green, red, brown colors.
1 = Background, cyan, magenta, white colors.

Bit 4

Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = Enable alternate color set in graphics mode.

Bit 3

Border Intensity.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects intensified foreground color.

Bit 2

Red Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects red border color.
320 by 200 Graphics Mode.
1 = Selects red background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 1

Green Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

Bit 0

Blue Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Select blue background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

9.10.5 CRT Status Register MDAOperation, Read Only Port = 3BA

BIT	FUNCTION
7	VSYNC Inactive
6 - 4	Reserved
3	B/W Video Enabled
2 - 1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.
0 = Indicates the raster is in vertical retrace mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bit (6:4)

reserved.

Bit 3

B/W Video Status.
0 = B/W Video disabled.
1 = B/W Video enabled.

Bit 2 - Bit 1

Reserved.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

9.10.6 CRT Status Register CGA Operation, Read Only Port = 3DA

BIT	FUNCTION
7 - 4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bit (7:4)

Reserved.

Bit 3

Vertical Retrace.
0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode.

Bit 2

Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open

Bit 1

Light Pen Latch.
0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking active; Display Enable is inactive.

9.10.7 AT&T/M24 Register, Write Only Port = 3DE

This is a write only, 8-bit register located at address 3DE. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting bit 7 in PR Register 2 (PR2).

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5, 4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in color text modes.
1 = Underline attribute selects white underlined foreground.

Bit (5:4)

Reserved.

Bit 3

Page Select.
Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B800:0H (16 KB length).
1 = Display memory address starts at BC00:0H (16 KB length).

Bit 2

Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or Non-IBM Graphics Mode. 400 line mode. A 400 line monitor is required for this mode.
0 = 200 line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400 line graphics.

9.11 WD90C00 PR REGISTERS

NAME	DESIGNATION	I/0 LOCATION
Address Offset A	PR0A(6:0)	3CF.09
Alternate Address Offset B	PR0B(6:0)	3CF.0A
Memory Size	PR1(7:0)	3CF.0B
Video Select	PR2(7:0)	3CF.0C
CRT Control	PR3(7:0)	3CF.0D
Video Control	PR4(7:0)	3CF.0E
Unlock PRO-PR4	PR5(7:0)	3CF.0F
Unlock PR11 - PR17	PR10(7:0)	3?5.29
EGA Switches	PR11(7:0)	3?5.2A
Scratch Pad	PR12(7:0)	3?5.2B
Interlace H/2 Start	PR13(7:0)	3?5.2C
Interlace H/2 End	PR14(7:0)	3?5.2D
Miscellaneous Control 1	PR15(7:0)	3?5.2E
Miscellaneous Control 2	PR16(7:0)	3?5.2F
Miscellaneous Control 3	PR17(0)	3?5.30
Reserved	---	3?5.31-3?5.3F

The WD90C00 has additional features that enhance the performance and functions of the Western Digital Imaging PVGA1A, introduced earlier, and the basic VGA subsystem. To accomplish this, the WD90C00 architecture is optimized with additional I/O registers.

The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

NOTES:

1. The designation 3?5 means that the register is mapped into either 3B5 in monochrome mode or 3D5 in color modes.

2. PR register notation - XXX.YY where XXX is the data port address and YY is the register index e.g. 3CF.0F implies 0F--3CEH (Select Index register) followed by (Data byte) -- 3CF (Data Port)

Registers PR0 through PR4 and PR11 through PR17 are normally locked. They are write protected at power-up by the hardware reset. In order to load those registers, the appropriate unlock register PR5 or PR10 must be loaded first with binary XXXXX101; a register remains unlocked until any other value is written to the unlocked register. Registers PR0 through PR5 are readable only if PR4 bit 1 = 0. Registers PR10 through PR17 are read protected at power up by hardware reset. In order to read registers PR10 through PR17 load PR10 with 1XXX0XXX. The register remains readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them would show data to be FFH. Setting PR4 bit 1 to 1 does not read protect registers PR10 through PR17. All PR registers are set to 0 at power on reset except where noted.

9.11.1 Address Offset Registers PR0A & PR0B

PR0A - Address Offset Register A
Read/Write Port = 3CF, Index = 09H

BIT	FUNCTION
7	Reserved
6 - 0	Primary Address Offset Bits

PR0B - Address Offset Register B
Read/Write Port = 3CF, Index = 0AH

BIT	FUNCTION
7	Reserved
6 - 0	Alternate Address Offset Bits

The WD90C00 can control up to one megabyte of video RAM. However, the memory map for IBM PC and compatible product assigns 128 Kbytes of the available 1Mbyte total system space to the video controller. Therefore, the video memory space starts at A000:0H and ends at BFFF:FH. To allow a second video card to co-exist, this space is further limited to a 64 Kbyte video memory partition.

The WD90C00 has two offset registers that help address 512 Kbytes of linear addressed memory. These are PR0A and PR0B. These registers contain an offset which gets added to the system address when accessing more than 64 Kbytes of video memory. Address offset register PR0A is the primary address offset register and is always enabled. Alternatively, Address offset register PR0B is enabled only if PR1 bit 3 is set to 1. PR0A and PR0B provide a seven bit offset that is added to address bits A (18:12) of the system address to form a 20-bit address. It can be thought of as being like segment register DS and ES of the 8088/80X86 architecture. PR0A and PR0B will then provide 4 Kbyte segments.

When PR0B is enabled by setting PR1 bit 3 = 1, PR address offset registers, in a 64K VGA address space (as defined by Graphics Miscellaneous Register Bits 3 and 2), PR0A and Alternate Offset Address register (PR0B) may be used to access two 32 Kbyte video RAM windows. PR0A window is mapped from A800:0H-AFFF:FH while PR0B is mapped from A000:0H-A7FF:FH.

When there is a 128 Kbyte address space (as defined by Graphics Miscellaneous Register bits 3 and 2), PR0A is mapped from B000:0H-BFFF:FH while PR0B is mapped from A000:0H-AFFF:FH when the Alternate Offset register is enabled.

9.11.2 PR1 - Memory Size, Read/write Port = 3CF, Index = 0BH

BIT	FUNCTION
7, 6	Memory Size Select
5, 4	Memory Map select
3	Enable Alternate Address Offset Register PR0B
2	16-Bit Video Memory
1	16-Bit BIOS ROM
0	BIOS ROM Map Out

This register is 8 bits wide. Bits PR1 (1:0) are latched internally at power on reset from the corresponding memory data bus pins MD(1:0), using either pull-up or pull-down external resistors. Pull-up resistors on MD(1:0) cause PR1(1:0) bits to be latched low.

Bits 7, 6

Memory Size.

BIT7	BIT6	PR16(1)	MEMORY SIZE	MAPPING
0	0	0	256 KB STANDARD VGA	VGA*
0	1	0	256 KB WD90C00 VGA	PVGA**
1	0	0	512 KB WD90C00 VGA	PVGA
1	1	0	1024 KB WD90C00 VGA	PVGA
X	X	1	ANY OF THE ABOVE	VGA*

NOTE:
* Only 64 Kbytes are accessible for chained 4 packed pixel mode.
** WDI extended modes can fully utilize up to 256 Kbytes.

According to the VGA video memory organization, 256 KB of the available memory space is divided into four 64 KB maps (0-3), each defining bit planes (0-3). In mode 13, the four bit planes are chained to form one large bit plane. The starting address of the 256 KB video memory buffer can be configured to match other video adapters, and/or, application programs. For example, 256 KB video display buffer with 128 KB or 64 KB segments can start at address A000:0 (Hex) while 32KB segments start at address B000:0 (Hex) or B800:0 (Hex). WD90C00 enhances memory size capability when bits 6 and 7 are programmed to extend video buffer size to 512 KB or 1024 KB. The DRAM organizations supported by the WD90C00 and its associated video space table are shown below.

DRAMS	MA8 PIN	VIDEO SPACE	MEMORY PLANES
64Kx4	N/U	256 KB	Four (64KB Per Plane)
64Kx4	BANK SELECT	512 KB	Four (128KB Per Plane)
256Kx4	DRAM PIN A8	1024KB	Four (256KB Per Plane)

When video memory size is 512 KB, and 64Kx4 DRAMs are used two banks of 64 KB form 128 KB per plane. MA8 provides the bank selection using an external multiplexer to access the appropriate bank in a plane by multiplexing the $\overline{CAS10}$ and $\overline{CAS32}$ signals. Four planes form the desired 512 KB video memory space. For 1024 KB video memory size, MA8 is directly connected to the A8 address pin of the 256Kx4 DRAMS, and two DRAMS form a 256 KB per plane. Four planes make the desired 1024 KB video memory space.

PR1 bits 7 and 6 must be set to reflect the amount of memory installed. These bits in conjunction with PR16(1) also select the way memory is mapped into the system address space. If PR16(1) is set to 1, the memory mapping is same as IBM VGA regardless of PR1 (6) and PR1(7).

RAM ADDRESSING:

PR1(7) **PR1(6)**
0 0 256K TOTAL;64K/PLANE; IBM VGA MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(0)	A(0)	CA(0)	A(16) or XRN(5)	CA(15) or CA(13)	A(14)	CA(12)

RAM ADDRESSING:

PR1(7) **PR1(6)**
0 1 256K TOTAL;64K/PLANE; WD90C00 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

RAM ADDRESSING:

PR1(7) **PR1(6)**
1 0 512K TOTAL;128KB/PLANE; WD90C00 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	0	0	0	0	0	0
MA(16) *	A(16)*	CA(16)*	A(17)*	CA(16)*	A(18)*	CA(16)*
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

NOTE: "*" Controls CAS external to WD90C00

RAM ADDRESSING:

PR1(7) **PR1(6)**
1 1 1024K TOTAL IN FOUR PLANES;256K/PLANE;
WD90C00 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)
MA(16)	A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)
MA(0)	A(0)	CA(0)	A(18)	CA(17)	A(18)	CA(16)

NOTES:
1. A(19:0) are WD90C00 internally modified system Addresses.
2. CA(17:0) are CRT Controller Character Address Counter Bits.
3. XRN(5) is Miscellaneous Output Register 3C2H, inverted bit 5. This bit selects the displayed page in chained modes. XRN(5) is selected as MA(0) if Graphics Register 6 bit 3 or bit 2 = 1.
4. CA(13) is selected as MA(0) if CRTC Mode Register 17 bit 5 = 0.

Bit5	Bit4	MEMORY MAP
0	0	VGA Mapping in 64 KB space - A000:0H to BFFF:FH Address Range
0	1	First 256 KB in 1MB space - 0000:0H to 3FFF:FH Address Range
1	0	First 512 KB in 1MB space - 0000:0H to 7FFF:FH Address Range
1	1	First 1024 KB in greater or equal to 1 MB space - 0000:0H to FFFF:FH Address Range

Bits 5 and 4 can be used in conjunction with external control of EMEM to map video memory decode above the 1 Mbyte address space.

Bit 3

Enable Alternate Address Offset Register PR0B

Bit 2

Enable 16-bit bus for Video Memory
When set to 1, $\overline{DS16}$ will be active low in text modes and packed pixel modes such as mode 13h. Planar graphics modes will always have $\overline{DS16}$ be inactive.

Bit 1

This bit will directly reflect signal pin $\overline{ROM16}$ in AT mode or $\overline{CDDS16}$ in MCA mode.
When set to 1, the BIOS ROM has 16 bits data path.

If set to 0, the BIOS ROM data path is 8 bits wide. A pull-up on MD (1) sets this bit to 0 at power on reset. $\overline{ROM16}$ will have the value of 0 when this bit is set.

Bit 0

If set to 1 the BIOS ROM is mapped out. Pull-up resistor latches 0 after power up. A pull-up on MD(0) sets this bit to 0 at power on reset.

9.11.3 PR2-Video Select Register, Read/Write Port = 3CF, Index = 0CH

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4, 3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7

Enable AT&T/M24 Register & mode

Bit 6

0: VGA or EGA mode
1: Non-VGA (6845) mode

Bit 5

Character Map Select. The following functions are overridden by setting PR15(2). This bit in conjunction with PR2(2) and bit 4 of the attribute code, enables character maps from planes 2 or 3 to be selected per the table below:

PR2(5)	PR2(2)	ATT(4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE:
Setting PR15(2) = 1 i.e. selecting page mode addressing overrides plane selected table shown above.

Bit(4:3)

Character clock period control

0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132 character mode)
1	0	9 dots
1	1	10 dots

Selecting 10 dots per character modifies the function of the horizontal PEL Panning register (3C0.13). Pixel panning in the 10 dot-character modes is obtained by storing the following values into the horizontal PEL Panning register.

PEL PANNING REGISTER VALUE	PELS SHIFTED LEFT
09	0
08	1
00	2
01	3
02	4
03	5
04	6
05	7
06	8
07	9

NOTE:
The character clock period control functions have no effect in graphics modes.

Bit 2

Underline and character map select. Setting this bit to 1 enables underline for all odd values of attribute codes, e.g. Programming 1 gives blue underline. It overrides the background color function of the attribute code bit 3, which is forced to 0. Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1

This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) is set to 1. When CNF(3) is set to 0, it locks the internal video clock select multiplexer.

Bit 0

Forces horizontal sync timing clock of the CRTC to VCLK.
Uses VCLK when sequencer register 1 bit 3 is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

9.11.4 PR3 - CRT Lock Control Register Read/Write Port=3CF, Index = 0H

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

9.11.5 WD90C00 CRT Controller Register Locking

Register locking is controlled by 4 bits. They are PR3 (5,1,0) and 3?5.11(7) (i.e. IBM Vertical Retrace End Register bit 7 controlled by index register 11). When bit 7 is 1, CRT controller registers (R0-7) are write protected per VGA definition. For more information on the five groups, and their locking schemes, refer to the sections below.

- **Group 0**

These registers are locked if PR3(5)=1 OR 3?5.11(7)=1
CRT controller register 00 --Horizontal Total Characters per scan
CRT controller register 01 --Horizontal Display Enable End
CRT controller register 02 --Start Horizontal Blanking
CRT controller register 03 --End Horizontal Blanking
CRT controller register 04 --Start Horizontal Retrace
CRT controller register 05 --End Horizontal Retrace

- **Group 1**

These registers are locked if PR3(1)=0 AND 3?5.11(7)=1
CRT controller register 07(Bit6) - Vert. Display Enable End bit 9
CRT controller register 07(Bit1) - Vert. Display Enable End bit 8

- **Group 2**

These registers are locked if PR3(0)=1 OR 3?5.11(7)=1
CRT controller register 06 --- Vertical Total
CRT controller register 07(Bit7) ---Vertical Retrace Start bit 9
CRT controller register 07(Bit5) ---Vertical Total bit 9
CRT controller register 07(Bit3) ---Start Vertical Blank bit 8
CRT controller register 07(Bit2) ---Vertical Retrace Start bit 8
CRT controller register 07(Bit0) ---Vertical Total bit 8

- **Group 3**

These registers are locked if PR3(0)=1
CRT controller register 09(Bit5) ---Start Vertical Blank bit 9
CRT controller register 10 ---Vertical Retrace Start
CRT controller register 11 [Bits(3:0)] ---Vertical Retrace End
CRT controller register 15 ---Start Vertical Blanking
CRT controller register 16 ---End Vertical Blanking

- **Group 4**

This register is locked if PR3(5)=1
CRTC mode control register 17(Bit2) ---Selects divide by two vertical timing

Bit7

Lock VSYNC polarity, as programmed in 3C2 bit 7

Bit 6

Lock HSYNC polarity, as programmed in 3C2 bit 6

Bit 5

Lock horizontal timing.
Locks CRTC registers of Group 0 and 4.
Prevents attempt by applications software to unlock Group 0 registers by setting 3?5.11 bit 7=0

Bit 4

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 9 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (17).

Bit 3

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (16).

Bit 2

Cursor start, stop, preset row scan, and maximum scan line address registers values multiplied by two.

Bit 1

1 = Prevents attempt by applications software to lock registers of Group 1 by its setting 3?5.11 bit 7=1.

Bit 0

Lock vertical timing. 1 = Locks CRTC registers of Groups 2 and 3. Overrides attempt by applications software to unlock Group 2 registers by its setting 3?5.11 bit 7=0.

9.11.6 PR4- Video Control Register Read/Write Port=3CF, Index = 0EH

The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAMDAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLNK}}$ / Display Enable
6	PCLK=VCLK
5	Tri-state Video Outputs
4	Tri-state Memory Control Outputs
3	Override CGA Enable Video bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Ext 256 color Shift Register control

Bit 7

This bit controls the output signal $\overline{\text{BLNK}}$. Normally in the VGA mode, $\overline{\text{BLNK}}$ is used by the external video DAC to generate blanking. If this bit = 1, the $\overline{\text{BLNK}}$ output supplies a display enable signal. A choice of two types of display enable timings can be selected, and is determined by PR15(1).

Bit 6

Select PCLK equal to VCLK.
0=PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1=PCLK is always the non-inverted VCLK input clock.

Bit 5

Tri-state the outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLNK}}$.

Bit 4

Tri-state the memory control outputs. The memory address bus MA(8:0), and all ten DRAM control signals are tri-stated when this bit is set to 1.

Bit 3

Overrides the CGA "enable video" bit 3 of mode register 3D8, only in 80 x 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2

Lock Internal palette and overscan registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode. It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3CO/3C1 change to write-only mode if the EGA compatibility bit is set. In addition to selecting EGA compatibility bit, setting this bit to 1 disables reading PR0-PR5. In VGA mode (PR(4) bit 1 is zero) 3C0 register is read/write while 3C1 register is read only, per the Attribute Controller registers definitions.

Bit 0

Shift register control. It configures the video shift registers for extended 256-color mode.

9.11.7 PR5 - General Purpose Status Bits Read/Write Port=3CF, Index = 0FH

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PRO-PR4 Unlock
1	PRO-PR4 Unlock
0	PRO-PR4 Unlock

Bits (2:0) are READ/WRITE bits and cleared to 0 by reset. They provide lock or unlock capability for PR registers PR0 through PR4 like the PVGA1A. The PR0 - PR4 registers are unlocked when "X5Hex" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register bits 4 through 8. Setting PR(4) bit 1 to 1, read protects registers PR0 - PR5.

Bit 7 CNF(7) [READ ONLY]
Bit 6 CNF(6) [READ ONLY]
Bit 5 CNF(5) [READ ONLY]
Bit 4 CNF(4) [READ ONLY]
Bit 3 CNF(8) [READ ONLY]

Bits (2:0)

READ/WRITE bits and cleared to 0 by reset. They control writing to PR registers PR0-PR4 as follows:

2 1 0	PR0-PR4
0 X X	Write protected
X 1 X	Write protected
X X 0	Write protected

9.11.8 PR10 Unlock PR11-PR17 Read/Write Port = 3?5, Index = 29

This register is READ/WRITE and cleared to 0 by reset. PR10 can be loaded if it contains XXXXX101, and can only be read if it has 1XXX0XXX. Bits (7,3), Bits(6:4), and Bits (2:0) control access to PR registers PR10-PR17. Bits 7 and 3 enable register read operation for PR10 - PR17. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 - PR17.

BIT	FUNCTION
7	PR10-PR17 - Read Enable Bit 1
6 - 4	PR10(6:4) - Scratch Pad
3	PR10-PR17 - Read Enable Bit 0
2 - 0	PR11-PR17 - Write Enable

BIT7	BIT3	PR10-PR17
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

BIT2	BIT1	BIT0	PR11-PR17
0	X	X	Write protected
X	1	X	Write protected
X	X	0	Write protected
1	0	1	Write Enabled

BIT6	BIT5	BIT4	PR10(6:4)
0	X	X	Scratch pad
X	1	X	Scratch pad
X	X	0	Scratch pad
1	0	1	Reserved for manufacturing test.

9.11.9 PR11 EGA Switches Read/Write Port = 3?5, Index = 2a

The EGA switch configuration details are stored in the PR11 register bits.

BIT	FUNCTION
7	EGASW4
6	EGASW3
5	EGASW2
4	EGASW1
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4)

EGA CONFIGURATION SWITCHES SW4-SW1. These bits are READ/WRITE and latched internally at power-on-reset from corresponding memory data bus pins MD(15:12), provided with either pull-up or pull-down external resistors. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. These bits can be read as bit 4 of port 3C2 if the EGA COMPATIBILITY BIT [PR4(1)] has been set to 1. Selection of the bit to be read is determined by bits 3 & 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE 3C2 bit 3	3C2 bit 2	READ 3C2 bit 4
0	0	PR11(7) [=EGA SW4]
0	1	PR11(6) [=EGA SW3]
1	0	PR11(5) [=EGA SW2]
1	1	PR11(4) [=EGA SW1]

PR11 Bits 3 through 0 are READ/WRITE and cleared to 0 at power on reset.

Bit 3

Select EGA Emulation on a PS/2 (VGA-compatible, analog) display.

Bit 2

Lock Clock Select. This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

Bit 1

Lock Graphics Controller/Sequencer screen control. Setting PR11(1) to 1 prevents modification of the following bits in the Graphics controller as well as the Sequencer:

Graphics controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by these graphics controller and sequencer bits are locked by setting PR11 bit 1 to 1, they appear unlocked to the system processor during read operation.

Bit 0

Lock 8/9 dots. Setting this bit to 1 prevents modification of clocking mode sequencer register 3C5.01 bit 0. Although 8 or 9 character timing is locked by setting PR11 bit 0 to 1, the 3C5.01 bit 0 appears unlocked to the system processor during reads.

9.11.10 PR12 Scratch Pad Read/Write Port = 3?5, Index = 2b

BIT	FUNCTION
7 - 0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power up.

9.11.11 PR13 Interlace H/2 Start Read/Write Port = 3?5, Index = 2C

BIT	FUNCTION
7 - 0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1. All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00):

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE:
In the above expression, HRD = Horizontal Retrace Delay, determined by bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

9.11.12 PR14 Interlace H/2 End Read/Write Port = 3?5, Index = 2d

Bits 4 through 0 are unaffected by hardware reset and undefined at power up. Bits 7 through 5 are cleared to 0 by reset.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4 - 0	Interlaced H/2 Start

Bit 7

Enable IRQ. This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to 0. This bit should not be set to 1 in MICRO CHANNEL operation.

Bit 6

Vertical double scan. This bit should be set to 1 when emulating EGA on PS/2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed line counter and row scan counter to be clocked by divide-by-two horizontal timing if vertical sync polarity (3C2 Bit 7=0) is programmed to be positive. Therefore, the relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is:

N=2(n+1)

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5

Interlaced mode.
Setting this bit to 1 selects interlaced mode. The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000.
Line compare and double scan are not supported.

Bits (4:0)

Interlaced H/2 end bits (4:0). Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

9.11.13 PR15 Miscellaneous Control 1 Read/Write Port = 3?5, Index = 2e

BIT	FUNCTION
7	Read 46E8 Enable
6	Low VCLK
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable reading port 46E8H. This bit is functional only if AT BUS architecture [CNF(2)=1] is selected. Setting this bit to 1 enables I/O port 46E8H to be read, regardless of the state of its own bits 3 and 4 and of port 102 bit 0 (sleep bit). Only bits (4:0) of port 46E8H are readable; bits (7:5) are 0.

Bit 6

Low VCLK. Setting this bit to 1 adjusts the memory timing to allow use of a video clock (VCLK) frequency which is much lower than the memory clock (MCLK) frequency. This bit should be set to 1 if the following expression is satisfied:

(MCLK in MHZ) / (VCLK in MHZ)>2

Bit 5

Latched VCLK1 and VCLK2. This bit is used only if CNF(3) = 1 which configures the VCLK1 and VCLK2 pins as outputs. Setting This bit to 1 causes outputs VCLK1 and VCLK2 to equal bits 2 and 3 of I/O write register (Miscellaneous output register) at 3C2H respectively.

Bit 4

Select MCLK as video clock. Setting this bit to 1 causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.

Bit 3

Interlaced Compatibility. This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to 1 if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to 1 causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of leading edge, as generated for VGA timing.
Setting this bit to 1 also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing. Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory by 30-40%. Set this bit to 1 if 132 character mode timing is selected (see description of PR2). Setting this bit to 1 in any alpha mode overrides the character map select functions of PR2(2) and PR2(5). When this bit is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight, 8K memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by bits (2:0) of this register while the map selection is determined by the bits (4:3). A pair of adjacent 8K character maps in planes 2 and 3, (adjacent in the sense that they have the same addressing) may be selected by bit 3 of the attribute code.
The Character attribute bit 3, in conjunction with bits 3 and 4 of the Character Map Select register (3C5.03), determine a character map from either Plane 2 or Plane 3 as shown by the table below.

3C5.03 BIT4	3C5.03 BIT 3	ATT BIT3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

Note:
The above Character Map Select functions override the functions override the functions of PR2(5) and PR2(2).
This bit must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select. This bit is used to select between two types of Display Enable timings available at output pin $\overline{BLNK}$ if PR4(7)=1. If PR4(7)=0, this bit has no effect.

0=$\overline{BLNK}$ supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = $\overline{BLNK}$ supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable border. Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

9.11.14 PR16 Miscellaneous Control 2 Read/Write Port = 3?5, Index = 2FH

BIT	FUNCTION
7	External reg. 46E8H lock
6	CRTC Address count Width bit 1
5	CRTC Address Count Width bit 0
4	CRTC Address Counter Offset bit 1
3	CRTC Address Counter Offset bit 0
2	Enable Odd/Even Page bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit (7)

Lock External 46E8H register.

Setting this bit to 1 causes $\overline{EBROM}$ output to be forced high (Inactive) during I/O writes to port 46E8H. This bit has no effect on loading the internal port 46E8H.

Bit (6:5)

CRTC Address Counter Width.

Power on reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512KB or 1024KB of video memory in which CRT controller is limited to only 64K or 128K locations. Bit PR16(6) should be set 1 to ensure VGA and EGA compatible operation of the address counter, limited to 64 K locations. The following table shows details:

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256KB
0	1	128K
1	X	64K

Bit (4:3)

CRTC Address Counter Offset
Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively, and the 2-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2

Enable Page Bit for Odd/Even
This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory, and setting 3C5.04(3) to 0 to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size bits PR1(7:6).

Bit 1

VGA Memory Mapping
Setting this bit to 1, selects 256KB IBM VGA Mapping, regardless of the Memory Size bits PR1(7:6).

Bit 0

Lock RAMDAC write strobe (3C6H - 3C9H)
Programming this bit to 1 causes output $\overline{WPLT}$ to be forced to 1 disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C00 is also protected from the modification but may still be read at the port 3C7h. For normal operation, program this bit to 0.

9.11.15 PR17 Miscellaneous Control 3 Read/Write Port = 3?5, Index = 30H

BIT	FUNCTION
7 - 1	Reserved
0	Map out 2K of BIOS ROM

Bit (7:1)

Reserved.

Bit (0)

Map out 2K of BIOS ROM.
Setting this bit to 1 disables access of the BIOS ROM in the system address range C600:0H - C67F:FH.
Power on reset sets this bit to 1. Clearing this bit to 0, enables access of all 32K addresses of the BIOS ROM from C000:0H - C7FF:FH.

9.12 INTERNAL I/O PORTS

9.12.1 AT Mode Write Only Port 46E8H (Also at Port 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7 - 5	Unused
4	Setup
3	Enable I/O & Memory
2 - 0	External BIOS ROM Page Select

Bit(7:5)

Unused

Bit 4

Setup
Puts WD90C00 into setup mode where only I/O port 102H is accessible.

Bit 3

Enable I/O and Memory Accesses. Does not affect Port 46E8H and 102H.

Bit(2:0)

Unused Internally
Used for BIOS ROM Page select. On I/O accesses to 46E8H, EBROMN becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits to define 4K pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0.

9.12.2 Setup Mode Video Enable (AT and Micro Channel Modes) Read/Write Port = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7 - 1	Unused
0	Wakeup VGA

Bit(7:1)

Unused

Bit 0

Wakeup VGA for I/O and Memory Accesses. Only lower 3 address bits are decoded for this port and WD90C00 must be in SETUP mode. VGA Enable Sleep bit or Programmable Option Select (POS) register 102H bit 0 is used to awaken the WD90C00 after power on in the MCA and AT mode. To enter the set up mode in AT bus applications, bit 4 of the partially decoded internal I/O port 46E8H is set to 1 before accessing the I/O port 102H. In MCA mode, when the VGASETUP ($\overline{EIO}$) signal pin is active low, the WD90C00 is in setup mode and port 102H can be accessed.

9.13 VIDEO RAMDAC PORTS

The Video RAMDAC is implemented externally to the WD90C00. However, the $\overline{WPLT}$ and $\overline{RPLT}$ signals required by the RAMDAC are provided by the WD90C00. Setting PR(16) bit 0 to a 1 forces $\overline{WPLT}$ to a high level disabling I/O writes to the RAMDAC. Normally, the $\overline{WPLT}$ and $\overline{RPLT}$ signals to the RAMDAC are generated when the following I/O ports are written to or read from.

DAC ADDRESS	DAC OPERATION	DETAILS
3C8H	PEL address port (write)	Read/write port
3C7H	PEL address port (read)	Write only port
*3C7H	*DAC state (read only)	*If bits 0/1 =1, DAC in read operation. When bits 0/1=0,DAC in write operation. Bits 2-7 are reserved.
3C6H	PEL mask (read/write)	Read/write
3C9H	PEL data register (read/write)	Three successive read/write bytes.

* NOTE: This port is internal to WD90C00.

9.13.1 WD90C00 Configuration Bits CNF (8:2) Non-Read/Non-Write Hardware Port

BIT	FUNCTION
8	Display Status
7 - 4	General Purpose Status
3	Video Clock Source Control
2	Bus Architecture Select

Bits CNF (3:2) are latched internally at power on reset from the corresponding memory data bus pins MD (3:2) while CNF (8) is latched from MD (11). They are connected to the external pull-up or pull-down resistors. Pull-up resistor sets MD(3:2) to logic 1 while pull down resistor sets MD(11) to logic 1. Note, that the configuration bits (3:2) are not readable since they are latched after power up. However, the configuration register bits (8:4) are readable after power up as PR5 bits (7:3). They appear as general purpose read only status bits in the PR5 register.

CNF (8)

ANALOG/TTL DISPLAY STATUS BIT
Bit CNF(8) is latched internally at power-on-reset from memory data bus pin MD(11), provided with either a pull-up or pull-down external resistor. Pulling up MD(11) causes CNF(8) to be latched Low. This bit controls no internal functions and is read only as bit 3 of PR5 (3CF.0F). Also, CNF(8) is unaffected by writing to PR5 (3CF.0F).

0 = Analog (VGA - compatible) display is attached
1 = TTL (EGA-compatible) display is attached.

CNF (7:4)

GENERAL PURPOSE STATUS BITS
Bits CNF (7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD (7:4), provided with either pull-up or pull-down external resistors. These are read only bits at PR5 (3CF.0F) positions (7:4). These bits are unaffected by writing to PR5(3CF.0F). Pulling up MD (7:4) causes CNF (7:4) to be latched low.

CNF (3)

VIDEO CLOCK SOURCE CONTROL
This bit cannot be written or read as I/O port pulling up MD (3) causes CNF(3) to be latched high. It configures WD90C00 pins VCLK1 and VCLK2 as inputs or outputs.

0=For inputs.
1=For outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of dot clock is by an internal multiplexer. When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip, during I/O writes to port 3C2H. This load pulse may be inhibited by setting PR11(2)=1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. Also, VCLK1 and VCLK2 outputs equal to bits 2 and 3 of the Miscellaneous output register at 3C2H respectively when PR15 bit 5 is set to 1.

CNF (2)

Bus Architecture Select
This bit cannot be written or read as I/O. Pulling up MD(2) causes CNF(2) to be latched high.

0 =Micro Channel architecture

1=AT BUS architecture

9.14 EXTERNAL I/O PORT CONSIDERATIONS

9.14.1 Video Subsystem Enable Register Micro Channel Only Read/Write Port 3C3H

BIT	FUNCTION
7 - 1	Unused
0	Video Subsystem Enable

Bit(7:1)

Reserved

Bit 0

When this bit is set to 1, the I/O and memory address decoding for the video subsystem are enabled. When set to 0, this bit disables the video I/O and memroy address decoding. Accessing this register does not affect addressing port 102h POS register.

The WDI WD90C00 does not internally support the 3C3H port in either the AT or Micro Channel mode. In the Micro Channel mode, bit D0 of this port is used to enable the video subsystem per IBM definition. If D0 is 1, the video I/O and memory address decoding is enabled. When D0 is 0, the video I/O and memory address is disabled. This port is set to enable (logic 1) after power on. It is not affected by the VGA sleep bit (I/O port 102H bit O) of the Programmable Option Select (POS). When, WD90C00 is used in the Micro Channel bus designs, the read or write I/O port at 3C3H is implemented externally.

APPENDIX

A.1 EGA MODE

For the register definitions that have not changed from the VGA modes, refer to the VGA description. Only the differences between the VGA and EGA registers are briefly described in this section. Also, refer to the prior section for VGA mode details. Not Used bits should be set to 0 unless otherwise noted.

A general procedure to enter EGA mode of operation is described. The actual software implementation details are not covered in this procedure. These steps are briefly defined to outline the EGA mode entry.

1. Load Configuration register bit 8. Logic 0 for VGA compatible PS/2 display or Logic 1 for EGA compatible TTL monitor by appropriate pull-up or pull-down resistor on MD(11). (Pull-up resistor on MD11 causes CNF(8) to be latched with logic 0, for Analog PS/2 compatible display). This is status for the BIOS or application to signify monitor type attached.
2. Unlock all the PR registers.
3. Program PR2(6) to 0 for EGA mode.
4. Set PR4 bit 1 to logic 1 for EGA compatibility.
5. Load PR11(7:4) with EGA Configuration switches by using pull-up or pull-down resistors on pins MD(15:12). (Pull-up resistor causes logic 1 to be latched after power on reset.)
6. The EGA switch setting may then be read from PR11(7:4) at I/O port 3C2 bit 4.
7. If EGA is to be emulated on the IBM PS/2 type analog display, follow the suggested steps listed below:

a) Initialize all the registers.
b) Lock CRT controller registers.
c) Force Clock Control rate of the CRT controller.
d) Set EGA emulation mode by programming:
PR11(3)=1; Set EGA emulation on PS/2 type display
PR14(6)=1; Vertical double scan
PR11(2)=1; Lock clock select
PR11(0)=1; Lock 8/9 dot timing.
PR14(7)=1; Enable IRQ (optional)
e) Lock the PR registers PRO-PR5 and PR10-PR17.
f) Read protect PR registers.

8. When EGA is required on a TTL monitor, the suggested steps are:

a) Initialize all the registers.
b) Set EGA TTL mode by programming:
PR11(3)=0;EGA TTL
PR14(7)=1;Enable IRQ
PR15(6)=1;Set Low Clock
PR14(7)=1;Enable IRQ
c) Lock PR registers PRO-PR5 and PR10-PR17
d) Read protect PR registers.

For more details on the PR registers, refer to the PR registers section. The EGA register summary shown on the next page highlights all the EGA mode registers.

A1.1 EGA Registers Summary

REGISTERS	EGA	I/O PORT
General Registers:		
Miscellaneous Output Reg	WO	3C2
Input Status Reg 0	RO	3C2
Input Status Reg 1	RO	3?A
Feature Control Reg	WO	3?A
Sequencer Registers:		
Sequencer Index Reg	WO	3C4
Sequencer Data Reg	WO	3C5
CRT Controller Registers:		
Index Reg	WO	3?4
CRT Controller Data Reg Except the following:	WO	3?5
Start Address High (Index=0C)	RW	3?5
Start Address Low (Index=0D)	RW	3?5
Cursor Location High (Index=0E)	RW	3?5
Cursor Location Low (Index=0F)	RW	3?5
Light Pen High, (Index=10)	R	3?5
Light Pen Low, (Index=11)	R	3?5
Graphics Controller Registers:		
Index Reg	WO	3CE
Other Graphics Reg	WO	3CF
Attribute Controller Registers:		
Index Reg	WO	3C0*
Attribute Controller Data Reg	WO	3C0*

NOTES:
1. RO = Read Only, WO = Write Only, and RW = Read/Write.
2. All Register addresses are in hex.
3. "?"= "B" in Monochrome modes or "D" in Color modes.
4. "*" = Identical responses from I/O ports 3C0 and 3C1.

A.2 GENERAL REGISTERS

Only the general registers and the bit definitions that differ between the VGA and EGA are addressed. Their EGA mode bit definitions are provided.

A.2.1 Miscellaneous Output Register (Write Port 3C2)

Bits (7:5)

EGA: Same as Miscellaneous Output Register Bits (7:5) definition in the VGA section.

Bit 4

Not used.

Bits (3:2)

EGA:

BIT 3	BIT 2	DESCRIPTION
0	0	14.318 Mhz clock (VCLK0) is selected.
0	1	16.257 Mhz clock (VCLK1) is selected if Configuration Register Bit 3 is 0.
1	0	External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is 0.
1	1	Not Used. VCLK2 selected if Configuration Register Bit 3 is 0

Bit (0)

EGA: Identical to Miscellaneous Output Register Bit 0 definition in the VGA section.

A.2.2 Input Status Register 0 (Read Port 3C2)

Bit 7

EGA: Same as input Status Register 0, Bit 7 definition in the VGA section.

Bits (6:5)

EGA: Not used

Bit 4

EGA: The four configuration switches' information stored in PR11 can be read at this bit if PR4(1) has been set to 1.

Bits (3:0)

EGA: Not used = 1

A.2.3 Input Status Register 1 (READ PORT 3?A)

Bit (7)

EGA: Not used

Bit 6

EGA: Not used = 1

Bits (5:3)

EGA: Identical to Input Status Register 1 Bits (5:3) definition in the VGA section.

Bit 2

EGA: Not used = 1

Bit 1

EGA: Unused

Bit (0)

EGA:
Same as Input Status Register 1 Bit 0 definition in the VGA Section.

A.2.4 Feature Control Register (Write Port 3?A)

Bits (7:0)
EGA: Not used

A.3 SEQUENCER REGISTERS INDEX PORT = 3C4, PORT 3C5

A.3.1 Clocking Mode register (Index = 01)

Bits (7:4)
EGA: Not Used

Bits (3,2)
EGA: Same as Clocking Mode Register Bits (3,2) definition in the VGA section.

Bit 1
EGA: Set to zero

Bit (0)
EGA: Identical to Clocking Mode Register Bit 0 definition in the VGA section.

A.3.2 Character Map Select Register (Index 03)

Bits (7:4)
EGA: Not Used

Bits (3:2)
EGA: Character Map Select A

BIT 3	BIT 2	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

Bits (1:0)
EGA: Character Map Select B

BIT 1	BIT 0	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

A.3.3 Memory Mode Register (Index = 04)

Bits (7:3)
EGA: Not Used

Bits (2:1)
EGA: Identical to Memory Mode Register Bits (2,1) definition in the VGA section.

Bit 0
EGA: Alpha mode bit.
A logic 1 shows that Alpha mode is active and character map selection is enabled. A logic 0 disables Alpha modes and enables non-Alpha modes.

A.4 CRT CONTROLLER REGISTERS INDEX PORT= 3?4 DATA PORT = 3?5

The EGA registers that are different are listed. For similar registers and identical bits within registers refer to the VGA section. Also, "?" implies that a register is mapped into either 3B5 or 3D5, for Monochrome or Color display modes, respectively.

A.4.1 Index Register (Port = 3?4)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Five bits point to the CRT Registers Address index where the data is to be written.

A.4.2 Horizontal Total Register (Index = 00)

Bits (7:0)

EGA:
Eight bits of value for the "Total Character Count Less 2" are loaded into this register. They define number of characters to be displayed per horizontal line.

A.4.3 End Horizontal Blanking Register (Index = 03)

Bits (7)

EGA: Not Used.

Bits (6:5)

EGA: They define display enable skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

EGA: Five bits of character count are loaded to determine when the horizontal blanking signal becomes inactive.

A.4.4 End Horizontal Retrace Register (Index = 05)

Bit 7

EGA: It defines the start of the odd or even CRT counter memory address following the horizontal retrace time. Logic "1" = Odd Address and logic "0" = Even Address.

Bits (6:0)

EGA: Same as End Horizontal Retrace Registers Bits (6:0) definition in VGA section.

A.4.5 Vertical Total Register (Index = 06)

Bits (7:0)

EGA: Lower eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

A.4.6 CRT Controller Overflow Register (Index = 08)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Identical to CRT Controller Overflow Register bits (4:0) in the VGA section.

A.4.7 Preset Row Scan Register (Index = 08)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Preset Row Scan Register Bits (4:0) definitions in the VGA section.

A.4.8 Maximum Scan Line Register (Index = 09)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Maximum Scan Line Register Bits (4:0) definition in the VGA section.

A.4.9 Cursor Start Register (Index = 0A)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Cursor Start Register Bits (4:0) definition in the VGA section.

A.4.10 Cursor End Register (Index = 0B)

Bit(7)

EGA: Not used.

Bits (6:5)

EGA: They define cursor signal skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	0
1	0	1
1	1	2

Bits (4:0)

EGA: These bits define Cursor End value of row scan address counter. The programmed value is equal to "N+1" where "N" is the last row of the Cursor to be displayed.

A.4.11 Vertical Retrace Start Register (Index = 10) - Write

(Light Pen High register, Index = 10 - Read)

Bits (7:0)

EGA: Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

A.4.12 Vertical Retrace End Register (Index = 11) - Write

(Light Pen Low register, Index = 11 - Read)

Bits (7:6)

EGA: Not used

Bit 5

Enable Vertical Retrace Interrupt.
EGA: It enables the IRQ output buffer control if Logic 0 is programmed. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal. If programmed as logic 1, the IRQ buffer is switched to a high impedance state.

Bit 4

Clear Vertical Retrace Interrupt.
EGA: When programmed to logic 0, the IRQ latch is reset and cleared to 0 if bit 5 = 0. If it is logic 1, the IRQ latch gets set at the end of the vertical display.

Bits (3:0)

EGA: Identical to Vertical Retrace End Register Bits (3:0) definition in the VGA section.

A.4.13 Underline Location Register (Index = 14)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Horizontal scan row where the underline will be displayed. Value programmed is one less than the scan line desired.

A.4.14 End Vertical Blanking Register (Index = 16)

Bits (7:5)
EGA: Not used.

Bits (4:0)
EGA: Identical to End Vertical Blanking Register Bits (4:0) definition in the VGA section.

A.4.15 Mode Control Register (Index = 17)

Bits (7:5)
EGA: Same as Mode Control Register Bits (7:5) definition in the VGA section.

Bit 4
EGA: Not used.

Bits (3:0)
EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.5 GRAPHICS CONTROLLER REGISTERS INDEX PORT = 3CEH DATA PORT = 3CFH

A.5.1 Read Map Select Register (Index = 04)

Bits (7:3)
EGA: Not Used.

Bits (2:0)
EGA: Map selected bits (2:0) which represent encoded value of the memory plane in binary as shown below:

D2	D1	D0	MAP SELECTED
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

A.5.2 Mode Register (Index = 05)

Bit (7:6)
EGA: Not Used

Bits (5:2)
EGA: Identical to Mode Register Bits (5:2) definition in the VGA section.

Bits (1:0)
EGA: Binary coded write bits define the write modes per the table below:

BIT 1	BIT 0	FUNCTION
0	0	Write mode 0 - Refer to earlier section
0	1	Write mode 1 - Refer to earlier section
1	0	Write mode 2 - Refer to earlier section
1	1	Write mode 3 - Not Legal. Selects write mode 1.

A.6 ATTRIBUTE CONTROLLER REGISTERS (PORTS = 3C0/3C1)

A.6.1 Palette Registers (Index = 00 through 0F)

Bits (7:6)
EGA: Not Used.

Bits (5:0)
EGA: Dynamic color selection. Logic 0 = Color deselection, and Logic 1 = color selection per the table below:

BITS	COLOR	PIXEL
5	Sec. Red	VID 5
4	Sec. Green/Inten	VID 4
3	Sec. Blue/Mono	VID 3
2	Red	VID 2
1	Green	VID 1
0	Blue	VID 0

A.6.2 Mode Control Register (Index = 10)

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.6.3 Overscan Color Register (Index = 11)

Bits (7:6)

EGA: Not Used

Bits (5:0)

EGA: Overscan color for the border. For a monochrome display, set all the six bits to logic 0. The border color is defined by the color table for the Palette registers shown above.

A.6.4 Color Plane Enable Register (Index = 12)

Bits (7:6)

EGA: Same as Color Plane Enable Register Bits (7,6) in the VGA section.

Bits (5:4)

EGA:
Determines two of six colors for the Video Status Multiplexer per the table listed:

BIT 5	BIT 4	INPUT STATUS REGISTER 1 (Port 3?A)	
		BIT 5	BIT 4
0	0	VID 2(Red)	VID 0 (Blue)
0	1	VID 5(SRed)	VID 4 (SGreen)
1	0	VID 3(SBlue)	VID 1 (Green)
1	1	VID 5(SRed)	VID 4 (SGreen)

Bits (3:0)

EGA: Same as Color Plane Enable Register Bits (3:0) definition in the VGA section.

A.6.5 Horizontal PEL Panning Register (Index = 13)

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: These four bits determine the horizontal left shift of the video data in number of pixels. In monochrome alpha numeric modes, (9 dots/character) image can be shifted by 9 pixels. For all other graphics or alpha numeric modes, a maximum left shift of 8 pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section.

A.7 APPLICATIONS

The WD90C00 applications section is divided into various interfaces such as processor (AT or Micro Channel mode), video memory, RAMDAC (INMOS G171), monitor, and clock. The description and block diagrams are generic. No attempt is made to present schematic level details. Currently available application notes, technical briefs, and referenced literature at the end of the data book should supplement the information provided in this section. External video subsystem enable I/O port at 3C3H is briefly explained. The Figures 11 through 20 are shown along with their brief description on the subsequent pages.

Figure 11 highlights the various WD90C00 Processor, memory, and I/0 interfaces.

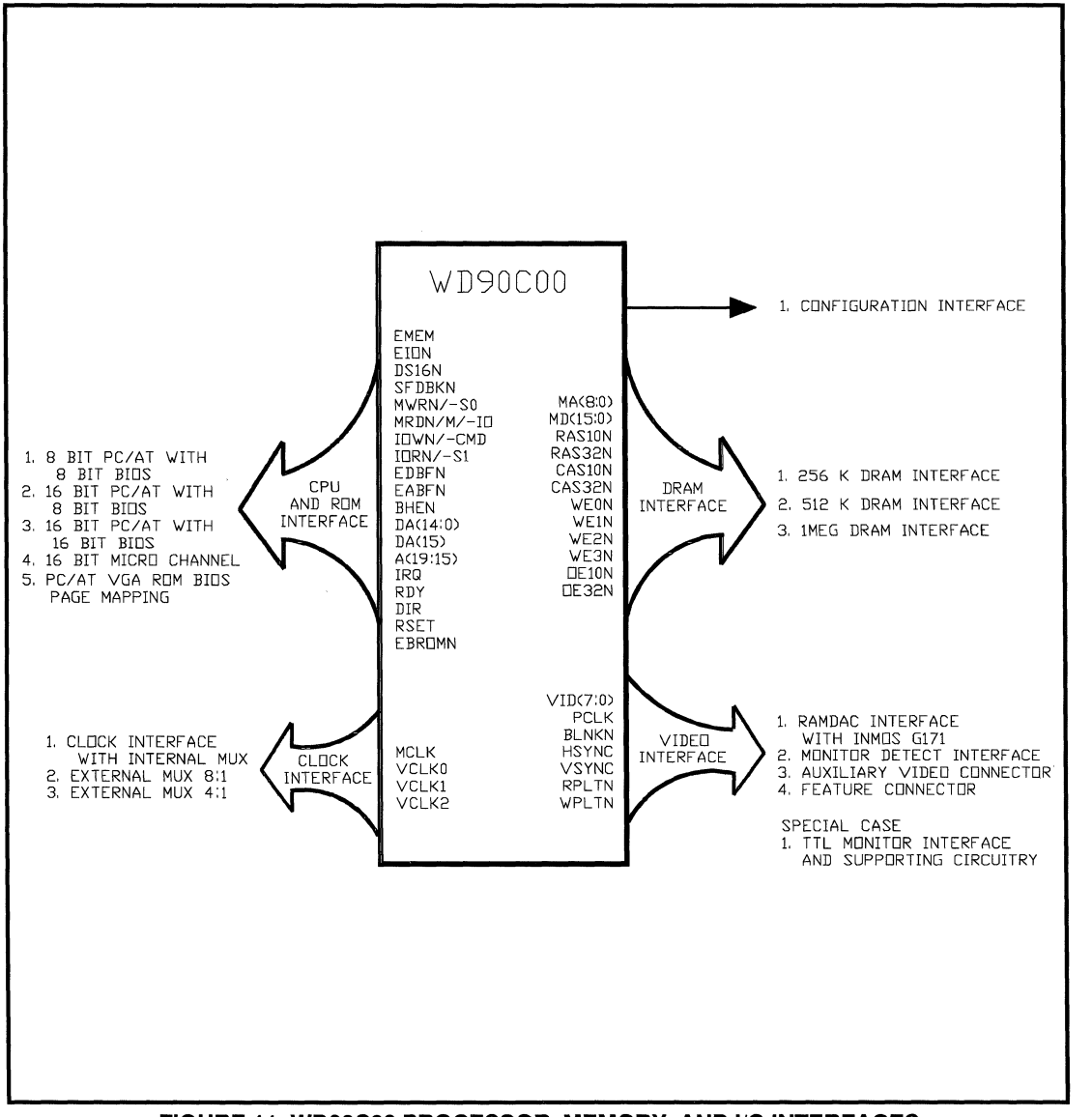


FIGURE 11. WD90C00 PROCESSOR, MEMORY, AND I/O INTERFACES

Figure 12 shows a block diagram of the WD90C00 with 8-bit PC/AT interface using an 8-bit BIOS. The system data bus SD(7:0) and address bus SA(19:0) are shown along with associated buffers and BIOS ROM. Auto monitor sense line is also included.

CONVENTION: "*" = Logic AND function, "/" = Inverted function, and "+" = Logic OR function.

"*" NOTE PA(14:12) CAN BE FROM PAGE MAPPING LOGIC.

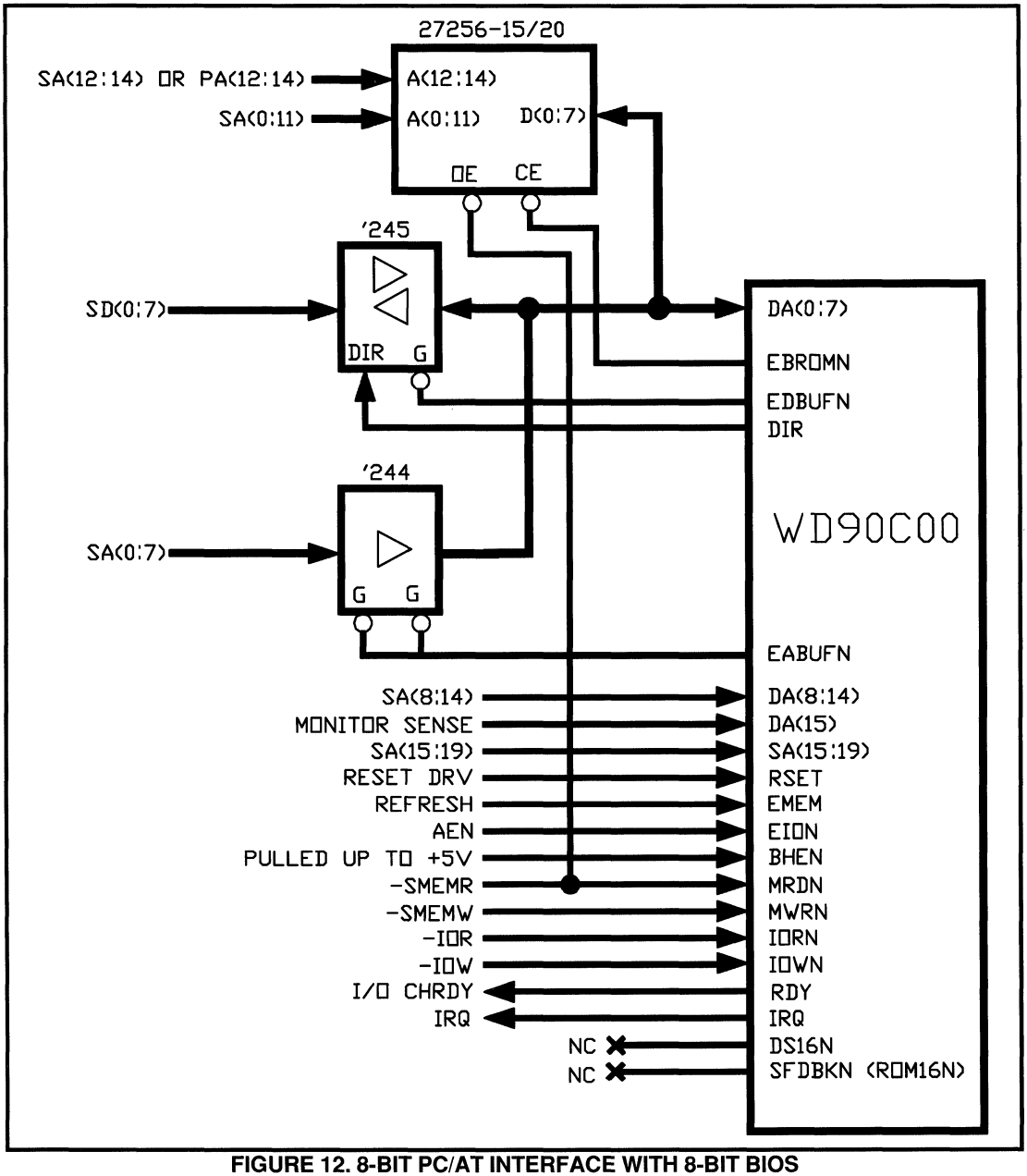


FIGURE 12. 8-BIT PC/AT INTERFACE WITH 8-BIT BIOS

Figure 13 illustrates 16-bit PC/AT interface with 8-bit BIOS using WD90C00. The processor data bus SD(15:0), and the system address bus SA(19:0) are shown. Associated address and data bus buffers, BIOS ROM, and auto monitor sense are also shown in it. Note, PA (14:12) to BIOS ROM can be derived from the BIOS page mapping logic if implemented. Logic equations for upper data bus buffer gate EDBFN1.

/EDBFN1 = /EDBUFN * EBROMN * /SMEMW * /SBHE * /DS16N + EDBUFN * EBROMN * /SMEMR * /SBHE * /DS16N.

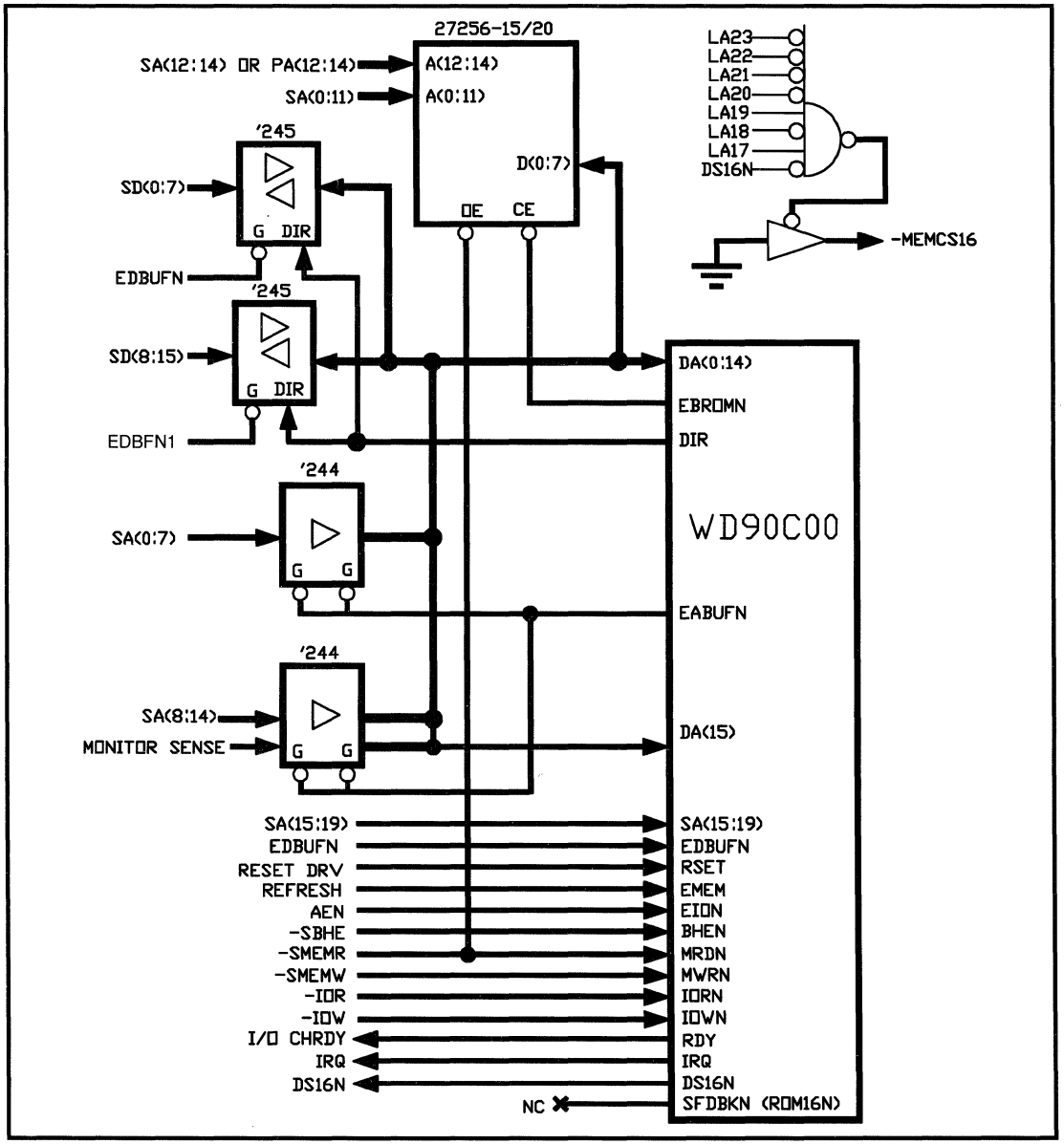


FIGURE 13. 16-BIT PC/AT INTERFACE WITH 8-BIT BIOS

Figure 14 illustrates a 16-bit PC/AT interface with a 16-bit BIOS ROM implementation using WD90C00. The system data bus SD(15:0), address and data bus buffers, and auto monitor sense input is presented. The (16K X 8) upper and lower byte EPROMS, output enable lines (EROM0 / EROM1), from the BIOS page mapping logic if it is implemented. Also, -MEMCS16 implementation is limited to certain bus speeds as SA15 and SA16 are used.

/EROM0 = /EBROMN * /SMEMR * /SA0

/EROM1 = /EBROMN * /SBHE * /SMEMR * /ROM16N + /EBROMN * SA0 * /SMEMR * ROM16N

/EDBFX = /EBROMN * SA0 * /SMEMR * ROM16N + /EBROMN * /SBHE * SA0 * /ROM16N * /SMEMR

/EDBUF1 = /EDBUFN * /SMEMW * /SBHE * /DS16N + /EBROMN * /SMEMR * /SBHE * /ROM16N + /EDBUFN * /SMEMR * /SBHE * /DS16N * EBROMN.

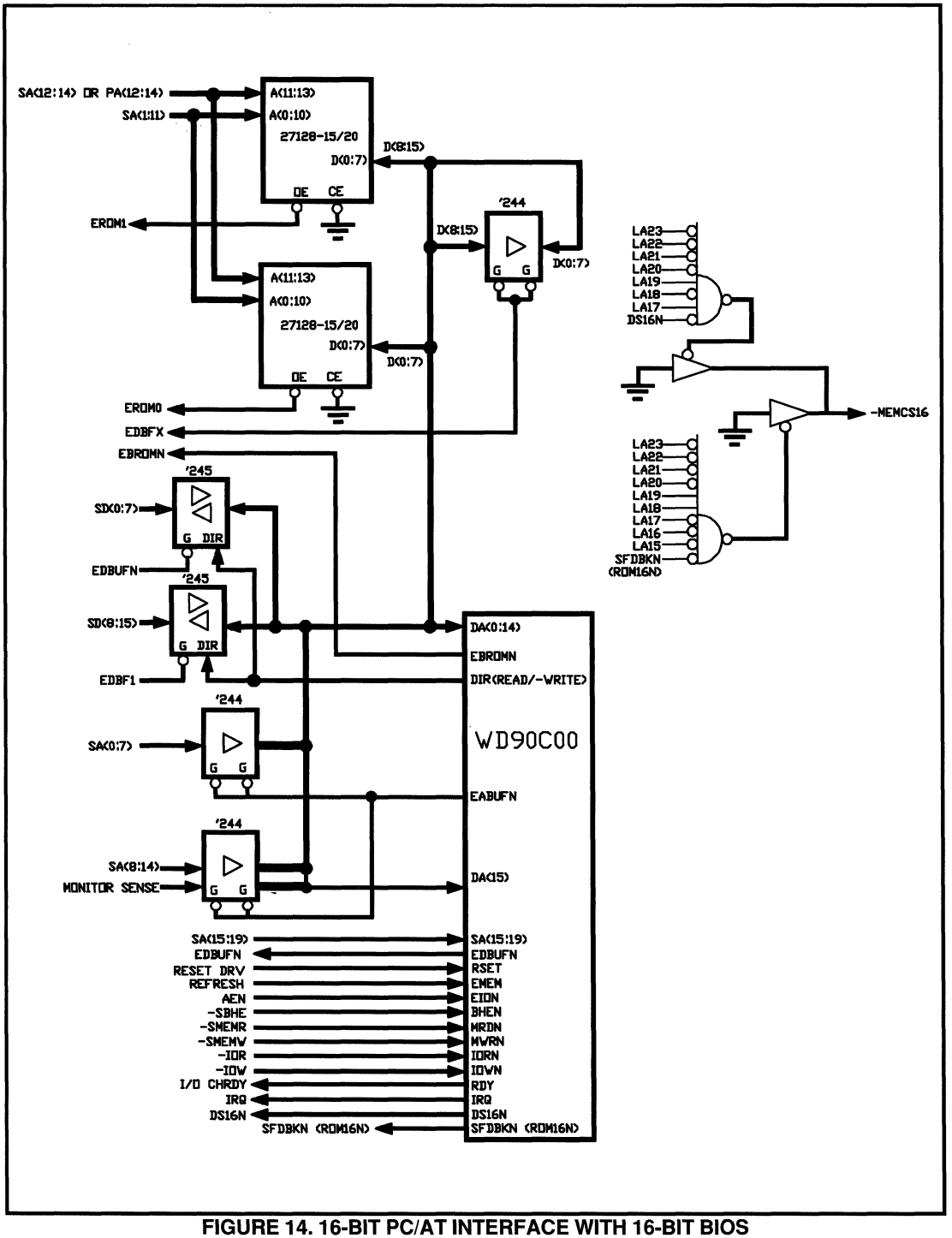


FIGURE 14. 16-BIT PC/AT INTERFACE WITH 16-BIT BIOS

Figure 15 illustrates the WD90C00 and a 16-bit Micro Channel interface. The system data bus upper byte bits D(14:8) and lower data bus byte D(7:0) are sampled and buffered for the WD90C00 input pins DA(14:0). Likewise, system address byte upper bits A(14:8) and lower address byte A(7:0) are buffered and gated to the WD90C00 input pins DA(14:0). The monitor sense input buffer and D15 are gated into the DA15 input of the WD90C00. The Micro Channel bus control signals provide the timing and are gated by the appropriate logic blocks to the WD90C00. Setup must be latched (OFF) with -CMD.

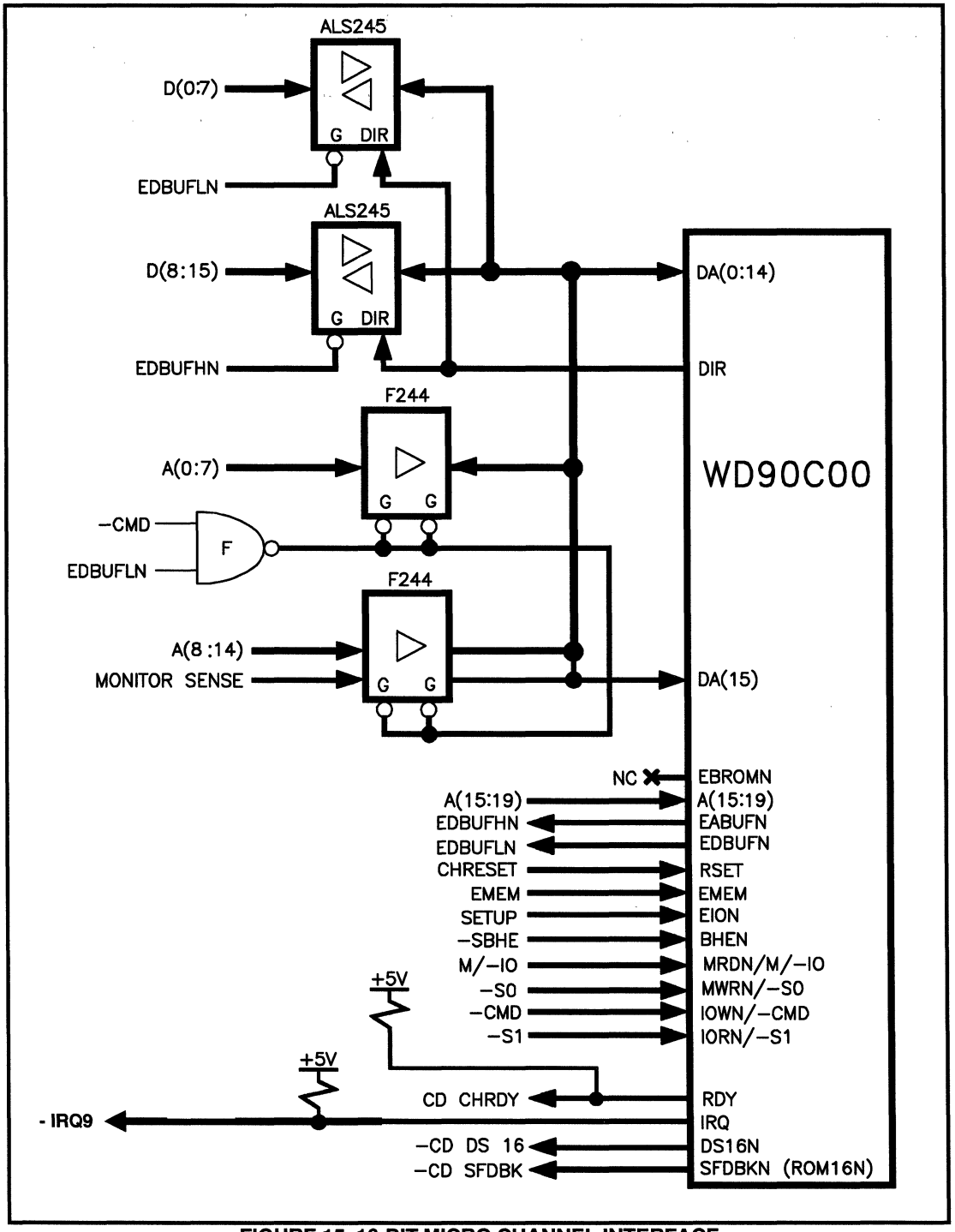


FIGURE 15. 16-BIT MICRO CHANNEL INTERFACE

Figure 16 illustrates the WD90C00 with 1024 KB video memory organization using four 256 KB maps. Each 256 KB map is made from two (256K X 4) DRAMs. The built in DRAM controller provides all the memory control signals and refresh cycles. The WD90C00 also supports 256 KB, or 512 KB video memory organization using (64K X 4) DRAM modules. The 256 KB configuration just does not have MA8 connected to the DRAMs. The 512 KB configuration uses MA8 as select to multiplex the $\overline{CAS10}$ and $\overline{CAS32}$ signals to two 256 KB banks of eight 64K X 4 DRAMs.

Figure 17 illustrates the WD90C00 and RAMDAC (INMOS G171) interface block diagram for analog monitors.

NOTE:
LA(1), LA(0) ARE LATCHED ADDRESSES.
DA(7:0) ARE MULTIPLEXED DATA BITS.

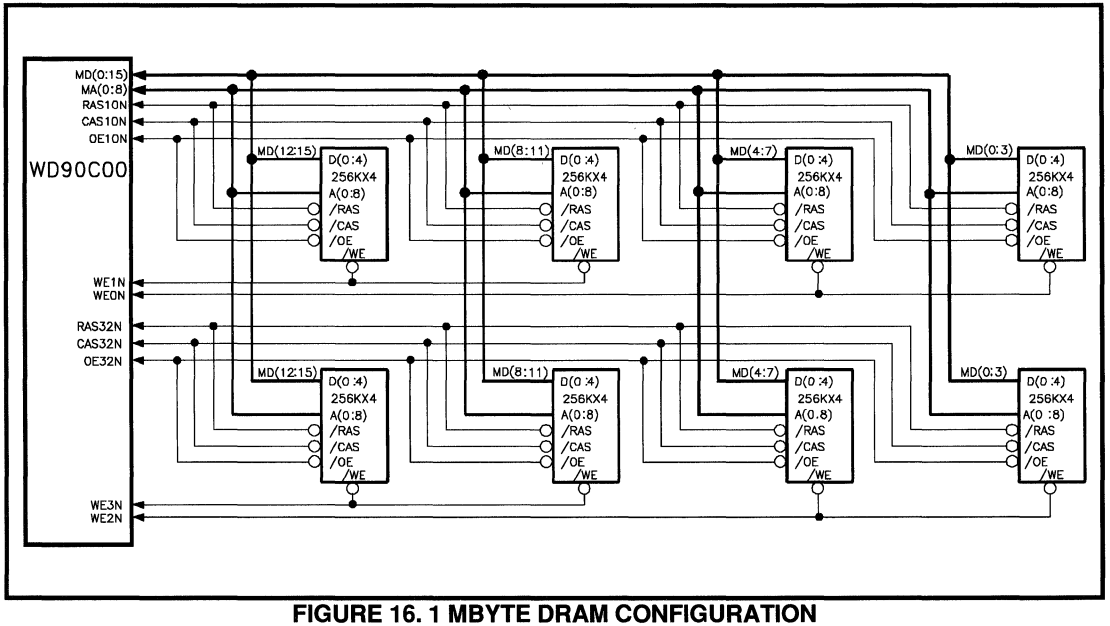


FIGURE 16. 1 MBYTE DRAM CONFIGURATION

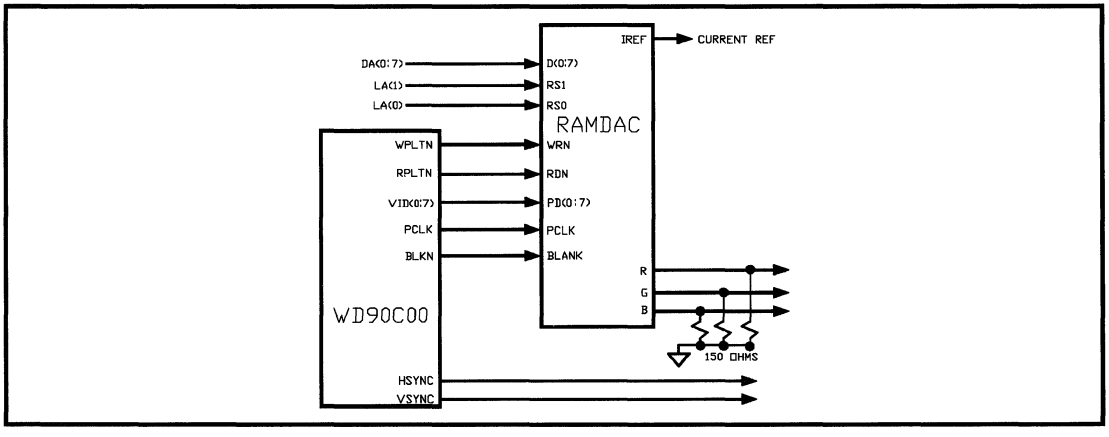


FIGURE 17. RAMDAC INTERFACE

Figure 18 illustrates the WD90C00 and TTL monitor connections.

NOTE:
1. VGA/TTL switch may be used to disable HSYNC and VSYNC for Analog or TTL Video connector.
2. MD(15:12) may also be connected as the EGAswitches if desired. See PR register and Pin out sections for more details.
3. For AT applications using WD90C00, install the IRQ9 resistor.
4. Transistor 2N2222A is used to emulate a Monochrome and a Color Display connection.

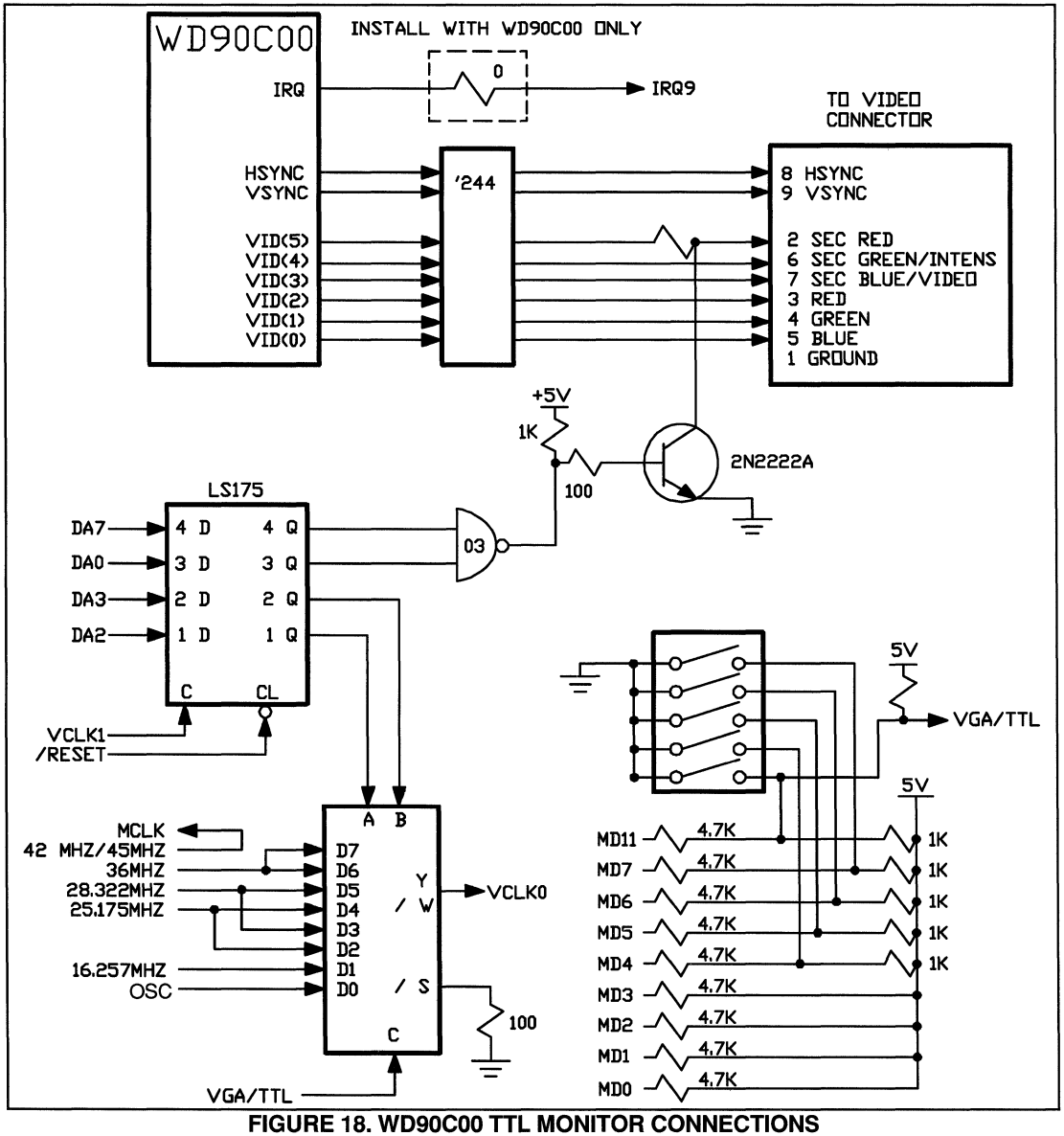


FIGURE 18. WD90C00 TTL MONITOR CONNECTIONS

Figure 19 presents WD90C00 with external oscillators at the clock pins configured as inputs. The clock selection is determined by register 3C2H bit 3 and bit 2. It is described by the table below:

3C2H BIT 3	3C2H BIT 2	CLOCK SELECTION
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

The Configuration register Bit 3 (MD3) should be tied low to make the WD90C00 signal pins (VCLK1, VCLK2) inputs with a 10K Ohm resistor.

Figure 20 illustrates WD90C00 pins VCLK1 and VCLK2 configured as outputs. This is done when the Configuration register Bit 3 (MD3) is tied high with a 4.7K Ohm resistor and PR 15 bit 5 = 1 .

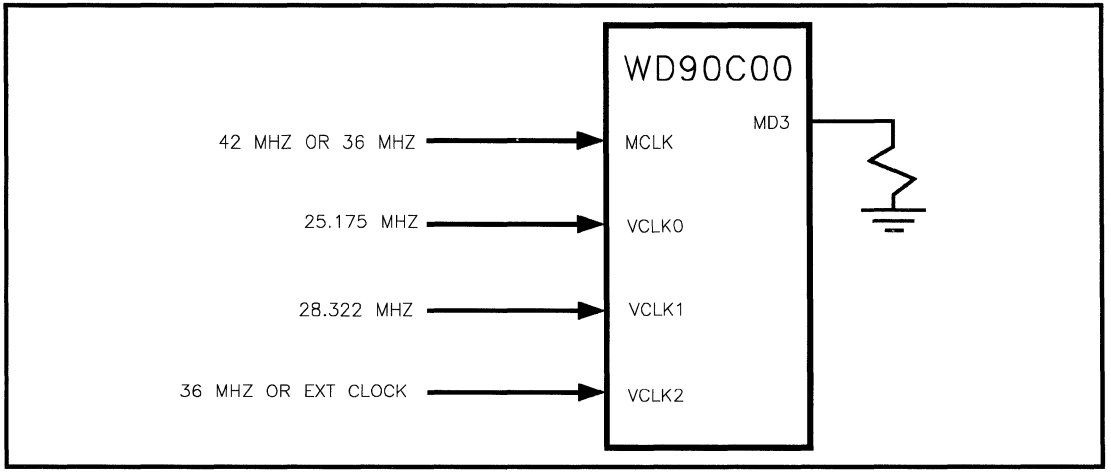


FIGURE 19. CLOCK INTERFACE

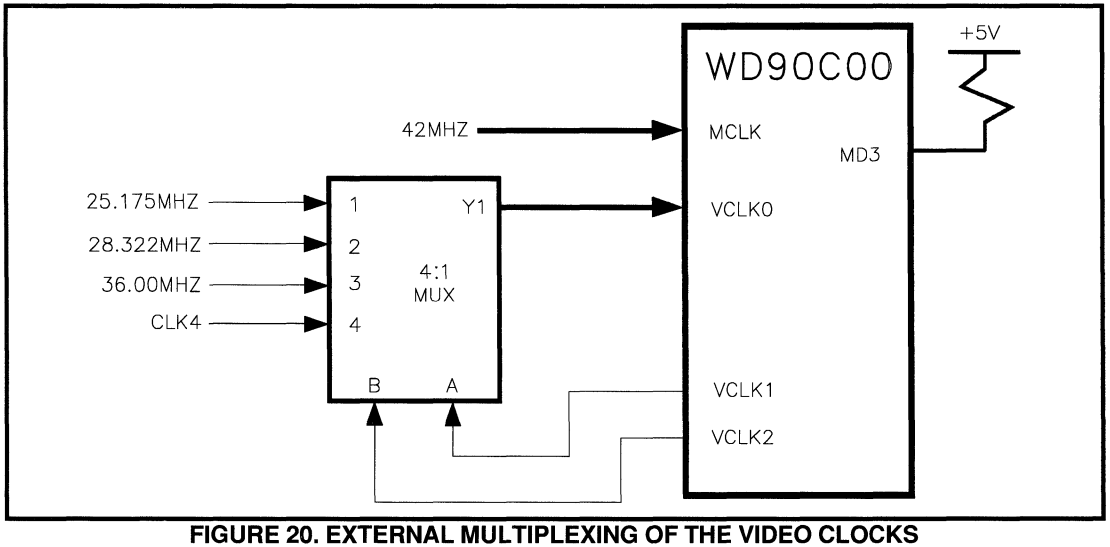


FIGURE 20. EXTERNAL MULTIPLEXING OF THE VIDEO CLOCKS

20

A.8 WD90C00 POWER UP CONFIGURATION

The WD90C00 uses the MD(0:7) and MD(11:15) input pins to configure itself at power up/reset. These lines will, upon power up/reset, latch logic values depending on whether there is a pull up or a pull down resister on them. PR1(1:0), PR11(7:4), and CNF(8:2) are the internal registers that are configured on power up. CNF(3:2) and PR11(7:4) will latch a noninverted value (pull up register = 1) into it and the other will latch an inverted value. For more details see the PR register and Pin out sections.

PR 1 bit 0 will latch the inverted value of MD(0). A value of 1 (pulled down) will map out the decoding of the BIOS ROM by the WD90C00. A value will map it in.

PR 1 bit 1 will latch the inverted value of MD(1). A value of 1 (pulled down) will signify to the WD90C00 that the ROM BIOS data path is 16 bits. The WD90C00 will bring SFDBKN active low in AT mode (static signal) and SFKBKN can be used to externally generate -MEMCS16 (of the AT bus) for 16 bit ROM accesses. In Micro Channel Mode, SFDBKN changes function to be the -CD SFDBK signal output and DS16N is driven active when PR1(1) is set and a valid ROM BIOS address is decoded.

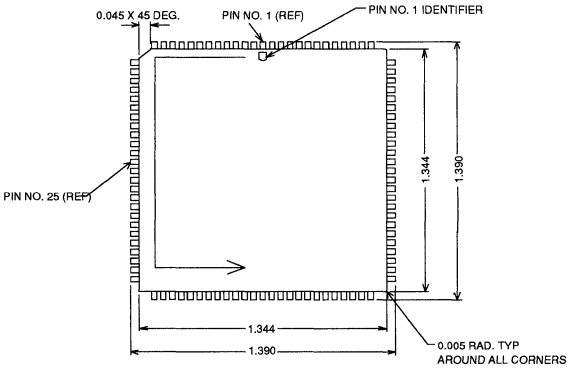
PR11(4:7) bits will latch the EGA switch settings (SW4:SW1) after power up. A pull up resistor will set the appropriate PR11 register bit (4:7) to a logic 1.

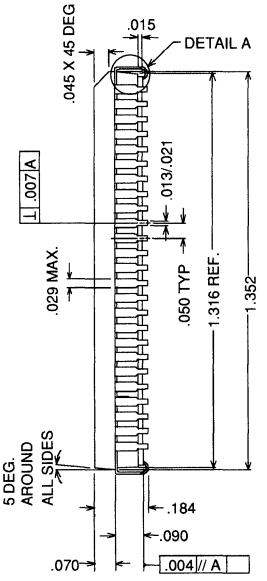
CNF(2) will latch the noninverted value of MD(2). A value of 1 (pulled up) will configure the WD90C00 for IBM PC/XT/AT architecture. A value of 0 will configure the WD90C00 for IBM PS/2 Micro Channel Architecture. WD90C00 Signal Pins and the interface will change functions depending on this value.

CNF(3) will latch the noninverted value of MD(3). This bit configures the WD90C00 pins VCLK1 and VCLK2 as inputs or as outputs. A value of 0 (pulled down) will configure these pins as inputs and a value of 1 sets them as outputs. When used as inputs, these pins when connected to clock crystals supply the video dot clock. The selection of these clocks, through an internal multiplexer and along with VCLK0, depends on the value of 3C2H bits 2 and 3. When used as outputs, VCLK1 becomes an active low load pulse when 3C2H is written to with data. VCLK2 becomes the static value determined by the state of PR2 bit 1. When these signal pins are selected as outputs, the internal multiplexer is locked to select the VCLK0 input pin as the video dot clock.

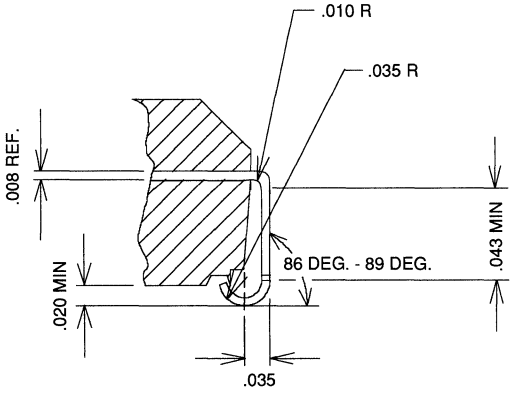
CNF(7:4) will latch the inverted value of MD(7:4). These bits can be read through PR Register PR5 bits 7 to 4. These are general purpose bits that may be used by the video BIOS. If unused by the BIOS, they are available to the application software.

CNF(8) will indicate that a TTL display or an analog monitor is present in the video subsystem. A Pull up resistor on MD(11) causes CNF(8) to be latched 0 indicating that VGA compatible analog display is in the video subsystem.





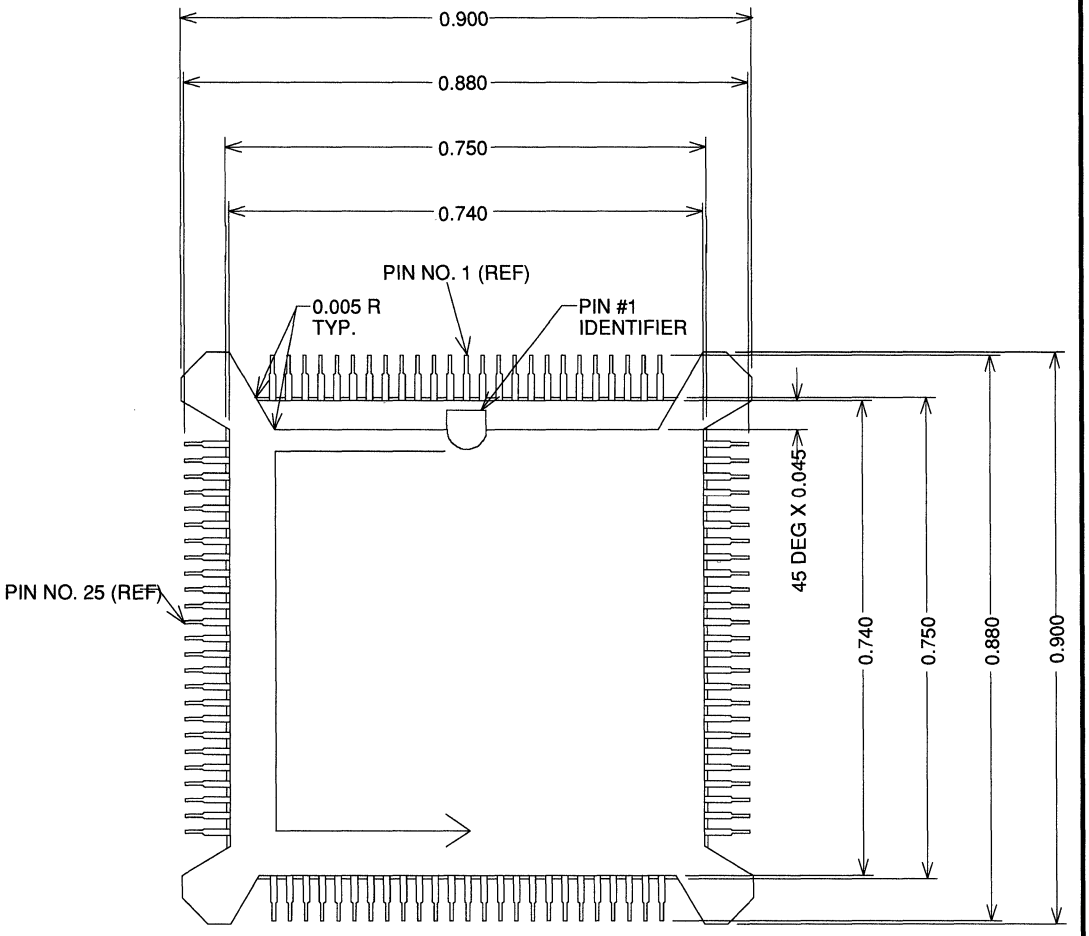
DETAIL A



NOTE: ALL DIMENSIONS ARE IN INCHES.

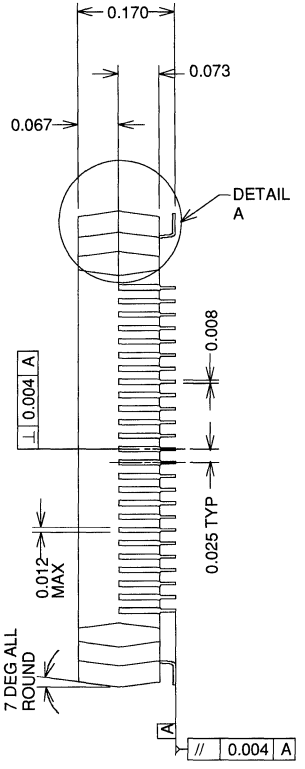
FIGURE 21. 100-PIN PLCC PACKAGE DIMENSIONS

20

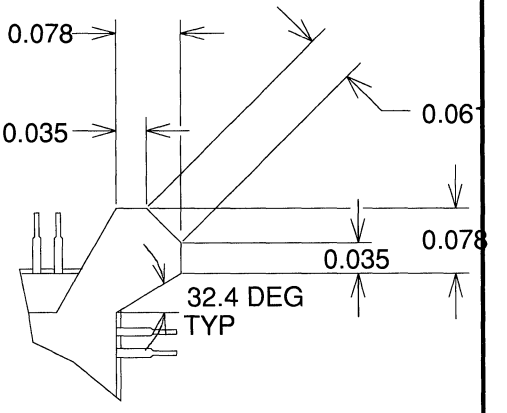


NOTE: ALL DIMENSIONS ARE IN INCHES.

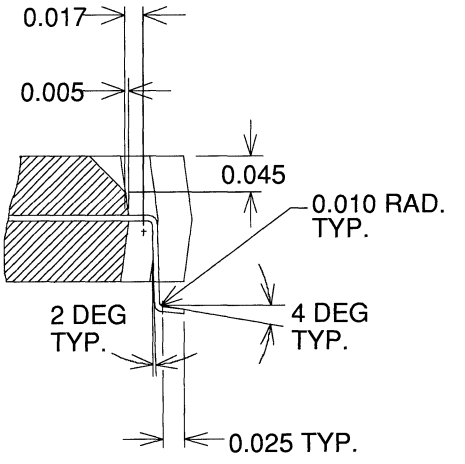
FIGURE 22. 100-PIN JEDEC PLASTIC QUAD FLAT PACKAGE (PQFP)



SIDE VIEW



BUMPER DETAIL



DETAIL A

NOTE: ALL DIMENSIONS ARE IN INCHES.

FIGURE 23. 100-PIN JEDEC (PQFP) PACKAGE DIMENSIONS

20

A.9 REFERENCES

A list of references for generating the WD90C00 data sheet is shown below:

- IBM Personal Computer Hardware User Guide (IBM # 6322510)
- IBM Personal Computer XT Hardware User Guide (IBM # 6322511)
- IBM Personal Computer AT hardware User Guide (IBM # 6280066)
- IBM Personal System 2 Model 30 Hardware User Guide (IBM # 68x2230)
- IBM Personal Computer AT Technical Reference Manual (IBM # 6280070)
- IBM Personal System 2 Model 30 Technical Reference Manual (IBM # 68x2201)
- IBM PC Options & Adapters Technical Reference Manual (IBM # 6322509)
- IBM Personal System 2 BIOS Reference Manual (IBM # 68x2260)
- Personal Computer Reference Manual (IBM # 6025005)
- AT&T Video Display Controller VDC 750 / VDC 600 Installation Guide
- Hercules Graphics Card Owner's Manual
- Paradise OEM Technical Publication Manual

The customers are urged to refer to the manuals listed above and supplement their knowledge from other books and literature available in the market.

WD90C10

(PVGA1M) Enhanced

VGA Controller

TABLE OF CONTENTS

APPENDICES

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

Western Digital Imaging WD90C10 is a 1.25 micron CMOS VLSI device that allows the design of a VGA graphics subsystem to interface with the PC/XT/AT bus, as well as the IBM Micro Channel Bus, while maintaining backwards compatibility with previous video standards such as MDA, EGA, CGA, Hercules and AT&T 6300. The enhancements include Western Digital registers for EGA register level compatibility for PS/2 and TTL monitors, 1024 by 768 color graphics support, and integrated Micro Channel and AT interface. A major advantage of the WD90C10 is that designs implementing this graphics controller will be able to run applications requiring VGA hardware and BIOS compatibility, and also EGA register level compatibility on analog, TTL, or multifrequency monitors, in interlace or non-interlace mode. The WD90C10 supports two 256 Kbyte by 4 DRAMs for operation.

This data book supplies sales order information, a functional overview, signal pin details, a block diagram, internal register descriptions, AC/DC characteristics, timing diagrams, VLSI package mechanical information, and a list of associated references.

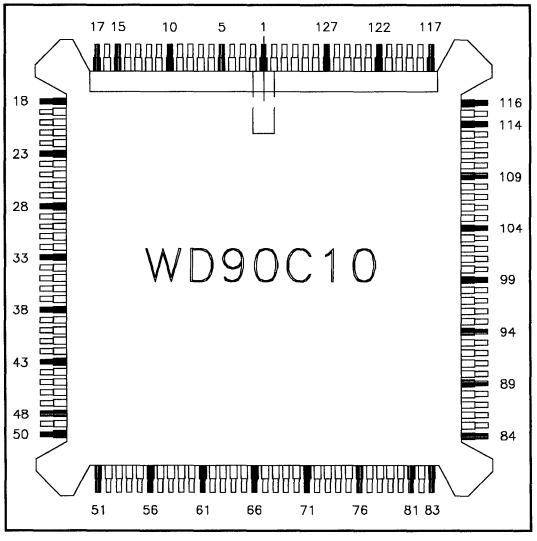


FIGURE 1. WD90C10 PIN DIAGRAM

Ordering Information: WD90C10 Part Number: WD90C10LR00 02.

1.1 FEATURES

- Provides single Chip Video Graphics Solution for IBM PC, XT, AT, and PS/2 compatible systems.
- Supports two 256 Kbyte by 4 DRAMs, providing high performance, high resolution, and 256 colors.
- Pin compatible with the WD90C11 and WD90C12.
- 100% hardware compatible with IBM's VGA and EGA with hidden register support.
- 100% CGA, MDA, Hercules Graphics, and AT&T Model 6300 compatible.
- With two 256K by 4 DRAMs will support 1024 by 768 by 2/4 colors, 800 by 600 by 16 colors, 132 column text.
- Write cache for improved CPU write performance.
- 8- or 16-bit data bus for I/O and memory. True 16-bit CPU to video memory transfer for all modes.
- Up to 65 MHz maximum video clock rate.
- Up to 42 MHz maximum memory clock rate.
- Up to four simultaneous displayable fonts.
- 6, 7, 8, and 9 pixel wide fonts.
- Up to 16 fonts can be loaded.
- Provides adapter video BIOS ROM decoding.
- Total of 18 address bits for cursor location and start address.
- Special double scanning and underline.
- Special display enable or blanking output signal.
- Special border disable.
- Lockable palette, RAMDAC, and overscan registers.
- Special register locking for flat panel applications.
- Supports 16-bit I/O register transfer to index/data register pairs.
- Adjustable internal FIFO and fast page memory interface.
- 132-pin Plastic Flat Pack (PFP) JEDEC package.
- Integrated Feature connector interface and external RAMDAC support.

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	A14	34	D8	67	MD14	100	VID0
2	A15	35	D7	68	MD13	101	VID1
3	A16	36	D6	69	MD12	102	VID2
4	A17	37	D5	70	MD11	103	VID3
5	A18	38	D4	71	MD10	104	VID4
6	A19	39	D3	72	MD9	105	VID5
7	A20	40	D2	73	MD8	106	VID6
8	A21	41	D1	74	MD7	107	VID7
9	A22	42	D0	75	MD6	108	+5VDC
10	A23	43	[$\overline{WE1}$]	76	MD5	109	$\overline{EXVID}$
11	$\overline{BHE}$	44	GND	77	GND	110	GND
12	EMEM	45	$\overline{MRD}$ (M/$\overline{IO}$)	78	MD4	111	VREF
13	$\overline{EIO}$ (3C3D0)	46	$\overline{MWR}$ ($\overline{S0}$)	79	MD3	112	MDET [FSADJ]
14	$\overline{IOCS16}$ ($\overline{CDSETUP}$)	47	$\overline{IOR}$ ($\overline{S1}$)	80	MD2	113	[GND-Analog]
15	GND	48	$\overline{IOW}$ ($\overline{CMD}$)	81	MD1	114	B
16	IRQ ($\overline{IRQ}$)	49	RSET	82	MD0	115	G
17	+5VDC	50	+5VDC	83	+5VDC	116	R
18	$\overline{EBROM}$	51	GND	84	$\overline{EXPCLK}$	117	A0
19	DIR	52	MA0	85	GND	118	A1
20	RDY	53	MA1	86	USR1	119	A2
21	$\overline{MEMCS16}$ ($\overline{CDDS16}$)	54	MA2	87	USR0	120	A3
22	$\overline{EDBUFH}$	55	MA3	88	PCLK	121	A4
23	$\overline{EDBUFL}$	56	MA4	89	$\overline{BLNK}$	122	A5
24	$\overline{ROM16}$ ($\overline{CSFB}$)	57	MA5	90	VSYNC	123	[+5 VDC-Analog]
25	$\overline{HTL}$	58	MA6	91	HSYNC	124	A6
26	D15	59	MA7	92	$\overline{RPLT}$	125	A7
27	D14	60	MA8	93	$\overline{WPLT}$	126	A8
28	GND	61	GND	94	VCLK2	127	A9
29	D13	62	$\overline{RAS}$	95	+5VDC	128	A10
30	D12	63	$\overline{CAS}$	96	VCLK1	129	A11
31	D11	64	$\overline{WE0}$	97	VCLK0	130	A12
32	D10	65	$\overline{OE}$	98	MCLK	131	GND
33	D9	66	MD15	99	GND	132	A13

TABLE 1. WD90C10 PIN ASSIGNMENTS

NOTE:
( ) Micro Channel only.
[ ] Reserved for WD90C11 and WD90C12 option.

2.0 WD90C10 ARCHITECTURE

The WD90C10 contains four major internal modules, the CRT Controller, the Sequencer, the Graphics Controller and the Attribute Controller. The WD90C10 also has four major interfaces: the CPU and BIOS ROM interface, the DRAM Display Buffer interface, the Video and RAMDAC interface, and the Clock interface.

The WD90C10 controls the interfacing between the system microprocessor and video memory. Since the WD90C10 arbitrates video memory between the system microprocessor and the CRT Controller contained within the WD90C10, all data passes through the WD90C10 when the system microprocessor writes to or reads from the video memory.

A FIFO is used internally to achieve the video display bandwidth necessary to interleave CPU accesses and display refresh cycles, using only two 256K by 4 DRAMs.

2.1 WD90C10 MODULES

The CRT Controller module maintains screen refresh functions for the various display modes defined by the BIOS ROM resident firmware. The CRT Controller module also generates horizontal sync (HSYNC), vertical sync (VSYNC), and blanking signal for the display monitor.

The Sequencer functions as a timing generator for the AT bus or Micro Channel interface, in I/O or memory cycles. It also provides the character clock in the alphanumeric mode, and the dot clock in the graphics mode, for the CRT, Graphics, and Attribute Controllers.

The Graphics Controller manages data flow between video memory and the Attribute Controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the Sequencer.

The Attribute Controller modifies the CRT display data stream in graphics and character modes. It controls blinking, underlining, cursor, pixel panning, reverse video, and background or foreground color in all display modes.

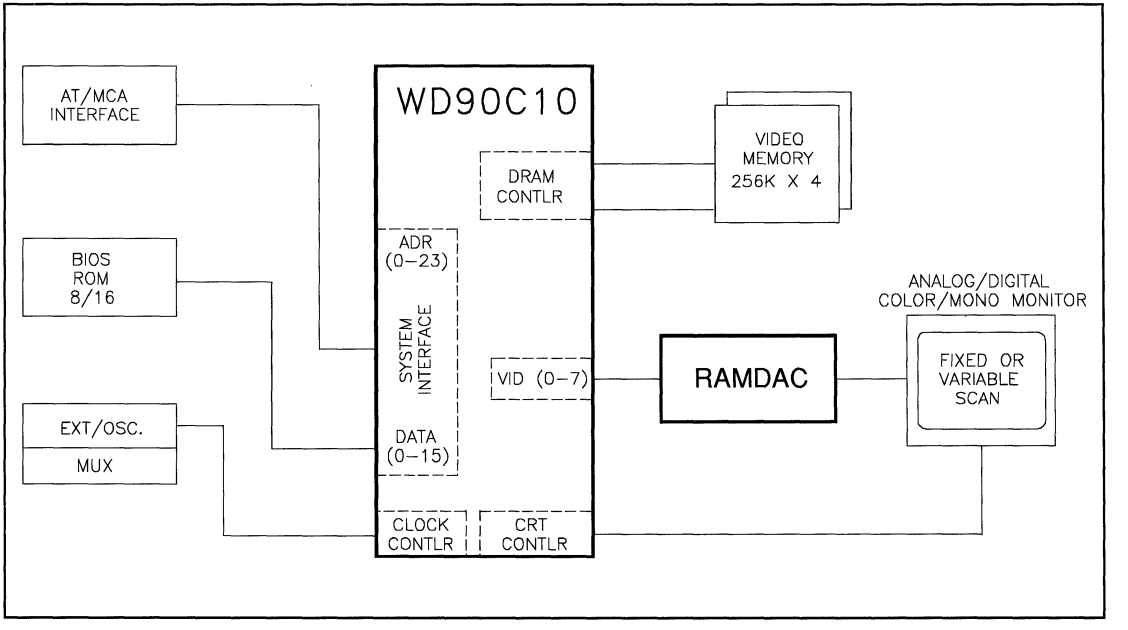


FIGURE 2. SYSTEM BLOCK DIAGRAM

3.0 WD90C10 INTERFACES

3.1 CPU AND BIOS ROM INTERFACE

The WD90C10 is designed to operate in both the PC/XT/AT Bus and the PS/2 Micro Channel Bus architecture configurations. The selection of the mode depends on the setting of a configuration register bit CNF(2), which is determined upon power-up/reset, and is described in the WD90C10 Configuration Bits section of this data book.

Whether configured for either AT or Micro Channel operation, the WD90C10 operates functionally in a manner conducive to PC/XT/AT or Micro Channel interfacing respectively. The signal pins, memory maps and I/O ports all operate to optimize this interface with minimal external circuitry.

The WD90C10 provides all the signals, and decodes all the necessary memory and I/O addresses to interface with the AT bus or the Micro Channel bus, in 8 or 16 bit data path modes. WD90C10 also provides the necessary decoding of the adapter video BIOS ROM. Using the provided signals, the customer can implement designs which operate in 8- or 16-bit mode and control an 8 or 16 bit BIOS ROM.

The I/O data path can be programmed to be either 16- or 8-bit. The CPU to display buffer data path can also be eight or sixteen bits wide for all modes. $\overline{\text{ROM16}}$, $\overline{\text{IOCS16}}$, and $\overline{\text{MEMCS16}}$ signals are generated by the WD90C10.

The WD90C10 has a display memory write cache which holds the CPU write data until it can be transferred to the display memory, allowing the CPU to continue. This feature greatly reduces CPU wait states while writing to the video memory.

The WD90C10 will provide the necessary wait states for CPU accesses to the video memory if necessary. Wait states for I/O accesses and BIOS ROM accesses are not generated.

Special I/O ports such as 46E8H for the AT for setup, and 102H for VGA enable, have been implemented internally in the WD90C10.

3.2 DRAM INTERFACE

The WD90C10 optimizes its interface to the video memory display buffer. The video memory DRAMs are organized as four planes to support all modes from only two 256K by 4 DRAMs by making use of its Fast Page Access of memory. Each plane can be configured as 64 KBytes (128 or 256 Kbyte total).

For display refresh cycles, the WD90C10 will perform page mode read operations on the video memory in graphics modes. In alpha modes, a choice of page video memory read operation is also provided. For video memory write operations during graphics or alpha modes, the WD90C10 will generate standard RAS/CAS cycles as needed. The WD90C10 will also refresh the DRAMs with 3 or 5 (CAS before RAS) refresh cycles after every horizontal scan line.

Two or four 256K by 4, 80 ns DRAMs and a 37.5 MHz MCLK are required for all modes. 70 ns DRAMs can be used with 42 MHz MCLK.

3.3 VIDEO INTERFACE

The WD90C10 is optimized to connect to an analog CRT monitor through a RAMDAC, but it may also be used to drive other types of displays, such as TTL monitors. In interfacing to an analog monitor through an external RAMDAC, the WD90C10 provides all the necessary signals to interface to the video RAMDAC.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and depth (bits/pixels) of the image desired. New monitors, such as multifrequency monitors, are less stringent because of the many sync frequencies available. The WD90C10 can be programmed to directly generate all the CRT signals for up to 8 bits/pixel (256 color) displays.

The Micro Channel Auxiliary Video Connector and the AT Feature Connector can be connected directly to the WD90C10. The WD90C10 also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

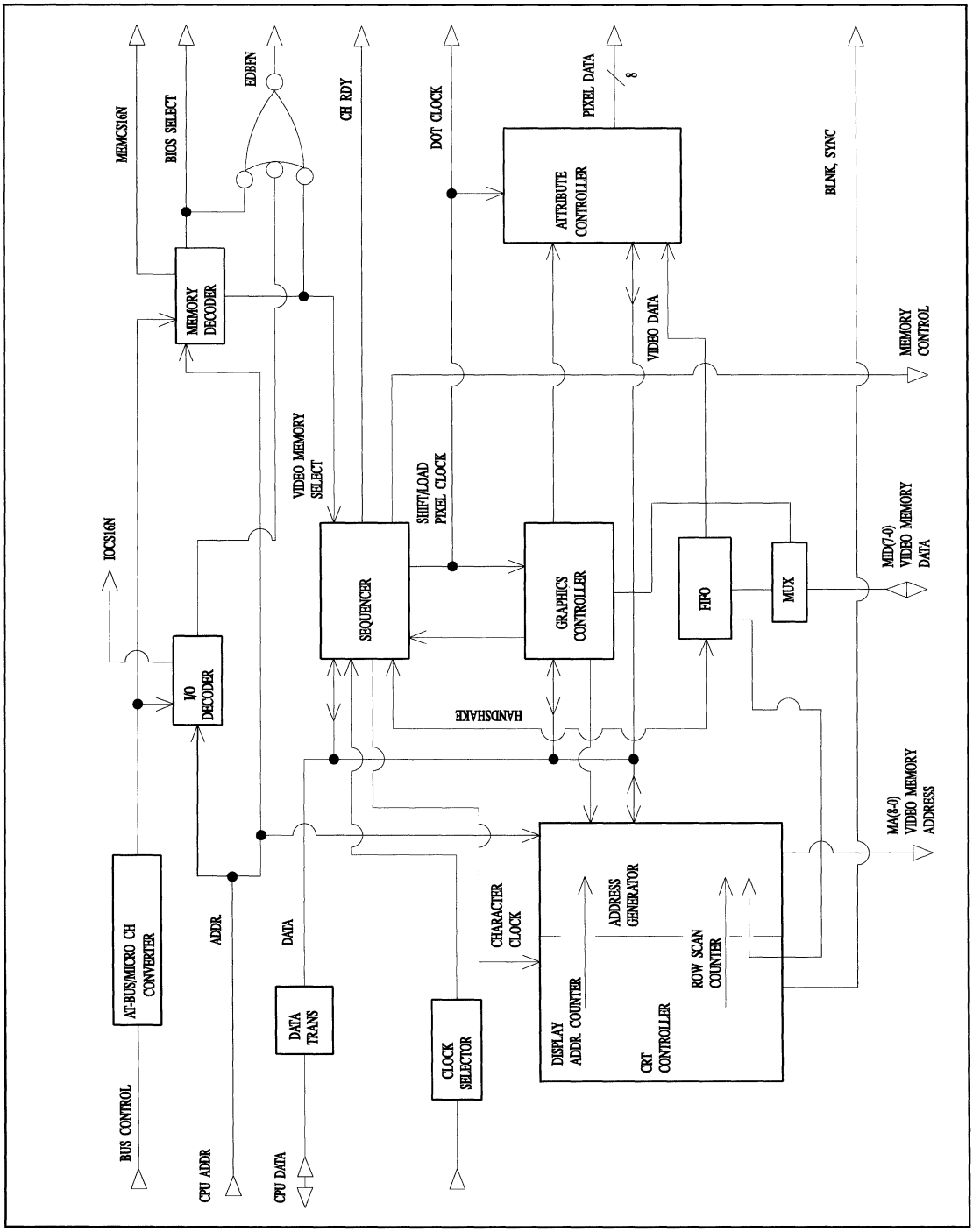


FIGURE 3. WD90C10 BLOCK DIAGRAM

3.4 CLOCK INTERFACE

The WD90C10 has four clock input signal pins; the separate memory clock, MCLK, which drives the DRAM and bus interface timing; and the three video clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing. VCK1 and VCK2 can also be programmed as outputs to provide the option to externally control a multiplexer that supplies the video clock. The MCLK can also be selected as a memory clock or video dot clock .

3.5 WD90C10 POWER-UP CONFIGURATION

The WD90C10 uses the memory data pins to configure an internal configuration register upon power- up/reset. CNF(2) will determine whether the WD90C10 will operate in AT or Micro Channel Architecture (MCA) implementation. Other CNF bits configured by the WD90C10 at power-up/reset are used as status bits, or for clock source control. For more information on WD90C10 power-up configuration, refer to the Configuration Bits section of this data book.

4.0 PIN DESCRIPTION

The following table provides pin definitions for the 132-pin WD90C10 package. The WD90C10 mnemonics are used.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
			POWER ON
49	RSET	I	RESET: This signal input will reset the WD90C10. MCLK and VCLK0 should be connected to WD90C10 in order for the WD90C10 to initialize during Reset. Western Digital configuration bits are initialized at power-up reset based on the logic level on the MD15-0 bus as determined by pull-up/pull-down resistors. The reset pulse width should be at least 10 MCLK clock periods.
			CLOCK SELECTION
98	MCLK	I	MEMORY CLOCK: This clock signal determines the VGA DRAM timing as well as system interface control timing. MCLK should be a minimum 37.5 MHz for 80 ns DRAMS.
97	VCLK0	I	VIDEO CLOCK 0: This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK is 25.175 MHz to display 640 pixels per horizontal display line. The Miscellaneous Output Register bits 2 and 3, both set to 0, will select this clock if VCLK1 and VCLK2 are used as inputs.
96	VCLK1	I/O	VIDEO CLOCK 1: This pin can be a second video display clock input or an output to external clock selection module. Pin direction is determined on Reset by a pull-up/down resistor on pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 is an active low pulse during I/O writes to port 3C2H (or it reflects the contents of 03C2, Miscellaneous Register, bit 2). Refer to the Configuration Register and PR15 Register, bit 5 description.
94	VCLK2	I/O	VIDEO CLOCK 2: A third video display clock input or an output to external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. Acts as a user-defined external clock input, or an output reflecting the content of bit PR2(1) (or it reflects the contents of 03C2, Miscellaneous Register, bit 3) if CNF (3) is set to 1. See the Configuration Register and PR15 Register, bit 5 description.

TABLE 2. PIN DESCRIPTION

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
		HOST INTERFACE	
10 9 8 7	A23 A22 A21 A20	I I I I	ADDRESS BUS (A23 - A20): These address bits should be connected to address bus SA23 - 20 in Micro Channel mode. In AT mode, if CNF(11) = 1, then A23-20 should be connected to LA23-20 of the AT address bus. If CNF(11) = 0, then A22-20 should be connected to LA19 - 17 of the AT address bus, and A23 should be connected to an externally decoded ($\overline{LA23}$ x $\overline{LA22}$ x $\overline{LA21}$ x $\overline{LA20}$) = 1 from the AT address bus. CNF(11) = 0 when MD8 is pulled down with a 4.7 Kohm resistor.
6 5 4 3 2 1 132 130 129 128 127 126 125 124 122 121 120 119 118 117	A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	I I I I I I I I I I I I I I I I I	ADDRESS BUS (SA19-SA0): These inputs are directly connected to the system address bus (SA19 - SA0). Latched address. A19 - A17 can be connected to LA19 - LA17 in 386 systems when CNF (11) = 1. Refer to CNF(11) definition.
26 27 29 30 31 32 33 34 35 36 37 38 39 40 41 42	D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	DATA BUS (SD15 - SD0): These bidirectional signals either may be connected directly to a local data bus requiring less than 8 mA of source/sink, or may be connected through two external bus buffers controlled by $\overline{EDBUFH}$, $\overline{EDBUFL}$, and DIR.

TABLE 2. PIN DESCRIPTION (CONT)

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
20	RDY	O	READY: An active high output which signals to the system processor that a memory access is completed, and is used to add wait states to the CPU bus cycles during video memory accesses. It may be pulled inactive by the WD90C10 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM.
16	IRQ/($\overline{IRQ}$)	O	INTERRUPT REQUEST: Programmable processor interrupt request. It is enabled via bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of Vertical Display occurs, this signal will transition active, causing the interrupt.It will stay latched until CRTC11 bit 4 clears it. In an AT system IRQ is usually not connected, but may be connected if desired. $\overline{IRQ}$ is used to generate interrupt, usually in the Micro Channel mode.
21	$\overline{MEMCS16}$ ($\overline{CDDS16}$)	O	MEMORY CHIP SELECT 16 BITS: In AT mode, this line is used to respond the host to enable 16-bit video memory data transfer. In Micro Channel mode, this line is used to indicate 16-bit video memory or I/O access.
13	$\overline{EIO}$ (3C3D0)	I	ENABLE I/O: In AT mode, this active low signal is used to enable I/O address decoding and is connected directly to the system bus signal AEN (address enable). In Micro Channel mode, this line is from I/O port 3C3 bit 0 to enable video subsystem memory and I/O address decoding. ("1" = enable)
18	$\overline{EBROM}$	O	ENABLE BIOS ROM: In AT mode, this is an active low signal to enable BIOS ROM (C0000H - C7FFFH) if enabled by PR1(0). A WRITE to WD90C10 internal I/O port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
25	$\overline{HTL}$	O	ENABLE HIGH-TO-LOW: (for 16-bit BIOS) If only an 8-bit CPU interface is used, this output enables a data buffer to allow reading the upper byte of ROM data on the lower data bus when 2 ROMs (16-bit) are supported.
12	EMEM	I	ENABLE MEMORY: This signal enables memory decoding when high. It is normally connected to the signal -Refresh.

TABLE 2. PIN DESCRIPTIONS (CONT)

NOTE:
( ) Micro Channel only.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
11	$\overline{BHE}$	I	BYTE HIGH ENABLE: If SA0 is "0", this signal enables 16-bit data transfer mode when $\overline{BHE}$ is "0". With SA0, this signal is also used to select high byte data (SD[15:8]) or low byte data (SD[7:0]). An internal pullup is on this input.
45	$\overline{MRD}$/(M/$\overline{IO}$)	I	MEMORY READ: In AT mode, this signal is called $\overline{MRD}$ and is an active low memory read strobe. In Micro Channel mode, the signal is called M/$\overline{IO}$. It distinguishes between memory and I/O cycles. When (M/$\overline{IO}$) is high, a memory cycle is in process. A low on (M/$\overline{IO}$) shows that an I/O cycle is in process.
46	$\overline{MWR}$/($\overline{S0}$)	I	MEMORY WRITE: The Active low memory write strobe in AT mode. In Micro Channel mode, it becomes $\overline{S0}$ and is the channel status signal which indicates the start and type of a channel cycle. Along with $\overline{S1}$, M/$\overline{IO}$, and $\overline{CMD}$ signals, it is decoded to interpret I/O and memory commands.
47	$\overline{IOR}$/($\overline{S1}$)	I	I/O READ: Active low I/O read strobe in AT mode. In Micro Channel mode, it becomes $\overline{S1}$ and is the channel status signal which indicates the start and type of a channel cycle.
48	$\overline{IOW}$/($\overline{CMD}$)	I	I/O WRITE: Active low strobe. In AT mode, the strobe signals an I/O write. In Micro Channel mode it is the bus data strobe $\overline{CMD}$; address bus validity is signaled by $\overline{CMD}$ going low while the rising edge of $\overline{CMD}$ indicates the end of a Micro Channel bus cycle.
14	$\overline{IOCS16}$ ($\overline{CDSETUP}$)	I/O	I/O CHIP SELECT 16 BITS: In AT mode, used to respond to the host to allow 16-bit I/O access. In Micro Channel mode, is driven by the host to individually select channel connector slots during system configuration.
19	DIR	O	DIRECTION CONTROL: Active high Direction Control for external bus buffers in AT and MCA implementation. The default state is low until a read cycle occurs. The WD90C10 will then drive DIR high to change the direction of the data buffers.
22	$\overline{EDBUFH}$	O	ENABLE DATA BUFFER HIGH: Active low signal allows control of an external data buffer for data bits D8 - D15.
23	$\overline{EDBUFL}$	O	ENABLE DATA BUFFER LOW: Active low signal allows control of an external data buffer for data bits D0 - D7.

TABLE 2. PIN DESCRIPTIONS (CONT)

NOTE:
( ) Micro Channel only.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
24	ROM16/ (CSFB)	O	BIOS ROM SELECT 16 BITS: This signal decodes the ROM address space C0000 - DFFFF. It may be combined with SA15 and SA16 to control MEMCS16 for the address space C0000 - C7FFF. This is an active low, totem-pole output. CARD SELECT FEEDBACK: (Micro Channel mode) This signal is used as Card Selected Feedback to provide positive acknowledgement of its presence at the host's addresses specified. This is an active low output.
DISPLAY MEMORY INTERFACE			
63	CAS	O	COLUMN ADDRESS STROBE: Active low CAS output signal (for both two and four DRAM configurations).
62	RAS	O	ROW ADDRESS STROBE: Active low RAS output signal (for both two and four DRAM configurations).
65	OE	O	OUTPUT ENABLE: Active low DRAM output enable signal (for both two and four DRAM configurations).
64	WE0	O	WRITE ENABLE: Active low write enable signal for first two DRAMs.
43	[WE1]	O	Reserved for WD90C11 and WD90C12.
PROGRAMMABLE OUTPUTS			
87	USR0	O	May be used to control special card or system features.
86	USR1	O	May be used to control special card or system features.

TABLE 2. PIN DESCRIPTION (CONT)

NOTE:
[ ] Reserved for WD90C11 and WD90C12.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
VIDEO MEMORY DATA			
66 67 68 69 70 71 72 73 74 75 76 78 79 80 81 82	MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8 MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	DISPLAY MEMORY DATA (MD15 - 0): These lines are the data bus to the video display DRAMS. The MD15-MD8 data lines are for use with 4-DRAM configurations of the WD90C10 or WD90C12 part. Data lines MD0-15 are pulled up by internal 50K ohm resistors or may be pulled down by external 4.7K ohm resistors to provide setup information on power-up (reset) as follows: **MD — POWER-UP FUNCTION — REGISTER (BIT)** 15 — EGA SW4 — PR11(7) + 14 — EGA SW3 — PR11(6) + 13 — EGA SW2 — PR11(5) + 12 — EGA SW1 — PR11(4) + 11 — Analog/TTL Display — CNF(8) * 10 — 8- or 16-bit ROMs — PR1 (1) * 9 — 3C3 or 46E8 I/O Port for Setup — CNF(9) + 8 — A23 - 20 Connection Select — CNF(11) + 7 — General Purpose — CNF(7) * 6 — General Purpose — CNF(6) * 5 — General Purpose — CNF(5) * 4 — General Purpose — CNF(4) * 3 — VCLK1,2 Input/Output — CNF(3) + 2 — AT/Micro Channel Mode — CNF(2) + 1 — 1 or 2 ROMs — CNF(1) * 0 — BIOS ROM Mapping — PR1(0) * NOTES: "*" Pulldown resistor sets these bits to logic 1. "+" Pulldown resistor sets these bits to logic 0. For more details refer to PR and Configuration Registers.
VIDEO MEMORY ADDRESS			
60 59 58 57 56 55 54 53 52	MA8 MA7 MA6 MA5 MA4 MA3 MA2 MA1 MA0	O O O O O O O O O	MEMORY ADDRESS (MA0 - MA8): Display memory DRAM address. For testing purposes, these pins can be tri-stated by setting Paradise Register PR4(4)=1.

TABLE 2. PIN DESCRIPTIONS

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
		RAMDAC INTERFACE	
107 106 105 104 013 102 101 100	VID7 VID6 VID5 VID4 VID3 VID2 VID1 VID0	O O O O O O O O	VIDEO (VD0-VD7): Pixel video data output to DAC and to Feature Connector. These lines can drive up to a 8 mA load.
92	$\overline{\text{RPLT}}$	O	READ PALETTE: Video DAC register and color palette read signal for an external RAMDAC. Active low during an I/O read of addresses 3C6H, 3C8H, and 3C9H.
93	$\overline{\text{WPLT}}$	O	WRITE PALETTE: Video DAC register and color palette write signal for an external RAMDAC. Active low during an I/O write to addresses 3C6H-3C9H.
88	PCLK	O	PIXEL CLOCK: Video pixel clock output used by the DAC to latch video signals VID0-7. Its source is one of the video clock inputs: VCLK0, VCLK1 or VCLK2 as determined by the Miscellaneous Output register.
		CRT CONTROL	
89	$\overline{\text{BLNK}}$	O	BLANK: Active low display monitor blank pulse to external RAMDAC.
91	HSYNC	O	HORIZONTAL SYNC: Display monitor horizontal synchronization pulse. Active high or low depending on the Miscellaneous Output Register programming.
90	VSYNC	O	VERTICAL SYNC: Display monitor vertical synchronization pulse. Active high or low, depending on the Miscellaneous Output Register programming.
112	MDET [FSADJ]	I I	MONITOR DETECT: This pin is used when the RAMDAC is external. It is used to determine the monitor type and can be read at port 3C2H bit 4. [FULL SCALE ADJUST]: This pin is used when the RAMDAC is internal (WD90C12). It is used to control the RED, GREEN and BLUE's full scale output current.

TABLE 2. PIN DESCRIPTIONS (CONT)

NOTE:
[ ] Reserved for WD90C12.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
INTERNAL RAMDAC [WD90C12]			
116	[RED]	O	RED CURRENT OUTPUT: Used with the WD90C12 - Internal RAMDAC RS170 output from RED DAC to drive an analog monitor.
115	[GREEN]	O	GREEN CURRENT OUTPUT: Used with the WD90C12 - Internal RAMDAC RS170 output from GREEN DAC to drive an analog monitor.
114	[BLUE]	O	BLUE CURRENT OUTPUT: Used with the WD90C12 - Internal RAMDAC RS170 output from BLUE DAC to drive an analog monitor.
111	[VREF]	I	VOLTAGE REFERENCE INPUT: Used with the WD90C12 - Internal RAMDAC input used to set the reference voltage for the RAMDAC.
FEATURE CONNECTOR SUPPORT			
109	$\overline{\text{EXVID}}$	I	ENABLE EXTERNAL VIDEO DATA: A Feature Connector input. A low tri-states the video data lines VID7:0. An internal pullup resistor is provided. In the WD90C12 the VID7:0 lines become inputs to the internal RAMDAC.
84	$\overline{\text{EXPCLK}}$	I	ENABLE EXTERNAL PIXEL CLOCK: A Feature Connector input. A low tri-states the PCKL output. An internal pullup resistor is provided.
POWER AND GROUND			
123	[VCC]	-----	[+5VDC - ANALOG for WD90C12]
113	[GND]	-----	[Ground - ANALOG for WD90C12]
17	VCC	-----	+5VDC
50	VCC	-----	+5VDC
83	VCC	-----	+5VDC
95	VCC	-----	+5VDC
108	VCC	-----	+5VDC
15	GND	-----	Ground
28	GND	-----	Ground
44	GND	-----	Ground
51	GND	-----	Ground
61	GND	-----	Ground
77	GND	-----	Ground
85	GND	-----	Ground
99	GND	-----	Ground
110	GND	-----	Ground
131	GND	-----	Ground

TABLE 2. PIN DESCRIPTIONS

NOTE:
[ ] Reserved for WD90C12.

5.0 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to V_{SS}	-0.3 to 7 Volts
Power Dissipation	1.0 Watt

NOTE
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

5.1 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0° to 70°C
Power Supply Voltage	4.75 to 5.25 Volts

5.2 D.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX	UNITS	CONDITIONS
V(IL)	Input Low Voltage	-0.3	0.8	V	VCC=5V±5%
V(IH)	Input High Voltage	2.0	VCC+0.3	V	VCC=5V±5%
I(IL)	Input Low Current	--	±10	uA	VIN=0.0V
I(IH)	Input High Current	--	±10	uA	VIN=VCC
V(OL)	Output Low Voltage	--	0.4	V	IOL +2.0mA[1]
V(OH)	Output High Voltage	2.4	--	V	IOH=-2.0mA[1]
I(OZ)	High Impedance Leakage Current	-10.0	10.0	uA	OV<VOUT<VCC
C(IN)	Input Capacitance	--	10	pF	FC=1 MHz
C(OUT)	Output Capacitance	--	10	pF	FC=1 MHz

TABLE 3. DC CHARACTERISTICS

NOTE:

The WD90C10 outputs have 2.0 mA maximum source and sink capability except as follows:

IRQ, RDY= 4.0 mA source and 24.0 mA sink.

$\overline{\text{MEMCS16}}$, $\overline{\text{IOCS16}}$ = 20 mA sink.

D15:0, PCLK, VID7:0, $\overline{\text{ROM16}}$ = 8.0 mA source/sink.

$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE0}}$, $\overline{\text{WE1}}$, $\overline{\text{OE}}$, MA8:0, MD15:0 = 1.0 mA source/sink.

6.0 AC TIMING CHARACTERISTICS

The following notes apply to all of the parameters presented in this section:

All units are in nanoseconds
C_L = 20 pF unless otherwise noted

NUMBER	PARAMETER	MIN	MAX	NOTES
	RESET TIMING			
1	Reset Pulse Width	10t		t = 1/MCLK
2	MD Setup to RSET low	50		
3	MD Hold from RSET low	30		
4	RSET low to first $\overline{IOW}$	10t		
	CLOCK TIMING			
1	VCLK Period	t		t = 1/VCLK
2	VCLK high	0.4t	0.6t	@1.4V
3	VCLK low	0.4t	0.6t	@1.4V
4*	Clock Rise Time		3	0.8V - 2.0V
5*	Clock Fall Time		3	0.8V - 2.0V
6	VCLK to PCLK Delay	8	30	45 ns @ 120 pF load up to 30MHz
7a	VCLK to Hsync Delay	8	35	
7b	VCLK to Vsync Delay	8	35	
7c	VCLK to $\overline{BLNK}$ Delay	8	30	
7d	VCLK to VID(7:0) Delay	8	30	45 ns @ 120 pF load up to 30 MHz
8	MCLK period	24	27	
9	MCLK high	10	17	@ 1.4V
10	MCLK low	10	17	@ 1.4V
11	VID (7:0) setup to PCLK	3		
12	VID (7:0) hold from PCLK	3		

TABLE 4. AC TIMING CHARACTERISTICS

* Apply to both VCLK and MCLK.

NUMBER	PARAMETER	MIN	MAX	NOTES
	I/O AND MEMORY READ/WRITE AT MODE TIMING			
1	EMEM setup to $\overline{MRD}$, $\overline{MWR}$ low	20		
2	EMEM hold from $\overline{MRD}$,$\overline{MWR}$ high	15		
3a	A(23:0) setup to $\overline{MRD}$,$\overline{MWR}$ low	20		
3b	A(15:0) setup to $\overline{IOR}$,$\overline{IOW}$ low	20		
3c	$\overline{BHE}$ setup to $\overline{MRD}$,$\overline{MWR}$,$\overline{IOR}$,$\overline{IOW}$ low	20		
4a	A(23:0) hold from $\overline{MRD}$, $\overline{MWR}$ low	15		
4b	A(15:0) hold from $\overline{IOR}$, $\overline{IOW}$ low	15		
4c	$\overline{BHE}$ hold from $\overline{MRD}$,$\overline{MWR}$,$\overline{IOR}$,$\overline{IOW}$ low	15		
5	$\overline{EIO}$ setup to $\overline{IOR}$/$\overline{IOW}$ low	20		
6	$\overline{EIO}$ hold from $\overline{IOR}$/$\overline{IOW}$ high	15		
7	EDBUFxN low from $\overline{IOR}$,$\overline{IOW}$,$\overline{MRD}$,$\overline{MWR}$ low		38	
8	EDBUFxN high from $\overline{IOR}$,$\overline{IOW}$,$\overline{MRD}$,$\overline{MWR}$ high		38	
9	DIR high from $\overline{IOR}$,$\overline{MRD}$ low		38	
10	DIR hold from $\overline{IOR}$ and $\overline{MRD}$ high		38	
11	D(15:0) write data setup to $\overline{IOW}$ & $\overline{MWR}$ high	30		
12a	D(15:0) read data hold from $\overline{IOR}$ high		30	
12b	D(15:0) read data hold from $\overline{MRD}$ high		30	
12c	D(15:0) write data hold from $\overline{IOW}$ high	15		
12d	D(15:0) write data hold from $\overline{MWR}$ high	15		
13a	D(15:0) read data valid from $\overline{IOR}$ low		90	C_L = 70 pF
13b	D(15:0) write data valid after $\overline{MWR}$ low		2t	t= 1/MCLK
14	RDY high from $\overline{MWR}$/$\overline{MRD}$ low *(max is for standard VGA modes)*	10	2.45 µs	
15*	Memory read data valid from RDY high		40	C_L = 70 pF
16	RDY low from $\overline{MWR}$/$\overline{MRD}$ low	10	30	C_L = 100 pF
17	RDY tristate from $\overline{MWR}$/$\overline{MRD}$ high	10	30	C_L = 100 pF
18	$\overline{EBROM}$ low from valid A(23:15)		40	
19	$\overline{EBROM}$ hold from $\overline{MRD}$ high		40	
20a	$\overline{WPLT}$ low from $\overline{IOW}$ low		30	
20b	$\overline{RPLT}$ low from $\overline{IOR}$ low		30	
21a	$\overline{WPLT}$ high from $\overline{IOW}$ high		30	
21b	$\overline{RPLT}$ high from $\overline{IOR}$ high		30	
22	$\overline{EBROM}$ low from $\overline{IOW}$ low (46E8H port)		40	
23	$\overline{EBROM}$ high from $\overline{IOW}$ high (46E8H port)		40	
24	VCLK1 low from $\overline{IOW}$ low (3C2 port)		30	
25	VCLK1 high from $\overline{IOW}$ high (3C2 port)		30	
26	A(15:0) valid to $\overline{IOCS16}$ low		40	C_L = 100 pF
27	$\overline{IOCS16}$ hold from $\overline{IOW}$ high		40	C_L = 100 pF
28	A(23:17) valid to $\overline{MEMCS16}$ low		40	C_L = 100 pF
29	$\overline{MEMCS16}$ hold after valid A(23:17)		40	C_L = 100 pF

TABLE 4. AC TIMING CHARACTERISTICS (CONT)

NUMBER	PARAMETER	MIN	MAX	NOTES
	I/O AND MEMORY READ/WRITE MICRO CHANNEL MODE TIMING			
1	A(23:0),EMEM,$\overline{BHE}$ setup to $\overline{CMD}$ low	20		
2	A(23:0),EMEM,$\overline{BHE}$ hold from $\overline{CMD}$ low	15		
3	$\overline{CDSETUP}$,$\overline{EIO}$ setup to $\overline{CMD}$ low	20		
4	$\overline{CDSETUP}$,$\overline{EIO}$ hold from $\overline{CMD}$ low	15		
5	STATUS setup to $\overline{CMD}$ low	20		
6	STATUS hold from $\overline{CMD}$ low	15		
7	$\overline{EDBUFH}$, $\overline{EDBUFL}$ low from $\overline{CMD}$ low		38	
8	$\overline{EDBUFH}$, $\overline{EDBUFL}$ high from $\overline{CMD}$ high		38	
9	DIR active from $\overline{CMD}$ low		38	
10	DIR inactive from $\overline{CMD}$ high		38	
11	$\overline{CSFB}$ delay from valid address/status		40	CL = 100 pF
12	$\overline{CSFB}$ hold from $\overline{CMD}$ high (I/O cycle)		30	CL = 100 pF
13	$\overline{CSFB}$ hold from invalid address (memory cycle)		30	CL = 100 pF
14	$\overline{CDDS16}$ delay from valid address		40	
15	$\overline{CDDS16}$ hold from invalid address		30	
16	D(15:0) I/O write data setup to $\overline{CMD}$ high		30	
17a	D(15:0) I/O Write data hold after $\overline{CMD}$ high	15		
17b	D(15:0) Memory Write data hold after $\overline{CMD}$ high	0		
17c	D(15:0) I/O Read data hold from $\overline{CMD}$ high	5	20	CL = 70 pF
17d	D(15:0) Memory Read data hold from $\overline{CMD}$ high	5	20	C_L = 70 pF
18a	D(15:0) Memory Write data valid after $\overline{CMD}$ low		50	
18b	D(15:0) I/O Read data valid from $\overline{CMD}$ low		90	C_L = 70 pF
19	RDY high delay from $\overline{CMD}$ low	0	2.45µs	
20*	D(15:0) Memory Read Data valid from RDY high		40	C_L = 70 pF
21	$\overline{CMD}$ high (inactive)	2t+15		
22	RDY low delay from valid address/status	10	30	
23	$\overline{EBROM}$ low from valid address		40	
24	$\overline{EBROM}$ high from $\overline{CMD}$ high		30	
25	$\overline{WPLT}$ /$\overline{RPLT}$ low from $\overline{CMD}$ low		30	
26	$\overline{WPLT}$ /$\overline{RPLT}$ high from $\overline{CMD}$ high		30	
27	VCLK1 low from $\overline{CMD}$ low (3C2 port)		30	
28	VCLK1 high from $\overline{CMD}$ high (3C2 port)		30	

TABLE 4. AC TIMING CHARACTERISTICS (CONT)

* Depends on setting of 3C5, Index 11, bit 4, 3.

0 0 max 40 ns
0 1 max 40 ns + 1t
1 0 max 40 ns + 1t
1 1 max 40 ns - 1t

(t = 1/MCLK)

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM TIMING			
1	$\overline{RAS}$ cycle time	6t	See Note	
2	$\overline{RAS}$ pulse width low	3.5t-6	See Note	
3	$\overline{RAS}$ high time (precharge)	2.5t+6		
4	$\overline{RAS}$ low to $\overline{CAS}$ low	2.5t-9	2.5t -6	
5	$\overline{CAS}$ cycle time	2t	2t	
6	$\overline{CAS}$ pulse width low	1t	1t	
7	$\overline{CAS}$ high time (precharge)	1t	1t	
8	Row address setup to $\overline{RAS}$ low	1.5t-10	1t	
9	Row address hold time from $\overline{RAS}$ low	1t-6	1t+10	
10	Column address setup to $\overline{CAS}$ low	1t-10	1 t	
11	Column address hold from $\overline{CAS}$ low	1t	1t+10	
12	Read Data valid before $\overline{CAS}$ high	2		
13	Read data hold after $\overline{CAS}$ high	0		
14	Write Data setup to $\overline{CAS}$ low	1t-21	1.5t	
15	Write Data hold after $\overline{CAS}$ low	1t-5	1t	
16	$\overline{WE0}$ low setup $\overline{CAS}$ low	1t-5	1t+5	
17	$\overline{WE0}$ low hold after $\overline{CAS}$ high	0	10	
18	$\overline{OE}$ high before $\overline{WE0}$ low	2t-5	2t+5	
19	$\overline{OE}$ low after $\overline{WE0}$ high	1t-5	1t+5	

MCLK edge to $\overline{RAS}$,$\overline{CAS}$, MA(8:0) edge delay may be up to 40 ns

Notes:
Page-mode CRT reads may be 4-32 $\overline{CAS}$ cycles.
CPU writes use 1-4 $\overline{CAS}$ cycles in Page-mode.
CPU reads use 4 $\overline{CAS}$ cycles in Page-mode.

t = 1/MCLK
It is recommended that MCLK = 37.5 MHz for 80 ns DRAM with longer RAS precharge. MCLK = 40 MHz for 80 ns DRAM with shorter RAS precharge. This can be accomplished with selected DRAMs.

TABLE 4. AC TIMING CHARACTERISTICS (CONT)

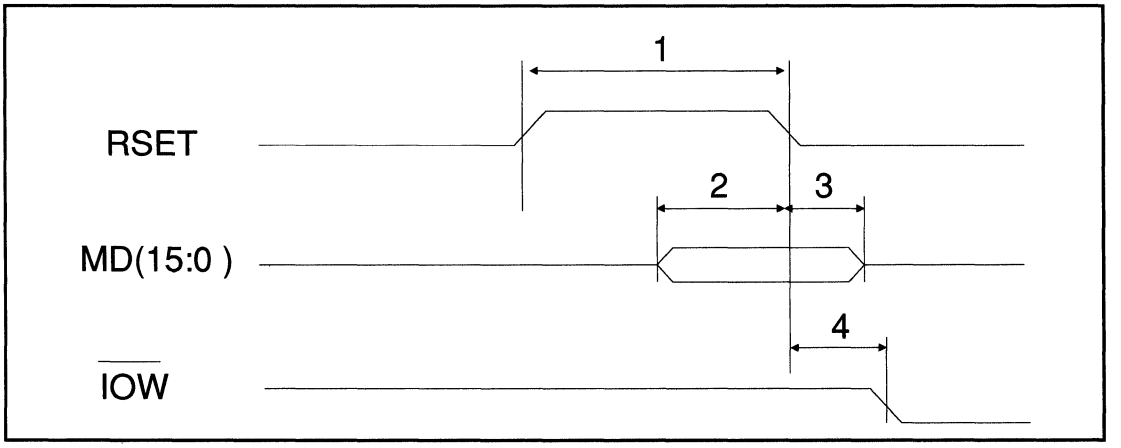


FIGURE 4. RESET TIMING

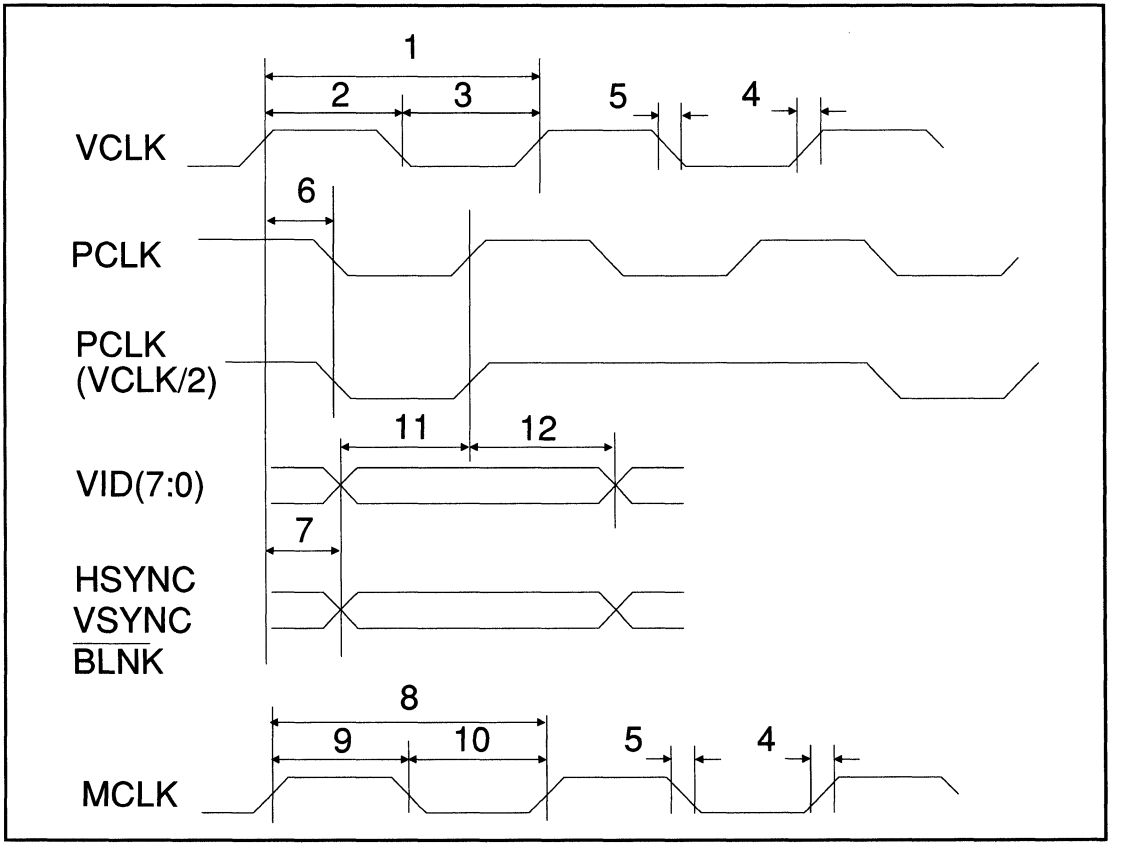


FIGURE 5. CLOCK AND VIDEO TIMING

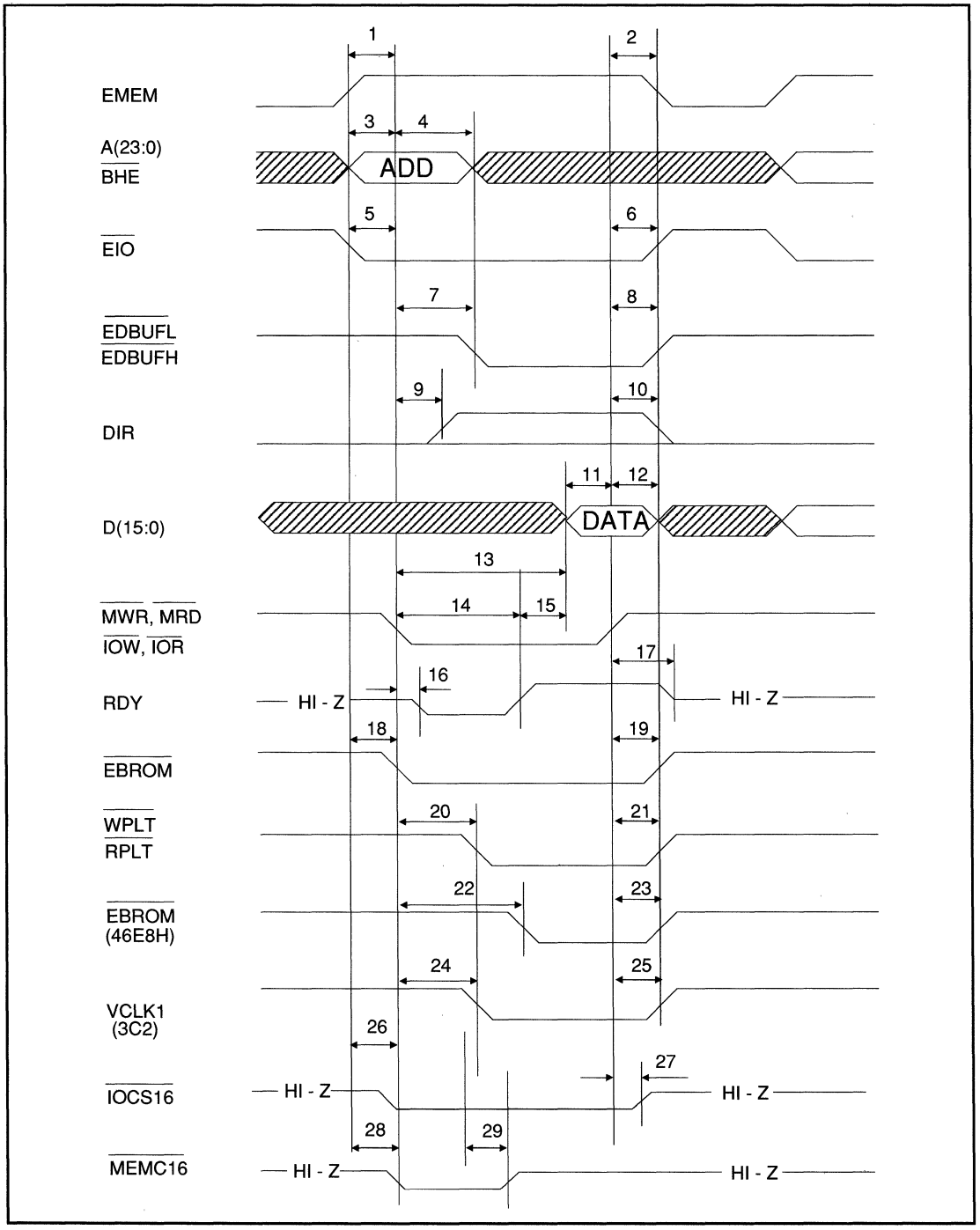


FIGURE 6. AT MODE BUS TIMING

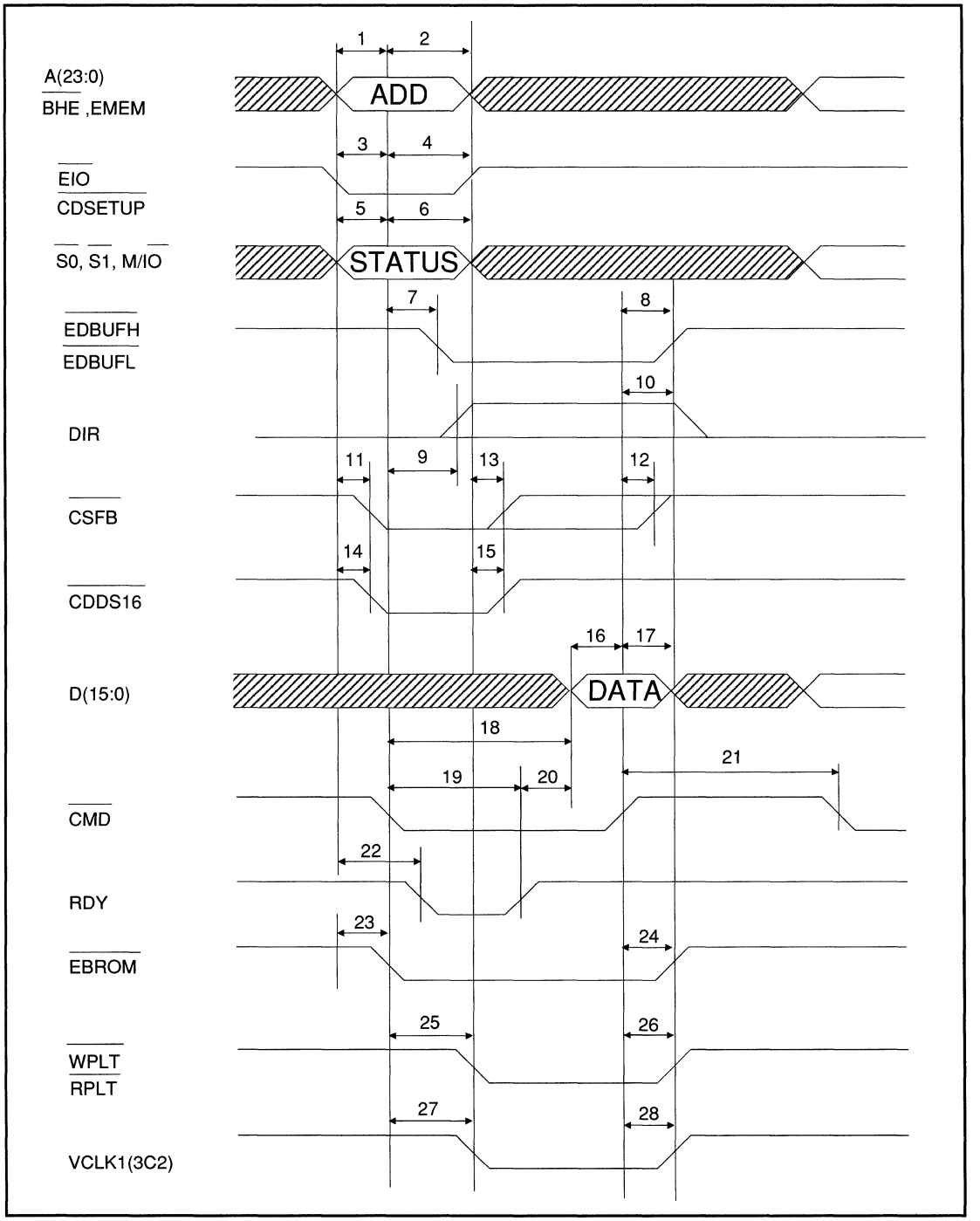


FIGURE 7. MICRO CHANNEL MODE BUS TIMING

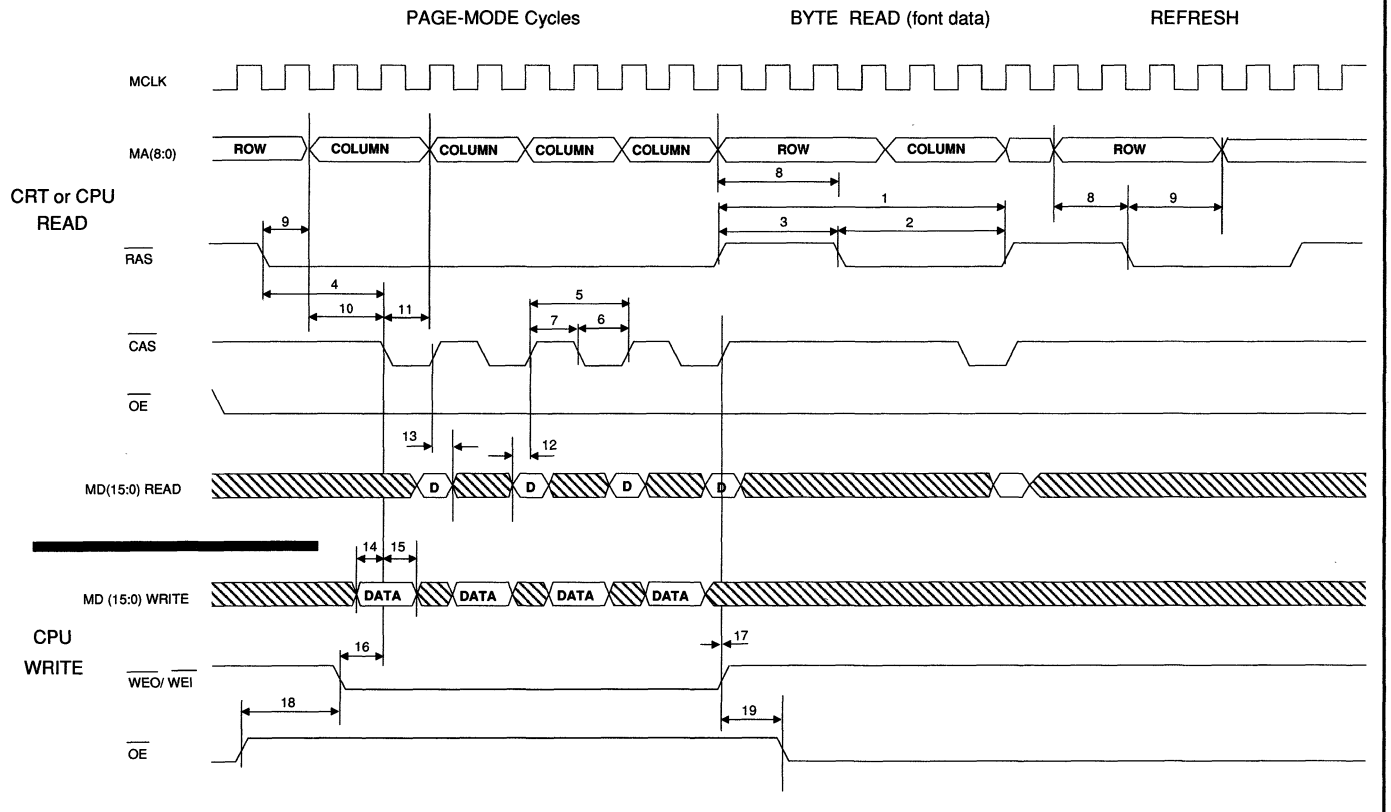


FIGURE 8. DRAM TIMING

7.0 WD90C10 REGISTERS

All the standard IBM registers incorporated inside the WD90C10 are functionally equivalent to the VGA implementation while additional Western Digital registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards defined earlier using the 6845 CRT Controller. This section describes the VGA registers in greater detail, followed by the VGA/EGA difference section and PR registers description. For more information, refer to the reference literature.

7.1 VGA REGISTERS SUMMARY

REGISTERS	RW	MONO	COLOR	EITHER
GENERAL REGISTERS				
Miscellaneous Output Reg	W			3C2
	R			3CC
Input Status Reg 0	RO			3C2
Input Status Reg 1	RO	3BA	3DA	
Feature Control Reg	W	3BA	3DA	
	R			3CA
*Video Subsystem Enable	RW			3C3
AT Mode Setup and Enable	W			46E8
Setup Video Enable	RW			102
* I/O Port 3C3 can be used to replace 46E8 (if CNF (9) = 0) for setup in AT mode. In Micro Channel mode, writes to 3C3, bit 0 = 1 enables memory and I/O address decoding.				
SEQUENCER REGISTERS				
Sequencer Index Reg	RW			3C4
Sequencer Data Reg	RW			3C5
CRT CONTROLLER REGISTERS				
Index Reg	RW	3B4	3D4	
CRT Controller Data Reg	RW	3B5	3D5	
GRAPHICS CONTROLLER REGISTERS				
Index Reg	RW			3CE
Other Graphics Reg	RW			3CF
ATTRIBUTE CONTROLLER REGISTERS				
Index Reg	RW			3C0
Attribute Controller Data Reg	W			3C0
	R			3C1
VIDEO DAC PALETTE REGISTERS				
Write Address	RW			3C8
Read Address	W			3C7
DAC State	R			3C7
Data	RW			3C9
Pel Mask	RW			3C6

1. RO = Read-Only, RW = Read/Write, W = Write, and R = Read.
2. All Register addresses are in hex.

TABLE 5. VGA REGISTERS SUMMARY

7.2 PR REGISTERS SUMMARY

REGISTERS	RW	MONOCHROME	COLOR
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
Reserved 3X5.31- 3X5.3F	RW	3B5.31 - 3B5.3F	3D5.31 - 3D5.3F
** CNF Configuration	-----	-----	-----
PR20 Unlock Sequencer Extended Registers	W	3C5.06	3C5.06
PR21Display Configuration and Scratch Pad	RW	3C5.07	3C5.07
PR30 Memory Interface and FIFO Control	RW	3C5.10	3C5.10
PR31 System Interface Control	RW	3C5.11	3C5.11
PR32 Miscellaneous Control 4	RW	3C5.12	3C5.12

NOTE:
All of the PR Registers may be read/write protected. Refer to the PR Registers' description for more details.

7.3 COMPATIBILITY REGISTERS SUMMARY

FUNCTIONS	RW	MDA	CGA	AT&T	HERCULES
Mode Control Reg	WO	3B8	3D8	3D8	3B8
Color Select Reg	WO		3D9	3D9	
Status Reg	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Reg	WO			3DE	
Hercules Reg	WO				3BF
+CRTC	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

NOTES:
1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. + = 6845 Mode Registers.
4. ** = This register is loaded during power on.

7.4 VGA REGISTERS

Throughout this section, all bit graphics and definitions apply to VGA mode followed by their brief description.

7.5 GENERAL REGISTERS

NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES:

1. Reserved bits should be set to zero.

2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes

   1 = D in Color Modes

7.5.1 Miscellaneous Output Register, Read Port = 3CC, Write Port = 3C2

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.
0= Positive vertical sync polarity.
1= Negative vertical sync polarity.

Bit 6 *

Horizontal Sync Polarity Selection.
0= Positive horizontal sync polarity.
1= Negative horizontal sync polarity.

NOTE:

*These bits determined the vertical size of the frame by the monitor. Their encoding is shown below:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.
When in modes 0-5, one memory page is selected from the two 64KB pages.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bit(3:2) Clock Select 1,0.

BIT 3	BIT 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

Bit 1

System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection. Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0= CRTC and status addresses for MDA mode (3BX).
1= CRTC and status addresses for CGA mode (3DX).

7.5.2 Input Status Register 0, Read Only Port = 3C2

BIT	FUNCTION
7	CRT Interrupt
6, 5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3: 0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit(6:5)

Reserved in VGA.

Bit 4

Monitor Detection in VGA mode. MDET monitor status (pin 112) is sampled and can be read from this bit.

Bit(3:0)

Reserved.

7.5.3 Input Status Register 1, Read Only Port = 3?A

BIT	FUNCTION
7, 6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved
0	Display Enable

Bit(7:6)

Reserved.

Bit(5:4)

Color Plane Diagnostics.
These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.
0= Vertical frame is displayed.
1= Vertical retrace is active.

Bit(2:1)

Reserved.

Bit 0

Display Enable Status.
0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

7.5.4 Feature Control Register, Read Port = 3CA, Write Port = 3?A

BIT	FUNCTION
7 - 4	Reserved
3	Vertical Sync Control
2 - 0	Reserved

Bits(7:4)

Reserved

Bit 3

Vertical Sync Control:
0: Vsync output enabled
1: Vsync output is logical "OR" of Vsync and Vertical Display Enable.

Bit(2:0)

Reserved

7.6 SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE: Reserved bits should be set to zero.

7.6.1 Sequencer Index Register, Read/Write Port = 3C4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Sequencer Address/Index Bits

Bit(7:3)

Reserved.

Bit(2:0)

Sequencer Address/Index.
The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer register to be accessed.

7.6.2 Reset Register, Read/Write Port = 3C5, Index = 00

BIT	FUNCTION
7 - 2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bit(7:2)

Reserved.

Bit 1

Synchronous Reset.
0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0

Asynchronous Reset.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

7.6.3 Clocking Mode Register, Read/Write Port = 3C5, Index = 01

BIT	FUNCTION
7, 6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bit(7:6)

Reserved.

Bit 5

Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character or every other character clock depending on bit 2.
1 = Serial shift registers loaded every 4th character clock (32 bit fetches).

Bit 3

Dot Clock Selection
0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360 pixels).

Bit 2

Shift Load. Effective only if bit 4=0.
0 = Video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.
Commands Sequencer to generate 8 or 9 dot wide character clock.
0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

7.6.4 Map Mask Register, Read/Write Port = 3C5, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bit(7:4)

Reserved.

Bit(3:0)

Controls Writing To Memory Maps (0-3) respectively.
0 = Writing to maps (0-3) disallowed.
1 = Maps (0-3) accessible.

7.6.5 Character Map Select Register Read/Write Port = 3C5, Index = 03

BIT	FUNCTION
7, 6	Reserved
5	Character Map Select A Bit 2
4	Character Map Select B Bit 2
3	Character Map Select A Bit 1
2	Character Map Select A Bit 0
1	Character Map Select B Bit 1
0	Character Map Select B Bit 0

If Sequencer Register 4 bit 1 is 1, then the attribute byte bit 3 in text modes is redefined to control switching between character sets. A 0 selects character map B. A 1 selects character map A. Character Map selection from either plane 2 or plane 3 is determined by PR2(2), PR2(5) and bit 4 of the attribute code.

Bit(7:6)

Reserved.

Bit 5

Character Map A MSB Select.
The Most Significant Bit (MSB) of character map A along with bits 3 and 2, select the location of character map A as shown below.

BITS 5 3 2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit 4

Character Map B MSB Select.
The MSB of character map B along with bits 1 and 0, select the location of character map B as shown below.

BITS 4 1 0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit(3:2)

Character Map Select A.
Refer to bit 5 table.

Bit(1:0)

Character Map Select B.
Refer to bit 4 table.

7.6.6 Memory Mode Register, Read/Write Port = 3C5, Index = 04

BIT	FUNCTION
7 - 4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bit(7:4)

Reserved.

Bit 3

Chains 4 Maps.
0 = Processor sequentially accesses data using map mask register.
1 = Directs the two lower order video memory address pins (MA0,MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.
0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.
1 = Sequential processor access as defined by map mask register.

Bit 1

Extended Video Memory.
0 = 64 KB of video memory.
1 = Greater than 64KB of memory for VGA/EGA modes.

Bit 0

Reserved.

7.7 CRT CONTROLLER REGISTERS

PORT	INDEX	VGA REGISTER NAME	*6845 REG NAME
3?4	---	CRT Controller Address Reg.	CRTC Address Reg
3?5	00	Horizontal Total	Hor. Total
3?5	01	Horizontal Display Enable End	Hor. Disp
3?5	02	Start Horizontal Blanking	+
3?5	03	End Horizontal Blanking	+
3?5	04	Start Horizontal Retrace	+
3?5	05	End Horizontal Retrace	+
3?5	06	Vertical Total	+Vert. Disp.
3?5	07	Overflow	+
3?5	08	Preset Row Scan	+
3?5	09	Maximum Scan Line/Others	Max. Scan Line Add.
3?5	0A	Cursor Start	Cursor Start
3?5	0B	Cursor End	Cursor End
3?5	0C	Start Address High	Start Add. High
3?5	0D	Start Address Low	Start Add. Low
3?5	0E	Cursor Location High	Cursor Loc. High
3?5	0F	Cursor Location Low	Cursor Loc. Low
3?5	10	Vertical Retrace Start	Light Pen High Read
3?5	11	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	
3?5	13	Offset	+
3?5	14	Underline Location	+
3?5	15	Start Vertical Blank	+
3?5	16	End Vertical Blank	+
3?5	17	CRTC Mode Control	+
3?5	18	Line Compare	+

TABLE 6. CRT CONTROLLER REGISTERS

NOTES:

1. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0=B in Monochrome Modes and
1=D in Color Modes

2. "*" 6845 Mode Registers are defined and explained in greater in the reference literature.

3. "+" This register can be programmed in VGA mode only. It is not applicable in 6845 mode.

4. Reserved bits should be set to zero.

7.7.1 CRT Address Register Read/Write Port = 3?4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Index bits

Bit(7:5)

Reserved.

Bit(4:0)

Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed hex.

7.7.2 Horizontal Total Register Read/Write Port = 3?5, Index=00H

BIT	FUNCTION
7 - 0	Horizontal Total Period

Bit(7:0)

Count Plus Retrace Less 5.

In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line.

7.7.3 Horizontal Display Enable End Register Read/Write Port = 3?5, Index 01H

BIT	FUNCTION
7 - 0	Displayed Characters per scan line

Bit(7:0)

The total displayed characters less one are programmed in this register. This register is locked if PR3(5) = 1 or the Vertical Retrace End Register bit 7= 1.

7.7.4 Start Horizontal Blanking Register Read/Write Port = 3?5, Index = 02H

BIT	FUNCTION
7 - 0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches this character clock value. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

7.7.5 End Horizontal Blanking Read/Write Port = 3?5, Index = 03H

BIT	FUNCTION
7	Reserved
6, 5	Display Enable Signal Skew Control
4 - 0	End Horizontal Blanking (lower 5 bits)

This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

Bit 7

Reserved

Bit(6:5)

Display Enable Signal Skew Control.
They define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

BIT 6	BIT 5	SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

End Horizontal Blanking.
End Horizontal Blank signal width "W" is determined as the value of start blanking register plus "W" in character clocks. The least significant five bits are programmed in this register, while the most significant bit is the End Horizontal Retrace Register (Index 05H) bit 7.

7.7.6 Start Horizontal Retrace Pulse Register Read/Write Port = 3?5, Index = 04H

BIT	FUNCTION
7 - 0	Start Horizontal Retrace Character Count

Bit(7:0)

Start Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

7.7.7 End Horizontal Retrace Register Read/Write Port = 3?5, Index = 05H

BIT	FUNCTION
7	End Horizontal Blank bit 6
6, 5	Horizontal Retrace Delay
4 - 0	End Horizontal Retrace

This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

Bit 7

MSB (Sixth Bit) Of End Horizontal Blanking Register.

Bit(6:5)

Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

BIT 6	BIT 5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

Bit(4:0)

End Horizontal Retrace Pulse Width "W".
Start retrace register value is added to the character count for width "W". The least significant five bits are programmed in this register. When the Start Horizontal Retrace Register value matches these five bits, the horizontal retrace signal is turned off.

7.7.8 Vertical Total Register Read/Write Port = 3?5,Index = 06H

BIT	FUNCTION
7 - 0	Vertical Total Scan Lines

Bit(7:0)

Raster Scan Line Total Less 2.
The least significant eight bits of a ten bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync are also included. The ninth and tenth bits of this count are loaded into the Vertical Overflow Register (index = 07H) bit 0 and bit 5 respectively. In 6845 modes, total vertical display time in rows is programmed into bit 6 - bit 0, while bit 7 is reserved. Scan count reduction is not necessary. (The number of scan lines in a row is determined by the maximum Scan Line Register (index 09H bits 0 through 4). This register is locked if the PR Register PR3 (0) = 1 or the Vertical Retrace End Register bit 7 = 1.

7.7.9 Overflow Vertical Register Read/Write Port = 3?5, Index = 07H

BIT	FUNCTION
7	Vert. Ret. Start Bit 9
6	Vert. Display Enable End Bit 9
5	Vert. Total Bit 9
4	Line Compare Bit 8
3	Start Vert. Blank Bit 8
2	Vert. Ret. Start Bit 8
1	Vert. Display Enable End Bit 8
0	Vert. Total Bit 8

++Bit 7

Vertical Retrace Start Bit 9 (index = 10H).

****Bit 6**

Vertical Display Enable End Bit 9 (index = 12H).

++Bit 5

Vertical Total Bit 9 (index = 06H).

Bit 4

Line Compare Bit 8 (index = 18H).

++Bit 3

Start Vertical Blank Bit 8 (index =15H).

++Bit 2

Vertical Retrace Start Bit 8 (index = 10H).

****Bit 1**

Vertical Display Enable End Bit 8 (index = 12)

++ Bit 0

Vertical Total Bit 8 (index = 06H)

NOTES:

+ This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

** This register is locked if the PR Register PR3(1)=0 AND the Vertical Retrace End Register bit 7 = 1.

++ This register is locked if the PR Register PR3(0) = 1 OR the Vertical Retrace End Register bit 7 = 1.

7.7.10 Preset Row Scan Register Read/Write Port = 3?5, Index = 08H

BIT	FUNCTION
7	Reserved
6, 5	Byte Panning Control
4 - 0	Preset Row Scan Count

Bit 7

Reserved.

Bit(6:5)

Byte Panning Control.
These bits allow up to 3 bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 byte left shift
1	0	2 bytes left shift
1	1	3 bytes left shift

Bit(4:0)

Preset Row Scan Count.
These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

7.7.11 Maximum Scan Line Register Read/Write Port=3?5, Index=09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare bit 9
5	Start Vertical Blank bit 9
4 - 0	Maximum Scan Line

Bit 7

200 To 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.
This is bit 9 of the Line Compare Register (index = 18H).

Bit 5

Start Vertical Blank.
This is bit 9 of the Start Vertical Blank Register (index = 15H). This register is locked if the PR Register PR3 (0) = 1.

Bit(4:0)

Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, bits 5-7 are reserved, and bits 4-0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported.

7.7.12 Cursor Start Register Read/Write Port = 3?5, Index = 0AH

BIT	FUNCTION
7, 6	Reserved
5	Cursor Control
4 - 0	Cursor Start Scan Line

Bit(7:6)

Reserved.

Bit 5

Cursor Control.
0=Cursor on.
1=Cursor off.

Bit(4:0)

These bits specify the row scan counter value within the character box where the cursor begins. These bits contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0BH), no cursor is generated. For 6845 modes, bit 7 is reserved. Bit 5 controls the cursor operation and bits 4-0 contain the cursor start value. Bit 6 is not used.

7.7.13 Cursor End Register Read/Write Port = 3?5h, Index = 0BH

BIT	FUNCTION
7	Reserved
6, 5	Cursor Skew
4 - 0	Cursor End Scan Line

Bit 7

Reserved.

Bit(6:5)

Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the table below.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

Cursor End Scanline
These bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, bits 7-5 are reserved and bits 4-0 contain row value of the cursor end.

NOTE: There are three types of cursors generated, depending upon the mode i.e, EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

7.7.14 Start Address High Register Read/Write Port 3?5H, Index = 0CH

BIT	FUNCTION
7 - 0	Start Address High Byte

Bit(7:0)

Display Screen Start Address Upper Byte Bits.
Eight high order bits of the 16 bit video memory address, used for screen refresh. The low order eight bit register is at index 0DH. The PR Register PR3 bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes bits 6 & 7 are forced to 0 regardless of this register's contents, while the lower order 8 bits are at index register 0DH.

7.7.15 Start Address Low Register Read/Write Port = 3?5H, Index = 0DH

BIT	FUNCTION
7 - 0	Start Address Low Byte

Bit(7:0)

The lower order eight bits of the 16 bit video memory address in VGA or 6845 modes.

9.7.16 Cursor Location High Register Read/Write Port = 3?5h, Index = 0Eh

BIT	FUNCTION
7 - 0	Cursor Location High Byte

Bit(7:0)

Cursor Address Upper Byte Bits.
The eight higher order bits of 16 bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0FH. In VGA mode, the PR Register PR3 bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, bits 6 and 7 are reserved, while bits 5 - 0 are the high order bits of the cursor.

7.7.17 Cursor Location Low Register Read/Write Port = 3?5, Index = 0FH

BIT	FUNCTION
7 - 0	Cursor Location Low Byte

Bit(7:0)

Cursor Address Lower Byte Bits.
The lower order eight bits of the 16 bit video memory address in VGA or 6845 mode.

7.7.18 Vertical Retrace Start Register Read/Write Port = 3?5, Index=10H

BIT	FUNCTION
7 - 0	Vertical Retrace Start (Lower eight bits)

Bit(7:0)

Vertical Retrace Start Pulse Lower Eight Bits.
The lower eight bits of the ten bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07H). In 6845 compatible mode, this register shows the high order six bits in positions 5 - 0 as the light pen read back value, and bits 6 an 7 are reserved. The lower order eight bits of the light pen read back register are at the index 11H. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3 (0) = 1.

7.7.19 Vertical Retrace End Register Read/Write Port = 3?5, Index = 11H

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3 - 0	Vertical Retrace End

This register is locked if the PR Register PR3(0)=1.

Bit 7

CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller index registers in the range of index 00H-07H. The line compare bit 4 in the Overflow Register (07H) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.
Selects DRAM refresh cycles per horizontal scan line.
0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.
0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4

Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by resetting (writing a 0 to) and internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

Bit(3:0)

Vertical Retrace End.
They specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan counter for "W" to the value of the Vertical Retrace Start Register. The 4 bit result is written in the Vertical Retrace End Register. In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of Light Pen Register.

7.7.20 Vertical Display Enable End Register Read/Write Port = 3?5, Index = 12H

BIT	FUNCTION
7 - 0	Vertical Display Enable End (Lower eight bits)

Bit(7:0)

Vertical Display Enable End Lower Eight Bits.
The eight lower bits of ten bit register that defines where the active display frame ends.
The programmed count is in scan lines minus 1. Bits 8 and 9 are in the Overflow Register (index 07H) at positions 1 and 6 respectively.

7.7.21 Offset Register Read/Write Port = 3?5, Index = 13H

BIT	FUNCTION
7 - 0	Logical Line Screen width

Bit(7:0)

Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:
Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K=2 in byte mode and K=4 in word mode.

7.7.22 Underline Location Register Read/Write Port = 3?5, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4 - 0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5

Count By 4 For Double word Access
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit(4:0)

Underline Location.
These bits specify the row scan counter value within a character matrix where under line is to be displayed. Load a value 1 less than the desired scan line number.

7.7.23 Start Vertical Blank Register Read/Write Port = 3?5, Index =15H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	Start Vertical Blank (Lower eight bits)

Bit(7:0)

Start Vertical Blank Lower Eight Bits.
The lower eight bits of the ten bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). The ten bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

7.7.24 End Vertical Blank Register Read/Write Port=3?5, Index=16H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	End Vertical Blank

Bit(7:0)

Vertical Blank inactive Count.
End Vertical Blank is an 8 bit value calculated as follows:
8 Bit End Vertical Blank value =
(value of Start Vertical Blank minus 1) + (value of Vertical Blank signal width in scan lines).

7.7.25 CRT Mode Control Register Read/Write Port = 3?5, Index = 17H

This register is locked if PR Register PR3(5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.
0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word Or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by 1 bit and the MSB of the address counter appears on the LSB. See the table below.
1 = Byte address mode.

MEMORY ADDRESS	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLEWORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE:
* See bit 5, defining address wrap. This table is only applicable when PR Register PR1 bits 7 and 6 equal zero, or PR16 bit 1 equals one.
The CRT Underline Location Register (index = 14H) bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) bit 6 controls addressing. See the table below:

CRT14H	CRT17H	ADDRESS
Bit 6	Bit 6	Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.
0 = In word address mode, this bit enables bit 13 to appear at MA0, otherwise bit 0 appears on MAO.
1 = Select MA15 for odd/even mode when 256KB of video memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2
0 = Character clock increments memory address counter.
1 = Character clock divided by 2 increments the address counter.

Bit 2

Horizontal Retrace Clock Rate Select For Vertical Timing Counter.
0 = Selects horizontal retrace clock rate
1 = Selects horizontal retrace clock rate divided by 2.

Bit 1

Select Row Scan Counter.
0 = Selects row scan counter bit 1 as output at MA14 address pin.
1 = Selects bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0

6845 CRT Controller compatibility mode support for CGA operation.
0 = Row scan address bit 0 is substituted for memory address bit 13 at MA13 output pin during active display time.
1 = Enable memory address pin 13 to be output at MA13 address pin.

7.7.26 Line Compare Register Read/Write Port = 3?5, Index = 18H

BIT	FUNCTION
7 - 0	Line Compare (lower eight bits)

Bit(7:0)

Line Compare Lower Eight Bits.
Lower eight bits of the ten bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared.

7.8 GRAPHICS CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

NOTE:
1. Reserved bits should be set to zero.

7.8.1 Graphics Index Register, Read/Write Port = 3CE

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Graphics Address Bits

Bit(7:4)

Reserved.

Bit(3:0)

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

7.8.2 Set/Reset Register, Read/Write Port 3CF, Index = 00

BIT	FUNCTION
7 - 4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined below:
0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE:
*The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05H) bit 1 and bit 0.

7.8.3 Enable Set/Reset Register, Read/Write Port = 3CF, Index = 01

BIT	FUNCTION
7 - 4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Enable Set/Reset Register (Index 00H).

0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00H) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.
1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00H), and the respective memory map is written with the Set/Reset Register value.

7.8.4 Color Compare Register, Read/Write PORT 3CF, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Color Compare.
The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a 1 is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05H), data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

7.8.5 Data Rotate Register, Read/Write Port = 3CF, Index = 03

BIT	FUNCTION
7 - 5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count 2 Bit 2
1	Rotate Count 1 Bit 1
0	Rotate Count 0 Bit 0

Bit(7:5)

Reserved.

Bit(4:3)

Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05H) is defined as follows.

BIT 4	BIT 3	FUNCTION
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches

Bit(2:0)

Rotate Count.
It specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05H).

7.8.6 Read Map Select Register, Read/Write Port = 3CF, Index = 04

BIT	FUNCTION
7 - 2	Reserved
1	Map Select 1
0	Map Select 0

Bit(7:2)

Reserved.

Bit(1:0)

Map Select.
These bits select memory map in system read operations. It has no effect on color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained maps 0 & 1 or value 10b or 11 to select the chained maps 2 & 3. Map read is defined as shown below.

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

7.8.7 Graphics Mode Register, Read/Write Port = 3CF, Index = 05

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7

Reserved.

Bit 6

256 Color Mode.
0 = Enables bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID6, VID7) are determined by bits 2 and 3 of the Color Select Register located at index = 14H within the Attribute Controller.
1 = Load video shift registers to support 256 color mode.

Bit 5

Shift Register.
Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.
0 = Map 0 - Map 3 data is placed into shift registers for normal operations.
1 = For CGA graphics mode compatibility, even numbered bits from all of the maps are shifted out of even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.
0 = normal
1 = CGA compatible odd/even system access mode. Sequential addressing as defined by bit 2 of the memory mode register (index = 04H) in the Sequencer Register. Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3

Read Mode.
0 = System reads data from memory maps selected by Read Map Select Register (index 04H). This setting will have no effect if bit 3 of the Sequencer Memory Mode Register = 1.
1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved.

Bit(1:0)

Write Mode.
The following table defines the four write modes.

BIT 1	BIT 0	WRITE MODE
0	0	Write Mode 0. If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	Write Mode 1. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	Write Mode 2. Memory maps (3:0) are filled with the 8-bit value of the corresponding CPU data bits (3:0). The 32 bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	Write Mode 3. Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

7.8.8 Miscellaneous Register, Read/Write Port = 3CF, Index = 06

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bit(7:4)

Reserved.

Bit(3:2)

Memory Map 1, 0
Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0H-BFFF:FH	128KB
0	1	A000:0H-AFFF:FH	64KB
1	0	B000:0H-B7FF:FH	32KB
1	1	B800:0H-BFFF:FH	32KB

Bit 1

Odd/Even Mode.
0 = CPU address bit A0 is the memory address bit MA0.
1 = CPU address bit A) is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode
This bit is programmed the same way as bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selects.
1 = Graphics mode selected.

7.8.9 Color Don't Care Register, Read/Write Port 3CF, Index = 07

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Memory Map Color Compare Operation.

0 = Disable color compare operation.
1 = Enable color compare operation.

7.8.10 Bit Mask Register, Read/Write Port = 3CF, Index = 08

BIT	FUNCTION
7 - 0	Bit Mask

Bit(7:0)

Bit mask operation applies simultaneously to all the four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

7.9 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CO	——	Index Register
3CO	00-0F	Palette Registers
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

NOTES:
1. Each attribute data register is written at 3C0 and register data is read from address 3C1.
2. Reserved bits should be set to zero.
3. ? " Value is controlled by Bit 0 of the Miscellaneous Output register and is programmed as shown below.

0 = B in Monochrome Modes and
1 = D in Color Modes

7.9.1 Attribute Index Register, Read/Write Port = 3C0

BIT	FUNCTION
7 - 6	Reserved
5	Palette Address Source
4 - 0	Attribute Address Bits

Bit(7:6)

Reserved.

Bit 5

Palette Address Source.
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 - 0FH).
1 = Enable internal color palette and normal video translation.

Bit(4:0)

Attribute Controller Index Register Address Bits

NOTE:
The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 3?A) clears the flip-flop and selects the Address Register, which is read thru address 3C1 and written at address 3C0. Once the Address Register has been loaded with an index, the next write operation to 3C0 will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address hex 3C0, but does not toggle for reads to address 3C1.

7.9.2 Palette Registers (00-0F Hex), Read Port 3C1/Write Port 3C0

BIT	FUNCTION
7 - 6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:6)

Reserved.

Bit(5:0)

Palette Pixel Colors.
They are defined as follows:
0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the table below.

Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

7.9.3 Attribute Mode Control Register Read Port 3C1/Write Port 3C0, Index = 10

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7

VID5, VID4 Select
0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14H) bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6

Pixel Width
0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.
1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility
Line Compare in the CRT Controller.
0 = A Line compare will have no effect on the PEL Panning Register.
1 = Allows a successful line compare to disable the PEL Panning Register and also bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4

Reserved.

Bit 3

Background Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code.
Set this bit to zero for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes

Bit 0

Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

7.9.4 Overscan Color Register Read Port 3C1/Write Port 3C0, Index = 11

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:0)

Overscan/Border Color.
They determine the overscan or border color. For monochrome display, this register is set to 0. Border colors are set as shown above.

7.9.5 Color Plane Enable Register Read Port 3C1/Write Port 3C0, Index = 12

BIT	FUNCTION
7 - 6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3 - 0	Enable Color Plane

Bit(7:6)

Reserved.

Bit(5:4)

Video Status Control.
These bits select 2 out of 8 color outputs which can be read by the Input Status Register 1 (port = 03?A) bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit(3:0)

Color Plane Enable.
0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

7.9.6 Horizontal Pel Panning Register Read Port 3C1/Write Port 3C0, Index = 13

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Horizontal PEL Panning

Bit(7:4)

Reserved.

Bit(3:0)

Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to 3 position pixel shift can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Character	8 dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7.9.7 Color Select Register Read Port 3C1/Write Port 3CO, Index = 14

BIT	FUNCTION
7 - 4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bit(7:4)

Reserved.

Bit(3:2)

Color Value MSB.
Two most two significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6

Bit(1:0)

Substituted Color Value Bits.
These bits can be substituted for VID5 an VID4 output by the Attribute Controller palette registers, to create eight bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10H).

7.10 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting PR Register PR2(6) = 1.

2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting PR Register PR2(7) = 1.

3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0 = B in Monochrome Modes
1 = D in Color Modes

7.10.1 Hercules/MDA Mode Control Register, MDA Operation Write Only Port = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode. If Bit 1=1 and Port 3BFH bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5

Enable Blink.
0 = Disable Blinking
1 = Enable Blinking

Bit 4

Reserved.

Bit 3

Video enable.
0 = Video Disable
1 = Video activated

Bit 2

Reserved.

Bit 1

Port 3BFH enable.
0 = Prevents setting of Port 3BF bit 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFh bit 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode. Should be 1.
0 = High resolution disabled.
1 = High resolution is enabled.

7.10.2 Hercules Registers

The Hercules Mode Register is a 2-bit write only register located at I/O port address 3BF. It affects the device operation only in the 6845 mode. The enable mode register located at the address 3B8 overrides the write port 3BF functions defined by its bits 0 and 1. The associated details are shown below.

7.10.3 Enable Mode Register 3B8

BIT	FUNCTION
7	Display Memory Page Address Graphics Mode
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BF Bit 0 Override
0	High Resolution Mode = 1

Bit 7

Display Memory Page Address In Graphics Mode.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit (6:2,0)

Not Applicable.

Bit 1

Port 3BF Bit 0 Override.
0 = Prevents setting of Port 3BF bit 0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BF bit 0 to switch for the alpha or graphics mode selection.

7.10.4 Hercules Compatibility Register Write Only Port = 3BFH

BIT	FUNCTION
7 - 2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)

Reserved.

Bit 1

Upper Memory Page Address.
Enable Mode Control Register (3B8) bit 7 selects the displayed memory page address in the graphics mode. When it is reset, bit 1 prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.
0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics.
Allows the Enable Mode Register (3B8) bit 1 to override.
0 = Alpha mode display.
1 = Graphics modes may be displayed.

7.10.5 Color CGA Operation Register, Write Only Port = 3D8

BIT	FUNCTION
7, 6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bit (7:6)

Reserved.

Bit 5

Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4

B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3

Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = B/W mode enabled.

Bit 2

B/W or Color Display Mode.
0 = Color Mode Selected.
1 = B/W Mode Selected.

Bit 1

Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = graphics mode (320 by 200) activated.

Bit 0

(40 by 25) or (80 by 25) Text Mode Selection.
0 = 40 by 25 alpha mode enabled.
1 = 80 by 25 alpha mode activated.

7.10.6 CGA Color Select Register Write Only Port = 3D9

BIT	FUNCTION
7, 6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bit (7:6)

Reserved.

Bit 5

320 by 200 Color Set Select for the CGA 2 bits per pixel.
0 = Background, green, red, brown colors.
1 = Background, cyan, magenta, white colors.

Bit 4

Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = enable alternate color set in graphics mode.

Bit 3

Border Intensity.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 2

Red Border/Background
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects red border color.
320 by 200 Graphics Mode.
1 = Selects red background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 1

Green Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

Bit 0

Blue Border/Background.
border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Select blue background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

7.10.7 CRT Status Register MDA Operation, Read Only Port = 3BA

BIT	FUNCTION
7	VSYNC Inactive
6 - 4	Reserved
3	B/W Video Enabled
2 - 1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.
0 = Indicates the raster is in vertical retrac e mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bit (6:4)

reserved.

Bit 3

B/W Video Status.
0 = B/W Video disabled.
1 = B/W Video enabled.

Bit 2 - Bit 1

Reserved.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

7.10.8 CRT Status Register CGA Operation, Read Only Port = 3DA

BIT	FUNCTION
7 - 4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bit (7:4)

Reserved.

Bit 3

Vertical Retrace.
0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode.

Bit 2

Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open

Bit 1

Light Pen Latch.
0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking active; Display Enable is inactive.

7.10.9 AT&T/M24 Register, Write Only Port = 3DE

This is a write only, 8-bit register located at address 3DE. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting bit 7 in PR Register 2 (PR2).

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5, 4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in-color text modes.
1 = Underline attribute selects white underlined foreground.

Bit (5:4)

Reserved.

Bit 3

Page Select.
Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B800:0H (16 KB length).
1 = Display memory address starts at BC00:0H (16 KB length).

Bit 2

Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or Non-IBM Graphics Mode. 400 line mode.
A 400 line monitor is required for this mode.
0 = 200 line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400 line graphics.

7.11 WD90C10 PR REGISTERS

REGISTERS	RW	MONOCHROME	COLOR
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
Reserved 3X5.31- 3X5.3F	RW	3B5.31 - 3B5.3F	3D5.31 - 3D5.3F
CNF Configuration (loaded during power-on)	-----	-----	-----
PR20 Unlock Sequencer Extended Registers	W	3C5.06	3C5.06
PR21Display Configuration and Scratch Pad	RW	3C5.07	3C5.07
PR30 Memory Interface and FIFO Control	RW	3C5.10	3C5.10
PR31 System Interface Control	RW	3C5.11	3C5.11
PR32 Miscellaneous Control 4	RW	3C5.12	3C5.12

NOTE:
All of the PR Registers may be read/write protected.

TABLE 7. PR REGISTERS SUMMARY

The WD90C10 has additional features that enhance the performance and functions of the Western Digital Imaging PVGA1A, introduced earlier, and the basic VGA subsystem. To accomplish this, the WD90C10 architecture is optimized with additional I/O registers.

The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

NOTES:

1. The designation 3?5 means that the register is mapped into either 3B5 in monochrome mode or 3D5 in color modes.

2. PR register notation - XXX.YY where XXX is the data port address and YY is the register index e.g. 3CF.0F implies 0F--3CEH (Select Index register) followed by (Data byte) -- 3CF (Data Port).

Registers PR0 through PR4 and PR11 through PR17 are normally locked. They are write protected at power-up by the hardware reset. In order to load those registers, the appropriate unlock register PR5 or PR10 must be loaded first with binary XXXXX101; a register remains unlocked until any other value is written to the unlocked register. Registers PR0 through PR5 are readable only if PR4 bit 1 = 0. Registers PR10 through PR17 are read protected at power up by hardware reset. In order to read registers PR10 through PR17 load PR10 with 1XXX0XXX. The register remains readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them would show data to be FFH. Setting PR4 bit 1 to 1 does not read protect registers PR10 through PR17. All PR registers are set to 0 at power on reset except where noted.

7.11.1 Address Offset Registers PROA & PROB

PROA - Address Offset Register A
Read/Write Port = 3CF, Index = 09

BIT	FUNCTION
7	Reserved
6 - 0	Primary Address Offset Bits

PROB - Address Offset Register B
Read/Write Port = 3CF, Index = 0A

BIT	FUNCTION
7	Reserved
6 - 0	Alternate Address Offset Bits

The WD90C10 can control up to 512 Kbytes of display memory. However, DOS only assigns 128 Kbytes total memory space for display memory, which starts at A0000H and ends at BFFFFH. To help VGA to reach the memory beyond this range, the WD90C10 has two CPU address offset registers PROA and PROB which can be used to support more than 128 Kbytes of linear display memory address space.
The contents of PROA (bit 6:0) or PROB (bit 6:0) are always added to the CPU address A(18:12) before they are translated to display memory address. This can be thought of as segment register DS and ES in the 8088/80X86 architecture, PROA and PROB will then provide 4 Kbyte segmentation of the display memory. (Increment PROA or PROB by one of its equivalents to jump from a 4 Kbyte segment to another 4 Kbyte segment of the display memory.)
PROA and PROB are all set to zero value at power on reset. There are two ways to control whether PROA or PROB get added into CPU address.

- **Sequencer Extension Register 3C5 (index 11) bit 7 = 0.**

PROA is the primary offset register being added with the CPU address. PR1, bit 3 enables PROB which becomes the secondary offset register. If PR1, bit 3 = 1 and Graphics Controller index 6, bits 3:2 = 00b, A000:0 for 128K, then PROA will offset the CPU address from B000:0H to BFFF:FH while PROB offsets the CPU address from A000:0H to AFFF:FH. If PR1, bit 3 = 1 and Graphics Controller index 6, bits 3:2 = 01(A000:0H for 64K), then PROA will offset the CPU address from A800:0H to AFFF:FH while PROB offsets the CPU address from A000:0H - A7FF:FH.

- **Sequencer extension register 3C5 (index 11) bit 7 = 1.**

Both PROA and PROB are enabled. A CPU memory write will select PROB as the offset register. Otherwise, PROA is selected as the offset register.

7.11.2 PR1 - Memory Size, Read/Write Port = 3CF, Index = 0B

BIT	FUNCTION
7, 6	Memory Size Select
5, 4	Reserved
3	Enable Alternate Address Offset Register PR0B
2	16-Bit Video Memory
1	ROM Data Width
0	BIOS ROM Map Out

This register is 8 bits wide. Bits PR1 (1:0) are latched internally at power on reset from the corresponding memory data bus pins MD(10), MD(0) using either pull-up or pull-down external resistors. Pull-up resistors on MD(10), MD(0) cause PR1(1:0) bits to be latched low.

Bits 7, 6

Memory Size.

These two bits control memory size and memory organization. They both must be set to reflect the amount of memory installed. These bits in conjunction with PR0A, PR0B, PR16 (1) select the way memory is mapped into the CPU address space. IF PR16 (1) is set to 1, the memory mapping will be set identical to the IBM VGA regardless of PR1 (7), PR1 (6).

The WD90C10 supports 512 Kbytes (four 256K by 4 DRAM) display memory. This makes it possible to support some extended graphics modes such as 640 by 480 by 256 colors and 800 by 600 by 256 colors.

The setting of these two bits will be overwritten by PR16 (1). When PR16(1) is set to 1, memory mapping will be identical to the IBM VGA (equivalent to PR1 (7,6) = 00).

The following tables list the different settings on these two bits for different memory organizations.

GRAPHICS MODE RAM ADDRESSING:

PR1(7) **PR1(6)**

0 0 256K TOTAL;64K/PLANE; IBM VGA MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(16)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(4)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(3)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(2)	A(0)	CA(0)	A(16) or XRN(5)	CA(15) or CA(13)	A(14)	CA(12)
MA(1)	See note, page 61					
MA(0)	See note, page 61					

PR1(7) **PR1(6)**
0 1 256K TOTAL;64K/PLANE; WD90C10 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(16)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(4)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(3)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(2)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

PR1(7) **PR1(6)**
1 1 RESERVED
1 0 RESERVED

NOTES:
1. A(19:0) are WD90C10 internally modified system Addresses.
2. CA(17:0) are CRT Controller Character Address Counter Bits.
3. XRN(5) is Miscellaneous Output Register 3C2H, inverted bit 5. This bit selects the displayed page in chained modes. XRN(5) is selected as MA(2) if Graphics Register 6 bit 3 or bit 2 = 1.
4. CA(13) is selected as MA(2) if CRTC Mode Register 17 bit 5 = 0.
5. For two 256K x 4 DRAMs, MA(1) and MA(0) are used as memory plane select for 256 Kbytes.

MA(1), MA(0) = 00 select plane 0
01 select plane 1
10 select plane 2
11 select plane 3

Bits 5, 4

Reserved

Bit 3

Enable Alternate Address Offset Register PROB

Bit 2

Enable 16 bit bus for Video Memory
When set to 1, MEMCS16 will be active low for all of the video memory cycles.

Bit 1

When set to 1 and bit 0=0, the BIOS ROM has a 16 bit data path from C000:0 - DFFF:FH (ROM16 will respond to ROM access). Otherwise, the BIOS ROM has an 8 bit data path.

A pull down resistor on MD(10) will set this bit to 1 after power-on reset. This bit can also be set to 1 by an I/O write to PR1 register if the CNF(1) = 1 (2 ROMs).

Bit 0

If set to 1 the BIOS ROM is mapped out. Pull-up resistor latches 0 after power up. A pull-up on MD(0) sets this bit to 0 at power on reset.

7.11.3 PR2-Video Select Register, Read/Write Port = 3CF, Index = 0C

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4, 3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7

Enable AT&T/M24 Register & mode

Bit 6

0: VGA or EGA mode
1: Non-VGA (6845) mode

Bit 5

Character Map Select. The following functions are overridden by setting PR15(2). This bit in conjunction with PR2(2) and bit 3 of the attribute code, enables character maps from planes 2 or 3 to be selected per the table below:

PR2(5)	PR2(2)	ATT(4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE:
Setting PR15(2) = 1 i.e. selecting page mode addressing overrides plane selected table shown above.

Bit(4:3)

Character clock period control

0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132 character text mode only)
1	0	6 dots (for text modes only)
1	1	6 dots (for text modes only)

NOTE:
The character clock period control functions have no effect in graphics modes.

Bit 2

Underline and character map select. Setting this bit to 1 enables underline for all odd values of attribute codes, e.g. Programming 1 gives blue underline. It overrides the background color function of the attribute code bit 3, which is forced to 0. Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1

This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) is set to 1. When CNF(3) is set to 0, it locks the internal video clock select multiplexer.

Bit 0

Forces horizontal sync timing clock of the CRTC to VCLK.
Uses VCLK when sequencer register 1 bit 3 is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

7.11.4 PR3 - CRT Lock Control Register Read/Write Port=3CF, Index = 0D

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

7.11.5 WD90C10 CRT Controller Register Locking

Register locking is controlled by 4 bits. They are PR3 (5,1,0) and 3?5.11(7) (i.e. IBM Vertical Retrace End Register bit 7 controlled by index register 11). 11 When bit 7 is 1, CRT controller registers (R0-7) are write protected per VGA definition. For more information on the five groups, and their locking schemes, refer to the sections below.

- **Group 0**

These registers are locked if PR3(5)=1 OR 3?5.11(7)=1
CRT controller register 00 --Horizontal Total Characters per scan
CRT controller register 01 --Horizontal Display Enable End
CRT controller register 02 --Start Horizontal Blanking
CRT controller register 03 --End Horizontal Blanking
CRT controller register 04 --Start Horizontal Retrace
CRT controller register 05 --End Horizontal Retrace

- **Group 1**

These registers are locked if PR3(1)=0 AND 3?5.11(7)=1
CRT controller register 07(Bit6) - Vert. Display Enable End bit 9
CRT controller register 07(Bit1) - Vert. Display Enable End bit 8

- **Group 2**

These registers are locked if PR3(0)=1 OR 3?5.11(7)=1
CRT controller register 06 --- Vertical Total
CRT controller register 07(Bit7) ---Vertical Retrace Start bit 9
CRT controller register 07(Bit5) ---Vertical Total bit 9
CRT controller register 07(Bit3) ---Start Vertical Blank bit 8
CRT controller register 07(Bit2) ---Vertical Retrace Start bit 8
CRT controller register 07(Bit0) ---Vertical Total bit 8

- **Group 3**

These registers are locked if PR3(0)=1
CRT controller register 09(Bit5) ---Start Vertical Blank bit 9
CRT controller register 10 ---Vertical Retrace Start
CRT controller register 11 [Bits(3:0)] ---Vertical Retrace End
CRT controller register 15 ---Start Vertical Blanking
CRT controller register 16 ---End Vertical Blanking

- **Group 4**

This register is locked if PR3(5)=1
CRTC mode control register 17(Bit2) ---Selects divide by two vertical timing

Bit7

Lock VSYNC polarity, as programmed in 3C2 bit 7

Bit 6

Lock HSYNC polarity, as programmed in 3C2 bit 6

Bit 5

Lock horizontal timing.
Locks CRTC registers of Group 0 and 4.
Prevents attempt by applications software to unlock Group 0 registers by setting 3?5.11 bit 7=0

Bit 4

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 9 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (17).

Bit 3

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (16).

Bit 2

Cursor start, stop, preset row scan, and maximum scan line address registers values multiplied by two.

Bit 1

1 = Prevents attempt by applications software to lock registers of Group 1 by its setting 3?5.11 bit 7=1.

Bit 0

Lock vertical timing. 1 = Locks CRTC registers of Groups 2 and 3. Overrides attempt by applications software to unlock Group 2 registers by its setting 3?5.11 bit 7=0.

7.11.6 PR4- Video Control Register Read/Write Port=3CF, Index = 0E

The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAMDAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLNK}}$ / Display Enable
6	PCLK=VCLK
5	Tri-state Video Outputs
4	Tri-state Memory Control Outputs
3	Override CGA Enable Video bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Ext 256 color Shift Register control

Bit 7

This bit controls the output signal $\overline{\text{BLNK}}$. Normally in the VGA mode, $\overline{\text{BLNK}}$ is used by the external video DAC to generate blanking. If this bit = 1, the $\overline{\text{BLNK}}$ output supplies a display enable signal. A choice of two types of display enable timings can be selected, and is determined by PR15(1).

Bit 6

Select PCLK equal to VCLK.
0=PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1=PCLK is always the non-inverted VCLK input clock.

Bit 5

Tri-state the outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLNK}}$.

Bit 4

Tri-state the memory control outputs. The memory address bus MA(8:0), and all DRAM control signals are tri-stated when this bit is set to 1.

Bit 3

Overrides the CGA "enable video" bit 3 of mode register 3D8, only in 80 x 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2

Lock Internal palette and overscan registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode. It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3CO/3C1 change to write-only mode if the EGA compatibility bit is set. In VGA mode (PR(4) bit 1 is zero) 3C0 register is read/write while 3C1 register is read only, per the Attribute Controller registers definitions.

Bit 0

Extended Shift Register Control.
This register should only be used with 4 DRAMs to configure the video shift register for extended 256 color modes.

7.11.7 PR5 - General Purpose Status Bits Read/Write Port=3CF, Index = 0F

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PRO-PR4 Unlock
1	PRO-PR4 Unlock
0	PRO-PR4 Unlock

Bits (2:0) are READ/WRITE bits and cleared to 0 by reset. They provide lock or unlock capability for PR registers PR0 through PR4 like the PVGA1A. The PR0 - PR4 registers are unlocked when "X5Hex" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register bits 4 through 8. Setting PR(4) bit 1 to 1, read protects registers PR0 - PR5.

Bit 7 CNF(7) [READ ONLY]
Bit 6 CNF(6) [READ ONLY]
Bit 5 CNF(5) [READ ONLY]
Bit 4 CNF(4) [READ ONLY]
Bit 3 CNF(8) [READ ONLY]

Bits (2:0)

READ/WRITE bits and cleared to 0 by reset. They control writing to PR registers PR0-PR4 as follows:

2 1 0	PR0-PR4
0 X X	Write protected
X 1 X	Write protected
X X 0	Write protected

7.11.8 PR10 Unlock PR11-PR17 Read/Write Port = 3?5, Index = 29

This register is READ/WRITE and cleared to 0 by reset. PR10 can be loaded if it contains XXXXX101, and can only be read if it has 1XXX0XXX. Bits (7,3), Bits(6:4), and Bits (2:0) control access to PR registers PR10-PR17. Bits 7 and 3 enable register read operation for PR10 - PR17. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 - PR17.

BIT	FUNCTION
7	PR10-PR17 - Read Enable Bit 1
6 - 4	PR10(6:4) - Scratch Pad
3	PR10-PR17 - Read Enable Bit 0
2 - 0	PR11-PR17 - Write Enable

BIT7	BIT3	PR10-PR17
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

BIT2	BIT1	BIT0	PR11-PR17
0	X	X	Write protected
X	1	X	Write protected
X	X	0	Write protected
1	0	1	Write Enabled

BIT6	BIT5	BIT4	PR10(6:4)
0	X	X	Scratch pad
X	1	X	Scratch pad
X	X	0	Scratch pad
1	0	1	Reserved for manufacturing test.

7.11.9 PR11 EGA Switches Read/Write Port = 3?5, Index = 2a

The EGA switch configuration details are stored in the PR11 register bits.

BIT	FUNCTION
7	EGASW4
6	EGASW3
5	EGASW2
4	EGASW1
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4)

EGA CONFIGURATION SWITCHES SW4-SW1. These bits are READ/WRITE and latched internally at power-on-reset from corresponding memory data bus pins MD(15:12), provided with either pull-up or pull-down external resistors. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. These bits can be read as bit 4 of port 3C2 if the EGA COMPATIBILITY BIT [PR4(1)] has been set to 1. Selection of the bit to be read is determined by bits 3 & 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE 3C2 bit 3	3C2 bit 2	READ 3C2 bit 4
0	0	PR11(7) [=EGA SW4]
0	1	PR11(6) [=EGA SW3]
1	0	PR11(5) [=EGA SW2]
1	1	PR11(4) [=EGA SW1]

PR11 Bits 3 through 0 are READ/WRITE and cleared to 0 at power on reset.

Bit 3

Select EGA Emulation on a PS/2 (VGA-compatible, analog) display.

Bit 2

Lock Clock Select. This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

Bit 1

Lock Graphics Controller/Sequencer screen control. Setting PR11(1) to 1 prevents modification of the following bits in the Graphics controller as well as the Sequencer:

Graphics controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by these graphics controller and sequencer bits are locked by setting PR11 bit 1 to 1, they appear unlocked to the system processor during read operation.

Bit 0

Lock 8/9 dots. Setting this bit to 1 prevents modification of clocking mode sequencer register 3C5.01 bit 0. Although 8 or 9 character timing is locked by setting PR11 bit 0 to 1, the 3C5.01 bit 0 appears unlocked to the system processor during reads.

7.11.10 PR12 Scratch Pad Read/Write Port = 3?5, Index = 2b

BIT	FUNCTION
7 - 0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power up.

7.11.11 PR13 Interlace H/2 Start Read/Write Port = 3?5, Index = 2C

BIT	FUNCTION
7 - 0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1. All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00):

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE:
In the above expression, HRD = Horizontal Retrace Delay, determined by bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

7.11.12 PR14 Interlace H/2 End Read/Write Port = 3?5, Index = 2d

Bits 4 through 0 are unaffected by hardware reset and undefined at power up. Bits 7 through 5 are cleared to 0 by reset.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4 - 0	Interlaced H/2 Start

Bit 7

Enable IRQ. This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to 0. This bit should not be set to 1 in MICRO CHANNEL operation.

Bit 6

Vertical double scan. This bit should be set to 1 when emulating EGA on PS/2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed line counter and row scan counter to be clocked by divide-by-two horizontal timing if vertical sync polarity (3C2 Bit 7=0) is programmed to be positive. Therefore, the relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is:

N=2(n+1)

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5

Interlaced mode.
Setting this bit to 1 selects interlaced mode. The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000.
Line compare and double scan are not supported.

Bits (4:0)

Interlaced H/2 end bits (4:0). Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

7.11.13 PR15 Miscellaneous Control 1 Read/Write Port = 3?5, Index = 2e

BIT	FUNCTION
7	Read 46E8 Enable
6	Reserved
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable reading port 46E8H. This bit is functional only if AT BUS architecture [CNF(2)=1] is selected. Setting this bit to 1 enables I/O port 46E8H to be read, regardless of the state of its own bits 3 and 4 and of port 102 bit 0 (sleep bit). Only bits (4:0) of port 46E8H are readable; bits (7:5) are 0.

Bit 6

Reserved.

Bit 5

Latched VCLK1 and VCLK2. This bit is used only if CNF(3) = 1 which configures the VCLK1 and VCLK2 pins as outputs. Setting This bit to 1 causes outputs VCLK1 and VCLK2 to equal bits 2 and 3 of I/O write register (Miscellaneous output register) at 3C2H respectively.

Bit 4

Select MCLK as video clock. Setting this bit to causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.

Bit 3

Interlaced Compatibility. This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to 1 if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to 1causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of leading edge, as generated for VGA timing.
Setting this bit to 1 also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing. Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory by 30-40%. Set this bit to 1 of 132 character mode timing is selected (see description of PR2). Setting this bit to any alpha mode overrides the character map select functions of PR2(2) and PR2(5). When this bit is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight, 8K memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by bits (2:0) of this register while the map selection is determined by the bits (4:3). A pair of adjacent 8K character maps in planes 2 and 3, (adjacent in the sense that they have the same addressing) may be selected by bit 3 of the attribute code.
The Character attribute bit 3, in conjunction with bits 3 and 4 of the Character Map Select register (3C5.03), determine a character map from either Plane 2 or Plane 3 as shown by the table below.

3C5.03 BIT4	3C5.03 BIT 3	ATT BIT3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

Note:
The above Character Map Select functions override the functions override the functions of PR2(5) and PR2(2).
This bit must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select. This bit is used to select between two types of Display Enable timings available at output pin BLNKN if PR4(7)=1. If PR4(7)=0, this bit has no effect.

0=BLNKN supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = BLNKN supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable border. Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

7.11.14 PR16 Miscellaneous Control 2 Read/Write Port = 3?5, Index = 2f

BIT	FUNCTION
7	External reg. 46E8H lock
6	CRTC Address count Width bit 1
5	CRTC Address Count Width bit 0
4	CRTC Address Counter Offset bit 1
3	CRTC Address Counter Offset bit 0
2	Enable Odd/Even Page bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit (7)

Lock External 46E8H register.

Setting this bit to 1 causes $\overline{\text{EBROM}}$ output to be forced high (Inactive) during I/O writes to port 46E8H. This bit has no effect on loading the internal port 46E8H.

Bit (6:5)

CRTC Address Counter Width.

Power on reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512KB or 1024KB of video memory in which CRT controller is limited to only 64K or 128K locations. Bit PR16(6) should be set 1 to ensure VGA and EGA compatible operation of the address counter, limited to 64 K locations. The following table shows details:

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256KB
0	1	128K
1	X	64K

Bit (4:3)

CRTC Address Counter Offset
Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively, and the 2-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2

Enable Page Bit for Odd/Even
This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory, and setting 3C5.04(3) to 0 to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size bits PR1(7:6).

Bit 1

VGA Memory Mapping
Setting this bit to 1, selects 256KB IBM VGA Mapping, regardless of the Memory Size bits PR1(7:6).

Bit 0

Lock RAMDAC write strobe (3C6H - 3C9H) Programming this bit to 1 causes output WPLTN to be forced to 1 disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C10 is also protected from the modification but may still be read at the port 3C7h. For normal operation, program this bit to 0.

7.11.15 PR17 Miscellaneous Control 3 Read/Write Port = 3?5, Index = 30

BIT	FUNCTION
7 - 4	Reserved
3	Map out 4K of BIOS ROM
2	Enable 64K BIOS ROM
1	Hercules Compatibility
0	Map out 2K of BIOS ROM

Bit (7:4)

Reserved.

Bit (3)

Map out 4K of BIOS ROM.
Setting this bit to 1 disables access of the BIOS ROM in the system address range C600:0H - C6FF:FH. Power on reset sets this bit to 0.

Bit (2)

Enable 64K BIOS ROM.
Setting this bit to 1 enables access of the BIOS ROM in the system address range C000:0H - CFFF:FH. Power on reset sets this bit to 0.

Bit (1)

Setting this bit to a 1 locks Hercules compatibility register (I/O port 3BF). Power on reset sets this bit to 0.

Bit (0)

Map out 2K of BIOS ROM.
Setting this bit to 1 disables access of the BIOS ROM in the system address range C600:0H - C67F:FH.
Power on reset sets this bit to 0.

7.11.16 PR20 3C5 Index 6: Unlock Sequencer Extended Registers (Reset State = Locked)

A value of X1X01XXXX (48H) must be loaded to allow R/W of the Sequencer Extended Registers. When the extended registers are locked, then the Sequencer index will be readable as three bits only. When unlocked, the Sequencer index reads as a full eight bits.

7.11.17 PR21 3C5 Index 7: Display Configuration Status and Scratch Pad Bits

This register provides a convenient location for determining the current VGA configuration state. This information is needed for many of the BIOS calls.

BIT	FUNCTION
7 - 4	Scratch Pad Bits
3	Status of 3C2 bit 0
2	Status of PR2 bit 6
1	Status of PR4 bit 1
0	Status of PR5 bit 3

Bits 7:4

Read/write scratch pad for any BIOS status data that may need to be saved. Reset state is 1111.

Bit 3

Reflects the setting of the I/O address select bit in the Miscellaneous Output Register.
A 1 means CGA (3Dx) addresses have been selected by this read-only bit, while a 0 means MDA (3Bx) addresses have been selected.

Bit 2

Reflects the setting of the VGA/6845 select bit in PR2 (3CF index C).
A 1 means 6845 compatibility has been selected by this read-only bit, while a 0 means VGA or EGA compatibility has been selected.

Bit 1

Reflects the setting of the VGA/EGA select bit in PR4 (3CF index E).
A 1 means EGA compatibility has been selected by this read-only bit, while a 0 means VGA was selected.

Bit 0

Reflects the setting of the Analog/TTL status bit in PR5 (3CF index F).
The video BIOS may define this as a 0 meaning an an analog monitor was selected by this read-only bit, while a 1 means a TTL-type monitor was selected.

7.11.18 PR30 3C5 Index 10 Memory Interface and FIFO Control Register (See Note)

This register controls display memory data width and its bandwidth. All of the bits are reset to zero at power on reset.

BIT	FUNCTION
7, 6	Reserved
5	8- or 16-bit Memory data path
4	Disable 16-bit CPU interface
3	Enable write buffer extension
2	4 or 8 level FIFO
1, 0	Display memory bandwidth

Bits (7,6)

Reserved

Bit 5

This bit must be set to zero. This bit is reserved for the WD90C11 and WD90C12.

Bit 4

When set to 1, the 16-bit CPU interface is unchained mode is disabled. This is for debug only and should be set to 0 under normal conditions.

Bit 3

When set to 1 enables the write buffer extension. This will make the write buffer effectively two deep. Should be set to 1 under normal conditions.

Bit 2

When set to 1, will set the internal FIFO to 4 levels deep. Otherwise the FIFO is 8 levels deep. In general, when 16-bits display memory is enabled (bit 1 of this register is set to 1), then the 4 level deep FIFO is recommended. In "Super VGA" mode (800 by 600 by 256 color) an 8 level deep FIFO will be required.

Bit 1, 0

These two bits can be used to adjust the display memory bandwidth. In general it is recommended that these two bits be set to 01 to accommodate most applications. These bits have no effect in any text mode. They are locked into 00 internally when a text mode is set.

00	FIFO requests for memory cycle when FIFO is:	one level empty
01	FIFO requests for memory cycle when FIFO is:	two levels empty
10	FIFO requests for memory cycle when FIFO is:	three levels empty
11	FIFO requests for memory cycle when FIFO is:	four levels empty

NOTE:
PR30 is reserved for next generation WD90C10.

7.11.19 PR31 3C5 Index 11: System Interface Control (Reset State = 00H)

This register provides the control bits for the system interface. This register should be set during the Post initialization routines of the VGA BIOS. The reset state is 100% IBM VGA compatible. Bit 7 will be used during some of the enhanced display modes.

BIT	FUNCTION
7	Read/Write Offset Enable
6	Turbo Mode for Blanked Lines
5	Turbo Mode for Text
4	CPU Read RDY release Control 1
3	CPU Read RDY release Control 0
2	Enable Write Buffer
1	Enable 16-bit I/O Operation on Attribute Controller
0	Enable 16-bit I/O Operation on CRTC, Sequencer and Graphics Controller

Bit 7

When set to 1, the offset register PR0-A will be added to the CPU address for read cycles, while PR0-B will be added for write cycles. When cleared to 0, the offset registers operate the same as in the PVGA1B. Refer to PR0A and PR0B definitions.

Bit 6

When set to 1, system performace is improved by 10% by removing extra memory cycles on blank lines.

Bit 5

When set to 1, text mode performance will be improved.

Bit 4:3

These two bits set the CPU's RDY timing to be optimized for different system timing. For slower systems, the RDY line may be released earlier because it will take longer for the read cycle to be completed.

00 = Power on reset condition. RDY is inserted at the end of a CPU memory cycle

01, 10 = RDY is inserted 1MCK before the end of a CPU memory cycle.

11 = RDY is inserted 1MCK after the end of a CPU read memory cycle. RDY is inserted at the end of a memory write cycle.

For 10 MHz or slower systems, the 01 setting is recommended. For 12 MHz or faster systems, the 11 setting is recommended.

Bit 2

When set to 1, a single-level , 16-bit write buffer is enabled. This willl greatly reduce the number of wait states for CPU writes to display memory.

Bit 1

If this bit and bit 0 are both set to 1, then the Attribute Controller (3C0/3C1) is configured for 16-bit access. The index is at 3C0, while the data is at 3C1, and the address toggle is disabled for 16-bit reads or writes. The address toggle functions in the standard way for 8-bit cycles. $\overline{\text{IOCS16}}$ is asserted for all cycles to 3C0 or 3C1.

Bit 0

When set to 1, this bit enables 16-bit access to the CRTC (3?4/3?5), Sequencer (3C4/3C5), and Graphics Controller (3CE/3CF). The output $\overline{\text{IOCS16}}$ will be active for any I/O read or write to these addresses. When set at 0, the VGA I/O is all 8-bit.

7.11.20 PR32 3C5 Index 12: Miscellaneous Control 4 (Reset State = 00H)

This register provides control for several different features. Some of these features help to support Genlock of the PVGA1M to another display controller for overlay.

BIT	FUNCTION
7	Enable External Sync Mode
6	Disable Cursor Blink
5	USR1 Function Select
4	USR1 Control
3	USR0 Function Select
2	USR0 Control
1	Allow readback in backward compatible modes
0	Force standard CPU addressing in 132-column mode

Bit 7

When set to 1, $\overline{\text{EXVID}}$ is configured to input external Horizontal Sync, and $\overline{\text{EXPCLK}}$ inputs external Vertical Sync. The external HSYNC signal also synchronizes the character clock timing. In this configuration, $\overline{\text{EXVID}}$ and $\overline{\text{EXPCLK}}$ do not control the VID7:0 and PCLK output buffers. A 0 setting places this bit into its normal operation mode.

Bit 6

When set to 1, the text cursor blink will be disabled, and the cursor will remain on. This option can be used if cursor blink is not desired.

Bit 5

A 1 setting causes the USR1 output to indicate when the WD90C10 is reading font data in text mode (FONTCYC). A 0 causes the USR1 output to reflect the state of bit 4, which can be used to control new features that the system board designer may wish to add.

Bit 4

Controls the USR1 output when selected by bit 5.

Bit 3

A 1 setting causes the USR0 output to indicate that the WD90C10 is reading both the character and the attribute data from the DRAMs in text mode (TEXTCYC). USR0 will be high during the RAS cycles for character/attribute read. The DRAM data may be sampled when USR0 is high. A 0 setting causes the USR0 output to reflect the state of bit 2, which can be used to control new features that the system board designer may wish to add.

Bit 2

Controls the USR0 output when selected by bit 3.

Bit 1

When set to 1, this bit allows reading the registers that are not readable in backward compatibility modes. This option may be used either as a test feature or by the BIOS during mode changes.

Bit 0

When set to 1, the special CPU address mapping for page mode font access in 132-column text is set for standard mapping without disturbing the display. This will be used only for special virtual VGA applications.

7.12 INTERNAL I/O PORTS

7.12.1 AT Mode Setup, Enable Write Only Port 46E8H (Also at Port 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7 - 5	Unused
4	Setup
3	Enable I/O & Memory
2 - 0	External BIOS ROM Page Select

Bit(7:5)

Unused

Bit 4

Setup
Puts WD90C10 into setup mode where only I/O port 102H is accessible.

Bit 3

Enable I/O and Memory Accesses

Bit(2:0)

Unused Internally
Used for BIOS ROM Page select. On I/O accesses to 46E8H, EBROMN becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits to define 4K pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0. The WD90C10 also provides an alternative port 3C3H instead of port 46E8H. If a pull down resistor is connected to MD(9) during power on reset (CNF9 = 0), then port 3C3H will be decoded instead of port 46E8H to support the same functions described above. Otherwise, port 46E8H is selected and decoded.

7.12.2 Setup Mode Video Enable (AT and Micro Channel Modes) Read/Write Port = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7 - 1	Unused
0	Wakeup VGA

Bit(7:1)

Unused

Bit 0

Wakeup VGA for I/O and Memory Accesses. Only lower 3 address bits are decoded for this port and WD90C10 must be in SETUP mode. VGA Enable Sleep bit or Programmable Option Select (POS) register 102H bit 0 is used to awaken the WD90C10 after power on in the MCA and AT mode. To enter the set up mode in AT bus applications, bit 4 of the partially decoded internal I/O port 46E8H is set to 1 before accessing the I/O port 102H. In MCA mode, when the VGASETUP (EION) signal pin is active low, the WD90C10 is in setup mode and port 102H can be accessed.

7.13 VIDEO RAMDAC PORTS

The Video RAMDAC is implemented externally to the WD90C10. However, the $\overline{\text{WPLT}}$ and $\overline{\text{RPLT}}$ signals required by the RAMDAC are provided by the WD90C10. Setting PR(16) bit 0 to a 1 forces $\overline{\text{WPLT}}$ to a high level disabling I/O writes to the RAMDAC. Normally, the $\overline{\text{WPLT}}$ and $\overline{\text{RPLT}}$ signals to the RAMDAC are generated when the following I/O ports are written to or read from.

DAC ADDRESS	DAC OPERATION	DETAILS
3C8H	PEL address port (write)	Read/write port
3C7H	PEL address port (read)	Write only port
*3C7H	*DAC state (read only)	*If bits 0/1 =1, DAC in read operation. When bits 0/1=0,DAC in write operation. Bits 2-7 are reserved.
3C6H	PEL mask (read/write)	Not to be written by application code or color look up table will be changed.
3C9H	PEL data register (read/write)	Three successive read/write bytes.

* This port is internal to the WD90C10.

7.14 CONFIGURATION BITS

Memory Data lines 15:0 are used to input configuration data at power-on reset (RST) by pullup or pulldown resistors. This configuration data then sets the bits in internal registers. Some of these bits can then be changed by software, while some are in non-writable registers. The non-writable bits set features such as bus type which are not changed after power-on.

BIT	FUNCTION
15 - 12	EGA Switches
11	A23 - A20 Connection Select
10	16-bit BIOS
9	46E8/3C3 Select
8	Display Status
7 - 4	General Purpose Status
3	Video Clock Source Control
2	Bus Architecture Select
1	ROM Configuration
0	Map out BIOS

7.14.1 WD90C10 Configuration Register Bits CNF(15:0)

CNF(15:12)

EGA CONFIGURATION SWITCHES SW4-SW1. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. PULLING DOWN MD(15:12) causes these bits to be latched LOW. PR11(7:4) are writable bits. These bits can be read as bit 4 of port 3C2H (as on a standard EGA) if the EGA COMPATIBILITY BIT [PR4(1)] has been set to 1. Selection of which bit is read is determined by bits 3 & 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE		READ
3c2 bit 3	3C2 bit 2	3C2 bit 4
0	0	PR11(7) [= EGA SW4]
0	1	PR11(6) [= EGA SW3]
1	0	PR11(5) [= EGA SW2]
1	1	PR11(4) [= EGA SW1]

CNF (11) (Refer to Figure 12)

A 4.7K pull down resistor on the pin MD 8 will set CNF(11) = 0. The pins A(22:20) should then be connected to the AT bus signals LA(19:17), unlatched CPU address. The pin A23 should be connected to the NOR of AT bus signals LA(23:20). The pins A(19:17) should be connected to AT bus SA(19:17), latched CPU address. This will allow the WD90C10 to directly drive MEMCS16 in AT bus which requires decoding of the early unlatched address LA(23:17). An external NOR is required to decode LA(23:20).
If there is no pull down resistor on MD8, the CNF(11) will be set to 1 by the internal pull up. Pins A(23:17) should be connected to AT bus signals LA(23:17). In most 80286 systems, the early address LA(23:17) is not latched during a bus operation. CNF(11) = 0 is required to ensure proper decoding of $\overline{\text{MEMCS16}}$ without many external components. In most 80386 systems, the early address LA(23:17) is latched during a bus operation. CNF(11) = 1 is recommended for design simplification. In Micro Channel applications, CNF(11) should be set to 1.

CNF (10)

A 4.7K pull down on pin MD10 will set CNF(10) = PR1(1). Upon power-up, the pin $\overline{\text{ROM16}}$ is enabled for 16-bit BIOS ROM decoding. Otherwise the internal pull up will set CNF(10) = PR1=0. To enable the 16-bit BIOS, PR1 must be set to 1 by writing to port 3CF (index 0B) and the CNF (1) must be 1. This bit is read/write at PR1(1).

CNF (9)

A 4.7K pull down on pin MD9 will set CNF(9) = 0. Then port 03C3 will be selected as the VGA setup and enable register instead of port 46E8 in the AT interface. Otherwise, the internal pull up will set CNF(9) = 1. Port 46E8 will be selected as VGA setup and enable register. This bit has no effect in Micro Channel applications.

CNF (8)

ANALOG/TTL DISPLAY STATUS BIT.
Bit CNF(8) is latched internally at power-on-reset from memory data bus pin MD(11), provided with either a pull-up or pull-down external resistor. Pulling up MD(11) causes CNF(8) to be latched Low. This bit controls no internal functions and is read only as bit 3 of PR5 (3CF.0F). Also, CNF(8) is unaffected by writing to PR5 (3CF.0F). Suggested implementation is:

0 = Analog (VGA - compatible) display is attached
1 = TTL (EGA-compatible) display is attached.

CNF (7:4)

GENERAL PURPOSE STATUS BITS.
Bits CNF (7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD (7:4), provided with either pull-up or pull-down external resistors. These are read only bits at PR5 (3CF.0F) positions (7:4). These bits are unaffected by writing to PR5(3CF.0F). Pulling up MD (7:4) causes CNF (7:4) to be latched high.

CNF (3)

VIDEO CLOCK SOURCE CONTROL.
This bit cannot be written or read as I/O port pulling up MD (3) causes CNF(3) to be latched high. It configures WD90C10 pins VCLK1 and VCLK2 as inputs or outputs.

0=For inputs.
1=For outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of dot clock is by an internal multiplexer. When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip, during I/O writes to port 3C2H. This load pulse may be inhibited by setting PR11(2)=1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. Also, VCLK1 and VCLK2 outputs equal to bits 2 and 3 of the Miscellaneous output register at 3C2H respectively when PR15 bit 5 is set to 1.

CNF (2)

BUS ARCHITECTURE SELECT.
This bit cannot be written or read as I/O. Pulling down MD(2) causes CNF(2) to be latched low.

0: Micro Channel architecture

1: AT BUS architecture

Select CNF(2) will change PINOUT definition between AT BUS and Micro Channel bus (see PINOUT description).

PC AT BUS	I/O	Micro Channel	I/O
MEMCS16	OUT	$\overline{\text{CDDS16}}$	OUT
$\overline{\text{ROM16}}$	OUT	$\overline{\text{CSFB}}$	OUT
$\overline{\text{EIO}}$	IN	3C3D0	IN
$\overline{\text{MRD}}$	IN	M/$\overline{\text{IO}}$	IN
$\overline{\text{MWR}}$	IN	$\overline{\text{S0}}$	IN
$\overline{\text{IOR}}$	IN	$\overline{\text{S1}}$	IN
$\overline{\text{IOW}}$	IN	CMD	IN
IRQ	OUT	$\overline{\text{IRQ}}$	OUT
$\overline{\text{IOCS16}}$	OUT	$\overline{\text{CDSETUP}}$	OUT

CNF (1)

ROM CONFIGURATION.
When set to 0, the WD90C10's data bus buffer controls are configured for 1 ROM (8 bits). An internal pullup on MD (1) sets this bit to 0 at power-on reset.
When set to 1, the WD90C10's data bus buffer controls are configured for 16-bits (as with two ROMs).
If CNF (1) = 0, then PR1(1) can not be set high. This bit can not be written or read.

CNF (0)

BIOS ROM MAPPING.
If set to 1, the BIOS ROM is mapped out. An internal pullup resistor on MD(0) sets this bit to 0 at power-on reset. An external 4.7 K ohm pulldown resistor may be used to set this bit to 1 on power-on (reset).
This bit is read/write at PR1(0).

APPENDIX

A.1 EGA MODE

For the register definitions that have not changed from the VGA modes, refer to the VGA description. Only the differences between the VGA and EGA registers are briefly described in this section. Also, refer to the prior section for VGA mode details. Not Used bits should be set to 0 unless otherwise noted.

A general procedure to enter EGA mode of operation is described. The actual software implementation details are not covered in this procedure. These steps are briefly defined to outline the EGA mode entry.

- Load Configuration register bit 8. Logic 0 for VGA compatible PS/2 display or Logic 1 for EGA compatible TTL monitor by appropriate pull-up or pull-down resistor on MD(11). (Pull-up resistor on MD11 causes CNF(8) to be latched with logic 0, for Analog PS/2 compatible display). This is status for the BIOS or application to signify monitor type attached.
- Unlock all the PR registers.
- Program PR2(6) to 0 for EGA mode.
- Set PR4 bit 1 to logic 1 for EGA compatibility.
- Load PR11(7:4) with EGA Configuration switches by using pull-up or pull-down resistors on pins MD(15:12). (Pull-up resistor causes logic 1 to be latched after power on reset.)
- The EGA switch setting may then be read from PR11(7:4) at I/O port 3C2 bit 4.
- If EGA is to be emulated on the IBM PS/2 type analog display, follow the suggested steps listed below:
  Initialize all the registers.
  Lock CRT controller registers.
  Force Clock Control rate of the CRT controller.
  - Set EGA emulation mode by programming:
    PR11(3)=1; Set EGA emulation on PS/2 type display
    PR14(6)=1; Vertical double scan
    PR11(2)=1; Lock clock select
    PR11(0)=1; Lock 8/9 dot timing.
    PR14(7)=1; Enable IRQ (optional)
  - Lock the PR registers PRO-PR5 and PR10-PR17.
  - Read protect PR registers.
- When EGA is required on a TTL monitor, the suggested steps are:
  - Initialize all the registers.
  - Set EGA TTL mode by programming:
    PR11(3)=0;EGA TTL
    PR14(7)=1;Enable IRQ
    PR15(6)=1;Set Low Clock
    PR14(7)=1;Enable IRQ
  - Lock PR registers PRO-PR5 and PR10-PR17
  - Read protect PR registers.

For more details on the PR registers, refer to the PR registers section. The EGA register summary shown on the next page highlight all the EGA mode registers.

A1.1 EGA Registers Summary

REGISTERS	EGA	I/O PORT
General Registers:		
Miscellaneous Output Reg	WO	3C2
Input Status Reg 0	RO	3C2
Input Status Reg 1	RO	3?A
Feature Control Reg	WO	3?A
Sequencer Registers:		
Sequencer Index Reg	WO	3C4
Sequencer Data Reg	WO	3C5
CRT Controller Registers:		
Index Reg	WO	3?4
CRT Controller Data Reg Except the following:	WO	3?5
Start Address High (Index=0C)	RW	3?5
Start Address Low (Index=0D)	RW	3?5
Cursor Location High (Index=0E)	RW	3?5
Cursor Location Low (Index=0F)	RW	3?5
Light Pen High, (Index=10)	R	3?5
Light Pen Low, (Index=11)	R	3?5
Graphics Controller Registers:		
Index Reg	WO	3CE
Other Graphics Reg	WO	3CF
Attribute Controller Registers:		
Index Reg	WO	3CO*
Attribute Controller Data Reg	WO	3CO*

NOTES:
1. RO = Read Only, WO = Write Only, and RW = Read/Write.
2. All Register addresses are in hex.
3. "?" = "B" in Monochrome modes or "D" in Color modes.
4. "*" = Identical responses from I/O ports 3C0 and 3C1.

TABLE 8. EGA REGISTERS SUMMARY

A.2 GENERAL REGISTERS

Only the general registers and the bit definitions that differ between the VGA and EGA are addressed. Their EGA mode bit definitions are provided.

A.2.1 Miscellaneous Output Register (Write Port 3C2)

Bits (7:5)

EGA: Same as Miscellaneous Output Register Bits (7:5) definition in the VGA section.

Bit 4

Not used.

Bits (3:2)

EGA:

BIT 3	BIT 2	DESCRIPTION
0	0	14.318 Mhz clock (VCLK0) is selected.
0	1	16.257 Mhz clock (VCLK1) is selected if Configuration Register Bit 3 is 0.
1	0	External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is 0.
1	1	Not Used. VCLK2 selected if Configuration Register Bit 3 is 0

Bit (0)

EGA: Identical to Miscellaneous Output Register Bit 0 definition in the VGA section.

A.2.2 Input Status Register 0 (Read Port 3C2)

Bit 7

EGA: Same as input Status Register 0, Bit 7 definition in the VGA section.

Bits (6:5)

EGA: Not used

Bit 4

EGA: The four configuration switches' information stored in PR11 can be read at this bit if PR4(1) has been set to 1.

Bits (3:0)

EGA: Not used = 1

A.2.3 Input Status Register 1 (READ PORT 3?A)

Bit (7)

EGA: Not used

Bit 6

EGA: Not used = 1

Bits (5:3)

EGA: Identical to Input Status Register 1 Bits (5:3) definition in the VGA section.

Bit 2

EGA: Not used = 1

Bit 1

EGA: Unused

Bit (0)

EGA:
Same as Input Status Register 1 Bit 0 definition in the VGA Section.

A.2.4 Feature Control Register (Write Port 3?A)

Bits (7:0)
EGA: Not used

A.3 SEQUENCER REGISTERS (PORT 3C5)

A.3.1 Clocking Mode register (Index = 01)

Bits (7:4)
EGA: Not Used

Bits (3,2)
EGA: Same as Clocking Mode Register Bits (3,2) definition in the VGA section.

Bit 1
EGA: Set to zero

Bit (0)
EGA: Identical to Clocking Mode Register Bit 0 definition in the VGA section.

A.3.2 Character Map Select Register (Index 03)

Bits (7:4)
EGA: Not Used

Bits (3:2)
EGA: Character Map Select A

BIT 3	BIT 2	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

Bits (1:0)
EGA: Character Map Select B

BIT 1	BIT 0	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

NOTE:
1. Character Map selection from Plane 2 is determined by bit 3 of the attribute code.

A.3.3 Memory Mode Register (Index = 04)

Bits (7:3)
EGA: Not Used

Bits (2:1)
EGA: Identical to Memory Mode Register Bits (2,1) definition in the VGA section.

Bit 0
EGA: Alpha mode bit.
A logic 1 shows that Alpha mode is active and character map selection is enabled. A logic 0 disables Alpha modes and enables non-Alpha modes.

A.4 CRT CONTROLLER REGISTERS (PORT 3?5)

The EGA registers that are different are listed. For similar registers and identical bits within registers refer to the VGA section. Also, "?" implies that a register is mapped into either 3B5 or 3D5, for Monochrome or Color display modes, respectively.

A.4.1 Index Register (Port = 3?4)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Five bits point to the CRT Registers Address index where the data is to be written.

A.4.2 Horizontal Total Register (Index = 00)

Bits (7:0)

EGA:
Eight bits of value for the "Total Character Count Less 2" are loaded into this register. They define number of characters to be displayed per horizontal line.

A.4.3 End Horizontal Blanking Register (Index = 03)

Bits (7)

EGA: Not Used.

Bits (6:5)

EGA: They define display enable skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

EGA: Five bits of character count are loaded to determine when the horizontal blanking signal becomes inactive.

A.4.4 End Horizontal Retrace Register (Index = 05)

Bit 7

EGA: It defines the start of the odd or even CRT counter memory address following the horizontal retrace time. Logic "1" = Odd Address and logic "0" = Even Address.

Bits (6:0)

EGA: Same as End Horizontal Retrace Registers Bits (6:0) definition in VGA section.

A.4.5 Vertical Total Register (Index = 06)

Bits (7:0)

EGA: Lower eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

A.4.6 CRT Controller Overflow Register (Index = 07)

Bits (7:5)

EGA: Not used.

Bits (4:0)

Identical to CRT Controller Overflow Register Bits (4:0) definitions in the VGA section.

A.4.7 Preset Row Scan Register (Index = 08)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Preset Row Scan Register Bits (4:0) definition in the VGA section.

A.4.8 Maximum Scan Line Register (Index = 09)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as maximum Scan Line Register Bits (4:0) definition in the VGA section.

A.4.9 Cursor Start Register (Index = 0A)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Cursor Start Register Bits (4:0) definition in the VGA section.

A.4.10 Cursor End Register (Index = 0B)

Bit(7)

EGA: Not used.

Bits (6:5)

EGA: They define cursor signal skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	0
1	0	1
1	1	2

Bits (4:0)

EGA: These bits define Cursor End value of row scan address counter. The programmed value is equal to "N+1" where "N" is the last row of the Cursor to be displayed.

A.4.11 Vertical Retrace Start Register (Index = 10) - Write

(Light Pen High register, Index = 10 - Read)

Bits (7:0)

EGA: Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

A.4.12 Vertical Retrace End Register (Index = 11) - Write

(Light Pen Low register, Index = 11 - Read)

Bits (7:6)

EGA: Not used

Bit 5

EGA: It enables the IRQ output buffer control if Logic 0 is programmed. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal. If programmed as logic 1, the IRQ buffer is switched to a high impedance state.

Bit 4

EGA: When programmed to logic 0, the IRQ latch is reset and cleared to 0 if bit 5 = 0. If it is logic 1, the IRQ latch gets set at the end of the vertical display.

Bits (3:0)

EGA: Identical to Vertical Retrace End Register Bits (3:0) definition in the VGA section.

A.4.13 Underline Location Register (Index = 14)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Horizontal scan row where the underline will be displayed. Value programmed is one less than the scan line desired.

A.4.14 End Vertical Blanking Register (Index = 16)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Identical to End Vertical Blanking Register Bits (4:0) definition in the VGA section.

A.4.15 Mode Control Register (Index = 17)

Bits (7:5)

EGA: Same as Mode Control Register Bits (7:5) definition in the VGA section.

Bit 4

EGA: Not used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.5 GRAPHICS CONTROLLER REGISTERS (PORT 3CF)

A.5.1 Read Map Select Register (Index = 04)

Bits (7:3)

EGA: Not Used.

Bits (2:0)

EGA: Map selected bits (2:0) which represent encoded value of the memory plane in binary as shown below:

D2	D1	D0	MAP SELECTED
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

A.5.2 Mode Register (Index = 05)

Bit (7:6)

EGA: Not Used

Bits (5:2)

EGA: Identical to Mode Register Bits (5:2) definition in the VGA section.

Bits (1:0)

EGA: Binary coded write bits define the write modes per table below:

BIT 1	BIT 0	FUNCTION
0	0	Write mode 0 - Refer to VGA section
0	1	Write mode 1 - Refer to VGA section
1	0	Write mode 2 - Refer to VGA section
1	1	Write mode 3 - Not Legal. Selects write mode 1.

A.6 ATTRIBUTE CONTROLLER REGISTERS (PORTS = 3C0/3C1)

A.6.1 Palette Registers (Index = 00 through 0F)

BIT	FUNCTION
7 - 6	Not used
5 - 0	Dynamic color selection

Bits (7:6)

EGA: Not Used.

Bits (5:0)

EGA: Dynamic color selection. Logic 0 = Color deselection, and Logic 1 = color selection per the table below:

BITS	COLOR	PIXEL
5	Sec. Red	VID 5
4	Sec Green/Inten	VID 4
3	Sec Blue/Mono	VID 3
2	Red	VID 2
1	Green	VID 1
0	Blue	VID 0

A.6.2 Mode Control Register (Index = 10)

BIT	FUNCTION
7 - 4	Not used
3 - 0	Same as Mode Control in VGA section

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.6.3 Overscan Color Register (Index = 11)

BIT	FUNCTION
7 - 6	Not used
5 - 0	Overscan color for border

Bits (7:6)

EGA: Not Used

Bits (5:0)

EGA: Overscan color for the border. For a monochrome display, set all the six bits to logic 0. The border color is defined by the color table for the Palette registers shown above.

A.6.4 Color Plane Enable Register (Index = 12)

BIT	FUNCTION
7 - 6	Same as Color Plane Enable - VGA
5 - 4	Video Status Multiplexer
3 - 0	Same as Color Plane Enable - VGA

Bits (7:6)

EGA: Same as Color Plane Enable Register Bits (7,6) in the VGA section.

Bits (5:4)

EGA:
Determines two of six colors for the Video Status Multiplexer per the table listed:

BIT 5	BIT 4	INPUT STATUS REGISTER 1 (Port 3?A)	
		BIT 5	BIT 4
0	0	VID 2(Red)	VID 0 (Blue)
0	1	VID 5(SRed)	VID 4 (SGreen)
1	0	VID 3(SBlue)	VID 1 (Green)
1	1	VID 5(SRed)	VID 4 (SGreen)

Bits (3:0)

EGA: Same as Color Plane Enable Register Bits (3:0) definition in the VGA section.

A.6.5 Horizontal PEL Panning Register (Index = 13)

BIT	FUNCTION
7 - 4	Not used
3 - 0	Horizontal left shift of the video data in number of pixels.

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: These four bits determine the horizontal left shift of the video data in number of pixels. In monochrome alpha numeric modes, (9 dots/character) image can be shifted by 9 pixels. For all other graphics or alpha numeric modes, a maximum left shift of 8 pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section.

A.7 APPLICATIONS

The WD90C10 applications section is divided into various interfaces such as processor (AT or Micro Channel mode), video memory, RAMDAC, monitor, and clock. The description and block diagrams are generic. No attempt is made to present schematic level details. Currently available application notes, technical briefs, and referenced literature at the end of the data sheet should supplement the information provided in this section. The Figures 9 through 17 are shown along with their brief description on the subsequent pages.

Figure 9 highlights the various WD90C10 Processor, memory, and I/0 interfaces.

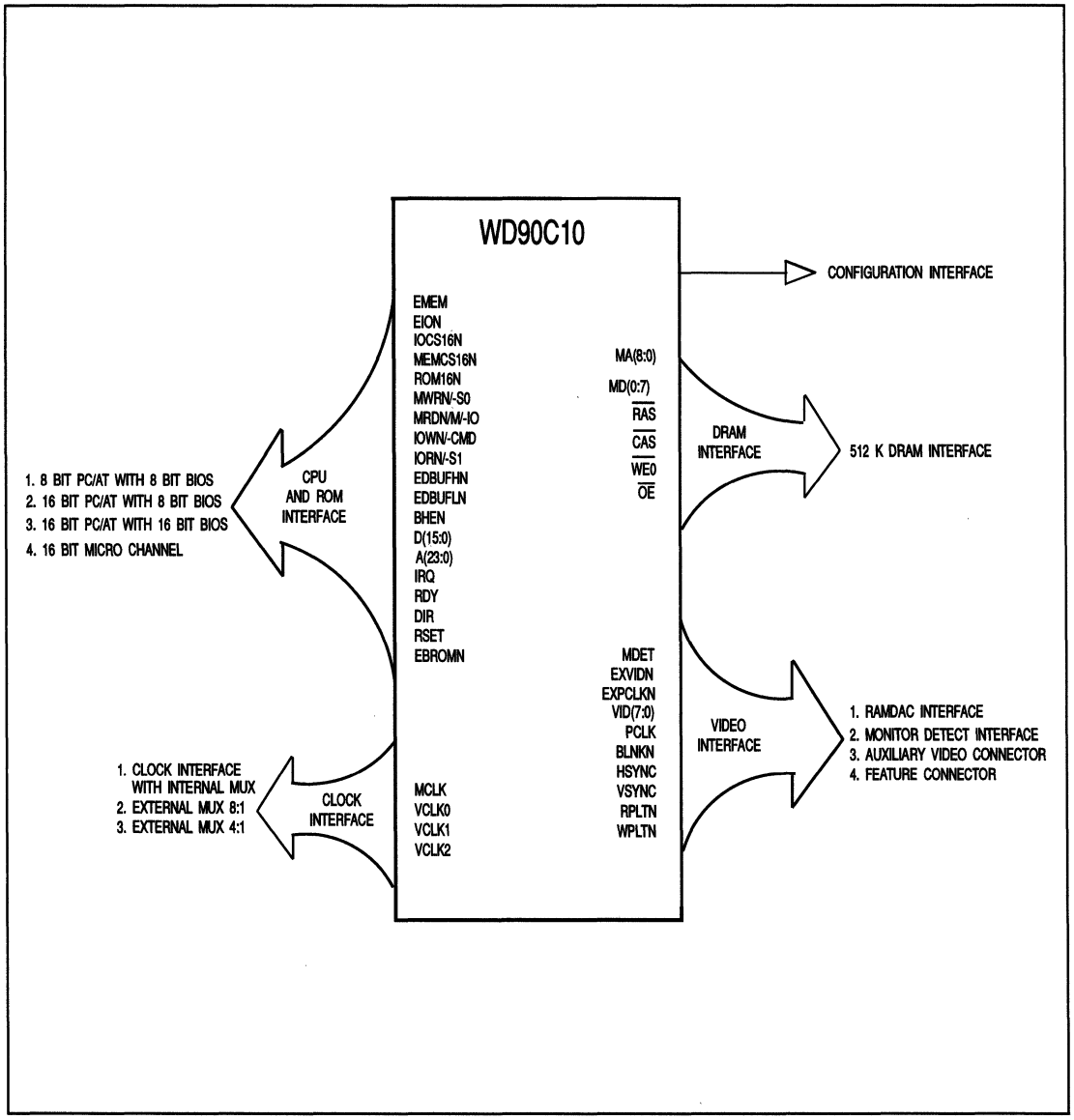


FIGURE 9. WD90C10 INTERFACES

Figure 10 shows a block diagram of the WD90C10 with 8 bit PC/AT interface using 8 bit BIOS. The system data bus SD(7:0) and address bus SA(19:0) are shown along with associated buffers and BIOS ROM.

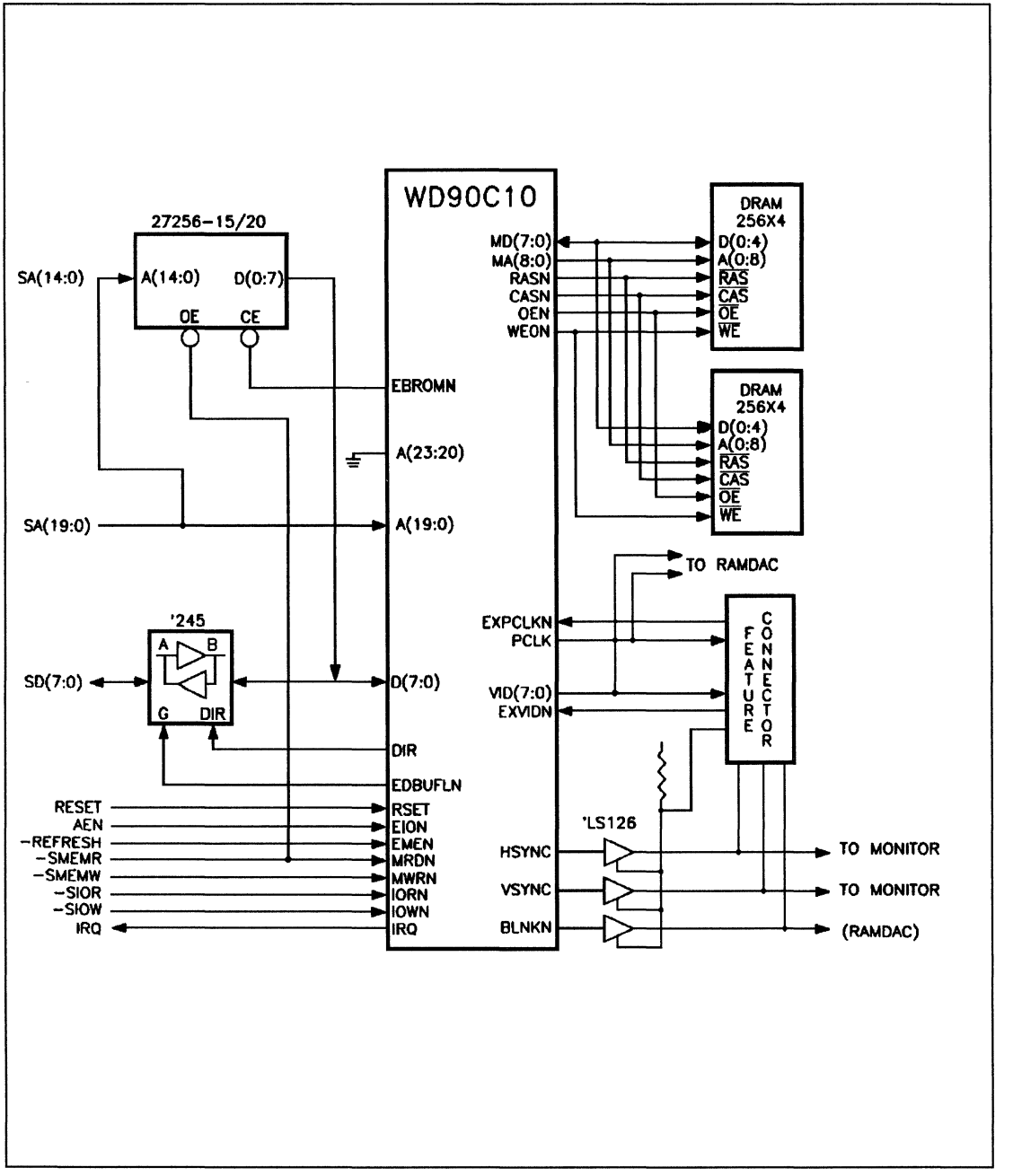


FIGURE 10. 8-BIT PC AT INTERFACE WITH 8-BIT BIOS

Figure 11 illustrates 16-bit PC/AT interface with 8-bit BIOS using WD90C10. For 386 systems, the processor data bus SD(15:0), and the system address bus SA(19:0) are shown. Associated address and data bus buffers and BIOS ROM are also shown in it.

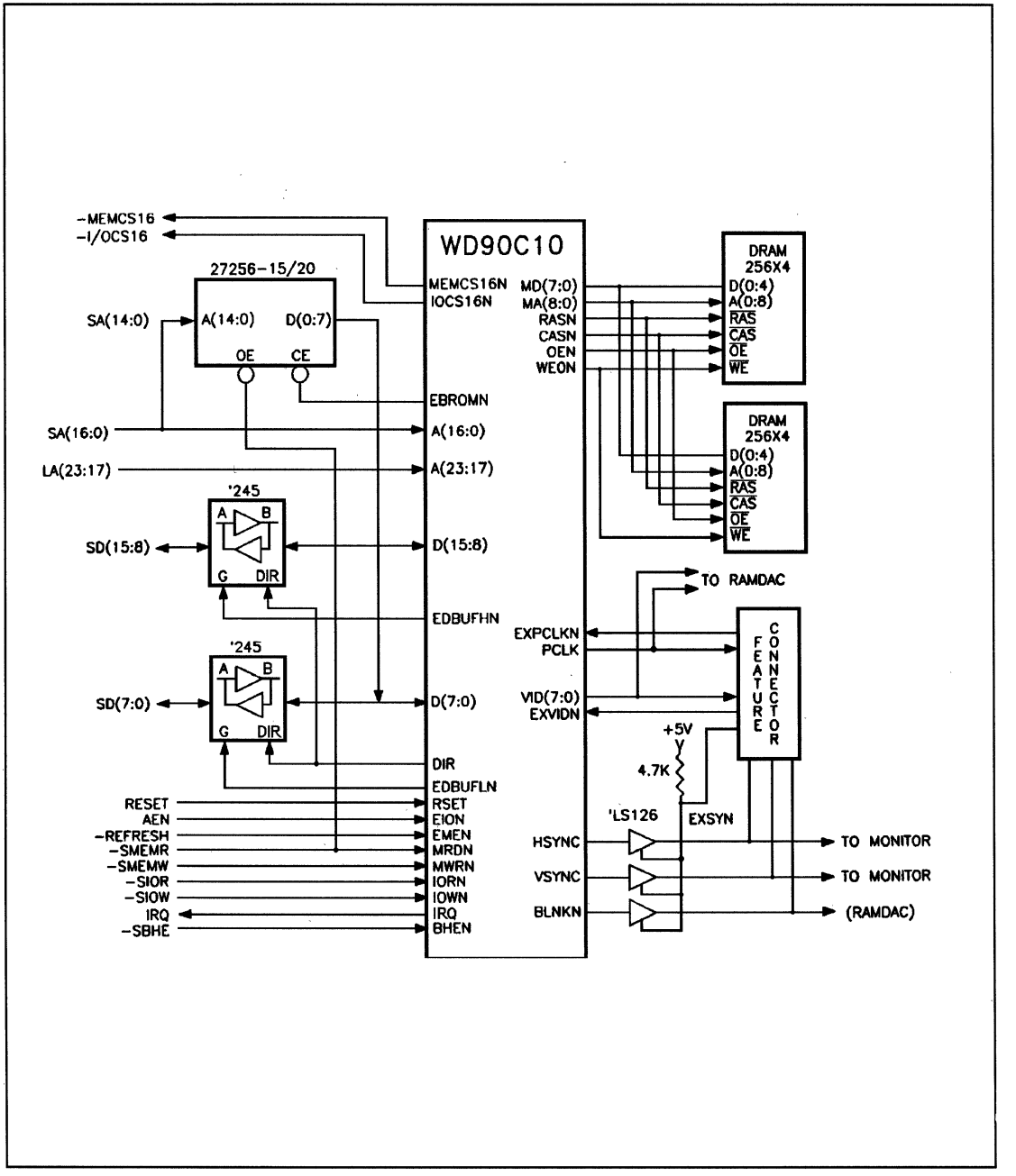


FIGURE 11. 16-BIT BIOS PC AT INTERFACE WITH 8-BIT BIOS

For 286 and some 386 systems, there may not be enough address hold time after SMEMRD or SMEMWR to generate $\overline{MEMC16}$ and $\overline{ROM16}$. Therefore, to allow continuous 16-bit memory and 16-bit BIOS access capability, configure the WD90C10 as illustrated in configuration 1. Configuration 2 can also be used, but it has some limitations.

CONFIGURATION 1:

This configuration uses a PAL to generate the $\overline{MEMC16}$ signal. This ensures 16-bit BIOS and 16-bit memory access capability at all times.

USR0 = 1 enables 16-bit memory accesses
USR1 = 1 enables 16-bit BIOS accesses

The BIOS initializes the USR outputs. The user must also set PR1, bit 1 and PR1, bit 2 to the values that correspond to the USR1 and USR0 settings, respectively. Refer to PR register descriptions.

PAL EQUATIONS

$\overline{Y1}$= USR0 * LA17 * $\overline{LA18}$ * LA19 * $\overline{LA20}$ * $\overline{LA21}$ * $\overline{LA22}$ * $\overline{LA23}$ + USR1 * $\overline{LA17}$ * LA18 * LA19 * $\overline{LA20}$ * $\overline{LA21}$ * $\overline{LA22}$ * $\overline{LA23}$ * SA[15] * $\overline{SA[16]}$

Y2=0

Y2 * TRST=Y1 (Output enabled when $\overline{Y1}$=0)

The first term of Y1 decodes the video region A0000 - BFFFF. The second term decodes the BIOS region C0000 - C7FFF.

CONFIGURATION 2:

Use of a PAL to generate $\overline{MEMC16}$ and discrete logic to decode the BIOS and provide 16-bit ROM accesses. USR0=1 enables 16-bit memory accesses.

This 16-bit BIOS implementation is limited with high bus speeds because ROM16 is delayed 40 ns from address valid (refer to timing information). For high bus speeds, 16-bit ROM accesses may not always occur in AT bus environments.

PAL has tri-state outputs.

Set the PR1, bits 1 and 2 to correspond to the USR0 setting and ROM data path respectively.

PAL EQUATIONS:

$\overline{Y1}$ = USR0 * LA17 * $\overline{LA18}$ * LA19 * $\overline{LA20}$ * $\overline{LA21}$ * $\overline{LA22}$ * $\overline{LA23}$ (A0000 - BFFFF)

Y2 = 0,Y2 * TRST = Y1

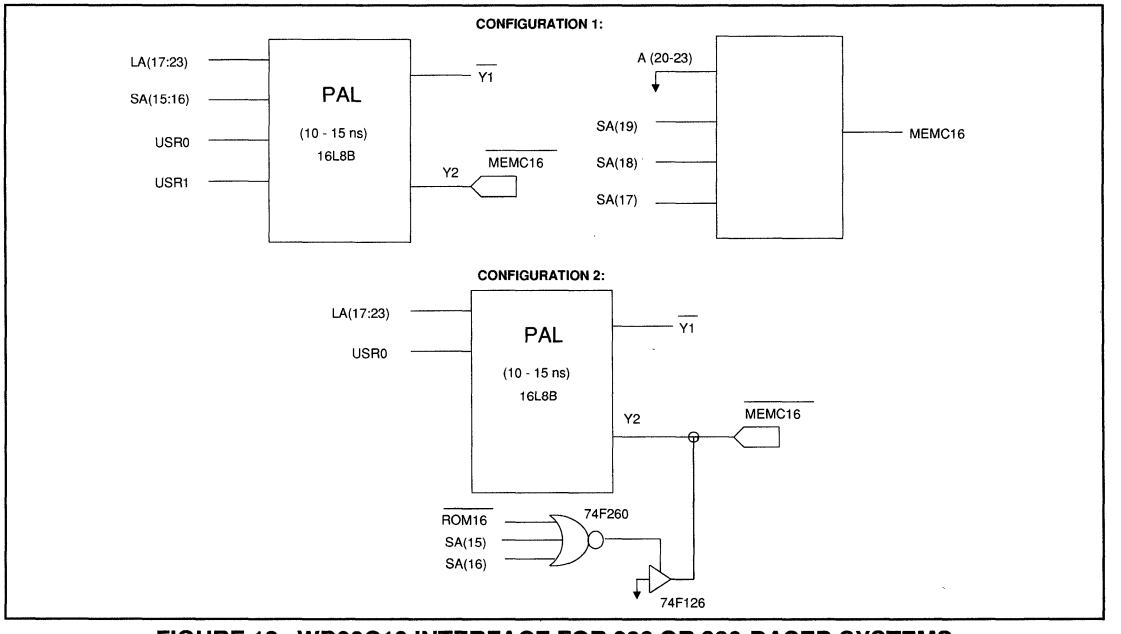


FIGURE 12. WD90C10 INTERFACE FOR 286 OR 386-BASED SYSTEMS

Figure 13 describes a 16-bit PC/AT interface with 16-bit BIOS ROM implementation using the WD90C10. The system data bus SD(15:0), address and data bus buffers are presented. Also, $\overline{\text{MEMCS16}}$ implementation is limited to certain bus speeds as SA15 and SA16 are used for the 16-bit BIOS. Refer to Figure 12 for 286-based systems.

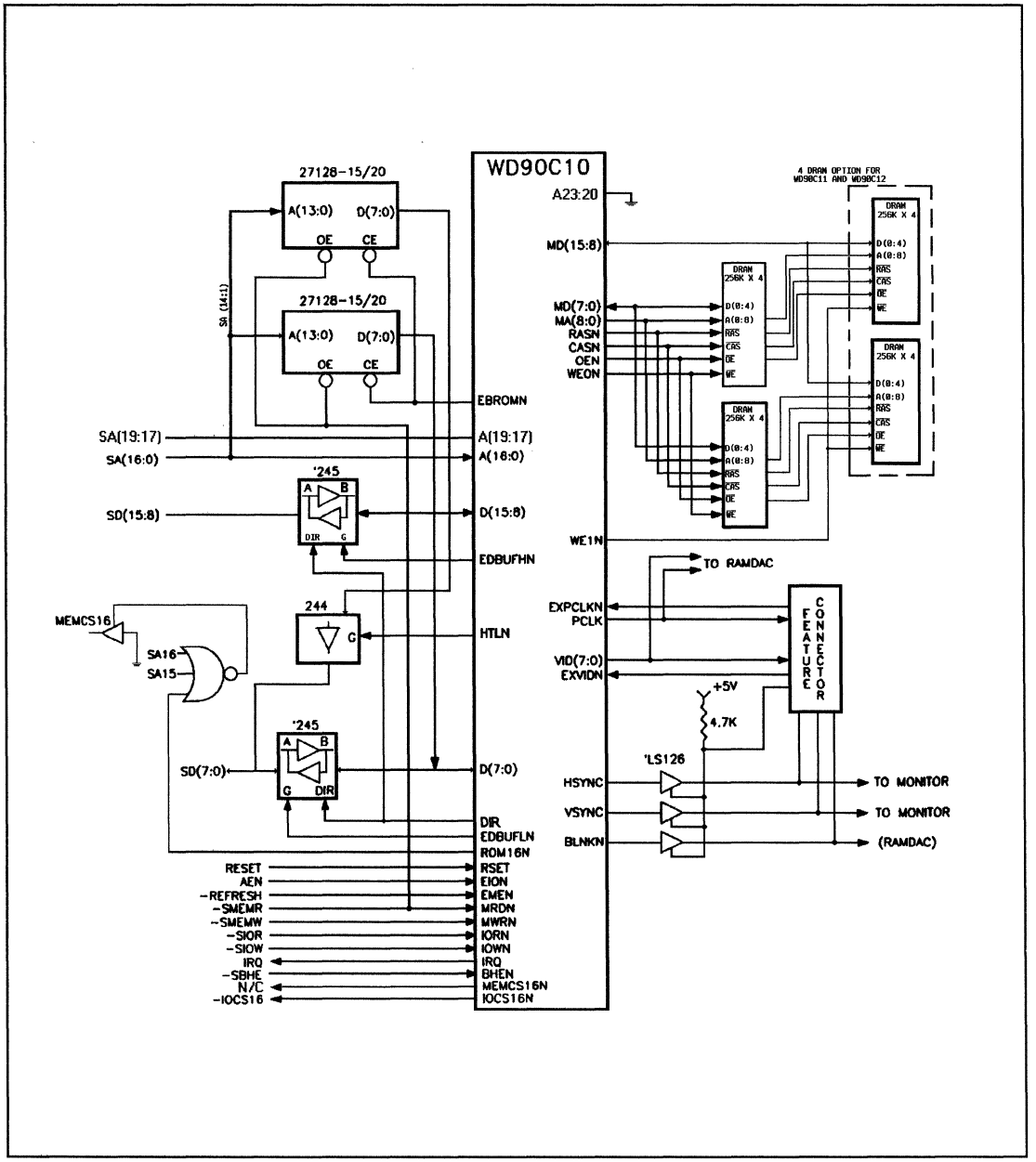


FIGURE 13. 16-BIT PC AT INTERFACE WITH 16-BIT BIOS (WITH OPTIONAL 512 KBYTES: 4- 256K BY 4 DRAM)

Figure 14 illustrates the WD90C10 and 16-bit Micro Channel interface. 3C3.D0 is output of port 3C3H bit 0 VGA Subsystem Enable Register.

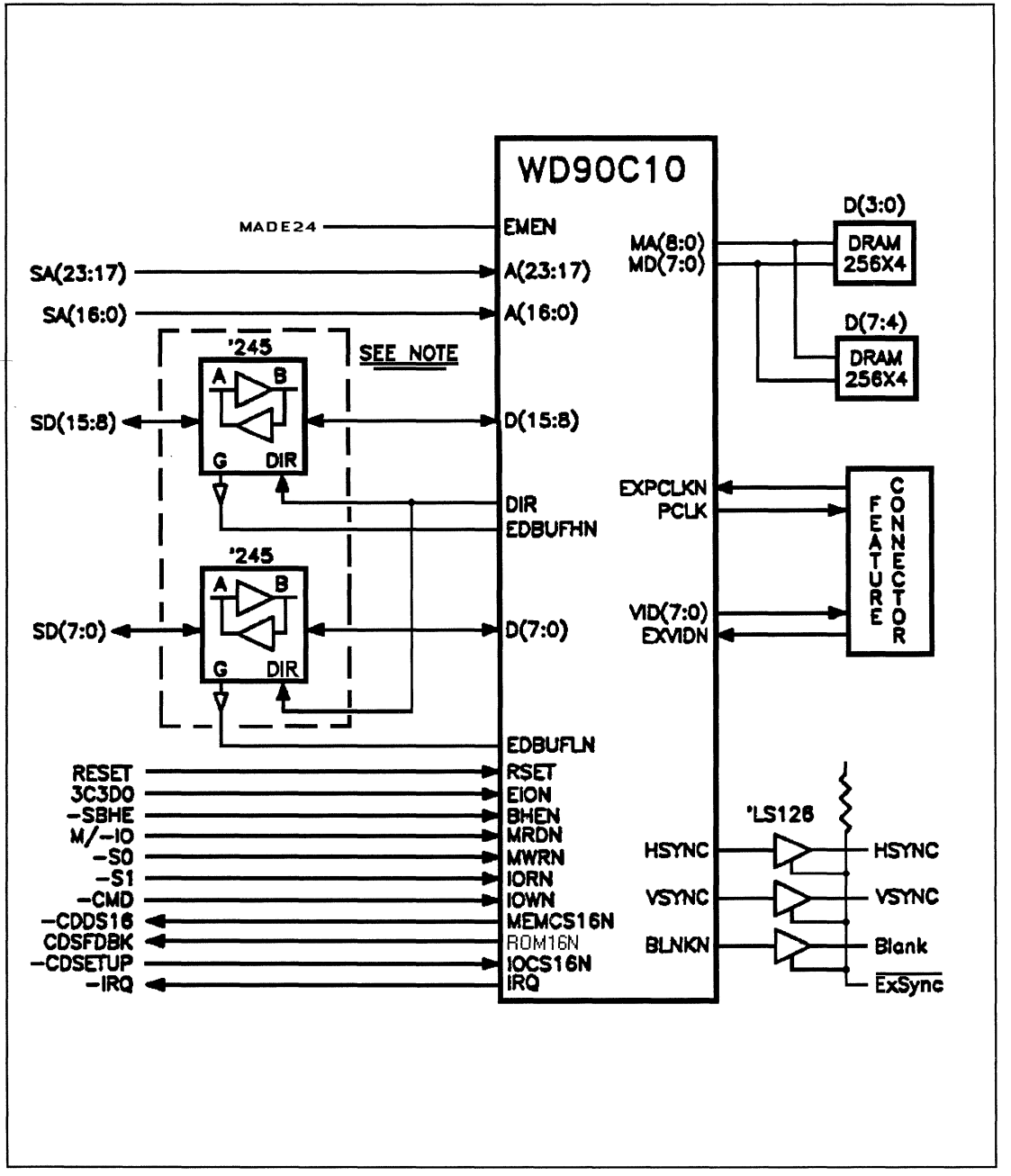


FIGURE 14. 16-BIT MICRO CHANNEL INTERFACE

Figure 15 illustrates the WD90C10 and RAMDAC (WD90C50) interface block diagram for analog monitors.

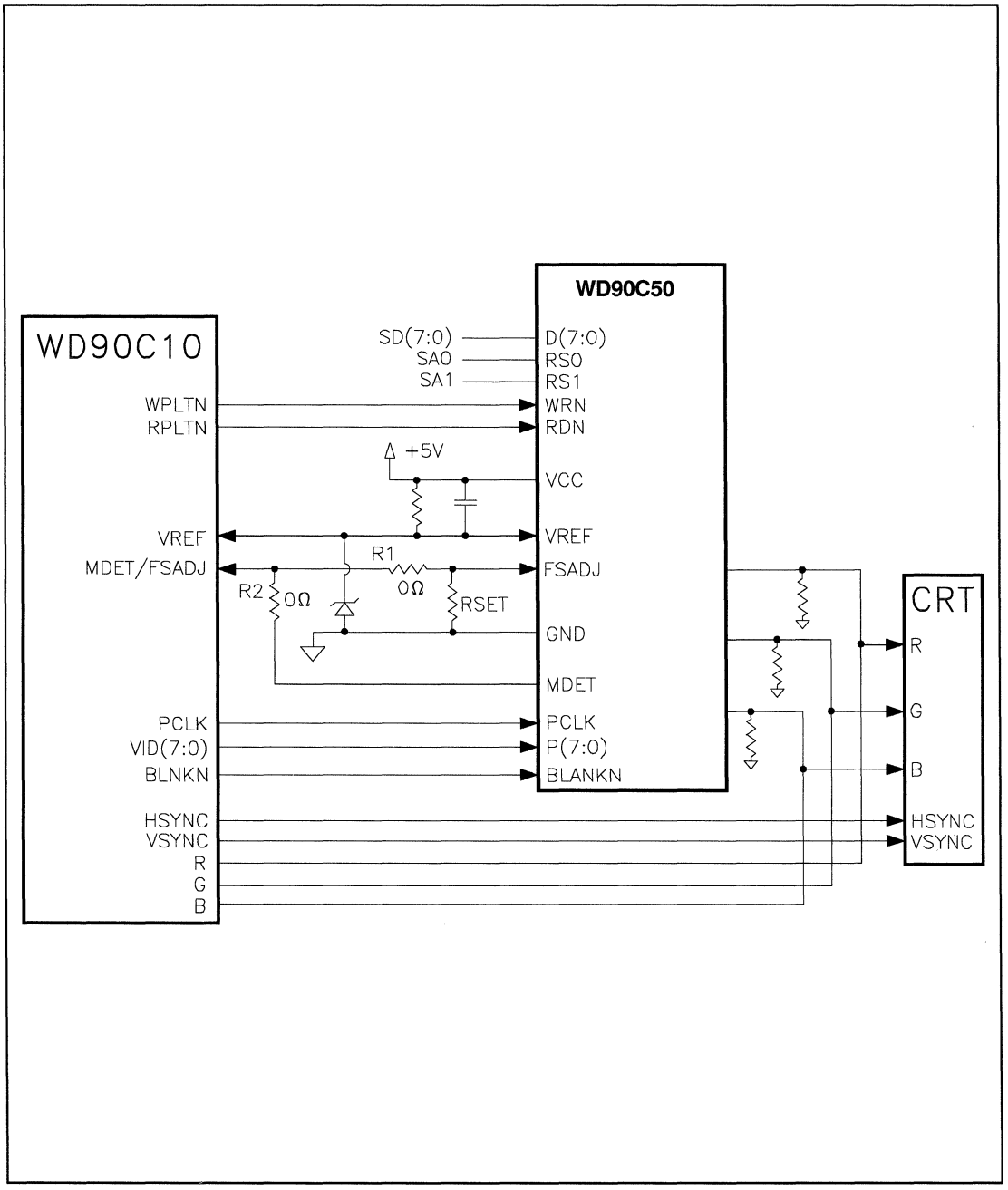


FIGURE 15. WD90C10 WITH RAMDAC INTERFACE

Figure 16 illustrates the WD90C10 and TTL monitor connections.

NOTE:

1. VGA/TTL switch may be used to disable HSYNC and VSYNC for Analog or TTL Video connector.
2. MD(15:12) may also be connected as the EGAswitches if desired. See PR register and Pin out sections for more details.
3. For AT applications using the WD90C10, install the IRQ9 resistor.
4. Transistor 2N2222A is used to emulate a Monochrome and a Color Display connection.

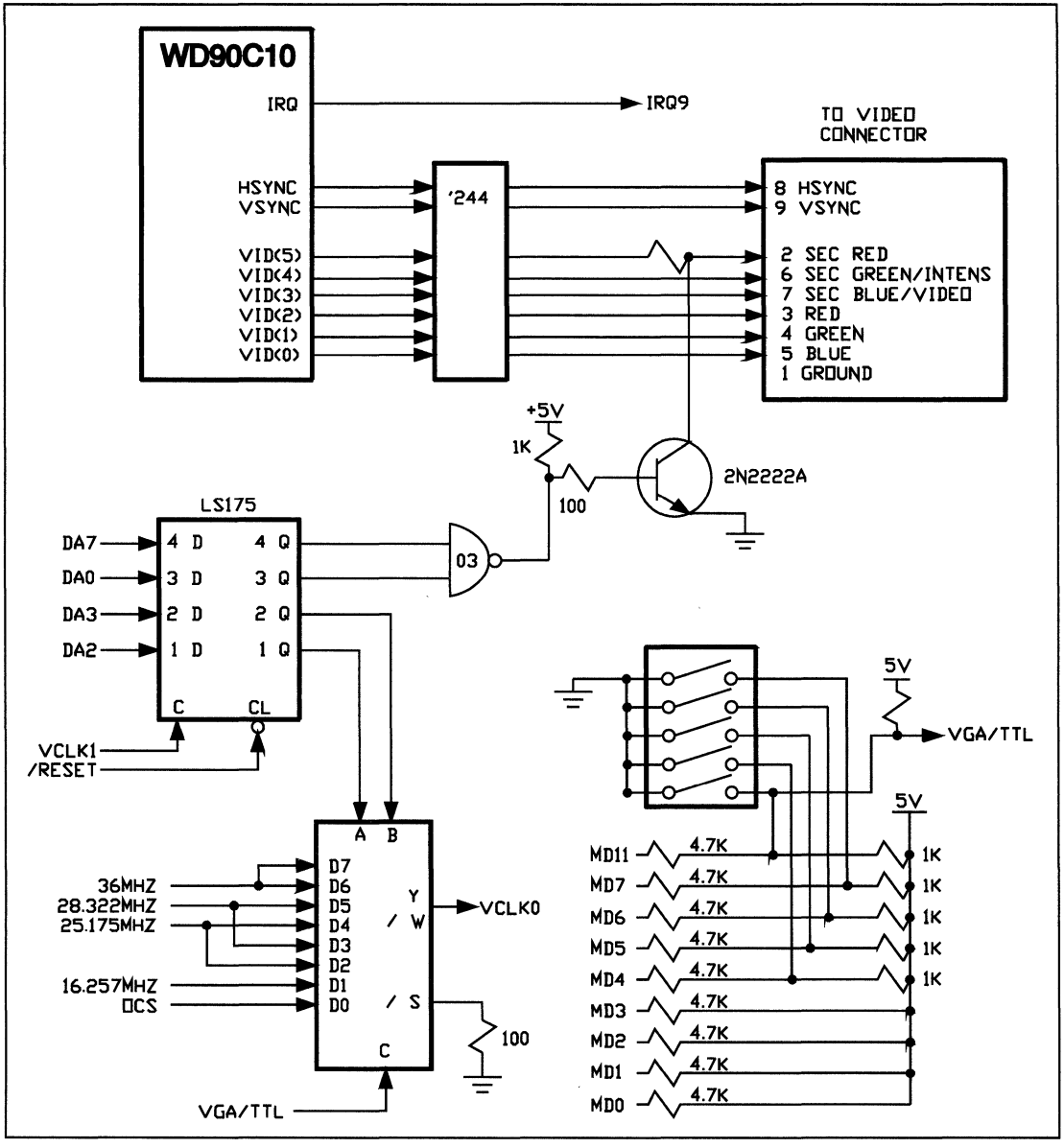


FIGURE 16. WD90C10 AND TTL MONITOR CONNECTIONS

Figure 17 illustrates the WD90C10 with external oscillators at the clock pins configured as inputs. The clock selection is determined by register 3C2H bit 3 and bit 2. It is described by the table below:

3C2H BIT 3	3C2H BIT 2	CLOCK SELECTION
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

The Configuration register Bit 3 (MD3) should be tied low to make the WD90C10 signal pins (VCLK1, VCLK2) inputs.

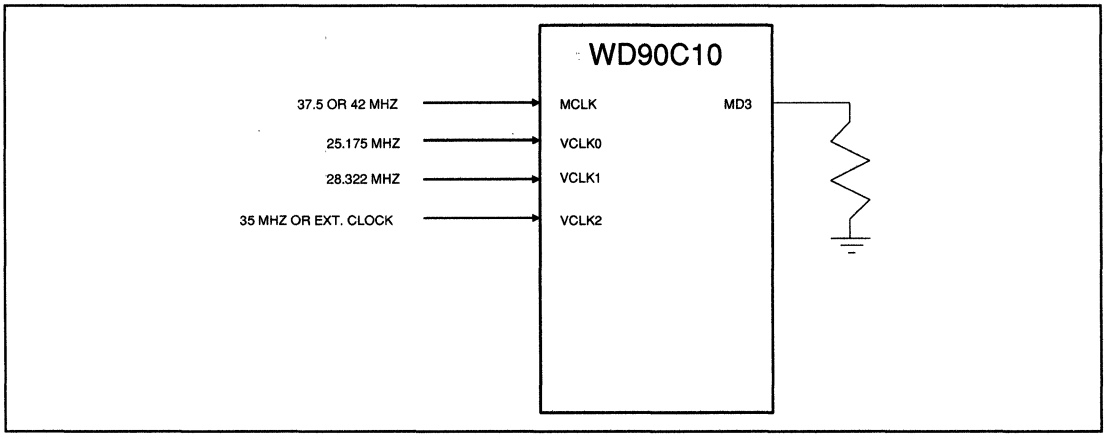


FIGURE 17. CLOCK INTERFACE

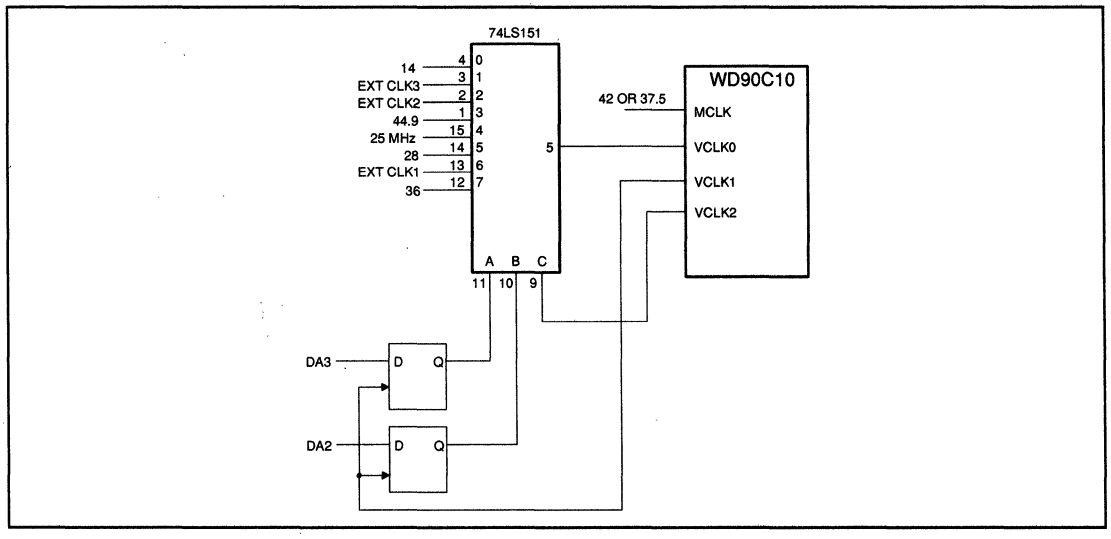


FIGURE 18. EXTERNAL VIDEO CLOCK MULTIPLEXING

A.8 REFERENCES

A list of references for generating the WD90C10 data book is shown below:

- IBM Personal Computer Hardware User Guide (IBM # 6322510)
- IBM Personal Computer XT Hardware User Guide (IBM # 6322511)
- IBM Personal Computer AT hardware User Guide (IBM # 6280066)
- IBM Personal System 2 Model 30 Hardware User Guide (IBM # 68x2230)
- IBM Personal Computer AT Technical Reference Manual (IBM # 6280070)
- IBM Personal System 2 Model 30 Technical Reference Manual (IBM # 68x2201)
- IBM PC Options & Adapters Technical Reference Manual (IBM # 6322509)
- IBM Personal System 2 BIOS Reference Manual (IBM # 68x2260)
- Personal Computer Reference Manual (IBM # 6025005)
- AT&T Video Display Controller VDC 750 / VDC 600 Installation Guide
- Hercules Graphics Card Owner's Manual
- Paradise OEM Technical Publication Manual

The customers are urged to refer to the manuals listed above and supplement their knowledge from other books and literature available.

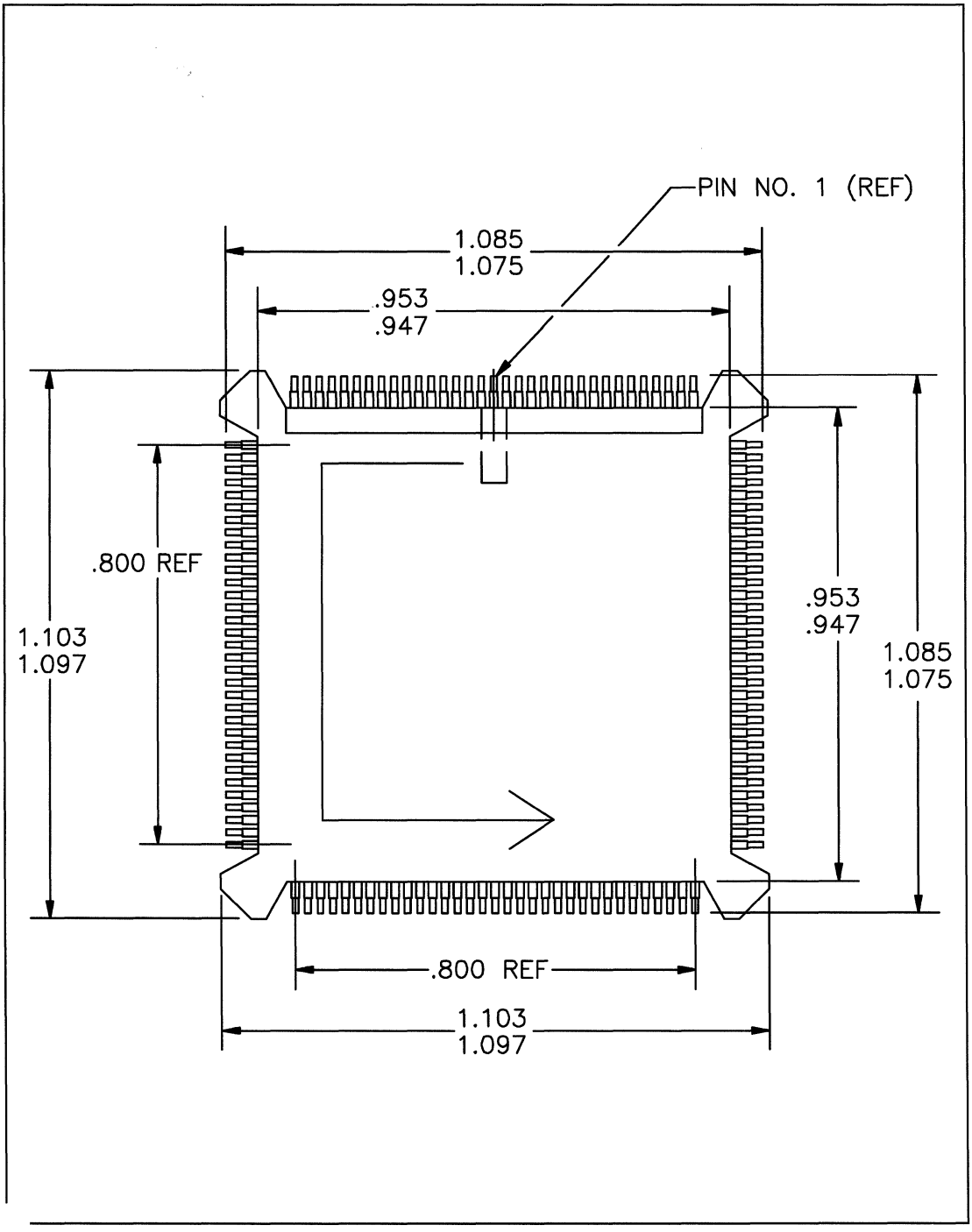


FIGURE 19. 132-PIN JEDEC PLASTIC FLAT PACKAGE (PFP) 1 OF 2

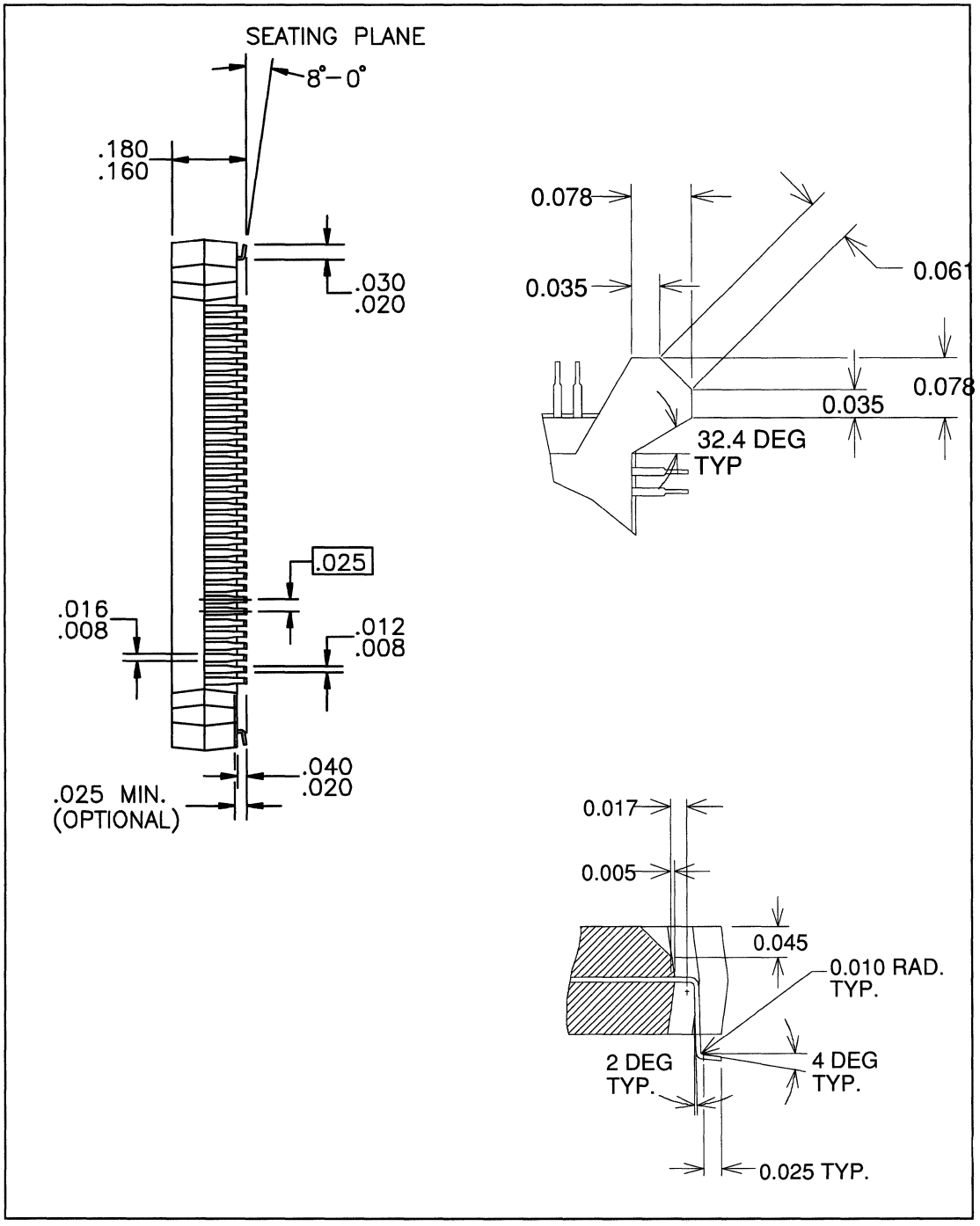


FIGURE 19. 132-PIN JEDEC PLASTIC FLAT PACKAGE (PFP) 2 OF 2

WD90C11

(PVGA1C) Enhanced

VGA Controller

WESTERN DIGITAL

TABLE OF CONTENTS

APPENDICES

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

The Western Digital Imaging WD90C11 is a 1.25 micron CMOS VLSI device that allows the design of a VGA graphics subsystem to interface with the PC/XT/AT bus, as well as the IBM Micro Channel bus, while maintaining backwards compatibility with previous video standards such as MDA, EGA, CGA, Hercules and AT&T 6300. The enhancements include Western Digital registers for EGA register level compatibility for PS/2 and TTL monitors, 1024 by 768 color graphics support, and integrated Micro Channel and AT interface. A major advantage of the WD90C11 is that designs implementing this graphics controller will be able to run applications requiring VGA hardware and BIOS compatibility, and also EGA register level compatibility on analog, TTL, or multifrequency monitors, in interlace or non-interlace mode. The WD90C11 supports either two or four 256 Kbyte by 4 DRAMs for operation.

This data book supplies order information, a functional overview, signal pin details, a block diagram, internal register descriptions, AC/DC characteristics, timing diagrams, VLSI package information, and associated references.

Ordering Information: WD90C11 Part Number: WD90C11LR00 02

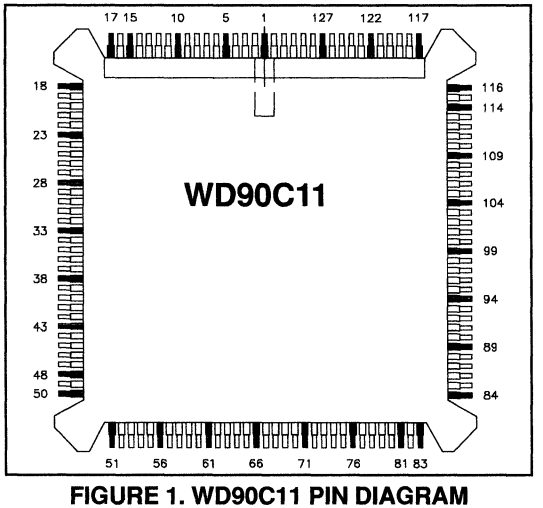


FIGURE 1. WD90C11 PIN DIAGRAM

1.1 FEATURES

- Provides single chip video graphics solution for IBM PC, XT, AT, and PS/2 compatible systems.
- Supports two or four 256 Kbyte by 4 DRAMs, providing high performance, high resolution, and 256 colors.
- Pin compatible with the WD90C12.
- 100% hardware compatible with IBM's VGA and EGA with hidden register support.
- 100% CGA, MDA, Hercules Graphics, and AT&T Model 6300 compatible.
- With 512 Kbytes of DRAM (four 256 Kb by 4), will support 1024 by 768 by 16 colors interlaced or non-interlaced, 640 by 400 by 256 colors, 640 by 480 by 256 colors, 800 by 600 by 256 colors. With two 256K by 4 DRAMs will support 1024 by 768 by 2/4 colors, 800 by 600 by 16 colors, 132 column text.
- Write cache for improved CPU write performance.
- 8- or 16-bit data bus for I/O and memory. True 16-bit CPU to video memory transfer for all modes.
- Up to 65 MHz maximum video clock rate.
- Up to 42 MHz maximum memory clock rate.
- Up to four simultaneous displayable fonts.
- 6, 7, 8, and 9 pixel wide fonts.
- Up to 16 fonts can be loaded.
- Provides adapter video BIOS ROM decoding.
- Total of 18 address bits for cursor location and start address.
- Special double scanning and underline.
- Special display enable or blanking output signal.
- Special border disable.
- Lockable palette, RAMDAC, and overscan registers.
- Special register locking for flat panel applications.
- Supports 16-bit I/O register transfer to index/data register pairs.
- Adjustable internal FIFO and fast page memory interface.
- 132-pin Plastic Flat Pack (PFP) JEDEC package.
- Integrated Feature connector interface and external RAMDAC support.
- Integrated bus interface for PC / XT / AT, and Micro Channel with minimum external component support.

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	A14	34	D8	67	MD14	100	VID0
2	A15	35	D7	68	MD13	101	VID1
3	A16	36	D6	69	MD12	102	VID2
4	A17	37	D5	70	MD11	103	VID3
5	A18	38	D4	71	MD10	104	VID4
6	A19	39	D3	72	MD9	105	VID5
7	A20	40	D2	73	MD8	106	VID6
8	A21	41	D1	74	MD7	107	VID7
9	A22	42	D0	75	MD6	108	+5VDC
10	A23	43	$\overline{WE1}$	76	MD5	109	$\overline{EXVID}$
11	$\overline{BHE}$	44	GND	77	GND	110	GND
12	EMEM	45	$\overline{MRD}$ (M/$\overline{IO}$)	78	MD4	111	VREF
13	$\overline{EIO}$ (3C3D0)	46	$\overline{MWR}$ ($\overline{S0}$)	79	MD3	112	MDET [FSADJ]
14	$\overline{IOCS16}$ ($\overline{CDSETUP}$)	47	$\overline{IOR}$ ($\overline{S1}$)	80	MD2	113	[GND-Analog]
15	GND	48	$\overline{IOW}$ ($\overline{CMD}$)	81	MD1	114	B
16	IRQ ($\overline{IRQ}$)	49	RSET	82	MD0	115	G
17	+5VDC	50	+5VDC	83	+5VDC	116	R
18	$\overline{EBROM}$	51	GND	84	$\overline{EXPCLK}$	117	A0
19	DIR	52	MA0	85	GND	118	A1
20	RDY	53	MA1	86	USR1	119	A2
21	$\overline{MEMCS16}$ ($\overline{CDDS16}$)	54	MA2	87	USR0	120	A3
22	$\overline{EDBUFH}$	55	MA3	88	PCLK	121	A4
23	$\overline{EDBUFL}$	56	MA4	89	$\overline{BLNK}$	122	A5
24	$\overline{ROM16}$ ($\overline{CSFB}$)	57	MA5	90	VSYNC	123	[+5 VDC-Analog]
25	$\overline{HTL}$	58	MA6	91	HSYNC	124	A6
26	D15	59	MA7	92	$\overline{RPLT}$	125	A7
27	D14	60	MA8	93	$\overline{WPLT}$	126	A8
28	GND	61	GND	94	VCLK2	127	A9
29	D13	62	$\overline{RAS}$	95	+5VDC	128	A10
30	D12	63	$\overline{CAS}$	96	VCLK1	129	A11
31	D11	64	$\overline{WE0}$	97	VCLK0	130	A12
32	D10	65	$\overline{OE}$	98	MCLK	131	GND
33	D9	66	MD15	99	GND	132	A13

TABLE 1. WD90C11 PIN ASSIGNMENTS

NOTE:
( ) Micro Channel only.
[ ] Reserved for WD90C12 option.

2.0 WD90C11 ARCHITECTURE

The WD90C11 contains four major internal modules, the CRT Controller, the Sequencer, the Graphics Controller and the Attribute Controller. The WD90C11 also has four major interfaces: the CPU and BIOS ROM interface, the DRAM Display Buffer interface, the Video and RAMDAC interface, and the Clock interface.

The WD90C11 controls the interfacing between the system microprocessor and video memory. Since the WD90C11 arbitrates video memory between the system microprocessor and the CRT Controller contained within the WD90C11, all data passes through the WD90C11 when the system microprocessor writes to or reads from the video memory.

A FIFO is used internally to achieve the video display bandwidth necessary to interleave CPU accesses and display refresh cycles, using only two or four 256K by 4 DRAMs.

2.1 WD90C11 MODULES

The CRT Controller module maintains screen refresh functions for the various display modes defined by the BIOS ROM resident firmware. The CRT Controller module also generates horizontal sync (HSYNC), vertical sync (VSYNC), and blanking signal for the display monitor.

The Sequencer functions as a timing generator for the AT bus or Micro Channel interface, in I/O or memory cycles. It also provides the character clock in the alphanumeric mode, and the dot clock in the graphics mode, for the CRT, Graphics, and Attribute Controllers.

The Graphics Controller manages data flow between video memory and the Attribute Controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the Sequencer.

The Attribute Controller modifies the CRT display data stream in graphics and character modes. It controls blinking, underlining, cursor, pixel panning, reverse video, and background or foreground color in all display modes.

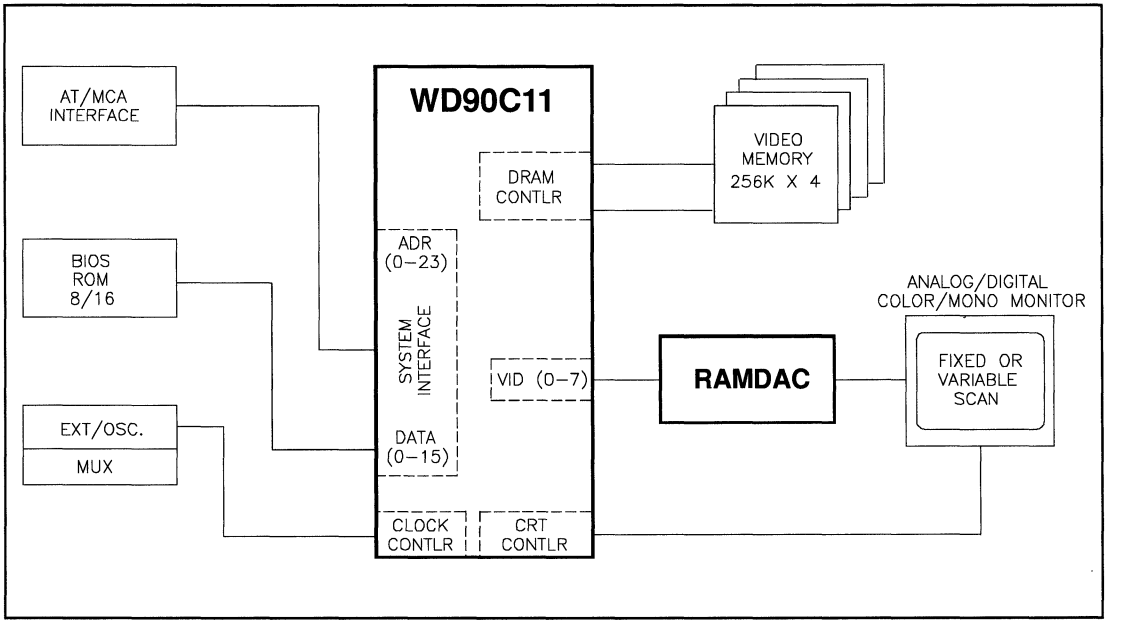


FIGURE 2. SYSTEM BLOCK DIAGRAM

3.0 WD90C11 INTERFACES

3.1 CPU AND BIOS ROM INTERFACE

The WD90C11 is designed to operate in both the PC/XT/AT Bus and the PS/2 Micro Channel Bus architecture configurations. The selection of the mode depends on the setting of a configuration register bit CNF(2), which is determined upon power-up/reset, and is described in the WD90C11 Configuration Bits section of this data book.

Whether configured for either AT or Micro Channel operation, the WD90C11 operates functionally in a manner conducive to PC/XT/AT or Micro Channel interfacing respectively. The signal pins, memory maps and I/O ports all operate to optimize this interface with minimal external circuitry.

The WD90C11 provides all the signals, and decodes all the necessary memory and I/O addresses to interface with the AT bus or the Micro Channel bus, in 8 or 16 bit data path modes. WD90C11 also provides the necessary decoding of the adapter video BIOS ROM. Using the provided signals, the customer can implement designs which operate in 8- or 16-bit mode and control an 8 or 16 bit BIOS ROM.

The I/O data path can be programmed to be either 16- or 8-bit. The CPU to display buffer data path can also be eight or sixteen bits wide for all modes. $\overline{\text{ROM16}}$, $\overline{\text{IOCS16}}$, and $\overline{\text{MEMCS16}}$ signals are generated by the WD90C11.

The WD90C11 has a display memory write cache which holds the CPU write data until it can be transferred to the display memory, allowing the CPU to continue. This feature greatly reduces CPU wait states while writing to the video memory.

The WD90C11 will provide the necessary wait states for CPU accesses to the video memory if necessary. Wait states for I/O accesses and BIOS ROM accesses are not generated.

Special I/O ports such as 46E8H for the AT for setup, and 102H for VGA enable, have been implemented internally in the WD90C11.

3.2 DRAM INTERFACE

The WD90C11 optimizes its interface to the video memory display buffer. The video memory DRAMs are organized as four planes to support all modes from only two or four 256K by 4 DRAMs by making use of its Fast Page Access of memory. Each plane can be configured as 64 KBytes (128, 256, or 512 Kbyte total).

For display refresh cycles, the WD90C11 will perform page mode read operations on the video memory in graphics modes. In alpha modes, a choice of page video memory read operation is also provided. For video memory write operations during graphics or alpha modes, the WD90C11 will generate standard RAS/CAS cycles as needed. The WD90C11 will also refresh the DRAMs with 3 or 5 (CAS before RAS) refresh cycles after every horizontal scan line.

Two or four 256K by 4, 80 ns DRAMs and a 37.5 MHz MCLK are required for all modes. 70 ns DRAMs can be used with 42 MHz MCLK.

3.3 VIDEO INTERFACE

The WD90C11 is optimized to connect to an analog CRT monitor through a RAMDAC, but it may also be used to drive other types of displays, such as TTL monitors. In interfacing to an analog monitor through an external RAMDAC, the WD90C11 provides all the necessary signals to interface to the video RAMDAC.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and depth (bits/pixels) of the image desired. New monitors, such as multifrequency monitors, are less stringent because of the many sync frequencies available. The WD90C11 can be programmed to directly generate all the CRT signals for up to 8 bits/pixel (256 color) displays.

The Micro Channel Auxiliary Video Connector and the AT Feature Connector can be connected directly to the WD90C11. The WD90C11 also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

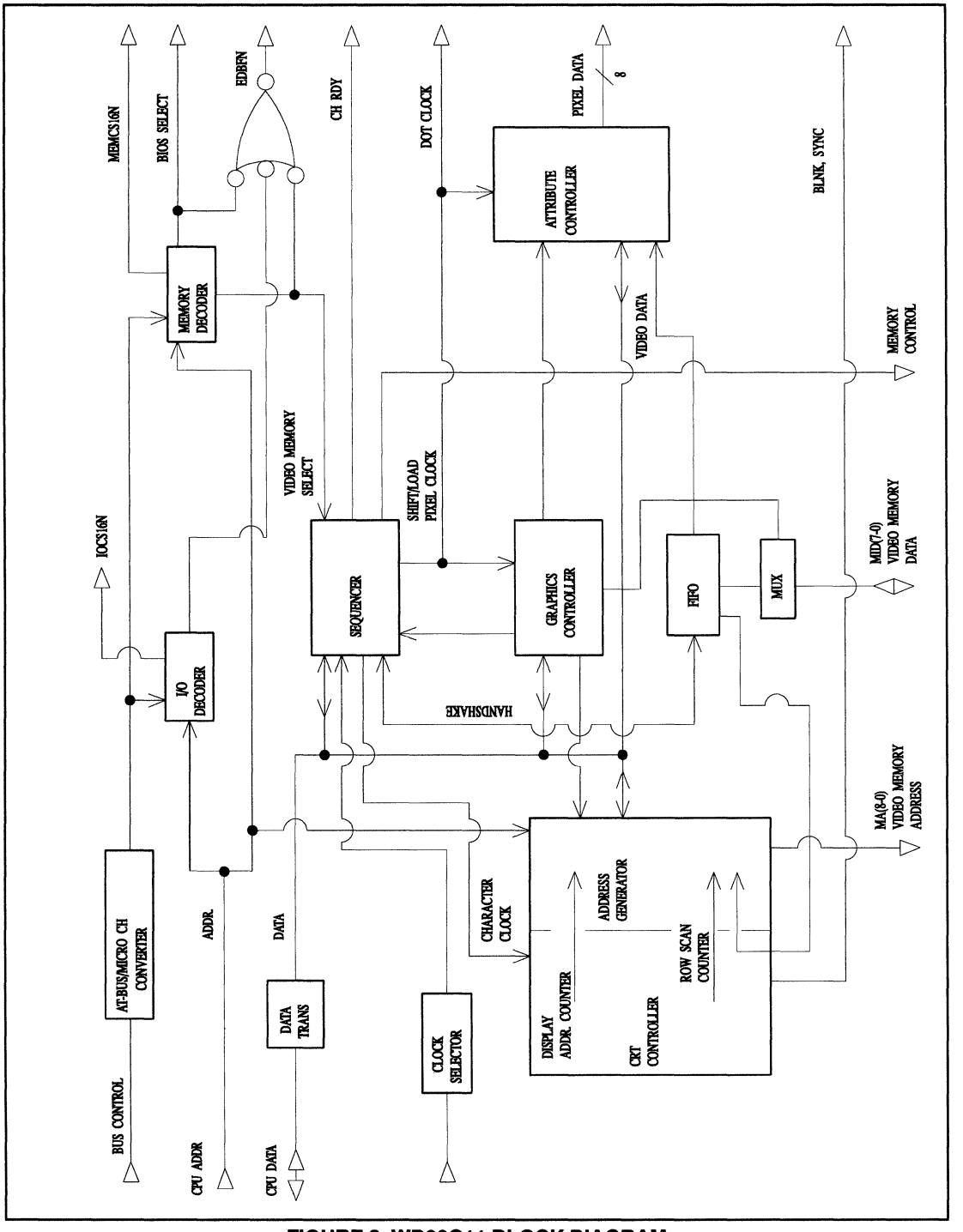


FIGURE 3. WD90C11 BLOCK DIAGRAM

3.4 CLOCK INTERFACE

The WD90C11 has four clock input signal pins; the separate memory clock, MCLK, which drives the DRAM and bus interface timing; and the three video clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing. VCK1 and VCK2 can also be programmed as outputs to provide the option to externally control a multiplexer that supplies the video clock. The MCLK can also be selected as a memory clock or video dot clock .

3.5 WD90C11 POWER-UP CONFIGURATION

The WD90C11 uses the memory data pins to configure an internal configuration register upon power- up/reset. CNF(2) will determine whether the WD90C11 will operate in AT or Micro Channel Architecture (MCA) implementation. Other CNF bits configured by the WD90C11 at power-up/reset are used as status bits, or for clock source control. For more information on WD90C11 power-up configuration, refer to the Configuration Bits section of this data book.

4.0 PIN DESCRIPTION

The following table provides pin definitions for the 132-pin WD90C11 package. The mnemonics are used.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
			POWER ON
49	RSET	I	RESET: This signal input will reset the WD90C11. MCLK and VCLK0 should be connected to WD90C11 in order for the WD90C11 to initialize during Reset. Western Digital configuration bits are initialized at power-up reset based on the logic level on the MD15-0 bus as determined by pull-up/pull-down resistors. The reset pulse width should be at least 10 MCLK clock periods.
			CLOCK SELECTION
98	MCLK	I	MEMORY CLOCK: This clock signal determines the VGA DRAM timing as well as system interface control timing. MCLK should be a minimum 37.5 MHz for 80 ns DRAMS.
97	VCLK0	I	VIDEO CLOCK 0: This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK is 25.175 MHz to display 640 pixels per horizontal display line. The Miscellaneous Output Register bits 2 and 3, both set to 0, will select this clock if VCLK1 and VCLK2 are used as inputs.
96	VCLK1	I/O	VIDEO CLOCK 1: This pin can be a second video display clock input or an output to external clock selection module. Pin direction is determined on Reset by a pull-up/down resistor on pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 is an active low pulse during I/O writes to port 3C2H (or it reflects the contents of 03C2, Miscellaneous Register, bit 2). Refer to the Configuration Register and PR15 Register, bit 5 description.
94	VCLK2	I/O	VIDEO CLOCK 2: A third video display clock input or an output to external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. Acts as a user-defined external clock input, or an output reflecting the content of bit PR2(1) (or it reflects the contents of 03C2, Miscellaneous Register, bit 3) if CNF (3) is set to 1. See the Configuration Register and PR15 Register, bit 5 description.

TABLE 2. PIN DESCRIPTION

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
			HOST INTERFACE
10 9 8 7	A23 A22 A21 A20	I I I I	ADDRESS BUS (A23 - A20): These address bits should be connected to address bus SA23 - 20 in Micro Channel mode. In AT mode, if CNF(11) = 1, then A23-20 should be connected to LA23-20 of the AT address bus. If CNF(11) = 0, then A22-20 should be connected to LA19 - 17 of the AT address bus, and A23 should be connected to an externally decoded ($\overline{LA23}$ x $\overline{LA22}$ x $\overline{LA21}$ x $\overline{LA20}$) = 1 from the AT address bus. CNF(11) = 0 when MD8 is pulled down with a 4.7 Kohm resistor.
6 5 4 3 2 1 132 130 129 128 127 126 125 124 122 121 120 119 118 117	A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	I I I I I I I I I I I I I I I I I	ADDRESS BUS (SA19-SA0): These inputs are directly connected to the system address bus (SA19 - SA0). Latched address. A19 - A17 can be connected to LA19 - LA17 in 386 systems when CNF (11) = 1. Refer to CNF(11) definition.
26 27 29 30 31 32 33 34 35 36 37 38 39 40 41 42	D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	DATA BUS (SD15 - SD0): These bidirectional signals either may be connected directly to a local data bus requiring less than 8 mA of source/sink, or may be connected through two external bus buffers controlled by $\overline{EDBUFH}$, $\overline{EDBUFL}$, and DIR.

TABLE 2. PIN DESCRIPTION (CONT)

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
20	RDY	O	READY: An active high output which signals to the system processor that a memory access is completed, and is used to add wait states to the CPU bus cycles during video memory accesses. It may be pulled inactive by the WD90C11 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM.
16	IRQ/($\overline{IRQ}$)	O	INTERRUPT REQUEST: Programmable processor interrupt request. It is enabled via bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of Vertical Display occurs, this signal will transition active, causing the interrupt.It will stay latched until CRTC11 bit 4 clears it. In an AT system IRQ is usually not connected, but may be connected if desired. $\overline{IRQ}$ is used to generate interrupt, usually in the Micro Channel mode.
21	$\overline{MEMCS16}$ ($\overline{CDDS16}$)	O	MEMORY CHIP SELECT 16 BITS: In AT mode, this line is used to respond the host to enable 16-bit video memory data transfer. In Micro Channel mode, this line is used to indicate 16-bit video memory or I/O access.
13	$\overline{EIO}$ (3C3D0)	I	ENABLE I/O: In AT mode, this active low signal is used to enable I/O address decoding and is connected directly to the system bus signal AEN (address enable). In Micro Channel mode, this line is from I/O port 3C3 bit 0 to enable video subsystem memory and I/O address decoding. ("1" = enable)
18	$\overline{EBROM}$	O	ENABLE BIOS ROM: In AT mode, this is an active low signal to enable BIOS ROM (C0000H - C7FFFH) if enabled by PR1(0). A WRITE to WD90C11 internal I/O port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
25	$\overline{HTL}$	O	ENABLE HIGH-TO-LOW: (for 16-bit BIOS) If only an 8-bit CPU interface is used, this output enables a data buffer to allow reading the upper byte of ROM data on the lower data bus when 2 ROMs (16-bit) are supported.
12	EMEM	I	ENABLE MEMORY: This signal enables memory decoding when high. It is normally connected to the signal -Refresh.

TABLE 2. PIN DESCRIPTIONS (CONT)

NOTE:
( ) Micro Channel only.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
11	$\overline{BHE}$	I	BYTE HIGH ENABLE: If SA0 is "0", this signal enables 16-bit data transfer mode when $\overline{BHE}$ is "0". With SA0, this signal is also used to select high byte data (SD[15:8]) or low byte data (SD[7:0]). An internal pullup is on this input.
45	$\overline{MRD}$/(M/$\overline{IO}$)	I	MEMORY READ: In AT mode, this signal is called $\overline{MRD}$ and is an active low memory read strobe. In Micro Channel mode, the signal is called M/$\overline{IO}$. It distinguishes between memory and I/O cycles. When (M/$\overline{IO}$) is high, a memory cycle is in process. A low on (M/$\overline{IO}$) shows that an I/O cycle is in process.
46	$\overline{MWR}$/($\overline{S0}$)	I	MEMORY WRITE: The Active low memory write strobe in AT mode. In Micro Channel mode, it becomes $\overline{S0}$ and is the channel status signal which indicates the start and type of a channel cycle. Along with $\overline{S1}$, M/$\overline{IO}$, and $\overline{CMD}$ signals, it is decoded to interpret I/O and memory commands.
47	$\overline{IOR}$/($\overline{S1}$)	I	I/O READ: Active low I/O read strobe in AT mode. In Micro Channel mode, it becomes $\overline{S1}$ and is the channel status signal which indicates the start and type of a channel cycle.
48	$\overline{IOW}$/($\overline{CMD}$)	I	I/O WRITE: Active low strobe. In AT mode, the strobe signals an I/O write. In Micro Channel mode it is the bus data strobe $\overline{CMD}$; address bus validity is signaled by $\overline{CMD}$ going low while the rising edge of $\overline{CMD}$ indicates the end of a Micro Channel bus cycle.
14	$\overline{IOCS16}$ ($\overline{CDSETUP}$)	I/O	I/O CHIP SELECT 16 BITS: In AT mode, used to respond to the host to allow 16-bit I/O access. In Micro Channel mode, is driven by the host to individually select channel connector slots during system configuration.
19	DIR	O	DIRECTION CONTROL: Active high Direction Control for external bus buffers in AT and MCA implementation. The default state is low until a read cycle occurs. The WD90C11 will then drive DIR high to change the direction of the data buffers.
22	$\overline{EDBUFH}$	O	ENABLE DATA BUFFER HIGH: Active low signal allows control of an external data buffer for data bits D8 - D15.
23	$\overline{EDBUFL}$	O	ENABLE DATA BUFFER LOW: Active low signal allows control of an external data buffer for data bits D0 - D7.

TABLE 2. PIN DESCRIPTIONS (CONT)

NOTE:
( ) Micro Channel only.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
24	$\overline{\text{ROM16}}$/ ($\overline{\text{CSFB}}$)	O	BIOS ROM SELECT 16 BITS: This signal decodes the ROM address space C0000 - DFFFF. It may be combined with SA15 and SA16 to control $\overline{\text{MEMCS16}}$ for the address space C0000 - C7FFF. This is an active low, totem-pole output. CARD SELECT FEEDBACK: (Micro Channel mode) This signal is used as Card Selected Feedback to provide positive acknowledgement of its presence at the host's addresses specified. This is an active low output.
DISPLAY MEMORY INTERFACE			
63	$\overline{\text{CAS}}$	O	COLUMN ADDRESS STROBE: Active low CAS output signal (for both two and four DRAM configurations).
62	$\overline{\text{RAS}}$	O	ROW ADDRESS STROBE: Active low RAS output signal (for both two and four DRAM configurations).
65	$\overline{\text{OE}}$	O	OUTPUT ENABLE: Active low DRAM output enable signal (for both two and four DRAM configurations).
64	$\overline{\text{WE0}}$	O	WRITE ENABLE: Active low write enable signal for first two DRAMs.
43	$\overline{\text{WE1}}$	O	WRITE ENABLE: [WD90C11 and WD90C12] Active low write enable signal for the second pair of DRAMs in a four-DRAM configuration.
PROGRAMMABLE OUTPUTS			
87	USR0	O	May be used to control special card or system features.
86	USR1	O	May be used to control special card or system features.

TABLE 2. PIN DESCRIPTION (CONT)

NOTE:
[ ] Reserved for WD90C12.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
			VIDEO MEMORY DATA
66 67 68 69 70 71 72 73 74 75 76 78 79 80 81 82	MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8 MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	DISPLAY MEMORY DATA (MD15 - 0): These lines are the data bus to the video display DRAMS. The MD15-MD8 data lines are for use with 4-DRAM configurations of the WD90C11 or WD90C12 part. Data lines MD0-15 are pulled up by internal 50K ohm resistors or may be pulled down by external 4.7K ohm resistors to provide setup information on power-up (reset) as follows: **MD — POWER-UP FUNCTION — REGISTER (BIT)** 15 — EGA SW4 — PR11(7) + 14 — EGA SW3 — PR11(6) + 13 — EGA SW2 — PR11(5) + 12 — EGA SW1 — PR11(4) + 11 — Analog/TTL Display — CNF(8) * 10 — 8- or 16-bit ROMs — PR1 (1) * 9 — 3C3 or 46E8 I/O Port for Setup — CNF(9) + 8 — A23 - 20 Connection Select — CNF(11) + 7 — General Purpose — CNF(7) * 6 — General Purpose — CNF(6) * 5 — General Purpose — CNF(5) * 4 — General Purpose — CNF(4) * 3 — VCLK1,2 Input/Output — CNF(3) + 2 — AT/Micro Channel Mode — CNF(2) + 1 — 1 or 2 ROMs — CNF(1) * 0 — BIOS ROM Mapping — PR1(0) * NOTES: "*" Pulldown resistor sets these bits to logic 1. "+" Pulldown resistor sets these bits to logic 0. For more details refer to PR and Configuration Registers.
			VIDEO MEMORY ADDRESS
60 59 58 57 56 55 54 53 52	MA8 MA7 MA6 MA5 MA4 MA3 MA2 MA1 MA0	O O O O O O O O O	MEMORY ADDRESS (MA0 - MA8): Display memory DRAM address. For testing purposes, these pins can be tri-stated by setting Paradise Register PR4(4)=1.

TABLE 2. PIN DESCRIPTIONS

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
		RAMDAC INTERFACE	
107 106 105 104 013 102 101 100	VID7 VID6 VID5 VID4 VID3 VID2 VID1 VID0	O O O O O O O O	VIDEO (VD0-VD7): Pixel video data output to DAC and to Feature Connector. These lines can drive up to a 8 mA load.
92	$\overline{\text{RPLT}}$	O	READ PALETTE: Video DAC register and color palette read signal for an external RAMDAC. Active low during an I/O read of addresses 3C6H, 3C8H, and 3C9H.
93	$\overline{\text{WPLT}}$	O	WRITE PALETTE: Video DAC register and color palette write signal for an external RAMDAC. Active low during an I/O write to addresses 3C6H-3C9H.
88	PCLK	O	PIXEL CLOCK: Video pixel clock output used by the DAC to latch video signals VID0-7. Its source is one of the video clock inputs: VCLK0, VCLK1 or VCLK2 as determined by the Miscellaneous Output register.
		CRT CONTROL	
89	$\overline{\text{BLNK}}$	O	BLANK: Active low display monitor blank pulse to external RAMDAC.
91	HSYNC	O	HORIZONTAL SYNC: Display monitor horizontal synchronization pulse. Active high or low depending on the Miscellaneous Output Register programming.
90	VSYNC	O	VERTICAL SYNC: Display monitor vertical synchronization pulse. Active high or low, depending on the Miscellaneous Output Register programming.
112	MDET [FSADJ]	I I	MONITOR DETECT: This pin is used when the RAMDAC is external. It is used to determine the monitor type and can be read at port 3C2H bit 4. [FULL SCALE ADJUST]: This pin is used when the RAMDAC is internal (WD90C12). It is used to control the RED, GREEN and BLUE's full scale output current.

TABLE 2. PIN DESCRIPTIONS (CONT)

NOTE:
[ ] Reserved for WD90C12.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
INTERNAL RAMDAC [WD90C12]			
116	[RED]	O	RED CURRENT OUTPUT: Used with the WD90C12 - Internal RAMDAC RS170 output from RED DAC to drive an analog monitor.
115	[GREEN]	O	GREEN CURRENT OUTPUT: Used with the WD90C12 - Internal RAMDAC RS170 output from GREEN DAC to drive an analog monitor.
114	[BLUE]	O	BLUE CURRENT OUTPUT: Used with the WD90C12 - Internal RAMDAC RS170 output from BLUE DAC to drive an analog monitor.
111	[VREF]	I	VOLTAGE REFERENCE INPUT: Used with the WD90C12 - Internal RAMDAC input used to set the reference voltage for the RAMDAC.
FEATURE CONNECTOR SUPPORT			
109	$\overline{\text{EXVID}}$	I	ENABLE EXTERNAL VIDEO DATA: A Feature Connector input. A low tri-states the video data lines VID7:0. An internal pullup resistor is provided. In the WD90C12 the VID7:0 lines become inputs to the internal RAMDAC.
84	$\overline{\text{EXPCLK}}$	I	ENABLE EXTERNAL PIXEL CLOCK: A Feature Connector input. A low tri-states the PCKL output. An internal pullup resistor is provided.
POWER AND GROUND			
123	[VCC]	-----	[+5VDC - ANALOG for WD90C12]
113	[GND]	-----	[Ground - ANALOG for WD90C12]
17	VCC	-----	+5VDC
50	VCC	-----	+5VDC
83	VCC	-----	+5VDC
95	VCC	-----	+5VDC
108	VCC	-----	+5VDC
15	GND	-----	Ground
28	GND	-----	Ground
44	GND	-----	Ground
51	GND	-----	Ground
61	GND	-----	Ground
77	GND	-----	Ground
85	GND	-----	Ground
99	GND	-----	Ground
110	GND	-----	Ground
131	GND	-----	Ground

TABLE 2. PIN DESCRIPTIONS

NOTE:
[ ] Reserved for WD90C12.

5.0 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to V_{SS}	-0.3 to 7 Volts
Power Dissipation	1.0 Watt

NOTE
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

5.1 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0° to 70°C
Power Supply Voltage	4.75 to 5.25 Volts

5.2 D.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX	UNITS	CONDITIONS
V(IL)	Input Low Voltage	-0.3	0.8	V	VCC=5V±5%
V(IH)	Input High Voltage	2.0	VCC+0.3	V	VCC=5V±5%
I(IL)	Input Low Current	--	±10	uA	VIN=0.0V
I(IH)	Input High Current	--	±10	uA	VIN=VCC
V(OL)	Output Low Voltage	--	0.4	V	IOL +2.0mA[1]
V(OH)	Output High Voltage	2.4	--	V	IOH=-2.0mA[1]
I(OZ)	High Impedance Leakage Current	-10.0	10.0	uA	OV<VOUT<VCC
C(IN)	Input Capacitance	--	10	pF	FC=1 MHz
C(OUT)	Output Capacitance	--	10	pF	FC=1 MHz

TABLE 3. DC CHARACTERISTICS

NOTE:

The WD90C11 outputs have 2.0 mA maximum source and sink capability except as follows:

IRQ, RDY= 4.0 mA source and 24.0 mA sink.

$\overline{\text{MEMCS16}}$, $\overline{\text{IOCS16}}$ = 20 mA sink.

D15:0, PCLK, VID7:0, $\overline{\text{ROM16}}$ = 8.0 mA source/sink.

$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE0}}$, $\overline{\text{WE1}}$, $\overline{\text{OE}}$, MA8:0, MD15:0 = 1.0 mA source/sink.

6.0 AC TIMING CHARACTERISTICS

The following notes apply to all of the parameters presented in this section:

All units are in nanoseconds
C_L = 20 pF unless otherwise noted

NUMBER	PARAMETER	MIN	MAX	NOTES
	RESET TIMING			
1	Reset Pulse Width	10t		t = 1/MCLK
2	MD Setup to RSET low	50		
3	MD Hold from RSET low	30		
4	RSET low to first $\overline{IOW}$	10t		
	CLOCK TIMING			
1	VCLK Period	t		t = 1/VCLK
2	VCLK high	0.4t	0.6t	@1.4V
3	VCLK low	0.4t	0.6t	@1.4V
4*	Clock Rise Time		3	0.8V - 2.0V
5*	Clock Fall Time		3	0.8V - 2.0V
6	VCLK to PCLK Delay	8	30	45 ns @ 120 pF load up to 30MHz
7a	VCLK to Hsync Delay	8	35	
7b	VCLK to Vsync Delay	8	35	
7c	VCLK to $\overline{BLNK}$ Delay	8	30	
7d	VCLK to VID(7:0) Delay	8	30	45 ns @ 120 pF load up to 30 MHz
8	MCLK period	24	27	
9	MCLK high	10	17	@ 1.4V
10	MCLK low	10	17	@ 1.4V
11	VID (7:0) setup to PCLK	3		
12	VID (7:0) hold from PCLK	3		

TABLE 4. AC TIMING CHARACTERISTICS

* Apply to both VCLK and MCLK.

NUMBER	PARAMETER	MIN	MAX	NOTES
	I/O AND MEMORY READ/WRITE AT MODE TIMING			
1	EMEM setup to $\overline{MRD}$, $\overline{MWR}$ low	20		
2	EMEM hold from $\overline{MRD}$,$\overline{MWR}$ high	15		
3a	A(23:0) setup to $\overline{MRD}$,$\overline{MWR}$ low	20		
3b	A(15:0) setup to $\overline{IOR}$,$\overline{IOW}$ low	20		
3c	$\overline{BHE}$ setup to $\overline{MRD}$,$\overline{MWR}$,$\overline{IOR}$,$\overline{IOW}$ low	20		
4a	A(23:0) hold from $\overline{MRD}$, $\overline{MWR}$ low	15		
4b	A(15:0) hold from $\overline{IOR}$, $\overline{IOW}$ low	15		
4c	$\overline{BHE}$ hold from $\overline{MRD}$,$\overline{MWR}$,$\overline{IOR}$,$\overline{IOW}$ low	15		
5	$\overline{EIO}$ setup to $\overline{IOR}$/$\overline{IOW}$ low	20		
6	$\overline{EIO}$ hold from $\overline{IOR}$/$\overline{IOW}$ high	15		
7	EDBUFxN low from $\overline{IOR}$,$\overline{IOW}$,$\overline{MRD}$,$\overline{MWR}$ low		38	
8	EDBUFxN high from $\overline{IOR}$,$\overline{IOW}$,$\overline{MRD}$,$\overline{MWR}$ high		38	
9	DIR high from $\overline{IOR}$,$\overline{MRD}$ low		38	
10	DIR hold from $\overline{IOR}$ and $\overline{MRD}$ high		38	
11	D(15:0) write data setup to $\overline{IOW}$ & $\overline{MWR}$ high	30		
12a	D(15:0) read data hold from $\overline{IOR}$ high		30	
12b	D(15:0) read data hold from $\overline{MRD}$ high		30	
12c	D(15:0) write data hold from $\overline{IOW}$ high	15		
12d	D(15:0) write data hold from $\overline{MWR}$ high	15		
13a	D(15:0) read data valid from $\overline{IOR}$ low		90	C_L = 70 pF
13b	D(15:0) write data valid after $\overline{MWR}$ low		2t	t= 1/MCLK
14	RDY high from $\overline{MWR}$/$\overline{MRD}$ low *(max is for standard VGA modes)*	10	2.45 µs	
15*	Memory read data valid from RDY high		40	C_L = 70 pF
16	RDY low from $\overline{MWR}$/$\overline{MRD}$ low	10	30	C_L = 100 pF
17	RDY tristate from $\overline{MWR}$/$\overline{MRD}$ high	10	30	C_L = 100 pF
18	$\overline{EBROM}$ low from valid A(23:15)		40	
19	$\overline{EBROM}$ hold from $\overline{MRD}$ high		40	
20a	$\overline{WPLT}$ low from $\overline{IOW}$ low		30	
20b	$\overline{RPLT}$ low from $\overline{IOR}$ low		30	
21a	$\overline{WPLT}$ high from $\overline{IOW}$ high		30	
21b	$\overline{RPLT}$ high from $\overline{IOR}$ high		30	
22	$\overline{EBROM}$ low from $\overline{IOW}$ low (46E8H port)		40	
23	$\overline{EBROM}$ high from $\overline{IOW}$ high (46E8H port)		40	
24	VCLK1 low from $\overline{IOW}$ low (3C2 port)		30	
25	VCLK1 high from $\overline{IOW}$ high (3C2 port)		30	
26	A(15:0) valid to $\overline{IOCS16}$ low		40	C_L = 100 pF
27	$\overline{IOCS16}$ hold from $\overline{IOW}$ high		40	C_L = 100 pF
28	A(23:17) valid to $\overline{MEMCS16}$ low		40	C_L = 100 pF
29	$\overline{MEMCS16}$ hold after valid A(23:17)		40	C_L = 100 pF

TABLE 4. AC TIMING CHARACTERISTICS (CONT)

NUMBER	PARAMETER	MIN	MAX	NOTES
	I/O AND MEMORY READ/WRITE MICRO CHANNEL MODE TIMING			
1	A(23:0),EMEM,$\overline{BHE}$ setup to $\overline{CMD}$ low	20		
2	A(23:0),EMEM,$\overline{BHE}$ hold from $\overline{CMD}$ low	15		
3	$\overline{CDSETUP}$,$\overline{EIO}$ setup to $\overline{CMD}$ low	20		
4	$\overline{CDSETUP}$,$\overline{EIO}$ hold from $\overline{CMD}$ low	15		
5	STATUS setup to $\overline{CMD}$ low	20		
6	STATUS hold from $\overline{CMD}$ low	15		
7	$\overline{EDBUFH}$, $\overline{EDBUFL}$ low from $\overline{CMD}$ low		38	
8	$\overline{EDBUFH}$, $\overline{EDBUFL}$ high from $\overline{CMD}$ high		38	
9	DIR active from $\overline{CMD}$ low		38	
10	DIR inactive from $\overline{CMD}$ high		38	
11	$\overline{CSFB}$ delay from valid address/status		40	CL = 100 pF
12	$\overline{CSFB}$ hold from $\overline{CMD}$ high (I/O cycle)		30	CL = 100 pF
13	$\overline{CSFB}$ hold from invalid address (memory cycle)		30	CL = 100 pF
14	$\overline{CDDS16}$ delay from valid address		40	
15	$\overline{CDDS16}$ hold from invalid address		30	
16	D(15:0) I/O write data setup to $\overline{CMD}$ high		30	
17a	D(15:0) I/O Write data hold after $\overline{CMD}$ high	15		
17b	D(15:0) Memory Write data hold after $\overline{CMD}$ high	0		
17c	D(15:0) I/O Read data hold from $\overline{CMD}$ high	5	20	CL = 70 pF
17d	D(15:0) Memory Read data hold from $\overline{CMD}$ high	5	20	C_L = 70 pF
18a	D(15:0) Memory Write data valid after $\overline{CMD}$ low		50	
18b	D(15:0) I/O Read data valid from $\overline{CMD}$ low		90	C_L = 70 pF
19	RDY high delay from $\overline{CMD}$ low	0	2.45µs	
20*	D(15:0) Memory Read Data valid from RDY high		40	C_L = 70 pF
21	$\overline{CMD}$ high (inactive)	2t+15		
22	RDY low delay from valid address/status	10	30	
23	$\overline{EBROM}$ low from valid address		40	
24	$\overline{EBROM}$ high from $\overline{CMD}$ high		30	
25	$\overline{WPLT}$ /$\overline{RPLT}$ low from $\overline{CMD}$ low		30	
26	$\overline{WPLT}$ /$\overline{RPLT}$ high from $\overline{CMD}$ high		30	
27	VCLK1 low from $\overline{CMD}$ low (3C2 port)		30	
28	VCLK1 high from $\overline{CMD}$ high (3C2 port)		30	

TABLE 4. AC TIMING CHARACTERISTICS (CONT)

* Depends on setting of 3C5, Index 11, bit 4, 3.

0 0 max 40 ns
0 1 max 40 ns + 1t
1 0 max 40 ns + 1t
1 1 max 40 ns - 1t

(t = 1/MCLK)

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM TIMING			
1	$\overline{RAS}$ cycle time	6t	See Note	
2	$\overline{RAS}$ pulse width low	3.5t-6	See Note	
3	$\overline{RAS}$ high time (precharge)	2.5t+6		
4	$\overline{RAS}$ low to $\overline{CAS}$ low	2.5t-9	2.5t -6	
5	$\overline{CAS}$ cycle time	2t	2t	
6	$\overline{CAS}$ pulse width low	1t	1t	
7	$\overline{CAS}$ high time (precharge)	1t	1t	
8	Row address setup to $\overline{RAS}$ low	1.5t-10	1t	
9	Row address hold time from $\overline{RAS}$ low	1t-6	1t+10	
10	Column address setup to $\overline{CAS}$ low	1t-10	1 t	
11	Column address hold from $\overline{CAS}$ low	1t	1t+10	
12	Read Data valid before $\overline{CAS}$ high	2		
13	Read data hold after $\overline{CAS}$ high	0		
14	Write Data setup to $\overline{CAS}$ low	1t-21	1.5t	
15	Write Data hold after $\overline{CAS}$ low	1t-5	1t	
16	$\overline{WE0}$ low setup $\overline{CAS}$ low	1t-5	1t+5	
17	$\overline{WE0}$ low hold after $\overline{CAS}$ high	0	10	
18	$\overline{OE}$ high before $\overline{WE0}$ low	2t-5	2t+5	
19	$\overline{OE}$ low after $\overline{WE0}$ high	1t-5	1t+5	

MCLK edge to $\overline{RAS}$,$\overline{CAS}$, MA(8:0) edge delay may be up to 40 ns

Notes:
Page-mode CRT reads may be 4-32 $\overline{CAS}$ cycles.
CPU writes use 1-4 $\overline{CAS}$ cycles in Page-mode.
CPU reads use 4 $\overline{CAS}$ cycles in Page-mode.

t = 1/MCLK
It is recommended that MCLK = 37.5 MHz for 80 ns DRAM with longer RAS precharge. MCLK = 40 MHz for 80 ns DRAM with shorter RAS precharge. This can be accomplished with selected DRAMs.

TABLE 4. AC TIMING CHARACTERISTICS (CONT)

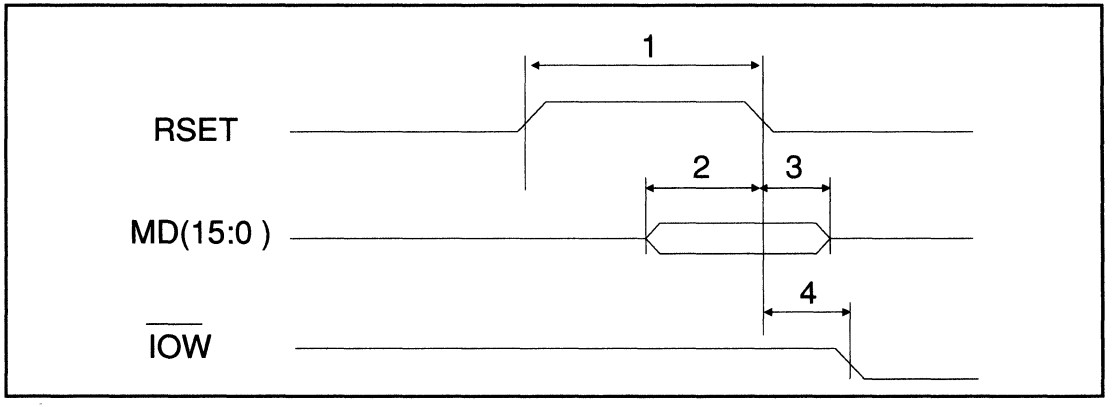


FIGURE 4. RESET TIMING

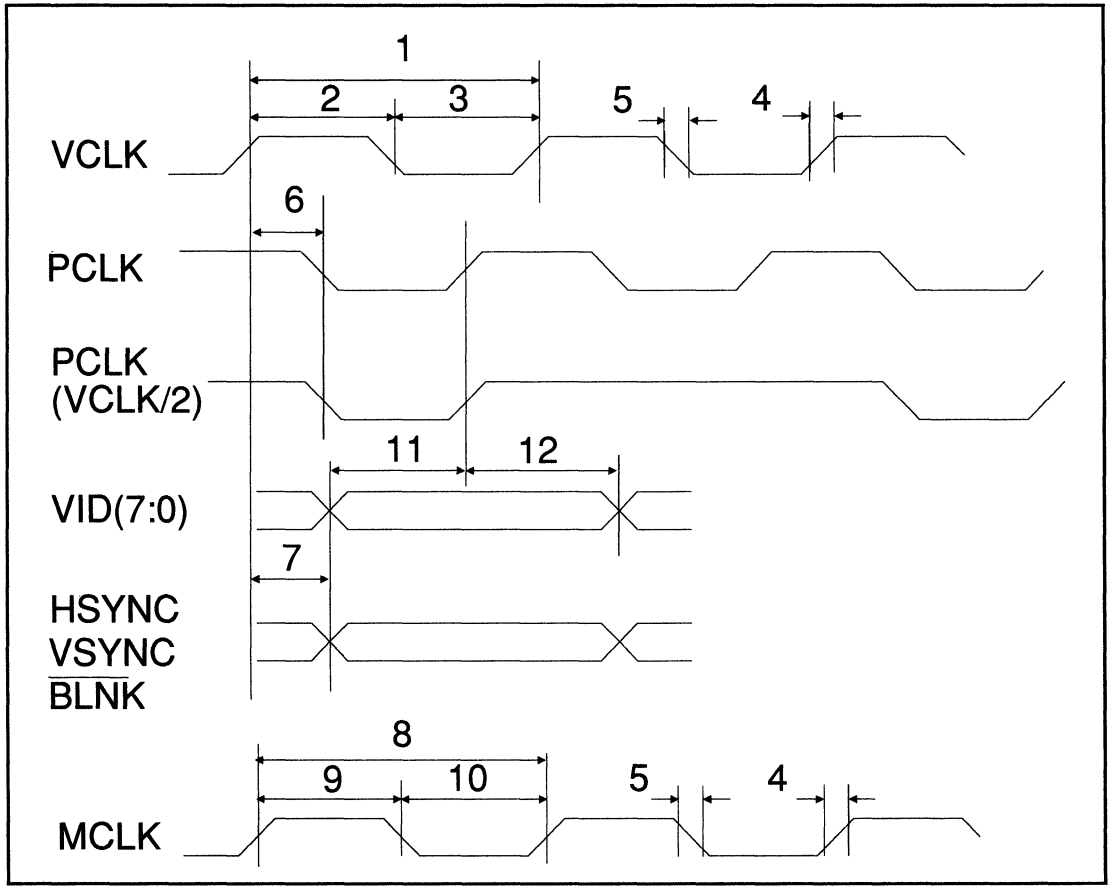


FIGURE 5. CLOCK AND VIDEO TIMING

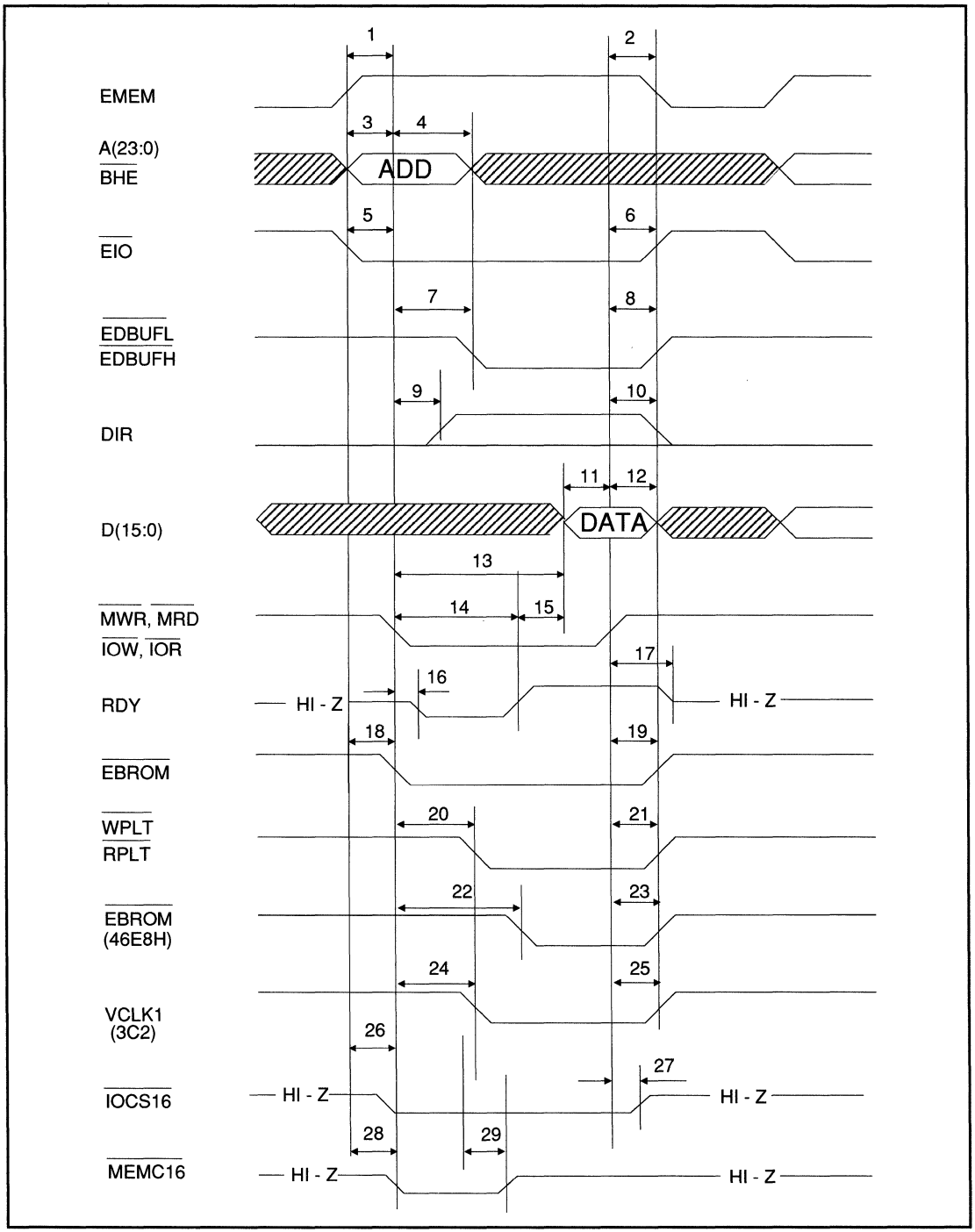


FIGURE 6. AT MODE BUS TIMING

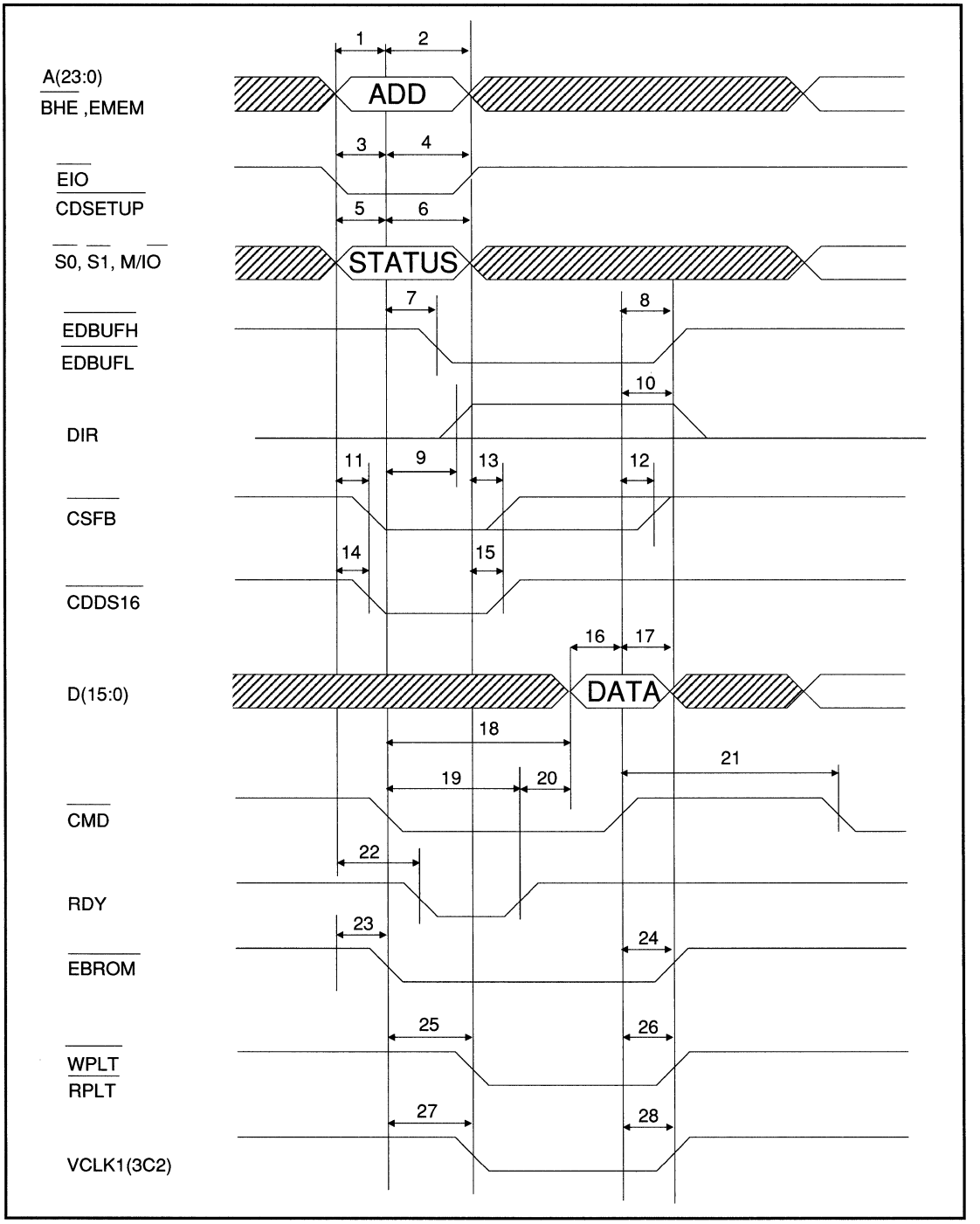


FIGURE 7. MICRO CHANNEL MODE BUS TIMING

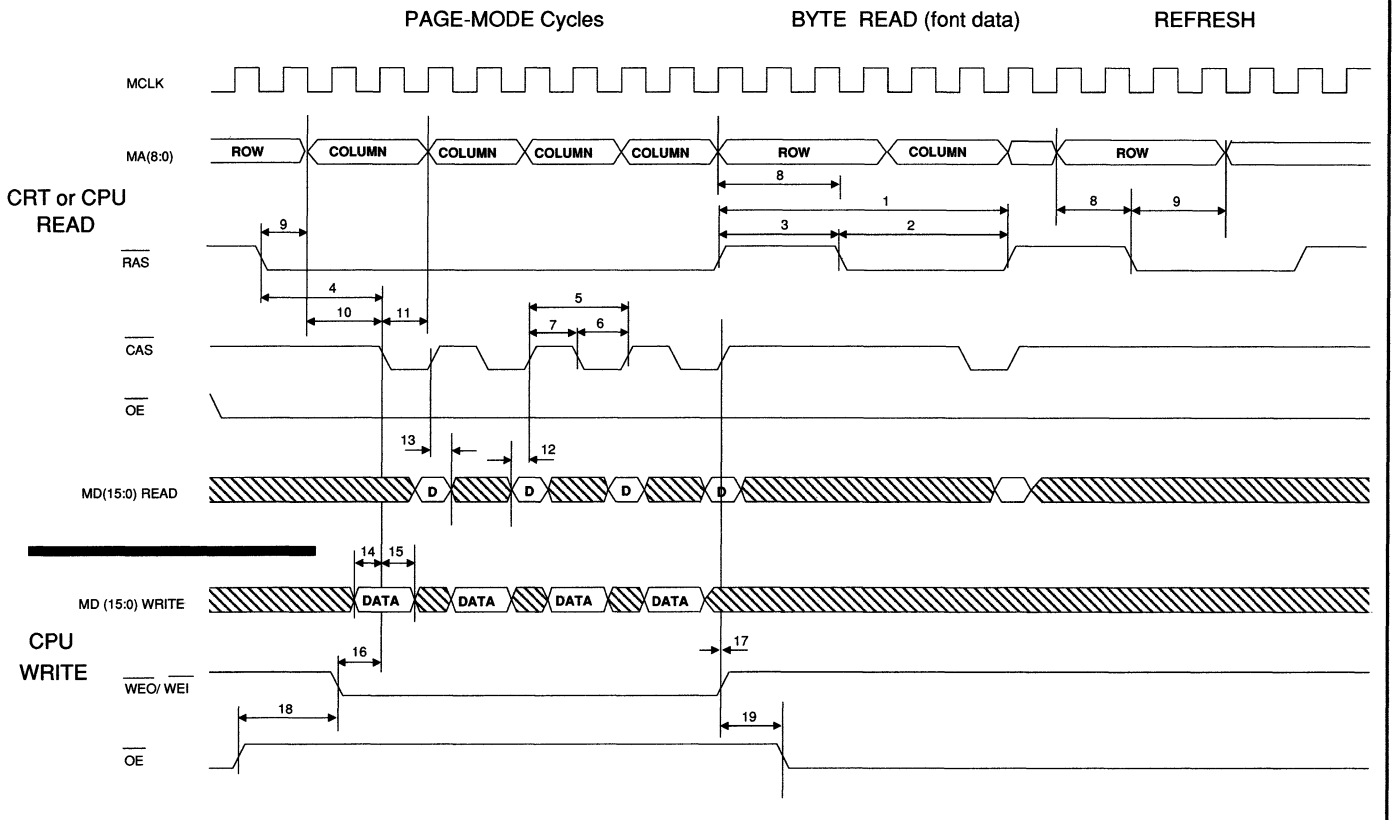


FIGURE 8. DRAM TIMING

7.0 WD90C11 REGISTERS

All the standard IBM registers incorporated inside the WD90C11 are functionally equivalent to the VGA implementation while additional Western Digital registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards defined earlier using the 6845 CRT Controller. This section describes the VGA registers in greater detail, followed by the VGA/EGA difference section and PR registers description. For more information, refer to the reference literature.

7.1 VGA REGISTERS SUMMARY

REGISTERS	RW	MONO	COLOR	EITHER
GENERAL REGISTERS				
Miscellaneous Output Reg	W			3C2
	R			3CC
Input Status Reg 0	RO			3C2
Input Status Reg 1	RO	3BA	3DA	
Feature Control Reg	W	3BA	3DA	
	R			3CA
*Video Subsystem Enable	RW			3C3
AT Mode Setup and Enable	W			46E8
Setup Video Enable	RW			102
* I/O Port 3C3 can be used to replace 46E8 (if CNF (9) = 0) for setup in AT mode. In Micro Channel mode, writes to 3C3, bit 0 = 1 enables memory and I/O address decoding.				
SEQUENCER REGISTERS				
Sequencer Index Reg	RW			3C4
Sequencer Data Reg	RW			3C5
CRT CONTROLLER REGISTERS				
Index Reg	RW	3B4	3D4	
CRT Controller Data Reg	RW	3B5	3D5	
GRAPHICS CONTROLLER REGISTERS				
Index Reg	RW			3CE
Other Graphics Reg	RW			3CF
ATTRIBUTE CONTROLLER REGISTERS				
Index Reg	RW			3C0
Attribute Controller Data Reg	W			3C0
	R			3C1
VIDEO DAC PALETTE REGISTERS				
Write Address	RW			3C8
Read Address	W			3C7
DAC State	R			3C7
Data	RW			3C9
Pel Mask	RW			3C6

1. RO = Read-Only, RW = Read/Write, W = Write, and R = Read.
2. All Register addresses are in hex.

TABLE 5. VGA REGISTERS SUMMARY

7.2 PR REGISTERS SUMMARY

REGISTERS	RW	MONOCHROME	COLOR
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
Reserved 3X5.31- 3X5.3F	RW	3B5.31 - 3B5.3F	3D5.31 - 3D5.3F
** CNF Configuration	-----	-----	-----
PR20 Unlock Sequencer Extended Registers	W	3C5.06	3C5.06
PR21Display Configuration and Scratch Pad	RW	3C5.07	3C5.07
PR30 Memory Interface and FIFO Control	RW	3C5.10	3C5.10
PR31 System Interface Control	RW	3C5.11	3C5.11
PR32 Miscellaneous Control 4	RW	3C5.12	3C5.12

NOTE:
All of the PR Registers may be read/write protected. Refer to the PR Registers' description for more details.

7.3 COMPATIBILITY REGISTERS SUMMARY

FUNCTIONS	RW	MDA	CGA	AT&T	HERCULES
Mode Control Reg	WO	3B8	3D8	3D8	3B8
Color Select Reg	WO		3D9	3D9	
Status Reg	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Reg	WO			3DE	
Hercules Reg	WO				3BF
+CRTC	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

NOTES:
1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. + = 6845 Mode Registers.
4. ** = This register is loaded during power on.

7.4 VGA REGISTERS

Throughout this section, all bit graphics and definitions apply to VGA mode followed by their brief description.

7.5 GENERAL REGISTERS

NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES:

1. Reserved bits should be set to zero.

2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes

   1 = D in Color Modes

7.5.1 Miscellaneous Output Register, Read Port = 3CC, Write Port = 3C2

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.
0= Positive vertical sync polarity.
1= Negative vertical sync polarity.

Bit 6 *

Horizontal Sync Polarity Selection.
0= Positive horizontal sync polarity.
1= Negative horizontal sync polarity.

NOTE:

*These bits determined the vertical size of the frame by the monitor. Their encoding is shown below:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.
When in modes 0-5, one memory page is selected from the two 64KB pages.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bit(3:2) Clock Select 1,0.

BIT 3	BIT 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

Bit 1

System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection. Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0= CRTC and status addresses for MDA mode (3BX).
1= CRTC and status addresses for CGA mode (3DX).

7.5.2 Input Status Register 0, Read Only Port = 3C2

BIT	FUNCTION
7	CRT Interrupt
6, 5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3: 0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit(6:5)

Reserved in VGA.

Bit 4

Monitor Detection in VGA mode. MDET monitor status (pin 112) is sampled and can be read from this bit.

Bit(3:0)

Reserved.

7.5.3 Input Status Register 1, Read Only Port = 3?A

BIT	FUNCTION
7, 6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved
0	Display Enable

Bit(7:6)

Reserved.

Bit(5:4)

Color Plane Diagnostics.
These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.
0= Vertical frame is displayed.
1= Vertical retrace is active.

Bit(2:1)

Reserved.

Bit 0

Display Enable Status.
0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

7.5.4 Feature Control Register, Read Port = 3CA, Write Port = 3?A

BIT	FUNCTION
7 - 4	Reserved
3	Vertical Sync Control
2 - 0	Reserved

Bits(7:4)

Reserved

Bit 3

Vertical Sync Control:
0: Vsync output enabled
1: Vsync output is logical "OR" of Vsync and Vertical Display Enable.

Bit(2:0)

Reserved

7.6 SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE: Reserved bits should be set to zero.

7.6.1 Sequencer Index Register, Read/Write Port = 3C4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Sequencer Address/Index Bits

Bit(7:3)

Reserved.

Bit(2:0)

Sequencer Address/Index.
The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer register to be accessed.

7.6.2 Reset Register, Read/Write Port = 3C5, Index = 00

BIT	FUNCTION
7 - 2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bit(7:2)

Reserved.

Bit 1

Synchronous Reset.
0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0

Asynchronous Reset.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

7.6.3 Clocking Mode Register, Read/Write Port = 3C5, Index = 01

BIT	FUNCTION
7, 6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bit(7:6)

Reserved.

Bit 5

Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character or every other character clock depending on bit 2.
1 = Serial shift registers loaded every 4th character clock (32 bit fetches).

Bit 3

Dot Clock Selection
0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360 pixels).

Bit 2

Shift Load. Effective only if bit 4=0.
0 = Video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.
Commands Sequencer to generate 8 or 9 dot wide character clock.
0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

7.6.4 Map Mask Register, Read/Write Port = 3C5, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bit(7:4)

Reserved.

Bit(3:0)

Controls Writing To Memory Maps (0-3) respectively.
0 = Writing to maps (0-3) disallowed.
1 = Maps (0-3) accessible.

7.6.5 Character Map Select Register Read/Write Port = 3C5, Index = 03

BIT	FUNCTION
7, 6	Reserved
5	Character Map Select A Bit 2
4	Character Map Select B Bit 2
3	Character Map Select A Bit 1
2	Character Map Select A Bit 0
1	Character Map Select B Bit 1
0	Character Map Select B Bit 0

If Sequencer Register 4 bit 1 is 1, then the attribute byte bit 3 in text modes is redefined to control switching between character sets. A 0 selects character map B. A 1 selects character map A. Character Map selection from either plane 2 or plane 3 is determined by PR2(2), PR2(5) and bit 4 of the attribute code.

Bit(7:6)

Reserved.

Bit 5

Character Map A MSB Select.
The Most Significant Bit (MSB) of character map A along with bits 3 and 2, select the location of character map A as shown below.

BITS 5 3 2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit 4

Character Map B MSB Select.
The MSB of character map B along with bits 1 and 0, select the location of character map B as shown below.

BITS 4 1 0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit(3:2)

Character Map Select A.
Refer to bit 5 table.

Bit(1:0)

Character Map Select B.
Refer to bit 4 table.

7.6.6 Memory Mode Register, Read/Write Port = 3C5, Index = 04

BIT	FUNCTION
7 - 4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bit(7:4)

Reserved.

Bit 3

Chains 4 Maps.
0 = Processor sequentially accesses data using map mask register.
1 = Directs the two lower order video memory address pins (MA0,MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.
0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.
1 = Sequential processor access as defined by map mask register.

Bit 1

Extended Video Memory.
0 = 64 KB of video memory.
1 = Greater than 64KB of memory for VGA/EGA modes.

Bit 0

Reserved.

7.7 CRT CONTROLLER REGISTERS

PORT	INDEX	VGA REGISTER NAME	*6845 REG NAME
3?4	---	CRT Controller Address Reg.	CRTC Address Reg
3?5	00	Horizontal Total	Hor. Total
3?5	01	Horizontal Display Enable End	Hor. Disp
3?5	02	Start Horizontal Blanking	+
3?5	03	End Horizontal Blanking	+
3?5	04	Start Horizontal Retrace	+
3?5	05	End Horizontal Retrace	+
3?5	06	Vertical Total	+Vert. Disp.
3?5	07	Overflow	+
3?5	08	Preset Row Scan	+
3?5	09	Maximum Scan Line/Others	Max. Scan Line Add.
3?5	0A	Cursor Start	Cursor Start
3?5	0B	Cursor End	Cursor End
3?5	0C	Start Address High	Start Add. High
3?5	0D	Start Address Low	Start Add. Low
3?5	0E	Cursor Location High	Cursor Loc. High
3?5	0F	Cursor Location Low	Cursor Loc. Low
3?5	10	Vertical Retrace Start	Light Pen High Read
3?5	11	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	
3?5	13	Offset	+
3?5	14	Underline Location	+
3?5	15	Start Vertical Blank	+
3?5	16	End Vertical Blank	+
3?5	17	CRTC Mode Control	+
3?5	18	Line Compare	+

TABLE 6. CRT CONTROLLER REGISTERS

NOTES:

1. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0=B in Monochrome Modes and
1=D in Color Modes

2. "*" 6845 Mode Registers are defined and explained in greater in the reference literature.

3. "+" This register can be programmed in VGA mode only. It is not applicable in 6845 mode.

4. Reserved bits should be set to zero.

7.7.1 CRT Address Register Read/Write Port = 3?4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Index bits

Bit(7:5)

Reserved.

Bit(4:0)

Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed hex.

7.7.2 Horizontal Total Register Read/Write Port = 3?5, Index=00H

BIT	FUNCTION
7 - 0	Horizontal Total Period

Bit(7:0)

Count Plus Retrace Less 5.

In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line.

7.7.3 Horizontal Display Enable End Register Read/Write Port = 3?5, Index 01H

BIT	FUNCTION
7 - 0	Displayed Characters per scan line

Bit(7:0)

The total displayed characters less one are programmed in this register. This register is locked if PR3(5) = 1 or the Vertical Retrace End Register bit 7= 1.

7.7.4 Start Horizontal Blanking Register Read/Write Port = 3?5, Index = 02H

BIT	FUNCTION
7 - 0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches this character clock value. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

7.7.5 End Horizontal Blanking Read/Write Port = 3?5, Index = 03H

BIT	FUNCTION
7	Reserved
6, 5	Display Enable Signal Skew Control
4 - 0	End Horizontal Blanking (lower 5 bits)

This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

Bit 7

Reserved

Bit(6:5)

Display Enable Signal Skew Control.
They define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

BIT 6	BIT 5	SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

End Horizontal Blanking.
End Horizontal Blank signal width "W" is determined as the value of start blanking register plus "W" in character clocks. The least significant five bits are programmed in this register, while the most significant bit is the End Horizontal Retrace Register (Index 05H) bit 7.

7.7.6 Start Horizontal Retrace Pulse Register Read/Write Port = 3?5, Index = 04H

BIT	FUNCTION
7 - 0	Start Horizontal Retrace Character Count

Bit(7:0)

Start Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

7.7.7 End Horizontal Retrace Register Read/Write Port = 3?5, Index = 05H

BIT	FUNCTION
7	End Horizontal Blank bit 6
6, 5	Horizontal Retrace Delay
4 - 0	End Horizontal Retrace

This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

Bit 7

MSB (Sixth Bit) Of End Horizontal Blanking Register.

Bit(6:5)

Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

BIT 6	BIT 5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

Bit(4:0)

End Horizontal Retrace Pulse Width "W".
Start retrace register value is added to the character count for width "W". The least significant five bits are programmed in this register. When the Start Horizontal Retrace Register value matches these five bits, the horizontal retrace signal is turned off.

7.7.8 Vertical Total Register Read/Write Port = 3?5,Index = 06H

BIT	FUNCTION
7 - 0	Vertical Total Scan Lines

Bit(7:0)

Raster Scan Line Total Less 2.
The least significant eight bits of a ten bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync are also included. The ninth and tenth bits of this count are loaded into the Vertical Overflow Register (index = 07H) bit 0 and bit 5 respectively. In 6845 modes, total vertical display time in rows is programmed into bit 6 - bit 0, while bit 7 is reserved. Scan count reduction is not necessary. (The number of scan lines in a row is determined by the maximum Scan Line Register (index 09H bits 0 through 4). This register is locked if the PR Register PR3 (0) = 1 or the Vertical Retrace End Register bit 7 = 1.

7.7.9 Overflow Vertical Register Read/Write Port = 3?5, Index = 07H

BIT	FUNCTION
7	Vert. Ret. Start Bit 9
6	Vert. Display Enable End Bit 9
5	Vert. Total Bit 9
4	Line Compare Bit 8
3	Start Vert. Blank Bit 8
2	Vert. Ret. Start Bit 8
1	Vert. Display Enable End Bit 8
0	Vert. Total Bit 8

++Bit 7

Vertical Retrace Start Bit 9 (index = 10H).

****Bit 6**

Vertical Display Enable End Bit 9 (index = 12H).

++Bit 5

Vertical Total Bit 9 (index = 06H).

Bit 4

Line Compare Bit 8 (index = 18H).

++Bit 3

Start Vertical Blank Bit 8 (index =15H).

++Bit 2

Vertical Retrace Start Bit 8 (index = 10H).

****Bit 1**

Vertical Display Enable End Bit 8 (index = 12)

++ Bit 0

Vertical Total Bit 8 (index = 06H)

NOTES:

+ This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

** This register is locked if the PR Register PR3(1)=0 AND the Vertical Retrace End Register bit 7 = 1.

++ This register is locked if the PR Register PR3(0) = 1 OR the Vertical Retrace End Register bit 7 = 1.

7.7.10 Preset Row Scan Register Read/Write Port = 3?5, Index = 08H

BIT	FUNCTION
7	Reserved
6, 5	Byte Panning Control
4 - 0	Preset Row Scan Count

Bit 7

Reserved.

Bit(6:5)

Byte Panning Control.
These bits allow up to 3 bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 byte left shift
1	0	2 bytes left shift
1	1	3 bytes left shift

Bit(4:0)

Preset Row Scan Count.
These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

7.7.11 Maximum Scan Line Register Read/Write Port=3?5, Index=09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare bit 9
5	Start Vertical Blank bit 9
4 - 0	Maximum Scan Line

Bit 7

200 To 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.
This is bit 9 of the Line Compare Register (index = 18H).

Bit 5

Start Vertical Blank.
This is bit 9 of the Start Vertical Blank Register (index = 15H). This register is locked if the PR Register PR3 (0) = 1.

Bit(4:0)

Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, bits 5-7 are reserved, and bits 4-0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported.

7.7.12 Cursor Start Register Read/Write Port = 3?5, Index = 0AH

BIT	FUNCTION
7, 6	Reserved
5	Cursor Control
4 - 0	Cursor Start Scan Line

Bit(7:6)

Reserved.

Bit 5

Cursor Control.
0=Cursor on.
1=Cursor off.

Bit(4:0)

These bits specify the row scan counter value within the character box where the cursor begins. These bits contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0BH), no cursor is generated. For 6845 modes, bit 7 is reserved. Bit 5 controls the cursor operation and bits 4-0 contain the cursor start value. Bit 6 is not used.

7.7.13 Cursor End Register Read/Write Port = 3?5h, Index = 0BH

BIT	FUNCTION
7	Reserved
6, 5	Cursor Skew
4 - 0	Cursor End Scan Line

Bit 7

Reserved.

Bit(6:5)

Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the table below.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

Cursor End Scanline
These bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, bits 7-5 are reserved and bits 4-0 contain row value of the cursor end.

NOTE: There are three types of cursors generated, depending upon the mode i.e, EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

7.7.14 Start Address High Register Read/Write Port 3?5H, Index = 0CH

BIT	FUNCTION
7 - 0	Start Address High Byte

Bit(7:0)

Display Screen Start Address Upper Byte Bits.
Eight high order bits of the 16 bit video memory address, used for screen refresh. The low order eight bit register is at index 0DH. The PR Register PR3 bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes bits 6 & 7 are forced to 0 regardless of this register's contents, while the lower order 8 bits are at index register 0DH.

7.7.15 Start Address Low Register Read/Write Port = 3?5H, Index = 0DH

BIT	FUNCTION
7 - 0	Start Address Low Byte

Bit(7:0)

The lower order eight bits of the 16 bit video memory address in VGA or 6845 modes.

9.7.16 Cursor Location High Register Read/Write Port = 3?5h, Index = 0Eh

BIT	FUNCTION
7 - 0	Cursor Location High Byte

Bit(7:0)

Cursor Address Upper Byte Bits.
The eight higher order bits of 16 bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0FH. In VGA mode, the PR Register PR3 bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, bits 6 and 7 are reserved, while bits 5 - 0 are the high order bits of the cursor.

7.7.17 Cursor Location Low Register Read/Write Port = 3?5, Index = 0FH

BIT	FUNCTION
7 - 0	Cursor Location Low Byte

Bit(7:0)

Cursor Address Lower Byte Bits.
The lower order eight bits of the 16 bit video memory address in VGA or 6845 mode.

7.7.18 Vertical Retrace Start Register Read/Write Port = 3?5, Index=10H

BIT	FUNCTION
7 - 0	Vertical Retrace Start (Lower eight bits)

Bit(7:0)

Vertical Retrace Start Pulse Lower Eight Bits.
The lower eight bits of the ten bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07H). In 6845 compatible mode, this register shows the high order six bits in positions 5 - 0 as the light pen read back value, and bits 6 an 7 are reserved. The lower order eight bits of the light pen read back register are at the index 11H. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3 (0) = 1.

7.7.19 Vertical Retrace End Register Read/Write Port = 3?5, Index = 11H

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3 - 0	Vertical Retrace End

This register is locked if the PR Register PR3(0)=1.

Bit 7

CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller index registers in the range of index 00H-07H. The line compare bit 4 in the Overflow Register (07H) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.
Selects DRAM refresh cycles per horizontal scan line.
0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.
0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4

Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by resetting (writing a 0 to) and internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

Bit(3:0)

Vertical Retrace End.
They specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan counter for "W" to the value of the Vertical Retrace Start Register. The 4 bit result is written in the Vertical Retrace End Register. In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of Light Pen Register.

7.7.20 Vertical Display Enable End Register Read/Write Port = 3?5, Index = 12H

BIT	FUNCTION
7 - 0	Vertical Display Enable End (Lower eight bits)

Bit(7:0)

Vertical Display Enable End Lower Eight Bits.
The eight lower bits of ten bit register that defines where the active display frame ends.
The programmed count is in scan lines minus 1. Bits 8 and 9 are in the Overflow Register (index 07H) at positions 1 and 6 respectively.

7.7.21 Offset Register Read/Write Port = 3?5, Index = 13H

BIT	FUNCTION
7 - 0	Logical Line Screen width

Bit(7:0)

Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:
Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K=2 in byte mode and K=4 in word mode.

7.7.22 Underline Location Register Read/Write Port = 3?5, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4 - 0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5

Count By 4 For Double word Access
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit(4:0)

Underline Location.
These bits specify the row scan counter value within a character matrix where under line is to be displayed. Load a value 1 less than the desired scan line number.

7.7.23 Start Vertical Blank Register Read/Write Port = 3?5, Index =15H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	Start Vertical Blank (Lower eight bits)

Bit(7:0)

Start Vertical Blank Lower Eight Bits.
The lower eight bits of the ten bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). The ten bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

7.7.24 End Vertical Blank Register Read/Write Port=3?5, Index=16H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	End Vertical Blank

Bit(7:0)

Vertical Blank inactive Count.
End Vertical Blank is an 8 bit value calculated as follows:
8 Bit End Vertical Blank value =
(value of Start Vertical Blank minus 1) + (value of Vertical Blank signal width in scan lines).

7.7.25 CRT Mode Control Register Read/Write Port = 3?5, Index = 17H

This register is locked if PR Register PR3(5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.
0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word Or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by 1 bit and the MSB of the address counter appears on the LSB. See the table below.
1 = Byte address mode.

MEMORY ADDRESS	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLEWORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE:
* See bit 5, defining address wrap. This table is only applicable when PR Register PR1 bits 7 and 6 equal zero, or PR16 bit 1 equals one.
The CRT Underline Location Register (index = 14H) bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) bit 6 controls addressing. See the table below:

CRT14H	CRT17H	ADDRESS
Bit 6	Bit 6	Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.
0 = In word address mode, this bit enables bit 13 to appear at MA0, otherwise bit 0 appears on MAO.
1 = Select MA15 for odd/even mode when 256KB of video memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2
0 = Character clock increments memory address counter.
1 = Character clock divided by 2 increments the address counter.

Bit 2

Horizontal Retrace Clock Rate Select For Vertical Timing Counter.
0 = Selects horizontal retrace clock rate
1 = Selects horizontal retrace clock rate divided by 2.

Bit 1

Select Row Scan Counter.
0 = Selects row scan counter bit 1 as output at MA14 address pin.
1 = Selects bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0

6845 CRT Controller compatibility mode support for CGA operation.
0 = Row scan address bit 0 is substituted for memory address bit 13 at MA13 output pin during active display time.
1 = Enable memory address pin 13 to be output at MA13 address pin.

7.7.26 Line Compare Register Read/Write Port = 3?5, Index = 18H

BIT	FUNCTION
7 - 0	Line Compare (lower eight bits)

Bit(7:0)

Line Compare Lower Eight Bits.
Lower eight bits of the ten bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared.

7.8 GRAPHICS CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

NOTE:
1. Reserved bits should be set to zero.

7.8.1 Graphics Index Register, Read/Write Port = 3CE

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Graphics Address Bits

Bit(7:4)

Reserved.

Bit(3:0)

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

7.8.2 Set/Reset Register, Read/Write Port 3CF, Index = 00

BIT	FUNCTION
7 - 4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined below:
0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE:
*The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05H) bit 1 and bit 0.

7.8.3 Enable Set/Reset Register, Read/Write Port = 3CF, Index = 01

BIT	FUNCTION
7 - 4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Enable Set/Reset Register (Index 00H).

0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00H) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.
1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00H), and the respective memory map is written with the Set/Reset Register value.

7.8.4 Color Compare Register, Read/Write PORT 3CF, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Color Compare.
The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a 1 is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05H), data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

7.8.5 Data Rotate Register, Read/Write Port = 3CF, Index = 03

BIT	FUNCTION
7 - 5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count 2 Bit 2
1	Rotate Count 1 Bit 1
0	Rotate Count 0 Bit 0

Bit(7:5)

Reserved.

Bit(4:3)

Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05H) is defined as follows.

BIT 4	BIT 3	FUNCTION
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches

Bit(2:0)

Rotate Count.
It specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05H).

7.8.6 Read Map Select Register, Read/Write Port = 3CF, Index = 04

BIT	FUNCTION
7 - 2	Reserved
1	Map Select 1
0	Map Select 0

Bit(7:2)

Reserved.

Bit(1:0)

Map Select.
These bits select memory map in system read operations. It has no effect on color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained maps 0 & 1 or value 10b or 11 to select the chained maps 2 & 3. Map read is defined as shown below.

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

7.8.7 Graphics Mode Register, Read/Write Port = 3CF, Index = 05

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7

Reserved.

Bit 6

256 Color Mode.
0 = Enables bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID6, VID7) are determined by bits 2 and 3 of the Color Select Register located at index = 14H within the Attribute Controller.
1 = Load video shift registers to support 256 color mode.

Bit 5

Shift Register.
Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.
0 = Map 0 - Map 3 data is placed into shift registers for normal operations.
1 = For CGA graphics mode compatibility, even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.
0 = normal
1 = CGA compatible odd/even system access mode. Sequential addressing as defined by bit 2 of the memory mode register (index = 04H) in the Sequencer Register. Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3

Read Mode.
0 = System reads data from memory maps selected by Read Map Select Register (index 04H). This setting will have no effect if bit 3 of the Sequencer Memory Mode Register = 1.
1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved.

Bit(1:0)

Write Mode.
The following table defines the four write modes.

BIT 1	BIT 0	WRITE MODE
0	0	Write Mode 0. If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	Write Mode 1. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	Write Mode 2. Memory maps (3:0) are filled with the 8-bit value of the corresponding CPU data bits (3:0). The 32 bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	Write Mode 3. Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

7.8.8 Miscellaneous Register, Read/Write Port = 3CF, Index = 06

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bit(7:4)

Reserved.

Bit(3:2)

Memory Map 1, 0
Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0H-BFFF:FH	128KB
0	1	A000:0H-AFFF:FH	64KB
1	0	B000:0H-B7FF:FH	32KB
1	1	B800:0H-BFFF:FH	32KB

Bit 1

Odd/Even Mode.
0 = CPU address bit A0 is the memory address bit MA0.
1 = CPU address bit A) is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode
This bit is programmed the same way as bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selects.
1 = Graphics mode selected.

7.8.9 Color Don't Care Register, Read/Write Port 3CF, Index = 07

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Memory Map Color Compare Operation.

0 = Disable color compare operation.
1 = Enable color compare operation.

7.8.10 Bit Mask Register, Read/Write Port = 3CF, Index = 08

BIT	FUNCTION
7 - 0	Bit Mask

Bit(7:0)

Bit mask operation applies simultaneously to all the four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

7.9 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CO	——	Index Register
3CO	00-0F	Palette Registers
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

NOTES:
1. Each attribute data register is written at 3C0 and register data is read from address 3C1.
2. Reserved bits should be set to zero.
3. ? " Value is controlled by Bit 0 of the Miscellaneous Output register and is programmed as follows:

0 = B in Monochrome Modes and
1 = D in Color Modes

7.9.1 Attribute Index Register, Read/Write Port = 3C0

BIT	FUNCTION
7 - 6	Reserved
5	Palette Address Source
4 - 0	Attribute Address Bits

Bit(7:6)

Reserved.

Bit 5

Palette Address Source.
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 - 0FH).
1 = Enable internal color palette and normal video translation.

Bit(4:0)

Attribute Controller Index Register Address Bits
NOTE:
The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 3?A) clears the flip-flop and selects the Address Register, which is read thru address 3C1 and written at address 3C0. Once the Address Register has been loaded with an index, the next write operation to 3C0 will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address hex 3C0, but does not toggle for reads to address 3C1.

7.9.2 Palette Registers (00-0F Hex), Read Port 3C1/Write Port 3C0

BIT	FUNCTION
7 - 6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:6)

Reserved.

Bit(5:0)

Palette Pixel Colors.
They are defined as follows:
0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the table below.

Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

7.9.3 Attribute Mode Control Register Read Port 3C1/Write Port 3C0, Index = 10

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7

VID5, VID4 Select
0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14H) bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6

Pixel Width
0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.
1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility
Line Compare in the CRT Controller.
0 = A Line compare will have no effect on the PEL Panning Register.
1 = Allows a successful line compare to disable the PEL Panning Register and also bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4

Reserved.

Bit 3

Background Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code.
Set this bit to zero for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes

Bit 0

Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

7.9.4 Overscan Color Register Read Port 3C1/Write Port 3C0, Index = 11

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:0)

Overscan/Border Color.
They determine the overscan or border color. For monochrome display, this register is set to 0. Border colors are set as shown above.

7.9.5 Color Plane Enable Register Read Port 3C1/Write Port 3C0, Index = 12

BIT	FUNCTION
7 - 6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3 - 0	Enable Color Plane

Bit(7:6)

Reserved.

Bit(5:4)

Video Status Control.
These bits select 2 out of 8 color outputs which can be read by the Input Status Register 1 (port = 03?A) bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit(3:0)

Color Plane Enable.
0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

7.9.6 Horizontal Pel Panning Register Read Port 3C1/Write Port 3C0, Index = 13

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Horizontal PEL Panning

Bit(7:4)

Reserved.

Bit(3:0)

Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to 3 position pixel shift can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Character	8 dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7.9.7 Color Select Register Read Port 3C1/Write Port 3CO, Index = 14

BIT	FUNCTION
7 - 4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bit(7:4)

Reserved.

Bit(3:2)

Color Value MSB.
Two most two significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6

Bit(1:0)

Substituted Color Value Bits.
These bits can be substituted for VID5 an VID4 output by the Attribute Controller palette registers, to create eight bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10H).

7.10 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting PR Register PR2(6) = 1.

2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting PR Register PR2(7) = 1.

3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0 = B in Monochrome Modes
1 = D in Color Modes

7.10.1 Hercules/MDA Mode Control Register, MDA Operation Write Only Port = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode. If Bit 1=1 and Port 3BFH bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5

Enable Blink.
0 = Disable Blinking
1 = Enable Blinking

Bit 4

Reserved.

Bit 3

Video enable.
0 = Video Disable
1 = Video activated

Bit 2

Reserved.

Bit 1

Port 3BFH enable.
0 = Prevents setting of Port 3BF bit 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFh bit 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode. Should be 1.
0 = High resolution disabled.
1 = High resolution is enabled.

7.10.2 Hercules Registers

The Hercules Mode Register is a 2-bit write only register located at I/O port address 3BF. It affects the device operation only in the 6845 mode. The enable mode register located at the address 3B8 overrides the write port 3BF functions defined by its bits 0 and 1. The associated details are shown below.

7.10.3 Enable Mode Register 3B8

BIT	FUNCTION
7	Display Memory Page Address Graphics Mode
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BF Bit 0 Override
0	High Resolution Mode = 1

Bit 7

Display Memory Page Address In Graphics Mode.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit (6:2,0)

Not Applicable.

Bit 1

Port 3BF Bit 0 Override.
0 = Prevents setting of Port 3BF bit 0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BF bit 0 to switch for the alpha or graphics mode selection.

7.10.4 Hercules Compatibility Register Write Only Port = 3BFH

BIT	FUNCTION
7 - 2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)

Reserved.

Bit 1

Upper Memory Page Address.
Enable Mode Control Register (3B8) bit 7 selects the displayed memory page address in the graphics mode. When it is reset, bit 1 prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.
0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics.
Allows the Enable Mode Register (3B8) bit 1 to override.
0 = Alpha mode display.
1 = Graphics modes may be displayed.

7.10.5 Color CGA Operation Register, Write Only Port = 3D8

BIT	FUNCTION
7, 6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bit (7:6)

Reserved.

Bit 5

Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4

B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3

Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = B/W mode enabled.

Bit 2

B/W or Color Display Mode.
0 = Color Mode Selected.
1 = B/W Mode Selected.

Bit 1

Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = graphics mode (320 by 200) activated.

Bit 0

(40 by 25) or (80 by 25) Text Mode Selection.
0 = 40 by 25 alpha mode enabled.
1 = 80 by 25 alpha mode activated.

7.10.6 CGA Color Select Register Write Only Port = 3D9

BIT	FUNCTION
7, 6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bit (7:6)

Reserved.

Bit 5

320 by 200 Color Set Select for the CGA 2 bits per pixel.
0 = Background, green, red, brown colors.
1 = Background, cyan, magenta, white colors.

Bit 4

Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = enable alternate color set in graphics mode.

Bit 3

Border Intensity.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 2

Red Border/Background
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects red border color.
320 by 200 Graphics Mode.
1 = Selects red background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 1

Green Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

Bit 0

Blue Border/Background.
border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Select blue background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

7.10.7 CRT Status Register MDA Operation, Read Only Port = 3BA

BIT	FUNCTION
7	VSYNC Inactive
6 - 4	Reserved
3	B/W Video Enabled
2 - 1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.
0 = Indicates the raster is in vertical retrac e mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bit (6:4)

reserved.

Bit 3

B/W Video Status.
0 = B/W Video disabled.
1 = B/W Video enabled.

Bit 2 - Bit 1

Reserved.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

7.10.8 CRT Status Register CGA Operation, Read Only Port = 3DA

BIT	FUNCTION
7 - 4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bit (7:4)

Reserved.

Bit 3

Vertical Retrace.
0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode.

Bit 2

Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open

Bit 1

Light Pen Latch.
0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking active; Display Enable is inactive.

7.10.9 AT&T/M24 Register, Write Only Port = 3DE

This is a write only, 8-bit register located at address 3DE. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting bit 7 in PR Register 2 (PR2).

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5, 4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in-color text modes.
1 = Underline attribute selects white underlined foreground.

Bit (5:4)

Reserved.

Bit 3

Page Select.
Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B800:0H (16 KB length).
1 = Display memory address starts at BC00:0H (16 KB length).

Bit 2

Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or Non-IBM Graphics Mode. 400 line mode. A 400 line monitor is required for this mode.
0 = 200 line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400 line graphics.

7.11 WD90C11 PR REGISTERS

REGISTERS	RW	MONOCHROME	COLOR
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
Reserved 3X5.31- 3X5.3F	RW	3B5.31 - 3B5.3F	3D5.31 - 3D5.3F
CNF Configuration (loaded during power-on)	-----	-----	-----
PR20 Unlock Sequencer Extended Registers	W	3C5.06	3C5.06
PR21Display Configuration and Scratch Pad	RW	3C5.07	3C5.07
PR30 Memory Interface and FIFO Control	RW	3C5.10	3C5.10
PR31 System Interface Control	RW	3C5.11	3C5.11
PR32 Miscellaneous Control 4	RW	3C5.12	3C5.12

NOTE:
All of the PR Registers may be read/write protected.

TABLE 7. PR REGISTERS SUMMARY

The WD90C11 has additional features that enhance the performance and functions of the Western Digital Imaging PVGA1A, introduced earlier, and the basic VGA subsystem. To accomplish this, the WD90C11 architecture is optimized with additional I/O registers.

The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

NOTES:

1. The designation 3?5 means that the register is mapped into either 3B5 in monochrome mode or 3D5 in color modes.

2. PR register notation - XXX.YY where XXX is the data port address and YY is the register index e.g. 3CF.0F implies 0F--3CEH (Select Index register) followed by (Data byte) -- 3CF (Data Port).

Registers PR0 through PR4 and PR11 through PR17 are normally locked. They are write protected at power-up by the hardware reset. In order to load those registers, the appropriate unlock register PR5 or PR10 must be loaded first with binary XXXXX101; a register remains unlocked until any other value is written to the unlocked register. Registers PR0 through PR5 are readable only if PR4 bit 1 = 0. Registers PR10 through PR17 are read protected at power up by hardware reset. In order to read registers PR10 through PR17 load PR10 with 1XXX0XXX. The register remains readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them would show data to be FFH. Setting PR4 bit 1 to 1 does not read protect registers PR10 through PR17. All PR registers are set to 0 at power on reset except where noted.

7.11.1 Address Offset Registers PROA & PROB

PROA - Address Offset Register A
Read/Write Port = 3CF, Index = 09

BIT	FUNCTION
7	Reserved
6 - 0	Primary Address Offset Bits

PROB - Address Offset Register B
Read/Write Port = 3CF, Index = 0A

BIT	FUNCTION
7	Reserved
6 - 0	Alternate Address Offset Bits

The WD90C11 can control up to 512 Kbytes of display memory. However, DOS only assigns 128 Kbytes total memory space for display memory, which starts at A0000H and ends at BFFFFH. To help VGA to reach the memory beyond this range, the WD90C11 has two CPU address offset registers PROA and PROB which can be used to support more than 128 Kbytes of linear display memory address space.
The contents of PROA (bit 6:0) or PROB (bit 6:0) are always added to the CPU address A(18:12) before they are translated to display memory address. This can be thought of as segment register DS and ES in the 8088/80X86 architecture, PROA and PROB will then provide 4 Kbyte segmentation of the display memory. (Increment PROA or PROB by one of its equivalents to jump from a 4 Kbyte segment to another 4 Kbyte segment of the display memory.)
PROA and PROB are all set to zero value at power on reset. There are two ways to control whether PROA or PROB get added into CPU address.

- **Sequencer Extension Register 3C5 (index 11) bit 7 = 0.**

PROA is the primary offset register being added with the CPU address. PR1, bit 3 enables PROB which becomes the secondary offset register. If PR1, bit 3 = 1 and Graphics Controller index 6, bits 3:2 = 00b, A000:0 for 128K, then PROA will offset the CPU address from B000:0H to BFFF:FH while PROB offsets the CPU address from A000:0H to AFFF:FH. If PR1, bit 3 = 1 and Graphics Controller index 6, bits 3:2 = 01(A000:0H for 64K), then PROA will offset the CPU address from A800:0H to AFFF:FH while PROB offsets the CPU address from A000:0H - A7FF:FH.

- **Sequencer extension register 3C5 (index 11) bit 7 = 1.**

Both PROA and PROB are enabled. A CPU memory write will select PROB as the offset register. Otherwise, PROA is selected as the offset register.

7.11.2 PR1 - Memory Size, Read/Write Port = 3CF, Index = 0B

BIT	FUNCTION
7, 6	Memory Size Select
5, 4	Reserved
3	Enable Alternate Address Offset Register PR0B
2	16-Bit Video Memory
1	ROM Data Width
0	BIOS ROM Map Out

This register is 8 bits wide. Bits PR1 (1:0) are latched internally at power on reset from the corresponding memory data bus pins MD(10), MD(0) using either pull-up or pull-down external resistors. Pull-up resistors on MD(10), MD(0) cause PR1(1:0) bits to be latched low.

Bits 7, 6

Memory Size.

These two bits control memory size and memory organization. They both must be set to reflect the amount of memory installed. These bits in conjunction with PR0A, PR0B, PR16 (1) select the way memory is mapped into the CPU address space. IF PR16 (1) is set to 1, the memory mapping will be set identical to the IBM VGA regardless of PR1 (7), PR1 (6).

The WD90C11 supports 512 Kbytes (four 256K by 4 DRAM) display memory. This makes it possible to support some extended graphics modes such as 640 by 480 by 256 colors and 800 by 600 by 256 colors.

The setting of these two bits will be overwritten by PR16 (1). When PR16(1) is set to 1, memory mapping will be identical to the IBM VGA (equivalent to PR1 (7,6) = 00).

The following tables list the different settings on these two bits for different memory organizations.

GRAPHICS MODE RAM ADDRESSING:

PR1(7) **PR1(6)**

0 0 256K TOTAL;64K/PLANE; IBM VGA MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(16)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(4)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(3)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(2)	A(0)	CA(0)	A(16) or XRN(5)	CA(15) or CA(13)	A(14)	CA(12)

PR1(7) **PR1(6)**
0 1 256K TOTAL;64K/PLANE; WD90C11 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(16)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(4)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(3)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(2)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

PR1(7) **PR1(6)**
1 1 RESERVED

PR1(7) **PR1(6)**
1 0 512K TOTAL IN FOUR PLANES; 128K/PLANE; WD90C11 MEMORY ORGANIZATION (EACH PLANE HAS TWO BANKS OF 64 KBYTES)

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(16)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
MA (15)	A(13)	CA(13)	A(13)	CA(12)	A(13)	CA(11)
---	---	---	---	---	---	---
MA(4)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(3)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(2)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)
MA0	A(16)	CA(16)	A(17)	CA(16)	A(18)	CA(16)

NOTES:
1. A(19:0) are WD90C11 internally modified system Addresses.
2. CA(17:0) are CRT Controller Character Address Counter Bits.
3. XRN(5) is Miscellaneous Output Register 3C2H, inverted bit 5. This bit selects the displayed page in chained modes. XRN(5) is selected as MA(2) if Graphics Register 6 bit 3 or bit 2 = 1.
4. CA(13) is selected as MA(2) if CRTC Mode Register 17 bit 5 = 0.
5. For two 256K x 4 DRAMs, MA(1) and MA(0) are used as memory plane select for 256 Kbytes. For four 256K by 4 DRAMs, MA(1) is the plane select, MA(0) selects one of two 64 Kbytes within a 128 Kbyte plane.

Bits 5, 4
Reserved

Bit 3
Enable Alternate Address Offset Register PROB

Bit 2
Enable 16 bit bus for Video Memory
When set to 1, $\overline{\text{MEMCS16}}$ will be active low for all of the video memory cycles.

Bit 1
When set to 1 and bit 0=0, the BIOS ROM has a 16 bit data path from C000:0 - DFFF:FH ($\overline{\text{ROM16}}$ will respond to ROM access). Otherwise, the BIOS ROM has an 8 bit data path.

A pull down resistor on MD(10) will set this bit to 1 after power-on reset. This bit can also be set to 1 by an I/O write to PR1 register if the CNF(1) = 1 (2 ROMs).

Bit 0
If set to 1 the BIOS ROM is mapped out. Pull-up resistor latches 0 after power up. A pull-up on MD(0) sets this bit to 0 at power on reset.

7.11.3 PR2-Video Select Register, Read/Write Port = 3CF, Index = 0C

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4, 3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7
Enable AT&T/M24 Register & mode

Bit 6
0: VGA or EGA mode
1: Non-VGA (6845) mode

Bit 5
Character Map Select. The following functions are overridden by setting PR15(2). This bit in conjunction with PR2(2) and bit 3 of the attribute code, enables character maps from planes 2 or 3 to be selected per the table below:

PR2(5)	PR2(2)	ATT(4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE:
Setting PR15(2) = 1 i.e. selecting page mode addressing overrides plane selected table shown above.

Bit(4:3)

Character clock period control

0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132 character text mode only)
1	0	6 dots (for text modes only)
1	1	6 dots (for text modes only)

NOTE:
The character clock period control functions have no effect in graphics modes.

Bit 2

Underline and character map select. Setting this bit to 1 enables underline for all odd values of attribute codes, e.g. Programming 1 gives blue underline. It overrides the background color function of the attribute code bit 3, which is forced to 0. Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1

This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) is set to 1. When CNF(3) is set to 0, it locks the internal video clock select multiplexer.

Bit 0

Forces horizontal sync timing clock of the CRTC to VCLK.
Uses VCLK when sequencer register 1 bit 3 is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

7.11.4 PR3 - CRT Lock Control Register Read/Write Port=3CF, Index = 0D

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

7.11.5 WD90C11 CRT Controller Register Locking

Register locking is controlled by 4 bits. They are PR3 (5,1,0) and 3?5.11(7) (i.e. IBM Vertical Retrace End Register bit 7 controlled by index register 11). 11 When bit 7 is 1, CRT controller registers (R0-7) are write protected per VGA definition. For more information on the five groups, and their locking schemes, refer to the sections below.

- **Group 0**

These registers are locked if PR3(5)=1 OR 3?5.11(7)=1
CRT controller register 00 --Horizontal Total Characters per scan
CRT controller register 01 --Horizontal Display Enable End
CRT controller register 02 --Start Horizontal Blanking
CRT controller register 03 --End Horizontal Blanking
CRT controller register 04 --Start Horizontal Retrace
CRT controller register 05 --End Horizontal Retrace

- **Group 1**

These registers are locked if PR3(1)=0 AND 3?5.11(7)=1
CRT controller register 07(Bit6) - Vert. Display Enable End bit 9
CRT controller register 07(Bit1) - Vert. Display Enable End bit 8

- **Group 2**

These registers are locked if PR3(0)=1 OR 3?5.11(7)=1
CRT controller register 06 --- Vertical Total
CRT controller register 07(Bit7) ---Vertical Retrace Start bit 9
CRT controller register 07(Bit5) ---Vertical Total bit 9
CRT controller register 07(Bit3) ---Start Vertical Blank bit 8
CRT controller register 07(Bit2) ---Vertical Retrace Start bit 8
CRT controller register 07(Bit0) ---Vertical Total bit 8

- **Group 3**

These registers are locked if PR3(0)=1
CRT controller register 09(Bit5) ---Start Vertical Blank bit 9
CRT controller register 10 ---Vertical Retrace Start
CRT controller register 11 [Bits(3:0)] ---Vertical Retrace End
CRT controller register 15 ---Start Vertical Blanking
CRT controller register 16 ---End Vertical Blanking

- **Group 4**

This register is locked if PR3(5)=1
CRTC mode control register 17(Bit2) ---Selects divide by two vertical timing

Bit7

Lock VSYNC polarity, as programmed in 3C2 bit 7

Bit 6

Lock HSYNC polarity, as programmed in 3C2 bit 6

Bit 5

Lock horizontal timing.
Locks CRTC registers of Group 0 and 4.
Prevents attempt by applications software to unlock Group 0 registers by setting 3?5.11 bit 7=0

Bit 4

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 9 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (17).

Bit 3

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (16).

Bit 2

Cursor start, stop, preset row scan, and maximum scan line address registers values multiplied by two.

Bit 1

1 = Prevents attempt by applications software to lock registers of Group 1 by its setting 3?5.11 bit 7=1.

Bit 0

Lock vertical timing. 1 = Locks CRTC registers of Groups 2 and 3. Overrides attempt by applications software to unlock Group 2 registers by its setting 3?5.11 bit 7=0.

7.11.6 PR4- Video Control Register Read/Write Port=3CF, Index = 0E

The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAM-DAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLNK}}$ / Display Enable
6	PCLK=VCLK
5	Tri-state Video Outputs
4	Tri-state Memory Control Outputs
3	Override CGA Enable Video bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Ext 256 color Shift Register control

Bit 7

This bit controls the output signal $\overline{\text{BLNK}}$. Normally in the VGA mode, $\overline{\text{BLNK}}$ is used by the external video DAC to generate blanking. If this bit = 1, the $\overline{\text{BLNK}}$ output supplies a display enable signal. A choice of two types of display enable timings can be selected, and is determined by PR15(1).

Bit 6

Select PCLK equal to VCLK.
0=PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1=PCLK is always the non-inverted VCLK input clock.

Bit 5

Tri-state the outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLNK}}$.

Bit 4

Tri-state the memory control outputs. The memory address bus MA(8:0), and all DRAM control signals are tri-stated when this bit is set to 1.

Bit 3

Overrides the CGA "enable video" bit 3 of mode register 3D8, only in 80 x 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2

Lock Internal palette and overscan registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode. It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3CO/3C1 change to write-only mode if the EGA compatibility bit is set. In VGA mode (PR(4) bit 1 is zero) 3C0 register is read/write while 3C1 register is read only, per the Attribute Controller registers definitions.

Bit 0

Extended Shift Register Control.
This register should only be used with 4 DRAMs to configure the video shift register for extended 256 color modes.

7.11.7 PR5 - General Purpose Status Bits Read/Write Port=3CF, Index = 0F

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PRO-PR4 Unlock
1	PRO-PR4 Unlock
0	PRO-PR4 Unlock

Bits (2:0) are READ/WRITE bits and cleared to 0 by reset. They provide lock or unlock capability for PR registers PR0 through PR4 like the PVGA1A. The PR0 - PR4 registers are unlocked when "X5Hex" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register bits 4 through 8. Setting PR(4) bit 1 to 1, read protects registers PR0 - PR5.

Bit 7	CNF(7) [READ ONLY]
Bit 6	CNF(6) [READ ONLY]
Bit 5	CNF(5) [READ ONLY]
Bit 4	CNF(4) [READ ONLY]
Bit 3	CNF(8) [READ ONLY]

Bits (2:0)

READ/WRITE bits and cleared to 0 by reset. They control writing to PR registers PR0-PR4 as follows:

2 1 0	PR0-PR4
0 X X	Write protected
X 1 X	Write protected
X X 0	Write protected

7.11.8 PR10 Unlock PR11-PR17 Read/Write Port = 3?5, Index = 29

This register is READ/WRITE and cleared to 0 by reset. PR10 can be loaded if it contains XXXXX101, and can only be read if it has 1XXX0XXX. Bits (7,3), Bits(6:4), and Bits (2:0) control access to PR registers PR10-PR17. Bits 7 and 3 enable register read operation for PR10 - PR17. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 - PR17.

BIT	FUNCTION
7	PR10-PR17 - Read Enable Bit 1
6 - 4	PR10(6:4) - Scratch Pad
3	PR10-PR17 - Read Enable Bit 0
2 - 0	PR11-PR17 - Write Enable

BIT7	BIT3	PR10-PR17
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

BIT2	BIT1	BIT0	PR11-PR17
0	X	X	Write protected
X	1	X	Write protected
X	X	0	Write protected
1	0	1	Write Enabled

BIT6	BIT5	BIT4	PR10(6:4)
0	X	X	Scratch pad
X	1	X	Scratch pad
X	X	0	Scratch pad
1	0	1	Reserved for manufacturing test.

7.11.9 PR11 EGA Switches Read/Write Port = 3?5, Index = 2a

The EGA switch configuration details are stored in the PR11 register bits.

BIT	FUNCTION
7	EGASW4
6	EGASW3
5	EGASW2
4	EGASW1
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4)

EGA CONFIGURATION SWITCHES SW4-SW1. These bits are READ/WRITE and latched internally at power-on-reset from corresponding memory data bus pins MD(15:12), provided with either pull-up or pull-down external resistors. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. These bits can be read as bit 4 of port 3C2 if the EGA COMPATIBILITY BIT [PR4(1)] has been set to 1. Selection of the bit to be read is determined by bits 3 & 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE 3C2 bit 3	3C2 bit 2	READ 3C2 bit 4
0	0	PR11(7) [=EGA SW4]
0	1	PR11(6) [=EGA SW3]
1	0	PR11(5) [=EGA SW2]
1	1	PR11(4) [=EGA SW1]

PR11 Bits 3 through 0 are READ/WRITE and cleared to 0 at power on reset.

Bit 3

Select EGA Emulation on a PS/2 (VGA-compatible, analog) display.

Bit 2

Lock Clock Select. This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

Bit 1

Lock Graphics Controller/Sequencer screen control. Setting PR11(1) to 1 prevents modification of the following bits in the Graphics controller as well as the Sequencer:

Graphics controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by these graphics controller and sequencer bits are locked by setting PR11 bit 1 to 1, they appear unlocked to the system processor during read operation.

Bit 0

Lock 8/9 dots. Setting this bit to 1 prevents modification of clocking mode sequencer register 3C5.01 bit 0. Although 8 or 9 character timing is locked by setting PR11 bit 0 to 1, the 3C5.01 bit 0 appears unlocked to the system processor during reads.

7.11.10 PR12 Scratch Pad Read/Write Port = 3?5, Index = 2b

BIT	FUNCTION
7 - 0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power up.

7.11.11 PR13 Interlace H/2 Start Read/Write Port = 3?5, Index = 2C

BIT	FUNCTION
7 - 0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1. All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00):

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE:
In the above expression, HRD = Horizontal Retrace Delay, determined by bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

7.11.12 PR14 Interlace H/2 End Read/Write Port = 3?5, Index = 2d

Bits 4 through 0 are unaffected by hardware reset and undefined at power up. Bits 7 through 5 are cleared to 0 by reset.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4 - 0	Interlaced H/2 Start

Bit 7

Enable IRQ. This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to 0. This bit should not be set to 1 in MICRO CHANNEL operation.

Bit 6

Vertical double scan. This bit should be set to 1 when emulating EGA on PS/2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed line counter and row scan counter to be clocked by divide-by-two horizontal timing if vertical sync polarity (3C2 Bit 7=0) is programmed to be positive. Therefore, the relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is:

N=2(n+1)

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5

Interlaced mode.
Setting this bit to 1 selects interlaced mode. The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000.
Line compare and double scan are not supported.

Bits (4:0)

Interlaced H/2 end bits (4:0). Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

7.11.13 PR15 Miscellaneous Control 1 Read/Write Port = 3?5, Index = 2e

BIT	FUNCTION
7	Read 46E8 Enable
6	Reserved
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable reading port 46E8H. This bit is functional only if AT BUS architecture [CNF(2)=1] is selected. Setting this bit to 1 enables I/O port 46E8H to be read, regardless of the state of its own bits 3 and 4 and of port 102 bit 0 (sleep bit). Only bits (4:0) of port 46E8H are readable; bits (7:5) are 0.

Bit 6

Reserved.

Bit 5

Latched VCLK1 and VCLK2. This bit is used only if CNF(3) = 1 which configures the VCLK1 and VCLK2 pins as outputs. Setting This bit to 1 causes outputs VCLK1 and VCLK2 to equal bits 2 and 3 of I/O write register (Miscellaneous output register) at 3C2H respectively.

Bit 4

Select MCLK as video clock. Setting this bit to causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.

Bit 3

Interlaced Compatibility. This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to 1 if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to 1causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of leading edge, as generated for VGA timing.
Setting this bit to 1 also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing. Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory by 30-40%. Set this bit to 1 of 132 character mode timing is selected (see description of PR2). Setting this bit to any alpha mode overrides the character map select functions of PR2(2) and PR2(5). When this bit is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight, 8K memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by bits (2:0) of this register while the map selection is determined by the bits (4:3). A pair of adjacent 8K character maps in planes 2 and 3, (adjacent in the sense that they have the same addressing) may be selected by bit 3 of the attribute code.
The Character attribute bit 3, in conjunction with bits 3 and 4 of the Character Map Select register (3C5.03), determine a character map from either Plane 2 or Plane 3 as shown by the table below.

3C5.03 BIT4	3C5.03 BIT 3	ATT BIT3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

Note:
The above Character Map Select functions override the functions override the functions of PR2(5) and PR2(2).
This bit must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select. This bit is used to select between two types of Display Enable timings available at output pin BLNKN if PR4(7)=1. If PR4(7)=0, this bit has no effect.

0=BLNKN supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = BLNKN supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable border. Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

7.11.14 PR16 Miscellaneous Control 2 Read/Write Port = 3?5, Index = 2f

BIT	FUNCTION
7	External reg. 46E8H lock
6	CRTC Address count Width bit 1
5	CRTC Address Count Width bit 0
4	CRTC Address Counter Offset bit 1
3	CRTC Address Counter Offset bit 0
2	Enable Odd/Even Page bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit (7)

Lock External 46E8H register.

Setting this bit to 1 causes $\overline{\text{EBROM}}$ output to be forced high (Inactive) during I/O writes to port 46E8H. This bit has no effect on loading the internal port 46E8H.

Bit (6:5)

CRTC Address Counter Width.

Power on reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512KB or 1024KB of video memory in which CRT controller is limited to only 64K or 128K locations. Bit PR16(6) should be set 1 to ensure VGA and EGA compatible operation of the address counter, limited to 64 K locations. The following table shows details:

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256KB
0	1	128K
1	X	64K

Bit (4:3)

CRTC Address Counter Offset
Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively, and the 2-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2

Enable Page Bit for Odd/Even
This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory, and setting 3C5.04(3) to 0 to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size bits PR1(7:6).

Bit 1

VGA Memory Mapping
Setting this bit to 1, selects 256KB IBM VGA Mapping, regardless of the Memory Size bits PR1(7:6).

Bit 0

Lock RAMDAC write strobe (3C6H - 3C9H) Programming this bit to 1 causes output WPLTN to be forced to 1 disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C11 is also protected from the modification but may still be read at the port 3C7h. For normal operation, program this bit to 0.

7.11.15 PR17 Miscellaneous Control 3 Read/Write Port = 3?5, Index = 30

BIT	FUNCTION
7 - 4	Reserved
3	Map out 4K of BIOS ROM
2	Enable 64K BIOS ROM
1	Hercules Compatibility
0	Map out 2K of BIOS ROM

Bit (7:4)

Reserved.

Bit (3)

Map out 4K of BIOS ROM.
Setting this bit to 1 disables access of the BIOS ROM in the system address range C600:0H - C6FF:FH. Power on reset sets this bit to 0.

Bit (2)

Enable 64K BIOS ROM.
Setting this bit to 1 enables access of the BIOS ROM in the system address range C000:0H - CFFF:FH. Power on reset sets this bit to 0.

Bit (1)

Setting this bit to a 1 locks Hercules compatibility register (I/O port 3BF). Power on reset sets this bit to 0.

Bit (0)

Map out 2K of BIOS ROM.
Setting this bit to 1 disables access of the BIOS ROM in the system address range C600:0H - C67F:FH.
Power on reset sets this bit to 0.

7.11.16 PR20 3C5 Index 6: Unlock Sequencer Extended Registers (Reset State = Locked)

A value of X1X01XXXX (48H) must be loaded to allow R/W of the Sequencer Extended Registers. When the extended registers are locked, then the Sequencer index will be readable as three bits only. When unlocked, the Sequencer index reads as a full eight bits.

7.11.17 PR21 3C5 Index 7: Display Configuration Status and Scratch Pad Bits

This register provides a convenient location for determining the current VGA configuration state. This information is needed for many of the BIOS calls.

BIT	FUNCTION
7 - 4	Scratch Pad Bits
3	Status of 3C2 bit 0
2	Status of PR2 bit 6
1	Status of PR4 bit 1
0	Status of PR5 bit 3

Bits 7:4

Read/write scratch pad for any BIOS status data that may need to be saved. Reset state is 1111.

Bit 3

Reflects the setting of the I/O address select bit in the Miscellaneous Output Register.
A 1 means CGA (3Dx) addresses have been selected by this read-only bit, while a 0 means MDA (3Bx) addresses have been selected.

Bit 2

Reflects the setting of the VGA/6845 select bit in PR2 (3CF index C).
A 1 means 6845 compatibility has been selected by this read-only bit, while a 0 means VGA or EGA compatibility has been selected.

Bit 1

Reflects the setting of the VGA/EGA select bit in PR4 (3CF index E).
A 1 means EGA compatibility has been selected by this read-only bit, while a 0 means VGA was selected.

Bit 0

Reflects the setting of the Analog/TTL status bit in PR5 (3CF index F).
The video BIOS may define this as a 0 meaning an an analog monitor was selected by this read-only bit, while a 1 means a TTL-type monitor was selected.

7.11.18 PR30 3C5 Index 10 Memory Interface and FIFO Control Register

This register controls display memory data width and its bandwidth. All of the bits are reset to zero at power on reset.

BIT	FUNCTION
7, 6	Reserved
5	8- or 16-bit Memory data path
4	Disable 16-bit CPU interface
3	Enable write buffer extension
2	4 or 8 level FIFO
1, 0	Display memory bandwidth

Bits (7,6)

Reserved

Bit 5

When set to 1, the display memory data path becomes 16-bits wide. Otherwise, the data path is 8-bits wide. The WD90C11 can support 8/16-bits memory data path with four 256 Kbyte by 4 DRAMs installed.

Bit 4

When set to 1, the 16-bit CPU interface is unchained mode is disabled. This is for debug only and should be set to 0 under normal conditions.

Bit 3

When set to 1 enables the write buffer extension. This will make the write buffer effectively two deep. Should be set to 1 under normal conditions.

Bit 2

When set to 1, will set the internal FIFO to 4 levels deep. Otherwise the FIFO is 8 levels deep. In general, when 16-bits display memory is enabled (bit 1 of this register is set to 1), then the 4 level deep FIFO is recommended. In "Super VGA" mode (800 by 600 by 256 color) an 8 level deep FIFO will be required.

Bit 1, 0

These two bits can be used to adjust the display memory bandwidth. In general it is recommended that these two bits be set to 01 to accommodate most applications. These bits have no effect in any text mode. They are locked into 00 internally when a text mode is set.

00	FIFO requests for memory cycle when FIFO is:	one level empty
01	FIFO requests for memory cycle when FIFO is:	two levels empty
10	FIFO requests for memory cycle when FIFO is:	three levels empty
11	FIFO requests for memory cycle when FIFO is:	four levels empty

7.11.19 PR31 3C5 Index 11: System Interface Control (Reset State = 00H)

This register provides the control bits for the system interface. This register should be set during the Post initialization routines of the VGA BIOS. The reset state is 100% IBM VGA compatible. Bit 7 will be used during some of the enhanced display modes.

BIT	FUNCTION
7	Read/Write Offset Enable
6	Turbo Mode for Blanked Lines
5	Turbo Mode for Text
4	CPU Read RDY release Control 1
3	CPU Read RDY release Control 0
2	Enable Write Buffer
1	Enable 16-bit I/O Operation on Attribute Controller
0	Enable 16-bit I/O Operation on CRTC, Sequencer and Graphics Controller

Bit 7

When set to 1, the offset register PR0-A will be added to the CPU address for read cycles, while PR0-B will be added for write cycles. When cleared to 0, the offset registers operate the same as in the PVGA1B. Refer to PR0A and PR0B definitions.

Bit 6

When set to 1, system performace is improved by 10% by removing extra memory cycles on blank lines.

Bit 5

When set to 1, text mode performance will be improved.

Bit 4:3

These two bits set the CPU's RDY timing to be optimized for different system timing. For slower systems, the RDY line may be released earlier because it will take longer for the read cycle to be completed.

00 = Power on reset condition. RDY is inserted at the end of a CPU memory cycle

01, 10 = RDY is inserted 1MCK before the end of a CPU memory cycle.

11 = RDY is inserted 1MCK after the end of a CPU read memory cycle. RDY is inserted at the end of a memory write cycle.

For 10 MHz or slower systems, the 01 setting is recommended. For 12 MHz or faster systems, the 11 setting is recommended.

Bit 2

When set to 1, a single-level , 16-bit write buffer is enabled. This willl greatly reduce the number of wait states for CPU writes to display memory.

Bit 1

If this bit and bit 0 are both set to 1, then the Attribute Controller (3C0/3C1) is configured for 16-bit access. The index is at 3C0, while the data is at 3C1, and the address toggle is disabled for 16-bit reads or writes. The address toggle functions in the standard way for 8-bit cycles. $\overline{\text{IOCS16}}$ is asserted for all cycles to 3C0 or 3C1.

Bit 0

When set to 1, this bit enables 16-bit access to the CRTC (3?4/3?5), Sequencer (3C4/3C5), and Graphics Controller (3CE/3CF). The output $\overline{\text{IOCS16}}$ will be active for any I/O read or write to these addresses. When set at 0, the VGA I/O is all 8-bit.

7.11.20 PR32 3C5 Index 12: Miscellaneous Control 4 (Reset State = 00H)

This register provides control for several different features. Some of these features help to support Genlock of the PVGA1M to another display controller for overlay.

BIT	FUNCTION
7	Enable External Sync Mode
6	Disable Cursor Blink
5	USR1 Function Select
4	USR1 Control
3	USR0 Function Select
2	USR0 Control
1	Allow readback in backward compatible modes
0	Force standard CPU addressing in 132-column mode

Bit 7

When set to 1, $\overline{\text{EXVID}}$ is configured to input external Horizontal Sync, and $\overline{\text{EXPCLK}}$ inputs external Vertical Sync. The external HSYNC signal also synchronizes the character clock timing. In this configuration, $\overline{\text{EXVID}}$ and $\overline{\text{EXPCLK}}$ do not control the VID7:0 and PCLK output buffers. A 0 setting places this bit into its normal operation mode.

Bit 6

When set to 1, the text cursor blink will be disabled, and the cursor will remain on. This option can be used if cursor blink is not desired.

Bit 5

A 1 setting causes the USR1 output to indicate when the WD90C11 is reading font data in text mode (FONTCYC). A 0 causes the USR1 output to reflect the state of bit 4, which can be used to control new features that the system board designer may wish to add.

Bit 4

Controls the USR1 output when selected by bit 5.

Bit 3

A 1 setting causes the USR0 output to indicate that the WD90C11 is reading both the character and the attribute data from the DRAMs in text mode (TEXTCYC). USR0 will be high during the RAS cycles for character/attribute read. The DRAM data may be sampled when USR0 is high. A 0 setting causes the USR0 output to reflect the state of bit 2, which can be used to control new features that the system board designer may wish to add.

Bit 2

Controls the USR0 output when selected by bit 3.

Bit 1

When set to 1, this bit allows reading the registers that are not readable in backward compatibility modes. This option may be used either as a test feature or by the BIOS during mode changes.

Bit 0

When set to 1, the special CPU address mapping for page mode font access in 132-column text is set for standard mapping without disturbing the display. This will be used only for special virtual VGA applications.

7.12 INTERNAL I/O PORTS

7.12.1 AT Mode Setup, Enable Write Only Port 46E8H (Also at Port 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7 - 5	Unused
4	Setup
3	Enable I/O & Memory
2 - 0	External BIOS ROM Page Select

Bit(7:5)

Unused

Bit 4

Setup
Puts WD90C11 into setup mode where only I/O port 102H is accessible.

Bit 3

Enable I/O and Memory Accesses

Bit(2:0)

Unused Internally
Used for BIOS ROM Page select. On I/O accesses to 46E8H, EBROMN becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits to define 4K pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0. The WD90C11 also provides an alternative port 3C3H instead of port 46E8H. If a pull down resistor is connected to MD(9) during power on reset (CNF9 = 0), then port 3C3H will be decoded instead of port 46E8H to support the same functions described above. Otherwise, port 46E8H is selected and decoded.

7.12.2 Setup Mode Video Enable (AT and Micro Channel Modes) Read/Write Port = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7 - 1	Unused
0	Wakeup VGA

Bit(7:1)

Unused

Bit 0

Wakeup VGA for I/O and Memory Accesses. Only lower 3 address bits are decoded for this port and WD90C11 must be in SETUP mode. VGA Enable Sleep bit or Programmable Option Select (POS) register 102H bit 0 is used to awaken the WD90C11 after power on in the MCA and AT mode. To enter the set up mode in AT bus applications, bit 4 of the partially decoded internal I/O port 46E8H is set to 1 before accessing the I/O port 102H. In MCA mode, when the VGASETUP (EION) signal pin is active low, the WD90C11 is in setup mode and port 102H can be accessed.

7.13 VIDEO RAMDAC PORTS

The Video RAMDAC is implemented externally to the WD90C11. However, the $\overline{WPLT}$ and $\overline{RPLT}$ signals required by the RAMDAC are provided by the WD90C11. Setting PR(16) bit 0 to a 1 forces $\overline{WPLT}$ to a high level disabling I/O writes to the RAMDAC. Normally, the $\overline{WPLT}$ and $\overline{RPLT}$ signals to the RAMDAC are generated when the following I/O ports are written to or read from.

DAC ADDRESS	DAC OPERATION	DETAILS
3C8H	PEL address port (write)	Read/write port
3C7H	PEL address port (read)	Write only port
*3C7H	*DAC state (read only)	*If bits 0/1 =1, DAC in read operation. When bits 0/1=0,DAC in write operation. Bits 2-7 are reserved.
3C6H	PEL mask (read/write)	Not to be written by application code or color look up table will be changed.
3C9H	PEL data register (read/write)	Three successive read/write bytes.

* This port is internal to the WD90C11.

7.14 CONFIGURATION BITS

Memory Data lines 15:0 are used to input configuration data at power-on reset (RST) by pullup or pulldown resistors. This configuration data then sets the bits in internal registers. Some of these bits can then be changed by software, while some are in non-writable registers. The non-writable bits set features such as bus type which are not changed after power-on.

BIT	FUNCTION
15 - 12	EGA Switches
11	A23 - A20 Connection Select
10	16-bit BIOS
9	46E8/3C3 Select
8	Display Status
7 - 4	General Purpose Status
3	Video Clock Source Control
2	Bus Architecture Select
1	ROM Configuration
0	Map out BIOS

7.14.1 WD90C11 Configuration Register Bits CNF(15:0)

CNF(15:12)

EGA CONFIGURATION SWITCHES SW4-SW1. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. PULLING DOWN MD(15:12) causes these bits to be latched LOW. PR11(7:4) are writable bits. These bits can be read as bit 4 of port 3C2H (as on a standard EGA) if the EGA COMPATIBILITY BIT [PR4(1)] has been set to 1. Selection of which bit is read is determined by bits 3 & 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE		READ
3c2 bit 3	3C2 bit 2	3C2 bit 4
0	0	PR11(7) [= EGA SW4]
0	1	PR11(6) [= EGA SW3]
1	0	PR11(5) [= EGA SW2]
1	1	PR11(4) [= EGA SW1]

CNF (11) (Refer to Figure 12)

A 4.7K pull down resistor on the pin MD 8 will set CNF(11) = 0. The pins A(22:20) should then be connected to the AT bus signals LA(19:17), unlatched CPU address. The pin A23 should be connected to the NOR of AT bus signals LA(23:20). The pins A(19:17) should be connected to AT bus SA(19:17), latched CPU address. This will allow the WD90C11 to directly drive MEMCS16 in AT bus which requires decoding of the early unlatched address LA(23:17). An external NOR is required to decode LA(23:20).
If there is no pull down resistor on MD8, the CNF(11) will be set to 1 by the internal pull up. Pins A(23:17) should be connected to AT bus signals LA(23:17). In most 80286 systems, the early address LA(23:17) is not latched during a bus operation. CNF(11) = 0 is required to ensure proper decoding of $\overline{\text{MEMCS16}}$ without many external components. In most 80386 systems, the early address LA(23:17) is latched during a bus operation. CNF(11) = 1 is recommended for design simplification. In Micro Channel applications, CNF(11) should be set to 1.

CNF (10)

A 4.7K pull down on pin MD10 will set CNF(10) = PR1(1). Upon power-up, the pin $\overline{\text{ROM16}}$ is enabled for 16-bit BIOS ROM decoding. Otherwise the internal pull up will set CNF(10) = PR1=0. To enable the 16-bit BIOS, PR1 must be set to 1 by writing to port 3CF (index 0B) and the CNF (1) must be 1. This bit is read/write at PR1(1).

CNF (9)

A 4.7K pull down on pin MD9 will set CNF(9) = 0. Then port 03C3 will be selected as the VGA setup and enable register instead of port 46E8 in the AT interface. Otherwise, the internal pull up will set CNF(9) = 1. Port 46E8 will be selected as VGA setup and enable register. This bit has no effect in Micro Channel applications.

CNF (8)

ANALOG/TTL DISPLAY STATUS BIT.
Bit CNF(8) is latched internally at power-on-reset from memory data bus pin MD(11), provided with either a pull-up or pull-down external resistor. Pulling up MD(11) causes CNF(8) to be latched Low. This bit controls no internal functions and is read only as bit 3 of PR5 (3CF.0F). Also, CNF(8) is unaffected by writing to PR5 (3CF.0F). Suggested implementation is:

0 = Analog (VGA - compatible) display is attached
1 = TTL (EGA-compatible) display is attached.

CNF (7:4)

GENERAL PURPOSE STATUS BITS.
Bits CNF (7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD (7:4), provided with either pull-up or pull-down external resistors. These are read only bits at PR5 (3CF.0F) positions (7:4). These bits are unaffected by writing to PR5(3CF.0F). Pulling up MD (7:4) causes CNF (7:4) to be latched high.

CNF (3)

VIDEO CLOCK SOURCE CONTROL.
This bit cannot be written or read as I/O port pulling up MD (3) causes CNF(3) to be latched high. It configures WD90C11 pins VCLK1 and VCLK2 as inputs or outputs.

0=For inputs.
1=For outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of dot clock is by an internal multiplexer. When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip, during I/O writes to port 3C2H. This load pulse may be inhibited by setting PR11(2)=1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. Also, VCLK1 and VCLK2 outputs equal to bits 2 and 3 of the Miscellaneous output register at 3C2H respectively when PR15 bit 5 is set to 1.

CNF (2)

BUS ARCHITECTURE SELECT.
This bit cannot be written or read as I/O. Pulling down MD(2) causes CNF(2) to be latched low.

0: Micro Channel architecture

1: AT BUS architecture

Select CNF(2) will change PINOUT definition between AT BUS and Micro Channel bus (see PINOUT description).

PC-AT BUS	I/O	Micro Channel	I/O
MEMCS16	OUT	$\overline{\text{CDDS16}}$	OUT
$\overline{\text{ROM16}}$	OUT	$\overline{\text{CSFB}}$	OUT
$\overline{\text{EIO}}$	IN	3C3D0	IN
$\overline{\text{MRD}}$	IN	M/$\overline{\text{IO}}$	IN
$\overline{\text{MWR}}$	IN	$\overline{\text{S0}}$	IN
$\overline{\text{IOR}}$	IN	$\overline{\text{S1}}$	IN
$\overline{\text{IOW}}$	IN	CMD	IN
IRQ	OUT	$\overline{\text{IRQ}}$	OUT
$\overline{\text{IOCS16}}$	OUT	$\overline{\text{CDSETUP}}$	OUT

CNF (1)

ROM CONFIGURATION.
When set to 0, the WD90C11's data bus buffer controls are configured for 1 ROM (8 bits). An internal pullup on MD (1) sets this bit to 0 at power-on reset.
When set to 1, the WD90C11's data bus buffer controls are configured for 16-bits (as with two ROMs).
If CNF (1) = 0, then PR1(1) can not be set high. This bit can not be written or read.

CNF (0)

BIOS ROM MAPPING.
If set to 1, the BIOS ROM is mapped out. An internal pullup resistor on MD(0) sets this bit to 0 at power-on reset. An external 4.7 K ohm pulldown resistor may be used to set this bit to 1 on power-on (reset).
This bit is read/write at PR1(0).

APPENDIX

A.1 EGA MODE

For the register definitions that have not changed from the VGA modes, refer to the VGA description. Only the differences between the VGA and EGA registers are briefly described in this section. Also, refer to the prior section for VGA mode details. Not Used bits should be set to 0 unless otherwise noted.

A general procedure to enter EGA mode of operation is described. The actual software implementation details are not covered in this procedure. These steps are briefly defined to outline the EGA mode entry.

- Load Configuration register bit 8. Logic 0 for VGA compatible PS/2 display or Logic 1 for EGA compatible TTL monitor by appropriate pull-up or pull-down resistor on MD(11). (Pull-up resistor on MD11 causes CNF(8) to be latched with logic 0, for Analog PS/2 compatible display). This is status for the BIOS or application to signify monitor type attached.
- Unlock all the PR registers.
- Program PR2(6) to 0 for EGA mode.
- Set PR4 bit 1 to logic 1 for EGA compatibility.
- Load PR11(7:4) with EGA Configuration switches by using pull-up or pull-down resistors on pins MD(15:12). (Pull-up resistor causes logic 1 to be latched after power on reset.)
- The EGA switch setting may then be read from PR11(7:4) at I/O port 3C2 bit 4.
- If EGA is to be emulated on the IBM PS/2 type analog display, follow the suggested steps listed below:
  Initialize all the registers.
  Lock CRT controller registers.
  Force Clock Control rate of the CRT controller.
  - Set EGA emulation mode by programming:
    PR11(3)=1; Set EGA emulation on PS/2 type display
    PR14(6)=1; Vertical double scan
    PR11(2)=1; Lock clock select
    PR11(0)=1; Lock 8/9 dot timing.
    PR14(7)=1; Enable IRQ (optional)
  - Lock the PR registers PRO-PR5 and PR10-PR17.
  - Read protect PR registers.
- When EGA is required on a TTL monitor, the suggested steps are:
  - Initialize all the registers.
  - Set EGA TTL mode by programming:
    PR11(3)=0;EGA TTL
    PR14(7)=1;Enable IRQ
    PR15(6)=1;Set Low Clock
    PR14(7)=1;Enable IRQ
  - Lock PR registers PRO-PR5 and PR10-PR17
  - Read protect PR registers.

For more details on the PR registers, refer to the PR registers section. The EGA register summary shown on the next page highlight all the EGA mode registers.

A1.1 EGA Registers Summary

REGISTERS	EGA	I/O PORT
General Registers:		
Miscellaneous Output Reg	WO	3C2
Input Status Reg 0	RO	3C2
Input Status Reg 1	RO	3?A
Feature Control Reg	WO	3?A
Sequencer Registers:		
Sequencer Index Reg	WO	3C4
Sequencer Data Reg	WO	3C5
CRT Controller Registers:		
Index Reg	WO	3?4
CRT Controller Data Reg Except the following:	WO	3?5
Start Address High (Index=0C)	RW	3?5
Start Address Low (Index=0D)	RW	3?5
Cursor Location High (Index=0E)	RW	3?5
Cursor Location Low (Index=0F)	RW	3?5
Light Pen High, (Index=10)	R	3?5
Light Pen Low, (Index=11)	R	3?5
Graphics Controller Registers:		
Index Reg	WO	3CE
Other Graphics Reg	WO	3CF
Attribute Controller Registers:		
Index Reg	WO	3CO*
Attribute Controller Data Reg	WO	3CO*

NOTES:
1. RO = Read Only, WO = Write Only, and RW = Read/Write.
2. All Register addresses are in hex.
3. "?" = "B" in Monochrome modes or "D" in Color modes.
4. "*" = Identical responses from I/O ports 3C0 and 3C1.

TABLE 8. EGA REGISTERS SUMMARY

A.2 GENERAL REGISTERS

Only the general registers and the bit definitions that differ between the VGA and EGA are addressed. Their EGA mode bit definitions are provided.

A.2.1 Miscellaneous Output Register (Write Port 3C2)

Bits (7:5)

EGA: Same as Miscellaneous Output Register Bits (7:5) definition in the VGA section.

Bit 4

Not used.

Bits (3:2)

EGA:

BIT 3	BIT 2	DESCRIPTION
0	0	14.318 Mhz clock (VCLK0) is selected.
0	1	16.257 Mhz clock (VCLK1) is selected if Configuration Register Bit 3 is 0.
1	0	External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is 0.
1	1	Not Used. VCLK2 selected if Configuration Register Bit 3 is 0

Bit (0)

EGA: Identical to Miscellaneous Output Register Bit 0 definition in the VGA section.

A.2.2 Input Status Register 0 (Read Port 3C2)

Bit 7

EGA: Same as input Status Register 0, Bit 7 definition in the VGA section.

Bits (6:5)

EGA: Not used

Bit 4

EGA: The four configuration switches' information stored in PR11 can be read at this bit if PR4(1) has been set to 1.

Bits (3:0)

EGA: Not used = 1

A.2.3 Input Status Register 1 (READ PORT 3?A)

Bit (7)

EGA: Not used

Bit 6

EGA: Not used = 1

Bits (5:3)

EGA: Identical to Input Status Register 1 Bits (5:3) definition in the VGA section.

Bit 2

EGA: Not used = 1

Bit 1

EGA: Unused

Bit (0)

EGA:
Same as Input Status Register 1 Bit 0 definition in the VGA Section.

A.2.4 Feature Control Register (Write Port 3?A)

Bits (7:0)
EGA: Not used

A.3 SEQUENCER REGISTERS (PORT 3C5)

A.3.1 Clocking Mode register (Index = 01)

Bits (7:4)
EGA: Not Used

Bits (3,2)
EGA: Same as Clocking Mode Register Bits (3,2) definition in the VGA section.

Bit 1
EGA: Set to zero

Bit (0)
EGA: Identical to Clocking Mode Register Bit 0 definition in the VGA section.

A.3.2 Character Map Select Register (Index 03)

Bits (7:4)
EGA: Not Used

Bits (3:2)
EGA: Character Map Select A

BIT 3	BIT 2	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

Bits (1:0)
EGA: Character Map Select B

BIT 1	BIT 0	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

NOTE:
1. Character Map selection from Plane 2 is determined by bit 3 of the attribute code.

A.3.3 Memory Mode Register (Index = 04)

Bits (7:3)
EGA: Not Used

Bits (2:1)
EGA: Identical to Memory Mode Register Bits (2,1) definition in the VGA section.

Bit 0
EGA: Alpha mode bit.
A logic 1 shows that Alpha mode is active and character map selection is enabled. A logic 0 disables Alpha modes and enables non-Alpha modes.

A.4 CRT CONTROLLER REGISTERS (PORT 3?5)

The EGA registers that are different are listed. For similar registers and identical bits within registers refer to the VGA section. Also, "?" implies that a register is mapped into either 3B5 or 3D5, for Monochrome or Color display modes, respectively.

A.4.1 Index Register (Port = 3?4)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Five bits point to the CRT Registers Address index where the data is to be written.

A.4.2 Horizontal Total Register (Index = 00)

Bits (7:0)

EGA:
Eight bits of value for the "Total Character Count Less 2" are loaded into this register. They define number of characters to be displayed per horizontal line.

A.4.3 End Horizontal Blanking Register (Index = 03)

Bits (7)

EGA: Not Used.

Bits (6:5)

EGA: They define display enable skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

EGA: Five bits of character count are loaded to determine when the horizontal blanking signal becomes inactive.

A.4.4 End Horizontal Retrace Register (Index = 05)

Bit 7

EGA: It defines the start of the odd or even CRT counter memory address following the horizontal retrace time. Logic "1" = Odd Address and logic "0" = Even Address.

Bits (6:0)

EGA: Same as End Horizontal Retrace Registers Bits (6:0) definition in VGA section.

A.4.5 Vertical Total Register (Index = 06)

Bits (7:0)

EGA: Lower eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

A.4.6 CRT Controller Overflow Register (Index = 07)

Bits (7:5)

EGA: Not used.

Bits (4:0)

Identical to CRT Controller Overflow Register Bits (4:0) definitions in the VGA section.

A.4.7 Preset Row Scan Register (Index = 08)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Preset Row Scan Register Bits (4:0) definition in the VGA section.

A.4.8 Maximum Scan Line Register (Index = 09)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as maximum Scan Line Register Bits (4:0) definition in the VGA section.

A.4.9 Cursor Start Register (Index = 0A)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Cursor Start Register Bits (4:0) definition in the VGA section.

A.4.10 Cursor End Register (Index = 0B)

Bit(7)

EGA: Not used.

Bits (6:5)

EGA: They define cursor signal skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	0
1	0	1
1	1	2

Bits (4:0)

EGA: These bits define Cursor End value of row scan address counter. The programmed value is equal to "N+1" where "N" is the last row of the Cursor to be displayed.

A.4.11 Vertical Retrace Start Register (Index = 10) - Write

(Light Pen High register, Index = 10 - Read)

Bits (7:0)

EGA: Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

A.4.12 Vertical Retrace End Register (Index = 11) - Write

(Light Pen Low register, Index = 11 - Read)

Bits (7:6)

EGA: Not used

Bit 5

EGA: It enables the IRQ output buffer control if Logic 0 is programmed. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal. If programmed as logic 1, the IRQ buffer is switched to a high impedance state.

Bit 4

EGA: When programmed to logic 0, the IRQ latch is reset and cleared to 0 if bit 5 = 0. If it is logic 1, the IRQ latch gets set at the end of the vertical display.

Bits (3:0)

EGA: Identical to Vertical Retrace End Register Bits (3:0) definition in the VGA section.

A.4.13 Underline Location Register (Index = 14)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Horizontal scan row where the underline will be displayed. Value programmed is one less than the scan line desired.

A.4.14 End Vertical Blanking Register (Index = 16)

Bits (7:5)
EGA: Not used.

Bits (4:0)
EGA: Identical to End Vertical Blanking Register Bits (4:0) definition in the VGA section.

A.4.15 Mode Control Register (Index = 17)

Bits (7:5)
EGA: Same as Mode Control Register Bits (7:5) definition in the VGA section.

Bit 4
EGA: Not used.

Bits (3:0)
EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.5 GRAPHICS CONTROLLER REGISTERS (PORT 3CF)

A.5.1 Read Map Select Register (Index = 04)

Bits (7:3)
EGA: Not Used.

Bits (2:0)
EGA: Map selected bits (2:0) which represent encoded value of the memory plane in binary as shown below:

D2	D1	D0	MAP SELECTED
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

A.5.2 Mode Register (Index = 05)

Bit (7:6)
EGA: Not Used

Bits (5:2)
EGA: Identical to Mode Register Bits (5:2) definition in the VGA section.

Bits (1:0)
EGA: Binary coded write bits define the write modes per table below:

BIT 1	BIT 0	FUNCTION
0	0	Write mode 0 - Refer to VGA section
0	1	Write mode 1 - Refer to VGA section
1	0	Write mode 2 - Refer to VGA section
1	1	Write mode 3 - Not Legal. Selects write mode 1.

A.6 ATTRIBUTE CONTROLLER REGISTERS (PORTS = 3C0/3C1)

A.6.1 Palette Registers (Index = 00 through 0F)

BIT	FUNCTION
7 - 6	Not used
5 - 0	Dynamic color selection

Bits (7:6)
EGA: Not Used.

Bits (5:0)
EGA: Dynamic color selection. Logic 0 = Color deselection, and Logic 1 = color selection per the table below:

BITS	COLOR	PIXEL
5	Sec. Red	VID 5
4	Sec Green/Inten	VID 4
3	Sec Blue/Mono	VID 3
2	Red	VID 2
1	Green	VID 1
0	Blue	VID 0

A.6.2 Mode Control Register (Index = 10)

BIT	FUNCTION
7 - 4	Not used
3 - 0	Same as Mode Control in VGA section

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.6.3 Overscan Color Register (Index = 11)

BIT	FUNCTION
7 - 6	Not used
5 - 0	Overscan color for border

Bits (7:6)

EGA: Not Used

Bits (5:0)

EGA: Overscan color for the border. For a monochrome display, set all the six bits to logic 0. The border color is defined by the color table for the Palette registers shown above.

A.6.4 Color Plane Enable Register (Index = 12)

BIT	FUNCTION
7 - 6	Same as Color Plane Enable - VGA
5 - 4	Video Status Multiplexer
3 - 0	Same as Color Plane Enable - VGA

Bits (7:6)

EGA: Same as Color Plane Enable Register Bits (7,6) in the VGA section.

Bits (5:4)

EGA:
Determines two of six colors for the Video Status Multiplexer per the table listed:

BIT 5	BIT 4	INPUT STATUS REGISTER 1 (Port 3?A)	
		BIT 5	BIT 4
0	0	VID 2(Red)	VID 0 (Blue)
0	1	VID 5(SRed)	VID 4 (SGreen)
1	0	VID 3(SBlue)	VID 1 (Green)
1	1	VID 5(SRed)	VID 4 (SGreen)

Bits (3:0)

EGA: Same as Color Plane Enable Register Bits (3:0) definition in the VGA section.

A.6.5 Horizontal PEL Panning Register (Index = 13)

BIT	FUNCTION
7 - 4	Not used
3 - 0	Horizontal left shift of the video data in number of pixels.

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: These four bits determine the horizontal left shift of the video data in number of pixels. In monochrome alpha numeric modes, (9 dots/character) image can be shifted by 9 pixels. For all other graphics or alpha numeric modes, a maximum left shift of 8 pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section.

A.7 APPLICATIONS

The WD90C11 applications section is divided into various interfaces such as processor (AT or Micro Channel mode), video memory, RAMDAC, monitor, and clock. The description and block diagrams are generic. No attempt is made to present schematic level details. Currently available application notes, technical briefs, and referenced literature at the end of the data book should supplement the information provided in this section. The Figures 9 through 17 are shown along with their brief description on the subsequent pages.

Figure 9 highlights the various WD90C11 Processor, memory, and I/0 interfaces.

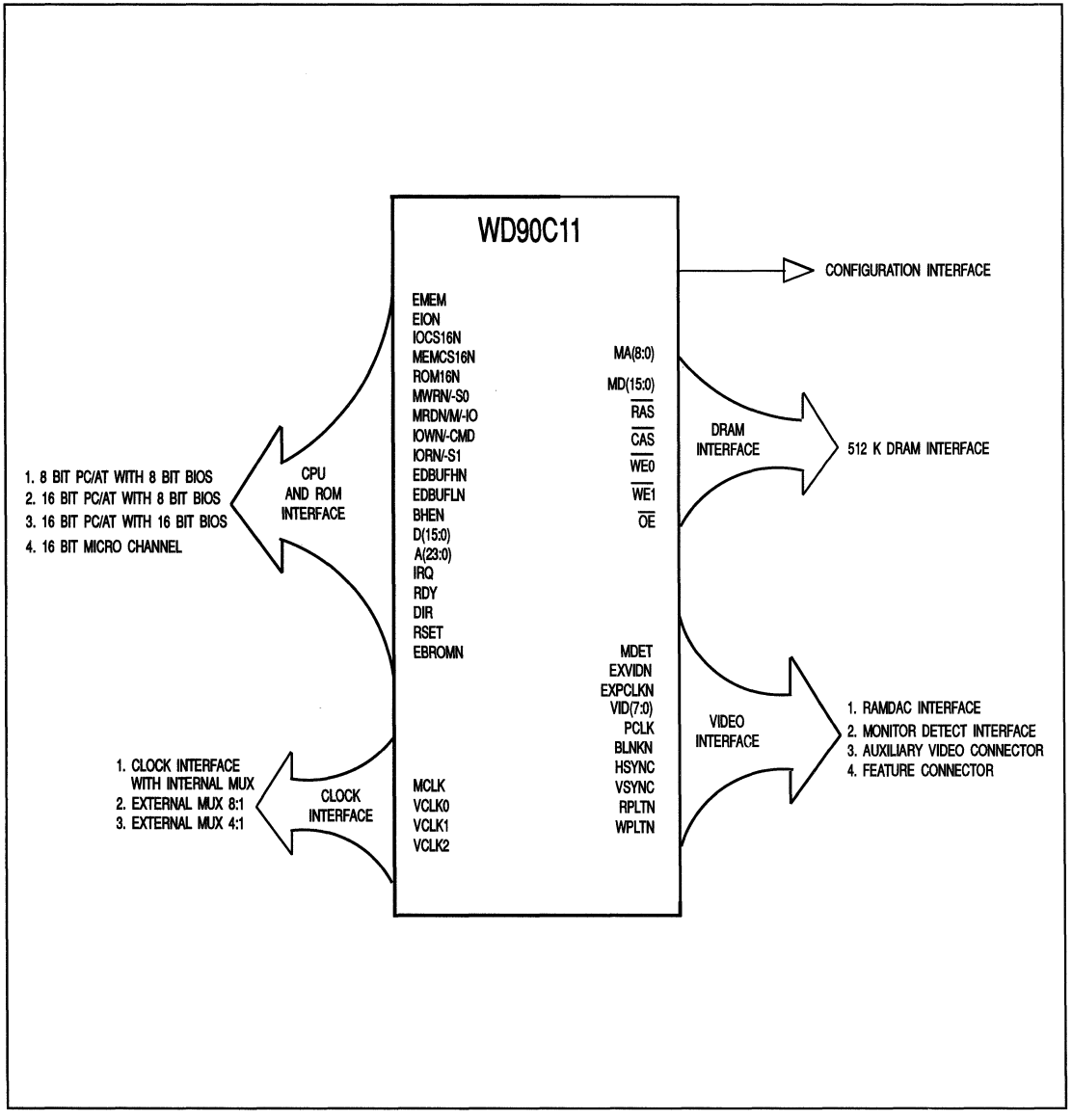


FIGURE 9. WD90C11 INTERFACES

Figure 10 shows a block diagram of the WD90C11 with 8 bit PC/AT interface using 8 bit BIOS. The system data bus SD(7:0) and address bus SA(19:0) are shown along with associated buffers and BIOS ROM.

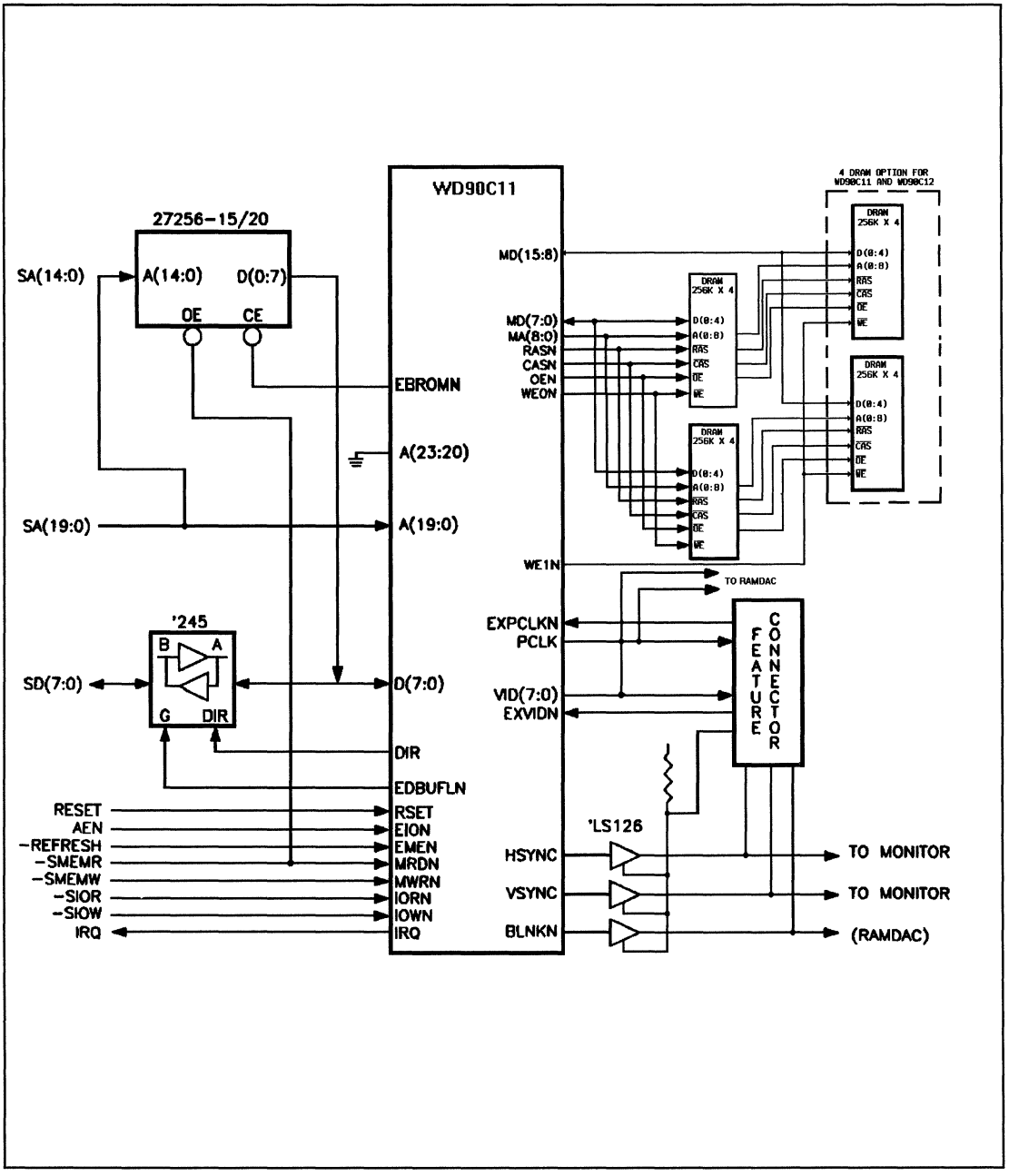


FIGURE 10. 8-BIT PC AT INTERFACE WITH 8-BIT BIOS

Figure 11 illustrates 16-bit PC/AT interface with 8-bit BIOS using WD90C11. For 386 systems, the processor data bus SD(15:0), and the system address bus SA(19:0) are shown. Associated address and data bus buffers and BIOS ROM are also shown in it.

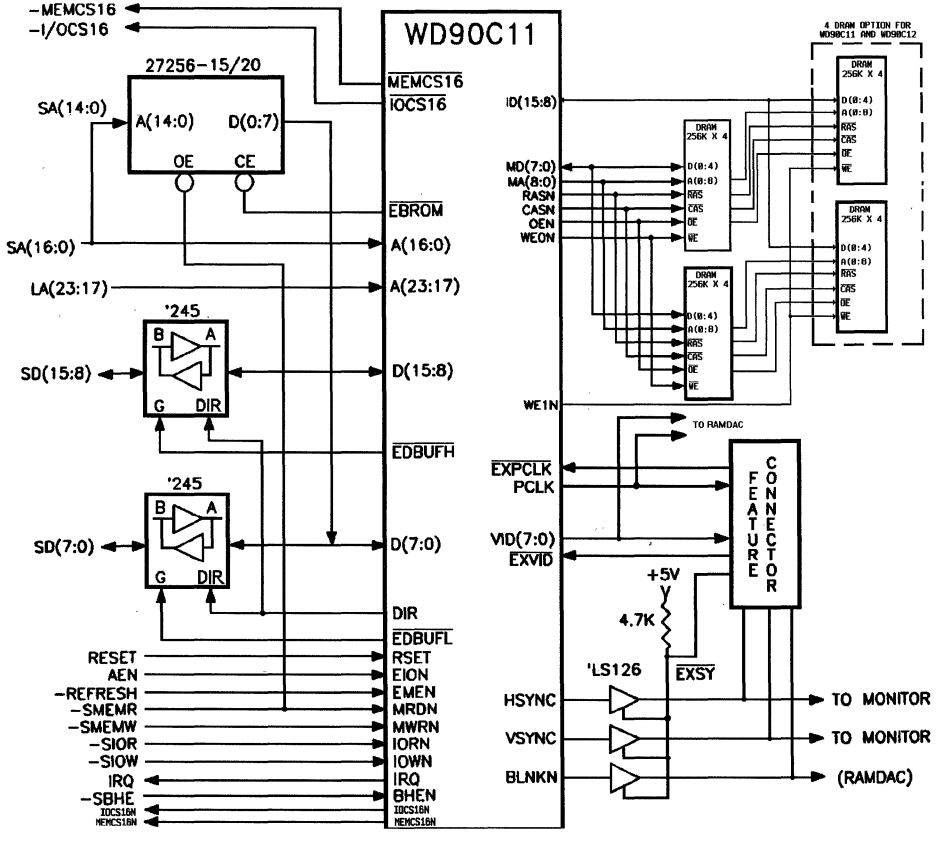


FIGURE 11. 16-BIT BIOS PC AT INTERFACE WITH 8-BIT BIOS

For systems that do not meet hold time of LA address valid from falling edge of MEMR or MEMW, then pull MD8 down and connect LA addresses and SA addresses as shown in Figure 12(a). This applies to most 286 systems. Otherwise, connect LA addresses and SA addresses as shown in Figure 12(b). This applies to most 386 systems

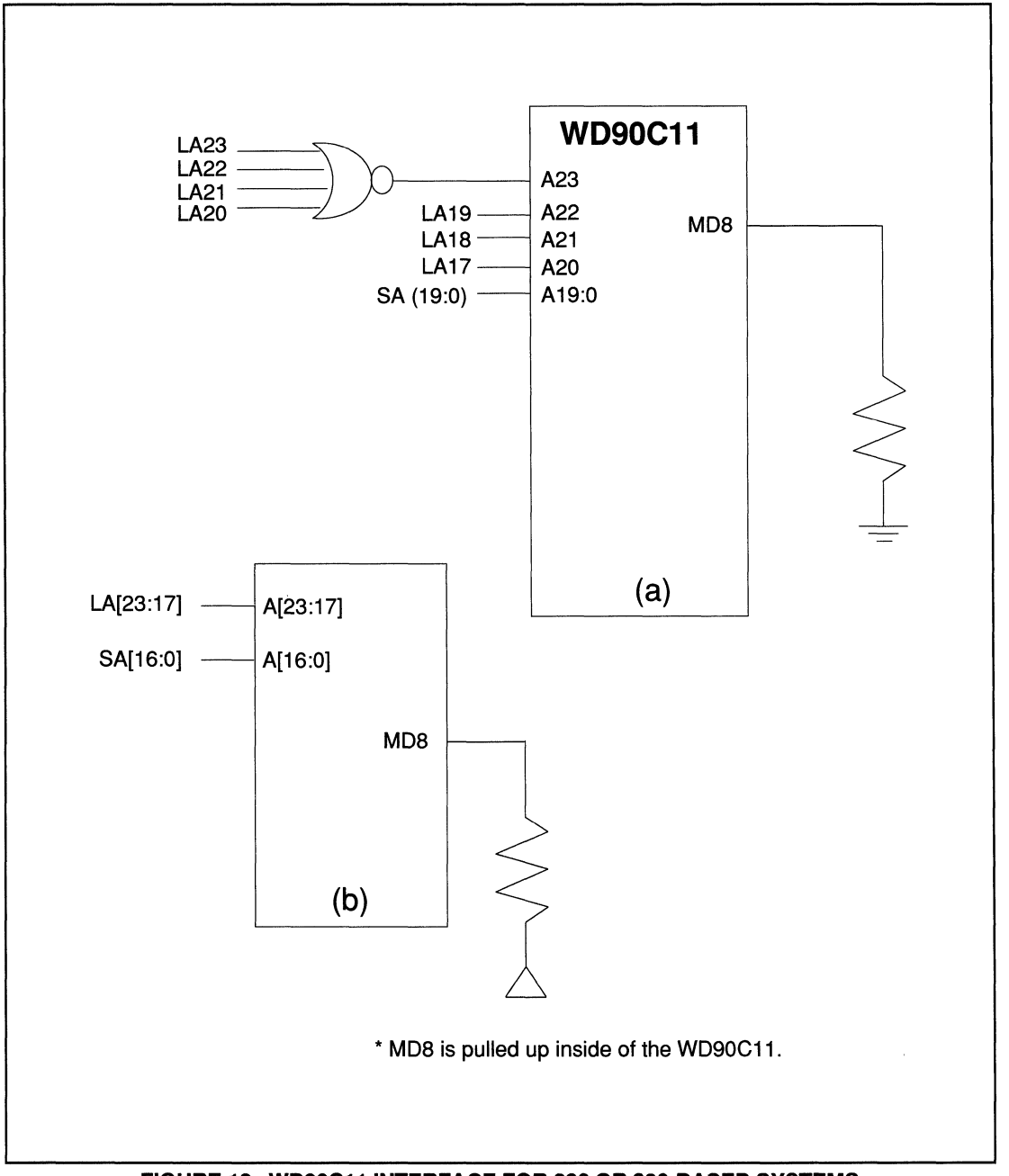


FIGURE 12. WD90C11 INTERFACE FOR 286 OR 386-BASED SYSTEMS

Figure 13 describes a 16-bit PC/AT interface with 16-bit BIOS ROM implementation using the WD90C11. The system data bus SD(15:0), address and data bus buffers are presented. Also, $\overline{\text{MEMCS16}}$ implementation is limited to certain bus speeds as SA15 and SA16 are used for the 16-bit BIOS. Refer to Figure 12 for 286-based systems.

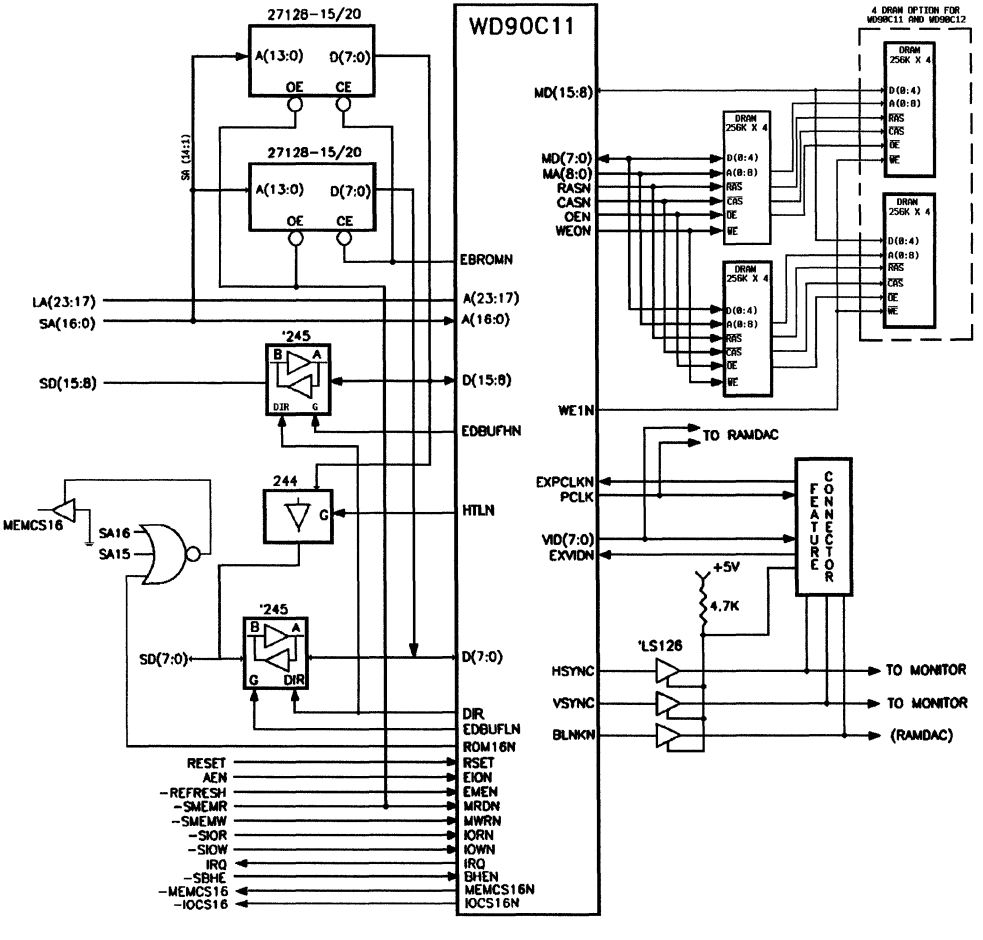


FIGURE 13. 16-BIT PC AT INTERFACE WITH 16-BIT BIOS (WITH OPTIONAL 512 KBYTES: 4- 256K BY 4 DRAM)

Figure 14 illustrates the WD90C11 and 16-bit Micro Channel interface. 3C3.D0 is output of port 3C3H bit 0 VGA Subsystem Enable Register.

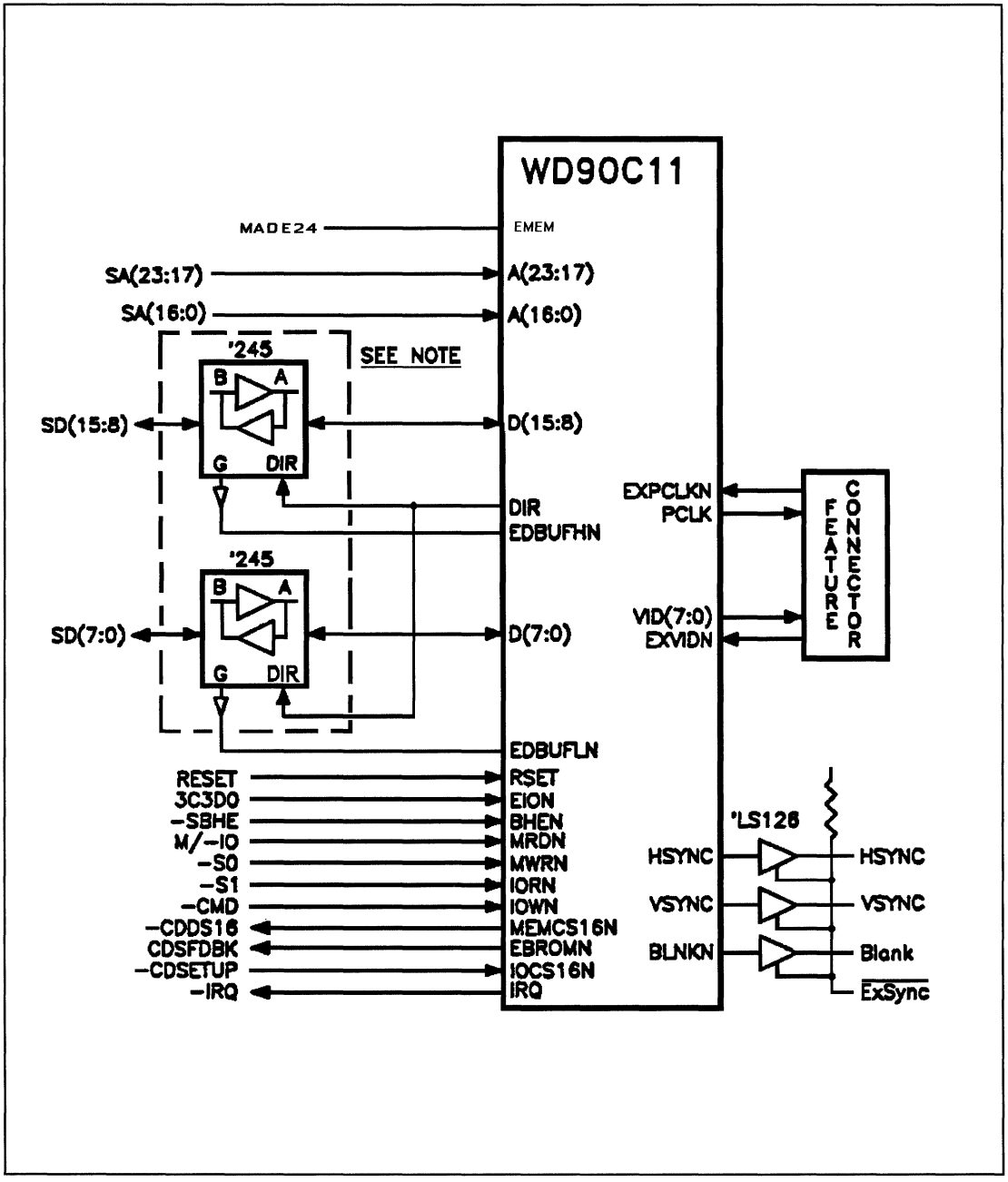


FIGURE 14. 16-BIT MICRO CHANNEL INTERFACE

Figure 15 illustrates the WD90C11 and RAMDAC (WD90C50) interface block diagram for analog monitors.

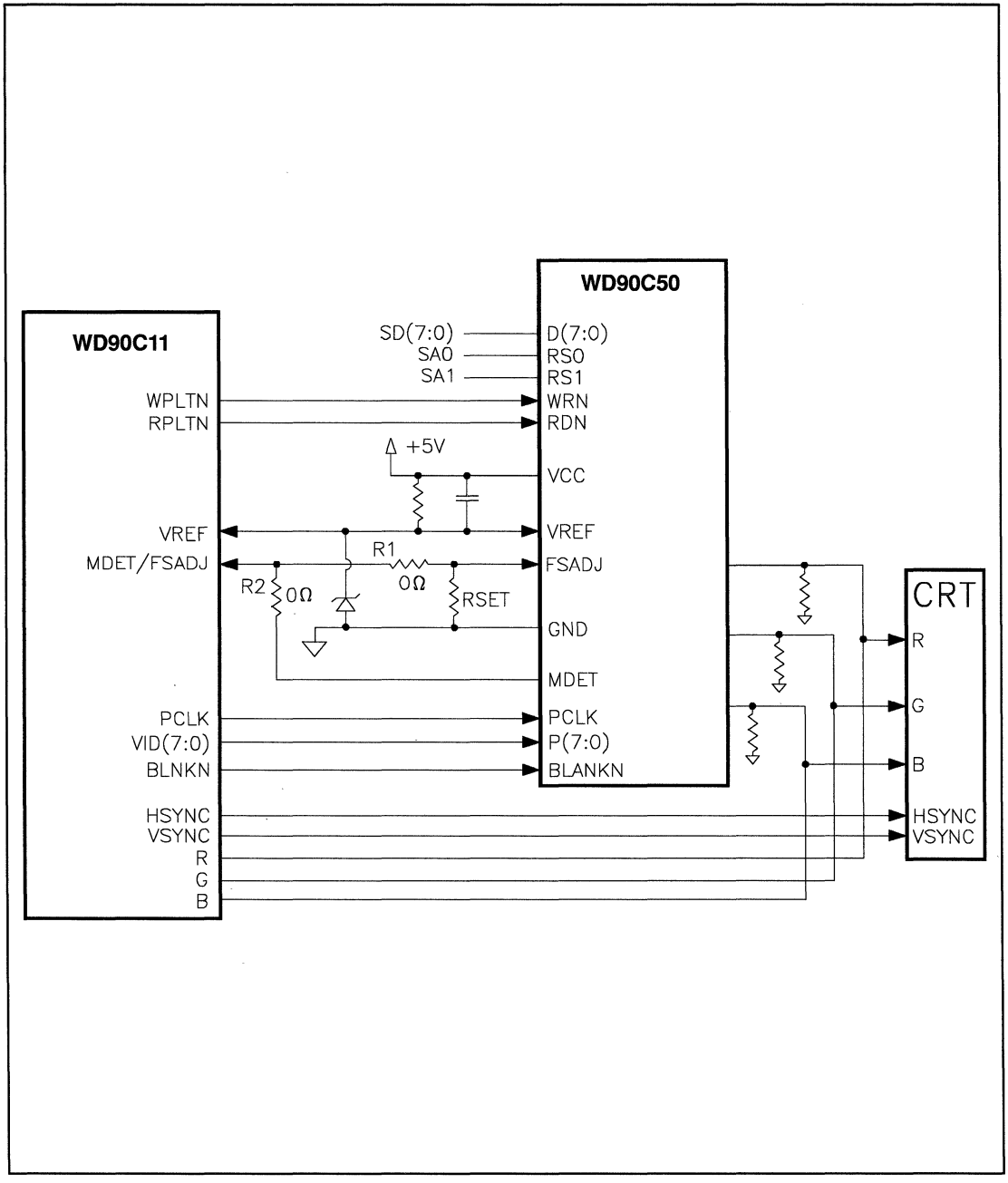


FIGURE 15. WD90C11 WITH RAMDAC INTERFACE

Figure 16 illustrates the WD90C11 and TTL monitor connections.

NOTES:

1. VGA/TTL switch may be used to disable HSYNC and VSYNC for Analog or TTL Video connector.
2. MD(15:12) may also be connected as the EGAswitches if desired. See PR register and Pin out sections for more details.
3. For AT applications using the WD90C11, install the IRQ9 resistor.
4. Transistor 2N2222A is used to emulate a Monochrome and a Color Display connection.

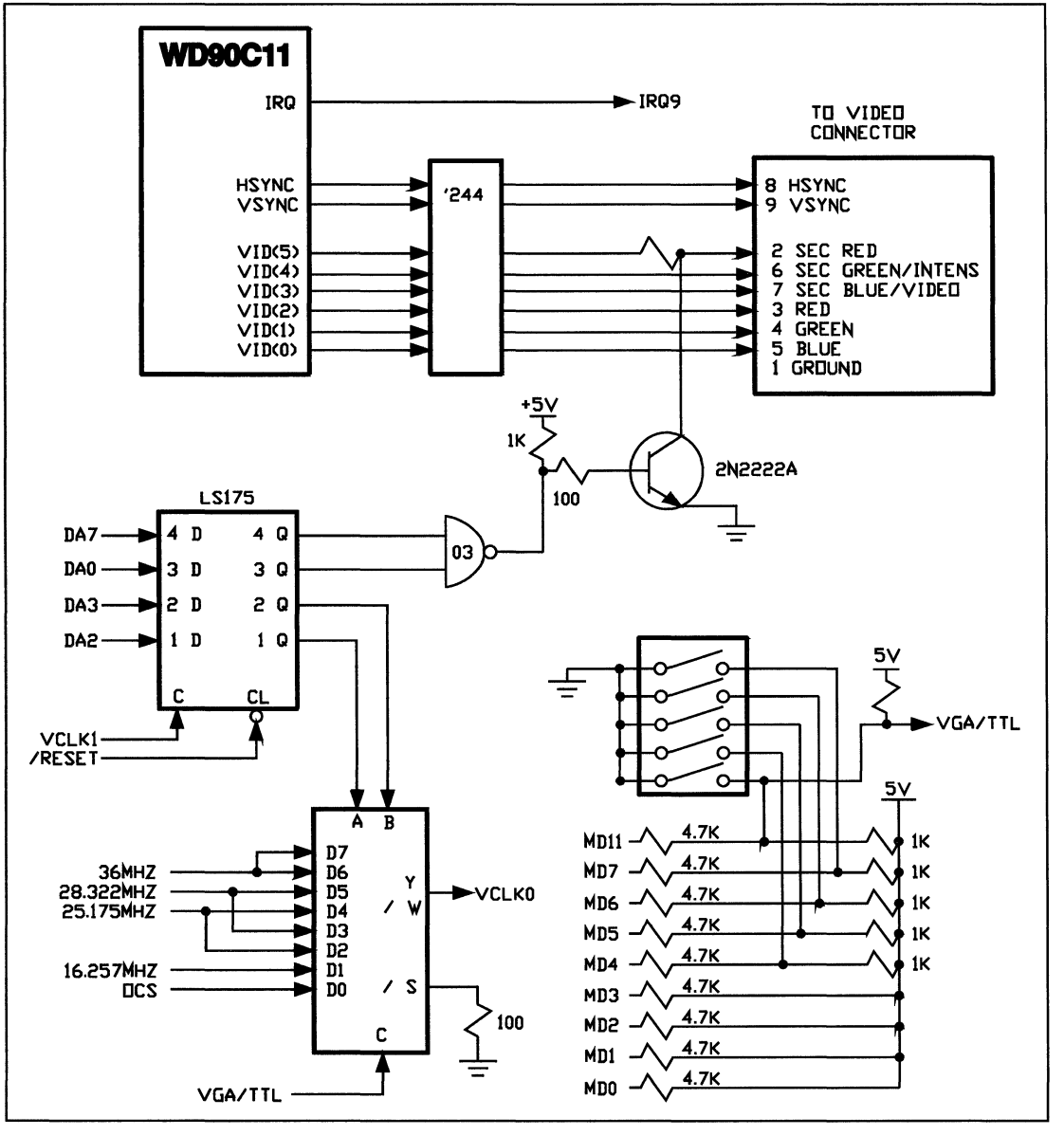


FIGURE 16. WD90C11 AND TTL MONITOR CONNECTIONS

Figure 17 illustrates the WD90C11 with external oscillators at the clock pins configured as inputs. The clock selection is determined by register 3C2H bit 3 and bit 2. It is described by the table below:

3C2H BIT 3	3C2H BIT 2	CLOCK SELECTION
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

The Configuration register Bit 3 (MD3) should be tied low to make the WD90C11 signal pins (VCLK1, VCLK2) inputs.

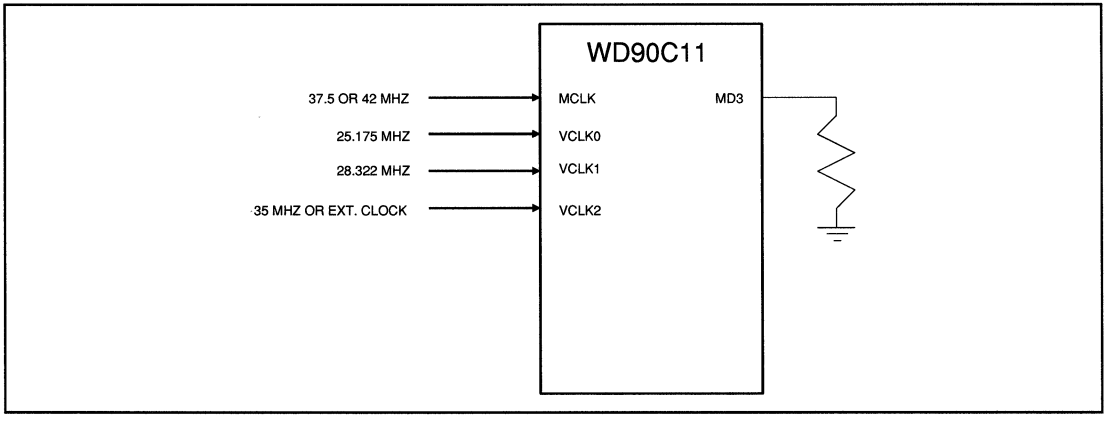


FIGURE 17. CLOCK INTERFACE

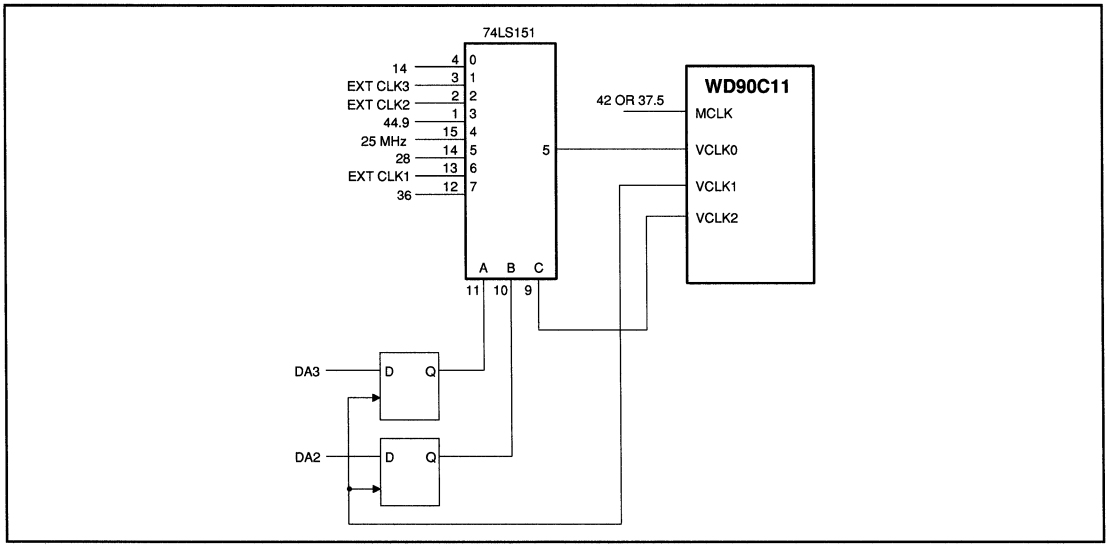


FIGURE 18. EXTERNAL VIDEO CLOCK MULTIPLEXING

A.8 REFERENCES

A list of references for generating the WD90C11 data book is shown below:

- IBM Personal Computer Hardware User Guide (IBM # 6322510)
- IBM Personal Computer XT Hardware User Guide (IBM # 6322511)
- IBM Personal Computer AT hardware User Guide (IBM # 6280066)
- IBM Personal System 2 Model 30 Hardware User Guide (IBM # 68x2230)
- IBM Personal Computer AT Technical Reference Manual (IBM # 6280070)
- IBM Personal System 2 Model 30 Technical Reference Manual (IBM # 68x2201)
- IBM PC Options & Adapters Technical Reference Manual (IBM # 6322509)
- IBM Personal System 2 BIOS Reference Manual (IBM # 68x2260)
- Personal Computer Reference Manual (IBM # 6025005)
- AT&T Video Display Controller VDC 750 / VDC 600 Installation Guide
- Hercules Graphics Card Owner's Manual
- Paradise OEM Technical Publication Manual

The customers are urged to refer to the manuals listed above and supplement their knowledge from other books and literature available.

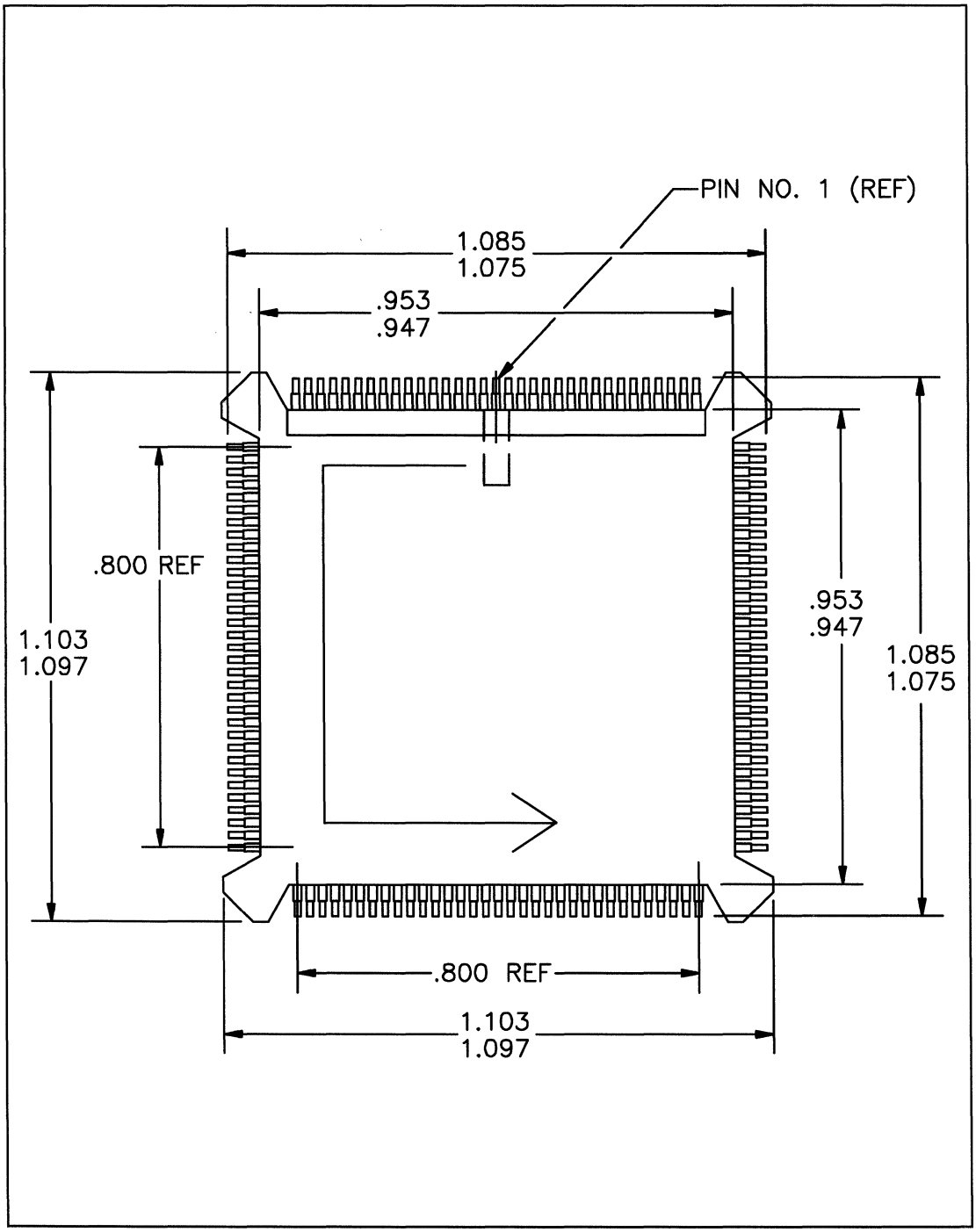


FIGURE 19. 132-PIN JEDEC PLASTIC FLAT PACKAGE (PFP) 1 OF 2

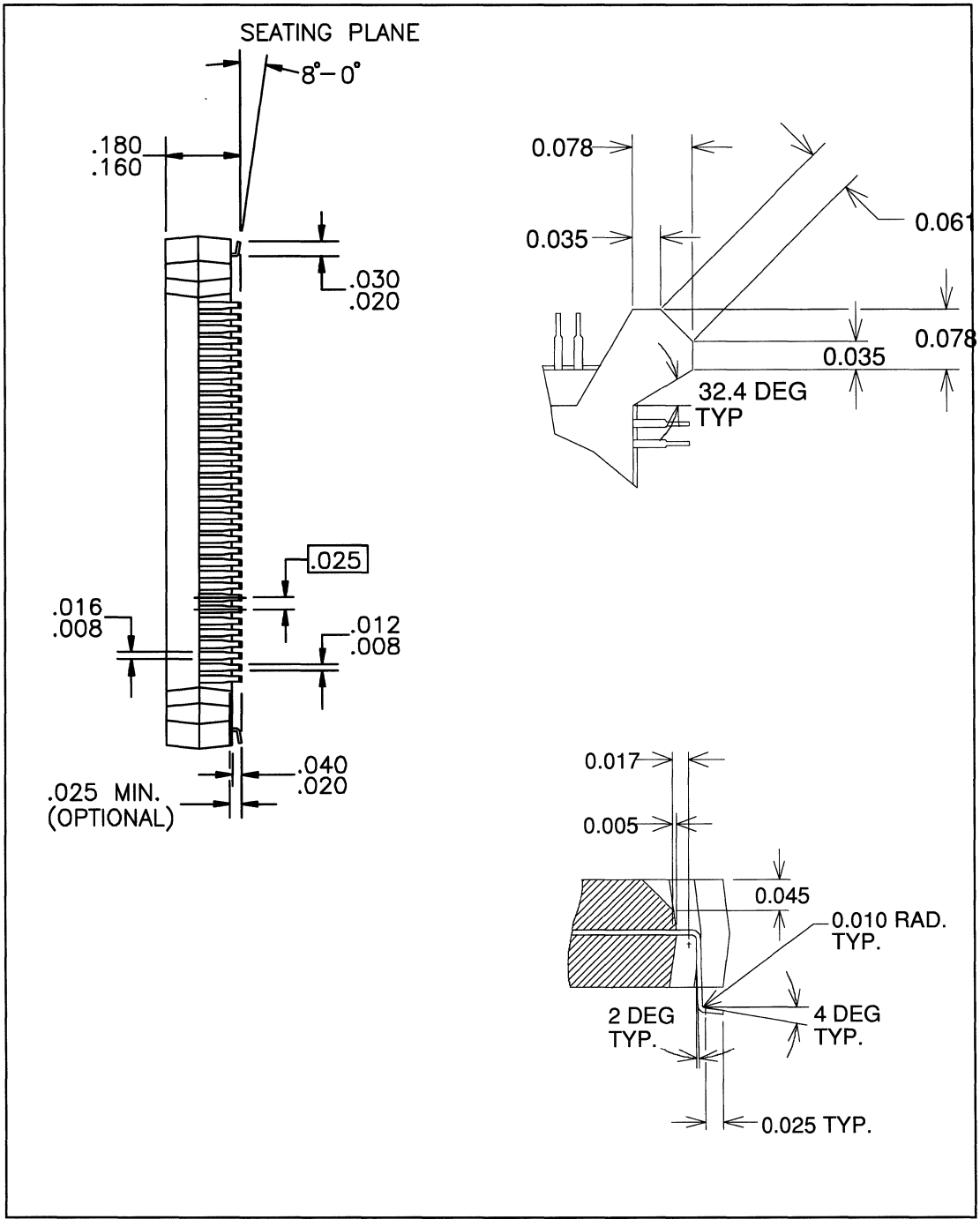
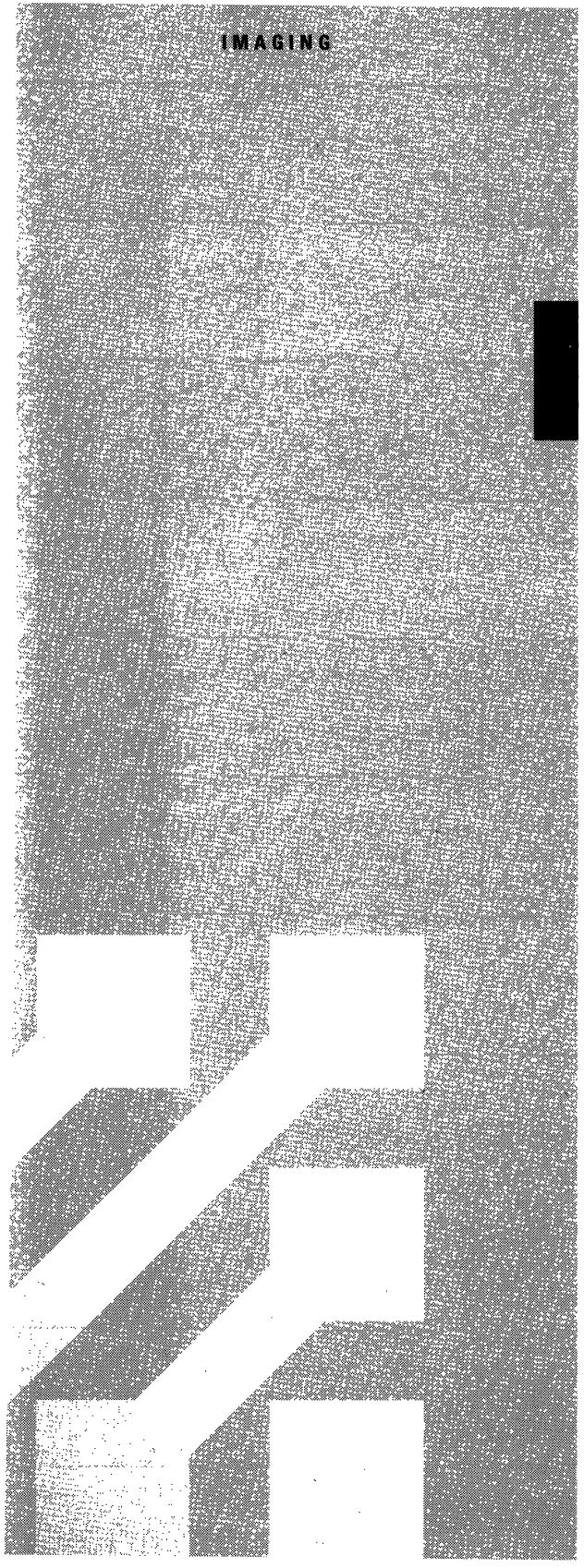


FIGURE 19. 132-PIN JEDEC PLASTIC FLAT PACKAGE (PFP) 2 OF 2

WD90C20, WD90C22

(PVGA1F) VGA Flat Panel

Display Controllers



WESTERN DIGITAL

TABLE OF CONTENTS

APPENDICES

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

1.0 DESCRIPTION AND APPLICATION

The information in this manual applies to the WD90C22 as well as to the WD90C20. The manual also describes the additional features of the 64 gray scale WD90C22.

The WD90C20 is a VGA display controller that has been optimized for applications that require flat panel display support. It is an extension of the WD90C00 and as such supports all of the WD90C00's features and modes when driving a standard CRT. The WD90C20's highly integrated design includes a complete Micro Channel or AT compatible bus interface, as well as an on-chip PS/2 compatible RAMDAC with integral monitor detection logic. The controller's 1.25 micron CMOS construction and power management features significantly reduce the power required for the display subsystem.

Flat panel displays supported include all 640 by 480 monochrome and color liquid crystal displays (LCD), as well as Plasma displays.

1.1 Features

- On-chip Micro Channel interface
- On-chip 8- or 16-bit AT bus interface
- Directly drives CRT, Plasma and monochrome and color LCD displays
- On-chip frame rate modulation logic
- Supports all functions of WD90C00 VGA chip in CRT mode
- 32, 16, or 8 shade gray scale mapping
- Software-selectable vertical screen centering
- On-chip PS/2 compatible RAMDAC
- On-chip monitor detection logic
- 45 MHz maximum video clock
- Flexible power management features
- Vcc may be removed in powered system
- 256 color support for TFT and DSTN color LCDs

2.0 THEORY OF OPERATION

The WD90C20 contains six major functional modules. In addition to the CRT controller, there is a sequencer, a graphics controller, an attribute controller, a flat panel interface, and a RAMDAC. The WD90C20 handles all display buffer management functions, including display refresh cycles, memory refresh cycles, and the arbitration and sequencing of host access cycles.

- **Sequencer**

The sequencer provides the display memory control signals and timing. It also provides the synchronization between the CRT controller and the attribute controller. The sequencer controls the arbitration between the CPU cycle and the CRT cycle, or the CPU cycle and the memory refresh cycle.

- **Graphics Controller**

The graphics controller manages data flow between video memory and the attribute controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the sequencer.

- **Attribute Controller**

The attribute controller modifies the CRT display data stream in graphics and character modes. It controls display attributes such as blinking, underlining, cursor, scrolling, reverse video (as well as background or foreground video) in VGA and enhanced VGA BIOS modes.

- **Flat Panel Adapter**

The flat panel adapter section includes color-to-gray scale mapping, RAM mapping, shading control, and panel interface logic.

- **RAMDAC**

The WD90C20's on-board RAMDAC is a low power, PS/2-compatible device with special power down modes and PS/2 monitor detection logic.

The RAMDAC's 256 by 18 color look-up table has triple 6-bit D/A converters, a pixel mask register, and composite blank generation on the

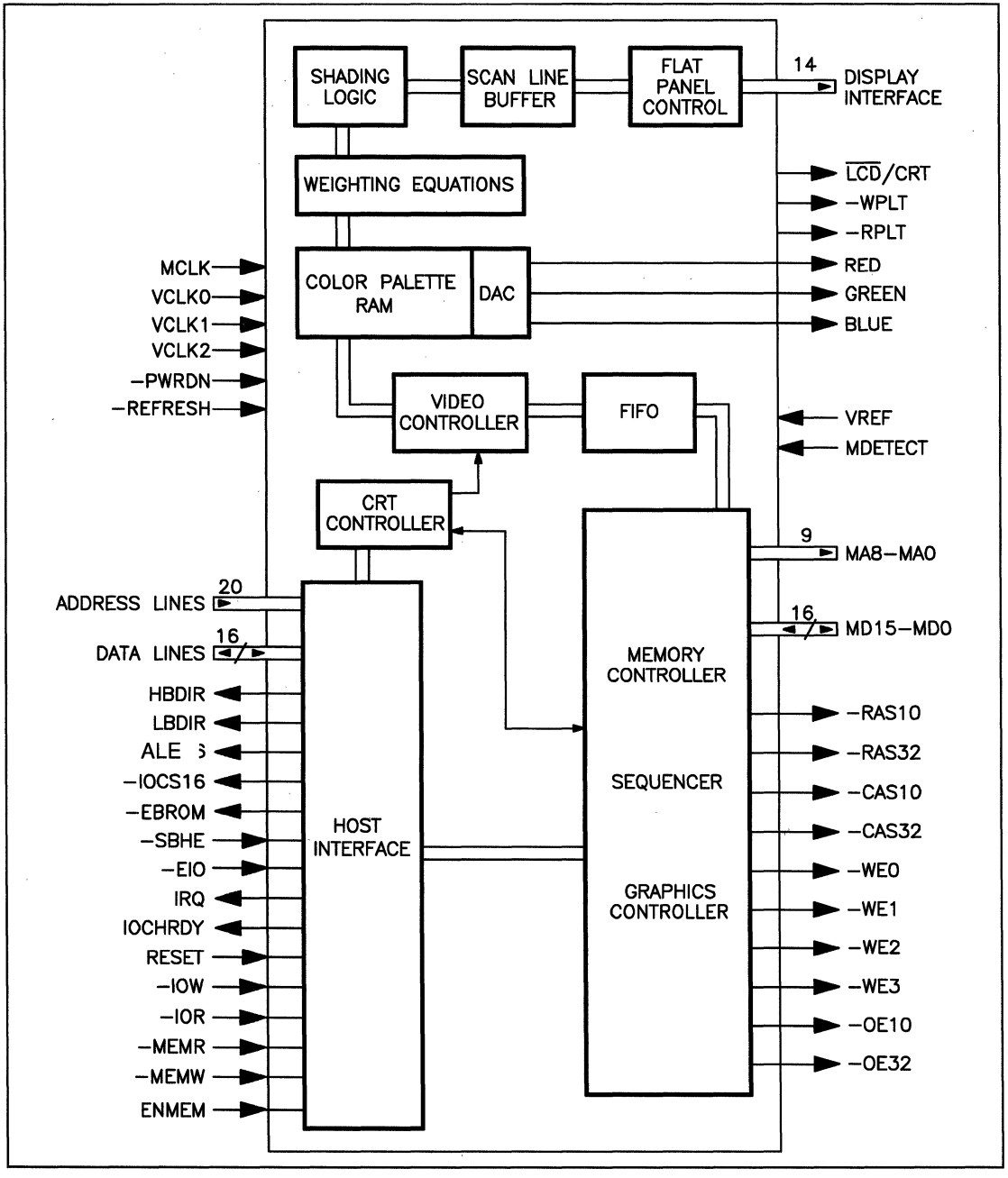


FIGURE 2-1. WD90C20 BLOCK DIAGRAM

three channels. Options supported include a programmable pedestal (0 or 7.5 IRE) and the use of an external voltage reference. Without external buffering the RAMDAC will generate RS-343A-compatible video signals into a singly terminated 75 ohm load. Integral and differential linearity errors are a maximum of ± 1/4 LSB.

2.1 WD90C20 INTERFACES

The WD90C20 has five main system interfaces: the CPU, a display memory, a RAMDAC/CRT, a clock, and a flat panel display. In most implementations, these interfaces eliminate the need for glue logic.

- **CPU Interface**

The WD90C20 host interface supports both the AT and Micro Channel buses with both eight and sixteen bit data path widths. The WD90C20 may also be directly connected to the bus if drive requirements permit. The bus mode is determined by the status of the configuration register bit, CNF(2), which is loaded by the de-assertion of reset. The value that is loaded reflects the status of one of the memory data pins at reset.

I/O transfers to and from the device are eight bits wide, and display memory transfers are eight or sixteen bits wide, depending on the video mode selected. Because of their architecture, EGA type planar modes are restricted to eight bit display data transfers. Text and 256 color extended modes allow 16 bit transfers on a 16 bit bus.

The controller generates wait states as required during display memory accesses. Wait states are not generated for I/O or video BIOS ROM accesses. Special I/O ports, such as 46E8H (when in AT bus mode) for setup, and 102H for VGA enable, are internally implemented.

- **Display Memory Interface**

The WD90C20 generates all signals and memory timing required to operate the display memory. It directly controls three display memory sizes, 256K, 512K, and one megabyte, as follows:

Memory Size	No. and Type of DRAM Required
256 Kbytes	8 64K x 4 DRAMs, or 2 64K x 16 DRAMS
512 kbytes	16 64K x 4 DRAMs or 4 64K x 16 DRAMs
1 MB	8 64K x 16 DRAMs or 8 256K x 4 DRAMs

Page mode memories are required for all configurations. With a 36 MHz memory clock (MCLK), 120nS devices may be used. If 256 color CRT modes are to be supported, 100nS DRAMs and a 45 MHz MCLK are required. The WD90C20 includes special offset registers that allow the host to address up to 1 Mbyte of display memory.

- **CRT/RAMDAC Interface**

In addition to its internal RAMDAC, the WD90C20 allows the use of an external RAMDAC. This is helpful in specialized applications where a 24-bit wide color lookup table or pixel demultiplexing (to obtain higher video rates) is required. The external RAMDAC interface will support any Bt471/478/476 compatible device.

- **Clock Interface**

The WD90C20 has four clock input signal pins. Three of these (VCLK0, VCLK1, and VCLK2) are normally connected to oscillators. VCKL1 and VCLK2 may be configured to control an external clock multiplexor or clock generator, such as the WD90C61. In this configuration, VCLK0 becomes the clock input while VCLK1 and VCLK2 become outputs used to drive the multiplexor select inputs.

The memory clock input, MCLK, is used by the internal logic to generate all memory timing and may be up to 36 MHz for 120ns DRAMs or 45 MHz for 100 ns DRAMs.

- **Flat Panel Interface**

The WD90C20 is designed to interface with 640 by 480 LCD or Plasma panels. The flat panel interface lines change function to support the specific panel type chosen. Table 2-1 summarizes their use for each mode of operation.

When in LCD mode, with frame rate modulation selected, the controller supplies 8 pixels per shift clock (four for the upper panel and four for the

lower). If pulse width modulation is selected, the controller provides two pixels per shift clock (one four bit pixel for the upper screen and one four bit pixel for the lower screen).

When in Plasma mode, pulse width modulation is used to provide shading, while the controller supplies one pixel (four bits per pixel) per clock.

When in color STN LCD mode, the controller supplies 2 pixels per shift clock and uses hardware dithering. Each pixel (three bits, one each for R, G, and B), with dithering, provides 16 colors. The user can select any 16 out of 26 colors by programming a 32 x 5 mapping RAM.

LCD	PLASMA	CRT
UD (3:0)	VD (3:0)	P (7:4)
LD (3:0)	Reserved	P (3:0)
FR	Reserved	BLANK
FP	VS	VSYNC
LP	HS	HSYNC
XSCLK	XSCLK	Reserved
WGTCLK	ENABLE	Reserved
Reserved	Reserved	PCLK

TABLE 2-1. DISPLAY INTERFACE OUTPUT FUNCTIONS

Monochrome LCD	Color LCD
UD (3)	B1
UD (2)	G1
UD (1)	R1
UD (0)	Border Information
LD (3)	B2
LD (2	G2
LD (1)	R2
LD (0)	Reserved

TABLE 2-2. LCD DATA BIT ASSIGNMENTS

- **Power Up Configuration**

An internal eight-bit configuration register, CNF, controls the behavior of the major interfaces. Its bits are loaded with the inverted state of memory data lines 0 through 7 at the time RESET is de-asserted. Pull-up or pull-down resistors on the MD lines are used to set the configuration.

3.0 FLAT PANEL SUPPORT CONSIDERATIONS

Supporting VGA compatible graphics on flat panel displays involves several non-trivial issues, including:

- Display timing differences
- Screen size mapping
- Color-to-gray scale mapping
- Shading mechanics
- Split screen refresh

The following paragraphs address each of these issues.

- **Display Timing Differences**

Typically, flat panel displays have different timing requirements from a CRT. To overcome this problem, the WD90C20 provides a set of hidden display timing registers, which are read/write protected in locked mode.

- **Screen Size Mapping**

Unlike those of a CRT, the pixels on a flat panel display are real, discrete entities of a fixed size. This can result in problems when different display modes are mapped onto a single panel. The WD90C20 has been designed to support VGA and various backward compatible display modes on a 640 by 480 dot flat panel and it provides integral hardware support to deal with screen size incompatibilities.

In case of backward compatible display modes, such as EGA, which has a maximum resolution of 640 by 350, the vertical resolution of the mode is less than the number of dots of vertical resolution of the panel. This results in an active display area that is smaller than that of the panel and shifted up on the display, as shown in Figure 3-1(A). There are two ways to handle such situations, both of which are supported by the WD90C20.

The simplest approach is to keep the vertical resolution of the display mode constant but center the active display area vertically on the panel. In the case of an EGA 350 line mode being displayed on a 480 line panel, this would involve shifting the active display area down 65 lines (that is, 480 minus 350, the quantity divided by two). The effect of such a mapping is shown in Figure 3-1(B).

If the goal is to have the active display area fill the panel in all modes, then the active display area can be expanded by double scanning a portion of the active scan lines. Previously available controllers simply double scan lines at regular intervals, every third line in the case of EGA 350 line modes.

Future revisions of the WD90C20 will use an advanced proprietary algorithm that automatically

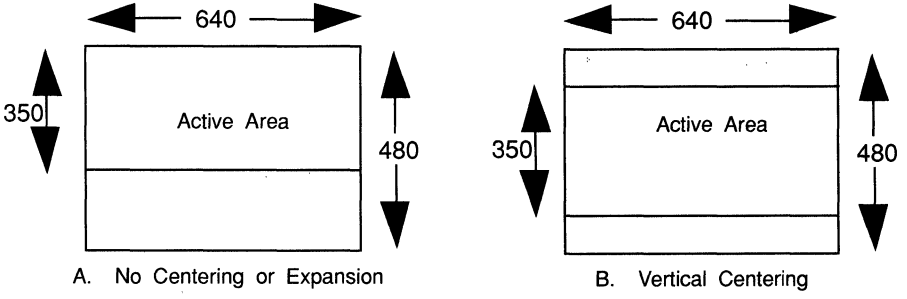


FIGURE 3-1. EXAMPLE OF SCREEN SIZE MAPPING.

expands to fill all 480 lines. This algorithm can be used to support better "screen scrolling" when in 350 line modes.

Under certain display conditions, any expansion scheme can result in undesirable aliasing effects of the displayed data. For this reason the WD90C20 allows the system designer flexibility to choose between vertical expansion or centering as appropriate.

Horizontal resolution issues involve 720 dot modes such as VGA text and Hercules graphics. In VGA test mode, the 9th dot in each character box is dropped. The net effect is a slight compression in the spacing between characters. Alternatively, a different font may be loaded, although a nonstandard font size may not be fully compatible.

- **Color-to-Gray Scale Mapping**

The VGA standard defines how colors are mapped to 64 gray scale values on monochrome monitors. The mapping is based on the following RGB weighting equation:

$$I = .30R + .59G + .11B$$

Unfortunately, many of the currently available panels support at most sixteen shades and some only support two. In order to provide faithful support of all of the standard VGA modes on a flat panel, the WD90C20 provides a range of features to map colors to intensities and control panel shading. Foremost among these is sophisticated logic that converts gray scale values into dithering patterns. Additionally, the device allows software modification of the weighting values used in the gray scale mapping equation. Figure 3-2 gives an overview of the color to gray scale support provided by the WD90C20.

- **Shading Mechanics**

The WD90C20 supports shading via either frame rate or pulse width modulation. Pulse width modulation is handled via the display panel. The controller transfers 2, 3, or 4 bits per pixel to the driver logic on the panel, along with a high speed clock signal used to sequence the shading logic. Frame rate modulation, on the other hand, must be implemented in the display controller. The WD90C20 provides support for 2, 4, 8, 16, or 32 shade frame rate modulation with its integrated dithering controller. Any combination of dithering patterns can be selected via the dithering controller's mapping RAM. This design allows the WD90C20 to provide flicker-free frame rate modulation with frame rates as low as 70 Hz.

- **Split Screen Refresh**

The WD90C20 provides complete support for panels that are split into upper and lower panels requiring simultaneous refresh. This type of refresh is typically used by non-active matrix LCDs and plasma panels.

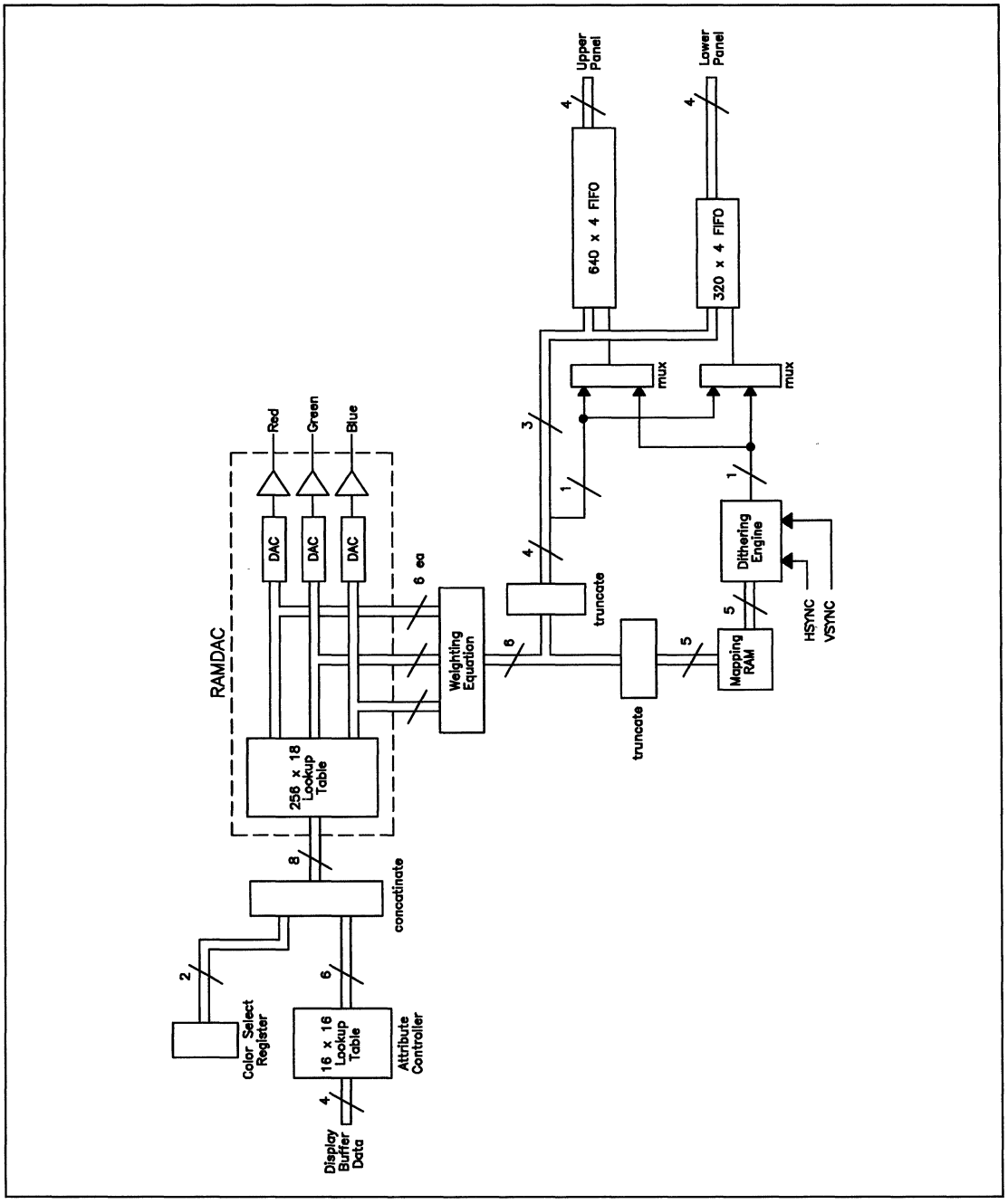


FIGURE 3-2. WD90C20 COLOR MAPPING

4.0 PIN DESCRIPTIONS

Figure 4-1 illustrates the 132 plastic flat pack (PFP). Table 4-1 lists all pins referenced in Figure 4-1 and provides a detailed description of each pin.

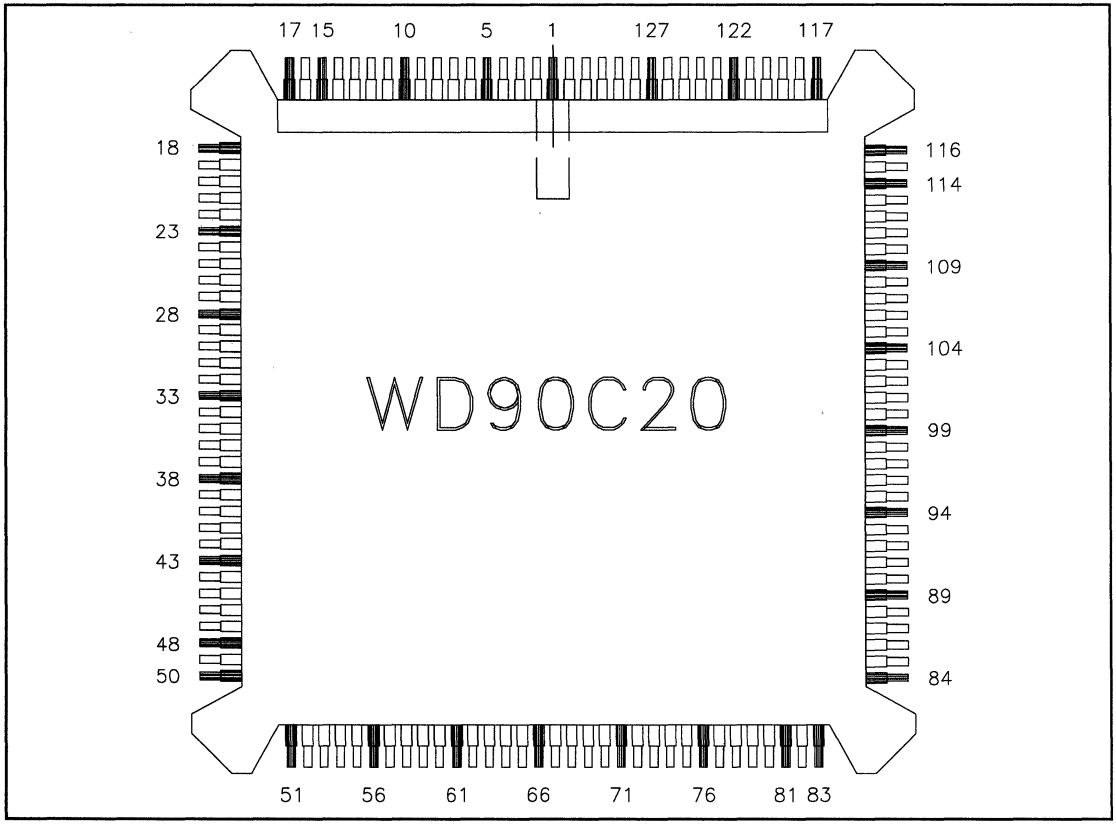


FIGURE 4-1. 132-PIN PFP (TOP VIEW)

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
	POWER ON		
42	RESET	I	RESET: This signal input will reset the WD90C20. MCLK and VCLK0 should be connected to the WD90C20 in order for the WD90C20 to initialize during reset. WD imaging registers, PR1 and CNF, are initialized at power-up reset based on the logic level on the MD15-0 bus as determined by pull-up/ pull-down resistors. The reset pulse width should be at least ten MCLK clock periods.
	CLOCK SELECTION		
96	VCLK2	I/O	VIDEO CLOCK 2: This pin can be a third video display clock input or an output to the external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. It acts as either a user-defined external clock input, or as an output reflecting the content of bit PR2(1) if CNF (3) is set to 1. Refer to the Configuration Register description. MCLK should be greater than or equal to VCLK2.
97	VCLK1	I/O	VIDEO CLOCK 1: This pin can be a second video display clock or an input or an output to the external clock selection module. Pin direction is determined on reset by a pull-up/down resistor on pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 is an active low pulse during I/O writes to port 3C2H. Refer to the Configuration Register description. MCLK should be greater than or equal to VCLK1.
98	MCLK	I	MEMORY CLOCK: This clock signal determines the VGA graphics mode video DRAM read/write access timing as well as system microprocessor I/O and memory timing. MCLK should be approximately 36 MHz for 120 ns DRAMS, and 42.0 MHz for 100 ns DRAMS.
99	VCLK0	I	VIDEO CLOCK 0: This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK0 is 25.175 MHz to display 640 pixels per horizontal display line. MCLK should be greater than or equal to VCLK0. The Miscellaneous Output Register bits 2 and 3, both set to 0, will select this clock if VCLK1 and VCLK2 are used as inputs.

TABLE 4-1. PIN DEFINITIONS

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
HOST INTERFACE			
2 1 132 131 130 129 128 127 126 125 124 123 121 120 119 118 117	SA16 SA15 SA14 SA13 SA12 SA11 SA10 SA9 SA8 SA7 SA6 SA5 SA4 SA3 SA2 SA1 SA0	I I I I I I I I I I I I I I I I I	ADDRESS BUS (SA16-SA0): These active high inputs form the lower order 17 bits of video memory address. These inputs are directly connected to the system bus.
5 4 3	LA19 LA18 LA17	I I I	UNLATCHED ADDRESS BUS (LA19 -LA17): These active high inputs form the high-order three bits of video memory address. These addresses are not decoded during I/O accesses in AT or Micro Channel modes. These inputs are directly connected to the system bus.
6	SBHE	I	SYSTEM BYTE HIGH ENABLE: If SA0 is "0", this signal is used to enable 16 bit data transfer mode when SBHE is "0". With SA0, this signal is also used to select high byte data (SD[15:8]) or low byte data (SD[7:0]).
7	MEMEN	I	MEMORY ENABLE: This line is driven by external decode logic. In AT mode, this signal is decoded by LA23 - LA20 and $\overline{\text{REFRESH}}$. In Micro Channel mode, this signal is decoded by LA23 - LA20 and MADE24 ("1" = enable).
8	$\overline{\text{EIO}}$/ 3C3D0	I	ENABLE I/O: In AT mode, this active low signal is used to enable I/O address decoding and is connected directly to the system bus signal AEN (address enable). In Micro Channel mode, this line is from I/O port 3C3 bit 0, and enables video sub-system memory and I/O address decoding ("1" = enable).

TABLE 4-1. PIN DEFINITIONS (Continued)

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
11	ALE	I/O	ALE: In AT mode, this line is ALE; in MicroChannel mode, it is driven by the host to individually select channel connector slots during system configuration and error recovery procedures.
12	IRQ / $\overline{IRQ}$	O	INTERRUPT REQUEST: Programmable processor interrupt request. It is enabled via bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of the vertical display occurs, this signal goes active, causing an interrupt. It will stay latched until CRTC11 bit 4 clears it. In an AT system $\overline{IRQ}$ is not connected, although you may connect it if you desire. $\overline{IRQ9}$ is used to generate an interrupt in Micro Channel mode. For further details, refer to the reference literature.
13	$\overline{EBROM}$ $\overline{CDSFDBK}$	O	ENABLE BIOS ROM: In AT mode, this is an active low signal to enable BIOS ROM (C0000H - C7FFFH) if enabled by PR1(0). It is not active for access to addresses in the range C60000H-C67FFH, but this address range may be mapped-in by setting PR17 (0) = 0. A write to the WD90C20 internal I/O port address, 46E8H, causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping. In Micro Channel mode, this signal is used as Card Selected Feedback to provide positive acknowledgement of its presence at the addresses specified by the host.
14	$\overline{MEMCS16}$/ $\overline{CDDS16}$	O	MEMORY CHIP SELECT 16 BITS: In AT mode, this line is used to respond to the host to enable a 16-bit video memory data transfer. In Micro Channel mode, this line must be inverted to provide $\overline{CDDS16}$ for 16-bit video memory or I/O access.
15	IOCHRDY	O	READY: An active high output which signals to the system processor that a memory access is complete. This signal is used only to add wait states to the bus cycles during video memory accesses. It is pulled inactive by the WD90C20 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM. For further details, refer to the reference literature.
16	HBDIR	O	HIGH BYTE DIRECTION: This line is used to control the data direction of an external high byte data buffer if the external data buffer is necessary for the implementation. This line will be driven "LOW" only in memory READ or I/O READ cycles.

TABLE 4-1. PIN DEFINITIONS (Continued)

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
17	LBDIR	O	LOW BYTE DIRECTION: This line is used to control the data direction of an external low byte data buffer if the external data buffer is necessary for the implementation. This line will be driven "LOW" only in memory READ or I/OREAD cycles.
19 20 21 22 23 24 25 26 29 30 31 32 33 34 35 36	SD15 SD14 SD13 SD12 SD11 SD10 SD9 SD8 SD7 SD6 SD5 SD4 SD3 SD2 SD1 SD0	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	DATA BUS (SD15 - SD0): These bidirectional signals may either be connected directly to a local data bus requiring less than 8 ma. of source/sink, or may be connected through two external bus buffers.
38	$\overline{\text{MEMR}}$/ M/$\overline{\text{IO}}$	I	MEMORY READ: In AT mode, this signal is called $\overline{\text{SMEMR}}$ and is an active low memory read strobe. It is asserted in 8/16 bit memory read cycles. In Micro Channel mode, the signal is called M/$\overline{\text{IO}}$. It distinguishes between memory and I/O cycles. When (M/$\overline{\text{IO}}$) is high, a memory cycle is in process. A low on (M/$\overline{\text{IO}}$) shows that an I/O cycle is in process. For further details, refer to the reference literature.
39	$\overline{\text{MEMW}}$/ $\overline{\text{S0}}$	I	MEMORY WRITE: The active low memory write strobe in AT mode for 8/16 bit data transfers. In Micro Channel mode, it becomes $\overline{\text{S0}}$ and is the channel status signal which indicates the start and type of a channel cycle. Along with the $\overline{\text{S1}}$, M/$\overline{\text{IO}}$ and $\overline{\text{CMD}}$ signals, it is decoded to interpret I/O and memory commands. For further details, refer to the reference literature.
43	$\overline{\text{REFRESH}}$	I	REFRESH: This active low input pin is connected to the system $\overline{\text{REFRESH}}$ signal from the I/O bus.

TABLE 4-1. PIN DEFINITIONS (Continued)

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
40	$\overline{IOR}$/ $\overline{S1}$	I	I/O READ: Active low I/O read strobe in AT mode. It is asserted in 8/16 bit I/O read bus cycles. $\overline{S1}$ is the alternate mnemonic used in Micro Channel mode to indicate the start and type of a channel cycle. For further details, refer to the reference literature.
41	$\overline{IOW}$/ $\overline{CMD}$	I	I/O WRITE: Active low strobe. In AT mode, the strobe signals an I/O write for 8/16 bit I/O write cycles. In Micro Channel mode it is synonymous with $\overline{CMD}$; address bus validity is signaled by $\overline{CMD}$ going low while the rising edge of $\overline{CMD}$ indicates the end of a Micro Channel bus cycle. For further details, refer to the reference literature.
DISPLAY MEMORY INTERFACE			
55 52 51 50 49 48 47 46 45	MA8 MA7 MA6 MA5 MA4 MA3 MA2 MA1 MA0	O O O O O O O O O	MEMORY ADDRESS (MA0 - MA8): Display memory DRAM address.
56	$\overline{RAS10}$	O	ROW ADDRESS STROBE: Active low Memory Maps 1 & 0 RAS output signal.
57	$\overline{RAS32}$	O	ROW ADDRESS STROBE: Active low Memory Maps 3 & 2 RAS output signal.
58	$\overline{CAS10}$	O	COLUMN ADDRESS STROBE: Active low Memory Maps 1 & 0 CAS output signal.
59	$\overline{CAS32}$	O	COLUMN ADDRESS STROBE: Active low Memory Maps 3 & 2 CAS output signal.
60	$\overline{WE0}$	O	WRITE ENABLE: Active low Memory Map 0 DRAM write enable signal.
61	$\overline{WE1}$	O	WRITE ENABLE: Active low Memory Map 1 DRAM write enable signal.

TABLE 4-1. PIN DEFINITIONS (Continued)

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
62	$\overline{WE2}$	O	WRITE ENABLE: Active low, Memory Map 2 write enable signal.
63	$\overline{WE3}$	O	WRITE ENABLE: Active low, Memory Map 3 write enable signal.
64	$\overline{OE10}$	O	OUTPUT ENABLE: Active low, Memory Maps 1 & 0 output enable signal.
65	$\overline{OE32}$	O	OUTPUT ENABLE: Active low, Memory Maps 3 & 2 output enable signal.
			Lines MD15 – 0 are the data bus to the video display DRAMS. Data lines MD0-15 are pulled up or down with resistors to provide setup information on power-up (reset) as shown below.

Pin No.	Memory Data Line	Pin Type	Power-Up Function	Data Stored at Name	Port
68	MD15	I/O	EGA SW4 / LCD Select*	PR11(7)**	3?5.2A.7
69	MD14	I/O	EGA SW3	PR11(6)**	3?5.2A.6
70	MD13	I/O	EGA SW2	PR11(5)**	3?5.2A.5
71	MD12	I/O	EGA SW1	PR11(4)**	3?5.2A.4
72	MD11	I/O	ANALOG/TTL Display	PR5(3)**	3CF.0F.3
73	MD10	I/O	–	–	–
74	MD9	I/O	Panel Select Bit 1	PR18(1)**	3?5.31.1
75	MD8	I/O	Panel Select Bit 0	PR18(0)**	3?5.31.0
77	MD7	I/O	General Purpose	PR5(7)***	3CF.0F.7
78	MD6	I/O	General Purpose	PR5(6)***	3CF.0F.6
79	MD5	I/O	General Purpose	PR5(5)***	3CF.0F.5
80	MD4	I/O	General Purpose	PR5(4)***	3CF.0F.4
81	MD3	I/O	VCLK1,2 (I/O)	None**	–
82	MD2	I/O	AT/Micro Channel Mode	None**	–
83	MD1	I/O	BIOS ROM Data Width	PR1(1)***	3CF.0B.1
84	MD0	I/O	BIOS ROM Mapping	PR1(0)***	3CF.0B.0

TABLE 4-1. PIN DEFINITIONS (Continued)

NOTES:

*PR11(7) = 0 : mono LCD, PR11(7) = 1 : color LCD.
**Pullup resistor sets these bits to logic 1.
***Pulldown resistor sets these bits to logic 1.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
		MISCELLANEOUS	
44	$\overline{\text{PWRDN}}$	I	POWER DOWN SELECTED: This active low input signal is used to disable screen refresh cycle.
110	$\overline{\text{LCD}}$/CRT	O	LCD OR CRT SELECTED: This active high output is used to power down an external RAMDAC chip whenever the WD90C20 operates in LCD mode. "1" is CRT mode, and "0" is LCD mode.
		DISPLAY INTERFACE*	
86	PCLK	O	PIXEL CLOCK: This line is used to clock the video outputs into a RAMDAC in a CRT interface.
87	XSCLK	O	SHIFT CLOCK: In an LCD interface, this signal is used to shift the upper and lower panel's data into the X-driver. In a Plasma interface, this signal is also used as shift clock.
88	WGTCLK	O	WEIGHT CONTROL CLOCK: In an LCD interface, this signal is required to generate a gray scale in panels using pulse width modulation. In a Plasma interface, it is an "ENABLE VIDEO" signal.
89	LP/HSYNC	O	LATCH PULSE: In an LCD interface, this signal is used to latch all the data in the current scan line. In either a Plasma or a CRT interface, this signal is used for horizontal sync.
90	FP/VSYNC	O	FRAME PULSE: This signal is used to indicate the start of scanning to the Y-driver in an LCD interface. In either a Plasma or a CRT interface, this signal is used for vertical sync.
91	FR/BLANK	O	FRAME CONTROL: In an LCD interface, it is an AC signal which is toggled every frame. In a CRT interface, it is the $\overline{\text{BLANK}}$ signal. Some panels call this signal "M."
103 102 101 100	LD3 LD2 LD1 LD0	O O O O	LOWER PANEL DATA BIT 3 to BIT 0: In an LCD interface, these signals are used for the lower panel data bus. In a Plasma interface, they are reserved. In a CRT interface, they are the lower four bits pixel video outputs to the RAMDAC.

TABLE 4-1. PIN DEFINITIONS (Continued)

*The display interface functions are redefined for each display mode – see Table 2-1 on page 4 for details.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
107 106 105 104	UD3 UD2 UD1 UD0	O O O O	UPPER PANEL DATA BIT 3 to BIT 0: In an LCD interface, these signals are used for the upper panel data bus. In a Plasma interface, they provide the pure 4-bit video data interface. In a CRT interface, they are the upper four bits pixel video outputs to the RAMDAC.
RAMDAC INTERFACE			
92	$\overline{\text{RPLT}}$	O	READ PALETTE: Video DAC register and color palette read signal. Active low during an I/O read of addresses 3C6H, 3C8H, and 3C9H. This line is active in both internal and external RAMDAC configurations.
93	WPLT/VD9	O	WRITE PALETTE: Video DAC register and color palette write signal. Active low during an I/O write to addresses 3C6H-3C9H. This line is active in both internal and external RAMDAC configurations. VIDEO DATA BIT 9: In color TFT mode, this is the ninth data bit of the LCD interface.
111	VREF	I	VOLTAGE REFERENCE INPUT: An external voltage reference of 1.2V is connected to this input for normal operation of the internal RAMDAC. Grounding this pin changes the function of pin 112 and disables the internal RAMDAC so that the WD90C20 can be used with an external RAMDAC.
112	MDETECT/ FSADJUST	I I	MONITOR DETECT: When pin 111 is grounded, this pin is used as a monitor detect input. The result of this input is read from 3C2H bit 4. FULL SCALE ADJUST: A resistor on this pin sets the full scale output current of the RED, GREEN, and BLUE DAC's.
114	BLUE	I/O	BLUE CURRENT OUTPUT: High impedance current source can directly drive a doubly-terminated 75-Ohm coaxial cable.
115	GREEN	I/O	GREEN CURRENT OUTPUT: High impedance current source can directly drive a doubly-terminated 75-Ohm coaxial cable.
116	RED	I/O	RED CURRENT OUTPUT: High impedance current source can directly drive a doubly-terminated 75-Ohm coaxial cable.

TABLE 4-1. PIN DEFINITIONS (Continued)

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
POWER AND GROUND			
9,28, 53,67, 94	Vcc	-	Power
10,18 27, 37, 54, 66, 76,85, 95	GND	-	Ground
123 113	AVcc AGND	- -	+ 5VDC - ANALOG (See Figure 4-2) Ground - ANALOG (See Figure 4-2)
108 109	RVcc RGND	- -	RAMDAC power (See Figure 4-2) RAMDAC ground (See Figure 4-2)

TABLE 4-1. PIN DEFINITIONS (Continued)

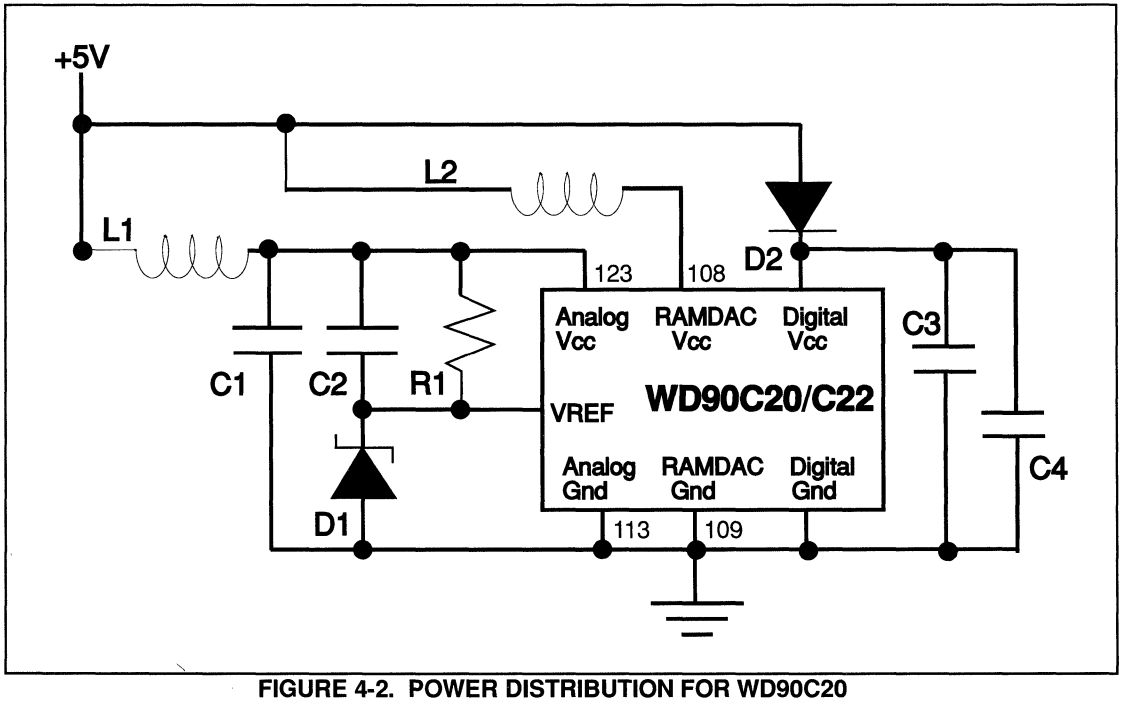


FIGURE 4-2. POWER DISTRIBUTION FOR WD90C20

5.0 WD90C20 REGISTERS

All standard IBM registers incorporated in the WD90C20 are functionally equivalent to the VGA implementation, while additional PR registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards using the 6845 CRT Controller. This section describes the VGA registers (and the differences between VGA and EGA), as well as the PR registers.

5.1 VGA REGISTERS SUMMARY

REGISTERS	RW	MONO	COLOR	EITHER
GENERAL REGISTERS				
Miscellaneous Output Reg	W			3C2
	R			3CC
Input Status Reg 0	RO			3C2
Input Status Reg 1	RO	3BA	3DA	
Feature Control Reg	W	3BA	3DA	
	R			3CA
*Video Subsystem Enable	RW			3C3
NOTE: *Video Subsystem Enable Register 3C3H needs to be implemented externally in a Micro Channel configuration.				
SEQUENCER REGISTERS				
Sequencer Index Reg	RW			3C4
Sequencer Data Reg	RW			3C5
CRT CONTROLLER REGISTERS				
Index Reg	RW	3B4	3D4	
CRT Controller Data Reg	RW	3B5	3D5	
GRAPHICS CONTROLLER REGISTERS				
Index Reg	RW			3CE
Other Graphics Reg	RW			3CF
ATTRIBUTE CONTROLLER REGISTERS				
Index Reg	RW			3C0
Attribute Controller Data Reg	W			3C0
	R			3C1
VIDEO DAC PALETTE REGISTERS				
Write Address	RW			3C8
Red Address	W			3C7
DAC State	R			3C7
Data	RW			3C9
Pel Mask	RW			3C6

TABLE 5-1. VGA REGISTERS SUMMARY

5.2 COMPATIBILITY REGISTERS

FUNCTIONS	RW[1]	MDA[2]	CGA[2]	AT&T[2]	HERCULES[2]
Mode Control Reg	WO	3B8	3D8	3D8	3B8
Color Select Reg	WO		3D9	3D9	
Status Reg	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Reg	WO			3DE	
Hercules Reg	WO				3BF
CRTC[3]	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

TABLE 5-2. COMPATIBILITY REGISTERS SUMMARY

NOTES:

1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. 6845 Mode Registers.

5.3 VGA REGISTERS

This section describes the VGA registers.

5.4 GENERAL REGISTERS

NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES:

1. Reserved bits should be set to zero.

2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes

   1 = D in Color Modes

5.4.1 Miscellaneous Output Register, Read Port = 3CC, Write Port = 3C2

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.
0= Positive vertical sync polarity.
1= Negative vertical sync polarity.

Bit 6 *

Horizontal Sync Polarity Selection.
0= Positive horizontal sync polarity.
1= Negative horizontal sync polarity.

NOTE:

*These bits determine the vertical size of the vertical frame by the monitor. Their encoding is shown below:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.
When in modes 0-5, one memory page is selected from the two 64KB pages.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bit(3:2) Clock Select 1,0.

BIT 3	BIT 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

Bit 1

System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection. Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0= CRTC and status addresses for MDA mode (3BX).
1= CRTC and status addresses for CGA mode (3DX).

5.4.2 Input Status Register 0, Read Only Port = 3C2

BIT	FUNCTION
7	CRT Interrupt
6, 5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3: 0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit(6:5)

Reserved in VGA.

Bit 4

The DAC output currents, I_{RED}, I_{GREEN}, and I_{BLUE}, develop a voltage across the load resistances R_{LD}. These voltages are sent to comparitors against a voltage derived from the external voltage reference V_{REF}. The output current is determined by the formula:

$$I = \frac{\text{code x .04}}{R_{SET}} \times V_{REF}$$

where the codes range from 0 to 63 (0H to 3FH) for a 6-bit DAC.

The output signal, MDETECT, is readable at port 3C2H bit 4. It is important that this output signal be read during active video ouput, not during retrace or any other blanking period.

Bit(3:0)

Reserved.

5.4.3 Input Status Register 1, Read Only Port = 3?A

BIT	FUNCTION
7, 6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved
0	Display Enable

Bit(7:6)

Reserved.

Bit(5:4)

Color Plane Diagnostics.
These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.
0= Vertical frame is displayed.
1= Vertical retrace is active.

Bit(2:1)

Reserved.

Bit 0

Display Enable Status.
0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

5.4.4 Feature Control Register, Read Port = 3CA, Write Port = 3?A

BIT	FUNCTION
7 - 4	Reserved
3	Vertical Sync Control
2 - 0	Reserved

Bits(7:4)

Reserved

Bit 3

Vertical Sync Control:
0: Vsync output enabled.
1: Vsync output is logical "OR" of Vsync and Vertical Display Enable.

Bit(2:0)

Reserved

5.5 SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE: Reserved bits should be set to zero.

5.5.1 Sequencer Index Register, Read/Write Port = 3C4

BIT	FUNCTION
7 - 3	Reserved
2 - 0	Sequencer Address/Index Bits

Bit(7:3)

Reserved.

Bit(2:0)

Sequencer Address/Index.
The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer register to be accessed.

5.5.2 Reset Register, Read/Write Port = 3C5, Index = 00

BIT	FUNCTION
7 - 2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bit(7:2)

Reserved.

Bit 1

Synchronous Reset.
0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0

Asynchronous Reset.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

5.5.3 Clocking Mode Register, Read/Write Port = 3C5, Index = 01

BIT	FUNCTION
7, 6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bit(7:6)

Reserved.

Bit 5

Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character or every other character clock depending on bit 2.
1 = Serial shift registers loaded every 4th character clock (32 bit fetches).

Bit 3

Dot Clock Selection.
0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360 pixels wide).

Bit 2

Shift Load. Effective only if bit 4=0.
0 = Video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.
Commands Sequencer to generate 8 or 9 dot wide character clock.
0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

5.5.4 Map Mask Register, Read/Write Port = 3C5, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bit(7:4)

Reserved.

Bit(3:0)

Controls Writing To Memory Maps (0-3), respectively.
0 = Writing to maps (0-3) disallowed.
1 = Maps (0-3) accessible.

5.5.5 Character Map Select Register Read/Write Port = 3C5, Index = 03

BIT	FUNCTION
7, 6	Reserved
5	Character Map Select A Bit 2
4	Character Map Select B Bit 2
3	Character Map Select A Bit 1
2	Character Map Select A Bit 0
1	Character Map Select B Bit 1
0	Character Map Select B Bit 0

If Sequencer Register 4 bit 1 is 1, then the attribute byte bit 3 in text modes is redefined to control switching between character sets. "0" selects character map B. "1" selects character map A. Character Map selection from either plane 2 or plane 3 is determined by PR2(2), PR2(5), and bit 4 of the attribute code.

Bit(7:6)

Reserved.

Bit 5

Character Map A MSB Select.
The Most Significant Bit (MSB) of character map A, along with bits 3 and 2, select the location of character map A as shown below.

BITS 5 3 2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit 4

Character Map B MSB Select.
The MSB of character map B, along with bits 1 and 0, select the location of character map B as shown below.

BITS 4 1 0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit(3:2)

Character Map Select A.
Refer to bit 5 table.

Bit(1:0)

Character Map Select B.
Refer to bit 4 table.

5.5.6 Memory Mode Register, Read/Write Port = 3C5, Index = 04

BIT	FUNCTION
7 - 4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bit(7:4)

Reserved.

Bit 3

Chains 4 Maps.
0 = Processor sequentially accesses data using map mask register.
1 = Directs the two lower order video memory address pins (MA0,MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.
0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.
1 = Sequential processor access as defined by map mask register.

Bit 1

Extended Video Memory.
0 = 64 KB of video memory.
1 = Greater than 64KB of memory for VGA/EGA modes.

Bit 0

Reserved.

5.6 CRT CONTROLLER REGISTERS

PORT[1]	INDEX	VGA REGISTER NAME	6845 REG NAME[2]
3?4	---	CRT Controller Address Reg.	CRTC Address Reg
3?5	00	Horizontal Total	Hor. Total
3?5	01	Horizontal Display Enable End	Hor. Disp
3?5	02	Start Horizontal Blanking	See note 3.
3?5	03	End Horizontal Blanking	See note 3.
3?5	04	Start Horizontal Retrace	See note 3.
3?5	05	End Horizontal Retrace	See note 3.
3?5	06	Vertical Total	Vert. Disp.
3?5	07	Overflow	See note 3.
3?5	08	Preset Row Scan	See note 3.
3?5	09	Maximum Scan Line/Others	Max. Scan Line Add.
3?5	0A	Cursor Start	Cursor Start
3?5	0B	Cursor End	Cursor End
3?5	0C	Start Address High	Start Add. High
3?5	0D	Start Address Low	Start Add. Low
3?5	0E	Cursor Location High	Cursor Loc. High
3?5	0F	Cursor Location Low	Cursor Loc. Low
3?5	10	Vertical Retrace Start	Light Pen High Read
3?5	11	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	
3?5	13	Offset	See note 3.
3?5	14	Underline Location	See note 3.
3?5	15	Start Vertical Blank	See note 3.
3?5	16	End Vertical Blank	See note 3.
3?5	17	CRTC Mode Control	See note 3.
3?5	18	Line Compare	See note 3.

TABLE 5-3. CRT CONTROLLER REGISTERS

NOTES:

1. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
?=B in monochrome modes.
?=D in color modes.

2. 6845 Mode Registers are defined and explained in greater in the reference literature.

3. This register can be programmed in VGA mode only. It is not applicable in 6845 mode.

4. Reserved bits should be set to zero.

5.6.1 CRT Address Register, Read/Write Port = 3?4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Index bits

Bit(7:5)

Reserved.

Bit(4:0)

Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed hex.

5.6.2 Horizontal Total Register, Read/Write Port = 3?5, Index=00H

BIT	FUNCTION
7 - 0	Horizontal Total Period

Bit(7:0)

Count Plus Retrace Less 5.

In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line.

5.6.3 Horizontal Display Enable End Register Read/Write Port = 3?5, Index 01H

BIT	FUNCTION
7 - 0	Displayed Characters per scan line

Bit(7:0)

Horizontal blanking begins when the horizontal character counter reaches this character clock value.

5.6.4 Start Horizontal Blanking Register, Read/Write Port = 3?5, Index = 03H

BIT	FUNCTION
7 - 0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches this character clock value. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

5.6.5 End Horizontal Blanking Read/Write Port = 3?5, Index = 03H

BIT	FUNCTION
7	Reserved
6, 5	Display Enable Signal Skew Control
4 - 0	End Horizontal Blanking (lower 5 bits)

This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

Bit 7

Reserved

Bit(6:5)

Display Enable Signal Skew Control.
These bits define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

BIT 6	BIT 5	SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

End Horizontal Signal Width.
End Horizontal Blank signal width "W" is determined as the value of start blanking register plus "W" in character clocks. The least significant five bits are programmed in this register, while the most significant bit is the End Horizontal Retrace Register (Index 05H) bit 7.

5.6.6 Start Horizontal Retrace Pulse Register, Read/Write Port = 3?5, Index = 04H

BIT	FUNCTION
7 - 0	Start Horizontal Retrace Character Count

Bit(7:0)

Start Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

5.6.7 End Horizontal Retrace Register, Read/Write Port = 3?5, Index = 05H

BIT	FUNCTION
7	End Horizontal Blank bit 6
6, 5	Horizontal Retrace Delay
4 - 0	End Horizontal Retrace

This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

Bit 7

MSB (Sixth Bit) Of End Horizontal Blanking Register.

Bit(6:5)

Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

BIT 6	BIT 5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

Bit(4:0)

End Horizontal Retrace Pulse Width "W".
Start retrace register value is added to the character count for width "W". The least significant five bits are programmed in this register. When the Start Horizontal Retrace Register value matches these five bits, the horizontal retrace signal is turned off.

5.6.8 Vertical Total Register, Read/Write Port = 3?5,Index = 06H

Bit(7:0)

Raster Scan Line Total Less 2.
The least significant eight bits of a ten bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync are also included. The ninth and tenth bits of this count are loaded into the Vertical Overflow Register (index = 07H) bit 0 and bit 5, respectively. In 6845 modes, total vertical display time in rows is programmed into bit 6 – bit 0, while bit 7 is reserved. Scan count reduction is not necessary. The number of scan lines in a row is determined by the maximum Scan Line Register (index 09H bits 0 through 4). This register is locked if the PR Register PR3 (0) = 1 or the Vertical Retrace End Register bit 7 = 1.

5.6.9 Overflow Vertical Register Read/Write Port = 3?5, Index = 07H

BIT	FUNCTION
7	Vert. Ret. Start Bit 9
6	Vert. Display Enable End Bit 9
5	Vert. Total Bit 9
4	Line Compare Bit 8
3	Start Vert. Blank Bit 8
2	Vert. Ret. Start Bit 8
1	Vert. Display Enable End Bit 8
0	Vert. Total Bit 8

++Bit 7

Vertical Retrace Start Bit 9 (index = 10H).

****Bit 6**

Vertical Display Enable End Bit 9 (index = 12H).

++Bit 5

Vertical Total Bit 9 (index = 06H).

Bit 4

Line Compare Bit 8 (index = 18H).

++Bit 3

Start Vertical Blank Bit 8 (index =15H).

++Bit 2

Vertical Retrace Start Bit 8 (index = 10H).

****Bit 1**

Vertical Display Enable End Bit 8 (index = 12H).

++Bit 0

Vertical Total Bit 8 (index = 06H).

NOTES:

+ This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

** This register is locked if the PR Register PR3(1)=0 AND the Vertical Retrace End Register bit 7 = 1.

++ This register is locked if the PR Register PR3(0) = 1 OR the Vertical Retrace End Register bit 7 = 1.

5.6.10 Preset Row Scan Register, Read/Write Port = 3?5, Index = 08H

BIT	FUNCTION
7	Reserved
6, 5	Byte Panning Control
4 - 0	Preset Row Scan Count

Bit 7

Reserved.

Bit(6:5)

Byte Panning Control.
These bits allow up to 3 bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 byte left shift
1	0	2 bytes left shift
1	1	3 bytes left shift

Bit(4:0)

Preset Row Scan Count.
These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

5.6.11 Maximum Scan Line Register, Read/Write Port=3?5, Index=09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare bit 9
5	Start Vertical Blank bit 9
4 - 0	Maximum Scan Line

Bit 7

200 to 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.
This is bit 9 of the Line Compare Register (index = 18H).

Bit 5

Start Vertical Blank.
This is bit 9 of the Start Vertical Blank Register (index = 15H). This register is locked if the PR Register PR3 (0) = 1.

Bit(4:0)

Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, bits 5-7 are reserved, and bits 4-0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported.

5.6.12 Cursor Start Register, Read/Write Port = 3?5, Index = 0AH

BIT	FUNCTION
7, 6	Reserved
5	Cursor Control
4 - 0	Cursor Start Scan Line

Bit(7:6)

Reserved.

Bit 5

Cursor Control.
0=Cursor on.
1=Cursor off.

Bit(4:0)

These bits specify the row scan counter value within the character box where the cursor begins. They contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0BH), no cursor is generated. For 6845 modes, bit 7 is reserved. Bit 5 controls the cursor operation and bits 4-0 contain the cursor start value. Bit 6 is not used.

5.6.13 Cursor End Register, Read/Write, Port = 3?5h, Index = 0BH

BIT	FUNCTION
7	Reserved
6, 5	Cursor Skew
4 - 0	Cursor End Scan Line

Bit 7

Reserved.

Bit(6:5)

Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks –e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the table below.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

These bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, bits 7-5 are reserved and bits 4-0 contain the row value of the cursor end.

NOTE: There are three types of cursors generated, depending upon the mode, i.e, EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

5.6.14 Start Address High Register Read/Write Port 3?5H, Index = 0CH

BIT	FUNCTION
7 - 0	Start Address High Byte

Bit(7:0)

Display Screen Start Address Upper Byte Bits. Eight high order bits of the 16 bit video memory address used for screen refresh. The low order eight bit register is at index 0DH. The PR Register PR3 bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes bits 6 and 7 are forced to "0" regardless of this register's contents, while the lower order 8 bits are at index register 0DH.

5.6.15 Start Address Low Register Read/Write Port = 3?5H, Index = 0DH

BIT	FUNCTION
7 - 0	Start Address Low Byte

Bit(7:0)

The lower order eight bits of the 16 bit video memory address in VGA or 6845 modes.

5.6.16 Cursor Location High Register Read/Write Port = 3?5h, Index = 0Eh

BIT	FUNCTION
7 - 0	Cursor Location High Byte

Bit(7:0)

Cursor Address Upper Byte Bits.
The eight higher order bits of 16 bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0FH. In VGA mode, the PR Register PR3 bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, bits 6 and 7 are reserved, while bits 5 - 0 are the high order bits of the cursor.

5.6.17 Cursor Location Low Register Read/Write Port = 3?5, Index = 0FH

BIT	FUNCTION
7 - 0	Cursor Location Low Byte

Bit(7:0)

Cursor Address Lower Byte Bits.
The lower order eight bits of the 16 bit video memory address in VGA or 6845 mode.

5.6.18 Vertical Retrace Start Register Read/Write Port = 3?5, Index=10H

BIT	FUNCTION
7 - 0	Vertical Retrace Start (Lower eight bits)

Bit(7:0)

Vertical Retrace Start Pulse Lower Eight Bits. The lower eight bits of the ten bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07H). In 6845 compatible mode, this register shows the high order six bits in positions 5 – 0 as the light pen read back value, and bits 6 an 7 are reserved. The lower order eight bits of the light pen read back register are at the index 11H. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3 (0) = 1.

5.6.19 Vertical Retrace End Register Read/Write Port = 3?5, Index = 11H

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3 - 0	Vertical Retrace End

This register is locked if the PR Register PR3(0)=1.

Bit 7

CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller index registers in the range of index 00H-07H. The line compare bit 4 in the Overflow Register (07H) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.
Selects DRAM refresh cycles per horizontal scan line.
0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.
0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4

Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by resetting (writing a 0 to) and internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

Bit(3:0)

Vertical Retrace End.
These bits specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan counter for "W" to the value of the Vertical Retrace Start Register. The 4 bit result is written in the Vertical Retrace End Register.

5.6.20 Vertical Display Enable End Register Read/Write Port = 3?5, Index = 12H

BIT	FUNCTION
7 - 0	Vertical Display Enable End (Lower eight bits)

Bit(7:0)

Vertical Display Enable End Lower Eight Bits.
The eight lower bits of ten bit register that defines where the active display frame ends.
The programmed count is in scan lines minus 1.
Bits 8 and 9 are in the Overflow Register (index 07H) at positions 1 and 6, respectively.

5.6.21 Offset Register Read/Write Port = 3?5, Index = 13H

BIT	FUNCTION
7 - 0	Logical Line Screen width

Bit(7:0)

Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:

Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K=2 in byte mode and K=4 in word mode.

5.6.22 Underline Location Register read/write Port = 3?5, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4 - 0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5

Count By 4 For Double Word Access
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit(4:0)

Underline Location.
These bits specify the row scan counter value within a character matrix where under line is to be displayed. Load a value 1 less than the desired scan line number.

5.6.23 Start Vertical Blank Register Read/Write Port = 3?5, Index =15H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	Start Vertical Blank (Lower eight bits)

Bit(7:0)

Start Vertical Blank Lower Eight Bits.
The lower eight bits of the ten bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). The ten bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

5.6.24 End Vertical Blank Register read/write Port=3?5, Index=16H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	End Vertical Blank

Bit(7:0)

Vertical Blank inactive Count. End Vertical Blank is an 8 bit value calculated as follows:

8 Bit End Vertical Blank value =
(value of Start Vertical Blank minus 1) + (value of Vertical Blank signal width in scan lines).

5.6.25 CRT Mode Control Register Read/Write Port = 3?5, Index = 17H

This register is locked if PR Register PR3(5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.
0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word Or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by 1 bit and the MSB of the address counter appears on the LSB. See the table below.
1 = Byte address mode.

MEMORY ADDRESS	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLEWORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE:
* See bit 5, defining address wrap. This table is applicable only when PR Register PR1 bits 7 and 6 equal zero, or PR16 bit 1 equals one.

The CRT Underline Location Register (index = 14H) bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) bit 6 controls addressing. See the table below:

CRT14H	CRT17H	ADDRESS
Bit 6	Bit 6	Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.
0 = In word address mode, this bit enables bit 13 to appear at MA0, otherwise bit 0 appears on MAO.
1 = Select MA15 for odd/even mode when 256KB of video memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2
0 = Character clock increments memory address counter.
1 = Character clock divided by 2 increments the address counter.

Bit 2

Horizontal Retrace Clock Rate Select For Vertical Timing Counter.
0 = Selects horizontal retrace clock rate.
1 = Selects horizontal retrace clock rate divided by 2.

Bit 1

Select Row Scan Counter.
0 = Selects row scan counter bit 1 as output at MA14 address pin.
1 = Selects bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0

6845 CRT Controller compatibility mode support for CGA operation.
0 = Row scan address bit 0 is substituted for memory address bit 13 at MA13 output pin during active display time.
1 = Enable memory address pin 13 to be output at MA13 address pin.

5.6.26 Line Compare Register Read/Write Port = 3?5, Index = 18H

BIT	FUNCTION
7 - 0	Line Compare (lower eight bits)

Bit(7:0)

Line Compare Lower Eight Bits.
Lower eight bits of the ten bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared.

5.7 GRAPHICS CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

NOTE:
1. Reserved bits should be set to zero.

5.7.1 Graphics Index Register, Read/ Write Port = 3CE

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Graphics Address Bits

Bit(7:4)

Reserved.

Bit(3:0)

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

5.7.2 Set/Reset Register, Read/Write Port 3CF, Index = 00

BIT	FUNCTION
7 - 4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined below:

0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE:
*The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05H) bit 1 and bit 0.

5.7.3 Enable Set/Reset Register, Read/Write Port = 3CF, Index = 01

BIT	FUNCTION
7 - 4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Enable Set/Reset Register (Index 00H).

0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00H) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.

1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00H), and the respective memory map is written with the Set/Reset Register value.

5.7.4 Color Compare Register, Read/Write PORT 3CF, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Color Compare.
The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a "1" is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05H), data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

5.7.5 Data Rotate Register, Read/Write Port = 3CF, Index = 03

BIT	FUNCTION
7 - 5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count 2 Bit 2
1	Rotate Count 1 Bit 1
0	Rotate Count 0 Bit 0

Bit(7:5)

Reserved.

Bit(4:3)

Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05H) is defined as follows.

BIT 4	BIT 3	FUNCTION
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches

Bit(2:0)

Rotate Count.
This specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05H).

5.7.6 Read Map Select Register, Read/Write Port = 3CF, Index = 04

BIT	FUNCTION
7 - 2	Reserved
1	Map Select 1
0	Map Select 0

Bit(7:2)

Reserved.

Bit(1:0)

Map Select.
These bits select memory map in system read operations. This operation has no effect on color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained maps 0 and 1 or value 10b or 11 to select the chained maps 2 and 3. Map read is defined as shown below.

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

5.7.7 Graphics Mode Register, Read/Write Port = 3CF, Index = 05

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7

Reserved.

Bit 6

256 Color Mode.
0 = Enables bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to six bits through internal palette and is sent out on the lower six bit pins (VID5 - VID0) every dot clock. The remaining two video outputs (VID6, VID7) are determined by bits 2 and 3 of the Color Select Register located at index = 14H within the Attribute Controller.
1 = Load video shift registers to support 256 color mode.

Bit 5

Shift Register.
Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.
0 = Map 0 – Map 3 data is placed into shift registers for normal operations.
1 = For CGA graphics mode compatibility, even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.
0 = normal
1 = CGA compatible odd/even system access mode. Sequential addressing as defined by bit 2 of the memory mode register (index = 04H) in the Sequencer Register. Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3

Read Mode.
0 = System reads data from memory maps selected by Read Map Select Register (index 04H). This setting will have no effect if bit 3 of the Sequencer Memory Mode Register = 1.
1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved.

Bit(1:0)

Write Mode.
The following table defines the four write modes.

BIT 0	BIT 1	WRITE MODE
0	0	Write Mode 0. If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	Write Mode 1. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	Write Mode 2. Memory maps (3:0) are filled with the 8-bit value of the corresponding CPU data bits (3:0). The 32 bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	Write Mode 3. Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

5.7.8 Miscellaneous Register, Read/Write Port = 3CF, Index = 06

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bit(7:4)

Reserved.

Bit(3:2)

Memory Map 1, 0
Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0H-BFFF:FH	128KB
0	1	A000:0H-AFFF:FH	64KB
1	0	B000:0H-B7FF:FH	32KB
1	1	B800:0H-BFFF:FH	32KB

Bit 1

Odd/Even Mode.
0 = CPU address bit A0 is the memory address bit MA0.
1 = CPU address bit A0 is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode.
This bit is programmed the same way as bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selects.
1 = Graphics mode selected.

5.7.9 Color Don't Care Register, Read/Write Port 3CF, Index = 07

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Memory Map Color Compare Operation.
0 = Disable color compare operation.
1 = Enable color compare operation.

5.7.10 Bit Mask Register, Read/Write Port = 3CF, Index = 08

BIT	FUNCTION
7 - 0	Bit Mask

Bit(7:0)

The bit mask operation applies simultaneously to all four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation affects any data written by the processor.

0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

5.8 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CO	——	Index Register
3CO	00-0F	Palette Registers
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

NOTES:
1. Each attribute data register is written at 3C0 and register data is read from address 3C1.
2. Reserved bits should be set to zero.
3. ? " Value is controlled by Bit 0 of the Miscellaneous Output register and is programmed as shown below.

0 = B in Monochrome Modes and
1 = D in Color Modes

5.8.1 Attribute Index Register, Read/Write Port = 3C0

BIT	FUNCTION
7 - 6	Reserved
5	Palette Address Source
4 - 0	Attribute Address Bits

Bit(7:6)

Reserved.

Bit 5

Palette Address Source.
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 - 0FH).
1 = Enable internal color palette and normal video translation.

Bit(4:0)

Attribute Controller Index Register Address Bits

NOTE:
The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 3?A) clears the flip-flop and selects the Address Register, which is read through address 3C1 and written at address 3C0. Once the Address Register has been loaded with an index, the next write operation to 3C0 will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address 3C0, but does not toggle for reads to address 3C1.

5.8.2 Palette Registers (00-0F Hex), Read Port 3C1/Write Port 3C0

BIT	FUNCTION
7 - 6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:6)

Reserved.

Bit(5:0)

Palette Pixel Colors.
They are defined as follows:
0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the table below.

Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

5.8.3 Attribute Mode Control Register Read Port 3C1/Write Port 3C0, Index = 10

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7

VID5, VID4 Select.
0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14H) bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6

Pixel Width.
0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.
1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility.
Line Compare in the CRT Controller.
0 = A Line compare will have no effect on the PEL Panning Register.
1 = Allows a successful line compare to disable the PEL Panning Register and also bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4

Reserved.

Bit 3

Background Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code.
Set this bit to zero for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes

Bit 0

Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

5.8.4 Overscan Color Register Read Port 3C1/Write Port 3C0, Index = 11

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:0)

Overscan/Border Color.

These bits determine the overscan or border color. For monochrome display, this register is set to 0. Border colors are set as shown above.

5.8.5 Color Plane Enable Register Read Port 3C1/Write Port 3C0, Index = 12

BIT	FUNCTION
7 - 6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3 - 0	Enable Color Plane

Bit(7:6)

Reserved.

Bit(5:4)

Video Status Control.
These bits select 2 out of 8 color outputs which can be read by the Input Status Register 1 (port = 03?A) bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit(3:0)

Color Plane Enable.
0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

5.8.6 Horizontal Pel Panning Register Read Port 3C1/Write Port 3C0, Index = 13

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Horizontal PEL Panning

Bit(7:4)

Reserved.

Bit(3:0)

Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to 3 position pixel shift can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Character	8 dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

5.8.7 Color Select Register Read Port 3C1/Write Port 3CO, Index = 14

BIT	FUNCTION
7 - 4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bit(7:4)

Reserved.

Bit(3:2)

Color Value MSB.
Two most two significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6

Bit(1:0)

Substituted Color Value Bits.
These bits can be substituted for VID5 and VID4 output by the Attribute Controller palette registers to create eight bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10H).

5.9 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting PR Register PR2(6) = 1.

2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting PR Register PR2(7) = 1.

3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0 = B in Monochrome Modes
1 = D in Color Modes

5.9.1 Hercules/MDA Mode Control Register, MDA Operation Write Only Port = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode. If Bit 1=1 and Port 3BFH bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5

Enable Blink.
0 = Disable Blinking.
1 = Enable Blinking.

Bit 4

Reserved.

Bit 3

Video enable.
0 = Video disable.
1 = Video activated.

Bit 2

Reserved.

Bit 1

Port 3BFH enable.
0 = Prevents setting of Port 3BF bit 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFh bit 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode. Should be 1.
0 = High resolution disabled.
1 = High resolution is enabled.

5.9.2 Hercules Registers

The Hercules Mode Register is a 2-bit write only register located at I/O port address 3BF. It affects the device operation only in the 6845 mode. The enable mode register located at the address 3B8 overrides the write port 3BF functions defined by its bits 0 and 1.

5.9.3 Enable Mode Register 3B8

BIT	FUNCTION
7	Display Memory Page Address Graphics Mode
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BF Bit 0 Override
0	High Resolution Mode = 1

Bit 7

Display Memory Page Address In Graphics Mode.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit (6:2,0)

Not Applicable.

Bit 1

Port 3BF Bit 0 Override.
0 = Prevents setting of Port 3BF bit 0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BF bit 0 to switch for the alpha or graphics mode selection.

5.9.4 Hercules Compatibility Register Write Only Port = 3BFH

BIT	FUNCTION
7 - 2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)

Reserved.

Bit 1

Upper Memory Page Address.
Enable Mode Control Register (3B8) bit 7 selects the displayed memory page address in the graphics mode. When it is reset, bit 1 prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.
0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics.
Allows the Enable Mode Register (3B8) bit 1 to override.
0 = Alpha mode display.
1 = Graphics modes may be displayed.

5.9.5 Color CGA Operation Register, Write Only Port = 3D8

BIT	FUNCTION
7, 6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bit (7:6)

Reserved.

Bit 5

Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4

B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3

Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = B/W mode enabled.

Bit 1

Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = graphics mode (320 by 200) activated.

Bit 0

(40 by 25) or (80 by 25) Text Mode Selection.
0 = 40 by 25 alpha mode enabled.
1 = 80 by 25 alpha mode activated.

5.9.6 CGA Color Select Register Write Only Port = 3D9

BIT	FUNCTION
7, 6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bit (7:6)

Reserved.

Bit 5

320 by 200 Color Set Select for the CGA 2 bits per pixel.
0 = Background, green, red, brown colors.
1 = Background, cyan, magenta, white colors.

Bit 4

Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = enable alternate color set in graphics mode.

Bit 3

Border Intensity.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 1

Green Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

Bit 0

Blue Border/Background.
border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Select blue background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

5.9.7 CRT Status Register MDA Operation, Read Only Port = 3BA

BIT	FUNCTION
7	VSYNC Inactive
6 - 4	Reserved
3	B/W Video Enabled
2 - 1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.
0 = Indicates the raster is in vertical retrace mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bit (6:4)

Reserved.

Bit 3

B/W Video Status.
0 = B/W Video disabled.
1 = B/W Video enabled.

Bit 2 - Bit 1

Reserved.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

5.9.8 CRT Status Register CGA Operation, Read Only Port = 3DA

BIT	FUNCTION
7 - 4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bit (7:4)

Reserved.

Bit 3

Vertical Retrace.
0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode.

Bit 2

Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open.

Bit 1

Light Pen Latch.
0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking active; Display Enable is inactive.

5.9.9 AT&T/M24 Register, Write Only Port = 3DE

This is a write only, 8-bit register located at address 3DE. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting bit 7 in PR Register 2 (PR2).

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5, 4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in-color text modes.
1 = Underline attribute selects white underlined foreground.

Bit (5:4)

Reserved.

Bit 3

Page Select.
Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B800:0H (16 KB length).
1 = Display memory address starts at BC00:0H (16 KB length).

Bit 2

Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or Non-IBM Graphics Mode. 400 line mode. A 400 line monitor is required for this mode.
0 = 200 line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400 line graphics.

5.10 WD90C20 PR REGISTERS

NAME PR REGISTER INDEX	RW [1]	DESIGNATION[2]	I/O LOCATION[3]	SECTION
Address Offset A	RW	PR0A(6:0)	3CF.09	5.11.1
Alternate Address Offset B	RW	PR0B(6:0)	3CF.0A	5.11.1
Memory Size	RW	PR1(7:0)	3CF.0B	5.11.2
Video Select	RW	PR2(7:0)	3CF.0C	5.11.3
CRT Control and Group Locking	RW	PR3(7:0)	3CF.0D	5.11.4
Video Control	RW	PR4(7:0)	3CF.0E	5.11.5
Unlock PRO-PR4	RW	PR5(7:0)	3CF.0F	5.11.6
Unlock PR11 - PR17	RW	PR10(7:0)	3?5.29[4]	5.11.7
EGA Switches	RW	PR11(7:0)	3?5.2A	5.11.8
Scratch Pad	RW	PR12(7:0)	3?5.2B	5.11.9
Interlace H/2 Start	RW	PR13(7:0)	3?5.2C	5.11.10
Interlace H/2 End	RW	PR14(7:0)	3?5.2D	5.11.11
Miscellaneous Control 1	RW	PR15(7:0)	3?5.2E	5.11.12
Miscellaneous Control 2	RW	PR16(7:0)	3?5.2F	5.11.13
Miscellaneous Control 3	RW	PR17(0)	3?5.30	5.11.14
Flat Panel Status	RO[5]	PR18(1:0)	3?5.31	5.11.15
Flat Panel Control I	RW	PR19(7:0)	3?5.32	5.11.16
Flat Panel Control II	RW	PR1A(7:0)	3?5.33	5.11.17
Flat Panel Unlock	WO	PR1B(7:0)	3?5.34	5.11.18
Mapping RAM Unlock	WO	PR30(7:0)	3?5.35	5.11.19
Mapping RAM Address Counter	RW	PR33(7:0)	3?5.38	5.11.20
Mapping RAM Data	RW	PR34(7:0)	3?5.39	5.11.21
Mapping RAM Control	RW[5]	PR35(1:0)	3?5.3A	5.11.22
LCD Panel Height Select	RW	PR36(7:0)	3?5.3B	5.11.23
Flat Panel Blinking Control	RW	PR37(7:0)	3?5.3C	5.11.24
Color LCD Control	RW	PR39(7:5)	3?5.3E	5.11.25
Vertical Expansion Initial Value	RW	PR41(7:0)	3?5.37	5.11.26
PR43 Unlock Register	WO	PR42(7:0)	3C5.06	5.11.27
Paradise VGA Status	RW	PR43(7:0)	3C5.07	5.11.28
CNF Configuration	HARD[6]	–	–	

TABLE 5-4. PR REGISTERS SUMMARY

NOTES:

1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. In the PR register notation, XXX.YY, XXX is the data port address and YY is the register index.
3. All register addresses are in hex.
4. The designation 3?5 means that the register is mapped into either 3B5 in monochrome mode or 3D5 in color modes.
5. This register is loaded during power on.
6. Not all bits in PR18 and 35 are readable.

The WD90C20 has additional features that enhance the performance and function of the Western Digital Imaging PVGA1A and basic VGA subsystem.

The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

Registers PRO through PR4 and PR11 through PR17 are normally locked. They are write-protected at power-up by the hardware reset. In order to load these registers, the appropriate unlock register, PR5 or PR10, must be loaded first with binary XXXXX101; the register remains unlocked until any other value is written to it. Registers PR0 through PR5 are readable only if PR4 bit 1 = 0. Registers PR10 through PR17 are read- protected at power up by hardware reset. To read registers PR10 through PR17, load PR10 with 1XXX0XXX. The registers remain readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them shows data to be FFH. Setting PR4 bit 1 to 1 does not read protect registers PR10 through PR17. All PR registers are set to 0 at power on reset except where noted.

5.10.1 Address Offset Registers PROA & PROB

PROA - Address Offset Register A
Read/Write Port = 3CF, Index = 09

BIT	FUNCTION
7	Reserved
6 - 0	Primary Address Offset Bits

PROB - Address Offset Register B
Read/Write Port = 3CF, Index = 0A

BIT	FUNCTION
7	Reserved
6 - 0	Alternate Address Offset Bits

The WD90C20 can control up to one megabyte of video RAM. However, the memory map for IBM PC and compatibles assigns 128 Kbytes of the available 1Mbyte total system space to the video controller. Therefore, the video memory space starts at A000:0H and ends at BFFF:FH. This space is further limited to a 64Kbyte video memory partition to allow a second video card to co-exist.

The WD90C20 has two offset registers that help address 512 Kbytes of linear addressed memory. These are PROA and PROB. These registers contain an offset which gets added to the system address when accessing more than 64 Kbytes of video memory. Address offset register PROA is the primary address offset register and is always enabled. Alternatively, Address offset register PROB is enabled only if PR1 bit 3 is set to 1. PROA and PROB provide a seven bit offset that is added to address bits A (18:12) of the system address to form a 20-bit address. The arrangement is similar to that of the segment register DS and ES of the 8088/80X86 architecture, with PROA and PROB providing 4 Kbyte segments.

In a 64K VGA address space (as defined by Graphics Miscellaneous Register Bits 3 and 2), when PROB is enabled by setting PR1 bit 3 = 1, PR address offset registers, PROA and Alternate Offset Address register (PROB), may be used to access two 32 Kbyte video RAM windows. PROA window is mapped from A800:0H–AFFF:FH while PROB is mapped from A000:0H–A7FF:FH.

When there is a 128 Kbyte address space (as defined by Graphics Miscellaneous Register bits 3 and 2) and the Alternate Offset register is enabled, PROA is mapped from B000:0H-BFFF:FH, while PROB is mapped from A000:0H-AFFF:FH.

23

5.10.2 PR1 - Memory Size, Read/write Port = 3CF, Index = 0B

BIT	FUNCTION
7, 6	Memory Size Select
5, 4	Memory Map select
3	Enable Alternate Address Offset Register PR0B
2	16-Bit Video Memory
1	16-Bit BIOS ROM
0	BIOS ROM Map Out

This register is 8 bits wide. Bits PR1 (1:0) are latched internally at power on reset from the corresponding memory data bus pins MD(1:0), using either pull-up or pull-down external resistors. Pull-up resistors on MD(1:0) cause PR1(1:0) bits to be latched low.

Bits 7, 6

Memory Size.

BIT7	BIT6	PR16(1)	MEMORY SIZE	MAPPING
0	0	0	256KB STANDARD VGA	VGA*
0	1	0	256KB WD90C00 VGA	PVGA**
1	0	0	512KB WD90C00 VGA	PVGA
1	1	0	1024KB WD90C00 VGA	PVGA
X	X	1	ANY OF THE ABOVE	VGA*

NOTE:

* Only 64 Kbytes are accessible for chained 4 packed pixel mode.

**WDI extended modes can fully utilize up to 256 Kbytes.

256KB of available VGA video memory space is divided into four 64KB maps (0-3), each defining bit planes (0-3). In mode 13, the four bit planes are chained to form one large bit plane. The starting address of the 256KB video memory buffer can be configured to match other video adapters and/or application programs. For example, 256KB video display buffer, with 128KB or 64KB segments, can start at address A000:0 (Hex), while 32KB segments start at address B000:0 (Hex) or B800:0 (Hex). WD90C20 enhances memory size capability when bits 6 and 7 are programmed to extend video buffer size to 512KB or 1024KB.

DRAMS	MA8 PIN	VIDEO SPACE	MEMORY PLANES
64Kx4	N/U	256KB	Four (64KB Per Plane)
64Kx4	BANK SELECT	512KB	Four (128KB Per Plane)
256Kx4	DRAM PIN A8	1024KB	Four (256KB Per Plane)

The DRAM organizations supported by the WD90C20 and its associated video space are shown in the table at the bottom of the page.

When video memory size is 512KB, and 64Kx4 DRAMs are used, two banks of 64KB form 128KB per plane. MA8 provides the bank selec-

tion using an external multiplexer to access the appropriate bank in a plane by multiplexing the CAS10N and CAS32N signals. Four planes form the desired 512KB video memory space. For 1024KB video memory size, MA8 is directly connected to the A8 address pin of the 256Kx4 DRAMS, and two DRAMS form a 256KB space per plane. Four planes make the desired 1024KB video memory space.

PR1 bits 7 and 6 must be set to reflect the amount of memory installed. These bits in conjunction with PR16(1) also select the way memory is mapped into the system address space. If PR16(1) is set to 1, the memory mapping is the same as IBM VGA regardless of PR1 (6) and PR1(7)

RAM ADDRESSING:

PR1(7) **PR1(6)**
0 0 256K TOTAL; 64KB/PLANE; IBM VGA MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	0	0	0	0	0	0
MA(16) *	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(0)	A(0)	CA(0)	A(16) or XRN(5)	CA(15) or CA(13)	A(14)	CA(12)

RAM ADDRESSING:

PR1(7) **PR1(6)**
0 1 256K TOTAL; 64K/PLANE;
WD90C20 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

RAM ADDRESSING:

PR1(7) **PR1(6)**

1 0 512K TOTAL;128KB/PLANE; WD90C20 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	0	0	0	0	0	0
MA(16) *	A(16)*	CA(16)*	A(17)*	CA(16)*	A(18)*	CA(16)*
*						
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

NOTE: * Controls CAS external to WD90C20

RAM ADDRESSING:

PR1(7) **PR1(6)**

1 1 1024K TOTAL IN FOUR PLANES;256K/PLANE; WD90C20 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)
MA(16)	A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)
MA(0)	A(0)	CA(0)	A(18)	CA(17)	A(18)	CA(16)

NOTES:

1. A(19:0) are WD90C00 internally modified system Addresses.
2. CA(17:0) are CRT Controller Character Address Counter Bits.
3. XRN(5) is Miscellaneous Output Register 3C2H, inverted bit 5. This bit selects the displayed page in chained modes. XRN(5) is selected as MA(0) if Graphics Register 6 bit 3 or bit 2 = 1.
4. CA(13) is selected as MA(0) if CRTC Mode Register 17 bit 5 = 0.

Bit5	Bit4	MEMORY MAP
0	0	VGA Mapping in 64KB space - A000:0H to BFFF:FH Address Range
0	1	First 256KB in 1MB space - 0000:0H to 3FFF:FH Address Range
1	0	First 512KB in 1MB space - 0000:0H to 7FFF:FH Address Range
1	1	First 1024KB in greater or equal to 1 MB space - 0000:0H to FFFF:FH Address Range

Bit 3

Enable Alternate Address Offset Register PROB.

Bit 2

Enable 16 bit bus for Video Memory.
When set to 1, DS16N will be active low in text modes and packed pixel modes such as mode 13h. Planar graphics modes will always have $\overline{DS16}$ inactive.

Bit 1

When set to 1, the BIOS ROM has a 16 bit data path.

If set to 0, the BIOS ROM data path is 8 bits wide. A pull-up on MD (1) sets this bit to 0 at power on reset. $\overline{ROM16}$ has the value of 0 when this bit is set.

Bit 0

If set to 1 the BIOS ROM is mapped out. A pull-up resistor latches 0 after power up. A pull-up on MD(0) sets this bit to 0 at power on reset.

5.10.3 PR2-Video Select Register, Read/Write Port = 3CF, Index = 0C

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4, 3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7

Enable AT&T/M24 Register & mode

Bit 6

0: VGA or EGA mode
1: Non-VGA (6845) mode

Bit 5

Character Map Select. The following functions are overridden by setting PR15(2). This bit, in conjunction with PR2(2) and bit 3 of the attribute code, enables character maps from planes 2 or 3 to be selected according to the table below:

PR2(5)	PR2(2)	ATT(4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE:
Setting PR15(2) = 1, i.e., selecting "page mode addressing" overrides the "plane selected" table shown above.

Bit(4:3)

Character clock period control

0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132 character mode)
1	0	9 dots
1	1	10 dots

Selecting 10 dots per character modifies the function of the horizontal PEL Panning register (3C0.13). Pixel panning in the 10 dot-character modes is obtained by storing the following values into the horizontal PEL Panning register.

PEL PANNING REGISTER VALUE	PELS SHIFTED LEFT
09	0
08	1
00	2
01	3
02	4
03	5
04	6
05	7
06	8
07	9

NOTE:
The character clock period control functions have no effect in graphics modes.

Bit 2

Underline and character map select. Setting this bit to 1 enables underline for all odd values of attribute codes, e.g., Programming 1 gives blue underline. It overrides the background color function of the attribute code bit 3, which is forced to 0. Therefore, only eight choices of background colors are available. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1

This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) is set to 1. When CNF(3) is set to 0, it locks the internal video clock select multiplexer.

Bit 0

Forces horizontal sync timing clock of the CRTC to VCLK.
Uses VCLK when sequencer register 1 bit 3 is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

5.10.4 PR3 - CRT Lock Control Register Read/Write Port=3CF, Index = 0D

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

Register locking is controlled by 4 bits. They are PR3 (5,1,0) and 3?5.11(7) (i.e., the IBM Vertical Retrace End Register bit 7 controlled by index register 11). When bit 7 is 1, CRT controller registers (R0-7) are write protected by VGA definition. Information on the five groups, and their locking schemes, is provided below.

- **Group 0**

These registers are locked if PR3(5)=1 OR 3?5.11(7)=1
CRT Controller Register 00 –Horizontal Total Characters per scan
CRT Controller Register 01 –Horizontal Display Enable End
CRT Controller Register 02 –Start Horizontal Blanking
CRT Controller Register 03 –End Horizontal Blanking
CRT Controller Register 04 –Start Horizontal Retrace
CRT Controller Register 05 –End Horizontal Retrace

- **Group 1**

These registers are locked if PR3(1)=0 AND 3?5.11(7)=1
CRT Controller Register 07(Bit6) –Vert. Display Enable End bit 9
CRT Controller Register 07(Bit1) –Vert. Display Enable End bit 8

- **Group 2**

These registers are locked if PR3(0)=1 OR 3?5.11(7)=1
CRT Controller Register 06 – Vertical Total
CRT Controller Register 07(Bit7) –Vertical Retrace Start bit 9
CRT Controller Register 07(Bit5) –Vertical Total bit 9
CRT Controller Register 07(Bit3) –Start Vertical Blank bit 8
CRT Controller Register 07(Bit2) –Vertical Retrace Start bit 8
CRT Controller Register 07(Bit0) –Vertical Total bit 8

- **Group 3**

These registers are locked if PR3(0)=1
CRT Controller Register 09(Bit5) –Start Vertical Blank bit 9
CRT Controller Register 10 –Vertical Retrace Start
CRT Controller Register 11 [Bits(3:0)] –Vertical Retrace End
CRT Controller Register 15 –Start Vertical Blanking
CRT Controller Register 16 –End Vertical Blanking

- **Group 4**

This register is locked if PR3(5)=1
CRTC mode Control Register 17(Bit2) –Selects divide by two vertical timing

Bit7

Lock VSYNC polarity, as programmed in 3C2 bit 7.

Bit 6

Lock HSYNC polarity, as programmed in 3C2 bit 6.

Bit 5

Lock horizontal timing.
Locks CRTC registers of Group 0 and 4. Prevents attempt by applications software to unlock Group 0 registers by setting 3?5.11 bit 7=0

Bit 4

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 9 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (17).

Bit 3

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (16).

Bit 2

Cursor start, stop, preset row scan, and maximum scan line address register values multiplied by two.

Bit 1

1 = Prevents attempt by applications software to lock registers of Group 1 by its setting 3?5.11 bit 7=1.

Bit 0

Lock vertical timing.
1 = Locks CRTC registers of Groups 2 and 3. Overrides attempt by applications software to unlock Group 2 registers by its setting 3?5.11 bit 7=0.

5.10.5 PR4- Video Control Register Read/Write Port=3CF, Index = 0E

The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAMDAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLNK}}$ / Display Enable
6	PCLK=VCLK
5	Tri-state Video Outputs
4	Tri-state Memory Control Outputs
3	Override CGA Enable Video bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Ext 256 color Shift Register control

Bit 7

This bit controls the output signal $\overline{\text{BLNK}}$. Normally in the VGA mode, $\overline{\text{BLNK}}$ is used by the external video DAC to generate blanking. If this bit = 1, the $\overline{\text{BLNK}}$ output supplies a display enable signal. One of two types of display enable timings can be selected; the choice is determined by PR15(1).

Bit 6

Select PCLK equal to VCLK.
0=PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1=PCLK is always the non-inverted VCLK input clock.

Bit 5

Tri-state the outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLNK}}$.

Bit 4

Tri-state the memory control outputs. The memory address bus, MA(8:0), and all ten DRAM control signals, are tri-stated when this bit is set to 1.

Bit 3

Overrides the CGA "enable video" bit 3 of mode register 3D8, only in 80 x 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2

Lock Internal palette and overscan registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode. It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3CO/3C1 change to write-only mode if the EGA compatibility bit is set. In addition to selecting EGA compatibility bit, setting this bit to 1 disables reading PR0-PR5. In VGA mode (PR(4) bit 1 is zero) 3C0 register is read/write while 3C1 register is read only, according to the Attribute Controller register definitions.

Bit 0

Shift register control. This bit configures the video shift registers for 256-color mode.

5.10.6 PR5 - General Purpose Status Bits Read/Write Port=3CF, Index = 0F

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PRO-PR4 Unlock
1	PRO-PR4 Unlock
0	PRO-PR4 Unlock

Bits (2:0) are READ/WRITE bits and cleared to 0 by reset. They provide lock or unlock capability for PR registers PR0 through PR4 like the PVGA1A. The PR0 – PR4 registers are unlocked when "X5Hex" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register bits 4 through 8. Setting PR(4) bit 1 to 1 read protects registers PR0 – PR5.

Bit 7	CNF(7) [READ ONLY]
Bit 6	CNF(6) [READ ONLY]
Bit 5	CNF(5) [READ ONLY]
Bit 4	CNF(4) [READ ONLY]
Bit 3	CNF(8) [READ ONLY]

Bits (2:0)

READ/WRITE bits and cleared to 0 by reset. They control writing to PR registers PR0-PR4 as follows:

2 1 0	PR0-PR4
0 X X	Write protected
X 1 X	Write protected
X X 0	Write protected

5.10.7 PR10 Unlock PR11-PR17 Read/Write Port = 3?5, Index = 29

This register is READ/WRITE and cleared to 0 by reset. PR10 can be loaded if it contains XXXXX101, and can only be read if it has 1XXX0XXX. Bits (7,3), Bits(6:4), and Bits (2:0) control access to PR registers PR10-PR17. Bits 7 and 3 enable register read operation for PR10 - PR17. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 - PR17.

BIT	FUNCTION
7	PR10-PR17 - Read Enable Bit 1
6 - 4	PR10(6:4) - Scratch Pad
3	PR10-PR17 - Read Enable Bit 0
2 - 0	PR11-PR17 - Write Enable

BIT7	BIT3	PR10-PR17
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

BIT2	BIT1	BIT0	PR11-PR17
0	X	X	Write protected
X	1	X	Write protected
X	X	0	Write protected
1	0	1	Write Enabled

BIT6	BIT5	BIT4	PR10(6:4)
0	X	X	Scratch pad
X	1	X	Scratch pad
X	X	0	Scratch pad
1	0	1	Reserved for manufacturing test.

5.10.8 PR11 EGA Switches Read/Write Port = 3?5, Index = 2A

The EGA switch configuration details are stored in the PR11 register bits.

BIT	FUNCTION
7	EGASW4
6	EGASW3
5	EGASW2
4	EGASW1
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4)

EGA CONFIGURATION SWITCHES SW4-SW1. These bits are READ/WRITE and latched internally at power-on-reset from corresponding memory data bus pins MD(15:12), provided with either pull-up or pull-down external resistors. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. These bits can be read as bit 4 of port 3C2 if the EGA COMPATIBILITY BIT [PR4(1)] has been set to 1. Selection of the bit to be read is determined by bits 3 and 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE 3C2 bit 3	3C2 bit 2	READ 3C2 bit 4
0	0	PR11(7) [=EGA SW4]
0	1	PR11(6) [=EGA SW3]
1	0	PR11(5) [=EGA SW2]
1	1	PR11(4) [=EGA SW1]

PR11 Bits 3 through 0 are READ/WRITE and cleared to 0 at power on reset.

Bit 3

Select EGA Emulation on a PS/2 (VGA-compatible analog) display.

Bit 2

Lock Clock Select. This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

Bit 1

Lock Graphics Controller/Sequencer screen control. Setting PR11(1) to 1 prevents modification of the following bits in the Graphics controller and Sequencer:

Graphics controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by these graphics controller and sequencer bits are locked by setting PR11 bit 1 to 1, they appear unlocked to the system processor during a read operation.

Bit 0

Lock 8/9 dots. Setting this bit to 1 prevents modification of clocking mode sequencer register 3C5.01 bit 0. Although 8 or 9 character timing is locked by setting PR11 bit 0 to 1, the 3C5.01 bit 0 appears unlocked to the system processor during reads.

5.10.9 PR12 Scratch Pad Read/Write Port = 3?5, Index = 2B

BIT	FUNCTION
7 - 0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power up.

5.10.10 PR13 Interlace H/2 Start Read/Write Port = 3?5, Index = 2C

BIT	FUNCTION
7 - 0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1. All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00). The equation is as follows:

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE:
HRD = Horizontal Retrace Delay, determined by bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

5.10.11 PR14 Interlace H/2 End Read/Write Port = 3?5, Index = 2D

Bits 4 through 0 are unaffected by hardware reset and undefined at power up. Bits 7 through 5 are cleared to 0 by reset.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4 - 0	Interlaced H/2 Start

Bit 7

Enable IRQ. This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to 0. This bit should not be set to 1 in MICRO CHANNEL operation.

Bit 6

Vertical double scan. This bit should be set to 1 when emulating EGA on a PS/2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed line counter and row scan counter to be clocked by divide-by-two horizontal timing if vertical sync polarity (3C2 Bit 7=0) is programmed to be positive. The relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is as follows:

$$N=2(n+1)$$

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5

Interlaced mode.
Setting this bit to 1 selects interlaced mode. Interlaced mode can be used in video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000. Line compare and double scan are not supported.

Bits (4:0)

Interlaced H/2 end bits (4:0). Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

5.10.12 PR15 Miscellaneous Control 1 Read/Write Port = 3?5, Index = 2E

BIT	FUNCTION
7	Read 46E8 Enable
6	Low VCLK
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable reading port 46E8H. This bit is functional only if AT BUS architecture [CNF(2)=1] is selected. Setting this bit to 1 enables I/O port 46E8H to be read, regardless of the state of its own bits 3 and 4 and of port 102 bit 0 (sleep bit). Only bits (4:0) of port 46E8H are readable; bits (7:5) are 0.

Bit 6

Low VCLK. Setting this bit to 1 adjusts the memory timing to allow use of a video clock (VCLK) frequency which is much lower than the memory clock (MCLK) frequency. This bit should be set to 1 if the following expression is satisfied:

(MCLK in MHZ) / (VCLK in MHZ)2

Bit 5

Latched VCLK1 and VCLK2. This bit is used only if CNF(3) = 1 (which configures the VCLK1 and VCLK2 pins as outputs). Setting this bit to 1 causes outputs VCLK1 and VCLK2 to equal bits 2 and 3 of I/O write register (Miscellaneous output register) at 3C2H, respectively.

Bit 4

Select MCLK as video clock. Setting this bit to 1 causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs cannot be selected when this bit is set.

Bit 3

Interlaced Compatibility. This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to 1 if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to 1 causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of leading edge, as generated for VGA timing.
Setting this bit to 1 also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing. Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory (by 30-40%). Set this bit to 1 if 132 character mode timing is selected (see description of PR2). Setting this bit to any alpha mode overrides the character map select functions of PR2(2) and PR2(5). When this bit is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight, 8K memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by bits (2:0) of this register, while the map selection is determined by the bits (4:3). A pair of adjacent 8K character maps in planes 2 and 3 (adjacent in the sense that they have the same addressing), may be selected by bit 3 of the attribute code.
The Character attribute bit 3, in conjunction with bits 3 and 4 of the Character Map Select register (3C5.03), determine a character map from either Plane 2 or Plane 3 as shown by the table below.

3C5.03 BIT4	3C5.03 BIT 3	ATT BIT3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

Note:
The above Character Map Select functions override the functions of PR2(5) and PR2(2).
This bit must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select.
This bit is used to choose between two types of Display Enable timings available at output pin BLNKN if PR4(7)=1. If PR4(7)=0, this bit has no effect.
0=BLNKN supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.
1 = BLNKN supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable border.
Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

5.10.13 PR16 Miscellaneous Control 2 Read/Write Port = 3?5, Index = 2f

BIT	FUNCTION
7	External reg. 46E8H lock
6	CRTC Address count Width bit 1
5	CRTC Address Count Width bit 0
4	CRTC Address Counter Offset bit 1
3	CRTC Address Counter Offset bit 0
2	Enable Odd/Even Page bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit (7)

Lock External 46E8H register.
Setting this bit to 1 causes EBROMN output to be forced high (inactive) during I/O writes to port 46E8H. This bit has no effect on loading the internal port 46E8H.

Bit (6:5)

CRTC Address Counter Width.
Power on reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512KB or 1024KB of video memory in which the CRT controller is limited to only 64K or 128K locations. Bit PR16(6) should be set 1 to ensure that the VGA and EGA compatible operation of the address counter is limited to 64 K locations. The following table shows details:

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256KB
0	1	128K
1	X	64K

Bit (4:3)

CRTC Address Counter Offset.
Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively. The 2-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2

Enable Page Bit for Odd/Even.
This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory, and setting 3C5.04(3) to 0 to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size bits PR1(7:6).

Bit 1

VGA Memory Mapping.
Setting this bit to 1 selects 256KB IBM VGA Mapping, regardless of the Memory Size bits PR1(7:6).

Bit 0

Lock RAMDAC write strobe (3C6H - 3C9H). Programming this bit to 1 causes output WPLTN to be forced to 1, disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C20, is also protected from the modification but may still be read at the port 3C7h. For normal operation, program this bit to 0.

5.10.14 PR17 Miscellaneous Control 3 Read/Write Port = 3?5, Index = 30

This two bit register can be loaded only if PR10 (3?5.29) contains XXXXX101. It can be read only if PR10 contains 1XXX0XXX, and both PR10 and PR30 are locked.

BIT	FUNCTION
(7:2)	Reserved
1	MDA Compatibility
0	Map out 2K from BIOS ROM

Bit (7:2)

Reserved.

Bit 1

MDA Compatibility Enable Bit.
Setting this bit to 1 enables MDA compatibility which will –

1. Disable I/O write to Hercules register 3BF.
2. Force bit 7 of 3BA to 1.
3. Select underline decode of attribute XXXXX001 (if this bit is 0, underline decode is X000X001).

Reset sets this bit to zero.

Bit 0

Map Out 2K of BIOS ROM.
Setting this bit to 1 disables access of the BIOS ROM in the system address range C6000H – C67FFH. Power on reset sets this bit to 1. Clearing this bit to 0 enables access to all 32K addresses of the BIOS ROM from CC000H – C7FFFH.

5.10.15 PR18 Flat Panel Status Register Read Only Port = 3?5, Index = 31

Bit 7

Reserved.

Bit 6

Enable Free Running Clock for Plasma or TFT Panel.
0 = Disable free running.
1 = Enable free running.
(This bit is used for the WD90C22 only.)

Bit 5

Enable 256K Colors in STN Color LCD.
0 = Select 4K colors.
1 = Select 256K colors.
(This bit is used for the WD90C22 only.)

Bit 4

Enable Reverse Video in Flat Panel Mode.
This bit is used to reverse the polarity of video output data UC(3:0) and LD (3:0).
0 = Disable reverse video, positive polarity.
1 = Enable reverse video, negative polarity.
(This bit is used for the WD90C22 only.)

Bit 3

Enable Highest Contrast Intensity in Text Mode.
0 = Disable.
1 = Enable.
(This bit is used for the WD90C22 only.)

Bit 2

TFT Color LCD Select.
This bit is not readable.
0 = Disable TFT type color LCD panel interface.
1 = Enable TFT type color LCD panel interface.

Bit(1:0)

Panel Select Bit 1 and Bit 0.

These two bits are used to select different sets of parameters which will be loaded into the CRT controller. The parameters should be locked after loading.

PSB (1)	PSB(0)	Panel Type
0	0	Dual Panel LCD display
0	1	Plasma display
1	0	EL display
1	1	Single Panel LCD display

5.10.16 PR19 Flat Panel Control Register Read/Write Port = 3?5, Index 32

BIT	FUNCTION
7	Plasma Panel Select
6	FP Timing Select
5	CRT Display Enable
4	Flat Panel Display Enable
3	Screen Auto-Centering/Vertical Expansion Select
2	Enable Auto Centering and Vertical Expansion
(1:0)	Number of Gray Scale Select

Bit 7

Plasma Panel Select.
This bit is used to select two different plasma panels.
0 = Select 4 data bits/1 pixel interface.
1 = Select 8 data bits/2 pixel interfaces (4 bits/pixel).

Bit 6

FP Timing Select.
This bit is used to select two different frame pulse (FP) timings for different LCD panels.
0 = Select ON time during first horizontal line.
1 = Select ON time during second horizontal line.

Bit 5

CRT Display Enable.
This bit selects either CRT or Flat Panel to be the main (current) display. When the bit is enabled, the CRT controller will be loaded with the parameters based on the CRT monitor. If bit 5 has been enabled, bit 4 should be disabled. If bit 5 is disabled, bit 4 can be either enabled or disabled.
0 = Disable CRT (default).
1 = Enable CRT.

Note: When the CRT is the selected display, outputs LD03 and UD0-3 are active and can be used to drive an external RAMDAC.

Bit 4

Flat Panel Display Enable.
This bit selects the flat panel as the main display.
0 = Disable Flat Panel display.
1 = Enable Flat Panel display (default).

PR18(1)	PR18(0)	pr19(5)	PR19(4)	CRT Controller (Timing)
0	0	0	1	Based on LCD
0	0	1	0	Based on CRT
0	1	0	1	Based on Plasma
0	1	1	0	Based on CRT
1	0	0	1	Based on EL
1	0	1	0	Based on CRT

Bit 3
Screen Auto Centering/Vertical Expansion Select.
0 = Auto-centering (default).
1 = Reserved for Vertical Expansion. (Set to 0.)

Bit 2
Enable Auto-Centering and Vertical Expansion.
0 = Disable (default).
1 = Enable.

Note: This is used only for pulse wave modulation on the LCD panel.

Bit (0:1)
Number of Gray Scale Select.

PR19(1)	PR19(0)	Gray Scale Number
0	0	2 (mono)
0	1	4
1	0	8
1	1	16

5.10.17 PR1A Flat Panel Control II Register Read/Write Port 3?5, Index = 33

BIT	FUNCTION
(7:6)	Select IOCHRDY Release Timing in CPU Memory Read Cycle
(5:4)	Select IOCHRDY Release Timing in CPU Memory Write Cycle
3	Enable CGA Color to Gray Scale Adjustment
2	Shading Method Select
1	Select Number of Memory Refresh Cycles
0	Select Memory Refresh Cycles Control

Bit(7:6)
Select IOCHRDY Release Timing in CPU Memory Read Cycle.

Bit 7	Bit 6	Release Timing
0	0	1 MCLK delay before CPU complete read cycle
0	1	2 MCLK delay before CPU complete read cycle
1	0	3 MCLK delay before CPU complete read cycle
1	1	4 MCLK delay before CPU complete read cycle

Bit (5:4)
Select IOCHRDY Release Timing in CPU Memory Write Cycle

Bit 5	Bit 4	Release Timing
0	0	1 MCLK delay before CPU complete write cycle
0	1	2 MCLK delay after CPU win arbitration
1	0	1 MCLK delay after CPU win arbitration
1	1	0 MCLK delay after CPU win arbitration

Bit 3
Enable CGA Color to Gray Scale Adjustment. This bit is used to add adjustment of weighting equation in CGA mode to get 16 different gray scale codes.
0 = Disable
1 = Enable

Bit 2

Shading Method Select.
0 = Frame rate modulation (default).
1= Pulse width modulation.

Bit 1

Select Number of Memory Refresh Cycles.
0 = Select 1 refresh cycle/horizontal line.
1 = Select 2 refresh cycles/horizontal line.

Bit 0

Select Memory Refresh Cycles Control.
0 = Memory refresh cycles controlled by CRT controller.
1 = Memory refresh cycles controlled by PR1A(1).

5.10.18 PR1B Flat Panel Unlock Register Write Only Port 3?5, Index = 34

This register is used to protect PR18, PR19, PR1A, PR36 - PR41, and PR44 from being read from or written to. In order to access these registers, PR1B must be loaded first with 101XXXXX, PR18, PR19, and PR1A. In addition, PR36-41 must remain unlocked (until another value is written to PR1B).
PR1B is also used to lock all Shadow registers. To unlock the Shadow registers, PR1B must be loaded first with XXXXX110; all Shadow registers remain unlocked until another value is written to the PR1B register.

5.10.19 PR30 Mapping RAM Unlock Register Write Only Port = 3?5, Index = 35

This register is used to protect mapping RAM registers (PR33 – PR35) from being accessed. In order to read or write to these registers, PR30 must be loaded first with X011XXXX; all mapping RAM registers remain unlocked until another value is written to the PR30 register.

5.10.20 PR33 Mapping RAM Address Counter Register Read/Write Port = 3?5, Index = 38

This register is used to select the RAM ADDRESS COUNTER register.

Note: Any I/O Read or Write to the I/O port 3?5.39H (Mapping RAM Data register) will increment the Mapping RAM Address Counter by one.

5.10.21 PR34 Mapping RAM Data Register Read/Write Port = 3?5, Index = 39

This register is used to select the RAM DATA register for memory read or memory write.

5.10.22 PR35 Mapping RAM and Power Down Control Register Read/Write Port = 3?5, Index = 3A

BIT	FUNCTION
7^1	Select System Power Down Mode/Display Idle Mode
6^1	Select Internal Divided By 8 Clock to Control General Power Down Mode
5^1	Host Release Control
4^1	Reserved; set to 1.
$3^{1,2}$	Select 64 Gray Scale Levels
$2^{1,2}$	Enable $\overline{CAS}$ before $\overline{RAS}$ Memory Refresh Cycle
1	Enable Weighting Equation
0	Reserved; set to 1.

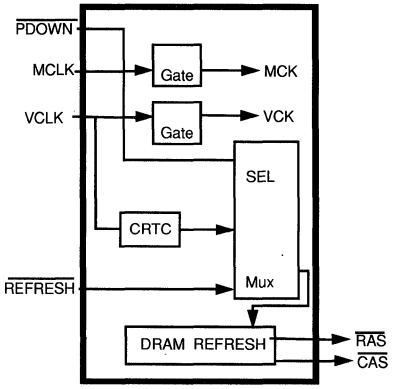
[1]Not Readable.
[2]Used in WD90C22 only.

Bit 7

Select system power down mode/display idle mode. Refer to Figure 5-1. This bit is not readable.
0 = Display idle mode (default).
1 = System power down mode; MCLK and VCLK turned off.

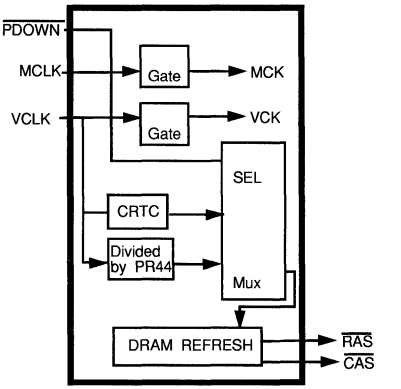
Bit 6

Select Internal Divided by 8 Clock to Control General Power Down Mode. This bit is active only when PR44(7) is set at 1. This bit is not readable.
0 = Disable internal clock.
1 = Enable internal clock; clock is divided by 8.



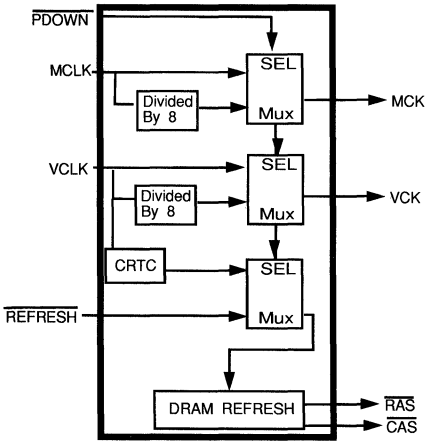
SYSTEM POWER DOWN MODE (SLEEP)

A. RAMDAC is off.
B. Clock inputs are turned off as they enter the chip.
C. CAS before RAS video memory refresh is generated from REFRESH input.
D. Neither video memory or I/O can be accessed in this mode.
E. RAMDAC and Mapping RAM contents are lost and must be reloaded to resume.



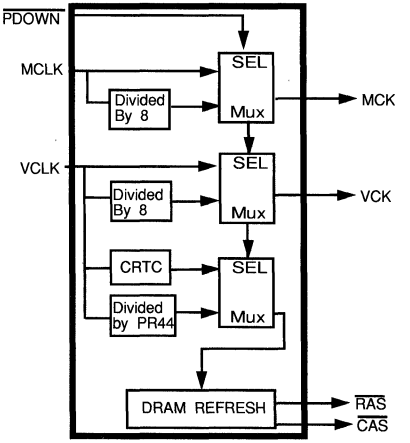
GENERAL POWER DOWN MODE (EXTERNAL CLOCK)

A. RAMDAC is off.
B. MCLK and VCLK are not modified; their speed is reduced by system resources.
C. Refresh cycles triggered by PR44 may be RAS only or CAS before RAS.
D. Video memory and I/O are accessable.



DISPLAY IDLE MODE (SUSPEND/RESUME)

A. RAMDAC is off.
B. MCLK and VCLK are divided by 8.
C. Refresh is CAS before RAS and generated by REFRESH input.
D. I/O is accessable and memory is not accessable.



GENERAL POWER DOWN MODE (INTERNAL CLOCK)

A. RAMDAC is off.
B. MCLK and VCLK are divided by 8.
C. Refresh cycles triggered by PR44 may be RAS only or CAS before RAS. PR44 can be RAS only.
D. Video memory and I/O are accessable.

FIGURE 5-1. SYSTEM POWER DOWN MODE/DISPLAY IDLE MODE

PR44(7)	PR35(7)	PR35(6)	MODE
0	1	X	System Power Down Mode: MCLK and VCLK are turned off. Video memory refresh is generated from PDREF. Neither memory nor I/O can be accessed. RAMDAC and Mapping RAM must be reloaded.
0	0	X	Display Idle Mode: MCLK and VCLK are divided by 8 before being distributed across the chip. Video memory refresh is generated from PDREF. Only I/O can be accessed.
1	X	0	General Power Down (External Clock Used): MCLK and VCLK inputs are used to drive the chip . The assumption is made that MCLK and VCLK have been reduced by some other part of the system. The video memory refresh period is readjusted for the slower clock by PR44(6:0). Both memory and I/O can be accessed.
1	X	1	General Power Down (Internal Clock Used): MCLK and VCLK inputs are divided by 8 before being distributed across the chip. The video memory refresh period is readjusted for the slower clock by PR44(6:0). Both memory and I/O can be accessed.

Bit 5

Host Release Control.
This bit is designed to allow another VGA controller in the I/O bus. When PR35(5) is set to 1 and PDOWN input is set to 0, the WD90C20 will not respond to any CPU memory or I/O accesses. All output buffers of the system interface are turned off (tri-state).

There are four power down modes. The following conditions are true in each power down mode.
1. Video memory is maintained.
2. RAMDAC outputs are turned off.
3. Panel outputs are turned off.

Bit 4

Reserved. This bit is set at 1.

Bit 3

Select 64 Gray Scale Levels (reserved for the WD90C22 chip).
0 = Select disabled; select 32 gray scale levels.
1= Select enabled; select 64 gray scale levels.

Bit 2

Enable $\overline{CAS}$ before $\overline{RAS}$ memory refresh cycle.
0 = $\overline{RAS}$ only refresh cycle (default).
1 = $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

Bit 1

Enable Weighting Equation.
This bit is used to turn the IBM VGA weighting equation on and off in either color mode or monochrome mode.
0 = Disable weighting equation.
1 = Enable weighting equation.

Bit 0

Reserved. This bit is set at 1.

5.10.23 PR36 Panel Height Select Register Read/Write Port = 3?5, Index = 3B

This register is loaded with the height, less 1, of a single panel. This information is used to calculate auto-centering, vertical expansion, and related values. In a 640 x 480 dual panel display, this register should be loaded with "EF". (480/2)-1 = 239_{10} = EFH. In a 640 x 400 dual panel display, the equation is: (400/2)-1 = 199_{10} = C7H.

5.10.24 PR37 Flat Panel Blinking Control, Read/Write Port = 3?5, Index = 3C

This register is used to select cursor or character blinking rate on flat panels. In CRT mode, this register is ignored.

Bit	2	1	0	CURSOR BLINKING RATE SELECT
	0	0	0	No cursor blinking
	0	0	1	8 frames (8 on, 8 off)
	0	1	0	16 frames (16 on, 16 off)
	0	1	1	32 frames
	1	0	0	64 frames
	1	0	1	128 frames
Bit	5	4	3	CHARACTER BLINKING RATE SELECT
	0	0	0	No cursor blinking
	0	0	1	8 frames (8 on, 8 off)
	0	1	0	16 frames (16 on, 16 off)
	0	1	1	32 frames
	1	0	0	64 frames
	1	0	1	128 frames
Bit	6			PLASMA SHIFT CLOCK SELECT
	0			Select falling edge of the clock to latch data
	1			Select rising edge of the clock to latch data
Bit	7			LCD LP SIGNAL SELECT
	0			LP will be disabled during vertical blanking period
	1			LP will be generated continuously during vertical blanking period (SCLK will be turned off)

5.10.25 PR39 Color LCD Control Register Read/Write Port = 3?5, Index = 3E

This register is used to support color LCD panel.

BIT	FUNCTION
7	Enable Border LP Control
6	Color LCD Panel Border Select
5	Enable Color LCD Panel
4-0	Reserved

Bit 7

Enable border LP control.
This bit is used to generate a special LP pulse to latch border information (black or white).
0 = Disable LP border control.
1 = Enable LP border control.

Bit 6

Color LCD panel border select.
0 = Select black border.
1 = Select white border.

Bit 5

Enable Color LCD Panel.
This bit is used to select monochrome LCD or color LCD.
0 = Disable color LCD panel select.
1 = Enable color LCD panel select.

5.10.26 PR41 Vertical Expansion Initial Value Register Read/Write Port = 3?5, Index = 37

This register is reserved.

5.10.27 PR42 – PR43 Unlock Register Write Only Port = 3C5, Index = 06

This register locks the PR VGA Status register. In order to read/write to the PR VGA status register (PR43), PR42 must be loaded first with X1X01XXX; PR43 will remain unlocked until another value is written to PR42.

5.10.28 PR43 PR VGA Status Register Read/Write Port = 3C5, Index = 07

This register is used to indicate the current status of the PR VGA chip and to enhance programming compatibility.

BIT	FUNCTION
(7:4)	Read/Write Scratch Pad Bits
3	Color/Monochrome Emulation Status
2	Mode Type
1	EGA Compatibility Set
0	Display Type

Bit(7:4)

Read/Write Sctatch Pad bits.
These four bits are available for temporary data storage.

Bit 3

Color/Monochrome Emulation Status.
Read only, Bit 0, of Miscellaneous Output register (3C2).
0 = Monochrome emulation is enabled.
1 = Color graphic emulation is enabled.

Bit 2

Mode Type.
Read only, Bit 6 of PR2.
0 = Either VGA or EGA mode is enabled.
1 = Non-VGA and non-EGA modes are enabled.

Bit 1

EGA Compatibility Set.
Read only of PR4, bit 1.
0 = EGA compatibility is disabled.
1 = EGA compatibility and the ability to read PR0 – PR5 registers are enabled.

Bit 0

Display Type.
Read only of PR5, bit 3.
0 = Analog (VGA-compatible) display is attached.
1 = TTL (EGA-compatible) display is attached.

5.10.29 PR44 Power-Down Memory Refresh Control Register, Read/Write Port = 3?5, Index = 3F

This register controls two power saving features when in the general power down modes. Bit 7 is used with PR35(7:6) to determine which power down mode is to be used. With some power down modes, the clocks used to refresh memory are slowed or stopped. This is done because the power consumption of the CMOS chip is proportional to its clock frequency. PR44(6:0) are loaded with a value that modifies the video memory refresh period during power down.

BIT	FUNCTION
7	General Power Down Mode Enable
(6:0)	Memory Refresh Cycle Period

Bit 7

General Power Down Mode Enable Bit. This bit enables general power down mode.
0 = Disables general power down.
1 = Enables general power down.

Bit(6:0)

Memory Refresh Cycle Period.
These bits are loaded with the value Z, which is used to determine the refresh period when general power down mode is used. Refresh period = VCLK x 8 x (Z+5). For example, assume:

1. Two memory refresh cycles are selected during horizontal blanking period in Flat Panel display mode.
2. Each horizontal line has 96 character clocks.
3. MCLK = 36 MHz, VCLK = 25 MHz.
4. PR44 = 8EH.

When in power-down mode, POWRDN = 0, MCLK = VCLK = 5 MHz.

1. Z = 14.
2. Refresh Cycle = 200 ns x 8 x (14 + 5).
3. Maximum Refresh Period = 200 ns x 8 x (14 + 5 - 7) = 19.2 µs.
4. Refresh Active Time = MCLK x 9 x 2 (cycle) = 200 ns x 9 x 2 = 3.6µs.

5.11 INTERNAL I/O PORTS

5.11.1 AT Mode, Write Only Port 46E8H (Also at Port 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7 - 5	Unused
4	Setup
3	Enable I/O & Memory
2 - 0	External BIOS ROM Page Select

Bit(7:5)

Unused.

Bit 4

Setup
Puts WD90C20 into setup mode where only I/O port 102H is accessible.

Bit 3

I/O and Memory Accesses.
0 = Disable I/O and memory accesses.
1 = Enable I/O and memory accesses.

Bit(2:0)

Unused Internally.
Used for BIOS ROM Page select. On I/O accesses to 46E8H, EBROMN becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits to define 4K pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0.

5.11.2 Setup Mode Video Enable, (AT and Micro Channel Modes) Read/Write Port = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7 - 1	Unused
0	Wakeup VGA

Bit(7:1)

Unused.

Bit 0

Wakeup VGA for I/O and Memory Accesses. Only lower 3 address bits are decoded for this port and WD90C20 must be in SETUP mode. VGA Enable Sleep bit or Programmable Option Select (POS) register 102H bit 0 is used to awaken the WD90C20 after power on in MCA and AT mode. To enter the set up mode in AT bus applications, bit 4 of the partially decoded internal I/O port 46E8H is set to 1 before accessing the I/O port 102H. In MCA mode, when the VGASETUP (EION) signal pin is active low, the WD90C20 is in setup mode and port 102H can be accessed.

DAC ADDRESS	TYPE	REGISTER NAME
3C6H	Read/Write	PEL Mask
3C7H	Read/Write	When written: PEL Address Read Mode; when read: DAC State Register.
3C6H	Read/Write	PEL Address (Write Mode)
3C9H	Read/Write	PEL Data Port

5.12 VIDEO RAMDAC PORTS

The WD90C20 incorporates a complete Micro Channel-compatible RAMDAC, as well as the ability to support an optional external RAMDAC. Selection of the internal or external RAMDAC option is based on the state of the VREF pin when reset is de-asserted.

Data from the internal RAMDAC is always written to the data bus, even when the internal RAMDAC is configured for use with external RAMDAC. RDPLT may be used as a gate to send data from an external RAMDAC to the data bus.

5.12.1 PEL Mask Register, Read/Write Port = 3C6

The eight-bit PEL Mask Register, along with the eight bits of color information from the combination of the attribute controller and the color select register, are ANDed together and become the index into the color lookup table of the RAMDAC during display refresh. The contents of this register have no effect on host access to the lookup table. The host may access this register at any time without disturbing the contents of the lookup table. The contents of this register are undefined after reset.

5.12.2 PEL Address – Read Mode, Read/Write Port = 03C7

The host reads data from the color palette RAM by first writing the index of the first location to be read into this register. When this is done, the RAMDAC loads the RAM data specified by the index into an eighteen bit holding register. The contents of this register are read out via three reads to the PEL Data Port. The data read during these reads consists of six bits of color information packed into the six least significant bits of the port. The two most significant bits of data during these reads are set to zero. The color information is delivered in the sequence: red, green, blue. After the three read cycles have completed, the contents of the PEL address register are automatically incremented by one. In this way, sequential locations can be read by sets of three reads from the PEL Data Port.

5.12.3 DAC State Register Register, Read/Write Port = 03C7

Bits 0 and 1 of this register indicate whether the last active operation to the DAC was a read or a write. These bits are both 0 if the bit was a read operation; they are both 1 if it was a write.

5.12.4 PEL Address – Write Mode, Read /Write Port = 03C8

The host writes data from the color palette RAM by first writing the index of the first location to be written into this register. Completed PEL data to be written is then loaded into an eighteen bit holding register via three writes to the PEL Data Port. This is accomplished by concatenating the six least significant bits of the data from the three writes. The color information is extracted in the sequence: red, green, blue. When this is done, the RAMDAC loads the contents of the holding register into the palette RAM location indexed by the contents of the PEL Address (write mode) register. After the data has been transferred to the RAM, the contents of the PEL address register are automatically incremented by 1. In this way, sequential locations can be written by sets of three writes to the PEL Data Port.

5.12.5 PEL Data Read/Write Port = 03C9

This port is used to transfer 6-bit PEL data values to and from the palette RAM. The eighteen bit palette locations are transferred in the order: red, green, blue.

5.13 WD90C20 CONFIGURATION BITS, CNF

The configuration register, CNF, is not a physical register, but a convenient way to reference the state of the video memory data lines which are latched at reset. These data lines–for the sake of convenience, collectively called the configuration register CNF– provide setup parameters to various areas on the chip.

When the WD90C20 is reset, it latches the state of the video memory data lines. This data provides setup parameters to various areas of the chip. In order to easily reference these individual bits, we collectively refer to them as the configuration register, (CNF). Only fifteen data lines are used in the WD90C20 and WD90C22; in both chips, data line MD10 is not used. (Refer to Table 4-1, page 17.)

CNF (11)

Color/Mono LCD Panel Select
This bit is latched internally at power on reset from corresponding memory data bus pin MD(15), provided with either pull-up or pull-down external resistors. This bit is read from PR11(7), I/O port 3?5.2A bit 7. This bit is affected by writing to 3?5.2A. Pulling up MD(15) causes CNF(11) to be latched high.
0 = Monochrome LCD panels.
1 = Color LCD panels.

CNF (10:9)

Panel Select Bits.
These bits are latched internally at power on reset from corresponding memory data bus pins MD(9:8), provided with either pull up or pull down external resistors. They are read only at I/O port 3?5.31 as bits 1:0 and are unaffected by writing to 3?5.31. Pulling up MD(9:8) data bus pin causes CNF (10:9) to be latched high.

CNF(10)	CNF(9)	DISPLAY TYPE
0	0	Dual panel LCD display
0	1	Plasma display
1	0	EL display
1	1	Single panel LCD display

CNF (8)

Analog/TTL Display Status Bit.
Bit CNF(8) is latched internally at power on reset from memory data bus pin MD(11), provided with either a pull-up or pull-down external resistor. Pulling up MD(11) causes CNF(8) to be latched low. This bit controls no internal functions and is read only as bit 3 of PR5 (3CF.0F). CNF(8) is unaffected by writing to PR5 (3CF.0F).
0 = Analog (VGA - compatible) display is attached.
1 = TTL (EGA-compatible) display is attached.

CNF (7:4)

General Purpose Status Bits.
Bits CNF (7:4) are latched internally at power on reset from corresponding memory data bus pins MD (7:4), provided with either pull-up or pull-down external resistors. These are read only bits at PR5 (3CF.0F) positions (7:4). They are unaffected by writing to PR5(3CF.0F). Pulling up MD (7:4) causes CNF (7:4) to be latched low.

CNF (3)

Video Clock Source Control.
This bit cannot be written to or read as I/O port. Pulling up MD (3) causes CNF(3) to be latched high. It configures WD90C20 pins VCLK1 and VCLK2 as inputs or outputs.
0=For inputs.
1=For outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of the dot clock is by an internal multiplexor. When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip during I/O writes to port 3C2H. This load pulse may be inhibited by setting PR11(2)=1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0

input. VCLK1 and VCLK2 outputs are equal to bits 2 and 3 of the Miscellaneous output register at 3C2H, respectively, when PR15 bit 5 is set to 1.

CNF (2)

Bus Architecture Select.
This bit cannot be written to or read as I/O. Pulling up MD(2) causes CNF(2) to be latched high.
0 = Micro Channel architecture
1 = AT BUS architecture

Selecting CNF(2) will change the pinout definition between AT bus and Micro Channel bus. Refer to the pinout description.

PC AT BUS	I/O	MC	I/O
$\overline{\text{MEMCS16}}$	OUT	$\overline{\text{CDDS16}}$	OUT
IOCHRDY	OUT	CDCHRDY	OUT
$\overline{\text{EBROM}}$	OUT	$\overline{\text{CDSFDBK}}$	OUT
$\overline{\text{EIO}}$	IN	3C3D0	IN
$\overline{\text{MEMR}}$	IN	M/IO	IN
$\overline{\text{MEMW}}$	IN	$\overline{\text{S0}}$	IN
$\overline{\text{IOR}}$	IN	$\overline{\text{S1}}$	IN
$\overline{\text{IOW}}$	IN	$\overline{\text{CMD}}$	IN
IRQ	OUT	$\overline{\text{IRQ}}$	OUT
ALE	OUT	$\overline{\text{CDSETUP}}$	IN

5.14 MAPPING RAM – 32 x 5 STATIC RAM

The 32 x 5 SRAM is designed for dithering pattern selecting. This memory is used to adjust the color-to-gray scale mapping from the weighting equation. This mapping RAM can be read or writ ten to by the CPU. During normal operation, the outputs from the weighting equation (5 bits) will be connected to the inputs of the mapping RAM (address input). The outputs of the mapping RAM (5 bits) are connected to the dithering logic.

For the 64 gray scale WD90C22, the mapping RAM is expanded to 32 x 6. This allows the selection of any shade in modes that use fewer than 64 shades.

To write:

OUT 3?4, 35H	Program the index register.
OUT 3?5, 33H	Unlock the mapping RAM registers.
OUT 3?4, 3AH	Program the index register.
OUT 3?5, 01H	Select mapping RAM.
OUT 3?4, 38H	Program the index register.
OUT 3?5, 00H	Load WRITE starting address register with 00.
OUT 3?4, 39H	Program the index register.
OUT 3?5, 0AH	Write 0A directly to the mapping RAM at location 00.
OUT 3?5, 0BH	Write 0B directly to the mapping RAM at location 01.

To read:

OUT 3?4, 35H	Program the index register.
OUT 3?5, 33H	Unlock mapping RAM registers.
OUT 3?4, 3AH	Program the index register.
OUT 3?5, 01H	Select mapping RAM.
OUT 3?4, 38H	Program the index register.
OUT 3?5, 00H	Load READ starting address register with 00.
OUT 3?4, 39H	Program the index register.
IN 3?5	Read directly from the mapping RAM at 00.
IN 3?5	Read directly from the mapping RAM at 01.

Note: There is a minimum timing requirement between two consecutive RAM reads or writes (4 x VCLK). If the system is running faster than 16 MHz, a "NOP" instruction should be inserted between consecutive reads and/or writes.

5.15 Shadow Timing Registers

The shadow timing registers control the timing in the CRTC. When the regular timing registers are written to, the shadow timing registers, if unlocked (in CRT mode, they are unlocked), receive the same data. Locking the Shadow timing registers is controlled by PR1A.

Timing data is always read from the regular timing registers. The shadow timing registers are never read from.

In Flat Panel mode, the shadow timing registers are loaded once and then locked by PR1A. Once they are locked, data written to the timing registers is not passed through to the shadow timing registers and the flat panel timing is not affected.

There are eleven shadow timing registers. All are indexed in port 03?5.

NAME	INDEX	SAMPLE VALUE*
Horizontal Total	00H	5FH
Start Horizontal Blanking	02H	50H
End Horizontal Blanking	03H	82H
Start Horizontal Retrace	04H	54H
End Horizontal Retrace	05H	80H
Vertical Total	06H	F2H
Overflow	07H	00H
Vertical Retrace Start	10H	FOH
Vertical Retrace End	11H	02H
Start Vertical Blank	15H	FOH
End Vertical Blank	16H	F2H

*The sample values are for a monochrome dual panel LCD with 640 x 480 pixels.

23

APPENDIX

A.1 APPLICATIONS APPENDIX

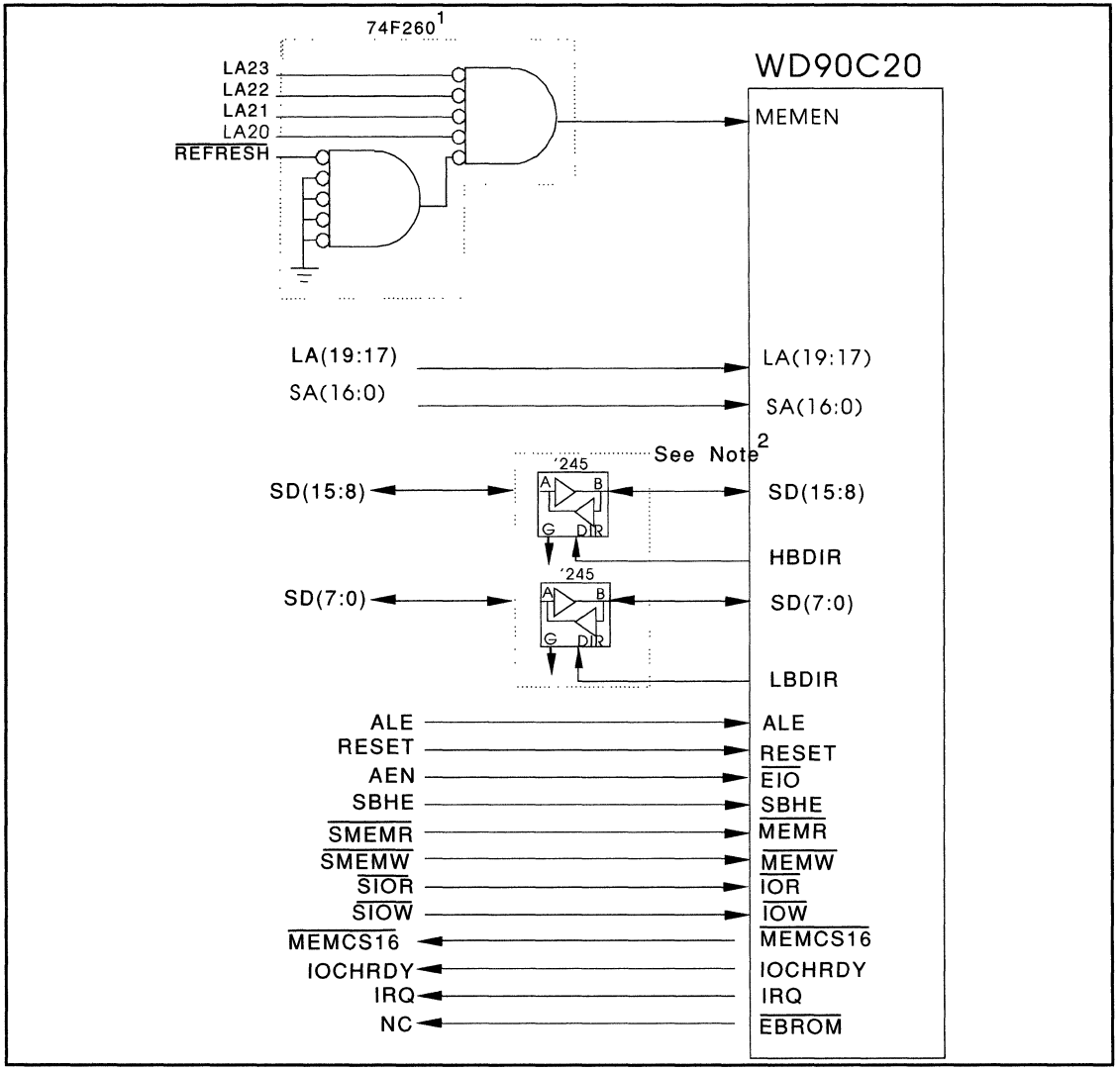


FIGURE A-1. PC/AT INTERFACE

Notes:

[1]The 74F260 is used to determine if the current address is in the first megabyte. This function is already provided by most core logic chip sets.

[2]The 74245 buffers are only needed if system drive requirements exceed chip capabilities.

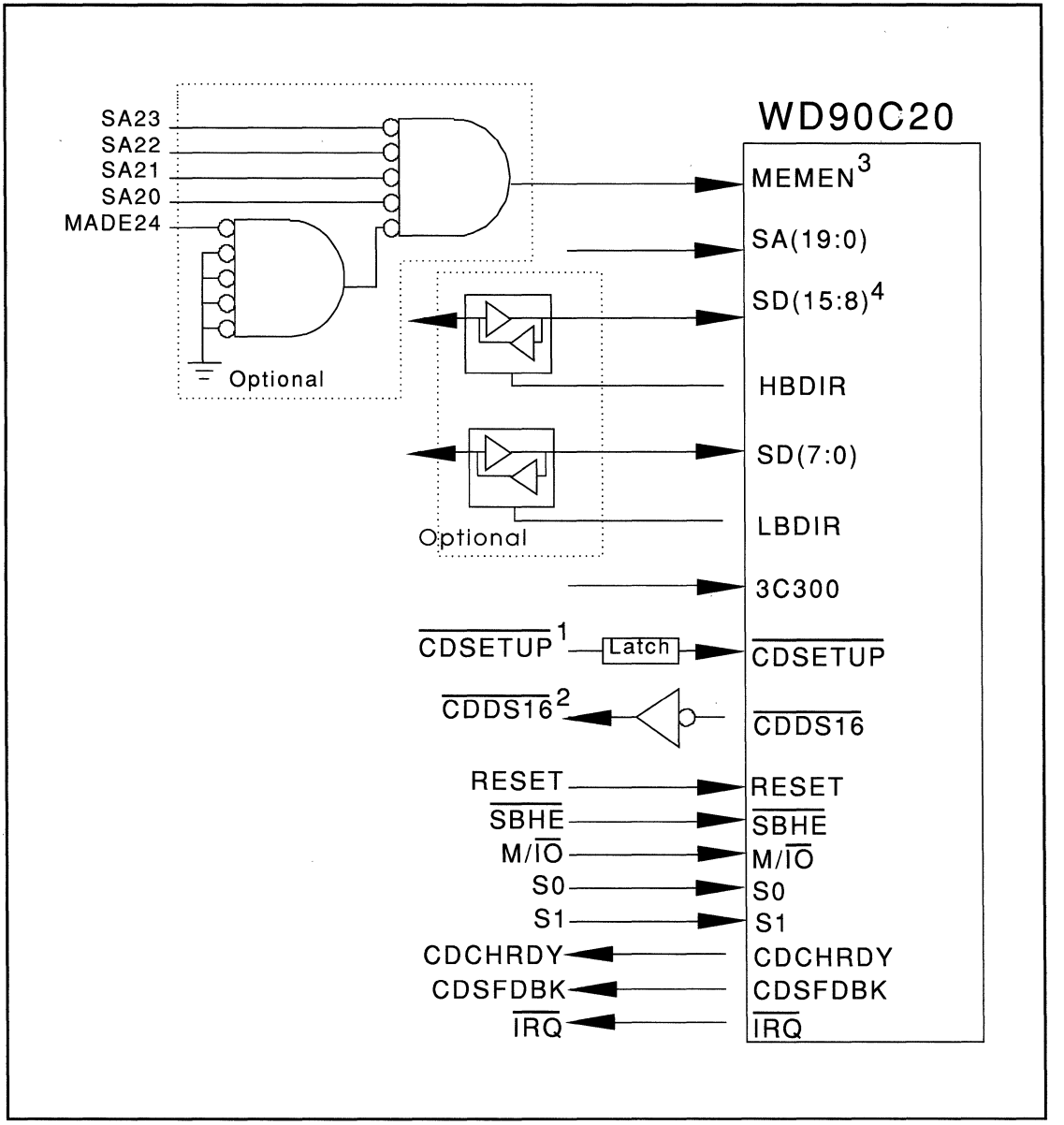


FIGURE A-2. MICRO CHANNEL INTERFACE

Notes:

1 $\overline{\text{CDSETUP}}$ must be latched if core logic does not already latch it.

2 $\overline{\text{CDDS16}}$ requires an inverter.

3 MEMEN must be qualified for the first megabyte of memory space. This is provided in many core logic designs; the two And Gates are not required.

4 The bidirectional buffers are only needed if the system design requires more current than the WD90C20 can deliver.

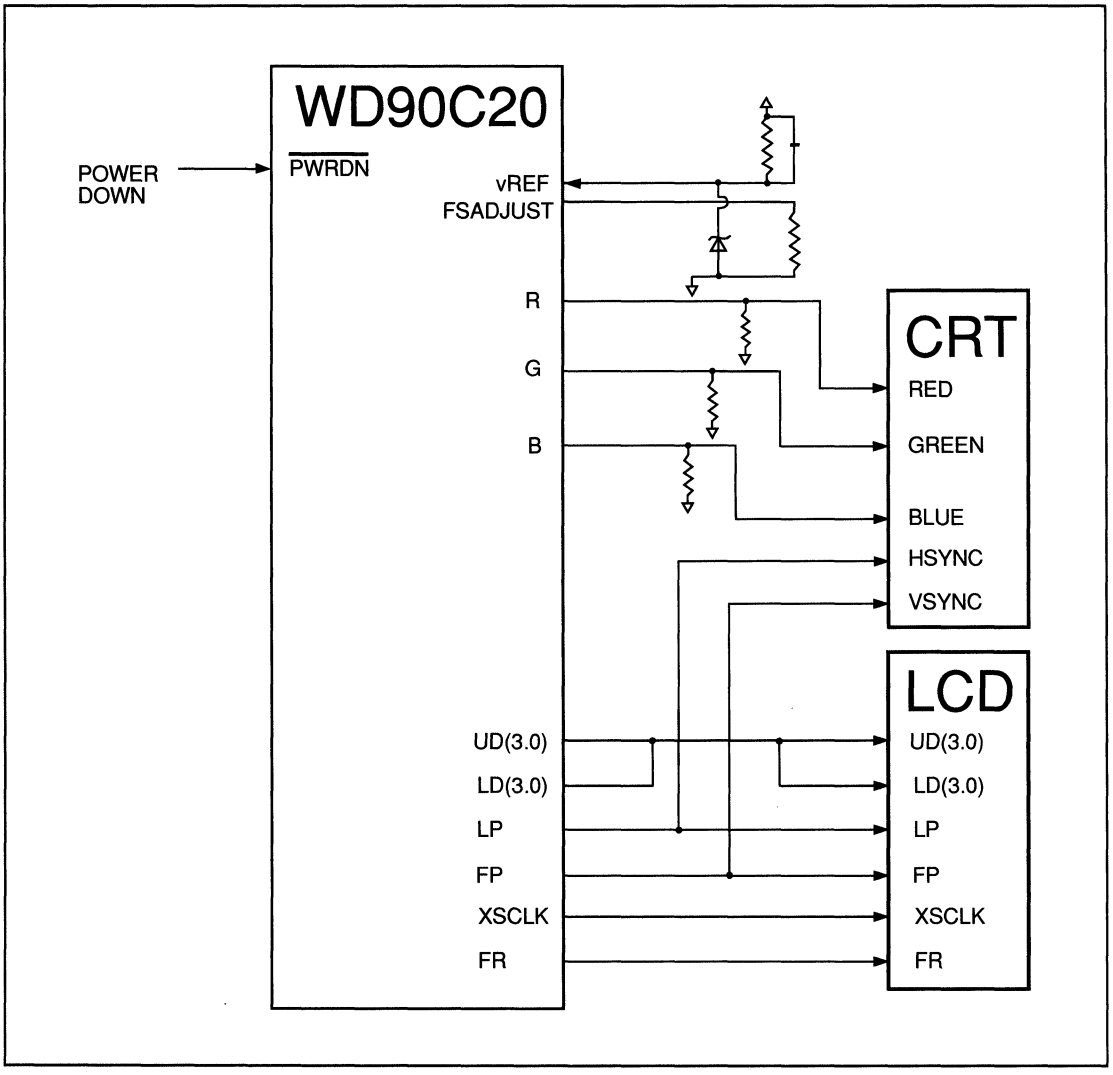


FIGURE A-3. WD90C20 DISPLAY INTERFACE

APPENDIX

B.1 EGA MODE

This appendix provides a general description of EGA mode. Details of the actual software implementation are not covered.

For those registers that are the same in both VGA and EGA mode, refer to the VGA description. Only the differences are described in this section. Bits not used should be set to 0 unless otherwise noted.

- Load Configuration register bit 8. Logic 0 for VGA compatible PS/2 display or Logic 1 for EGA compatible TTL monitor by appropriate pull-up or pull-down resistor on MD(11). (Pull-up resistor on MD11 causes CNF(8) to be latched with logic 0, for Analog PS/2 compatible display). This is status for the BIOS or application to signify monitor type attached.
- Unlock all the PR registers.
- Program PR2(6) to 0 for EGA mode.
- Set PR4 bit 1 to logic 1 for EGA compatibility.
- Load PR11(7:4) with EGA Configuration switches by using pull-up or pull-down resistors on pins MD(15:12). (Pull-up resistor causes logic 1 to be latched after power on reset.)
- The EGA switch setting may then be read from PR11(7:4) at I/O port 3C2 bit 4.

- If EGA is to be emulated on the IBM PS/2 type analog display, follow the steps listed below:
  Initialize all the registers.
  Lock CRT controller registers.
  Force Clock Control rate of the CRT controller.
  - Set EGA emulation mode by programming:
    PR11(3)=1; Set EGA emulation on PS/2 type display
    PR14(6)=1; Vertical double scan
    PR11(2)=1; Lock clock select
    PR11(0)=1; Lock 8/9 dot timing
    PR14(7)=1; Enable IRQ (optional)
  - Lock the PR registers PRO-PR5 and PR10-PR17
  - Read protect PR registers

- When EGA is required on a TTL monitor, the suggested steps are:
  - Initialize all the registers
  - Set EGA TTL mode by programming:
    PR11(3)=0;EGA TTL
    PR14(7)=1;Enable IRQ
    PR15(6)=1;Set Low Clock
    PR14(7)=1;Enable IRQ
  - Lock PR registers PRO-PR5 and PR10-PR17
  - Read protect PR registers

For more details on the PR registers, refer to the PR registers section. The EGA register summary shown on the next page highlight all the EGA mode registers.

B.1.1 EGA Registers Summary

REGISTERS	EGA	I/O PORT
General Registers:		
Miscellaneous Output Reg	WO	3C2
Input Status Reg 0	RO	3C2
Input Status Reg 1	RO	3?A
Feature Control Reg	WO	3?A
Sequencer Registers:		
Sequencer Index Reg	WO	3C4
Sequencer Data Reg	WO	3C5
CRT Controller Registers:		
Index Reg	WO	3?4
CRT Controller Data Reg Except the following:	WO	3?5
Start Address High (Index=0C)	RW	3?5
Start Address Low (Index=0D)	RW	3?5
Cursor Location High (Index=0E)	RW	3?5
Cursor Location Low (Index=0F)	RW	3?5
High Pen High (Index=10)	R	3?5
Light Pen Low (Index=11)	R	3?5
Graphics Controller Registers		
Index Reg	WO	3CE
Other Graphics Reg	WO	3CF
Attribute Controller Registers:		
Index Reg	WO	3CO*
Attribute Controller Data Reg	WO	3CO*

NOTES:

1. RO = Read Only, WO = Write Only, and RW = Read/Write.
2. All register addresses are in hex.
3. ? = B in monochrome modes or D in color modes.
4. * = Identical responses from I/O ports 3CO and 3C1.

B.2 GENERAL REGISTERS

Only the general registers and the bit definitions that differ from VGA mode are covered.

B.2.1 Miscellaneous Output Register (Write Port 3C2)

Bits (7:5)

EGA: Same as Miscellaneous Output Register Bits (7:5) definition in the VGA section.

Bit 4

Disables internal video drivers.
0 = Activate video drivers.
1 = Disable video drivers.

Bits (3:2)

EGA:

BIT 3	BIT 2	DESCRIPTION
0	0	14.318 Mhz clock (VCLK0) is selected.
0	1	16.257 Mhz clock (VCLK1) is selected if Configuration Register Bit 3 is 0.
1	0	External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is 0.
1	1	Not Used. VCLK2 selected if Configuration Register Bit 3 is 0

Bit (0)

EGA: Identical to Miscellaneous Output Register Bit 0 definition in the VGA section.

B.2.2 Input Status Register 0 (Read Port 3C2)

Bit 7

EGA: Same as input Status Register 0, Bit 7 definition in the VGA section.

Bits (6:5)

EGA: Not used.

Bit 4

EGA: Information on the four configuration switches stored in PR11 can be read at this bit if PR4(1) has been set to 1.

Bits (3:0)

EGA: Not used = 1

B.2.3 Input Status Register 1 (READ PORT 3?A)

Bit (7)

EGA: Not used.

Bit 6

EGA: Not used = 1.

Bits (5:3)

EGA: Identical to Input Status Register 1 Bits (5:3) definition in the VGA section.

Bit 2

EGA: The following Light Pen Switch definition is applicable:
0 = Light Pen Switch is Closed.
1 = Light Pen Switch is Open.

Bit 1

EGA: The following Light Pen Trigger definition is applicable:
0 = Light Pen Trigger is Reset.
1 = Light Pen Trigger is Set.

Bit (0)

EGA:
Same as Input Status Register 1 Bit 0 definition in the VGA Section.

B.2.4 Feature Control Register (Write Port 3?A)

Bits (7:0)

EGA: Not used.

B.3 SEQUENCER REGISTERS (PORT 3C5)

B.3.1 Clocking Mode register (Index = 01)

Bits (7:4)

EGA: Not Used.

Bits (3,2)

EGA: Same as Clocking Mode Register Bits (3,2) definition in the VGA section.

Bit 1

EGA: Set to zero.

Bit (0)

EGA: Identical to Clocking Mode Register Bit 0 definition in the VGA section.

B.3.2 Character Map Select Register (Index 03)

Bits (7:4)

EGA: Not Used.

Bits (3:2)

EGA: Character Map Select A:

BIT 3	BIT 2	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

Bits (1:0)

EGA: Character Map Select B

BIT 1	BIT 0	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

NOTE:
1. Character Map selection from Plane 2 is determined by bit 3 of the attribute code.

B.3.3 Memory Mode Register (Index = 04)

Bits (7:3)

EGA: Not Used.

Bits (2:1)

EGA: Identical to Memory Mode Register Bits (2,1) definition in the VGA section.

Bit 0

EGA: Alpha mode bit.
A logic 1 shows that Alpha mode is active and character map selection is enabled. A logic 0 disables Alpha mode and enables non-Alpha mode.

B.4 CRT CONTROLLER REGISTERS (PORT 3?5)

The EGA registers that are different are listed. For similar registers and identical bits within registers refer to the VGA section. A "?" implies that a register is mapped into either 3B5 or 3D5 for Monochrome or Color display modes, respectively.

B.4.1 Index Register (Port = 3?4)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Five bits point to the CRT Register Address index where the data is to be written.

B.4.2 Horizontal Total Register (Index = 00)

Bits (7:0)

EGA:
Eight bits of value for the "Total Character Count Less 2" are loaded into this register. They define number of characters to be displayed per horizontal line.

B.4.3 End Horizontal Blanking Register (Index = 03)

Bits (7)

EGA: Not Used.

Bits (6:5)

EGA: These bits define display enable skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

EGA: Five bits of character count are loaded to determine when the horizontal blanking signal becomes inactive.

B.4.4 End Horizontal Retrace Register (Index = 05)

Bit 7

EGA: It defines the start of the odd or even CRT counter memory address following the horizontal retrace time. Logic "1" = Odd Address and logic "0" = Even Address.

Bits (6:0)

EGA: Same as End Horizontal Retrace Registers Bits (6:0) definition in VGA section.

B.4.5 Vertical Total Register (Index = 06)

Bits (7:0)

EGA: Lower eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

B.4.6 CRT controller Overflow Register (Index = 07)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Preset Row Scan Register Bit (4:0) definitions in the VGA section.

B.4.7 Preset Row Scan Register (Index = 08)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Preset Row Scan Register (4:0) definition in the VGA section.

B.4.8 Maximum Scan Line Register (Index = 09)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as maximum Scan Line Register Bits (4:0) definition in the VGA section.

B.4.9 Cursor Start Register (Index = 0A)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Cursor Start Register Bits (4:0) definition in the VGA section.

B.4.10 Cursor End Register (Index = 0B)

Bit(7)

EGA: Not used.

Bits (6:5)

EGA: They define cursor signal skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	0
1	0	1
1	1	2

Bits (4:0)

EGA: These bits define Cursor End value of row scan address counter. The programmed value is equal to "N+1" where "N" is the last row of the Cursor to be displayed.

B.4.11 Vertical Retrace Start Register (Index = 10) - Write

(Light Pen High register, Index = 10 - Read)

Bits (7:0)

EGA: Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

B.4.12 Vertical Retrace End Register (Index = 11) - Write

(Light Pen Low register, Index = 11 - Read)

Bits (7:6)

EGA: Not used.

Bit 5

EGA: It enables the IRQ output buffer control if Logic 0 is programmed. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal. If programmed as logic 1, the IRQ buffer is switched to a high impedance state.

Bit 4

EGA: When programmed to logic 0, the IRQ latch is reset and cleared to 0 if bit 5 = 0. If it is logic 1, the IRQ latch gets set at the end of the vertical display.

Bits (3:0)

EGA: Identical to Vertical Retrace End Register Bits (3:0) definition in the VGA section.

B.4.13 Underline Location Register (Index = 14)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Horizontal scan row where the underline will be displayed. Value programmed is one less than the scan line desired.

B.4.13 End Vertical Blanking Register (Index = 16)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Identical to End Vertical Blanking Register Bits (4:0) definition in the VGA section.

B.4.15 Mode Control Register (Index = 17)

Bits (7:5)

EGA: Same as Mode Control Register Bits (7:5) definition in the VGA section.

Bit 4

EGA: Not used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

B.5 GRAPHICS CONTROLLER REGISTERS (PORT 3CF)

B.5.1 Read Map Select Register (Index = 04)

Bits (7:3)

EGA: Not Used.

Bits (2:0)

EGA: Map selected bits (2:0) which represent encoded value of the memory plane in binary as shown below:

D2	D1	D0	MAP SELECTED
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

B.5.2 Mode Register (Index = 05)

Bit (7:6)

EGA: Not Used.

Bits (5:2)

EGA: Identical to Mode Register Bits (5:2) definition in the VGA section.

Bits (1:0)

EGA: Binary coded write bits define the write modes per table below:

BIT 1	BIT 0	FUNCTION
0	0	Write mode 0 - Refer to earlier section
0	1	Write mode 1 - Refer to earlier section
1	0	Write mode 2 - Refer to earlier section
1	1	Write mode 3 - Not Legal. Selects write mode 1.

B.6 ATTRIBUTE CONTROLLER REGISTERS (PORTS = 3C0/3C1)

Palette Registers (Index = 00 through 0F)

Bits (7:6)

EGA: Not Used.

Bits (5:0)

EGA: Dynamic color selection. Logic 0 = Color deselection, and Logic 1 = color selection per the table below:

BITS	COLOR	PIXEL
5	Sec. Red	VID 5
4	Sec Green/Inten	VID 4
3	Sec Blue/Mono	VID 3
2	Red	VID 2
1	Green	VID 1
0	Blue	VID 0

B.6.1 Mode Control Register (Index = 10)

Bits (7:4)

EGA: Not Used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

B.6.2 Overscan Color Register (Index = 11)

Bits (7:6)

EGA: Not Used.

Bits (5:0)

EGA: Overscan color for the border. For a monochrome display, set all the six bits to logic 0. The border color is defined by the color table for the Palette registers shown above.

B.6.3 Color Plane Enable Register (Index = 12)

Bits (7:6)

EGA: Same as Color Plane Enable Register Bits (7,6) in the VGA section.

Bits (5:4)

EGA:
Determines two of six colors for the Video Status Multiplexer according to the table below.

BIT 5	BIT 4	INPUT STATUS REGISTER 1 (Port 3?A)	
		BIT 5	BIT 4
0	0	VID 2(Red)	VID 0 (Blue)
0	1	VID 5(SRed)	VID 4 (SGreen)
1	0	VID 3(SBlue)	VID 1 (Green)
1	1	VID 5(SRed)	VID 4 (SGreen)

Bits (3:0)

EGA: Same as Color Plane Enable Register Bits (3:0) definition in the VGA section.

B.6.4 Horizontal PEL Panning Register (Index = 13)

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: These four bits determine the horizontal left shift of the video data in number of pixels. In monochrome alpha numeric modes, a 9-dots/character image can be shifted by 9 pixels. For all other graphics or alpha numeric modes, a maximum left shift of 8 pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section.

B.7.0 Monitor Detection

The DAC output currents I_{RED}, I_{GREEN}, and I_{BLUE}, develop a voltage across the load resistances R_{LD}. These voltages are sent to comparitors against a voltage derived from the external voltage reference V_{REF}. The output current is determined by the formula:

$$I = \frac{\text{code} \times 04}{R_{SET}} \times V_{REF}$$

where the codes range from 0 to 63 (0H to 3FH) for a 6-bit DAC.

The output signal MDETECT is readable at port 3C2H bit 4. It is important to read during active video ouput, not duing retrace or any other blanking period.

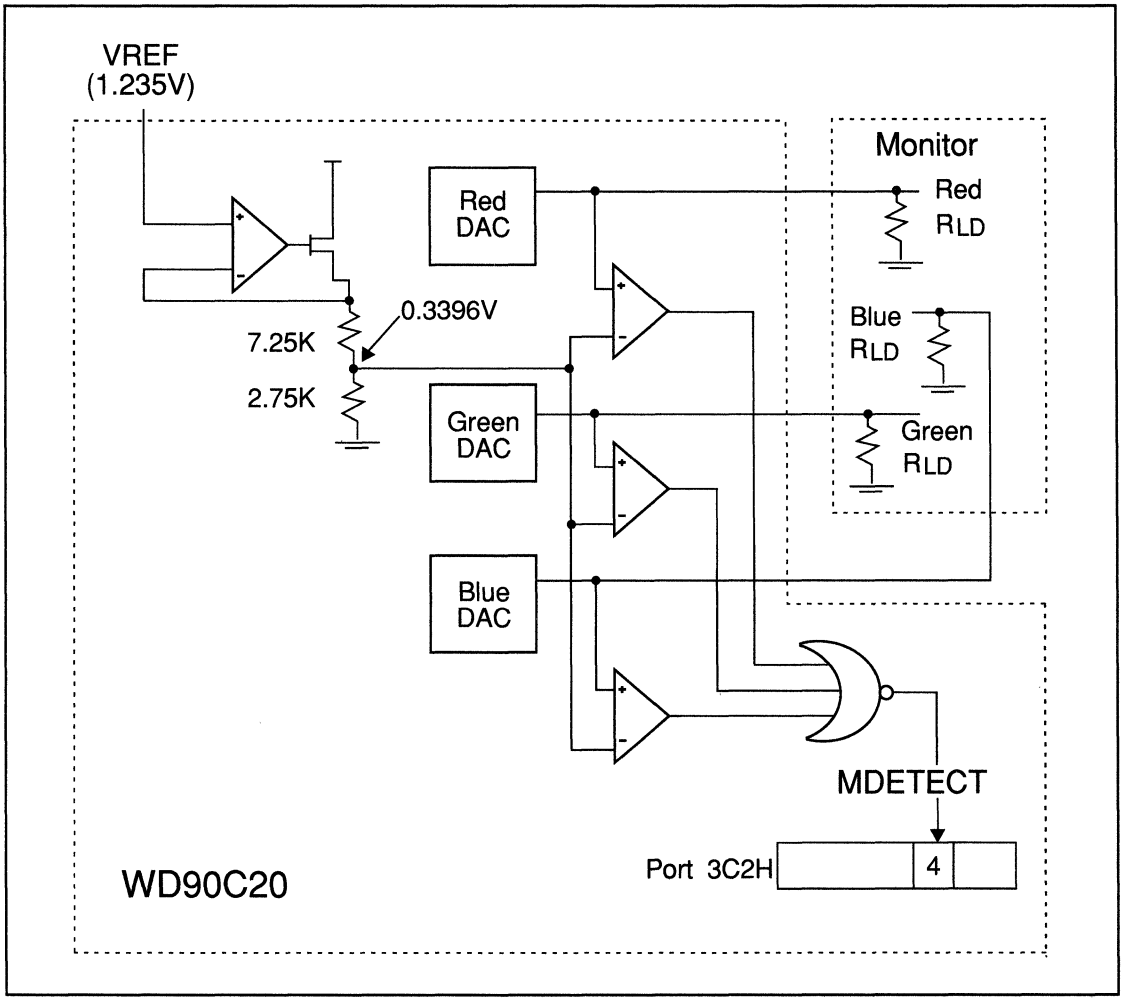


FIGURE B-1. MONITOR DETECTION

APPENDIX

C.1 AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

TABLE C-2. TIMING DIAGRAMS

FIGURE NUMBER	TITLE
C-1	I/O Write – Micro Channel Mode
C-2	Memory Read – AT Mode
C-3	I/O Read – Micro Channel Mode
C-4	Memory Write – Micro Channel Mode
C-5	Memory Read – Micro Channel Mode
C-6	CPU Read Non-Page Mode, CRT Read
C-7	CPU with Non-Page Mode
C-8	DRAM Page Mode Read Timing
C-9	WD90C20 LCD Timing (t = VCLK)
C-10	I/O Write – AT Mode
C-11	I/O Read – AT Mode
C-12	Memory Write – AT Mode

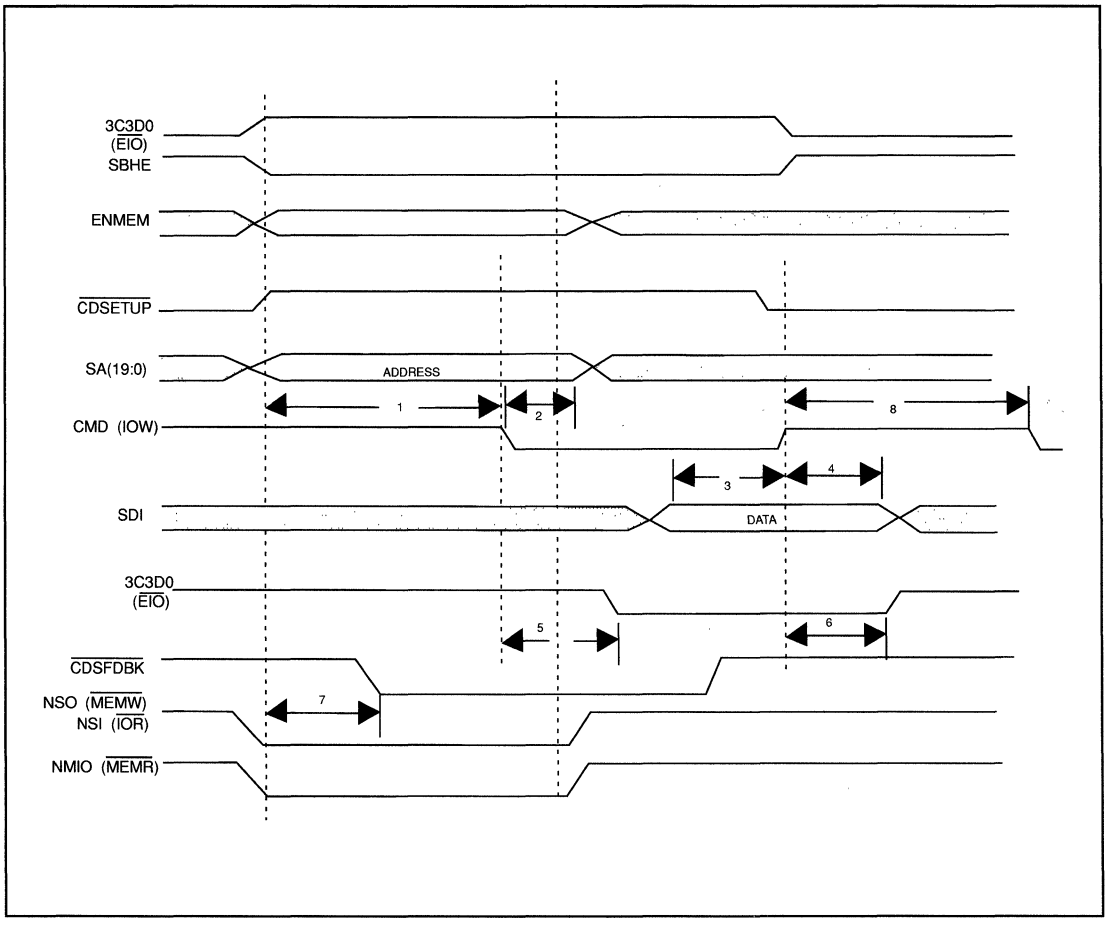


FIGURE C-1. I/O WRITE – MICRO CHANNEL MODE

I/O WRITE – MC MODE			MIN.	TYP.
1. SA(19:0), NS0, NS1	setup to	↓CMD	15	
2. SA(19:0), NS0, NS1	hold from	↓CMD	10	
3. Write data SDI	setup to	CMD Inactive	30	
4. Write data SDI	hold from	CMD Inactive	5	
5. WPLT	active from	CMD Active		29
6. WPLT	inactive from	CMD Inactive		22
7. CDSFDBK	active from	Address Valid	15	

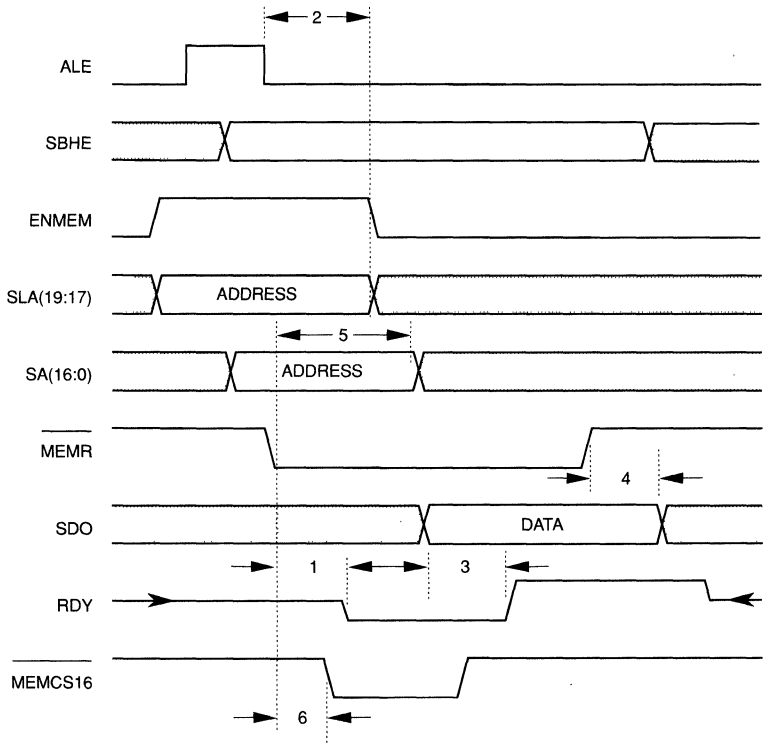


FIGURE C-2. MEMORY READ – AT MODE

I/O WRITE – AT MODE			MIN.	TYP.	MAX.
1. RDY	inactive from	$\overline{\text{MEMR}}$ active (max. worst case delay)	25		
2. SLA(19:17), ENMEM	min. hold from	ALE↓	5		
3. Data SDO	valid setup to	RDY (min. setup time)	0		30
4. Data SDO	hold from	$\overline{\text{MEMR}}$ (min. hold time)	10		
5. SA(16:0)	hold from	$\overline{\text{MEMR}}$ active	10		
6. $\overline{\text{MEMCS16}}$	valid from	SLA(19:17) ENMEM valid	9	143	

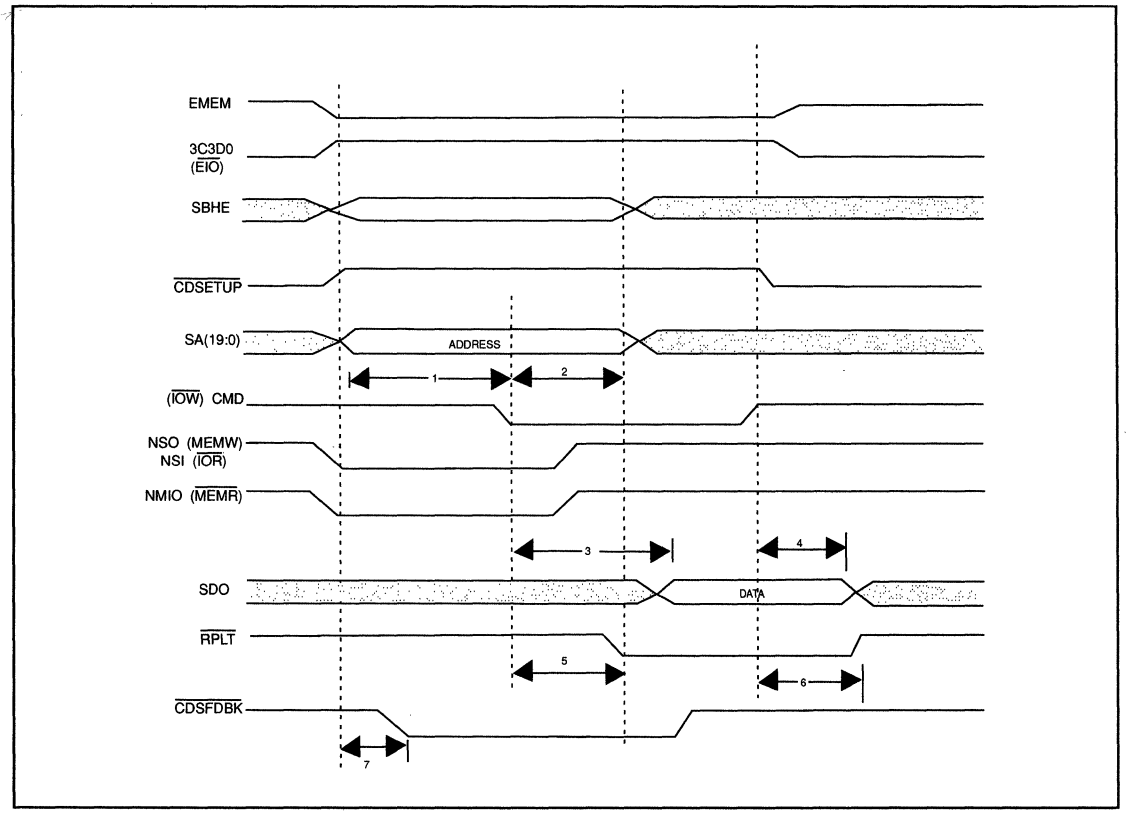


FIGURE C-3. I/O READ – MICRO CHANNEL MODE

I/O READ MC MODE			MIN.	TYP.	MAX.
1. SA(19:0), NS0, NS1	setup to	↓CMD	15		
2. SA(19:0), NS0 NS1	hold from	↓CMD	10		
3. Read data SDO	valid from	CMD active (max. worst case delay)	60		
4. Read data SDO	hold from	CMD inactive (min. delay)	10		
5. RPLT	active from	CMD Active (max. worst case delay)		29	
6. RDLT	inactive from	CMD Inactive (max. worst case delay)		22	
7. CDSFDBK	active from	Address Valid	15		

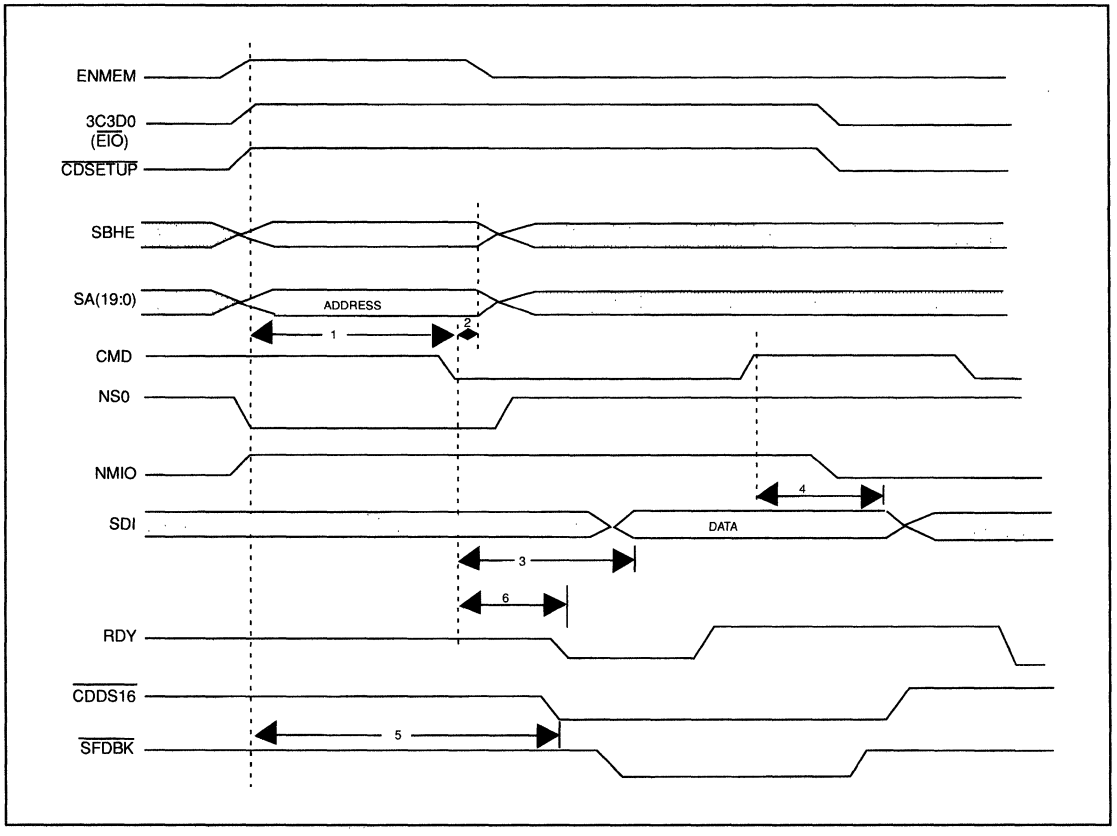


FIGURE C-4. MEMORY WRITE – MICRO CHANNEL MODE

MEMORY WRITE MC MODE			MIN.	TYP.	MAX.
1. SA(19:0), NS0, NS1	setup to	↓CMD	15		
2. SA(19:0), NS0 NS1	hold from	↓CMD	10		
3. Data SDI	valid from	CMD Active (min.)	25		
4. Data SDI	hold from	CMD Inactive (min.)	0		
5. $\overline{\text{CDDS16}}$	valid from	SA(19:0) ENMEM	9	14	
6. RDY	inactive from	CMD active	25		

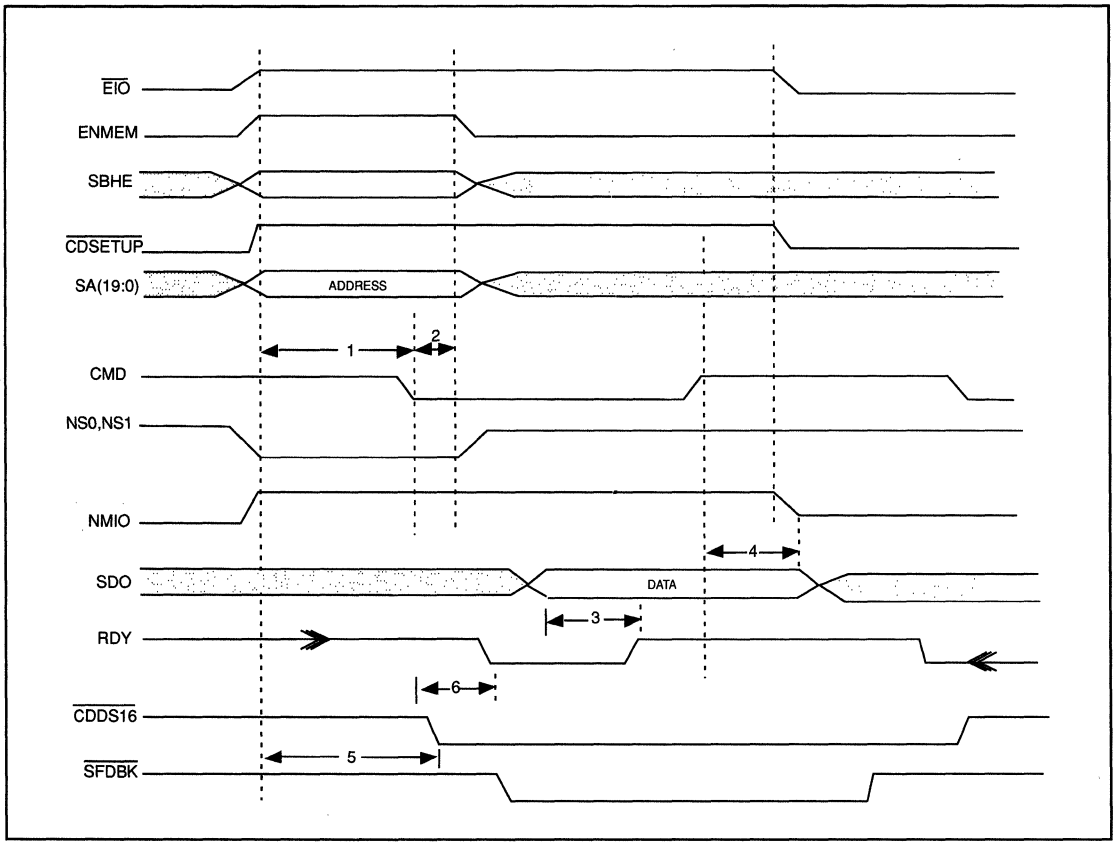


FIGURE C-5. MEMORY READ – MICRO CHANNEL MODE

MEMORY WRITE MC MODE			MIN.	TYP.	MAX.
1. SA(19:0), NS0, NS1	setup to	↓CMD	15		
2. SA(19:0), NS0 NS1	hold from	↓CMD	10		
3. Read data SDO valid	setup to	RDY (min. setup time)	0		30
4. Read data SDO	hold from	CMD Inactive (min. hold time)	10		
5. CDDS16	valid from	SA(19:0) ENME	9	14	
6. RDY	Inactive from	CMD active	25		

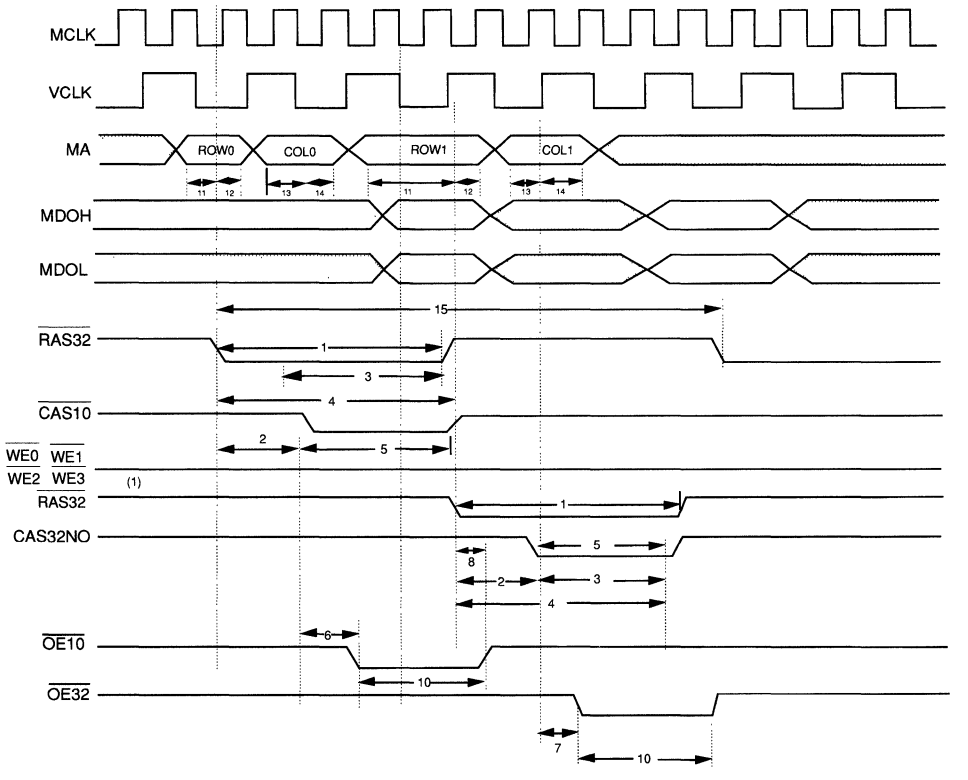


FIGURE C-6. CPU READ NON-PAGE MODE, CRT READ

CPU READ AND CRT READ, NON-PAGE MODE		MCLK = 45.046 MHz	
1. $\overline{\text{RAS10}}$ ($\overline{\text{RAS32}}$)	pulse width low		103
2. $\overline{\text{RAS10}}$ ($\overline{\text{RAS32}}$)	low to	$\overline{\text{CAS10}}$ ($\overline{\text{CAS32}}$) (low)	365
3. $\overline{\text{CAS10}}$ ($\overline{\text{CAS32}}$)	low to	$\overline{\text{RAS10}}$ ($\overline{\text{RAS32}}$) (high)	66
4. $\overline{\text{RAS10}}$ ($\overline{\text{RAS32}}$)	low to	$\overline{\text{CAS10}}$ ($\overline{\text{CAS32}}$) (high)	103
5. $\overline{\text{CAS10}}$ ($\overline{\text{CAS32}}$)	pulse width low		66
6. $\overline{\text{OE10}}$ low	setup to	$\overline{\text{CAS10}}$ low	21
7. $\overline{\text{OE32}}$ low	setup to	$\overline{\text{CAS32}}$ low	22.5
8. $\overline{\text{OE10}}$ high	after	$\overline{\text{CAS10}}$ high	22.5

CPU READ AND CRT READ, NON-PAGE MODE		**MCLK = 45.046 MHz**	
9. $\overline{OE32}$ high	after	$\overline{CAS10}$ high	22
10. OE	pulse width		66.5
11. Row address	setup to	$\overline{RAS10}$, $\overline{RAS32}$ (low)	
12. Row Address	hold from	$\overline{RAS10}$, $\overline{RAS32}$ (low)	
13. Column Address	setup to	$\overline{CAS10}$, $\overline{RAS32}$ (low)	
14. Column Address	hold from	$\overline{CAS10}$,$\overline{CAS32}$ (low)	
15. Random Read Cycle			

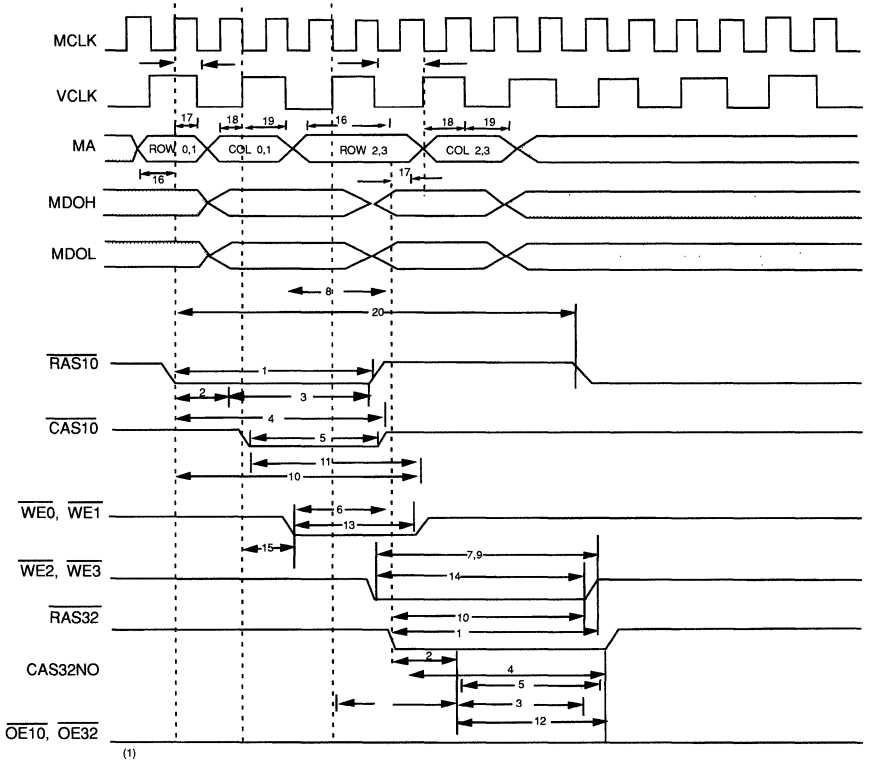


FIGURE C-7. CPU WITH NON-PAGE MODE

CPU WRITE	MCLK = 45.046 MHz		
1. RAS10 (RAS32)	pulse width low		103
2. RAS10 (RAS32)	low to	CAS10 (CAS32) (low)	365
3. CAS10 (CAS32)	low to	RAS10 (RAS32) (high)	66
4. RAS10 (RAS32)	low to	CAS10 (CAS32) (low)	103
5. CAS10 (CAS32)	pulse width low		66
6. WE low	setup to	CAS10	50.5
7. WE low	setup to	CAS32 high	103.5
8. WE low	setup to	RAS10 high	50.5
9. WE low	setup to	RAS32 high	103.5
10. WE high	hold after	RAS10, RAS32	118
11. WE high	hold after	CAS10low	121.5

CPU WRITE	**MCLK = 45.046 MHz**		
12. WE high	hold after	$\overline{CAS32}$ low	109.5
13. $\overline{WE0}$, $\overline{WE1}$	pulse duration		66
14. $\overline{WE3}$, $\overline{WE2}$	pulse duration		109.5
15. $\overline{WE0}$, $\overline{WE1}$	low from	$\overline{CAS10}$ low	15.5
16. Row address	setup to	$\overline{RAS10}$, $\overline{RAS32}$ (low)	10
17. Row address	hold from	$\overline{RAS10}$, $\overline{RAS32}$	
18. Column address	setup to	$\overline{CAS10}$, $\overline{RAS32}$ (low)	
19. Column address	hold from	$\overline{CAS10}$, $\overline{CAS32}$ (low)	
20. Random Write Cycle			198

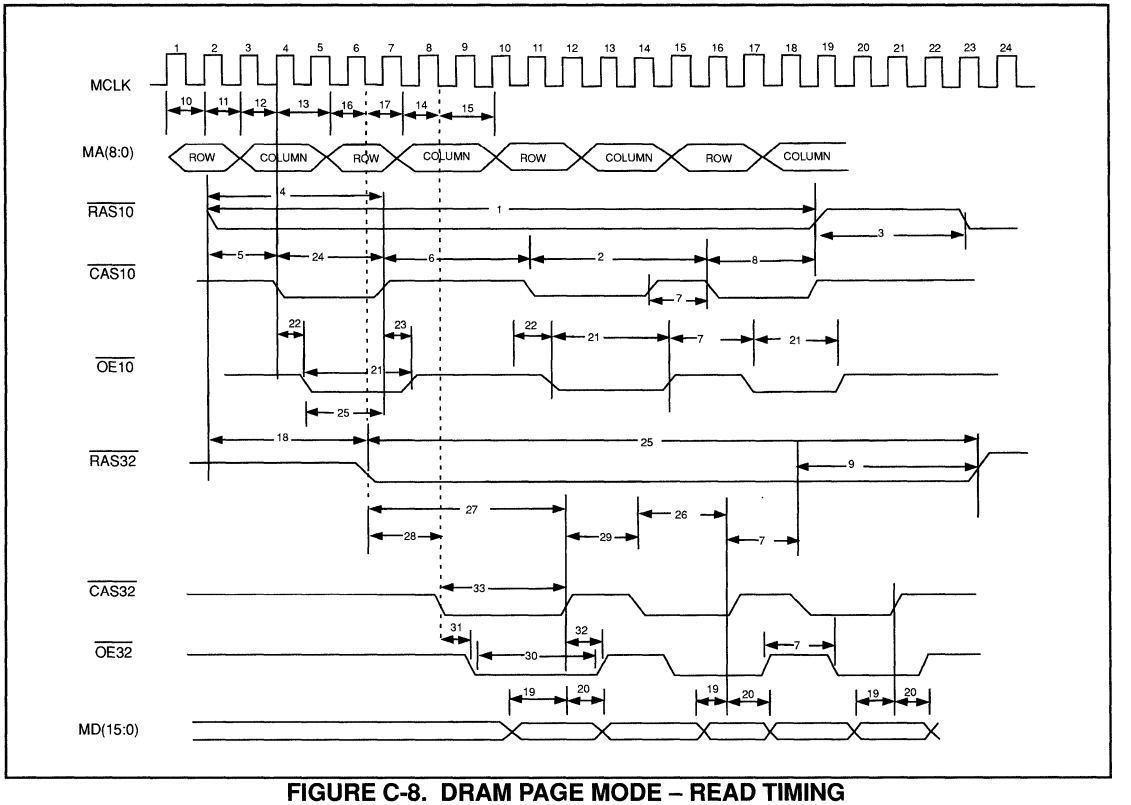


FIGURE C-8. DRAM PAGE MODE – READ TIMING

PAGE MODE READ ACCESSES **MCLK = 45.046 HHz**	
1. $\overline{\text{RAS10}}$ pulse duration	370.2
2. Page mode cycle time $\overline{\text{CAS10}}$ low to CAS low	111
3. $\overline{\text{RAS10}}$ Precharge	96
4. $\overline{\text{RAS10}}$ low to $\overline{\text{CAS10}}$ high (first)	101.6
5. $\overline{\text{RAS10}}$ low to $\overline{\text{CAS10}}$ low	35.6
6. First $\overline{\text{CAS10}}$ pulse width high	89.4
7. $\overline{\text{CAS10}}$ pulse width high	45
8. $\overline{\text{CAS10}}$ low to $\overline{\text{RAS10}}$ high	67.8
9. $\overline{\text{CAS32}}$ low to $\overline{\text{RAS32}}$ high	112.4
10. Row address setup to $\overline{\text{RAS10}}$ low	22
11. Row address hold from $\overline{\text{RAS10}}$ low	22
12. Column address setup to $\overline{\text{CAS10}}$ low	108
13. Column address hold from $\overline{\text{CAS10}}$	22
14. Column address setup to $\overline{\text{CAS32}}$	8

PAGE MODE READ ACCESSES MCLK = 45.046 HHz	
15. Column address hold from $\overline{CAS32}$ low	22
16. Row address setup to $\overline{RAS23}$ low	8
17. Row address hold from $\overline{RAS32}$ low	22
18. $\overline{RAS32}$ low from $\overline{RAS10}$ low	100.4
19. Read data setup to CAS high	–
20. Read data hold from CAS high	–
21. $\overline{OE10}$ pulse width low	66.4
22. $\overline{OE10}$ low after CAS10 low	21.3
23. $\overline{OE10}$ high after CAS10 high	21.8
24. $\overline{CAS10}$ pulse width low	66
25. $\overline{RAS32}$ pulse duration	369.0
26. Page mode cycle time $\overline{CAS32}$ low to CAS low	110.4
27. $\overline{RAS32}$ low to $\overline{CAS32}$ high (first)	101.1
28. $\overline{RAS32}$ low to $\overline{CAS32}$ low	35.7
29. First $\overline{CAS32}$ pulse width high	45
30. $\overline{OE32}$ pulse width low	66.0
31. $\overline{OE32}$ low after $\overline{CAS32}$	21.2
32. $\overline{OE32}$ high after $\overline{CAS32}$ high	21.8
33. $\overline{CAS32}$ pulse width low	64.4

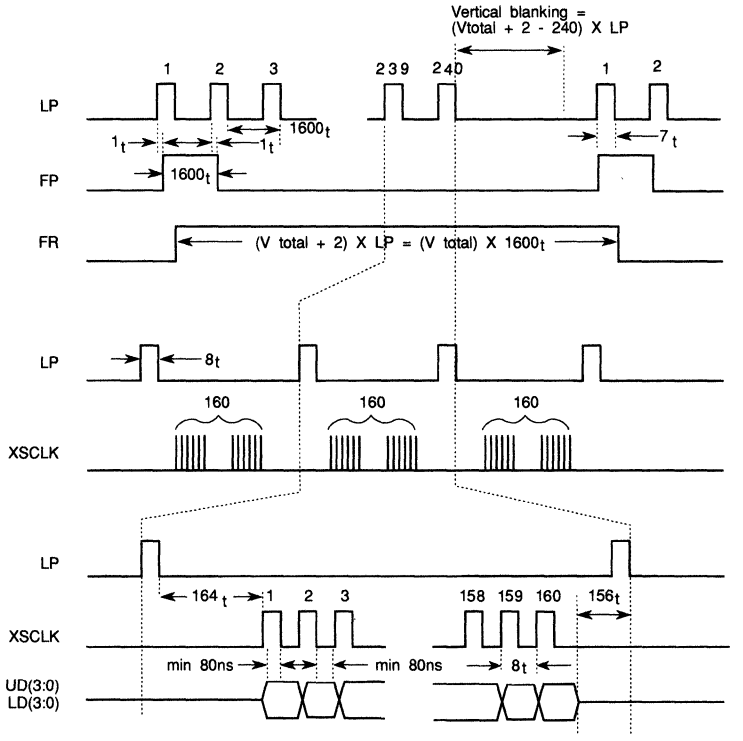


FIGURE C-9. WD90C20 LCD TIMING DIAGRAM (t = VCLK)

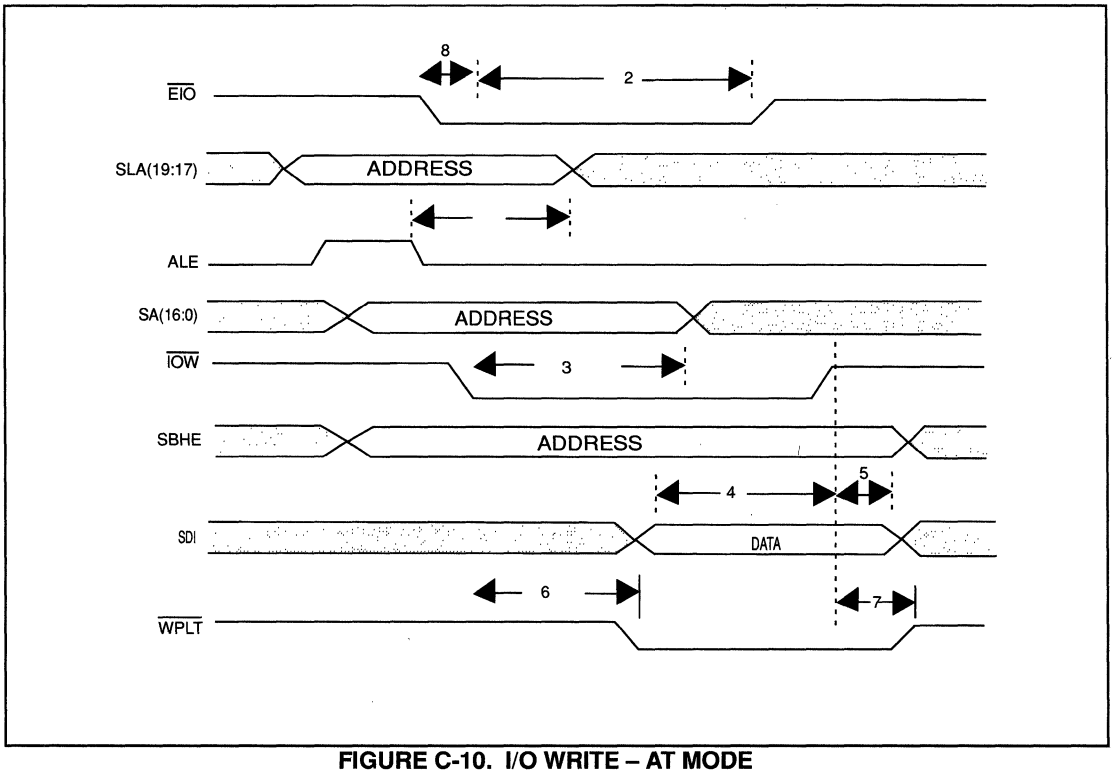


FIGURE C-10. I/O WRITE – AT MODE

I/O WRITE AT MODE			MIN.	TYP.	MAX.
1. SLA(19:17)	hold from	ALE inactive	5		
2. EIO	hold from	IOW active (low)	10		
3. SA(16:0)	hold from	IOW active (low)	10		
4. Write Data SDI	setup to	IOW inactive (high)	30		
5. Write Data SDI	hold from	IOW inactive (high)	5		
6. WPLT	active from	IOW Active (max. worst case delay)		29	
7. WPLT	inactive from	IOW inactive (max. worst case delay)		22	
8. EIO, SA(16:0)	setup to	IOW active (low)	15		

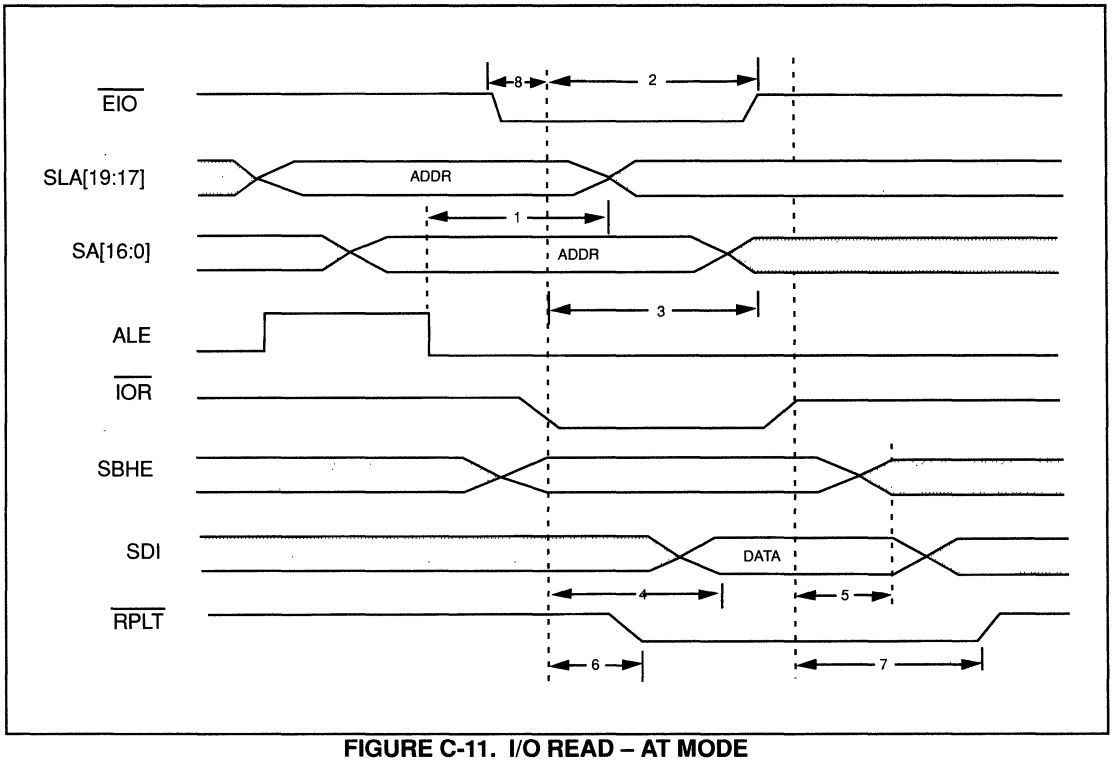


FIGURE C-11. I/O READ – AT MODE

I/O READ AT MODE			MIN.	TYP.	MAX.
1. SLA(19:17)	hold from	ALE inactive	5		
2. EIO	hold from	IOR active (low)	10		
3. SA(16:0)	hold from	IOR active (low)	10		
4. Read Data SDO	valid from	IOR active (low; max. worst case delay)	60		
5. Read Data SDO	hold from	IOR inactive (min. delay)	10		
6. RPLT	active from	IOR active		29	
7. RPLT	inactive from	IOR inactive		22	
8. EIO, SA(16:0)	setup to	IOR active (low)	15		

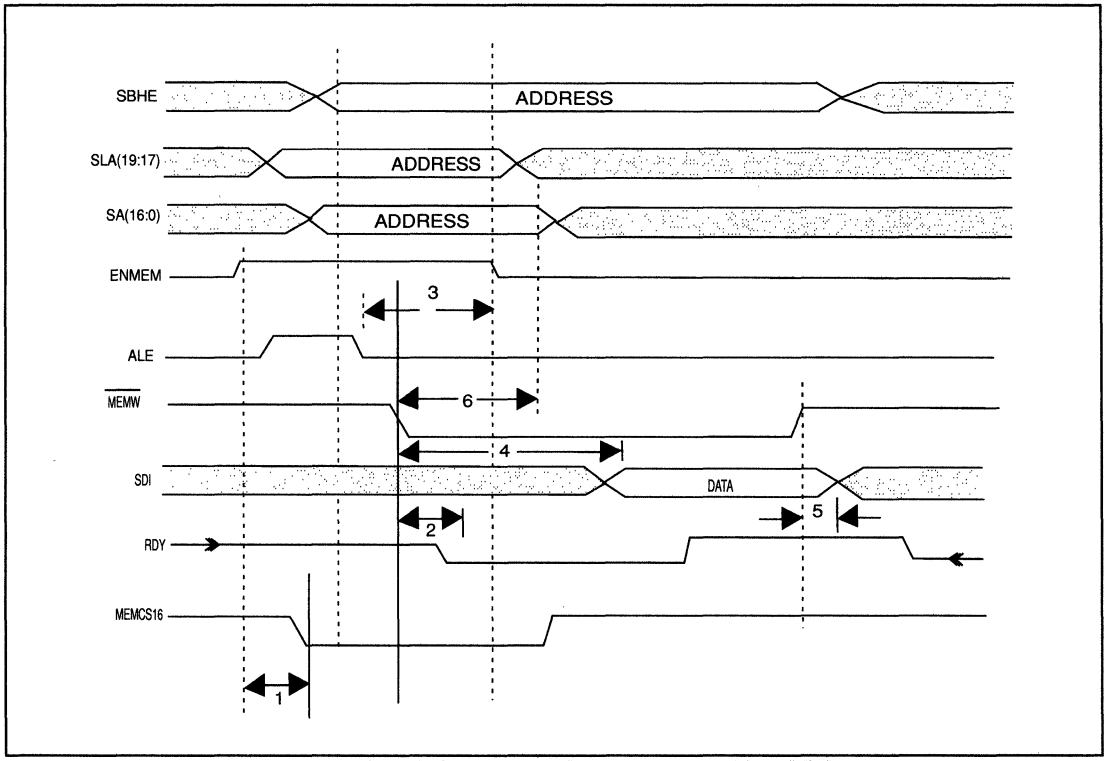


FIGURE C-12. MEMORY WRITE – AT MODE

MEMORY WRITE AT MODE			MIN.	TYP.	MAX.
1. $\overline{\text{MEMCS16}}$	valid from	SLA (19:17) ENMEM valid (max. worst case delay)	9	14	
2. RDY	inactive from	$\overline{\text{MEMW}}$ active (max. worst case delay)	0		30
3. SLA(19:17) ENMEM	min. hold from	ALE↓	5		
4. Data SDI	valid from	MEMWM active (min.)	30		
5. Data SDI	hold from	MEMWM inactive (min.)	5		
6. SA(16:0)	hold from	MEMWM active	10		

APPENDIX

23

D.1 PACKAGE DIMENSIONS AND SPECIFICATIONS

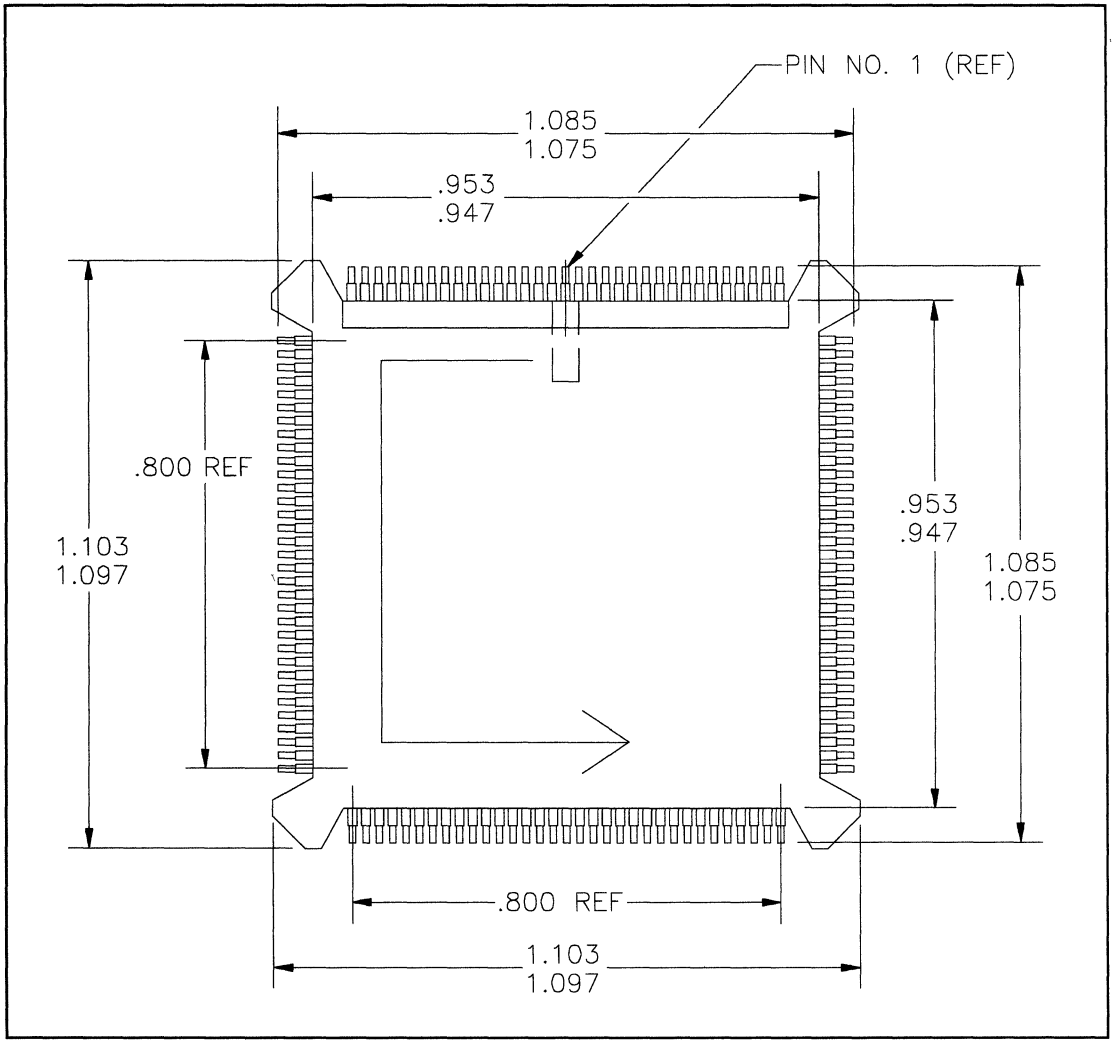
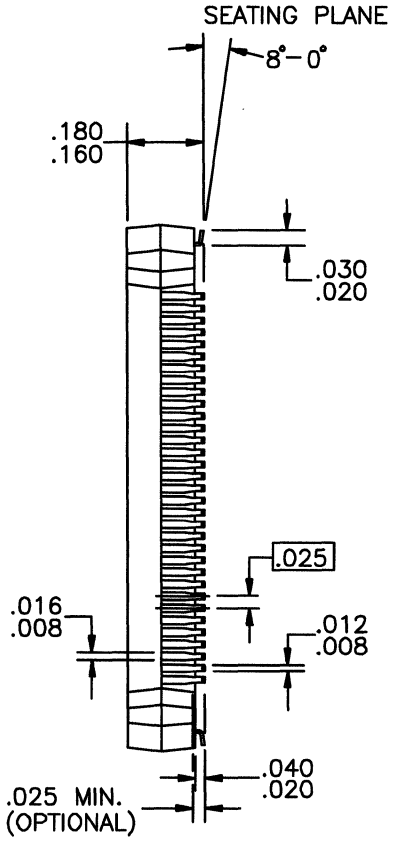
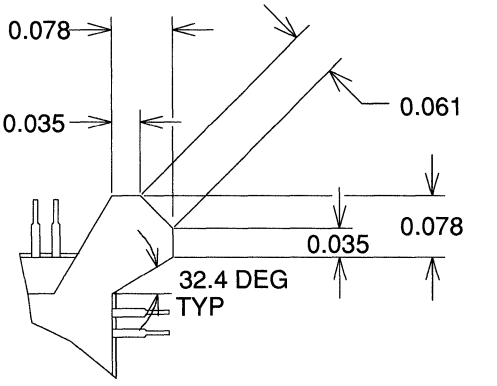


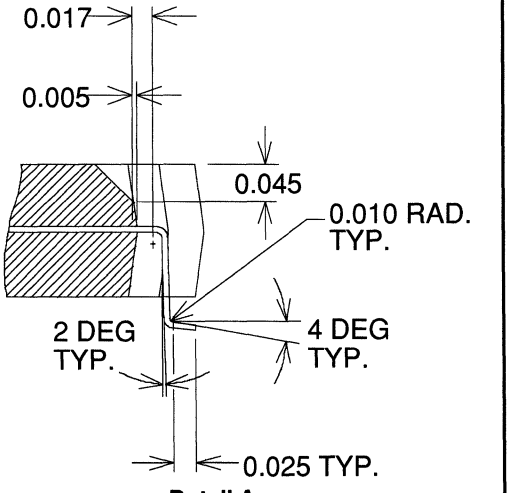
FIGURE D-1. 132 PIN JEDEC PLASTIC FLAT PACKAGE



Side View



Bumper Detail



Detail A

FIGURE D-1. 132 PIN JEDEC PLASTIC FLAT PACKAGE (continued)

APPENDIX

E.1 ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0°C to 70°C
Storage temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to Vss	-0.3 to 6.5 Volts
Power dissipation	1.2 Watts

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

E.1.1 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to Vss (0V Ground). Positive current flows into the referenced pin.

Operating temperature range	0° to 70°C
Power supply voltage	4.00 to 4.60 Volts

E.1.2 DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS	NOTES
V_{IL}	Input Low Voltage	-0.3	0.8	V	V_{CC} = 5V ± 5%	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	V_{CC} = 5V ± 5%	
I_{IL}	Input Low Current	–	± 10	µA	V_{IN} = 0V	
I_{IH}	Input High Current	–	± 10	µA	V_{IN} =V_{CC}	
V_{OL}	Output Low Voltage	–	0.4	V	I_{OL} + 4.0 mA	1
V_{OH}	Output High Voltage					
I_{OZ}	High Impedance	2.4	–	V	I_{OH} = 4.0 mA	1
	Leakage Current	-10.0	10.0	µA	OV < V_{OUT} <V_{CC}	
C_{IN}	Input Capacitance	–	10	pF	PC = 1 MHz	
C_{OUT}	Output Capacitance	–	10	pF	PC = 1 MHz	

NOTES:

1. WD90C20 outputs have 6.0 mA maximum source and sink capability except as follows:
   RDY = 24.0 mA sink and 4.0 mA source.
   IRQ = 24.0 mA sink and 4.0 mA source.

WD90C61

(PCLK2) Video

Graphics Array Clock

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

The Western Digital® Imaging WD90C61 is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, the other is the video dot clock.

The WD90C61 Video Graphics Array clock generator is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with every Western Digital Imaging Video Graphics Array device to optimize video subsystem performance.

The video dot clock output may be one of six internally generated frequencies or one of two external inputs. The selection of the video dot clock frequency is done through four inputs: VSEL0, VSEL1, VGA/TTL, and FCLKSEL. The video clock selection is latched by the SELEN signal. See Table 1 below.

The inputs and truth table have been designed to allow a direct connection to one of the many Western Digital Imaging VGA controllers. When a Western Digital Imaging controller is used with a WD90C61, two of the VGA's video clock inputs become outputs and directly drive the SELEN and VGA/TTL inputs.

The WD90C61 generates the VCLK output as shown in Table 1. The VSEL0 and VSEL1 inputs are latched with SELEN. VGA/TTL is an additional select input that selects frequencies for VGA modes when left high and frequencies for TTL modes when pulled low. Select input FCLKSEL overrides internal clock generation and passes through the FCLKIN clock input.

The MCLK output is generated as shown in Table 2. The various VCLK and MCLK frequencies are achieved by multiplying the 14.318 MHz input frequency by a factor of N/32 (e.g., 44.74 is obtained with N = 100).

The VCLKEN and MCLKEN inputs can tri-state the VCLK and MCLK outputs to facilitate board level testing. External filter components are attached to the MCAP and VCAP pins for the internal phase lock loops.

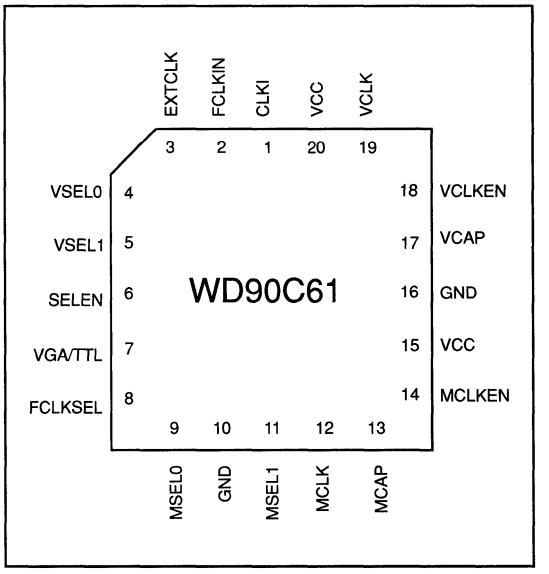


FIGURE 1. WD90C61 PIN DIAGRAM

This data book supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

1.1 FEATURES

- Clock generator for the IBM compatible Western Digital Imaging Video Graphics Array (VGA) chips.
- Generates six video clock frequencies (25.057, 28.189, 36.242, 16.108, 32.216 and 44.744 MHz) derived from a 14.318 MHz system clock reference frequency.
- On-chip generation of four (36.242, 41.612, 37.586 and 44.744 MHz) memory clock frequencies.
- Video clock is selectable among the six internally generated clocks and two external clocks.
- CMOS technology.
- Available in a 20-pin PLCC package.

VCLKEN	FCLKSEL	VGA/TTL	VSEL0	VSEL1	SELEN†	VCLK FREQUENCY
Open	1 or Open	1 or Open	0	0	↑	25.057 MHz
Open	1 or Open	1 or Open	0	1	↑	28.189 MHz
Open	1 or Open	1 or Open	1	0	↑	EXTCLK pass-through
Open	1 or Open	1 or Open	1	1	↑	36. 242 MHz
Open	1 or Open	0	0	0	↑	14.318 MHz
Open	1 or Open	0	0	1	↑	16.108 MHz
Open	1 or Open	0	1	0	↑	32.216 MHz
Open	1 or Open	0	1	1	x	44.744 MHz
Open	0	x	x	x	x	FCLKIN pass-through

TABLE 1. VCLK SELECTION

† rising edge for SELEN (↑)

MCLKEN	MSEL0	MSEL1	MCLK FREQUENCY
Open	1 or Open	1 or Open	44.744 MHz
Open	1 or Open	0	37.585 MHz
Open	0	1 or Open	36.242 MHz
Open	0	0	41.612 MHz
0	x	x	DISABLED

TABLE 2. MCLK SELECTION

2.0 WD90C61 INTERFACE

The WD90C61 has three system interfaces: System Bus, Feature Connector and VGA Controller, as well as analog filters and four user programmed inputs. Figure 2 shows how the Western Digital Imaging VGA Clock WD90C61 is connected to a VGA controller. Western Digital Imaging VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs VCLK1 and VCLK2 to outputs. These outputs are used to select the required video clock frequency.

2.1 SYSTEM BUS INPUTS

The system bus inputs are listed below:

- CLKI
- VSEL0
- VSEL1

The WD90C61 uses the 14 MHz system bus clock as a reference to generate all its frequencies for both video and memory clocks. Address lines D2 and D3 are also commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

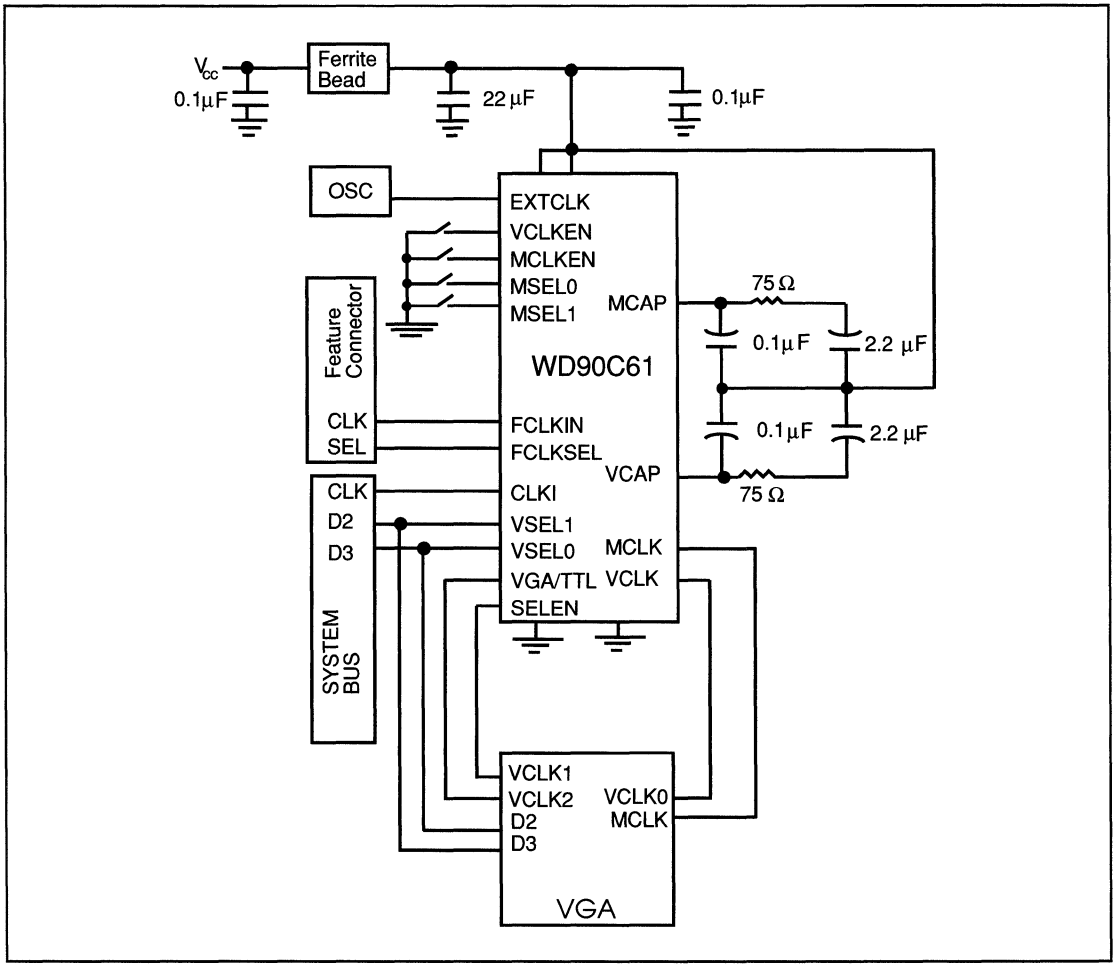


FIGURE 2. WD90C61 INTERFACE

2.2 SYSTEM BUS OUTPUTS

None

2.3 VGA CONTROLLER INPUTS

The VGA controller inputs are listed below:

- VGA/TTL
- SELEN

The WD90C61 is programmed to generate different video clock frequencies using the inputs of VSEL0, VSEL1, and VGA/TTL. The signal VGA/TTL may be supplied by the VGA controller as is the case in Western Digital Imaging VGA controllers. The inputs VGA/TTL, VSEL0, and VSEL1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital Imaging VGA controllers during I/O writes to 3C2H.

2.4 VGA CONTROLLER OUTPUTS

The VGA controller outputs are listed below:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

2.5 FEATURE CONNECTOR INPUTS

The feature connector inputs are listed below:

- FCLKIN
- FCLKSEL

There are two inputs from the feature connector: FCLKIN and FCLKSEL. FCLKIN may be used as an alternate video clock. FCLKIN becomes the selected video clock if FCLKSEL goes low.

2.6 FEATURE CONNECTOR OUTPUTS

None

2.7 ANALOG FILTERS

The analog filters are lsited below:

- MCAP
- VCAP

These connections are for the analog filters. The component values of the filters are critical. Care must be taken to ensure proper values over the entire operating range desired for the final product. Figure 2 shows the filter circuit. The capacitator tolerances are ± 20%. The resistor tolerance is 2%.

2.8 USER DEFINEABLE INPUTS

The user defineable inputs are listed below:

- EXTCLK
- VCLKEN
- MCLKEN
- MSEL0
- MSEL1

EXTCLK is an additional input that may be routed to the VCLK0 output. This additional input is useful for supporting modes that require frequencies not provided by the WD90C61. VCLKEN and MCLKEN are the output enable signals for VCLK and MCLK.

MSEL0 and MSEL1 are the memory clock (MCLK) select lines. Table 2 shows how MCLK frequencies are selected. All signals in this group have internal pullup resistors.

3.0 WD90C61 FUNCTIONAL BLOCK DIAGRAM

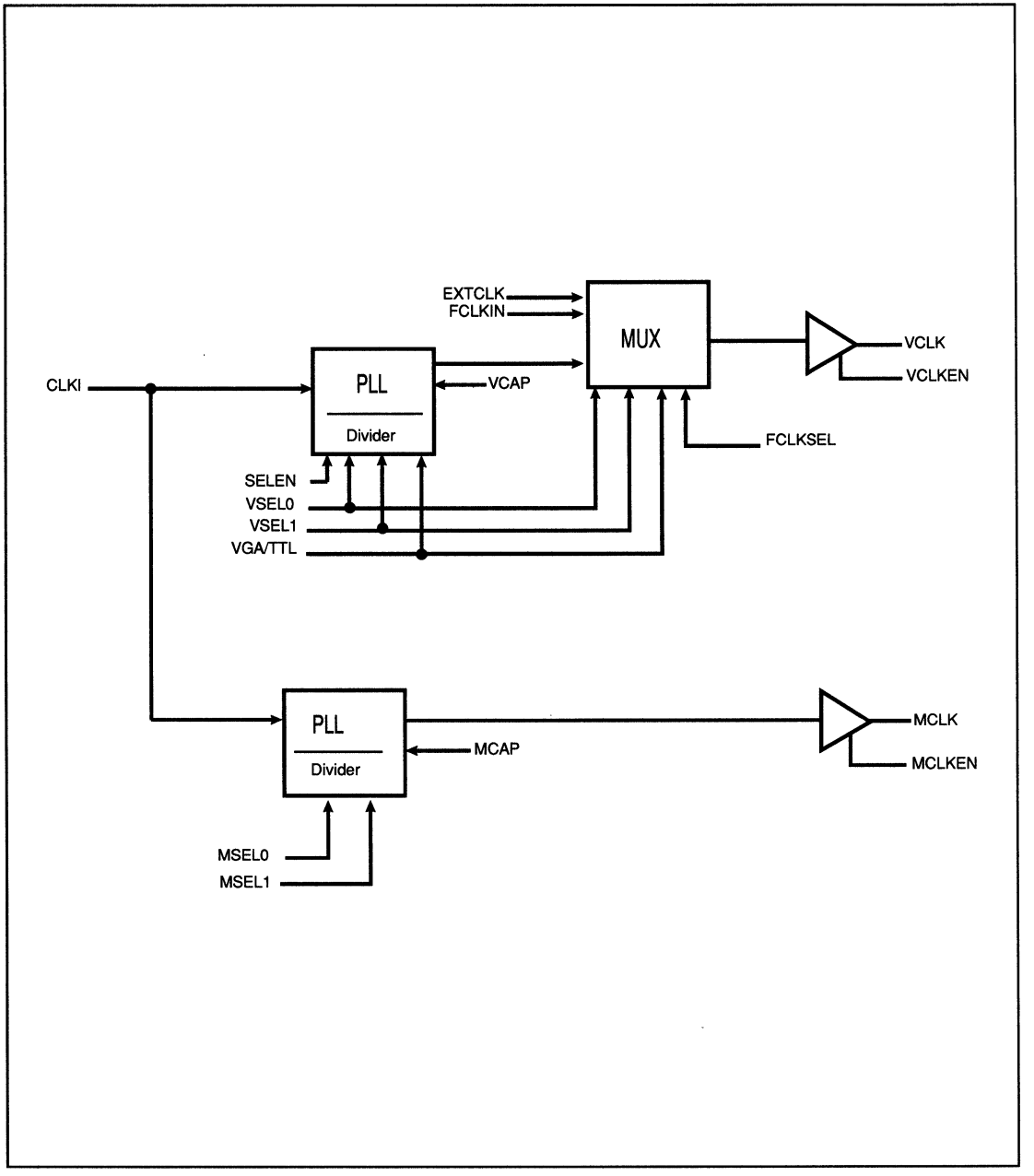


FIGURE 3. WD90C61 FUNCTIONAL BLOCK DIAGRAM

4.0 PIN DESCRIPTION

The following table provides the pin definitions for the 20-pin WD90C61 package.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
1	CLKI	IN	Reference Input Clock from system (14.318MHz)
2	FCLKIN	IN	Clock input from Feature Connector
3	EXTCLK	IN	External Clock input for an additional frequency
4	VSEL0	IN	Control Input for VCLK selection
5	VSEL1	IN	Control Input for VCLK selection
6	SELEN	IN	Strobe for latching SEL0 and SEL1
7	VGA/TTL	IN	Select input for VCLK selection
8	FCLKSEL	IN	Select input for VCLK. When pulled low, passes through FCLKIN
9	MSEL0	IN	Select input for MCLK selection
10	GND	---	Ground for digital circuit
11	MSEL1	IN	Select input for MCLK selection
12	MCLK	OUT	Memory Clock (MCLK) output
13	MCAP	IN	External filter connection for MCLK generation
14	MCLKEN	IN	Enable input for MCLK output. When pulled low, tri-states MCLK
15	VCC	---	Power supply for analog circuit
16	GND	---	Ground for analog circuit
17	VCAP	IN	External filter connection for VCLK generation
18	VCLKEN	IN	Enable input for VCLK output. When pulled low, tri-states VCLK
19	VCLK	OUT	Video Clock (VCLK) output
20	VCC	---	Power supply for digital circuit

TABLE 3. PIN DESCRIPTIONS

NOTE
CLKI, FCLKIN, EXTCLK, VSEL0, VSEL1, SELEN, VGA/TTL, FCLKSEL, MSEL0, MSEL1, MCLKEN, VCLKEN input pins have internal pull-up resistance.

5.0 ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0°C to 70°C
Storage temperature	-40° C to 125° C
Voltage on all inputs and outputs with respect to V_{SS}	0.5 to 7 Volts

NOTE
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

5.1 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating temperature range	0° to 70° C
Power supply voltage	4.75 to 5.25 Volts

5.2 D.C . CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	VCC = 5V
V_{IH}	Input High Voltage	2.0	VCC	V	VCC = 5V
I_{IH}	Input Leakage Current	---	20	µA	$V_{IN} = V_{CC}$
V_{OL}	Output Low Voltage	---	0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output High Voltage	2.4	---	V	I_{OH} = 4.0 mA
I_{CC}	Supply Current	---	30	mA	V_{CC} = 5V
R_{UP}	Internal Pullup Resistors	25	---	KOhm	VCC = 5V
Cin	Input Pin Capacitance	---	8	pF	Fc = 1 MHz
Cout	Output Pin Capacitance	---	12	pF	Fc = 1 MHz

TABLE 4. DC CHARACTERISTICS

NOTE:
CLKI, FCLKIN, EXTCLK, VSEL0, VSEL1, SELEN, VGA/TTL, FCLKSEL, MSEL0, MSEL1, MCLKEN, VCLKEN input pins have internal pullup resistance.

6.0 AC TIMING CHARACTERISTICS

The following notes apply to all of the parameters presented in this section:

1. REFCLK = 14.318 MHz
2. $t_c = 1/f_c$
3. All units are in nanoseconds (ns)
4. Maximum jitter within a range of 30 µs after triggering on a 400 MHz scope.
5. Rise and fall time between 0.8 and 2.0 VDC.
6. Output pin loading = 25 pF.
7. Duty cycle measured at 1.4 V

SYMBOL	PARAMETER	MIN	MAX	NOTES
	SELEN TIMING			
t_{pwen}	Enable Pulse Width	20	---	
t_{suen}	Setup Time Data to Enable	20	---	
t_{hden}	Hold Time Data to Enable	10	---	
	Reference Input Clock			
t_r	Rise Time	---	10	Phase Jitter 1 ns max
t_f	Fall Time	---	10	Duty Cycle 42.5% min to 57.5% max
	MCLK & VCLK TIMINGS			
t_r	Rise time	---	3	Phase Jitter 5 ns max
t_f	Fall time	---	3	Duty Cycle 40% min to 60% max
---	Frequency Error		1	%
---	Pass through Frequency		56	MHz
---	Propogation Delay for Pass through frequency	---	20	
---	Output Enable to tri-state (into and out of) time	---	15	

TABLE 5. AC TIMING CHARACTERISTICS

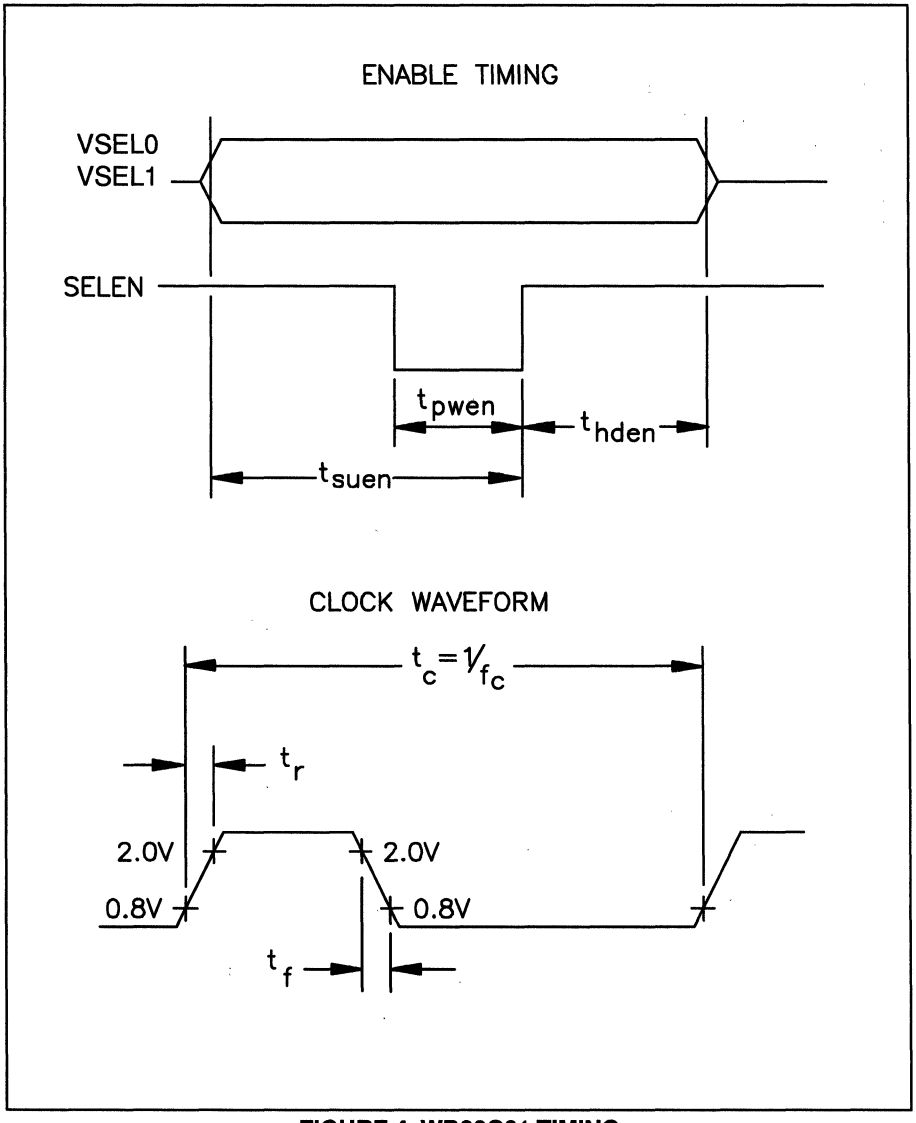


FIGURE 4. WD90C61 TIMING

7.0 ORDERING INFORMATION

Package Type: 20-Pin PLCC

Part Number: WD90C61JE00 02

7.1 PACKAGE DIMENSIONS

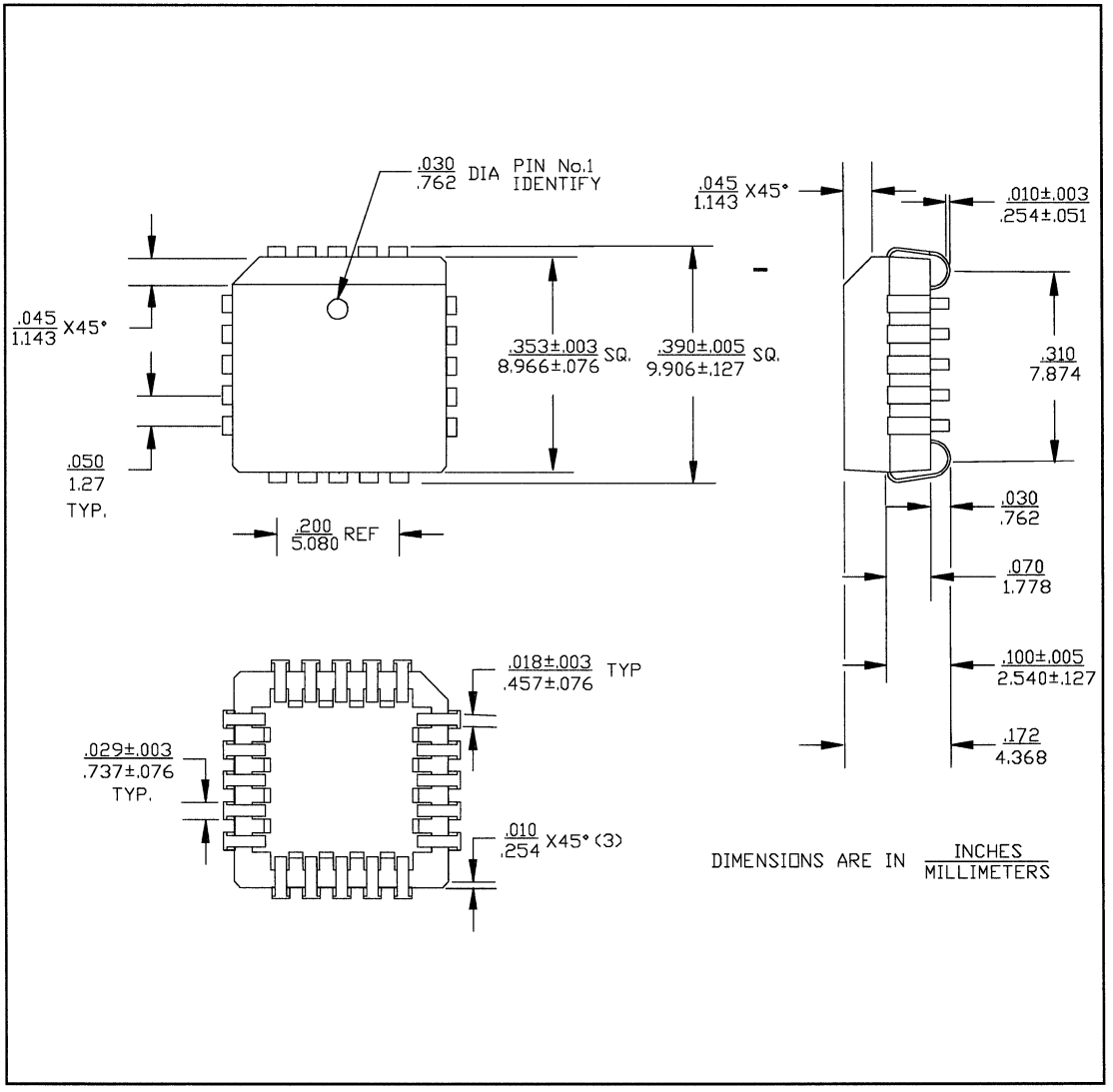
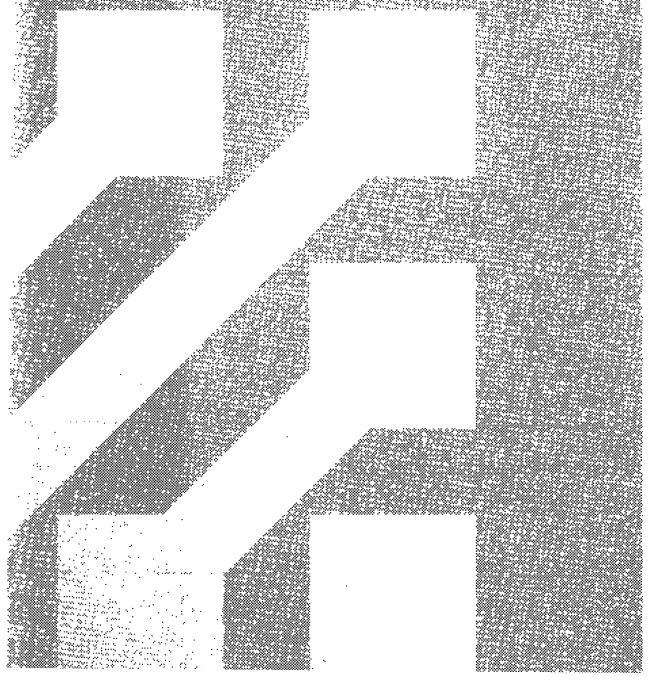


FIGURE 5. WD90C61 20-PIN PLCC PACKAGE DIMENSIONS

WD9500

(PWGA) Enhanced 8514/A

Compatible Chip Set



WESTERN DIGITAL

TABLE OF CONTENTS

Section **Title** **Page**

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

The Western Digital Imaging WD9500-SET1 is a set of two proprietary VLSI chips (Pixel Address Manager and Pixel Data Manager). These chips are designed to serve as the primary components of intelligent high-resolution graphics add-in boards and motherboards for PC/AT, PS/2 Micro Channel and E.I.S.A. computer systems and compatibles. When the remaining board-level components and software are properly selected and integrated, the WD9500-SET1 will provide full compatibility with the IBM 8514/A Display Adapter with superior performance plus functional enhancements (Western Digital Extensions). In order to take full advantage of all features, including the unique extensions, Western Digital supplies key software drivers, with specific performance improvements including 8514/A Adapter compatible interface, Microsoft Windows 286 and 386 drivers, and Display List drivers for AutoCAD.

1.1 FEATURES

Full functional compatibility with the IBM 8514/A Display Adapter, including hardware compatibility with the registers that any application would access.

- Integrated bus interface: PC/AT, PS/2 Micro Channel and E.I.S.A.
- Transparently runs software written for 8514/A interlaced monitors on non-interlaced monitors.
- Performance averages 30% to 100% faster than 8514/A on graphics operations.
- BITBLT performance 4.5 times that of IBM 8514/A in Turbo 4-bit mode. Turbo 4-bit BITBLT is two times faster than regular 4-bit or 8-bit BITBLT.
- Enhanced resolution: one page of 1280x1024 pixels 256 colors; two pages of 1024x768 pixels 256 colors; two pages of 640x480 pixels 256 colors.
- Enhanced graphics commands for high-speed hardware generation of textured lines and enhanced solid lines.
- Flicker-free video DAC programming.
- 60MHz Graphics Processor Clock Rate.
- All features, including most extensions, are supported by Western Digital Imaging Adapter Interface (A.I.) driver software.
- Performance enhanced software drivers for key software packages including Windows 286/386 and AutoCAD.
- Supports 256Kx4 VRAM in different speed grades (120ns or faster) with programmable VRAM timing to minimize wait states.
- Independent Video and Data Clocks.
- Supports both INMOS and Brooktree video DACs and compatibles, with back-end integration to minimize external glue logic.
- Supports both interlaced and non-interlaced monitors up to 70Hz vertical refresh rate. Software written for 8514/A interlaced monitors needs no modification for non-interlaced monitors.
- 132-Pin JEDEC Plastic Quad Fine Pitch Flat Pack.
- 1.25 Micron CMOS Technology.

25

1.2 DESCRIPTION

In addition to full compatibility with the IBM 8514/A, which provides intelligent graphics functions such as polyline drawing, pattern fill for rectangles, "areas" (polygons), and "scissoring" (clipping), the WD9500-SET1 provides several functional enhancements and options as well as superior performance.

A major enhancement is the support of higher screen resolution, 1280x1024 pixels with 256 simultaneously displayable colors, as opposed to the 1024x768 maximum for the IBM 8514/A. Alternatively, the WD9500-SET1 can support a second screen page at the highest 8514/A resolution.

The WD9500-SET1 will give end user dramatic speed improvement in almost all graphics operation. In regular 4-bit mode, the WD9500-SET1 performs Bit Block Transfers (BITBLTs) twice as fast as the IBM 8514/A. In Turbo 4-bit mode, it is 4.5 times as fast. In particular, enhanced performance will be obvious when moving large images on the screen (e.g. scrolling). Under turbo mode all horizontal data movement will be twice as fast. This includes BITBLT, rectangle fill, horizontal line, and polygon search and fill.

Users will also notice considerable performance improvement with the WD9500-SET1 in all new line-drawing operations, because it directly performs several functions that the IBM 8514/A must perform in much slower CPU software. One such improvement is the direct generation of textured line; another is the automatic, high-speed calculation of line parameters by the WD9500-SET1,

replacing the tedious CPU software procedures with simple specifications of only the beginning and ending points of any line.

Whereas the IBM Display Adapter 8514/A is designed only for use in the PS/2 computer models that use the Micro Channel bus, the WD9500-SET1 provides an alternate interface to allow full 8514/A functionality (with extensions) for the Micro Channel, and more importantly, for all PC/AT computers and compatibles. The interface selection is made with a single device pin that is "strapped" at board design time.

Many graphics applications result in noticeable screen flickering when the software steals refresh cycles to modify the color palette in the video DAC. A unique low-cost board design option will provide flicker-free display operation by allowing the WD9500-SET1 to buffer the new palette values and apply them during the monitor's horizontal retrace (flyback).

WD9500-SET1 based boards can accommodate both interlaced display monitors, such as the IBM 8514, and non-interlaced monitors; the WD9500-SET1 will drive either, automatically configuring itself at reset time based on the signals in the monitor interface cable (for IBM-compatible interlaced monitors) or on user selection through on-board switches or on user selection through a software utility. End users can thus exploit cost/performance tradeoffs that are not available with the IBM 8514/A board.

Software written directly to 8514/A registers programs the video registers to IBM 8514/A display interlaced timing for 1024x768 resolution. To achieve maximum flexibility for driving different monitors, two sets of video registers are provided; one for 1024x768 resolution and one for 640x480 resolution. These registers can be programmed by the BIOS EPROM at power up and their values locked in so that direct access by software later will not affect the preset video timing.

For the board designer, the WD9500-SET1 provides several further cost/function/performance trade-off opportunities, and also saves design time, board space, and component costs by integrating much of the peripheral logic into its design. The designer can choose among several video memory (VRAM) architectures, using 256Kx4 VRAM chips, with back-end logic integrated into the WD9500-SET1 for 8514/A emulation and extension to two pages of 1024x768x8 (1280x1024 extended resolution requires off-chip logic support). The designer may also exploit the use of different clock rates for the drawing process and the screen refresh process; and bypass design of video data multiplexing and serializing, as these functions are integrated into the WD9500-SET1 chips.

2.0 ARCHITECTURE

Figure 1 illustrates the logical architecture of a WD9500-SET1 based board in block diagram style. Each of its major elements, which for now are presented as functional "black boxes", is discussed below.

The WD9500-SET1 consists of two 132-pin chips: the PAM (Pixel Address Manager) and the PDM (Pixel Data Manager).

The VRAM block in Figure 1 represents the video memory subsystem, used to store screen images generated in the WD9500-SET1 (as a result of CPU drawing instructions) or sent from the CPU (typically for the purpose of restoring previously drawn images that had been stored elsewhere in the system). The WD9500-SET1 then accesses these images for automatic display-screen refresh. Drawing operations take place within a pixel coordinate space of 2K by 2K; similar to the 8514/A, remaining VRAM storage is available to the WD9500-SET1 and the CPU for "off-screen" use, including storage of fill patters and scratchpad data. Section 3.2 describes VRAM operation and defines the detailed interface of the VRAM subsystem to the WD9500-SET1 chip set.

In the standard board configuration, the WD9500-SET1 is responsible for serializing and multiplexing data extracted form VRAM for screen refresh, and then forwarding the data to the DAC via the video interface logic block. In VRAM architectures using external back-end support, which is necessary to achieve 1280x1024 pixel resolution, serializing and multiplexing is done within the VRAM block, and the resultant screen refresh data bypasses the WD9500-SET1, as shown in Figure 1.

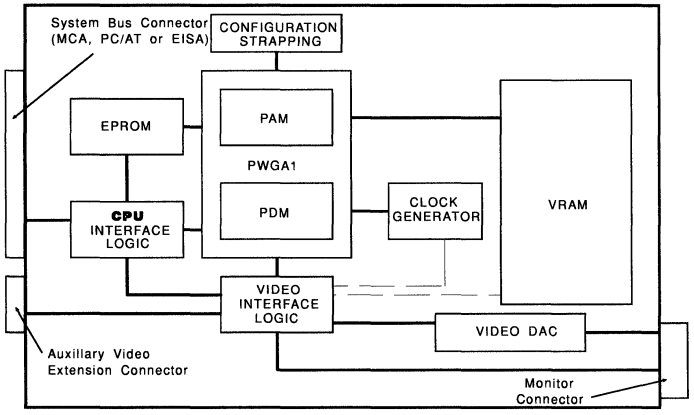


FIGURE 1. ARCHITECTURE

The video DAC (Digital-to-Analog Converter) has the primary function of generating analog intensity signals for the red, green, and blue guns of the display monitor, carrying these values in synchronization with pixel coordinates as the guns sweep across the screen. The source of these values is the "pixel data" that the WD9500-SET1 reads out of VRAM in its screen refresh operation. With external back-end support, extra intelligence is required in the DAC to assist in the data formatting begun in the serializing and multiplexing logic within the VRAM block. The DAC contains the color palette, a small memory that maps a given pixel data valued into a specific combination of RGB intensities according to the contents of each of the cells in palette memory. For example, in a 256-color arrangement, an eight- bit pixel data value select one of 256 palette memory cells. Each of the latter have been loaded with an 18-bit datum partitioned into three 6-bit fields whose values are in turn converted into red, green, and blue signal intensities when that cell is selected. Palette values may be loaded directly from the CPU, or with the Western Digital flicker-free option, indirectly through the WD9500-SET1.

The video DAC and its interfaces, the auxiliary video extension (used to drive the monitor from an off-board source, normally the system VGA), the monitor interface, and other related logic and interfaces together comprise the "video DAC and interface subsystem", described in detail in Chapter. Note that the small block in Figure 1 labeled "Video Interface Logic" represents only a modest amount of logic and, in fact, consists largely of pass-through routing of signals; the block is drawn chiefly for convenience in explanation.

The CPU Interface Logic block contains the bus transceivers and TTL glue logic necessary to interface the WD9500-SET1 chips to the system bus (either the IBM PS/2 Micro Channel of the IBM PC/AT bus, or compatible busses). This block also provides a data path to the DAC used by the CPU to directly access palette values, and to the

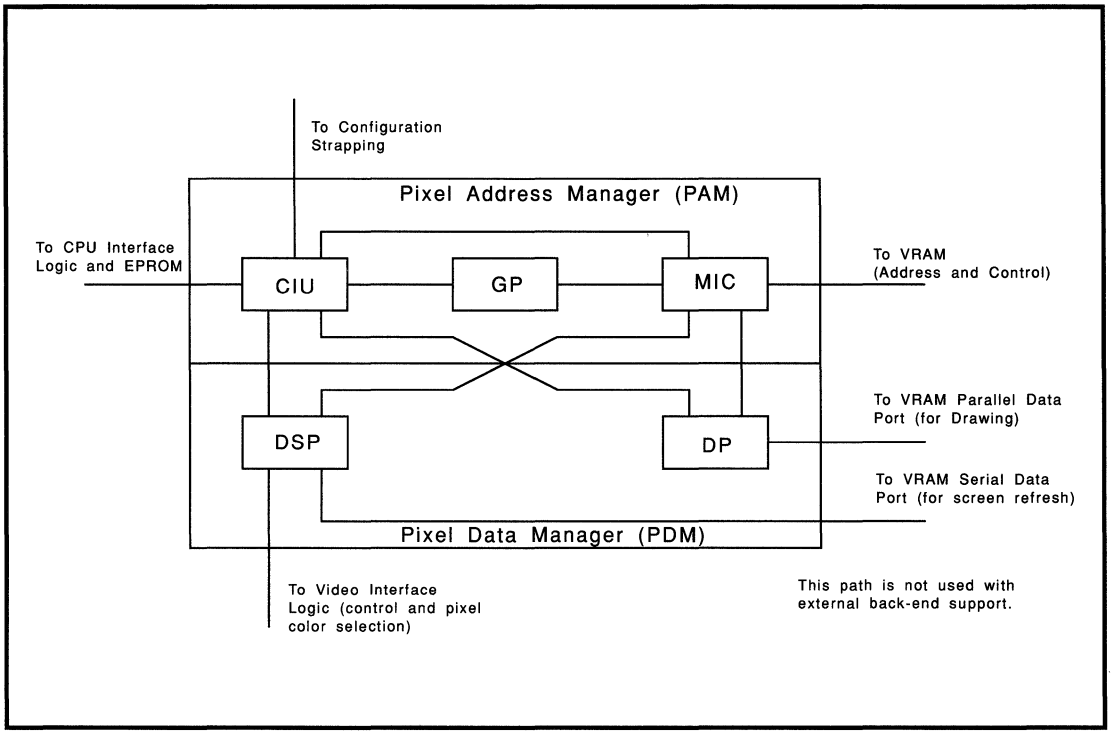


FIGURE 2. FUNCTIONAL ORGANIZATION

EPROM. The CPU interface logic is described in detail in Section 3.1.

The remaining board elements are the EPROM (containing Western Digital-supplied BIOS extension firmware), the clock generators, and a group of minor components (pull-up/down logic and DIP switches) used by the WD9500-SET1 to sense its environmental configuration; whether Micro Channel or AT bus, VRAM organization, etc. These elements are described in Section 3.0, together with the inter-chip (PAM-PDM) connections.

Finally, the WD9500-SET1 contains a set of user-accessible internal register that are compatible with those on the IBM 8514/A board, plus certain extra registers to support Western Digital extensions. From the user's point of view, these registers exist chiefly as destinations for software commands ("orders" in IBM terminology) and their parameters.

2.1 FUNCTIONAL ORGANIZATION

Figure 2 introduces the internal functional blocks of the PAM and PDM chips. Communication between the two chips is mediated by two Internal Bus Interface Units (IBIUs); they are transparent to user operations, and are not shown in the diagram.

In addition to the internal registers and the IBIUs, the functional modules within the WD9500-SET1 are as follows:

Within the **PAM**:

- **CIU:** CPU Interface Unit
- **GP:** Graphics Processor
- **MIC:** Memory Interface Controller

Within the **PDM**:

- **DP:** Data Processor
- **DSP:** Display Processor

The **CIU** controls communication with the system bus (via the CPU interface logic block external to the chip set), and passes data to and from all the other units on the chip set. It also performs certain miscellaneous functions, such as forwarding addresses from the system bus to the EPROM.

The **GP** performs the actual drawing computations; it supports all 8514/A graphics modes, plus Western Digital extensions. The modes include line drawing, area fill area outline drawing (arbitrary polygons), rectangle drawing, image transfer from the CPU, BITBLT copying (Bit Block Transfer within VRAM), and scissoring. The GP receives its drawing instructions form the CIU and sends the resulting pixel coordinates to the MIC.

The **MIC** controls VRAM addressing and access. In a typical drawing operation, it will convert the DP supplied pixel coordinates into VRAM addresses, cause the VRAM to send the addressed data (pixel color values) to the DP for modification, and then rewrite back into VRAM. When not involved in a drawing or special-purpose access, the MIC manages the VRAM addressing portion of the constantly on-going screen refresh process. The MIC gives screen refresh the highest priority for VRAM access; next is timer-based VRAM chip refresh, with DP-requested drawing access given the lowest priority.

The **DP** is responsible for updating VRAM in support of drawing and data transfer operations and altering pixel data (color values) according to masks and parameters, including "mix" specifications supplied in shared internal registers by the DP and GP. The DP receives pixel data on a bidirectional bus from the VRAM, modifies it, and then writes it back to the VRAM on the same bus.

The **DSP** manages the DAC and monitor, coordinating its role in the screen refresh process with the MIC. With an integrated back-end VRAM design, the DSP serializes and multiplexes pixel data, "pumped" out of VRAM by the MIC, to the DAC, in synchronization with the timing of the monitor's sweep across the display screen. (With external back-end support, this DSP function is assumed by external logic within the VRAM block and the DAC).

2.2 BOARD OPERATION OVERVIEW

The functions of any WD9500-SET1 based board, as well as those of the IBM 8514/A, can be summarized as follows:

A. Screen refresh: A key function is driving the display monitor. The board reads data form its VRAM stored representation of the screen image, and then converts the data, pixel by pixel, into RGB signal for the display monitor, in synchronization with the sweeping of the monitor's RGB guns across its screen.

B. Drawing: The other major board function , less time-critical then screen refresh, is the generation of new lines and areas within VRAM in response to commands from the system CPU. In this context, "drawing" includes filling polygon shapes with patters, establishing boundaries for "scissoring" (clipping), and similar operations. Drawing operations can involve complex algorithms, and they require correspondingly sophisticated processing by the WD9500-SET1.

C. Image transfer: In most graphics work, it is common to save board-drawn images (e.g. pop-up menus) elsewhere in main system memory and/or on disk for later restoration to on-board video memory and thence to the display screen.

D. VGA input: The host CPU may request that the monitor be driven by the VGA (Video Graphics Array), a similar but less sophisticated graphics facility located elsewhere in the system; in this case the WD9500-SET1 based board (or the 8514/A) essentially becomes a passive pass-through channel, taking video data and sync signals from the "auxiliary video extension" bus connector. Note that another monitor can be attached directly to the VGA; if the WD9500- SET1 based board (or 8514/A) is not in pass-through mode, then the two monitors can simultaneously display different images.

E. Palette loading: Pixel color interpretation is mediated by a small "palette" memory in the video DAC on the board. The CPU can very rapidly effect changes on the screen by changing the contents of this memory, as distinct from issuing drawing commands.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
62-69, 71-82	A0-A19	I	CPU addaress bits 0 through 19
85	AUP	I	Decoding of upper CPU address bits 23-20, plus MADE24; all these should be 0 if the lower 20 bits of address are to be considered valid for the WD9500 based board.
57	M/$\overline{IO}$	I	Distinguishes memory access from I/O access
59	$\overline{S0}$	I	Status Bit 0
58	$\overline{S1}$	I	Status Bit 1
61	$\overline{ADL}$	I	Address Latch
60	$\overline{CMD}$	I	Command
56	$\overline{SBHE}$	I	System Byte High Enable
52	RESET	I	Channel Reset
86	$\overline{CDSETUP}$	I	Card Setup
90	CD CHRDY	O	Channel Ready
88	$\overline{IRQ}$	O	Interrupt Request; tied to Micro Channel IRQ 9
89	$\overline{CD\ SFFBK}$	O	Card Selected Feedback
55	$\overline{CD\ DS16}$	O	Card Data Size 16
91	$\overline{DBEN}$	O	Data Bus Enable
94-98, 100-110	D0-D15	I/O	CPU Data Bus Bits 0 through 16
92	DBDIR	O	Data Bus Direction (high for CPU read, low for CPU write)

TABLE 1. CPU INTERFACE PINS (PAM) FOR MICRO CHANNEL

F. *EPROM access:* The board includes a small EPROM containing a BIOS extension available to the CPU. The EPROM is mainly for initialization an diagnostic testing during power up. (Note that a portion of EPROM contains certain board configuration information read by the WD9500-SET1 upon power up.)

G. *Other:* Finally, the board design must provide for customary CPU handshaking, interrupts, and miscellaneous bus interface signals.

3.0 WD9500 INTERFACES

3.1 CPU INTERFACE

The PAM provides interface pins to connect to either the IBM PS/2 Micro Channel of the AT bus via a small amount of external logic, illustrated in Figures 1 and 2. The CIO configures itself for one of the two different interfaces according to the value of a configuration strapping pin, described later in this chapter (Table 12).

Because of the two possible external environments, most of these CPU interface pins have two alternate interpretations, as shown in the following tables. In both cases, however, the names and uses of most of these pins correspond precisely to the IBM specifications for theMicro Channel or AT bus, and so do not need special explanation.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
62-69, 71-82	SA0-SA19	I	CPU addaress bits 0 through 19
85	AUP	I	Decoding of upper CPU address bits 23-20, plus MADE24; all these should be 0 if the lower 20 bits of address are to be considered valid for the WD9500 based board.
56	$\overline{\text{SBHE}}$	I	System Byte High Enable
57	$\overline{\text{MEMR}}$	I	Memory Read
59	$\overline{\text{MEMW}}$	I	Memory Write
58	$\overline{\text{IOR}}$	I	I/O Read
60	$\overline{\text{IOW}}$	I	I/O Write
61	BALE	I	Buffered Address Latch Enable
86	$\overline{\text{AEN}}$	I	Address Enable
52	RESET	I	System Reset
88	$\overline{\text{IRQ}}$	O	Interrupt Request; tied to any AT bus interrupt
55	$\overline{\text{CD CS16}}$	O	I/O 16-bit Chip Select
91	$\overline{\text{DBEN}}$	O	Data Bus Enable
94-98, 100-110	SD0-SD15	I/O	CPU Data Bus Bits 0 through 16
92	DBDIR	O	Data Bus Direction (high for CPU read, low for CPU write)
84	ATCLK	I	AT Bus Clock

TABLE 2. CPU INTERFACE PINS (PAM) FOR AT BUS

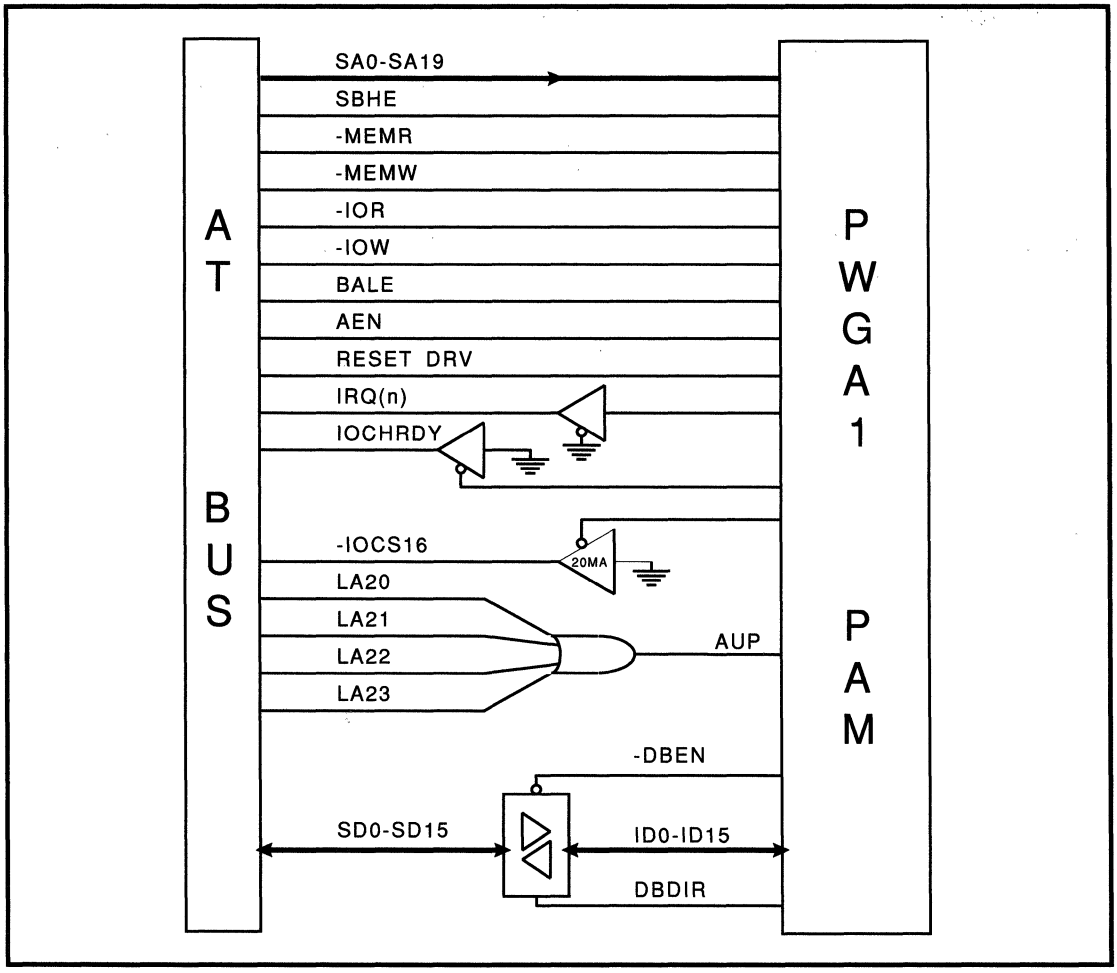


FIGURE 3. CPU INTERFACE LOGIC - AT BUS

I/E*	NUMBER OF CHIPS	PIXEL RESOLUTION	PIXEL DEPTH	NUMBER OF SCREEN PAGES	S/W**
I	4	1024x768	4	1	S
		640x480	4	2	S
	8	1024x768	8	1	S
		1024x768	4	2	W
		640x480	8	1	S
	16	1024x768	8	2	W
		1024x768	4	2	W
		640x480	8	2	W
E	8	1280X1024	4	1	W
		1024x768	8	1	S
		1024x768	4	2	W
		640x480	8	1	S
	16	1280x1024	8	1	W
		1024x768	8	2	W
		1024x768	4	2	W
		640x480	8	2	W

*I = Integrated Back-end Support

E = External Back-end Support

**S = Standard capability within 8514/A emulation

W = Western Digital extension to 8514/A capability

TABLE 3. VRAM PARAMETERS

3.2 VRAM DESIGN AND INTERFACE

The WD9500-SET1 supports two VRAM designs. Each of these in turn can be implemented with two or three levels of chip population, for a total of five implementations. The design choice depends on the desired combination of the following criteria (with only certain combinations possible):

- pixel resolution: 640x480, 1024x768, 1280x1024
- pixel depth: 4 or 8 bits per pixel
- number of screen pages: one or two
- number of VRAM chips (and hence board size)
- field upgradeability
- type of design: with back-end (serializing and multiplexing of pixel data for screen refresh) integrated within the WD9500-SET1, or with external back-end support

External back-end support: includes the use of a more sophisticated DAC - is required to achieve 1280x1024 resolution.

3.2.1 INTEGRATED BACK-END VRAM DESIGN

The capabilities of the various VRAM designs, with their several levels of chip population, are shown in Table 3. Note: Although not shown, each level of chip loading for a given design includes the capabilities of the smaller chip population(s).

If maximum IBM 8514/A resolution is desired, this design should be implemented to at least the 8-chip level; implementation at the 16-chip level provides for the extended capability of doubling the number of screen pages supported by the 8-

PIN NUMBER	PIN SYMBOL	DESCRIPTION
19, 16-10	MA7-MA0	Low order address lines, into all quads.
34	LA13	Used as high-order address bit (MA8) for quads Q1, Q3, and their counterparts, in all designs.
35	LA24	Used as high-order address bit (MA8) for quads Q2, Q4, and their counterparts, in all designs.
22	$\overline{RAS0}$	Row Address Strobe 0 (Quads 1 & 2)
23	$\overline{RAS1}$	Row Address Strobe 1 (Quads 3 & 4)
20	$\overline{CAS12}$	Column Address Strobe 1 (Quads 1 & 2)
21	$\overline{CAS34}$	Column Address Strobe (Quads 3 & 4)
31-24	WE7-WE0	Pixel data Write Enable lines to enable writing into VRAM on the PD bus (bidirectional Parallel Data bus, between VRAM and DP; A given quad receives either WE0-3 or WE4-7.
32	$\overline{DT/OE}$	Transfer cycle control and serial data output enable, used by all quads.

TABLE 4. PAM PIN INTERFACE TO VRAM

chip version. See Appendix A for an illustration of the 16-chip version with indications of which chips should be left unpopulated if field upgradeable 4-chip and/or 16-chip versions are to be produced. The same diagram can also serve as the basis for an 8-chip design, with half of those chips omitted for future field upgrade if desired.

See Appendix A for a detailed connection drawing for VRAM to PAM and PDM.

Tables 4 and 5 show the PAM and PDM pins used to form the VRAM interface. See Appendix A for VRAM design diagrams.

All the Pins in Table 4 drive control signals generated by the MIC.

The PD Pixel Data bus is managed by the Data Processor module (DP); all other pins in Table 5 are managed by the Display Processor (DSP).

WE0-3 are for pixel positions 0-3, respectively. In turbo mode, WE4-7 are for positions 4-7. For x8 mode, WE4-7 are the same as WE0-3.

In the VRAM design diagrams (see Appendix A), the PD lines connect to the parallel data ports of the VRAM chips, while the SD lines connect to their serial data ports.

The different resolution modes require different memory addressing schemes to configure the display memory properly for screen pixel position.

3.2.2 EXTERNAL BACK-END VRAM DESIGN

See Appendix A for an illustration of the 16-chip version with external back-end support. A Brooktree 8-bit video DAC BT458 is used.

3.3 VIDEO DAC AND INTERFACE SUB-SYSTEM

This section includes the following information for the board designer:

Routing of VRAM pixel data to the DAC. This involves two alternative designs, depending on weather back-end support is performed by the WD9500-SET1 or by external components.

Routing of control information from the WD9500-SET1 to the DAC and the monitor.

Signal routing in support of "VGA modes", in which the monitor is driven by control and data signals originating off-board, in the system VGA, and passed through to the monitor from the auxiliary extension connector.

PIN NUMBER	PIN SYMBOL	DESCRIPTION
90-93, 95-98, 100-114, 117-125	PD31-PD0	Parallel Data bus connecting the DP module to the VRAM block; data is bidirectional. (This is the path through which the DP first reads, then rewrites pixels in support of drawing operations).
46-49, 52-67, 71-82	SD31-SD0	Serial Data bus, in VRAM designs with integrated back-end support, this is the path by which screen refresh data is extracted (by a transfer cycle) from the serial ports of the VRAM chips and then moved to the DSP module for serializing and multiplexing before being sent to the DAC. In VRAM designs with external back-end support, the serial data bus to the DSP is not used; instead, the DSP reconfigures itself to use some of these pins (SD0, SD1, SD4, SD5, SD6) as output drivers for additional control signals to the VRAM (see External Back-End VRAM Design).
87,85,86,84	SE12A, SE34A, SE12B, SE34B	Serial Data Output Enable
88	SC13	Serial Data Clock 1
89	SC24	Serial Data Clock 2
The following pins are changed for external back-end support:		
82	SC3 (SD0)	Serial Data Clock 3
81	SC2(SD1)	Serial Data Clock 4
78	SEL0(SD4)	Mux Select 0
77	SEL1(SD5)	Mux Select 1
76	LDCLK (SD6)	LDCLK signal to the DAC

TABLE 5. PDM PIN INTERFACE TO VRAM

Palette access, with the board design option of implementing "flicker-free mode", a Western Digital extension.

Note that a related topic, WD9500-SET1 recognition of monitor type, is grouped with other configuration strapping issues, and is discussed later in this chapter.

The PDM pins associated with the video interface subsystem are all outputs from the DSP, and are shown in Table 6.

Appendix B describes board implementation of the video DAC and interface subsystem with integrated and external back-end support. The flicker-free option applies to both and is discussed later. The WD9500-SET1 chip set supports INMOS IMS G171/176/178, Brooktree BT471/478 and compatible video DACs for 8514/A modes. It also supports Brooktree BT451/458 and compatible DACs for Western Digital enhanced 1280x1024 mode. The Brooktree BT471 DACs include a 256x18 palette, loaded with 6-bit R, G, and B color intensity values; the high two bits of the 8-bit data lines supplying these values are ignored. The BT478 substitute a 256x24 palette, with all eight bits used for finer control of color. The DAC8 pin from the PAM can be used to select 6-bit or 8-bit palette fields. Note that the palette overlay capabilities are not used; the DAC's RS2 and OL0-OL3 pins should be tied down. Without the flicker-free option, CPU software writes data into the DAC's color palette on the low eight bits of the system CPU data bus.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
30-27, 24-21	VDATA0-7	O	With integrated back-end support, these pins output the video data for the DAC. With external back-end support, they are not used for this purpose, since the DAC receives its data from the external logic within the VRAM block. In both cases, however, these same pins are the source of palette-loading data in flicker-free mode. (tri-state output)
132	SELVD	O	With the flicker-free design option, this pin selects the source of palette-loading data to be either the low eight bits of the PC data bus (normal mode) or VDATA0-7 (flicker-free mode). SELVD is also the tri-state control signal for $\overline{\text{DACRD}}$ and $\overline{\text{DACWR}}$ from the PAM. When high, PAM $\overline{\text{DACRD}}$ and $\overline{\text{DACWR}}$ signals are disabled.
25	VCLK	O	Video clock for the DAC (tri-state output)
20	BLANK	O	Video blank signal for the DAC (tri-state output)
31	$\overline{\text{DACRD}}$	O	DAC palette read. Note that data read from the palette is always routed to the PC data bus in the CPU interface logic.
32	$\overline{\text{DACWR}}$	O	DAC palette write (see SELVD above)
33	HSYNC	O	Horizontal sync to the monitor (tri-state output).
34	VSYNC	O	Vertical sync to the monitor (tri-state output)
42	$\overline{\text{ENVGA}}$	O	Enables VGA pass-through mode. This signal selects the source of video data to the DAC (either VDATA0-7 from the PDM or P0-7 from the auxiliary vedeo extension). It also selects the control sitgnals to the DAC (either VCLK and BLANK from the PDM, or HSYNC and VSYNC from the PDM, or HSYNC and VSYNC from the auxiliary video extension).
76	LDCLK	O	For external back-end support. This output signal drives the LD (load) input of the BT458/451 DAC, where it synchronizes the serialization of the 32 bits of pixel data from the VRAM into four 8-bit pixel color selections. With integrated back-end support this pin is SD6 of the serial data bus from VRAM.

TABLE 6. PDM PIN INTERFACE TO VIDEO SUBSYSTEM

PIN NUMBER	PIN SYMBOL	I/O	DESCRIPTION
54, 53, 49-37	BSA0-BSA14	O	EPROM BIOS address lines
36	$\overline{\text{BSOE}}$	O	$\overline{\text{EPROM BIOS}}$ output enable

TABLE 7. EPROM INTERFACE PINS

	MICRO CHANNEL	AT BUS	
		IAD5 = 0*	IAD5 = 1*
2K (Fixed)	C6800-C6FFF	C8800-C8FFF	D8800-D8FFF
4K (Bank Selectable)	C7000-C7FFF	C9000-C9FFF	D9000-D9FFF
2K (Fixed)	CA000-CA7FFF	N/A	N/A

TABLE 8. BIOS EPROM ADDRESS MAPPING

The WD9500-SET1 intercepts CPU addressing and controls DAC access using the low two bits of its EPROM address bus, BIOSA1 and BIOSA0. When the flicker-free option is incorporated into the board design, as shown in Appendix B, the CPU software can invoke flicker-free mode. In this mode, palette data is buffered by the WD9500-SET1 and released to the DAC over the VDATA0-7 lines, with the SELD control signal activated to select the VDATA lines in preference to the system data bus. Routing of the latter lines to the DAC via the SELD multiplexer is still required, both to allow for non-flicker- free mode (8514/A emulation) and for palette reads.

Appendix B shows the implementation of 1280x1024 resolution with external back-end support and two DACs. The fast DAC BT451/458 is used for 1280x1024 and 1024x768 resolutions. The slow DAC BT471/478 is used for VGA pass-through. The flicker-free capabilities do not apply to that DAC.

3.4 OTHER BOARD DESIGN ELEMENTS

3.4.1 EPROM

A 27256 32K UV EPROM is used on the Micro Channel board to store the Western Digital BIOS extension plus two configuration parameters that the WD9500-SET1 loads into internal registers upon board reset: the POS ID (for PS/2 Micro Channel system integration), chosen by the customer, and a VRAM wait-state control parameter (dependant upon characteristics of the VRAM chips chosen for the board, and automatically selected from among four choices depending on how two configuration parameter pins are strapped); see Appendix C.

The EPROM is remapped for the AT bus board because of VGA conflict and widespread use of Shadow RAM in 80386 machines. BIOS EPROM Address mapping for WD9500-SET1 chip set is as stated in Table 7.

For PC/AT and compatibles, 2 sets of addresses that minimize memory conflict with other products have been selected, i.e. C8800-C9FFF or D8800-D9FFF. Either address can be selected by a jumper in a board design.

The EPROM is accessed through the CIU on the PAM, which generates addressing for the EPROM and activated an output enable line. Data from EPROM ties to both the CIU and the system data bus through an 8-bit connection to the internal data bus. (See Figures 1 and 2). The PAM pins involved are shown in Table 8.

3.4.2 PAM-PDM INTERFACE

The PAM and PDM are connected to each other through a 22-pin interface. Both chips include an internal bus interface unit (IBIU) which controls inter-chip communication; one of its functions is to buffer data transfers larger than eight bits, since the general purpose inter-chip bus is eight-bits wide due to pin count constraints. Inter-chip communication is transparent to the user. See Table 9.

PAM PIN NUMBER	SIGNAL DIRECTION	PDM PIN NUMBER	PIN SYMBOL
PAM 125-132	↔	PDM 9-2	IAD0-7
PAM 124	→	PDM 10	IADSTAT
PAM 8	→	PDM 126	RWCAS
PAM 123	→	PDM 11	RD/WR
PAM 122	→	PDM 12	AS
PAM 121	→	PDM 13	DS
PAM 114	←	PDM 19	RMWE
PAM 2	←	PDM 132	SELVD
PAM 119	←	PDM 15	SLC
PAM 118	←	PDM 16	SLD
PAM 6	→	PDM 128	WROE
PAM 3	→	PDM 131	MDT0
PAM 4	→	PDM 130	MDT1

TABLE 9. INTERCHIP INTERFACE PINS

3.4.3 CONFIGURATION STRAPPING

The WD9500-SET1 configures itself to its board design environment by latching the values of certain strapped input pins on the rising edge of the CPU's RESET signal. (It also reads two parameters from the EPROM, as mentioned earlier). One of these pins, which distinguishes between the Micro Channel and PC/AT bus CPU interfaces, is dedicated to this purpose. Three other dedicated pins receive monitor type information. The remaining pins, which all deal with VRAM configuration information, are actually part of the inter-chip communication interface; the strapped values are driven to the inter-chip lines through tri-state buffers. See Tables 10 - 13.

Note: If a field-upgradeable VRAM design is selected (with the VRAM chips partially populated), the appropriate strappings should be implemented with jumpers, switches or some other method that allows the use to change the strapped values in the course of field upgrade.

3.4.4 CLOCK CONSIDERATIONS

A major design element of the WD9500-SET1 is the provision for two separate and independent clock rates; one for drawing operations, the other for screen refresh. In particular, faster monitors can be used without changing the clock rate of the drawing facilities within the WD9500-SET1, and conversely, use of slower monitors will not degrade drawing speed.

The system clock signal, provided by an external 60MHz oscillator, drives the drawing process within the WD9500-SET1, and is used to generated VRAM timing. The pixel clock, used to drive the screen refresh process, is selected from among eight oscillator outputs to accommodate different types of monitors. Three PDM output signals, CLKSEL2, CLKSEL1, and CLKSEL0, are provided to make the selection.

In the United States, non-interlaced video monitors use a vertical refresh frequency of 60Hz; in Europe, the standard is 70Hz. Including the interlaced IBM 8514 monitor (vertical frequency 43.48Hz) produces Table 14, in which the "Pixel Frequency" is the frequency of the oscillator selected by CLKSEL2, CLKSEL1, and CLKSEL0 as input to the PDM's PCLK pin.

The typical WD9500-SET1 board will therefore be configured with oscillators at 25.28, 44.90 and 64.37MHz for use with U.S. standard monitors, or with oscillators at 31.40, 44.90, and 74.16MHz for use with European standard monitors. A more am-

PAM PIN NUMBER	PDM PIN NUMBER	PIN SYMBOL	DESCRIPTION
120		MC/$\overline{AT}$	High if Micro Channel; low if PC/AT bus
	36-38	MID2-MID0	Monitor ID Bits 2-0
130	3	IAD5	EPROM location for AT bus design (not used in Micro Channel); low for EPROM memory address at C8800H-C9FFFH, high for address at D8800H-D9FFFH.
131	3	IAD6	Test Mode. Low for test mode; high for normal operation.
132	2	IAD7	DAC Type.Low foar 6-bit DAC; high for 8-bit DAC.
129	5	IAD4	VRAM Chip Speed. Low for -8 spec; high for -10 spec.
128	6	IAD3	External Back-End. This pin specifies the maximum resolution allowed by VRAM design: low for 1280 x 1024 resolution (external back-end required), high for 1024 x 768 (internal back-end)
125	9	IAD0	VRAM Chip Type. Must be tied high.
126	8	IAD1	Chip Count 0. Low order bit of 2-bit VRAM chip count field (see below)
127	7	IAD2	Chip Count 1. High order bit of 2-bit VRAM chip count field (see below.
122	12	$\overline{AS}$	Monitor Type 0 (see below)
123	11	RD/WR	Monitor Type 1 (see below)

TABLE 10. CONFIGURATION STRAPPING PINS

	Chip Count 1	Chip Count 0
4 Chips	0	0
8 Chips	0	1
16 Chips	1	0
Reserved	1	1

TABLE 11. CHIP COUNT STRAPPING

Type of Monitor	Monitor Type 0	Monitor Type 1
8514 Display	0	0
60 Hz monitor	0	1
Reserved	1	0
70 Hz monitor	1	1

TABLE 12. MONITOR SELECTION

bitious design might include all seven clock frequencies, with the MID2-MID0 inputs (as per "Configuration Strapping" earlier in this chapter) aiding in the selection.

The WD9500-SET1 pins involved in clock signal generation and use are summarized in Table 14.

MID2	MID1	MID0	MONITOR TYPE
0	0	0	Not Defined
0	0	1	Not Defined
0	1	0	IBM 8514 (color monitor, 1024 x 768 interlaced)
0	1	1	Not defined
1	0	0	Not defined
1	0	1	IBM 8503 (monochrome, 640 x 480, non-interlaced)
1	1	0	IBM 8513 (color, 640 x 480, non-interlaced & 8514
1	1	1	Other display*

Note: MID2-0 have internal pull-up resistors. During reset, MID2-0 can also be used to test PDM internal counters. For in-circuit board test, MID2-0 should be high when REST is asserted.

TABLE 13. MONITOR ID INTERPRETATION

CLKSEL			RESOLUTION*	VERTICAL FREQUENCY	HORIZONTAL FREQUENCY	PIXEL FREQUENCY
2	1	0				
0	0	0	640 X 480N	60 Hz	31.47 KHz	25.18 MHz
1	0	0	640 X 480N	70 Hz	37.28 KHz	31.32 MHz
0	0	1	1024 X 768I	43.48 Hz	35.52 KHz	44.90 MHz
1	0	1	1280 X 1024N	60 Hz	63.78 KHz	109.64 MHz**
0	1	0	1280 X 1024N	70 Hz	74.83 KHz	136.71 MHz**
0	1	1	1024 X 768N	60 Hz	49.06 KHz	63.98 MHz
1	1	1	1024 X 768N	70 Hz	56.17 KHz	74.16 MHz

*N = Non-interlaced

I = Interlaced

** In these cases the oscillator frequency must be halved (to 54.82 MHz or 68.36 MHz) before being connected to the PCLK input pin of the PDM. Since this resolution requires external back-end support, however, the original frequency, as shown, must remain intact to drive the

TABLE 14. PIXEL CLOCK FREQUENCY DERIVATION

NAME	PAM/PDM PIN#	I/O	DESCRIPTION
SCLK	PAM 113/PDM 39	I	System clock input; requires 60 MHz
CLKSEL2	PDM 43	O	Selects from seven frequencies for PCLK (see Table 14)
CLKSEL1	PDM 44	O	See Table 14
CLKSEL0	PDM 45	O	See Table 14
PCLK	PDM 68	I	Pixel clock input
VCLK	PDM 25	O	DAC clock source
LDCLK (SD6)	PDM 76	O	LD signal for BT451/458 DAC for external back-end support

TABLE 15. CLOCK PIN SUMMARY

4.0 ABSOLUTE MAXIMUM RATINGS AND DC CHARACTERISTICS

PAM ELECTRICAL SPECIFICATIONS			
PAM AC Specifications			
CLK period: 16 ns minimum, 16.7 ns atypical.			
CLK rise and fall time (o.4 v to 2.4 v): 2.5 ns maximum			
All outputs rise and fall time (10% to 90%): t.b.d.			
Input capacitance: 10 pF maximum			
PAM DC SPECIFICATIONS			
Absolute maximum ratings:			
Voltages on all inputs and outputs with respect to GND		-0.3 V to 7.0 V	
Operating ambient temperature		$0^{o}C \leq TA \leq 65^{o}$ C	
Storage temperature		$-65^{o}C$ to $150^{o}C$	
DC Characteristics			
	Minimum	Maximum	Unit
Supply voltage (VCC)	4.75	5.25	Volts
Input low voltage (VIL)	-0.3	0.8	Volts
Input high voltage (VIH)	2.0	VCC	Volts
Output low voltage (VOL)		0.4	Volts
Output high voltagae (VOH)	2.4		
Input leakage current (ILI)		± 10	µA*
Tri-state output leakage current (IOL)		± 10	µA**
Power supply current (ICC)		t.b.d.	mA

*VIN = 0 to VCC
**VOUT = 0.4V to VCC

Note: All inputs have static charge and latch up protection circuits. All inputs, including bi-directional pads, have 20K ohm pull-up resistors.

TABLE 16. PAM ELECTRICAL SPECIFICATIONS

SIGNAL NAME	I/O	IOL (Min) @0.4V	IOH (Min) @ 2.4V	Capacitive Loading
D15-0	I/O	1.0 mA	200 µA	75 pF
$\overline{\text{CDDS16}}$	O	2.0 mA	200 µA	250 pF
$\overline{\text{IRQ}}$	O	2.0 mA	200 µA	250 pF
CHRDY	O	2.0 mA	200 µA	250 pF
SFDBK	O	2.0 mA	200 µA	250 pF
$\overline{\text{BIOSOE}}$	O	1.0 mA	200 µA	50 pF
BIOSA14-0	O	1.0 mA	200 µA	50 pF
$\overline{\text{DBEN}}$	O	1.0 mA	200 µA	50 pF
DBDIR	O	1.0 mA	200 µA	50 pF
WROE	O	1.0 mA	200 µA	50 pF
$\overline{\text{DACWR}}$	O	1.0 mA	200 µA	100 pF
$\overline{\text{DACRD}}$	O	1.0 mA	200 µA	100 pF
DAC8	O	0.5 mA	200 µA	50 pF
$\overline{\text{RWCAS}}$	O	1.0 mA	200 µA	50 pF
IADSTAT	O	1.0 mA	200 µA	50 pF
IAD7-0	I/O	1.0 mA	200 µA	50 pF
RD/$\overline{\text{WR}}$	O	1.0 mA	200 µA	50 pF
$\overline{\text{AS}}$	O	1.0 mA	200 µA	50 pF
$\overline{\text{DS}}$	O	1.0 mA	200 µA	50 pF
SWAP	O	1.0 mA	200 µA	50 pF
MDT2-0	O	1.0 mA	200 µA	50 pF
MA7-0	O	1.0 mA	200 µA	130 pF
LA13	O	1.0 mA	200 µA	80 pF
LA24	O	1.0 mA	200 µA	80 pF
LA24	O	1.0 mA	200 µA	100 pF
$\overline{\text{RAS1}}$	O	1.0 mA	200 µA	100 pF
$\overline{\text{RAS0}}$	O	1.0 mA	200 µA	100 pF
$\overline{\text{CAS12}}$	O	1.0 mA	200 µA	100 pF
$\overline{\text{CAS34}}$	O	1.0 mA	200 µA	100 pF
WE7-0	O	1.0 mA	200 µA	50 pF
$\overline{\text{DTOE}}$	O	1.0 mA	200 µA	160 pF

TABLE 17. PAM OUTPUT SPECIFICATIONS

PDM ELECTRICAL SPECIFICATIONS			
PAM AC Specifications			
SCLK period: 16 ns minimum, 16.7 ns atypical.			
PCLK PERIOD: 13.5 ns minimum; 15.4 OR 22.2 ns typical.			
All outputs rise and fall time (10% to 90%): t.b.d.			
Input capacitance: 10 pF maximum			
PDM DC SPECIFICATIONS			
Absolute maximum ratings:			
Voltages on all inputs and outputs with respect to GND		-0.3 V to 7.0 V	
Operating ambient temperature		$0^{o}C \leq TA \leq 65^{o}$ C	
Storage temperature		$-65^{o}C$ to $150^{o}C$	
DC Characteristics			
	Minimum	Maximum	Unit
Supply voltage (VCC)	4.75	5.25	Volts
Input low voltage (VIL)	-0.3	0.8	Volts
Input high voltage (VIH)	2.0	VCC	Volts
Output low voltage (VOL)		0.4	Volts
Output high voltagae (VOH)	2.4		
Input leakage current (ILI)		± 10	µA*
Tri-state output leakage current (IOL)		± 10	µA**
Power supply current (ICC)		t.b.d.	mA

*VIN = 0 to VCC
**VOUT = 0.4V to VCC

Note: All inputs have static charge and latch up protection circuits. All inputs, including bi-directional pads, have 20K ohm pull-up resistors.

TABLE 18. PDM ELECTRICAL SPECIFICATIONS

SIGNAL NAME	I/O	IOL (Min) @0.4V	IOH (Min) @ 2.4V	Capacitive Loading
IAD7-IAD0	I/O	4.20 mA	200 µA	50
RMWE	O	1.00 mA	200 µA	50
SLC	O	4.20 mA	200 µA	50
SLD/TOUT	O	4.20 mA	200 µA	50
PD31-PD0	I/O	4.20 mA	200 µA	50
VCLK	O	4.20 mA	200 µA	30
HSYNC	O	4.20 mA	200 µA	50
VSYNC	O	4.20 mA	200 µA	70
BLANK	O	4.20 mA	200 µA	70
VDATA7-VDATA0	O	4.20 mA	200 µA	30
$\overline{\text{DACWR}}$ ($\overline{\text{DACWE}}$)	O	4.20 mA	200 µA	30
$\overline{\text{DACRD}}$ $\overline{\text{DACRD}}$)	O	4.20 mA	200 µA	50
SELVD	O	4.20 mA	200 µA	50
CLKSEL2-CLKSEL0	O	0.80	200 µA	50
$\overline{\text{ENVGA}}$	O	4.80 mA	200 µA	100
SE12A, SE34A, SE12B, SE34B	O	4.20 mA	200 µA	70
SC13, SC24	O	4.20 mA	200 µA	70
SD6, SD5	I/O	4.20 mA	200 µA	100

TABLE 19. PDM OUTPUT SPECIFICATIONS

5.0 AC TIMING CHARACTERISTICS

To be supplied.

6.0 WD9500 REGISTERS

Although a WD9500 based board is significantly more capable than the IBM 8514/A, especially when configured with sufficient VRAM, the base mode of the board's operations is that of exact 8514/A emulation, including exact compatibility with the 8514/A's user-accessible registers.

The WD9500 internal registers that are compatible with the IBM 8514/A are defined in this section. A summary of 8514/A compatible registers is shown in Table 25 and Table 26 respectively.

All WD9500 registers, except DAC interface registers, are 16-bit word-addressed. The unused bits are either not shown or marked the letter U in the description of the register definitions below. The reserved bits are marked with the letter R both unused and reserved bits default to 0.

6.1 DAC INTERFACE REGISTERS

The 8-bit registers in Table 21 are used to program the external video DAC. It is possible to write and read the DAC. Once the read/write index is written, multiple read/write operations can be performed without having to set the index for each entry.

POS register interface (Micro Channel only)		
The POS registers are used to identify the WD9500 to IBM's setup program. They operate only when the CDSETUP pin goes low. Returns POS ID LSByte from EPROM.		
SETUP MODE IDENTIFICATION	**SETUP_ID1**	**BYTE ACCESSIBLE**
Read only		Setup address 100
Returns POS ID LSByte from EPROM		
SETUP MODE IDENTIFICATION	**SETUP_ID2**	**BYTE ACCESSIBLE**
Returns POS ID MSByte from EPROM		
SETUP MODE IDENTIFICATION	**SETUP_OPT**	**BYTE ACCESSIBLE**
Bit 0 of the Setup Mode Option Select register can be used by the host PC to disable the PWGA in case of an address conflict. Bit 0 = 1 Enable WD9500 registers Bit 0 = 0 Disable WD9500 registers		

TABLE 20. POS REGISTER INTERFACE (MICRO CHANNEL ONLY)

COLOR PROGRAMMING			**8514/A**	**VGA**
DAC Mask	R/W	DAC_MASK	02EA	03C6
DAC Read Index	R/W	DAC_R_INDEX	02EB	03C7 (Write Only) 03C7 (Read Only)
DAC Write Indes	R/W	DAC_W_INDEX	02EC	03C8
DAC Data	R/W	DAC_DATA	02ED	03C9
The 851114/A DAC can be written but not read at the VGA addresses when in VGA pass-through mode (4AE8 bit 0 = 0).				

TABLE 21. DAC COLOR PROGRAMMING REGISTERS

Procedure to write to the DAC: (1) Set start write color index at 02ECH; (2) Write three bytes [RGB values] at 02EDH [The index auto increments the next write entry]; (3) Repeat step 2 until the desired number of entries have been programmed.

Procedure to read from the DAC: (1) Set start read color index at 02EBH. (2) Write three bytes [R. G. B. values] at 02EDH [The index auto increments to the next read entry]. (3) Repeat step 2 until the desired number of entries have been read.

6.2 ADVANCED FUNCTION CONTROL REGISTER (WRITE ONLY - 4AE8H)

Graphics mode is selected by writing to the Advanced Function Control (ADVFUNC_CTL). This register is used by all modules within the WD9500.

BIT	FUNCTION
0	Set to 0 for VGA pass-through mode Set to 1 for 8514/A graphics mode
1	Mode extension - set to 1
2	Screen Resolution Set to 0 for 640 x 480 (25.18 MHz) Set to 1 for 1024 x 768 (44.9 MHz)
3	Reserved for Mode Extension Default = 0
4-15	Unused - Default = 0

MNEMONIC	NAME	ADDRESSS
H_TOTAL	Horizontal Total Register	02E8
H_DISP	Horizontal Displayed Register	06E8
H_SYNC_START	Horizontal Sync Start Register	0AE8
H_SYNC_WID	Horizontal Sync Width Register	0EE8
V_TOTAL	Vertical Total Register	12E8
V_DISP	Vertical Displayed Register	16E8
V_SYNC_START	Vertical Sync Start Register	1AE8
V_SYNC_WID	Vertical Sync Width Register	1EE8
DISP_CNTL	Display Control Register	22E8

TABLE 22. VIDEO TIMING SETUP REGISTER

6.3 VIDEO TIMING SETUP REGISTERS

There are nine registers for setting up video timing: four for horizontal, four for vertical, and one for control. Two sets of these registers (Table 3) are provided by WD9500 to allow video timing parameters to be pre-programmed and locked in for 640x480 and 1024x768 resolutions by Western Digital's BIOS. This extended feature is designed for interfacing with different monitors requiring different timing parameters. Once the timing parameters are locked in, application software that writes directly to the video registers will not need to be changed for different monitors, e.g. interlaced vs. non-interlaced. These registers affect the DSP module of the WD9500. The horizontal and vertical registers are set by the selected resolution. For example, 1024x768 is the graphics mode selected by the ADVFUNC_CNTL Register, then the horizontal and vertical registers are set accordingly. The following tables show the format for the horizontal and vertical registers. Vertical timing is programmed in line resolution. Horizontal timing is programmed in 8-pixel resolution.

6.3.1 HORIZONTAL TOTAL REGISTER (WRITE ONLY - ADDRESS 02E8H)

7	6	5	4	3	2	1	0

Set number of pixels per line, including blanking. Eight pixel blocks.

6.3.2 HORIZONTAL DISPLAYED (WRITE ONLY - ADDRESS 06E8H)

7	6	5	4	3	2	1	0
0							

Set number of pixels per line, including blanking. Eight pixel blocks.

6.3.3 HORIZONTAL SYNC START REGISTER (WRITE ONLY - ADDRESS 0AE8H)

7	6	5	4	3	2	1	0

Set Horizontal Sync Start. Eight pixel increments.

6.3.4 HORIZONTAL SYNC WIDTH REGISTER (WRITE ONLY - ADDRESS 0EE8H)

7	6	5	4	3	2	1	0
0	0						

Bit 5 = Polarity (1 = negative; 0 = positive)
Bits 0-4 = Set Horizontal Sync Width. Eight pixel increments

6.3.5 VERTICAL TOTAL REGISTER (WRITE ONLY - ADDRESS 12E8H)

11	10	9	8	7	6	5	4	3	2	1	0
Set number of lines per frame.											

6.3.6 VERTICAL DISPLAYED REGISTER (WRITE ONLY - ADDRESS 16E8H)

11	10	9	8	7	6	5	4	3	2	1	0
Set number of lines displayed.											

6.3.7 VERTICAL SYNC START REGISTER (WRITE ONLY - ADDRESS 1AE8H)

11	10	9	8	7	6	5	4	3	2	1	0
Set vertical sync start.											

6.3.8 VERTICAL SYNC WIDTH POLARITY REGISTER (WRITE ONLY - ADDRESS 1EE8H)

7	6	5	4	3	2	1	0
0	0						
Bit 5 = Polarity (1 = negative; 0 = positive) Bits 0-4 = Set Vertical Sync Width.							

6.3.9 DISPLAY CONTROL REGISTER (WRITE ONLY - ADDRESS 22E8H)

The Display Control DISP_CNTL Register sets various control features for the display functions.

BIT	POSITION
1 & 2	Specify resolution. These bits should match bits 2 and 3 of BEE8-5.
3	Scan. Set to specifies a double scan; 0 specifies a single scan.
4	Interlace. Set to 1 specifies interlaced mode; 0 specifies non-interlaced mode.
5 & 6	Enable Display. Together these bits enable/reset the display. The display is enabled when bits 5 and 6 are set to 01; and reset when set to 10. These bits are not affected by the locked-in extended feature.

		1024 x 768			640 x 480 (4 or 8)	
Frame Rate		43 Hz I	60 Hz NI	70 Hz NI	60 Hz NI	70 Hz NI
pclk		44.90MHz 22.27ns	63.98MHz 15.63ns	74.16MHz 13.46ns	25.18MHz 39.92ns	31.32MHz 31.93ns
02EH	Htotal	9d	a2	a4	63	68
06E8	Hdisplay	7f	7f	7f	4f	4f
0AE8	Hsync position	81	83	83	52	54
0EE8	Hsync & polarity	16	16	16	2c	2c
12E8	Vtotal	660	660	642	830(4) 418 (8)	848 (4) 426 (8)
16E8	Vdisplay	5fb	5fb	5fb	779(4) 3bb(8)	779 (4) 3bb (8)
1AE8	Vsync position	600	600	600	7a8 (4) 3d2 (8)	7b8 (4) 3de (8)
1EE8	Vsync & polarity	8	8	8	22	22
22E8	Control	33	23	23	21 (4) 23 (8)	21 (4) 23 (8)
Htotal	µ	28.25	20.38	17.80	31.78	26.82
Hdisp.	µ	22.89	16.00	13.81	25.42	20.44
Hblank	µ	5.37	4.376	3.99	6.355	6.39
Hsync	µ	3.93	2.751	2.373	3.813	3.07
Hfporch	µ	0.178	0.375	0.323	0.636	1.02
Hbporch	µ	1.25	1.250	1.294	1.906	2.30
Vtotal	ms	23.08	16.65	14.29	16.68	14.24
Vdisp.	ms	21.70	15.65	13.67	15.25	12.87
Vblank	ms	0.706 (even) 0.678 (odd)	0.999	0.623	1.430	1.368
Vsync	ms	0.113	0.082	0.071	0.079	0.067
Vfporch	ms	0.0141 (even) 0 (odd)	0.020	0.018	0.350	0.402
Vbporch	ms	0.579 (even) 0.565 (odd)	0.897	0.534	1.00	0.898
HS polarity	ms	+	+	+	-	-
VS polarity	ms	+	+	+	-	-

TABLE 23. CRT CONTROL REGISTER PARAMETERS AND TIMING

6.4 ROM PAGE SELECT REGISTER (WRITE ONLY - ADDRESS 46E8 MC/36E8 AT)

The ROM Page Select (ROM_PAGE_SEL) Register is used by the CIU to enable ROM bank selection and select a bank of ROM. The register format for bank selection is shown below. Bit 3 enables/disables bank selection. This register is remapped to 36E8h for AT Bus because VGA used the 46E8h register.

7	6	5	4	3	2	1	0
U	U	U	U	I			
Bits 0-2 select the ROM bank							

2 1 0	Select Bank
0 0 0	0
0 0 1	1
0 1 0	2
1 1 1	3
1 0 0	4
1 0 1	5
1 1 0	6
1 1 1	7

6.5 SUBSYSTEM CONTROL REGISTER (WRITE ONLY - ADDRESS 42E8H)

The Subsystem Control (SYBSYS_CNTL) Register is used for interrupt and reset control of the WD9500 FIFO and other CPU interface functions. This register affects Bits 3-0 of the Subsystem status (SUBSYS_CNTL) Register (see "Subsystem Status Register").

BIT	POSITION
0	Puts a 0 in the vertical sync status bit of the IS Register that can be read at address 42E8h. (1 = clear; 0 = no change)
1	Puts a 0 in the GE busy status bit of the IS Register; readable at address 42E8h. (1 = clear; 0 = no change)
2	Puts a 0 in the FIFO overflow status bit of the IS Register; readable at address 42E8h. This bit is cleared at the end of every line during a reac across the plane. (1 = clear; 0 = no change)
3	Puts a 0 in the FIFO empty status bit of the IS Register; readable at address 42E8h. (1 = clear; 0 = no change)
8	Enables/disables the vertical sync interrupt. (1 = enable; 0 = disable)
9	Enables/disables the GE busy interrupt. (1 = enable; 0 = disable)
10	Enables/disables the FIFO overflow interrupt. (1 = enable; 0 = disable)
11	Enables/disables the FIFO empty interrupt. (1 = enable; 0 = disable)
12 & 13	Selects normal mode or test mode.
14 & 15	Graphic Engine Reset - Used to switch between normal mode and reset.

Bit 13	Bit 12	
0	0	No Change
0	1	Normal
1	0	Test

Bit 15	Bit 14	
0	1	Normal
1	0	Reset
0	0	No Change

6.6 DRAWING CONTROL REGISTERS

There are sixteen registers involved in drawing control. These registers affect the operation of the GP, DP, MIC and CIU Current Y Position Register.

6.6.1 CURRENT Y POSITION REGISTER (READ/WRITE - ADDRESS 82E8H)

The 16-bit CUR_Y Register at address 82E8h uses Bits 10-0 to define the current position of Y for the pixel being drawn. The value is 11 bits unsigned. Bit 11 is reserved for higher resolution. WD9500's enhanced resolution (1280x1024) mode does not use this bit.

BIT	POSITION
0-10	Current Y of drawing point value
11	Reserved
12-15	Unused

6.6.2 CURRENT X REGISTER (READ/WRITE - ADDRESS 86E8H)

The CUR_X Register at address 82E8h uses Bits 10-0 to define the current position of X for the pixel being drawn. The value is 11 bits unsigned. Note that Bit 11 is reserved for higher resolution. WD9500's enhanced resolution (1280x1024) mode does not use this bit. The status of this register can be read.

BIT	POSITION
0-10	Current X of drawing point value
11	Reserved
12-15	Unused

6.6.3 DESTINATION Y POSITION/AXIAL STEP CONSTANT REGISTER (WRITE ONLY - ADDRESS 8AE8H)

The command performed is specified by the Command (CMD) Register. Value is 12 bits unsigned when line drawing is specified. The minterm for the line drawing is: (Increment 1 = 2*(min(|dx|,dy|)).

BIT	POSITION
Line Drawing Mode: Increment line parameter 1.	
0-11	Defines increment 1 value
12-15	Unused
BITBLT Copying Mode: Copy Y Destination	
0-10	Defines Y destination
11	Reserved
12-15	Unused

6.6.4 DESTINATION X POSITION/DIAGONAL STEP CONSTANT REGISTER (WRITE ONLY - ADDRESS 8EE8H)

The command performed is specified by the Command (CMD) Register. Value is 12 bits unsigned when line drawing is specified. The minterm for the line drawing is: (Increment 1 = 2*(min(|dx|,dy|)-max(|dx|,dy|)).

BIT	POSITION
Line Drawing Mode: Increment line parameter 2.	
0-11	Defines increment 2 value
12-15	Unused
BITBLT Copying Mode: Copy X Destination	
0-10	Defines X destination
11	Reserved
12-15	Unused

6.6.5 ERROR TERM REGISTER (READ/WRITE - 92E8H)

The minterm for the line drawing is: 2*[min(dx|,|dy)]-max(|dx,dy|)-1 if starting x ending x, and 2*[min(|dx,|dy|)] - max(|dk|,|dy|) if starting x = ending x. The status of this register, when read after line drawing, is sign extended to 16 bits.

BIT	POSITION
0-12	Defines the delta for the current line drawing. Value is 13 bits signed 2's complement.
13-15	Sign extension.

6.6.6 MAJOR AXIS PIXEL COUNT REGISTER (WRITE ONLY - ADDRESS 96E8H)

This parameter is used for line drawing. BITBLT, or rectangle commands. The value is 11 bits unsigned. When line drawing is specified, the minterm for the line drawing is: Line Parameter = max(|dx|,|dy|). For BITBLT or rectangle commands, Rectangle Width Value = Rectangle Width -1.

BIT	POSITION
0-10	Defines either the width for a rectangle in BITBLT or rectangle mode or defines the length of a line in a line draw.
11-15	Unused

6.6.7 COMMAND REGISTER (WRITE ONLY - ADDRESS 9AE8H)

The CMD Register at Address 9AE8h provides commands for drawing. All parameters have to be set before this command is sent to activate the drawing.

BIT	POSITION
0	R/W: 1 = Write; 0 = Read.
1	Pixel mode: 1 = multi; 0 = single.
2	Last pixel: 1 = off; 0 = on.
3	DIR type: 1 = deg; 0 = XY
4	Draw: 1 = yes; 0 = no.
5-7	Drawing Direction
8	Wait: 1 = yes; 0 = no.
9	Bus select: 1 = 16; 0 = 8.
10	Don't care
11	Reserved
12	Swap MSB/LSB: 1 = yes; 0 = no.
13-15	Drawing function command

BITS	DRAWING DIRECTION	
7 6 5	Bit 3 = 1	Bit 3 = 0
0 0 0	0 degrees	Y neg, X major, X neg
0 0 1	45 degrees	Y neg, X major, X pos
0 1 0	90 degrees	Y neg, Y major, X neg
0 1 1	135 degrees	Y neg, Y major, X pos
1 0 0	180 degrees	Y pos, X major, X neg
1 0 1	225 degrees	Y pos, X major, X pos
1 1 0	270 degrees	Y pos, Y major, X neg
1 1 1	315 degrees	Y pos, Y major, X pos

BITS 7 6 5	DRAWING FUNCTION COMMAND
0 0 0	No operation
0 0 1	Draw line
0 1 0	Fill rectangle (Hor. 1st by 4 hor. pixels); Search & fill (see BEE8-A)
0 1 1	Fill rectangle (Vert. 1st by 2 vert. pixels - see BEE8-A)
1 0 0	Fill rectangle (vert. 1st by 4 hor. pixels)
1 0 1	Draw line (polygon boundary)
1 1 0	BITBLT
1 1 1	Not defined

6.6.8 COMMAND REGISTER (WRITE ONLY - ADDRESS 9AE8H)

BIT	FUNCTION
0	R/W: specifies a read operation when set to 0 or a write operation when set to 1.
1	Pixel Mode: specifies single pixel mode when set to 0 or a multi-pixel mode when set to 1.
2	Last pixel Off: specifies the last pixel drawn when set to 0; turned off when set to 1.
3	Dir type: specifies the type of line drawing direction as either radial
4	Draw: Specifies draw when set to 1and updates the drawing point only when set to 0.
5-7	Drawing Direction: Specifies the direction of the draw using the direction type indicated by Bit 3.

			4	3	2	1	0	
			Plane 3	Plane 2	Plane 1	Plane 0		**4-bit Bit Plane**
BITBLT	7	6	5	4				
	Plane 6	Plane 5	Plane 4	Plane 3	Plane 2	Plane 1	Plane 0	Plane 7	**8-bit Bit Plane**
	7	6	5	4	3	2	1	0
	Plane 7	Plane 6	Plane 5	Plane 4	Plane 3	Plane 2	Plane 1	Plane 0

* = Plane number corresponds to bit number for search and fill

For each plane: 1 = use source; 0 = do not use source

FIGURE 4. BIT PLANE READ MASK REGISTER

BIT	FUNCTION (CONT'D)
8	Wait: Provides a wait state when set to 1 to allow waiting for CPU data during functions such as image transfer and texture line drawing.
9	Bus Select: Specifies that the 16-bit data bus is selected when set to 1; the 8-bit data bus is selected when set to 0.
10	Future: Allows the PAM to interface with two PDM chips. This capability is not currently supported.
12	Swap MSB/LSB: When set to 1, specifies that the most significant byte (MSB) be swapped with the least significant byte (LSB) when the 16-bit data bus is selected. Bit 12 is normally set to 0; the MSB is drawn first, then the LSB.
13-15	Command type: Specify the commands for drawing.

6.6.9 SHORT STROKE VECTOR TRANSFER REGISTER (WRITE ONLY - ADDRESS 9EE8H)

Provides two types of data. Each byte specifies the length, direction, and move draw control for a short vector.

BITS	FUNCTION
0-3, 8-11	Pixel line length
4, 12	Move/Draw: Indicates a drraw function when set to 1; indicates a move function when set to 0.
5-7, 13-15	Drawing direction: Specifies the direction of the draw when using the direction type, either radial-based or coordinate-based, as specified by Bit 3 of the CMD register.

BITS	DRAWING DIRECTION	
15 14 13 7 6 5	**Command Register: Bit 3 = 1**	**Bit 3 = 0**
0 0 0	0 degrees	X major, X neg (Left)
0 0 1	45 degrees	X major, X pos (Right)
0 1 0	90 degrees	Y major, Y neg (Up)
0 1 1	135 degrees	Y major, Y neg (Up)
1 0 0	180 degrees	X major, X neg (Left)
1 0 1	225 degrees	X major, X pos (Right)
1 1 0	270 degrees	Y major, Y pos(Down)
1 1 1	315 degrees	Y major, Y pos(Down)

6.6.10 BACKGROUND COLOR REGISTER (WRITE ONLY - ADDRESS A2E8H)

The BKGD_COLOR Register specifies the background color. The MSB in this 8-bit word is not used.

6.6.11 FOREGROUND COLOR REGISTER (WRITE ONLY - ADDRESS A6E8H)

The FRGD_COLOR Register specifies the foreground color. The MSB in this 8-bit word is not used

6.6.12 WRITE MASK REGISTER (WRITE ONLY - ADDRESS AAE8H)

Specifies the bit-plane selected for graphics or text update. The MSB in this word is not used.

BIT	FUNCTION
0-7	Planes 0-7

6.6.13 READ MASK REGISTER (WRITE ONLY - ADDRESS AEE8H)

Specifies the read source mask for Image read or fill operations. The value is the true mask rotated left one bit. Bit 0 is the mask for plane 7 and bits 1-7 are the mask bits for planes 0-6, respectively. However, for polygon fill, bits 2, 3, and 4 are for planes 2, 3, and 4, respectively. The MSB in this word is not used. See Figure 4.

6.6.14 COLOR COMPARE REGISTER (WRITE ONLY - ADDRESS B2E8H)

Specifies the comparison color. The MSB in this 8-bit word is not used.

6.6.15 BACKGROUND MIX REGISTER (WRITE ONLY - ADDRESS B6E8H)

Specifies the background mix. The MSB in this word is not used.

BIT	FUNCTION
0-4	Background mix command
5,6	Color select

BITS 6 5	BACKGROUND SOURCE SELECT
0 0	BGC
0 1	FGC
1 0	CPU data
1 1	Display memory

6.6.16 FOREGROUND MIX REGISTER (WRITE ONLY - ADDRESS BAE8H)

Specifies the foreground mix. The MSB in this 16-bit word is not used.

BIT	FUNCTION
0-4	Foreground mix command
5,6	Color select
7-15	Unused

BITS 6 5	FOREGROUND SOURCE SELECT
0 0	BGC
0 1	FGC
1 0	CPU data
1 1	Display memory

BITS 4-0	FOREGROUND MIX COMMAND
00	Not screen
01	Zero
02	One
03	Leave alone
04	Not new
05	Xor
06	Not screen xor new
07	Overpaint
08	Not screen or not new
09	Screen or not new
0A	Not screen or new
0B	Screen or new
0C	Screen and new
0D	Not screen and new
0E	Screen and not new
0F	Not screen and not new
10	Minimum
11	(Screen-new) without saturate
12	(New-screen) without saturate

BITS 4-0	FOREGROUND MIX COMMAND
13	(New+screen) without saturate
14	Maximum
15	(Screen-new)/2 without saturate
16	(New-screen)/2 without saturate*
17	Average = (new + screen)/2 w/o saturate
18	(Screen-new) with saturate
19	(Screen-new) with saturate
1A	(New-screen) with saturate
1B	(New+screen) with saturate
1C	(Screen-new)/2 with saturate
1D	(Screen-new)/2 with saturate
1E	(New-screen)/2 with saturate**
1F	(Screen + new)/2 with saturate
*Borrow included in shifting	
**Set to 0 in borrow = 1	

6.6.17 MULTIFUNCTION CONTROL REGISTER (WRITE ONLY - ADDRESS BEE8-0,1,2,3,4)

Specifies several drawing control parameters. Bits 15-12 control the use of this register when these bits are changed, the register changes function.

BIT	FUNCTION
0-10	Rectangle/clipping parameter value
11	Reserved (don't care for BEE8-0)
12-15	Drawing select

15 14 13 12	ADDR	PARAMETER
0 0 0 0	BEE8-0	Minor Axis Pixel Count Index
0 0 0 1	BEE8-1	Top Scissors Index
0 0 1 0	BEE8-2	Left Scissors Index
0 0 1 1	BEE8-3	Bottom Scissors Index
0 1 0 0	BEE8-4	Right Scissors Index

Minor Axis Pixel Count Index (MIN_AXIS_PCNT) - When bits 15-12 are set to 0, the value of bits 10-0 specifies the rectangle height. Value = rectangle height - 1
Top Scissors Index (SCISSORS_T) - When bits 15-12 are set to 1, the value of bits 10-0 specifies the clipping window top limit.
Left Scissors Index (SCISSORS_L) - When bits 15-12 are set to 3, the value in bits 10-0 specifies the clipping window left limit.
Bottom Scissors Index ((SCISSORS_B) - When bits 15-12 are set to 3, the value of bits 10-0 specifies the clipping window bottom limit.
Right Scissors Index (SCISSORS_R) - When bits 15-12 are set to 4, the value in bits 10-0 specifies the clipping window right limit.
Note: Reading display memory outside of the clipping window returns the content of that memory location.

6.6.18 MEMORY CONTROL INDEX REGISTER (WRITE ONLY - ADDRESS BEE8-5)

BIT	FUNCTION
0,1	X coordinate control: Reserved, Bit 0 should be set to 0. Bit 1 should be set to 1. X coordinate control.
2,3	Specifies resolution- Y coordinate control.
4	Specifies planes for drawing: 0 specifies lower 4 planes; 1 specifies upper 4 planes.
5-7	Reserved
8-11	Unused
15-12	Selects memory configuration when set to 0101.

Y Coordinate Control	3 2	Resolution
Skip Z & YI	0 0	640x480x4 (Bit 1 of 22E8H must be 0)
Skip Y2	0 1	1024x768 or 640x480x8
Not used	1 0	Not defined
Not used	1 1	Not defined

6.6.19 FIXED PATTERN LOW INDEX REGISTER FIXED PATTERN HIGH INDEX REGISTER (WRITE ONLY - ADDRESS BEE8-8, BEE8-9)

BIT	POSITION
0	Bit 0 = 0
5-11	Unused
Fixed Pattern Low Index Register (PATTERN_L):	
4-1	Specifies pixel position mix control for pixels 0-3. A 0 selects the background color source; 1 selects the foreground color source (if enabled by bits 6,7 of the Pixel Control Index Register.
15-12	When set to 8, Fixed Pattern Low is selected.
Fixed Pattern High Index Register (PATTERN_H):	
4-1	Specifies pixel position mix control for pixels 4-7. A 0 selects the background color source; 1 selects the foreground color source (if enabled by bits 6,7 of the Pixel Control Index Register.
15-12	When set to 9, Fixed Pattern High is selected.

6.6.20 PIXEL CONTROL INDEX REGISTER (WRITE ONLY - ADDRESS BEE8-A)

BIT	POSITION
0	Bit 0 = 0
1	Mask select poly-fill operations. Read mask = 0; write mask = 1.
2	Packed Data/Search Enable
3-5	Data compare
6-7	These bits define the source of the bit pattern used to select color and the mix operation to be used.
11-8	0000
15-12	1010

Bit 2	Packed Data		Use
1	Enabled	Read	Read packed data
		Write	Search and fill mode
0	No	Read/Write	Normal

BITS 3-5	COMPARISON TYPE
0	False (always draw)
1	True (never draw)
2	Plane data > = comparison
3	Plane data < comparison
4	Plane data <> comparison
5	Plane data = comparison
6	Plane data <= comparison
7	Plane data > comparison

7 6	**Data Extension** Bit pattern from the following source	**Use** Depending on the color source and mix
0 0	Bit pattern always = 1; BGRD_MIX not used.	BAE8h bits 6,5 = 01 → regular solid BAE8h bits 6,5 = 10 → regular image write BAE8h bits 6,5 = 11 → regular BIT BLT
01	Pixel position mix control (BEE8-8,9)	BAE8h bits 6,5 = 01 → horizontal text line B6E8h bits 6,5 = 00 → horizontal text line
1 0	CPU pixel data	FMX → CPU 10-bit pattern image BMX → transfer to display memory BAE8h bits 6,5 = 01; B6E8h = 00 : image write across the plane or from 1 bit plane to FGC and BGC

Bits 7 6	Data Extension Bit pattern from the following source	Use Depending on the color source and mix
10	Display memory used to display packed data* bit pattern	BAE8h bits 6,5 = 01; B6E8h bits 6,5 = 00: BITBLT across the plane or from 1 bit plane to FGC and BGC BAE8h bits 6,5 = 10; B6E8h bits 6,5 = 00: Special multi-color marker mode**

* Packed data - When in an operation involving read, packed data is computed from the source. Packed Data is defined as "the screen data ORed with the complement of the bit plane read mask". If the result is all 1's, then 1 is extracted, otherwise 0 is extracted per pixel. When a write operation is selected, WD9500 goes into a special search and fill mode. The screen data is read and if the packed data extracted is 0, write operation is suspended. When a paced data "1" is encountered, write operation is enable until the next "1". This mode is used to detect the boundary of a polygon for fill operation.

** Marker - special BITBLT mode used for multi-color marker. A 10 pattern is stored in display memory. During BITBLT, if display memory data = 1, CPU data is used.

6.6.21 PIXEL DATA TRANSFER REGISTER (READ/WRITE - ADDRESS E2E8H)

The Pixel Data Transfer (PIX_TRANS) Register specifies the read/write port for image transfer. For across the plane image transfer, read/write data is determined by nibble boundary on the screen. The starting point will fall on the first nibble group for word mode, two nibbles of data can be transferred for each read/write. For through the plane image transfer, two pixels can be transferred for each read/write operation in work mode.

BIT	FUNCTION
	Across The Plane
0, 6-8, 13-15	Unused
4-1	Pixel read/write value: Pixels 4-7
12-9	Pixel read/write value: Pixels 0-3
	Through the Plane
0-7	Pixel 2: bp0-bp7
8-15	Pixel 1 if 16-bit mode selected: bp0-bp7
Note: For Image Read operation, all data (including the last pixel) must be read from the CPU before issuing a new command to the Graphics Processor.	

6.7 STATUS REGISTERS

There are three status registers that can be read to acquire information: the Subsystem Status (SUBSYS_STAT) register at address 42E8h, the Graphics Processor Status (GP_STAT) register at address 9AE8h, and the Display Status (DISP_STAT) register at address 02E8h.

6.7.1 SUBSYSTEM STATUS REGISTER (READ ONLY - ADDRESS 42E8H)

Subsystem Status Register (SUBSYS_STAT) Register provides interrupt status, monitor ID, and plane size.

BIT	FUNCTION
0	Vsync: when set to 1, it indicates a vertical sync interrupt.
1	GE Busy: When set to 1, indicates GE busy.
2	FIFO Overflow: When set to 1, indicates FIFO overflow.
3	FIFO Empty: When set to 1, indicates FIFO empty.
4-6	Monitor ID: Indicates the monitor type being driven by the WD9500 or 8514/A.
7	Plane size: Indicates a 4-bit planae when set to 0 or an 8-bit plane when set to 1.
8-15	Reserved for hardware test

Address Decoding Table for Read				
Bits 15-12 / 11-0	**2e8**	**6e8**	**ae8**	**ee8h**
0	2e8	2e8	2e8	2e8
1	2e8	2e8	2e8	2e8
2	2e8	2e8	2e8	2e8
3	2e8	2e8	2e8	2e8
4	42e8	42e8	42e8	42e8
5	42e8	42e8	42e8	42e8
6	42e8	42e8	42e8	42e8
7	42e8	42e8	42e8	42e8
8	82e8	86e8	0*	0*
9	92e8	0*	9ae8	0*
a	e2e8	e2e8	0*	0*
b	0*	0*	0*	0*
c	82e8	86e8	0*	0*
d	92e8	0*	9ae8	0*
e	e2e8	e2e8	0*	0*
f	0*	0*	0*	0*
* A value of zero will be read.				
Address Decoding Table for Write				
Bits 15-12 / 11-0	**2e8**	**6e8**	**ae8**	**ee8h**
0	2e8	6e8	ae8	ee8
1	12e8	16e8	1ae8	1ee8
2	22e8	X	X	X
3	X	X	X	X
4	42e8	46e8	4ae8	X
5	42e8	46e8	4ae8	X
6	42e8	46e8	4ae8	X
7	42e8	46e8	4ae8	X
8	82e8	86e8	8ae8	8ee8
9	92e8	96e8	9ae8	9ee8
a	a2e8	a6e8	aae8	aee8
b	b2e8	b6e8	bae8	bee8
c	82e8	86e8	8ae8	8ee8
d	92e8	96e8	9ae8	9ee8
e	a2e8	a6e8	aae8	aee8
f	b2e8	b6e8	bae8	bee8

TABLE 24. ADDRESS DECODING TABLES FOR 8514/A REGISTERS

6 5 4	Monitor ID
0 1 0	8514/A color 16"
1 0 1	VGA 8503 mono 12"
1 1 0	VGA 8513 color 12"
1 1 0	VGA 8512 color 14"
1 1 1	No monitor or other monitor

6.7.2 GRAPHICS PROCESSOR STATUS REGISTER (READ ONLY - ADDRESS 9AE8H)

Provides FIFO status information. PC read data status, and hardware busy status.

BIT	FUNCTION
7-0	FIFO Entries 7-0: Indicates data status of the FIFO (i.e., a 1 indicates that an input entry is occupied by data.
8	Data Available: Indicates that PC read data is available when set to1; not available when set to 0.
9	Hardware Busy: Indicates that the hardware is busy when set to 1; not busy when set to 0.
15-10	Not used.

6.7.3 DISPLAY STATUS REGISTER (READ ONLY - ADDRESS 02E8H)

Provides video status information.

BIT	FUNCTION
0	Analog RGB signal test: 0 = R, G, or B greater than 0.30 volts; 1 = R, G, and B all less than 0.30 volts
1	Vertical Sync
2	Line Count
3	0
4-15	Unused

Table 24 illustrates how the addresses are decoded for 8514/A compatible registers. The left most column gives the hexadecimal value of address bits 15-12, and the top row shows the value of the rest of the twelve address bits, for example, the read address A2E8 (hex) is decoded as "E2E8" column at the a-th row. This also means an I/O read from A2E8 is the same as if reading from address E2E8, the IRW register. Address decoding for read is different from that for write.

6.8 SOFTWARE INTERFACE EXTENSIONS

25

Suitable CPU Adapter Interface software (AI), such as the Western Digital Adapter Interface (WDAI) can make use of the WD9500's advanced capabilities by invoking "Western Digital Enhanced Mode" on a short-term basis, as explained later There two consequences to this software interface design. First, a WD9500-based board can be inserted into a system with no change in software, and it will function as a faster 8514/A. Second, it provides for performance enhancement for custom software. In order to minimize future register conflict, all functions for Western Digital Enhanced Mode are implemented using one register address, 96E8h. A dummy IO read at address 28E9h must precede any access to 96E8h for Western Digital Enhanced Mode. Under 8514/A emulation mode. 96E8h is a write only register for Rectangle Width.

Extended Register Operation To identify the WD9500 chip set, see Figure 5. To escape to Western Digital Enhanced Mode, the AI should execute a byte read of I/O address 28E9h. (The purpose of the byte read is to perform the escape; the WD9500 does not return any data). This operation is a no-op for the IBM 8514/A since it involves a write-only register, which furthermore does not respond to any access to an odd-numbered byte address. This operation will tag the next register access through a special bit in the FIFO. FIFO is fully functional in Western Digital Enhanced Mode. After escaping to Western Digital Enhanced Mode, the WD9500 will automatically reset itself back to 8514/A emulation mode in one of these four circumstances:

1. If, as its next board access immediately after the escape, the AI reads the Western Digital Status Register (I/O address 96E8h).

2. If, as its next board access immediately after escape, the AI writes to one of the six Western Digital Control Registers, or to the Rectangle Width Register (I/O address 96E8h).

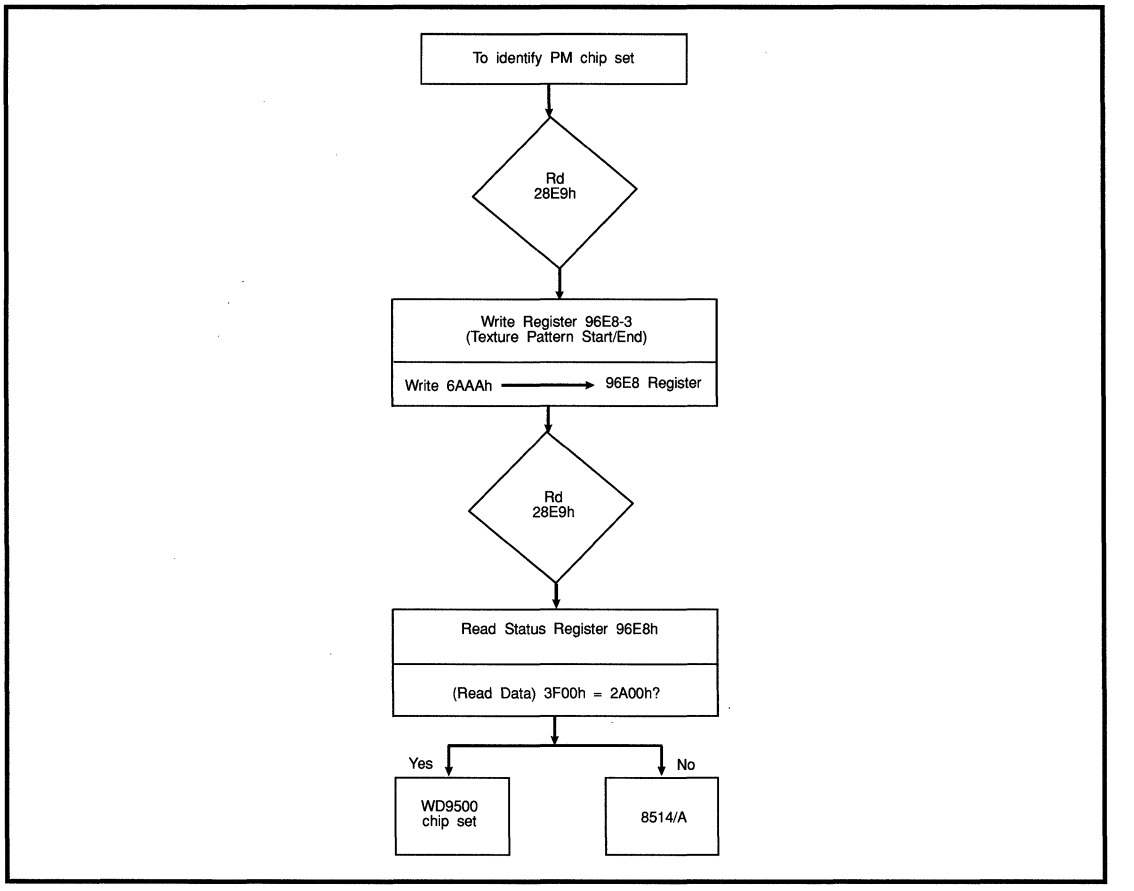


FIGURE 5. METHOD OF IDENTIFYING WD9500 CHIP SET

3. If, as its next board access immediately after an escape, the AI writes to either I/O address 82E8(register name in 8514/A Emulation Mode: Copy Y Destination/Incr 1 Register). Figure 5. Method of Identifying WD9500 Chip Set.

The purpose of the second two, however, deserves explanation. Western Digital enhancements simplify and speed line drawing commands in two ways: first, line drawing parameters are simpler, in that the AI needs to specify only the pixel coordinates of the line's end point, rather than the tediously calculated parameters used by the 8514/A. Therefore, the WD9500 needs to be in Western Digital Enhanced Mode to "know" that the write into register 8AE8 contains the Y ending point parameter, in preparation for line-drawing command (case 4). Second, in 640x480 resolution, the WD9500 can, through Western Digital Enhanced Mode, make use of a much simpler Y-coordinate format than is required by the 8514/A, and therefore must be "told" by being in Western Digital Enhanced Mode, that this simpler format is being written to one of the Y-coordinate registers (82E8 or 8AE8, case 3 above). The parameters are defined in this chapter in "Enhanced Solid Line Drawing".

The same system I/O address (96E8) is used to access the Western Digital Status Register, and all six of the Western Digital Control Register. In 8514/A Emulation Mode, this address is that of the Rectangle Width Register.

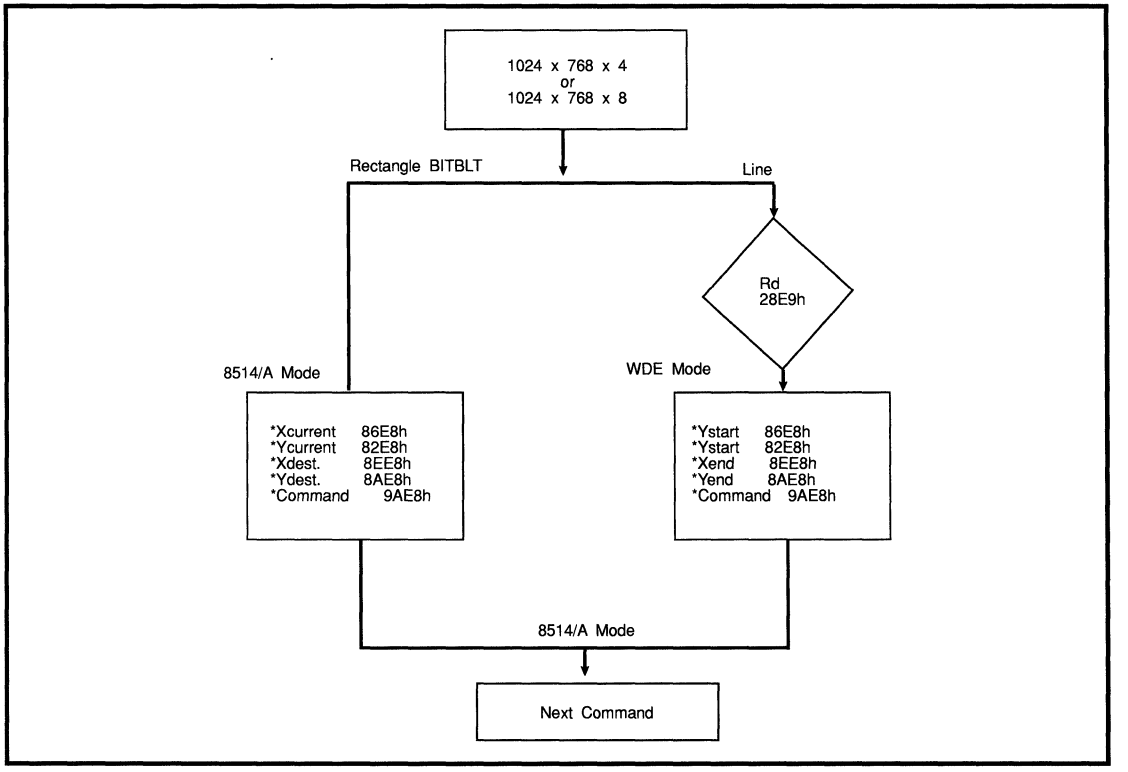


FIGURE 6. WD ENHANCED MODE USAGE IN 1024 X 768 RESOLUTION

6.8.1 WESTERN DIGITAL ESCAPE REGISTER (READ ONLY - ADDRESS 28E9)

A read of the Western Digital Escape Register allows access to WD enhancements. The data returned is not significant.

6.8.2 WESTERN DIGITAL STATUS REGISTER (READ ONLY - 96E8H)

BIT	FUNCTION
0	VRAM type: 1 = 256k; 0 = 64k
1,2	Indicates the number of VRAM chips
3	Resolution: indicates the maximum resolution permitted by the VRAM design. When set to 0, it indicates 1024x768; when set to 1, it indicates 1280x1204.
4	Pal Write: indicates whether a palette write is pending. When set to 0, a palette write is not pending; when set to 1, a palette write is pending.
5	DAC Type: Indicates whether the DAC used is 6-bit only or a switchable 6-bit/8-bit. The 6-bit/8-bit DAC allows compatibility at 6-bit color to 8514/A and a large 8-bit color palette that requires special programming. 1 = 6/8 bit color; 0 = 6-bit color only.
7, 6	Monitor Selection
13-8	Current texture pattern position
15, 14	Chip set revision number

A byte read at 28E9 followed by a 16-bit read of this address, 96E8, yields the contents of the

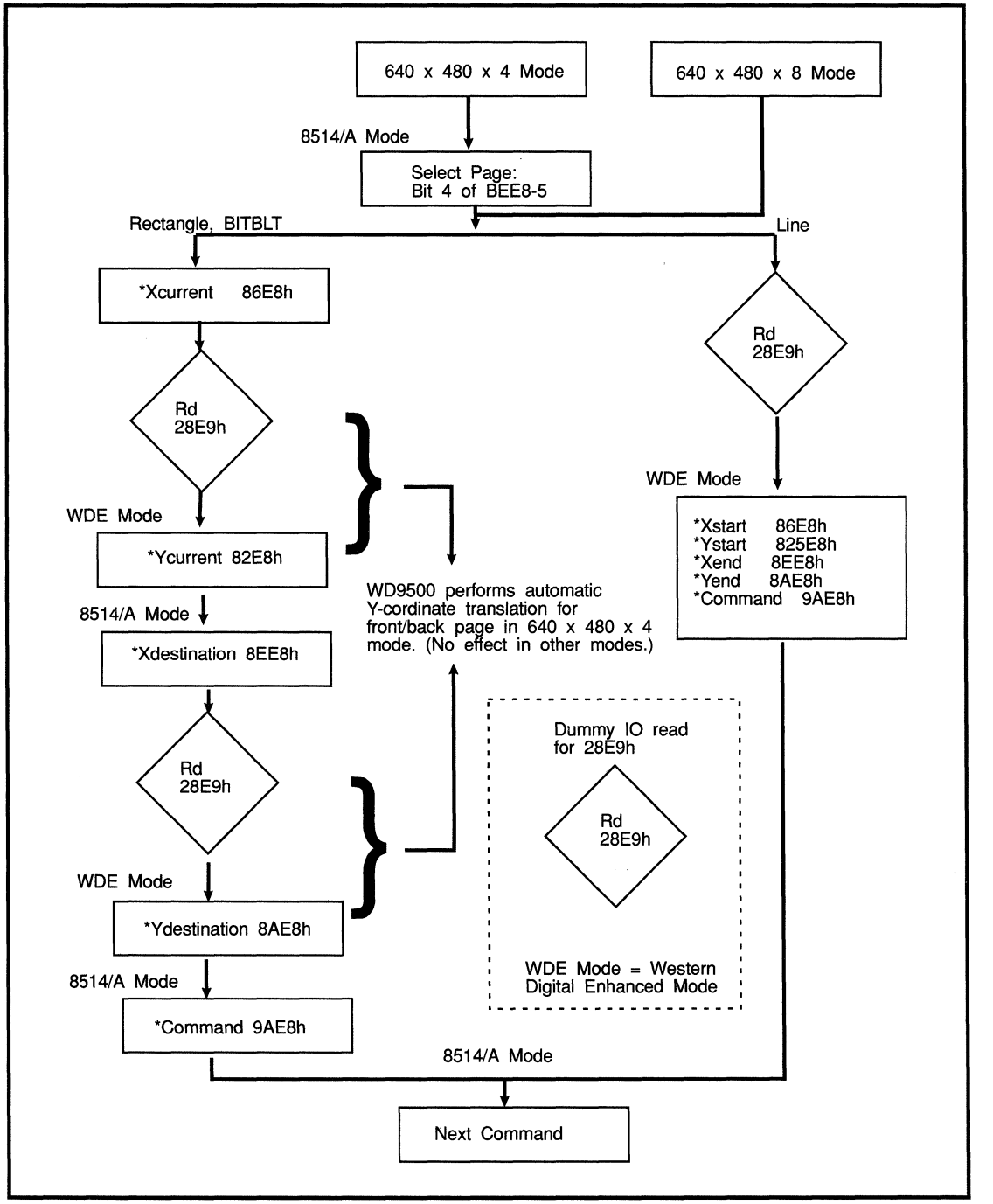


FIGURE 7. WD ENHANCED MODE USAGE IN 640 X 480 RESOLUTION

Western Digital Status Register. Note that in 8514/A Emulation Mode, 96E8 is a write-only register.

6.8.3 WESTERN DIGITAL CONTROL REGISTER (WRITE ONLY - ADDRESS 96E8)

In Western Digital Enhanced Mode, when a 16-bit write is made to address 96E8, theWD9500 interprets the high 3-bits as a selection of one of six Western Digital Control Register destinations for the lower 13 bits of data. In this sense, address 96E8 can be thought of as a "gateway" for writes to the six Western Digital Control Registers, and the notations 96E8-1,96E8-2,...., 96E8-7 are used to refer to those registers. Note also that this design provides "double insurance" against accidental 8514/A-mode access to these registers: first, they can be accessed only after escaping to Western Digital Enhanced Mode; second, the rectangle width parameter should never be so large as to involve 1-bits in the high three bit positions of the 16-bit data (and in fact, "96E8-1)" leads to the "real" rectangle width register). When Bits 15-13 are set to 3, bits 12-6 specify the texture pattern ending position and Bits 5-0 specify the texture pattern starting position within the 48 bits available in the four texture pattern registers (see "Textured Line Drawing" in this chapter), bit 12 is unused. The following table defines the Western Digital Enhanced Mode Register (ie., bits 12-0 of 96E8 when bits 15-13 = 001). All the control fields in this register are one-bit mode control; they select between two alternate modes, and the selected mode remains in effect through all future operations until the AI changes it by inverting the associated control bit.

BIT	FUNCTION
0	Pixel Depth: Specifies the number of bit planes t o be used in all operations. Four-bit planes are specified when set to 0; 8-bit planes are specified when set to 1.
1	Page Select Draw: In modes other than 640x480x4, bit 1 specifies screen page selection for drawing (if the VRAM supports two screen pages at the current resolution). Page 1 is selected when set to 0 and page 2 is selected when set to 1. Note that the page select controls provide a simple mechanism for drawing in the background so that the user can instantly replace one screen image with another.
2	Page Select View: In modes other than 640x480x4, bit 2 specifies screen page selection for viewing (source of screen refresh). Page 1 is selected when set to 0 and page 2 is selected when set to 1. Note that the 1 is selected when set to 0 and page 2 is selected when set to 1. Note that the page select controls provide a simple mechanism for drawing in the background so that the user can instantly replace one screen image with another.
3	Mode Extension: In conjunction with bit 2 of register 4AE8 this bit is used to select different resolutions. Bit 3 = 0 is the default for 8514/A resolution modes (i.e., 1024x768 and 640x480).
4	Flicker-free mode: specifies flicker-free palette loading mode control. Setting this bit to 1 enables this mode and a 0 clears the mode.
5	Texture Mode: specifies Western Digital textured line mode. Setting this bit to 1 enables this mode and a 0 clears the mode.

MODE EXT.	8513/A MODE	MONITOR TYPE (BIT 8)	VERTICAL REFRESH FREQUENCY (BIT 7)	CLKSEL 2-0
0	0	X	0	**000**, 640x480, 60 Hz
0	0	X	1	**100**, 640x480, 70 Hz
0	1	0	0	**001**, 1024x768, 43 Hz
0	1	1	0	**011**, 1024x768, 60 Hz
0	1	X	1	**111**, 1024x768, 70 Hz

BIT	FUNCTION
6	DAC Palette: Used only if the board has a 8/6 bit/color switchable DAC. (See Selection, Western Digital Status Register.) Bit 6 = 1 selcts 6-bit/color mode (default); Bit 6 = 1 = 8-bit DAC.
8-7	Monitor Type and Vertical Refresh Frequency: Combined with the mode extension bit and 8514/A bit (Bit 2 of 4AE8) sets the CLKSEL values that select the pixel clock frequency. Bit 2 of 4AE8 automatically selects a proper frequency after the control bits are programmed by the BIOS. When bit 7 is set to 0, it selects a vertical refresh frequency of 60 Hz or 43 Hz; when set to 1, it selects 70 Hz. When bit 8 is set to 0, it selects a 43 Hz monitor type; when set to 1 it selects 60 Hz/70 Hz.
9	Standard Video Registers Enable: Controls the programming of the standard video registers. The default 0 setting disables loading.
10	Standard Video Registers Ena ble: Controls the programming of the alternate video registers (WD9500 extended feature). The default 0 setting disables loading.
11	When set, causes a wait on I/O read or write cycles (when address bit 14 is set). Bit 11 = 0 = disable wait.

BIT	FUNCTION
12	Specifies the length of wait for I/O access when address bit 14 is set. A 0 specifies 4.8 µseconds; 1 specifies ? µseconds.
15-13	Western Digital Control Register Select

BITS 15 14 13	Western Digital Control Registers
0 0 0	Rectangle Width Register (96E8-0) (Same as regular 8514A register)
0 0 1	Western Digital Enhanced Mode Register (96E8-1)*
0 1 0	Reserved (96E8-2)
0 1 1	Texture Pattern Start/End (96E8-3)*
1 0 0	Texture Pattern 11-0 (96E8-4)*
1 0 1	Texture Pattern 23-12 (96E8-5)*
1 1 0	Texture Pattern 35-24 (96E8-6)*
1 1 1	Texture Pattern 47-36 (96E8-7)*

6.8.4 TEXTURE PATTERN START/END REGISTER (WRITE ONLY - ADDRESS 96E8-3)

BIT	FUNCTION
5-0	Starting Bit Position
11-6	Ending Bit Position
12	Reserved
15-13	0 1 1

BITS 10 9	DESCRIPTION
0 1	Load standard video timing registers (default)
1 0	Load alternate video timing registers
1 1	Load both register sets
0 0	Activate automatic switching between register sets and locks registers 4AE8h Bit 2 = 0 (640x480) selects Standard Register Set; bit 2 = 1 (1024x768) selects Alternate Register Set

BIT 3	4AE8 BIT 2	RESOLUTION
0	0	640x480
0	1	1024x768
1	0	800x600
1	1	1280x1024

6.9 ENHANCED SOLID LINE DRAWING

The following procedure should be used to draw a solid line in Wester Digital Enhanced Mode:

1. Escape to Western Digital Enhanced Mode by doing a byte read of I/O address 28E9.
2. Write the X pixel coordinate of the beginning point of the new line to I/O address 86E8 (Current X Drawing Point Register). If this value has not changed since the last drawing operation (i.e. the new line will start witn the X-coordinate of the current drawing point), then instead, the X pixel coordinate of the ending point of the new line should now be written to I/O address 8EE8 (Ending X Register in Western Digital Enhanced Mode), even if that X coordinate has not changed. The reason is that at least one of the two X-coordinate registers must be loaded prior to loading a Y-coordinate register to avoid leaving Western Digital Enhanced Mode prematurely.
3. Write the Y pixel coordinate of the beginning point of the new line to I/O address 82E8 (Current Y Drawing Point Register). If the value has not changed since the last drawing operation (i.e., the new line will start with the same Y-coordinate as where the last one ended), this step may be skipped.
4. Unless already done in step 2, write the X pixel coordinate of the ending point of the new line to I/O address 8EE8 (Ending X Register in Western Digital Enhanced Mode). If this value has not changed since the last drawing operation, this step may be skipped.
5. Write the Y pixel coordinate of the ending point of the new line to I/O address 8AE8 (Ending Y Register in Western Digital Enhanced Mode). This step has to be done to start the line parameter calculation.
6. Conclude by writing the standard line drawing command to the Command Register at I/O address 9AE8.

Western Digital Enhanced Mode simplifies the calculation of Y coordinates when using two pages, including the case of 640x480 resolution. In contrast to the 8514/A Emulation Mode, Western Digital Enhanced Mode requires no transformations; the desired page-oriented Y coordinate can be written directly into the Y-coordinate register. The coordinates will apply to the page selected by their 640x480x4 drawing page selection bit in the MEM_CNTL register In both 8514/A Emulation Mode and Western Digital Enhanced Mode, however, the user must be aware of pixel coordinate usage with regard to boundaries.

First, under all circumstances, X and Y coordinates wrap around at the 2K boundary; in other words, pixel coordinates are processed as 11-bit values and hence manipulated modulo 2048.

Second, under all circumstances, Y coordinates between 1K and 2K are "lost" (i.e., drawn objects or parts of drawn objects whose Y coordinates are between 1K and 2K are not recorded in VRAM.)

Third, where only one page is available (except for the 1280x1024 case), X coordinates between 1K and 2K are similarly "lost" (See below for 1280x1024.)

Fourth, where two pages are available, first-page X coordinates between 1K and 2K will "intrude" into the second page (modulo 1024), and second-page X coordinates between 1K and 2K will intrude into the first page (modulo 1024). The reason is that when two pages are provided, the 1Kx1K pages are arranged "side by side" in physical memory, with the logical (page-oriented) X coordinate internally processed as a physical X coordinate between 0 and 2K. The intrusion can be avoided by establishing clipping boundaries at the 1K page limit (or less).

Finally, images drawn within a (1K by 1K) page but beyond the screen viewing boundary (1Kx768 or 640x480) are not "lost", and can be copied from their "off-screen" location into the viewing area by a BITBLT operation. In the (single page) case of 1280x1024 resolution, off-screen" storage is provided for coordinates between 1280 and 2K.

6.10 TEXTURED-LINE DRAWING

In Western Digital Enhanced Mode, textured lines can be drawn directly. After the "texture pattern" and its pointers have been set up as described below, the AI need only turn on the Western Digital textured-line mode control bits, 7 & 6 of BEE8-A to 01, set bits 6 & 5 of BAE8 to 01, and then use the same procedure as for solid-line drawing (see "Enhanced Solid-Line Drawing" in this chapter). The texture pattern is a string of bits whose 0/1 values are consulted in sequence as the PWGA1 draws the line, applying the current mix to the combination of current texture-pattern bit and current pixel. (For example, a "1" bit in the texture pattern might be interpreted as an overpaint instruction). The pattern may be up to 48 bits long. Four Western Digital Control Registers 96E8-4, 96E8-5, 96E8-6, and 96E8-7 are provided for its storage. (Bit 12 of each of these registers is reserved.) The pattern must be defined beginning at Bit 47, but need not continue to Bit 0; the 6-bit "ending position" field in Western Digital Control Register 96E8-3 is provided to specify the number of its last bit. The related 6-bit "starting position" field, however, is used differently. It specifies where (between Bit 47 and the ending-position bit) the texture-pattern pointer should be placed at the beginning of a textured line-drawing process from that start position toward the defined ending position (i.e., from high-order to low-order bits within the texture pattern); after the WD9500 used the texture-pattern bit at the ending position, it will circulate the pointer back, not to the specified starting position but to Bit 47, and then repeat the process. After the line is complete, the wd9500 will place the current position of the texture-pattern pointer into the appropriate field within the Western Digital Status Register, where it may be read by the AI. If the user does not store a new value into the starting position field, then in its next textured-line-drawing operation, the WD9500 will use the current pointer from the status register. The chief purpose of this feature is convenience in allowing the user to automatically continue a texture pattern from one line to the next without needing to do an explicit read and write of the pointer position; for example, a dashed line will properly turn a corner without user concern for the texture pattern pointer. Note that after board reset, all texture controls, including current position, are undefined, and must be initialized by the AI.

6.11 FLICKER-FREE PALETTE LOADING

When using the IBM 8514/A, the CPU must wait for vertical screen refresh before reloading its color palette, In a high resolution design, however, especially with a non-interlaced monitor, the vertical retrace time (typically less than 600 microseconds) may not be long enough to program all 256 color entries. When the Western Digital flicker-free option is incorporated into the design of a WD9500-based board ("Video DAC and Interface Subsystem" in section 3), the WD9500 can accept palette writes from the CPU at any time, but will buffer them in the DSP until horizontal retrace time; during horizontal flyback, it will write them to the DAC's palette, avoiding flicker. Note that in VGA pass-through mode, any VGA palette-loading operation also loads the DAC on the 8514/A (and hence will do the same on a WD9500-based board). Flicker-free programming does not apply in VGA pass-through mode. Flicker-free mode is enabled by setting Bit 4 of the Western Digital Enhanced Mode Control Register. When sending color data to the board, however, the AI must monitor Bit 4 of the Western Digital Status Register; if set, this bit indicates that a palette write is pending, and no further palette color data should be sent until the WD9500 clears the bit. When clear, the AI can then send three

I/O ADDRESS	READ/WRITE	FUNCTION
O2EA/03C6	R/W	DAC Mask
O2EB/03C7	W	DAC Read Index
O2EB/03C7	R	DAC State
O2EC/03C8	R/W	DAC Write Index
O2ED/03C9	R/W	DAC Data
02E8	R	Display Status
02E8	W	Horizontal Total
06E8	W	Horizontal Displayed
0AE8	W	Horizontal Sync Start
0EE8	W	Horizontal Sync Width
12E8	W	Vertical Total
16E8	W	Vertical Displayed
1AE8	W	Vertical Sync Start
1EE8	W	Vertical Sync Width
22E8	W	Display Control
42E8	W	Subsystem Status
42E8	W	Subsystem Control
46E8	W	ROM Page Select (MC)
4AE8	W	Advanced Function Control
82E8	R/W	Current Y Position
86E8	R/W	Current X Position
8AE8	W	Destination Y Position/Axial Step Constant
8EE8	W	Destination X Position/Diagonal Step Constant
92E8	R/W	Error Term
96E8	W	Major Axis Pixel Count
9AE8	R	Graphics Processor Status
9AE8	W	Command
9EE8	W	Short Stroke Transfer
A2E8	W	Background Color
A6E8	W	Foreground Color
AAE8	W	Write Mask
AEE8	W	Read Mask

TABLE 25. IBM 8514/A COMPATIBLE REGISTERS

bytes, representing the contents of one of the 256 entries in the palette. Other AI accesses of the DAC, including reading color values, are independent of the flicker-free design, and should emulate 8514/A operations.

I/O ADDRESS	READ/WRITE	FUNCTION
B2E8	W	Color Compare
B6E8	W	Background Mix
BAE8	W	Foreground Mix
BEE8		Multifunction Control
BEE8(0)	W	Minor Axis Pixel Count
BEE8(1)	W	Top Scissors
BEE8(2)	W	Left Scissors
BEE8(3)	W	Bottom Scissors
BEE8(4)	W	Right Scissors
BEE8(5)	W	Memory Control
BEE8(8)	W	Fixed Pattern - Low
BEE8(9)	W	Fixed Pattern - High
BEE8(A)	W	Pixel Control

TABLE 25. IBM 8514/A COMPATIBLE REGISTERS (CONT'D)

I/O ADDRESS	READ/WRITE	FUNCTION
28E9	R	Dummy Read/Enable for 96E8
36E8	W	EPROM Select--AT Bus Only
8AE8	W	Ending X Point for Line
8EE8	W	Ending Y Point for Line
96E8	R	Western Digital Status
96E8(1)	W	Western Digital Enhanced Mode
96E8(3)	W	Texture Pattern Start End
96E8(4)	W	Texture Pattern 11-0
96E8(5)	W	Texture Pattern 23-12
96E8(6)	W	Texture Pattern 35-24
96E8(7)	W	Texture Pattern 47-36

TABLE 26. WD9500 ENHANCED REGISTERS

APPENDIX A. VRAM DESIGN - TBD

APPENDIX B. IMPLEMENTATION OF VIDEO DAC - TBD

APPENDIX C. EPROM - TBD

ADS10C00A

Winchester Disk

Controller

WESTERN DIGITAL

ADS10C00A DATA BOOK ADDENDUM

The following Data Book applies to both the ADS10C00 and the ADS10C00A versions.

Part Numbers:

STATUS	MODEL NUMBER	MANF. NUMBER	DESCRIPTION
Current	ADS10C00A JT 00 02	1000KB00JTL02	68-pin PLCC, released 6/90
Obsolete	ADS10C00 JT 00 02	1000PA00JTL02	68-pin PLCC

ADS10C00A Data Book Corrections

The following changes should be made to the existing ADS10C00:

Several pins are incorrectly labeled for the pinout drawing.

PIN#	WAS	CORRECTION
9	GN0	GND
8-1	D00-D07	DB0-DB7
63	WR20	NRZ0
59	R6	RG
58	W6	WG

List of Differences

There are no functional differences between the ADS10C00 and the ADS10C00A. Production process improvements were made to improve reliability.

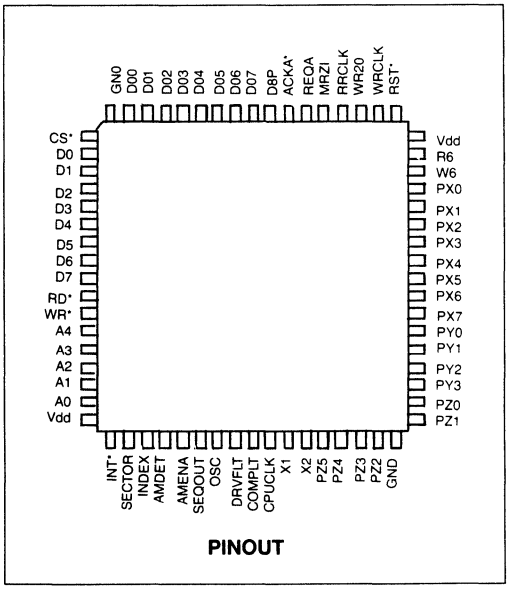
1. Change: Input buffers for the DB bus inputs were improved and signal routing optimized in order to improve DB bus setup and hold times with respect to CS and WR. The new input buffers have modified device sizes and decreased capacitance. These changes allow a greater margin in meeting the specified setup and hold times. No logic or specifications changes were involved.

2. Change: A potential race condition existed between a clock (CLK) and the inversion of that clock (CLKN). Previously both clocks were generated in parallel from a master clock; CLK through a buffer and CLKN through an inverting buffer. This was changed to CLK being generated serially from the CLKN signal by an inverting buffer. A minor routing/logic change was involved, no specification change.

ADS10C00 Winchester Disk Controller

FEATURES

- DISK INTERFACES AND FORMATS SUPPORTED INCLUDE ST412, ST412HP, ESDI, SMD, AND CPTICAL DISKS
- FULL MULTISECTOR OPERATION WITH FOUR BYTE ID AUTO-INCREMENT
- UP TO 24 MBITS/SECOND MAXIMUM TRANSFER RATE
- INTERNAL 48-BIT ECC, 32-BIT ECC, OR 16-BIT CRC-CCITT POLYNOMIAL, OR EXTERNAL USER DEFINED ECC
- INTERNAL SUPPORT FOR 4 TO 18 BIT ERROR CORRECTION SPANS
- UP TO 1:1 INTERLEAVE OPERATION
- FLEXIBLE ERROR RECOVERY, INCLUDING REDUNDANT ID AND SYNC FIELDS
- SECTOR SIZES TO 4096 BYTES, HARD OR SOFT SECTOR, LARGER SIZES POSSIBLE WITH SPECIAL TECHNIQUES
- BUILT IN CRYSTAL DRIVER FOR DATA RATE AND/OR CPU USE



PINOUT

- GENERIC CPU BUS INTERFACE WITH INTERRUPTS
- SEPARATE CPU AND DISK DATA BUSSES
- ASYNCHRONOUS DATA BUFFER INTERFACE WITH FULL 'THROUGH' PARITY
- ON THE FLY COMPARE AGAINST BUFFER DATA
- 20 I/O LINES FOR DISK DRIVE CONTROL
- 68 PIN PLCC PACKAGE

GENERAL DESCRIPTION

The ADS10C00 is a VLSI Winchester Disk Controller chip that provides the data handling and control for an intelligent Winchester disk controller. The ADS10C00 interfaces to nearly any serial disk interface, including ST412, ST412HP, ESDI, SMD, and many optical disk interfaces. The ADS10C00 provides great flexibility in format design, allowing for multiple ID fields, special sync requirements, special information fields, or almost any other special requirement. The ADS10C00 can provide all of the data, status, and control signals required by these interfaces.

The ADS10C00 requires only a buffer controller, such as the ADS60C40 buffer manager, a microprocessor, a data buffer memory, an optional data encoder and decoder, and drivers and receivers to make an intelligent disk controller. The ADS60C80 can be added to provide external Reed-Solomon ECC for optical disk formats.

The ADS10C00 performs all of the disk data serialization and deserialization, formatting, and error detection and correction tasks. The ADS10C00 also has data verify and compare capability, and generates and checks parity. The ADS10C00 can perform full track operations without CPU control through the use of a sector counter and auto-incrementing ID registers.

The ADS10C00 has a generic microprocessor bus interface that allows the ADS10C00 to be used with all popular 8-bit microprocessors. The ADS10C00 has interrupt capability, which means the microprocessor is freed from constant polling of the device. The ADS10C00 also has a built in crystal oscillator driver that can be used to generate data reference, buffer management, or microprocessor clocks. Two separate outputs are provided with internal programmable dividers. Both outputs have the extra drive voltage and current necessary for driving MOS microprocessor clock inputs.

The ADS10C00 has 20 lines dedicated to external I/O control lines that the microprocessor can use for drive and head select, seek command and status, and drive status. Eight lines are output only, six lines are input only, and four other lines can be individually programmed for input or output. Two other latch and hold input lines are tied to the interrupt logic and can be used to detect fault or attention conditions without constant polling.

The ADS10C00 provides error detection and correction support. The device can be programmed to use 16-bit CRC-CCITT, 32-bit ECC, or 48-bit ECC. The internal checksum register can be accessed by the microprocessor to aid in the correction of error bursts up to 18 bits. The ADS10C00 can also be programmed to use an external ECC generator and checker.

The highly programmable nature of the ADS10C00 allows the use of redundant ID and data sync fields within a single sector. This feature, along with the 48-bit ECC, gives the ADS10C00 a greater capability for recovering user data in a sector with 'grown' defects.

PIN DESCRIPTION

The following section describes the external signals available on the ADS10C00. Conventions are as follows:

I	indicates that a signal is an input to the ADS10C00.
O	indicates that a signal is an output from the ADS10C00.
I/O	indicates that a signal is bidirectional.
I,O	indicates that a signal can be input or output.

CPU INTERFACE

Name	Dir	Pin #	Description
A0-A4	I	25-21	CPU ADDRESS BUS. These signals are used to address internal ADS10C00 registers.
CPUCLK	O	36	CPU CLOCK OUTPUT. This is the OSC output (see below) divided by two or three, selected by an internal register. This output has extra drive for use with certain microprocessors.
$\overline{CS}$	I	10	CHIP SELECT. This active low signal enables the ADS10C00 bus interface logic.
D0-D7	I/O	11-18	CPU DATA I/O BUS. Used to transfer ADS10C00 control and status with the CPU.
$\overline{INT}$	O	27	CPU INTERRUPT.This active low, open drain, output is asserted whenever an enabled interrupt condition occurs on the ADS10C00.
OSC	O	33	OSCILLATOR OUTPUT. The 1x crystal oscillator output, optionally divided by two. This signal has the same drive capability as CPUCLK.
$\overline{RD}$	I	19	CPU READ STROBE. This active low signal enables data from the ADS10C00 on to the CPU data bus.
$\overline{RST}$	I	61	RESET. This active low signal resets all internal circuits that must be reset at power on. A complete list is given later in this document. The reset is latched and the condition must be cleared by the CPU.
$\overline{WR}$	I	20	CPU WRITE STROBE. This active low signal strobes data into the selected ADS10C00 register from the CPU data bus.
X1	I	37	CRYSTAL DRIVER INPUT. X1 can also be driven by an external clock.
X2	O	38	CRYSTAL DRIVER OUTPUT.

BUFFER INTERFACE

Name	Dir	Pin #	Description
$\overline{\text{ACKA}}$	I	67	BUFFER DATA ACKNOWLEDGE. This active low signal indicates to the ADS10C00 that data can now be transfered to or from the data buffer.
DB0-7	I/O	8-1	BUFFER MEMORY DATA BUS. This is an eight bit data bus that interfaces the ADS10C00 with the disk data buffer memory.
DBP	I/O	68	DATA BUS PARITY. This signal is used to generate and check parity with the disk data buffer memory.
REQA	O	66	BUFFER DATA REQUEST. This signal is asserted when the ADS10C00 has data to write to the data buffer, or needs data from the data buffer.

DISK DATA INTERFACE

Name	Dir	Pin #	Description
AMDET	I	30	ADDRESS MARK DETECTED. Used only in ST412 type interfaces that use missing clocks or other qualifiers to the sync bytes that mark the start of a field.
AMENA	O	31	ADDRESS MARK ENABLE. Used to write a missing clock sync byte (ST412) or soft sector mark (ESDI, SMD) on the media.
NRZI	I	65	NRZ READ DATA IN. Serial data input from the disk phase-locked loop. This signal is clocked in by the rising edge of RRCLK.
NRZO	O	63	NRZ WRITE DATA OUT. Serial data output. NRZO is valid on the rising edge of WRCLK.
RG	O	59	READ GATE. Active when reading from the disk drive. This signal is turned off for one byte time on an ID search error to reset external data decoders.
RRCLK	I	64	READ/REFERENCE CLOCK. This is the reference clock used to set the data rate for write, and is the recovered clock for read. The switching must be glitch free. NRZI is clocked into the ADS10C00 by the rising edge of this clock.
SEQOUT	O	32	SEQUENCER OUTPUT. This signal is a user definable output bit that is set up in the control byte of the sequencer control store (see below). This signal can be used to control an external ECC generator and checker, and is byte aligned with both read and write data.
WG	O	58	WRITE GATE. Active when writing to the disk drive.
WRCLK	O	62	WRITE CLOCK. This is output during write for drives that require it. NRZO data is valid on the rising edge of this clock.

DISK CONTROL INTERFACE

Name	Dir	Pin #	Description
COMPLT	I	35	COMPLETE. This signal is used to detect function complete conditions, such as seeks or status requests. The signal only generates a CPU interrupt, and does not interfere with a read or write operation.
DRVFLT	I	34	DRIVE FAULT. This signal is used to detect faults from the drive. The signal only generates a CPU interrupt, and does not interfere with a read or write operation.
INDEX	I	29	INDEX. This signal is used to indicate the start of a track. This signal is latched for CPU status and interrupt.
PX0-7	O	57-50	PORT X. This general purpose output port is intended for use as drive select and head select signals.
PY0-3	I,O	49-46	PORT Y. This general purpose port is intended for use as other control outputs or inputs. Each bit is selectable as input or output, but all bits are initialized to input when the ADS10C00 is reset.
PZ0-5	I	45,44, 42-39	PORT Z. This general purpose input port is used to receive drive status signals.
SECTOR	I	28	SECTOR MARK. This signal is used for marking sector start locations on the media. This can either be a hard sector mark, or a soft mark written on the media using AMENA (ESDI or SMD).

DEVICE POWER

Name	Dir	Pin #	Description
V_{dd}	I	26,60	+5 VOLTS DC.
V_{ss}	I	9,43	GROUND.

FUNCTIONAL DESCRIPTION

The ADS10C00 consists of the functional blocks shown in the block diagram, Figure 1. Vdd and Vss are applied to the device through two separate pins each to improve noise immunity. The top and right hand sides of the diagram show CPU interface features, the left hand side shows disk interface features, and the bottom shows buffer interface features. These blocks are discussed in the following paragraphs.

The PORT DECODE block generates the 32 write strobes and 23 read strobes used by the microprocessor to access the various internal control and status ports. These include the interrupt registers, external disk control ports, control store, control store control, configuration, ECC control, and ID registers.

The BUFFER CPU DATA block buffers the transfer of data between the microprocessor and the internal registers. The direction control is qualified by chip select ($\overline{CS}$) and read strobe ($\overline{RD}$).

The CPU CONFIGURATION PORTS are used to reset the ADS10C00, select checksum polynomials, set the address mark enable timing, set the buffer interface timing, and select the frequency of the clock outputs, OSC and CPUCLK.

The OSCILLATORS AND DIVIDERS block generates the clock outputs, OSC and CPUCLK, using an external crystal (or clock input) and dividers to select the frequency. Frequency selection is glitch free.

The INTERRUPT STATUS AND MASK registers are used to check and mask interrupts. The mask register does not affect the status register inputs. The interrupt sources include index and sector mark, drive fault and operation complete, and internal event status.

The EXTERNAL PORTS are used to generate control signals and read status with the disk drive. Eight bits are output, six are input, and four are individually programmable for either input or output.

The CONTROL STORE consists of 32 words of 28 bits that are used to program the format of the disk sector. The data source, field length, error handling and checksum selection, and control signals, like Read Gate and Write Gate, are controlled by the data stored here.

The CONTROL STORE CONTROL determines the next address in the control store to use, whether the next sequential address or a jump to another address. This block includes the sector counter used for multisector commands. This block also includes the BIT RING COUNTER, which determines the timing of data transfers in the ADS10C00.

The WAIT SEQUENCER handles searches for index, sector mark, address mark, and byte synchronization.

The ID WRITE REGISTERS are 8 eight bit registers that are used to set the ID write field for format, or the search field for read/update write. Four of the registers are counters that auto-increment during multisector commands. The other four registers do not increment, and are used for defect and flag information. The first byte of the four counters can be disabled for three byte ID fields.

The ID READ REGISTERS are used to read the last ID read from the media to aid in defect handling.

The CHECKSUM block sets the ECC/CRC polynomial, generates the checksums, and is also used to correct data errors.

The VALUE register holds immediate data from the control store when generating gaps, sync fields, and address mark bytes.

The SHIFT OUT register serializes internal or external (buffer) data for writing on the disk. The output is multiplexed with the output of the checksum register.

The SHIFT IN register deserializes the read data from the disk, clocked in by RRCLK. The data is also transfered to the checksum register for checking.

The COMPARE block is used to compare incoming read data with an internal or external data source. These include byte synchronization detection, ID field search, and buffer data compare.

The BUFFER INTERFACE handles the fetching and writing of data with the external data buffer. This includes parity generation and checking, and data handshake with the buffer controller.

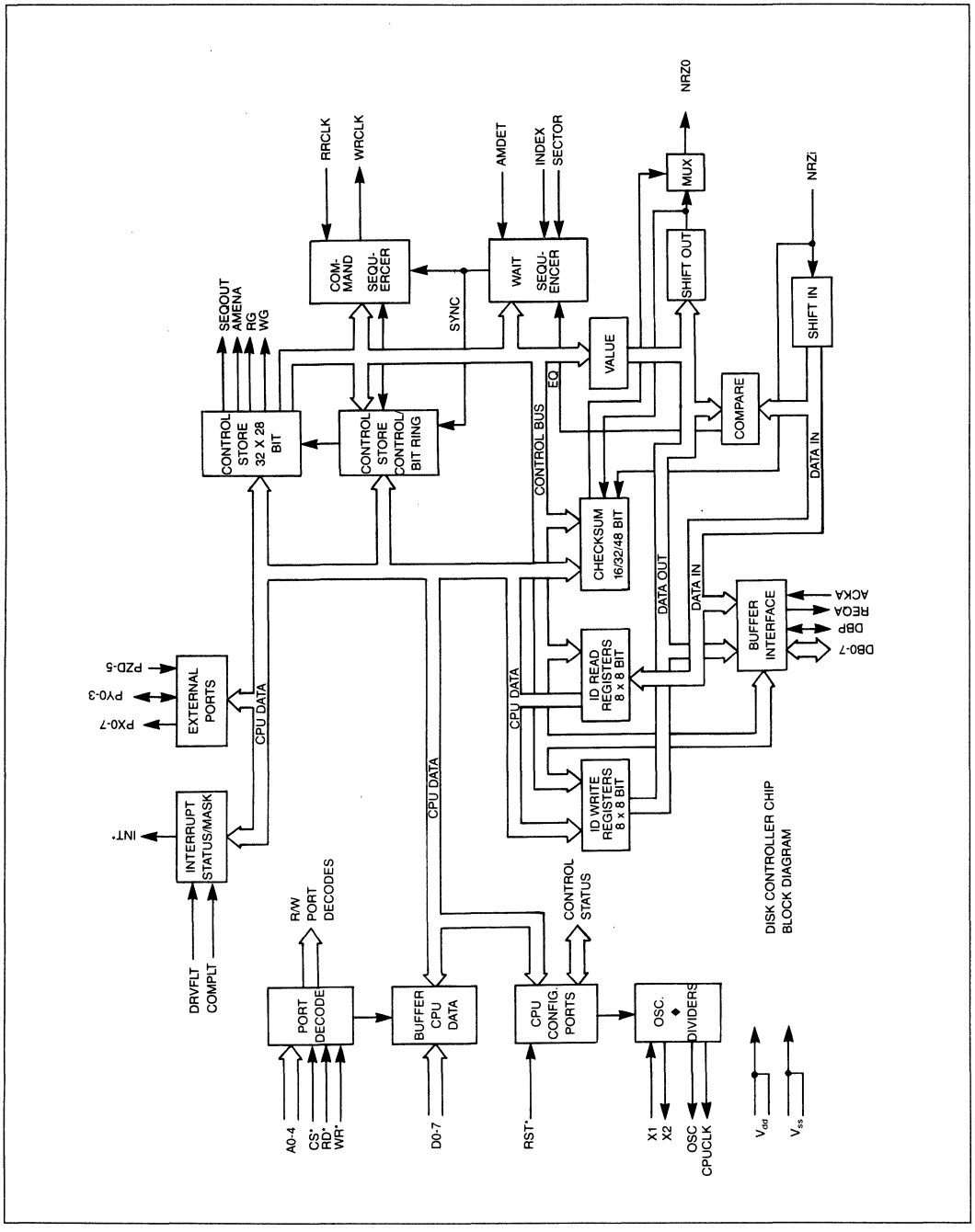


FIGURE 1. ADS10C00 BLOCK DIAGRAM

RESET CONDITIONS

The following list defines what is reset when $\overline{RST}$ is asserted on the ADS10C00, or the CPU sets the internal reset bit (SRST in SRESET register):

- SRST bit in SRESET is left set, and must be cleared by the CPU to take the ADS10C00 out of the reset state
- interrupts are disabled
- PY0-3 are set to input
- DB0-7,P are disabled
- OSC is set to X1/2
- CPUCLK is set to X1/6
- command sequencer stops
- The following CPU registers are reset to zero:
  - PORT X
  - PORT Y CONFIGURATION
  - ECC CONTROL (ECCSHT bit)
  - SECTOR COUNTER
  - INTERRUPT MASK REGISTER
  - SRESET REGISTER (except SRST)
- The following outputs are reset to zero:
  - PX0-7
  - SEQOUT
  - AMENA
  - RG
  - WG
  - NRZO
  - REQA
- The following error status bits are reset to zero:
  - IDERR
  - PTYERR

CRYSTAL OSCILLATOR APPLICATION

For applications that use the internal oscillator capability of the ADS10C00, a series resonant crystal must be used. This crystal must meet the following internal specifications:

C_S = 7 pf MAX

R_S = 30 ohms MAX

The oscillator also requires bypass capacitors, as shown in the following diagram:

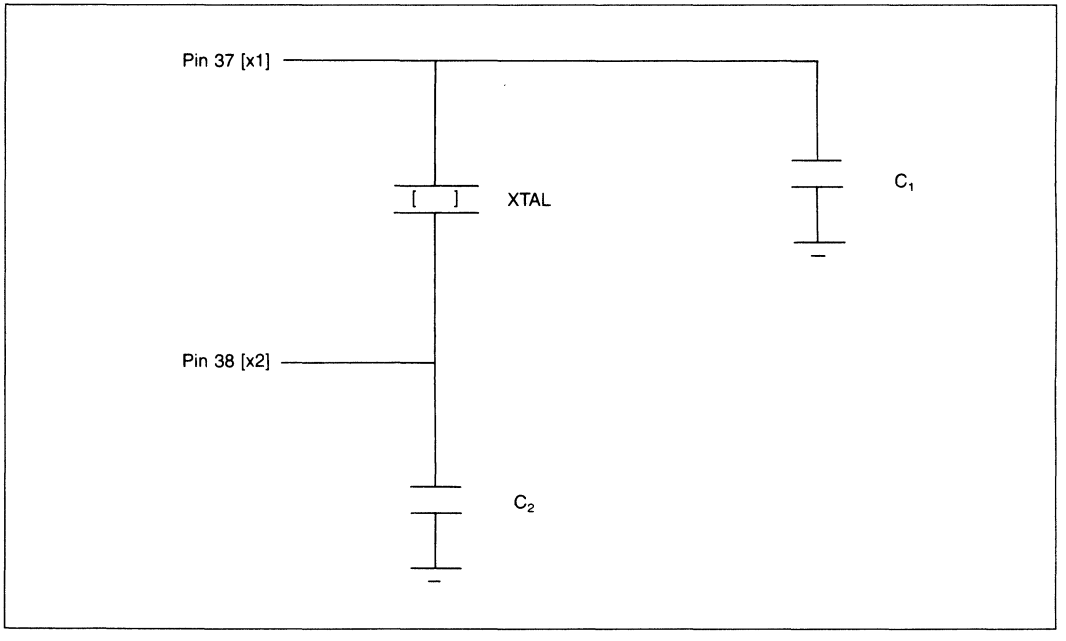


FIGURE 2. OSCILLATOR WITH CAPACITORS

The following table lists values for C_1 and C_2 for several typical crystal frequencies. The capacitor tolerances are +—10%. Values for intermediate frequencies (not listed in the table) may be extrapolated.

FREQ (MHz)	C_1 (pf)	C_2 (pf)
8	180	100
10	180	68
12	150	47
14	120	56
16	82	56
20	82	33
24	56	27
25	56	22
30	39	12
32	33	12

SPECIFICATIONS

NON-OPERATIONAL SPECIFICATIONS (absolute maximums)

	MIN	TYP	MAX	UNITS
Storage Temperature:	−65		150	Degrees C
Voltage on any pin with respect to V_{SS}:	−0.3		V_{DD} + 0.3	Volts
Voltage on V_{dd}, with respect to V_{SS}:			7.0	Volts

OPERATIONAL SPECIFICATIONS

	MIN	TYP	MAX	UNITS
Ambient Air Temperature:	0	25	70	Degrees C
V_{dd} Supply Voltage with respect to V_{SS}:	4.50	5.0	5.50	Volts
I_{CC} Supply Current: (X1 = 32MHz, RRCLK = 27MHz) (Full spec output loading)			100	Milliamps
Power Dissipation:			500	Milliwatts
Leakage Current on all input pins:			+/− 10	Microamps
Latch-Up Current:	+/− 40			Milliamps
Input Voltage			0.8	Volts
Logic 0 (V_{IL})				
Logic 1 (V_{IH})	2.0			Volts
X1 Drive Current (for TTL levels):			600	Microamps
Logic 0 (V_{IL} = 0.8)				
Logic 1 (V_{IH} = 2.0)			−600	Microamps

	MIN	TYP	MAX	UNITS
Output Voltages (all outputs except X2,CPUCLK,OSC,D0-D7) (*1)				
Logic 0 (V_{OL}) (I_{OL} = 2 mA)			0.40	Volts
Logic 1 (V_{OH}) (I_{OH} = −400 uA)	2.8			Volts
Output Voltages (CPUCLK and OSC only) (*1)				
Logic 0 (V_{OL}) (I_{OL} = 4 mA)			0.40	Volts
Logic 1 (V_{OH}) (I_{OH} = −800 uA)	V_{dd}-0.5			Volts
Output Voltages (D0-D7, $\overline{INT}$ Logic 0) (*1)				
Logic 0 (V_{OL}) (D0-D7, $\overline{INT}$) (I_{OL} = 6 mA)			0.40	Volts
Logic 1 (V_{OH}) (D0-D7) 2.8 (I_{OH} = −2.5 mA)				Volts
Input Capacitance (all inputs)			10	Picofarads
Output Capacitance Loading:				
All outputs except D0-D7, BMD0-BMD7, BMP, OSC, and CPUCLK			50	Picofarads
Outputs D0-D7, BMD0-BMD7, and BMP			100	Picofarads
Outputs OSC and CPUCLK			100	Picofarads
Input Static Discharge Protection (*2)			2000	Volts
Operating Humidity	20		95	Percent
X1 Input Operational Frequency:				
Using Crystal	8.0		32.0	MHz
TTL Source	---		25.0	MHz

NOTES:

(*1): Even under worst case AC transient switching conditions, V_{ol} = 0.4V shall not be exceeded on any output pin at any time.

(*2): This applies for both "human body" and "charged device" models.

TIMING SPECIFICATIONS

These timing relationships assume the maximum capacitive loading for both inputs and outputs, V_{DD} = 4.50 volts to 5.50 volts. Temp = 0 to 70 deg. C. All timing is measured between 0.8 volts logic low and 2.0 volts logic high, unless otherwise noted.

OSC AND CPUCLK TIMING

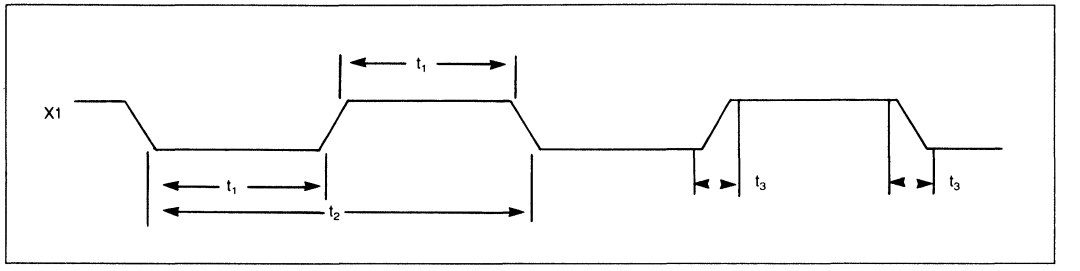


FIGURE 3. TTL SOURCE X1 CLOCK INPUT

The following table summarizes the relationship between the clock at X1 and the resultant outputs at OSC and CPUCLK. OSCDIV and CPUDIV are control bits in the RESET register that determine how the X1 clock is divided to produce OSC and CPUCLK. See the programming manual for more information.

OSCDIV	CLKDIV	OSC	CPUCLK
0	0	X1/2	X1/6
0	1	X1/2	X1/4
1	0	X1/1	X1/3
1	1	X1/1	X1/2

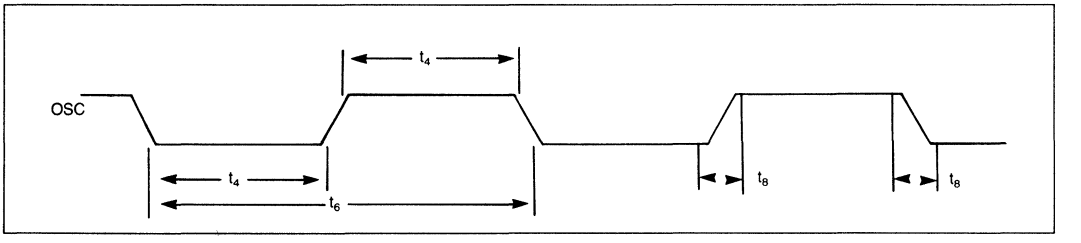


FIGURE 4. OSC OUTPUT

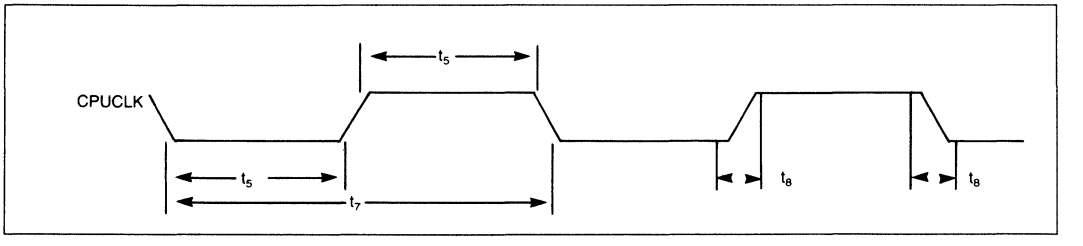


FIGURE 5. CPUCLK OUTPUT

CPU INTERFACE TIMING

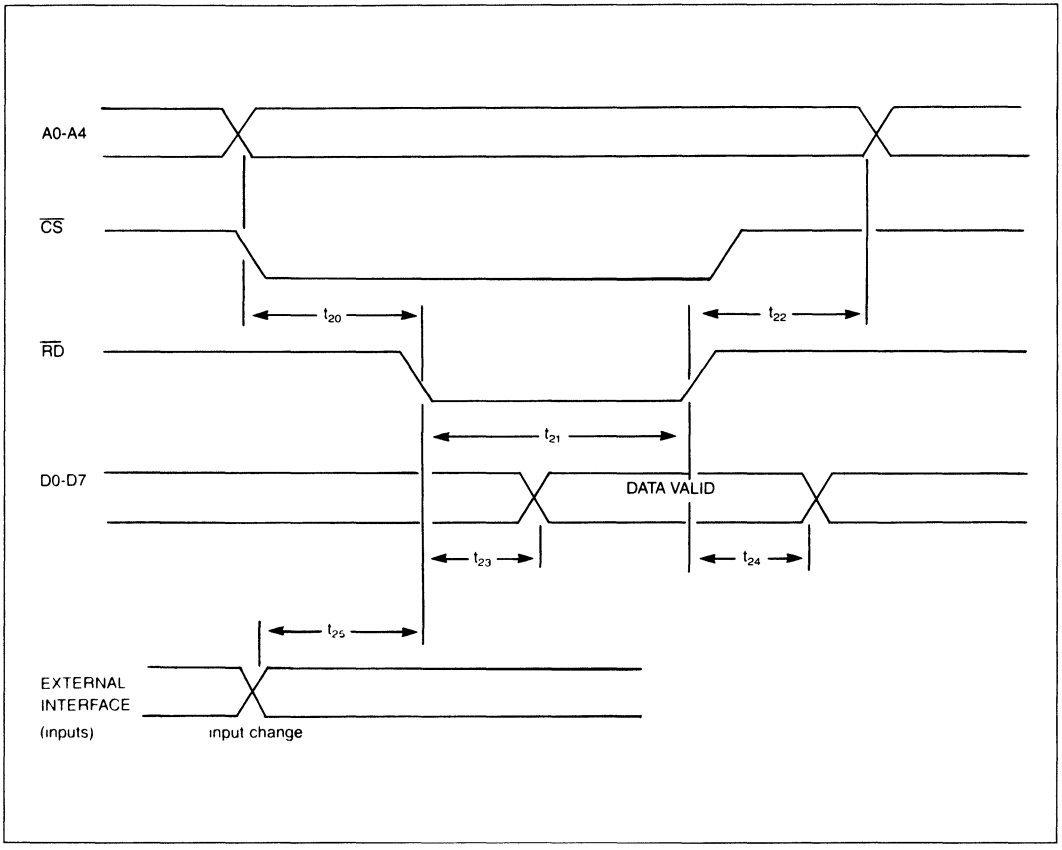


FIGURE 6. MICROPROCESSOR RD TIMING (RD CONTROLLED)

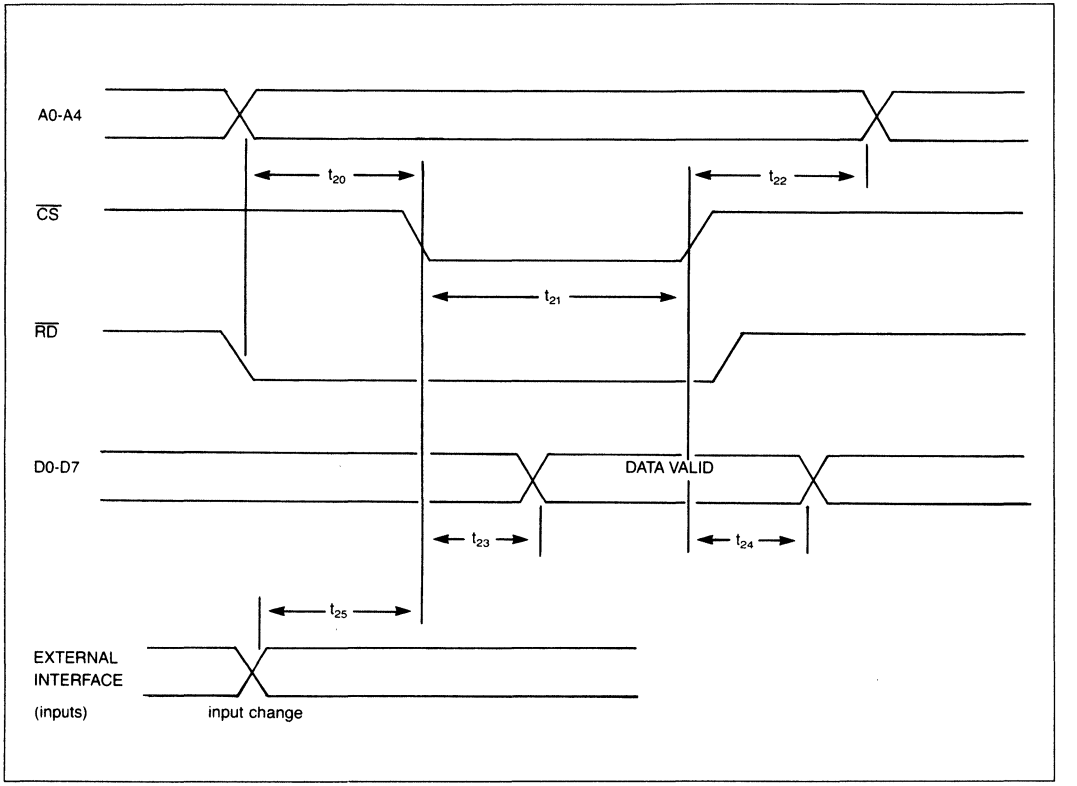


FIGURE 7. MICROPROCESSOR $\overline{RD}$ TIMING ($\overline{CS}$ CONTROLLED)

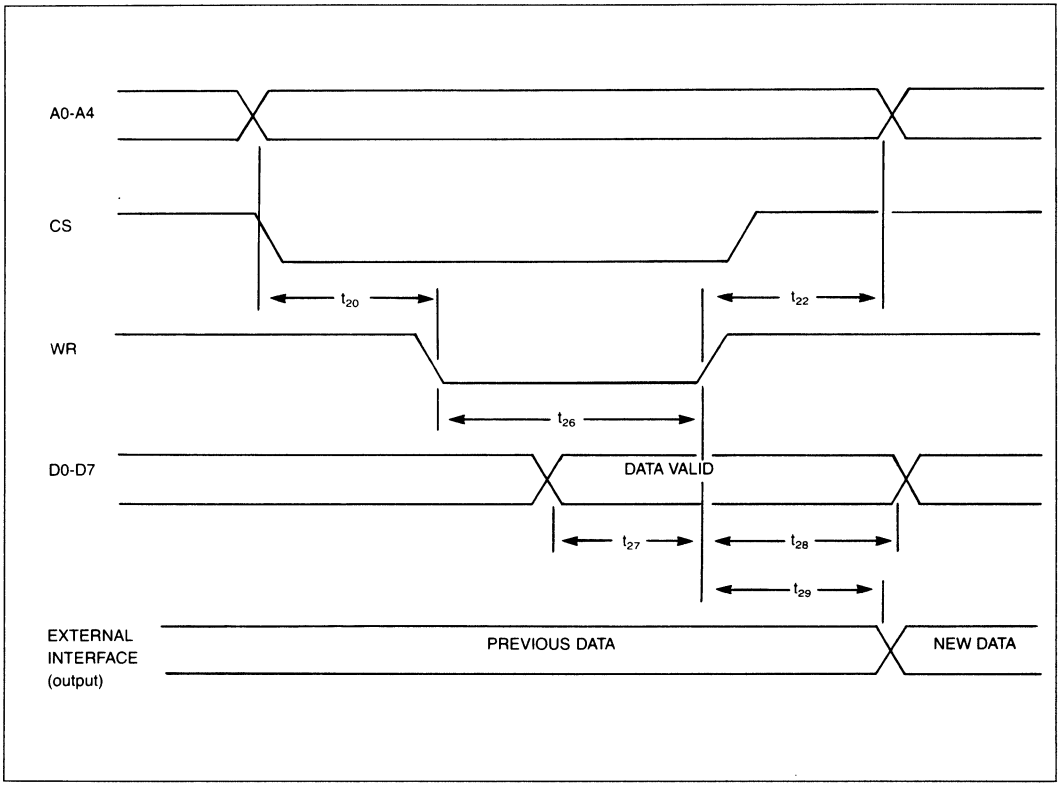


FIGURE 8. MICROPROCESSOR $\overline{WR}$ TIMING ($\overline{WR}$ CONTROLLED)

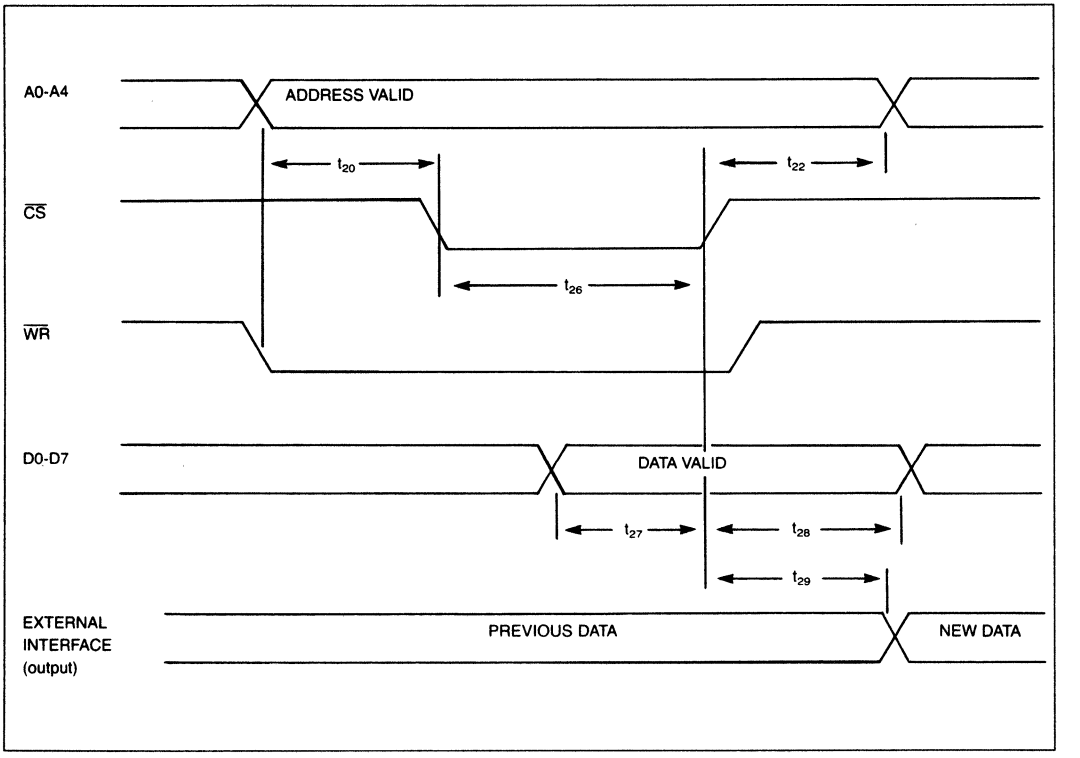


FIGURE 9. MICROPROCESSOR $\overline{WR}$ TIMING ($\overline{CS}$ CONTROLLED)

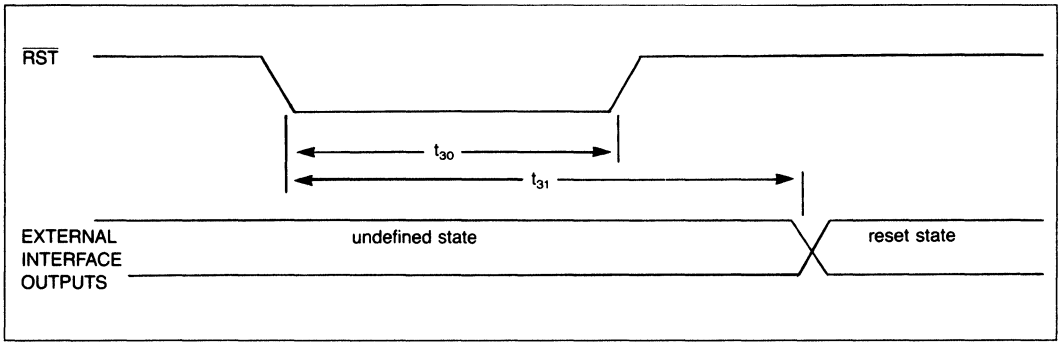


FIGURE 10. RESET TIMING

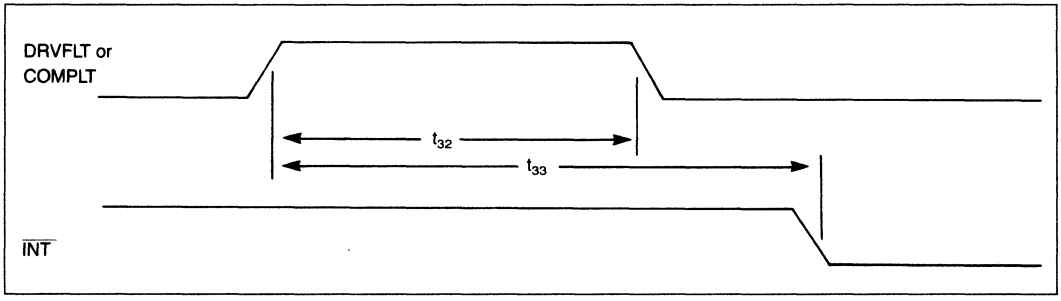


FIGURE 11. EXTERNALLY GENERATED INTERRUPT TIMING

BUFFER INTERFACE TIMING

(Data is coming out of the ADS10C00)
REQTIM = 1 in RESET register. (REQA true when internal data register is full.)

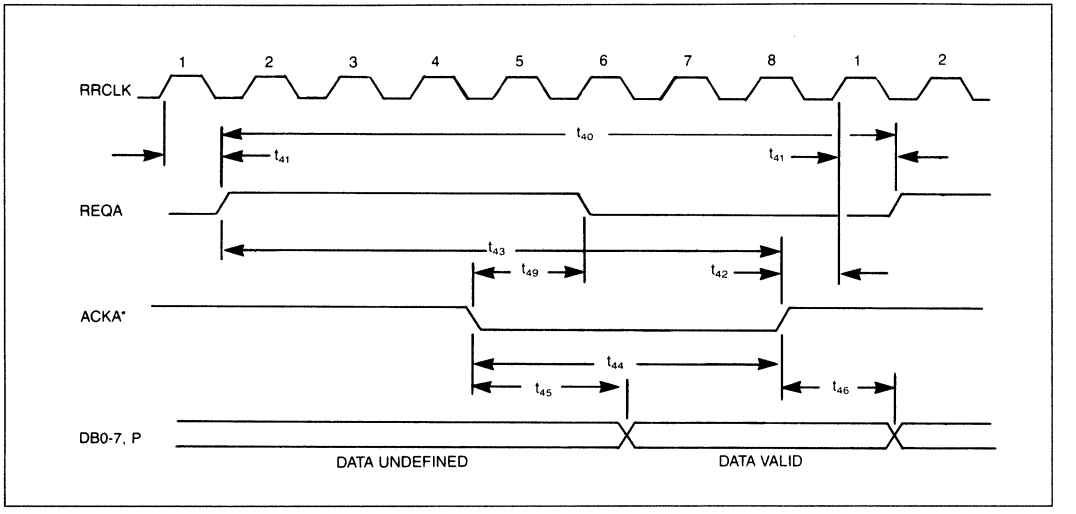


FIGURE 12. ASYNCHRONOUS MODE DATA BUS READ TIMING

REQTIM = 0 in RESET register. (REQA true one bit time before internal data register is full. Note that the cycles overlap by one bit time.)

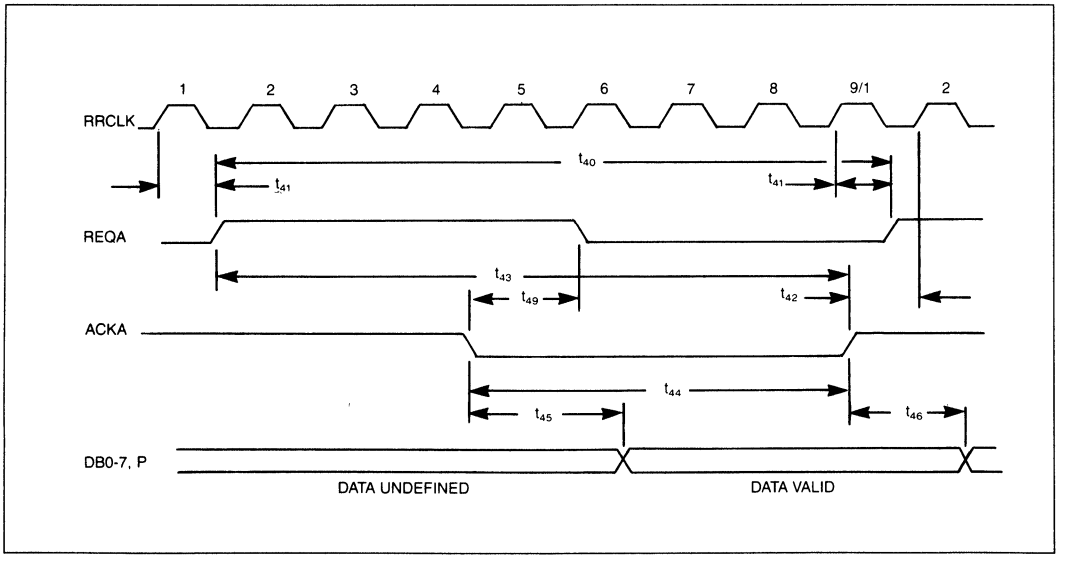


FIGURE 12A. ASYNCHRONOUS MODE DATA BUS READ TIMING

(Data is going into the ADS10C00)
REQTIM = 0 in RESET register. (REQA true when internal data register is empty.)

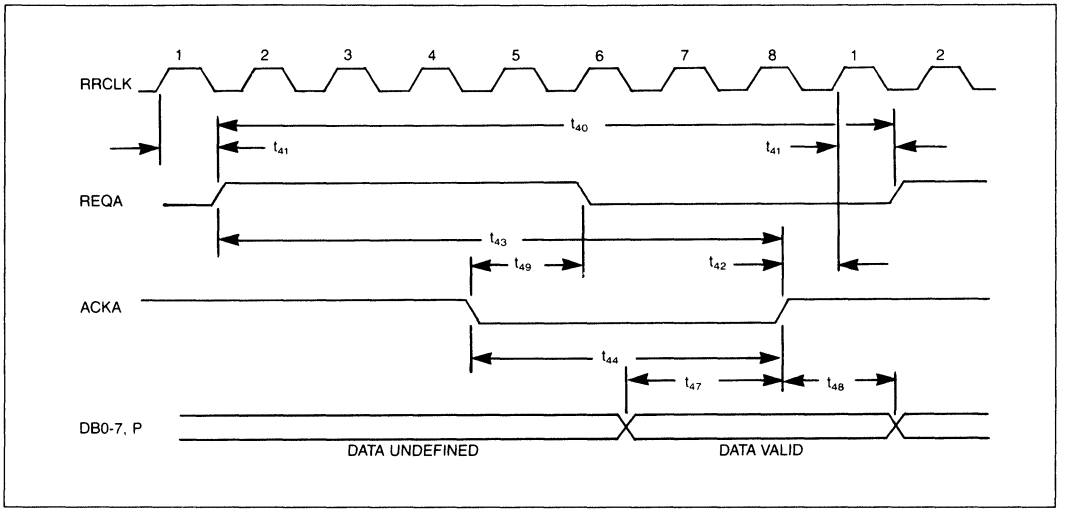


FIGURE 13. ASYNCHRONOUS MODE DATA BUS WRITE TIMING

REQTIM = 0 in RESET register. (REQA true one bit time before internal data register is empty. Note that the cycles overlap by one bit time.)

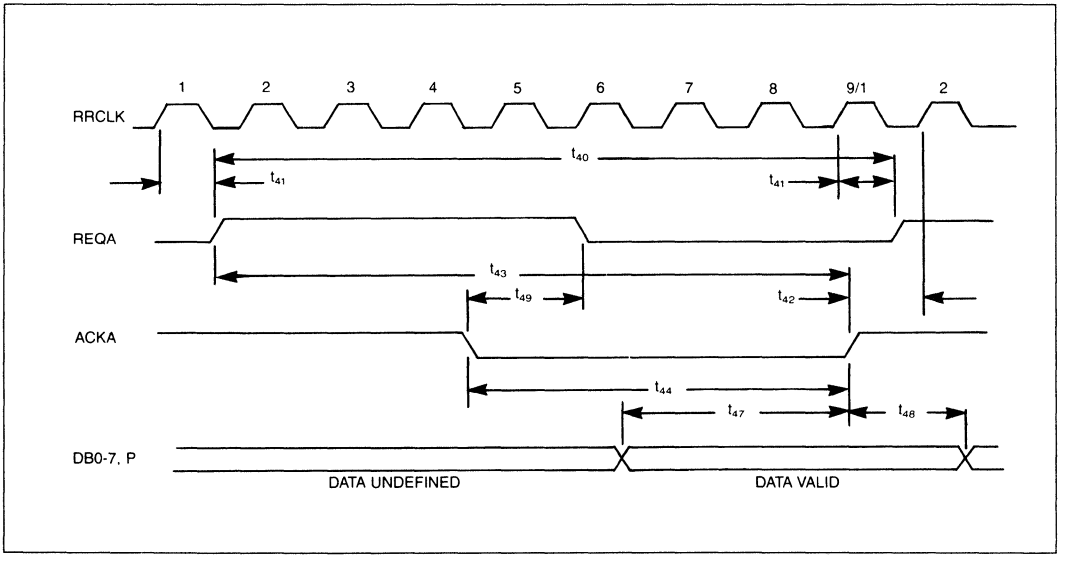


FIGURE 13A. ASYNCHRONOUS MODE DATA BUS WRITE TIMING

SERIAL DATA TIMING

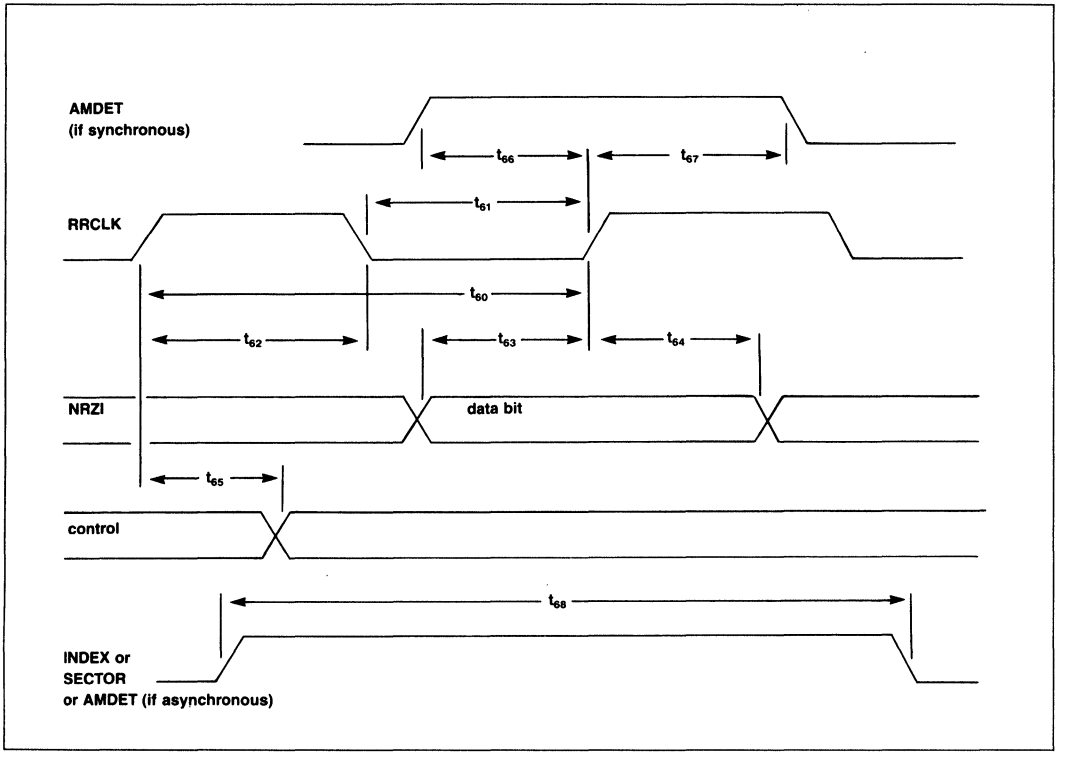


FIGURE 14. NRZ DATA INPUT TIMING

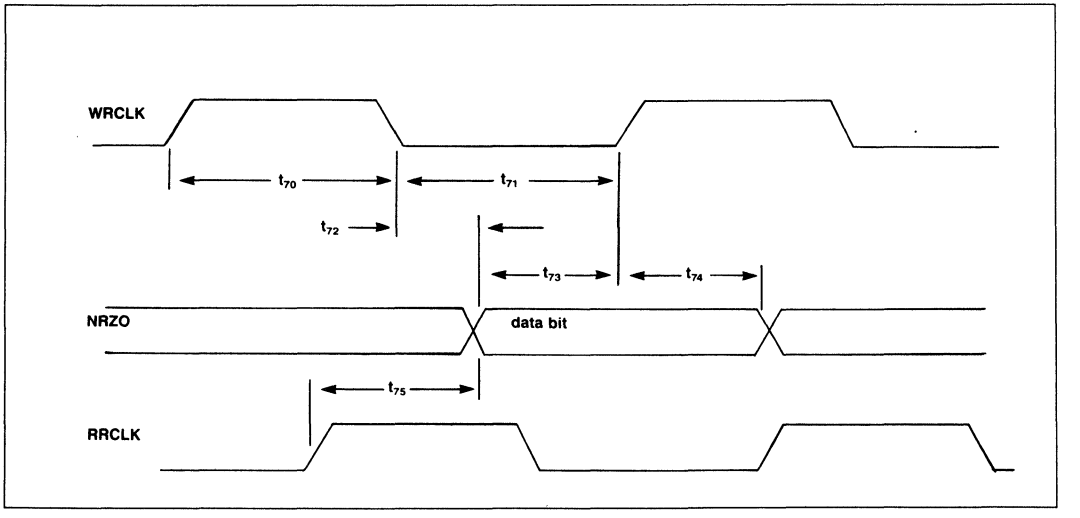


FIGURE 15. NRZ DATA OUTPUT TIMING

AC CHARACTERISTICS

CPUCLK AND OSC TIMING

Timing Parameter	Description	Min	Max	Units
t_1	TTL source X1 high or low (*1)	13		ns
t_2	TTL source X1 cycle time	40		ns
t_3	TTL source X1 rise or fall time (*1)		5	ns
t_4	OSC high or low when: (*2)			
	X1/1 crystal (*3)	10	---	ns
	X1/2 crystal (*3)	27	33	ns
	X1/1 TTL source (*5)	16	24	ns
	X1/2 TTL source (*4)	36	44	ns
t_5	CPUCLK high or low when: (*2)			
	X1/2 crystal (*3)	27	33	ns
	X1/3 crystal (*3)	36	54	ns
	X1/4 crystal (*3)	54	66	ns
	X1/6 crystal (*3)	81	99	ns
	X1/2 TTL source (*4)	36	44	ns
	X1/3 TTL source (*5)	48	72	ns
	X1/4 TTL source (*4)	72	88	ns
	X1/6 TTL source (*4)	108	132	ns
t_6	OSC cycle time when:			
	X1/1 crystal (*3)	30	125	ns
	X1/2 crystal (*3)	60	250	ns
	X1/1 TTL source (*4)	40	---	ns
	X1/2 TTL source (*4)	80	---	ns
t_7	CPUCLK cycle time when:			
	X1/2 crystal (*3)	60	250	ns
	X1/3 crystal (*3)	90	375	ns
	X1/4 crystal (*3)	120	500	ns
	X1/6 crystal (*3)	180	750	ns
	X1/2 TTL source (*4)	80	---	ns
	X1/3 TTL source (*4)	120	---	ns
	X1/4 TTL source (*4)	160	---	ns
	X1/6 TTL source (*4)	240	---	ns
t_8	CPUCLK and OSC rise or fall time (*2)		5	ns

NOTES:

(*1): Times are measured relative to V_{IH} and V_{IL}.

(*2): High and low times are measured relative to the midpoints between V_{OL} and V_{OH}. Rise and fall times are measured bewteen V_{OH} and V_{OL}.

(*3): Assumes 33.3 MHz crystal across X1 and X2 for min times, 8.0 MHz crystal for max times.

(*4): Assumes 25.0 MHz TTL source to X1.

(*5): Assumes 25.0 MHz TTL source to X1, 50/50 duty cycle.

CPU INTERFACE TIMING

NOTE: $\overline{RE}$ = $\overline{RD}$ or $\overline{CS}$. $\overline{WE}$ = $\overline{WR}$ or $\overline{CS}$.

Timing Parameter	Description	Min	Max	Units
t_{20}	address valid to $\overline{RE}$ or $\overline{WE}$	20		ns
t_{21}	$\overline{RE}$ pulse width	100		ns
t_{22}	$\overline{RE}$ or $\overline{WE}$ to address change	0		ns
t_{23}	$\overline{RE}$ true to data valid		95	ns
t_{24}	$\overline{RE}$ false to data hold	20	60	ns
t_{25}	input port setup to $\overline{RE}$ true (*1)	80		ns
t_{26}	$\overline{WE}$ pulse width	100		ns
t_{27}	data setup to $\overline{WE}$ false	80		ns
t_{28}	$\overline{WE}$ false to data hold	0		ns
t_{29}	$\overline{WE}$ false to output change (*2)		80	ns
t_{30}	$\overline{RST}$ pulse width	100		ns
t_{31}	$\overline{RST}$ true to stable outputs		150	ns
t_{32}	DRVFLT or COMPLT pulse width	100		ns
t_{33}	DRVFLT or COMPLT high to $\overline{INT}$ low		150	ns

NOTES:

(*1): Inputs are: PZ0-5, PY0-3 when defined as inputs, and AMDET when being used as a simple input pin.

(*2): Outputs are: PX0-7, and PY0-3 when defined as outputs.

BUFFER INTERFACE TIMING

Timing Parameter	Description	Min	Max	Units
t_{40}	DMA (REQA) cycle time (*1)		$8*t_{cyc}$	
t_{41}	RRCLK true to REQA true		40	ns
t_{42}	$\overline{ACKA}$ false to RRCLK true	20		ns
t_{43}	REQA true to $\overline{ACKA}$ false: (*1) REQTIM = 0 REQTIM = 1			 $8*t_{cyc}-t_{41}-t_{42}$ $9*t_{cyc}-t_{41}-t_{42}$
t_{44}	$\overline{ACKA}$ active low	100		ns
t_{45}	$\overline{ACKA}$ true to data valid		60	ns
t_{46}	$\overline{ACKA}$ false to data hold	10	60	ns
t_{47}	data setup to $\overline{ACKA}$ false	30		ns
t_{48}	$\overline{ACKA}$ false to data hold	5		ns
t_{49}	$\overline{ACKA}$ true to REQA false		35	ns

NOTES:
(*1): t_{cyc} is the RRCLK cycle time used.

SERIAL DATA TIMING

Timing Parameter	Description	Min	Max	Units
t_{60}	RRCLK cycle time	37		ns
t_{61}	RRCLK low (*1)	14		ns
t_{62}	RRCLK high (*1)	14		ns
t_{63}	NRZI setup to RRCLK high	10		ns
t_{64}	RRCLK high to NRZI hold	10		ns
t_{65}	RRCLK high to new control out (*3)		30	ns
t_{66}	AMDET setup to RRCLK high (*4)	10		ns
t_{67}	RRCLK high to AMDET hold (*4)	10		ns
t_{68}	asynchronous input width (*2) (*5)	$2*t_{cyc}$		ns
t_{70}	WRCLK high (*2) (*6)	t_{rlo}–6.0		ns
t_{71}	WRCLK low (*2) (*6)	t_{rhi}–6.0		ns
t_{72}	WRCLK low to NRZO change (*6)	–3.5	3.5	ns
t_{73}	NRZO setup to WRCLK high (*6)	t_{rhi}-9.5		ns
t_{74}	WRCLK high to NRZO hold (*6)	t_{rlo}-9.5		ns
t_{75}	RRCLK high to NRZO change		30	ns

NOTES:

(*1): High and low times measured relative to V_{IH} and V_{IL}.

(*2): t_{rlo} and t_{rhi} are the clock low and clock high (respectively) for the RRCLK input used. t_{cyc} is RRCLK cycle time used.

(*3): Control outputs are: SEQOUT, WG, RG, and AMENA.

(*4): When AMDET is supplied from a synchronous source.

(*5): Asynchronous inputs are: INDEX, SECTOR, and AMDET when it is supplied from an asynchronous source.

(*6): Where the RRCLK input is driven from 0.4V (V_{IL}) to 2.4V (V_{IH}).

PIN/SIGNAL SUMMARY

PIN	SIGNAL	I/O	FUNCTION	PIN	SIGNAL	I/O	FUNCTION
1	DB7	I/O	BUFFER	35	COMPLT	I	DISK CONTROL
2	DB6	I/O	BUFFER	36	CPUCLK	O	CPU INTERFACE
3	DB5	I/O	BUFFER	37	X1	I	CPU INTERFACE
4	DB4	I/O	BUFFER	38	X2	O	CPU INTERFACE
5	DB3	I/O	BUFFER	39	PZ5	I	DISK CONTROL
6	DB2	I/O	BUFFER	40	PZ4	I	DISK CONTROL
7	DB1	I/O	BUFFER	41	PZ3	I	DISK CONTROL
8	DB0	I/O	BUFFER	42	PZ2	I	DISK CONTROL
9	V_{SS}	I	GROUND	43	V_{SS}	I	GROUND
10	$\overline{CS}$	I	CPU INTERFACE	44	PZ1	I	DISK CONTROL
11	D0	I/O	CPU INTERFACE	45	PZ0	I	DISK CONTROL
12	D1	I/O	CPU INTERFACE	46	PY3	I,O	DISK CONTROL
13	D2	I/O	CPU INTERFACE	47	PY2	I,O	DISK CONTROL
14	D3	I/O	CPU INTERFACE	48	PY1	I,O	DISK CONTROL
15	D4	I/O	CPU INTERFACE	49	PY0	I,O	DISK CONTROL
16	D5	I/O	CPU INTERFACE	50	PX7	O	DISK CONTROL
17	D6	I/O	CPU INTERFACE	51	PX6	O	DISK CONTROL
18	D7	I/O	CPU INTERFACE	52	PX5	O	DISK CONTROL
19	$\overline{RD}$	I	CPU INTERFACE	53	PX4	O	DISK CONTROL
20	$\overline{WR}$	I	CPU INTERFACE	54	PX3	O	DISK CONTROL
21	A4	I	CPU INTERFACE	55	PX2	O	DISK CONTROL
22	A3	I	CPU INTERFACE	56	PX1	O	DISK CONTROL
23	A2	I	CPU INTERFACE	57	PX0	O	DISK CONTROL
24	A1	I	CPU INTERFACE	58	WG	O	DISK DATA
25	A0	I	CPU INTERFACE	59	RG	O	DISK DATA
26	V_{dd}	I	+5 VOLTS	60	V_{dd}	I	+5 VOLTS
27	$\overline{INT}$	O	CPU INTERFACE	61	$\overline{RST}$	I	CPU INTERFACE
28	SECTOR	I	DISK CONTROL	62	WRCLK	O	DISK DATA
29	INDEX	I	DISK CONTROL	63	NRZO	O	DISK DATA
30	AMDET	I	DISK DATA	64	RRCLK	I	DISK DATA
31	AMENA	O	DISK DATA	65	NRZI	I	DISK DATA
32	SEQOUT	O	DISK DATA	66	$\overline{REQA}$	O	BUFFER
33	OSC	O	CPU INTERFACE	67	$\overline{ACKA}$	I	BUFFER
34	DRVFLT	I	DISK CONTROL	68	DBP	I/O	BUFFER

ADS10C00 PROGRAMMERS BENCH REFERENCE (PBR)

Addr	Name	Dir	Size	Addr	Name	Dir	Size
00	SRESET	W	7–0	10	ECC0	W	7–0
01	SISR	R/W	7–0	11	ECC1	W	7–0
02	SIMR	R/W	7–0	12	ECC2	W	7–0
03	SEQSTS/PYC	R/W	7–0/3–0	13	ECC3	W	7–0
04	CSERR	R/W	3–0	14	ECC4	W	7–0
05	CSCTL	R/W	7–0	15	ECC5	W	7–0
06	CSVAL	R/W	7–2;7–0	16	do not use — test only		
07	CSCNT	R/W	7–4,0;7–0	17	SKIP	W	4–0
08	PORTX	R/W	7–0	18	ID0	R/W	7–0
09	PORTY	R/W	3–0	19	ID1	R/W	7–0
0A	PORTZ/AMC	R/W	5–0/7–0	1A	ID2	R/W	7–0
0B	SEQCTL	R/W	5–0	1B	ID3	R/W	7–0
0C	START	R/W	4–0	1C	ID4	R/W	7–0
0D	ECCZ/LOOP	R/W	7–0/4–0	1D	ID5	R/W	7–0
0E	ECCCTL	R/W	7–0	1E	ID6	R/W	7–0
0F	SECCNT	R/W	7–0	1F	ID7	R/W	7–0

TRUE = 1 FOR ALL BITS

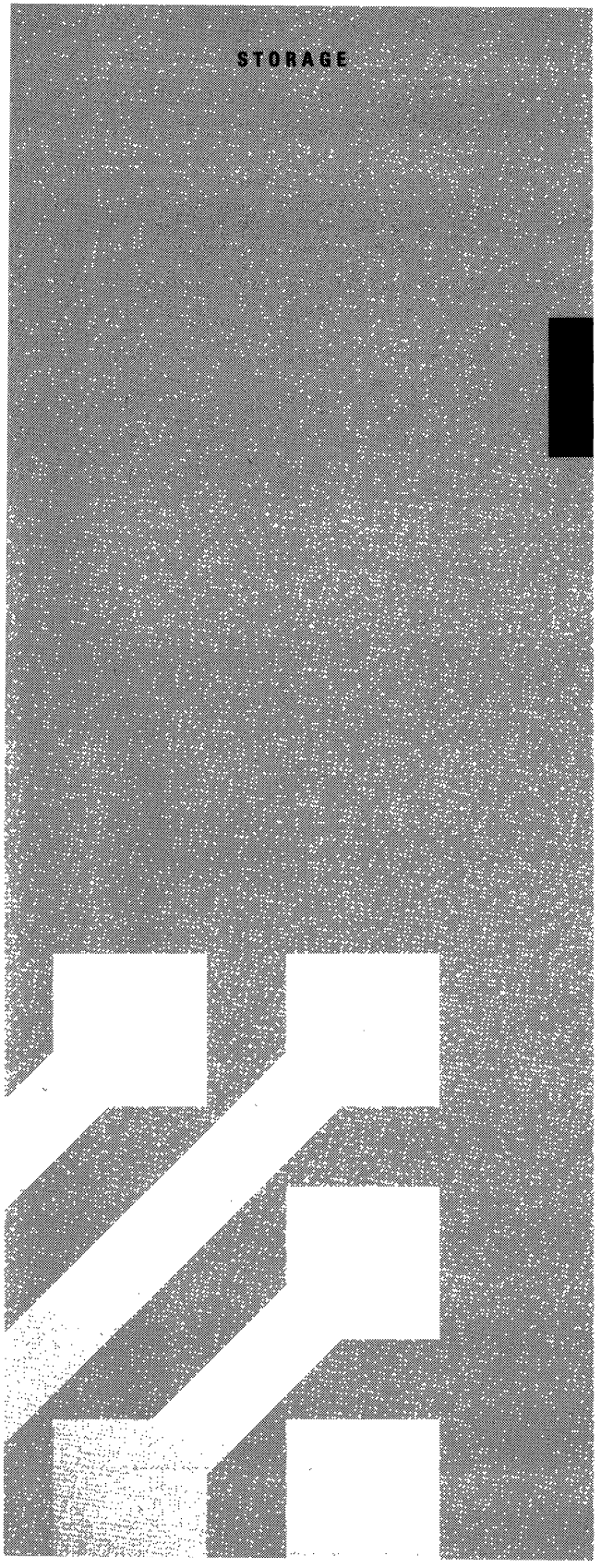
SRESET (00)		SISR (01) AND SIMR (02)	
bit	**output**	**bit**	**input/output**
7	CLKDIV	7	GINT
6	OSCDIV	6	IDFULL
5	IDCHK	5	DXFER
4	DCHK	4	COMPLT
3	ECCSIZ	3	SEQSTP
2	REQTIM	2	SECEND
1	ID3$4	1	SM$IX
0	SRST	0	FAULT
SEQSTS (03)		**PYC (03)**	
bit	**input**	**bit**	**output**
7	DATFLD	7	
6	ECCEN	6	
5	LAST	5	
4	ID	4	
3	CHK	3	PY3OUT
2	WAIT	2	PY2OUT
1	AMDET	1	PY1OUT
0	SEQOUT	0	PY0OUT
CSERR (04)		**CSCTL (05)**	
bit	**input/output**	**bit**	**input/output**
7		7	SVSEL
6		6	CWSEL
5		5	WG
4		4	RG
3	FAIL	3	AM
2	RTY	2	CMPEN
1	DAC	1	SKPEN
0	SEQOUT	0	JMPEN
CSVAL (06)		**CSCNT (07)**	
bit	**input/output**	**bit**	**input/output**
7	BUFF	7	WDAM (COUNT)
6	NOXFER	6	WIAM
5	LAST	5	WIX
4	ID	4	WSM
3	CHK	3	
2		2	
1		1	
0		0	STOP

SEQCTL (0B)			ECCCTL (0E)		
bit	**input**	**output**	**bit**	**input**	**output**
7		RGERLY	7	ECCOUT	ECCINL
6			6	COR04B	ECCSHT
5	ECCERR		5	COR05B	ECCCLR
4	IDERR		4	COR06B	ECCSET
3	PTYERR	IXMASK	3	COR07B	ECCNIT
2	SYNCER	SMMASK	2	COR08B	DISCHK
1	CMPERR	RCMP	1	COR09B	DISPTY
0		KILL	0	COR10B	ECCINM
ECCZ (0D)					
bit	**input**	**output**			
7	COR11B				
6	COR12B				
5	COR13B				
4	COR14B				
3	COR15B				
2	COR16B				
1	COR17B				
0	COR18B				

WD10C23

Self-Adjusting

Data Separator



WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

The WD10C23 Read/Write Channel is an LSI device implemented in 1.25 micron high-speed CMOS. It is specifically designed to be compatible with the Western Digital WD53C22/ 42C22/ WD50C12 series of Hard Disk Controllers, and with disk drives conforming to the popular ST506/412 interface standard and recent speed-enhanced versions. In addition it will support optical applications when used with the WD60C31A ENDEC.

1.1 Features

- 5-15Mbit/sec data rates with no component changes
- Fixed/variable frequency control for zone bit recording
- Pin selectible hard/soft sector support and 2,7 RLL coding
- Precision internal self-adjusting VCO
  - —compensates for component, temperature, voltage, and aging variations
  - —one sigma phase jitter to within 250 psec at 15 Mbit/sec
- Dual gain charge pump
  - —high gain for faster frequency acquisition
  - —low gain for greater jitter rejection
  - —charge pump balance to within ± 5%
- Dual mode phase frequency detector
  - —phase frequency detection for velocity lock on XTALIN reference and on the data synchronization field , thus eliminating quadrature and harmonic locks
  - —phase only detection (phase lock) while tracking data
  - —phase window centering is precisely controlled to within ±1 nsec
- Frequency independent data detection window optimization
  - —window centering is precisely controlled to within ±1 nsec
  - —window loss controlled to within 1 nsec
  - —"built in" PMA with window shifting from 0 to 100% at ±1 nsec accuracy
  - —adaptive window centering for correction for channel antisymmetry
- Crystal controlled processing of the write data

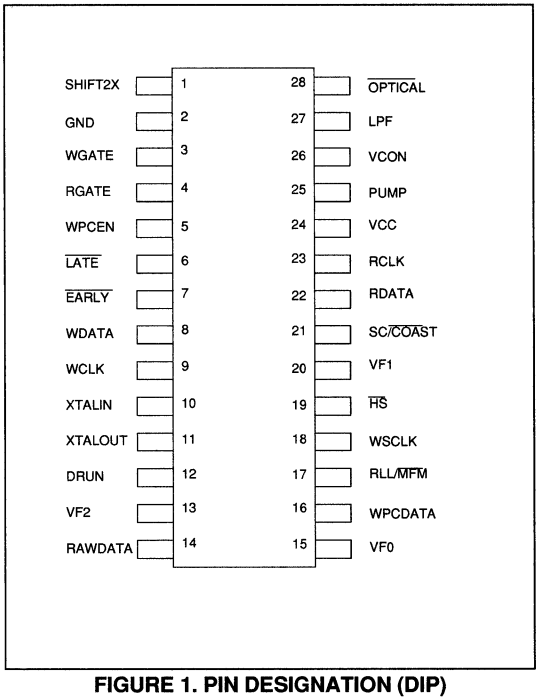


FIGURE 1. PIN DESIGNATION (DIP)

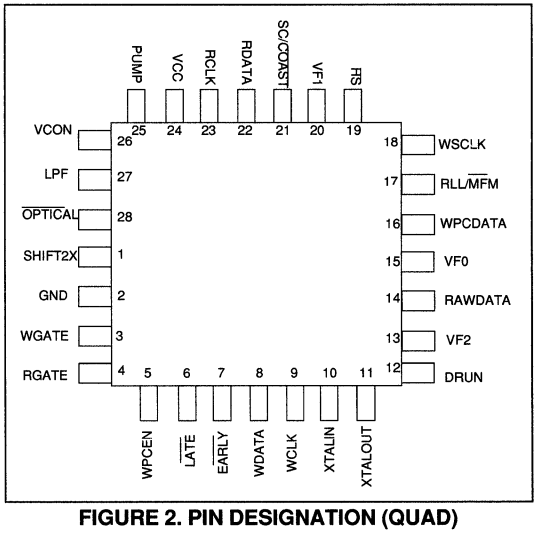


FIGURE 2. PIN DESIGNATION (QUAD)

- Dual level precompensation of ±6.25% and/or ±12.5% of the window, accurate to within ±1 nsec

2.0 DESCRIPTION

The WD10C23 uses a single 5 volt supply and has been designed for 5Mbit/sec MFM encoding, or 5 to 15 Mbit/sec data rates using RLL encoding. Variable frequency applications, or various fixed frequency applications may be accommodated through selection of the VF control bus.

One of the key features of the WD10C23 is the group of internal delay lines, that are automatically set by the XTALIN frequency. These precision elements allow for a high degree of accuracy in the handling of write precompensation, window centering, and window shifting. Further developments in this technology enable the unique implementation of Adaptive Window Shifting/Centering (AWS).

In a typical application, the WD10C23 performs all of the handling of the sensitive read/write signals between a disk controller and data drivers and receivers. Read data corresponds to previous write data, with added phase, frequency, and write splice noise. The fundamental purpose of the WD10C23 is to remove these sources of noise, and present a clean digital signal to the controller.

2.1 Zone Bit Recording

The WD10C23 was designed for use in zone bit recording schemes. In these applications, the data rate is varied to create a fixed bit density (flux transitions/inch or FCI) from the outer radius of the media.

To maintain optimum performance as the data rate changes, loop parameters (i.e., gain, bandwidth, etc.) must be modified. This is accomplished through selection of appropriate frequency bands. The WD10C23 accommodates five different bands.

COMP:	5 Mbit/sec MFM and 7.5 Mbit/sec RLL
BAND0:	RLL, variable frequencies ranging from 5 to 7.5 Mbit/sec
BAND1:	RLL, variable frequencies ranging from 7.5 to 10.6 Mbit/sec
BAND2:	RLL, variable frequencies ranging from 10.6 to 15 Mbit/sec
BAND3:	RLL, 15 Mbit/sec

BAND0-3 may be programmed for zone bit recording, or strapped for fixed frequency applications. In these four bands, LPF must be connected to the external filter, and an external resistor placed across PUMP and VCON.

The COMP band allows for backwards compatibility with previous Western Digital data separators through component de-population.

See Table 1 for information to help you select a frequency band that is appropriate for your application.

The Table 1 columns, K_o and K_d, when unbroken, represent regions across which the gains are montonic. Across these boundaries, defined by a change in the state of the VFO/VF1 controls, the gains are re-centered to optimize for the respective frequency bands.

Recording Mode Select	VF1	VF0	RLL	Frequency Band (Data Rate MHz)	Band Name	VCO Gain Ko	Charge Pump Gain ** K_d	Open Loop Gain K_{ol}	Filter Resistors* Pump-VCON LPF†			
									INT‡	EXT	INT	EXT
Fixed Frequency	z	z	0	f=5.0	Comp	K_{om}	Kd2	K_{olm}	3kΩ	∞	∞	∞
			1	f=7.5								
Fixed or Variable Frequency Formats	0	0	1	5.0 ≤ f<7.5	Band0	K_{or} K_{o0} K_{o1}		K_{olr} K_{ol0} K_{ol1}	∞	3kΩ		
	0	1		7.5≤ f≤10.6	Band1						2.8kΩ	
	1	1		10.6< f <15.0	Band2	K_{o2}		K_{ol2}	6kΩ		525Ω	307Ω
	1	0		f=15.0	Band3	K_{o3}	Kd3	K_{ol3}	3.5kΩ		150Ω	

TABLE 1. FREQUENCY BAND SELECTION

*The following information is not intended to represent device specifications, but is indicative of typical values. See the PLL section for actual specifications.

**Charge Pump Gain, and thus, Loop Gain, is reduced by half in phase lock.

†LPF internal resistance is to GROUND, external resistance is to the filter

‡PUMP to VCON internal resistor is shorted during velocity lock

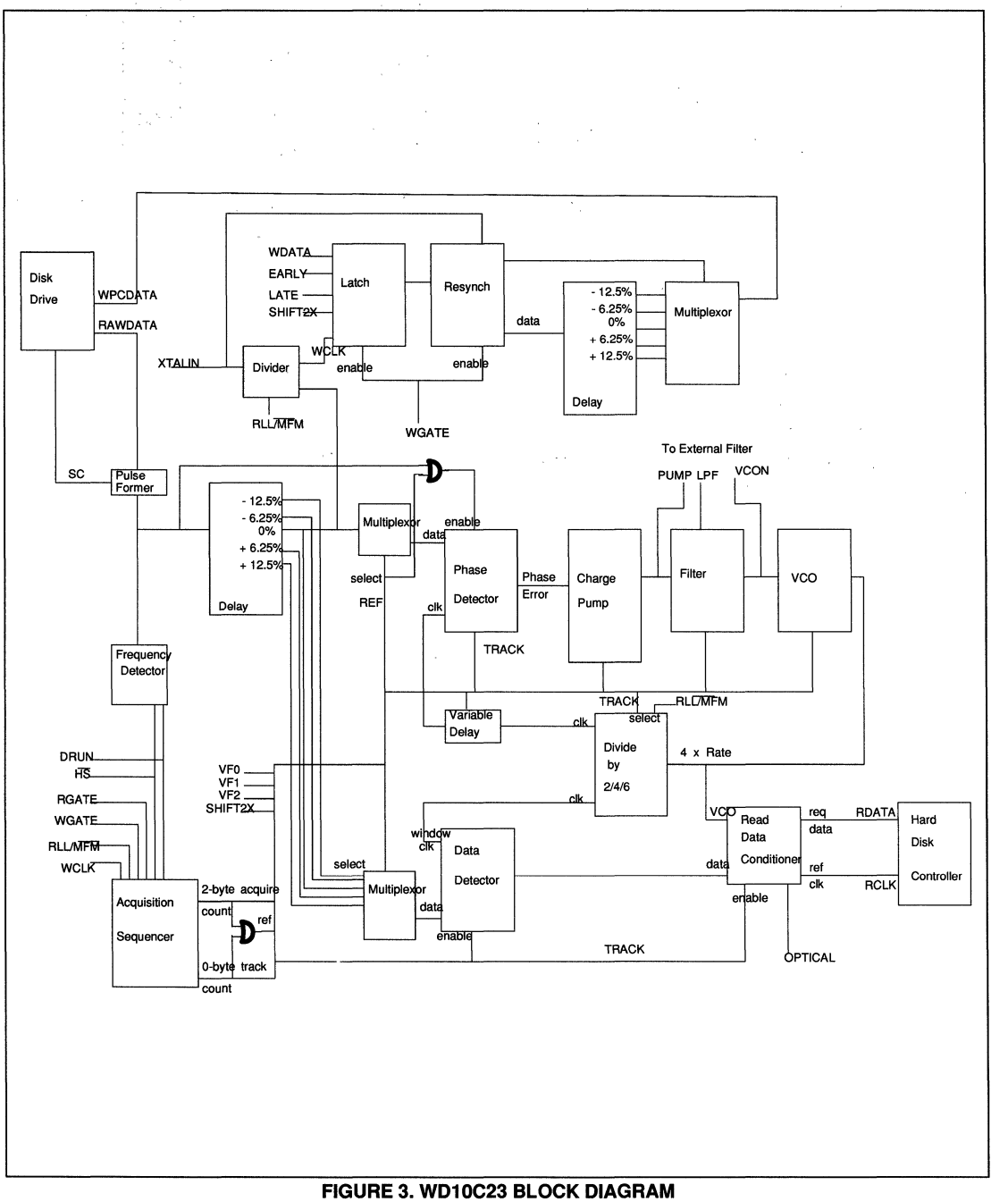


FIGURE 3. WD10C23 BLOCK DIAGRAM

2.2 Read Operations

The WD10C23 performs phase-locked loop data synchronization on read data from the drive. For soft-sector applications, an on-board synch field detector automatically switches the PLL from the stable crystal reference to the read data. Phase-frequency detection (velocity lock) is used at the beginning of the synch field to quickly and reliably acquire lock to the data. Use of this technique eliminates susceptibility to harmonics and asymmetry. The WD10C23 then switches to phase-only detection to complete the phase acquisition before the end of the synch field, and to enable tracking of random read data. The phase jump at the acquisition-to-tracking switchover due to multiplexing, seen in other circuits, is avoided through the use of a zero phase jump design.

When switching to phase detection, the WD10C23 reduces the charge pump gain for better jitter rejection. A precisely centered detector samples the data at twice the underlying data rate to remove the phase jitter. A proprietary technique adjusts the window width, T, to the current data rate, providing greater phase margin. The regenerated signal, along with a fixed-phase synchronous clock, are output for the controller's digital circuits.

2.3 Write Operations

The WD10C23 performs conditioning on write data to the drive. Data from the controller is precisely synchronized with the crystal reference at twice the data frequency, thus minimizing the addition of digital phase jitter on the write data to the drive. If enabled, precompensation is achieved via delay taps available through proprietary CMOS delay line technology. The delay line is servo-controlled to the crystal reference for precision. Synchronized, precompensated write data is thus sent directly to the drive's write circuits.

Precompensation levels are programmable to be either 12.5 or 6.25 percent of the window, defined by the inverse of the crystal frequency. The SHIFT2X input allows dynamic control of early and late precompensation magnitude for more complex precompensation schemes. In addition, SHIFT2X may be programmed using track information for zone bit precompensation schemes.

3.0 EXTERNAL COMPONENTS PARTS LIST

The parts list shown below gives typical component values for 5 Mbit/sec MFM and 5-15 Mbit/sec RLL data rates.

See the diagram on the opposite page for the location of each component.

Contact your local Western Digital sales representative for more information on how to change these values, to accommodate different data rates.

10C23 EXTERNAL COMPONENTS for 5 Mbits/sec (MFM) and 5-15 Mbits/sec (RLL)

PART #	TYPE	VALUE	SPECIFICATIONS
C111	capacitor	4700 pF	cer. , 5%, 50V, COG
C112	capacitor	150 pF	cer. , 5%, 50V, COG
C101	capacitor	47 µF	tan. , 20%,10V
C106	capacitor	0.1 µF	+80-20%, 50V, z5u
L101	----------	3.3 ohm	5%, 1/4 w
R107	resistor	590 ohm	1%, 1/4 w, 100 ppm
R301	resistor	301 ohm	1%, 1/4 w, 100 ppm
R302	resistor	3.01K ohm	1%, 1/4 w, 100 ppm
Y101	crystal	10-15 MHz	.01%, 3 leads
C104	capacitor	68 pF	cer. , 5%, 50V, COG
C105	capacitor	47 pF	cer. , 5%, 50V, COG
Y101	crystal	15-20 MHz	.01%, 3 leads
C104	capacitor	33 pF	cer. , 5%, 50V, COG
C105	capacitor	22 pF	cer. , 5%, 50V, COG
Y101	crystal	20-30 MHz	.01%, 3 leads
C104	capacitor	22 pF	cer. , 5%, 50V, COG
C105	capacitor	10 pF	cer. , 5%, 50V, COG

R302 resistor is left open for compatibility mode.
R301 & R302 resistors are left open for BAND0.

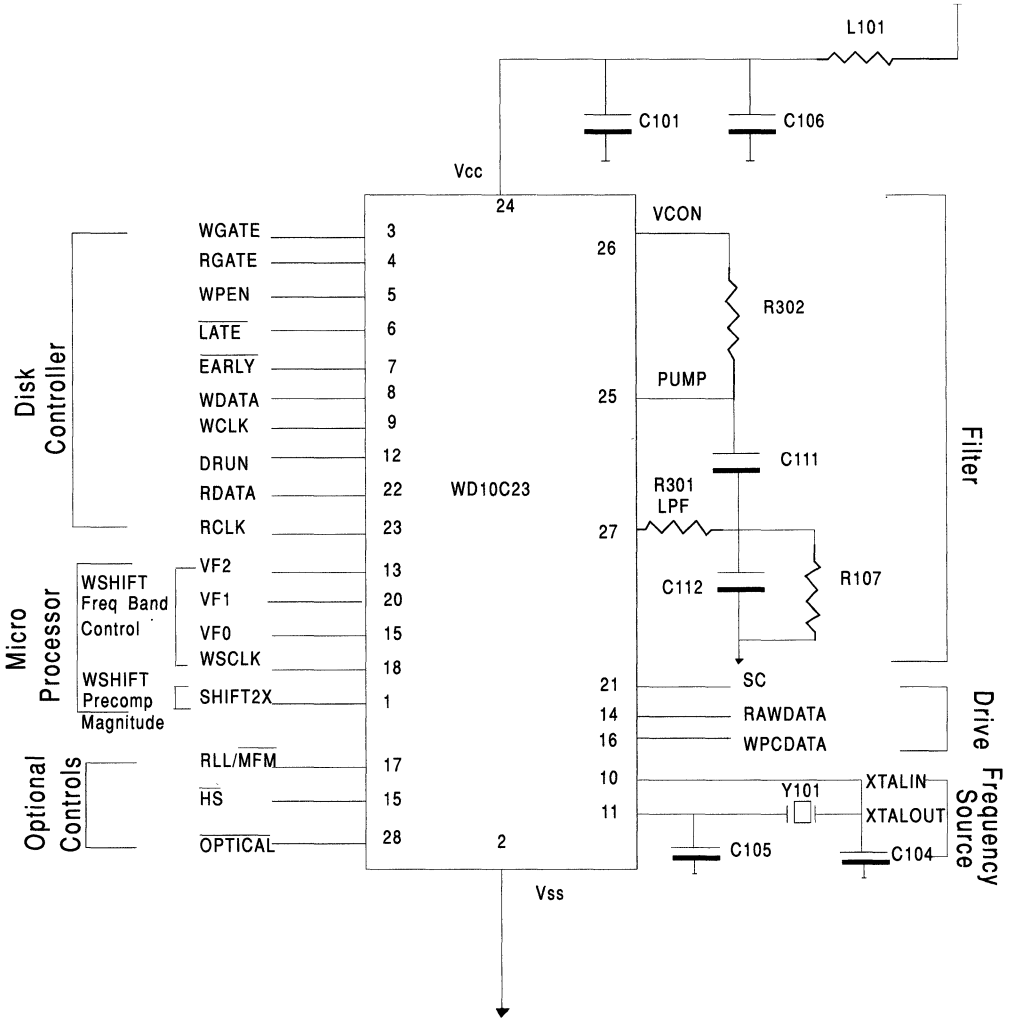


FIGURE 4. EXTERNAL COMPONENTS

4.0 PIN DESCRIPTIONS

Signals have the same pin numbers for both packages.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	SHIFT2X	SHIFT2X	I	Shift two times. When false, selects ±6.25% of the window for write precompensation and window shifting. When true, selects two times that amount or ±12.5 of the window. Internal pullup.
2	GND	GROUND	I	GROUND.
3	WGATE	WRITE GATE	I	Write gate. Set high when recording onto the disk. Write gate takes precedence over read gate.
4	RGATE	READ GATE	I	Read gate. Set high when the Controller intends to read.
5	WPCEN	WRITE PRECOMP ENABLE	I	Write precompensation enable. When high, it enables EARLY, LATE, and SHIFT2X for precompensation.
6	$\overline{\text{LATE}}$	LATE	I	Negative true inputs used to delay write data for write precompensation.
7	$\overline{\text{EARLY}}$	EARLY	I	Negative true inputs used to advance write data for write precompensation. Internal pullup.
8	WDATA	WRITE DATA	I	Write data to be conditioned and sent out through WPCDATA to be written onto the disk.
9	WCLK	WRITE CLOCK	O	Clock signal at one half the XTALIN frequency.
10	XTALIN	XTALIN	I	Input pins for a crystal oscillator circuit. If an external frequency source is desired, XTALIN can be driven and XTALOUT left open.
11	XTALOUT	XTALOUT	O	Output pins for a crystal oscillator circuit.
12	DRUN	DATA RUN	O	The output of a frequency detector connected to RAWDATA. Short, high frequency periods cause it to go high; long, low frequency periods cause it to go low. Used for detecting high frequency synch fields. Not used in hard sector.
13	VF2	VARIABLE FREQUENCY CONTROL	I	Tri-state input used during reads to select the operating frequency bands for PLL. Also selects the window shift diagnostic modes. VF2 is compatible with the WSHIFT pin on the 10C20A/21A/20B/22B when VF0 and VF1 are open.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
14	RAWDATA	RAW DATA	I	Data received from the drive read circuits. Includes an internal pullup resistor to allow tri-state multiplexing of the drives' data receivers.
15	VF0	VARIABLE FREQUENCY	I	Variable frequency tri-state input used during reads to select the operating frequency bands for PLL. Also selects the window shift diagnostic modes.
16	WPCDATA	WRITE PRECOMP DATA	O	Write precompensation data sent to the drive write circuits. Low when WGATE is low.
17	RLL/$\overline{\text{MFM}}$	RLL/$\overline{\text{MFM}}$ SELECT	I	When high, selects RLL (2,7) mode. When low, selects MFM (1,3) mode. Internal pullup.
18	WSCLK	WINDOW SHIFT CLOCK	I	Window shift clock reference. Internal pullup.
19	$\overline{\text{HS}}$	HARD SECTOR	I	When true, disables DRUN qualification on reads. RGATE controls the acquisition sequence to and from data. Internal pullup.
20	VF1	VARIABLE FREQUENCY	I	Variable frequency tri-state input used during reads to select the operating frequency bands for PLL. Also selects the window shift diagnostic modes.
21	SC/$\overline{\text{COAST}}$	SEEK COMPLETE	I	When low, disables RAWDATA and keeps VCO on reference. May be used to coast through defects when tracking. Internal pullup.
22	RDATA	READ DATA	O	Detected and regenerated version of RAWDATA. Jitter has been removed and pulses have been synchronized with RCLK.
23	RCLK	READ CLOCK	O	VCO divided to the data rate. Tracks the base frequency of RAWDATA during a read operation; otherwise tracks the crystal frequency.
24	V_{CC}	POWER SUPPLY	I	+5 Volts. Power supply input.
25	PUMP	PUMP	I/O	Charge pump output to the external filter.
26	VCON	VCO INPUT	I	Input to the external filter.
27	LPF	FILTER OUTPUT	O	Output of the external filter.
28	$\overline{\text{OPTICAL}}$	OPTICAL	I/O	Optical mode select. Used to enable test modes. Internal pullup.

5.0 ARCHITECTURE

The twelve major functions within the WD10C23 are listed below:

- Synchronization Field Detector
- Acquisition Sequencer
- Phase-Locked Loop (PLL)
  - —Phase-Frequency Detector
  - —Charge Pumps
  - —Filter
  - —Voltage Controller Oscillator (VCO)
- Read Data Conditioner
- Read Data Detector
- Phase Margining
- Crystal Oscillator
- Write Data Conditioner
- Delay-Locked Loop (DLL)
- Pulse Former
- Power-on Reset
- Test Modes

5.1 Synchronization Field Detector

The purpose of this circuit is to reliability discriminate between the high frequency of a PLL synchronization field and the lower frequencies immediately preceding it. The criterion used is pulse period discrimination on RAWDATA. If the period between consecutive rising edges of RAWDATA is short with respect to the threshold, then DRUN will go high; if long, then DRUN will go low.The pulses in the synchronization field must have the shortest period in the format (i.e. 3T for 2, 7 RLL; 2T for 1, 3 MFM). The pulses in the field preceding the synchronization field must have a period sufficient to drop DRUN.

In MFM mode, the optimum discrimination threshold is set using an internal delay line. In RLL mode, the threshold is set digitally.

When a synchronization field is detected, DRUN will remain high until address mark detection. At this time, the Synchronization Field Detector is put to sleep. Upon de-assertion of RGATE, the Detector will be awakened.

Although the Synchronization Field Detector is not used in hard sector mode (by either the controller or the internal Acquisition Sequencer), DRUN will still respond to pulse period information on RAWDATA.

5.2 Acquisition Sequencer

The Acquisition Sequencer sends sequencing control signals to the appropriate circuits when the WD10C23 switches between the read, write, and idle modes.

5.2.1 Idle-to-Read Sequencing

The soft sector read sequence begins when the Synchronization Field Detector raises DRUN in response to high frequency data on the RAWDATA input. If DRUN remains high for two NRZ byte times, the Sequencer switches the Phase - Frequency Detector from the crystal reference to the incoming data. The Phase-Frequency Detector is in phase-frequency (velocity lock) mode with the PLL set at high gain.

At the end of six bytes of velocity lock to data, RGATE is polled. If the controller has been issued a read command, RGATE will be true, and the Sequencer will switch the Phase-Frequency Detector to phase lock mode phase lock. The charge pump are set for low gain for improved jitter rejection.

At this time, the Acquisition Sequencer is put to sleep and disables the Synchronization Field Detector. Upon the dropping of RGATE, the Sequencer awakens the Synchronization Field Detector, sets the Phase Detector back to velocity lock, and sets the charge pumps back to high gain.

For hard sector formats, the acquisition sequence is slightly altered. RGATE alone initiates the acquisition sequence data, without qualification of the Synchronization Field Detector. At the end of eight bytes in velocity lock, the sequence is as described above.

5.2.2 Idle-to-Write Sequencing

The write sequencer is initiated by the assertion of WGATE. WGATE disables the Aquisistion Sequencer, which in turn puts the Synchronization Field Detector to sleep. The Phase Detector is forced to remain on the crystal reference for the duration of the write.

5.3 Phase-Locked Loop (PLL)

5.3.1 Phase-Frequency Detector

The Phase-Frequency Detector can be operated in two modes. The velocity lock mode is used for acquisition when the PLL is switched to read data, and is always used when the PLL is following the reference crystal oscillator. Whenever the device is not reading, the PLL is locked to XTALIN.

The second mode, phase lock, is standard phase-only detection. The Acquisition Sequencer switches to this mode when frequency acquisition is essentially complete on data, and phase acquisition is nearly complete as well. Phase-only mode must, of course, be used to lock to the data following the synch field, since that will contain the three frequencies inherent in MFM or the six frequencies inherent in RLL mode.

In either mode, the Phase-Frequency detector converts a phase difference between the VCO and input to a pulse width equal to the phase difference. The polarity of the phase error determines whether a signal will be routed to the pump up or pump down circuitry in the Charge Pump section.

5.3.2 Charge Pumps

This circuit converts the pulse widths received from the Phase-Frequency Detector to proportional amounts of charge into or out of the Filter. The symmetry of the Charge Pumps is continuously determined by the voltage on the VCON. A proprietary technique selects a pump up current which precisely matches that of the pump down at the given filter voltage.

When in phase lock, the gain is reduced by two.

5.3.3 Filter

The Filter converts the current pulses from the Charge Pumps to a voltage output to the VCO.

The Filter has been carefully designed to the specific requirements of damping factor, acquisition time, capture range, and jitter rejection; and within the context of its effect on VCO operation. Roughly speaking, it functions to filter out high frequency signals due to RAWDATA read data jitter, while passing the low frequency signals associated with the more slowly varying underlying frequency of RAWDATA, and handling a step change in input frequency when switching between drive data and reference.

The Filter is internal, with the exception of external components. In variable frequency applications, two additional external resistors are required.

5.3.4 Voltage Controlled Oscillator(VCO)

The VCO consists of an internal charge pump and ring oscillator. Thus, the VCO requires no expensive components, and has no tuning requirements for voltage, temperature, or aging.

The VCO converts the voltage developed by the Filter to a control voltage for the ring oscillator. The non-linear I-V characteristic inherent in most internal VCO designs, is eliminated by a proprietary technique, and loop gain is linearized over a wide frequency band.

The VCO runs at four times the channel rate and is divided down for extremely high precision duty cycles.

5.4 Read Data Conditioner

This circuit synchronizes the output of the Read Data Detector and produces the signals RCLK and RDATA. RCLK is a square wave at either one or two times the data rate selected via the OPTICAL input (see Table 3). During data tracking, the frequency of RCLK mirrors the slowly varying frequency of the raw data from the drive, RAWDATA. RDATA is a regenerated form of RAWDATA, with all jitter removed and positive pulses one window wide. It is synchronous with RCLK. RCLK edges occur nominally in the center of RDATA pulses to allow sufficient setup and hold time for the digital circuits in the controllers that use these signals. For the 2XRCLK, RDATA and RCLK edges are coincident. RDATA is DC low during velocity lock, and is activated by the Acquisition Sequencer approximately at the transition to phase lock.

RCLK will stop for several windows at the transition to phase lock for internal synchronization of the Read Data Detector and Read Data Conditioner.

5.5 Read Data Detector

The Read Data Detector latches the incoming drive data and presents it to the synchronization circuits of the Read Data Conditioner. Window shifting is performed here using one of several techniques described below.

To maximize phase margin, the window at the Read Data Detector is precisely centered and tracks the frequency of the incoming data.

5.6 Phase Margining

Phase margining is performed at the Read Data Detector by shifting the incoming raw read data either early or late with respect to the Read Data Detector's sampling clock or strobe. Window shifting is accomplished in one of two fashions described below, and is summarized in Table 2.

5.6.1 Window Shifting as Percentage of the Window

The first technique is compatible with previous Western Digital data separator designs. Window shifting is achieved by advancing or delaying the raw read data to the Read Data Detector through precision internal delay stages. Shifting is programmable to either ±6.25% or ±12.5% of the window, and is inversely proportional to the crystal frequency.

Window shifting as a percentage of the window applies for fixed frequency as well as variable frequency applications.

5.6.2 Adaptive Window Shifting/Centering (AWS)

This technique uses an external reference clock, WSCLK, to set the timing relationship of the raw read data to the Data Detector strobe. By allowing for a continuous, precision, user controlled strobe placement, the effective detection window may be advanced or delayed as desired. This feature, when used in conjunction with micro-processor interaction at the VF0-2 inputs (see Table 2) may be used to:

- Create an adaptive window centering scheme to offset any asymmetry induced by the read channel electronics
- Provide system self-test in the form of built-in PMA capabilities
- Execute error recovery algorithms

Using AWS, the absolute range of window placement is dictated by the VF0-2 control pins. Once the range, N, has been selected, window placement within that range is proportional to the period of the reference (WSCLK) with a gain of approximately 1/2 to 1/6. Thus, for every 1ns of change on the external source, window shift resolution ranges from 166 ps to 500 ps.

The value of N is the closest value which represents one quarter of the window, T/4, for any given data rate. For each of the twelve ranges, there exists some frequency on WSCLK for which the range is optimum. That is, the window position may be programmed symmetrically about this frequency up to plus or minus one-half window. When this center frequency is equal to the data rate, it is known as the Optimum Center Frequency, denoted f(N). Since "range" is now equal to "window", strobing may be programmed about f(N) up to ±window/2, denoted T/2.

As the data rate varies from f(N), the range set by N may be insuffient to achieve window placement across the full window. However, placement across the full window may be obtained by using a different value of N for early shifting than that for late shifting. Here are some examples.

Example 1:

If the actual data rate is 10.4Mbit/sec, selecting N=12 gives a 10.4Mbit/sec center frequency, $f(12)$. We have selected an Optimum Center Frequency. The window at 10.4Mbit/sec is 48ns. Varying WSCLK from 4.44Mhz to 12.32Mhz will allow window shifting over a range of 24ns to 72ns, or 48ns $\pm$T/2 (Figure 5).

For the partial range of 24ns to just under 48ns, the data is shifted from window center to the late edge of the window, respectively. This is equivalent to window shifting from 0ns to 24ns, or 0ns to +T/2.

For the partial range of just over 48ns to 72ns, the data is shifted into the next window, from that window's early edge to its center, respectively. This is equivelant to window shifting from -24ns to 0ns, or -T/2 ns to 0ns.

In the example, window shifting of $\pm$T/2 was achieved.

If however the actual data rate was 10Mbit/sec, a single value of N would be insufficient (we would not be at an Optimum Center Frequency).

Example 2:

For an actual data rate of 10Mbit/sec the window is 50ns. Again selecting N=12, the range of shifting achieved by varying WSCLK from 4.44Mhz to 12.32Mhz will be 24ns to 72ns, as in the example above (Figure 6).

For the partial range of 25ns to just under 50ns, the data is shifted from window center to the late edge of the window respectively. This is equivelent to window shifting from 0ns to 25ns respectively, or 0ns to +T/2.

For the partial range of just over 50ns to 72ns, the data is shifted into the next window, from that window's early edge to 3ns from its center respectively. This is equivelant to window shifting from -25ns to -3ns respectively, or -window/2 ns to -3ns.

Thus the range provided by N=12 is not sufficient to allow early window shifting over the full half window. If N were selected to be 13, the range would change from 24-72ns, to 26-78ns. Using the same analysis as above, this would allow early window shifting from -24ns to 0ns, and late window shifting of 0ns to 25ns, or 0ns to +T/2.

Thus by using one value of N for the early window shifting, and another value for late, the full range of $\pm$window/2 may be achieved.

Selection of N may be made by looking for the Optimum Center Frequency $f(N)$ which is closest the data rate in Table 2. N may also be determined using the relationships listed after Table 2.

27

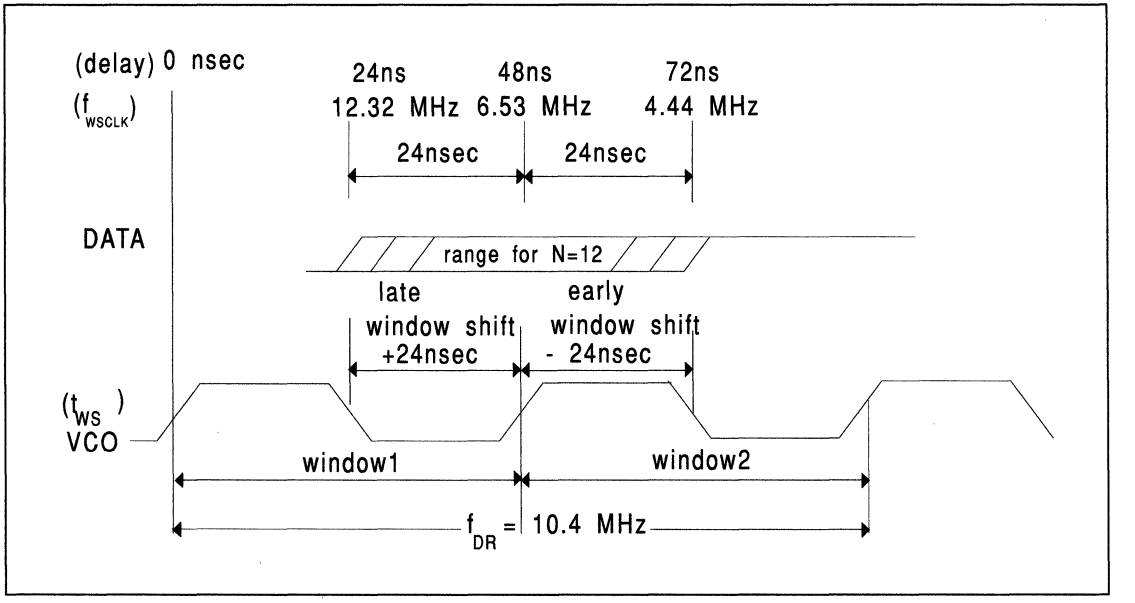


FIGURE 5. AWS OPTIMUM CENTER FREQUENCY

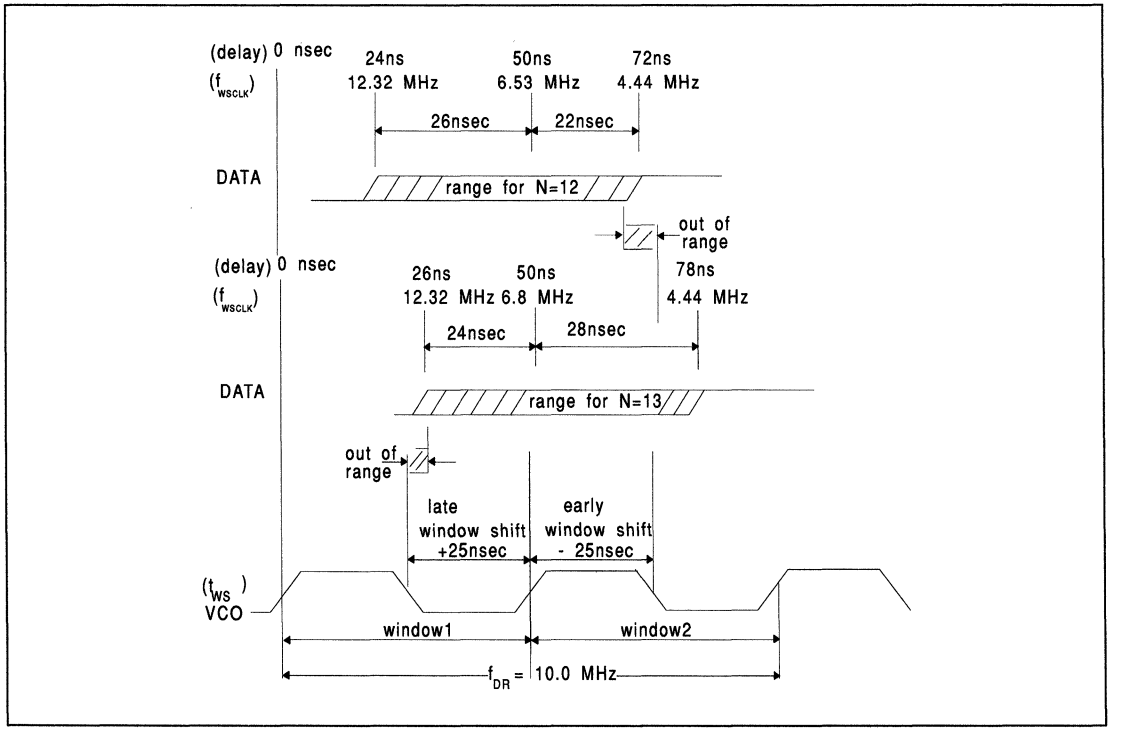


FIGURE 6. AWS NON-OPTIMUM FREQUENCY

Mode Selected	VF2	VF1	VF0	Data Rate (MHz)	Window Shift	Optimum Ctr f(N) MHz	Range N (T/4)
	0	0	z	$7.5 \leq f \leq 10.6$	Ext. Ref	7.4	17
	0	z	0	$7.5 \leq f \leq 10.6$	Ext. Ref	7.8	16
	0	z	1	$7.5 \leq f \leq 10.6$	Ext. Ref	8.3	15
	0	1	z	$7.5 \leq f \leq 10.6$	Ext. Ref	8.9	14
	z	0	z	$7.5 \leq f \leq 10.6$	Ext. Ref	9.6	13
Variable	z	z	0	$7.5 \leq f \leq 10.6$	Ext. Ref	10.4	12
Frequency -	z	z	1	$10.6 < f < 15.0$	Ext. Ref	11.4	11
Adaptive	z	1	z	$10.6 < f < 15.0$	Ext. Ref	12.5	10
Window Shift	1	0	z	$10.6 < f < 15.0$	Ext. Ref	13.9	9
	1	z	0	$15.0 = f$	Ext. Ref	15.6	8
	1	z	1	$15.0 = f$	Ext. Ref	17.8	7
	1	1	z	$15.0 = f$	Ext. Ref	20.8	6
	0	0	0	$5.0 \leq f < 7.5$	EARLY		
	0	0	1	$7.5 \leq f \leq 10.6$	EARLY		
	0	1	1	$10.6 < f < 15.0$	EARLY		
	0	1	0	$15.0 = f$	EARLY		
	z	0	0	$5.0 \leq f < 7.5$	None		
Variable	z	0	1	$7.5 \leq f \leq 10.6$	None		
Frequency -	z	1	1	$10.6 < f < 15.0$	None		
Percentage	z	1	0	$15.0 = f$	None		
Window Shift	1	0	0	$5.0 \leq f < 7.5$	LATE		
	1	0	1	$7.5 \leq f \leq 10.6$	LATE		
	1	1	1	$10.6 < f < 15.0$	LATE		
	1	1	0	$15.0 = f$	LATE		
Compatibility	0	z	z	5.0 MFM	EARLY		
Percentage	z	z	z	or	None		
Window Shift	1	z	z	7.5 RLL	LATE		

TABLE 2. PHASE MARGIN CONTROL

Relationships for Selecting Window Position:

1. t_{ws} = desired window shift in nsec, where $-2N \leq t_{ws} \leq 2N$
2. T_{wsclk} = required WSCLK period in MHz, where $4.44 \text{ MHz} \leq f_{wsclk} \leq 12.32 \text{ MHz}$
3. T_{dr} = data rate in nsec
4. $T_{wsclk}(N, t_{ws}, T_{dr}) = \{ (36/N)\, t_{ws} + [(9/N) T_{dr} + 9.2] \quad (t_{ws} \geq 0 \text{ ns})$
   $\{ (36/N)\, t_{ws} + [(27/N) T_{dr} + 9.2] \quad (t_{ws} \leq 0 \text{ ns})$

5.7 Crystal Oscillator

The Crystal Oscillator is designed to operate in the parallel resonant mode, with an external crystal and two capacitors. It generates the WCLK signal used externally. It is used primarily for internal reference when the PLL is not on data, and for accurate generation of the precompensated write data.

When an externally generated clock is desired, the crystal and capacitors are omitted. The XTALIN pin is connected to the clock source, with XTALOUT left unconnected.

The oscillator circuit includes a special implementation to better guarantee startup and to startup more quickly. A low value resistor is connected across the gain stage during the internal power-on reset. This quickly charges the external capacitors to the threshold value. As the resistor is disconnected, capacitive coupling induces a transient into the circuit, which helps to quickly achieve oscillation. A high value resistor is always present.

The oscillator should not be connected to any external circuits.WCLK may drive only high impedence MOS inputs. See the DC Electrical Characteristics section for specific limitations.

5.8 Write Data Conditioner

The Write Data Conditioner samples and precisely synchronizes WDATA, EARLY, LATE and SHIFT2X on the rising and falling edges of WCLK. They are immediately pipelined into flip-flops that are sampled on one edge of the XTALIN frequency (twice WCLK) to remove all jitter due to differential rise and fall times of WCLK.

When WGATE is active, the synchronized WDATA is channeled through an internal delay line for precompensation. If WPCEN is low, then the nominal delay is selected and passed to the WPCDATA output pin. If WPCEN is high, then the EARLY and LATE signals will select the early or late delays, respectively with SHIFT2X selecting the magnitude of shift. If both EARLY and LATE are inactive, or in the illegal case when they are simultaneously active, the nominal delay will be selected.

The differential delay between the early WPCDATA and nominal WPCDATA defines the amount of early precompensation, and similar, nominal WPCDATA to late WPCDATA defines the amount of late precompensation. The value is nominally 6.25%, or 12.5% with SHIFT2X active.

It should be noted that SHIFT2X may be used for dynamic dual level precompensation, or programmed with track information for zone level precompensation.

Finally, in MFM soft sector formats, the third WPCDATA output pulse on any given write operation is suppressed. This is done to ensure a low frequency interval after the write splice, required for initialization of the Acquisition Sequencer on subsequent reads.

5.9 Delay-Locked Loop (DLL)

This section includes the integrated delay lines and RAWDATA pulse forming logic of the WD10C23.

The Delay-Locked Loop consists of an integrated active delay line, phase detector, charge pump, and internal filter. The DLL has special start-up and monitoring circuitry to prevent harmonic lock and to provide for faster acquisition.

The DLL, when locked to the incoming XTALIN reference, will provide a 360^0 phase shift through its sixteen delay stages. Thus, each delay stage will accurately provide delays of XTALIN period/16. Since the XTALIN period is equal to the window, each delay cell represents $\pm$6.25% window. It is these delay stages which are used for accurate write data precompensation, window centering during reads, and window shifting as a percentage of the window.

5.10 Pulse Former

Pulse forming on RAWDATA is used to provide internal pulses suitable for use by the internal circuitry. In response to input rising edges on RAWDATA, it produces internal positive pulses terminated by a Delay Line tap. Pulse forming makes the WD10C23 extremely insensitive to the normal pulse width modulation seen on the raw read data from the read channel circuits.

5.11 Power-on Reset

This integrated function is used to reliably initialize the flip-flops to a predictable state during the application of V_{CC}. It is also used by the Crystal Oscillator startup circuit and DLL for fast and reliable startup.

5.12 Test Modes

The WD10C23 has several built-in modes for testability. Test modes are activated via one of two sequences.

The primary method of invoking test modes is through the OPTICAL pin. With the appropriate selection of EARLY,LATE, and WPCEN, one of the following tests may be selected:

5.12.1 Optical Mode

This mode allows RCLK to be generated at two times the data rate for compability with the WD60C31A optical ENDEC.

5.12.2 Acquisition Sequencer Mode

This mode passes the CRGATE and PLOCK signals to RDATA and RCLK respectively. CRGATE is a composite read gate signal, activated upon the switchover from reference to raw read data after two bytes of high frequency data have been sensed by the Synchronization Field Detector. PLOCK is asserted just prior to the transition from VLOCK to PLOCK.

5.12.3 Pump Up Mode

This test disables the data input to the Phase Detector, forcing a DC pump down. In this mode, the internal feedback from VCON to PUMP is opened, and the PUMP clamp defeated. With VCON forced to its locked voltage, the PUMP'S source I-V characteristics may be obtained.

5.12.4 Pump Down Mode

This test disables the data input to the Phase Detector, forcing a DC pump down. In this mode, the internal feedback from VCON (VCO control voltage) to PUMP (Charge Pump output) is opened. With VCON forced to its locked voltage, the PUMP's sink I-V characteristics may be obtained.

5.12.5 Phase Detector Mode

This test passes the Phase Detector's phase error signals to the Read Data Conditioner output, RDATA and RCLK. RDATA will represent frequency up, and RCLK frequency down. These signals, when used differentially, can be used to reconstruct the error amplifier envelope. This test may be used in conjunction with Pump Up/Down Tests when forcing D.C. pump up/down.

The second method of envoking tests is through illegal states.

5.12.6 Reset/Synchronization Mode

This mode is envoked by pulling $\overline{\text{EARLY}}$ and LATE low (illegal), and pulling WGATE high. Once in this configuration, the WPCEN pin may be used to generate an internal synchronization/reset pulse. The pulse will begin on the leading edge of WPCEN and end on the falling edge of WPEN.

This test is used to initialize internal logic states which may be otherwise unknown. For instance, WCLK is a divide-by-two of XTALIN, and its phase relationship is not important to system operation. For testablility however, the phase is important.

In this mode WCLK is set high, RCLK is set high, the internal VCO divider, is initialized, the VCO ring oscillator is halted, the Phase Detector is initialized, the Charge Pump is tristated, the Acquisition Sequencer is placed in velocity lock mode, the PUMP to VCON internal resistior is opened, and the PUMP clamp is defeated.

RGATE must not be true on the falling edge of WPEN. See External VCO Test.

5.12.7 Internal/External VCO Modes

The External VCO mode is envoked by pulling EARLY and LATE low (illegal), and pulling RGATE and WGATE high (illegal). WPCEN is now pulsed high for a duration of at least five XTALIN clocks. On the falling edge of WPCEN, an internal clock edge is created. This internal clock edge latches the state of the VCO selector: RGATE high selects External VCO mode; RGATE low selects Internal VCO mode.

This sequence is identical to the Synchronization/Reset Test above. When WPEN is true, this test is executed.

In External VCO mode, the PLL is running open loop with the VCO clock supplied through the OPTICAL input. The external VCO must be four times the data rate.

In External mode, PUMP to VCON internal resistance is open; the PUMP clamp is defeated, and OPTICAL is internally decoded as an active low. This allows OPTICAL to be used as the VCO input, while still allowing test mode selection.

Caution should be used to ensure that a test mode is not inadvertantly selected via the states of EARLY, LATE, WPCEN, RGATE, and WGATE.

EARLY	LATE	WPCEN	OPTICAL†	WGATE	RGATE	TEST MODE
x	x	x	1	x	x	Normal Operation
0	0	1	x	1	x	Reset/Synch Mode
0	0	⎍	x	1	0	Internal VCO Mode
0	0	⎍	x	1	1	External VCO Mode†
0	0	0	0	x	x	Phase Detector Mode
0	0	1	0	0	x	Acquisition Sequencer Mode
0	1	0	0	x	x	Pump Up/Phase Det Mode
0	1	1	0	x	x	Pump Up Mode
1	0	0	0	x	x	Pump Dn/Phase Det Mode
1	0	1	0	x	x	Pump Down Mode
1	1	0	0	x	x	Optical Mode
1	1	1	0	x	x	Normal Operation

TABLE 3. TEST MODE MATRIX

† After latching the external VCO mode of operation, $\overline{\text{OPTICAL}}$ is internally decoded as a logic low to allow for the enabling of the various test modes. Caution should be used to avoid inadvertantly enabling test modes under this condition.

6.0 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Operating Temperature	0°C (32°F) to 70°C (158°F)
Storage Temperature	-55°C (-67°F) to +125°C (257°F)
Voltage on any pin with respect to ground (except XTALIN):	-0.5 to V_{CC}+0.5 volts
Voltage on XTALIN with respect to ground	-0.1 to V_{CC}+0.5 volts
Supply Voltage with respect to ground	+5.5 volts

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the above.

6.2 Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to ground.

Operating temperature (TA)	0°C (32°F) to 70°C (158°F)
Power supply voltage (VCC)	+5.0V±.25V

27

6.3 Digital Signals

Input Signals:WGATE, RGATE, WPCEN,

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Voltage input high	2.0			V	
V_{IL}	Voltage input low			0.8	V	

Input Signals: SHIFT2X,RAWDATA,RLL/$\overline{MFM}$,WSCLK,$\overline{HS}$, SC/$\overline{COAST}$,$\overline{OPTICAL}$,WDATA,$\overline{EARLY}$,$\overline{LATE}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Voltage input high	2.0			V	
V_{IL}	Voltage input low			0.8	V	

Input Signals: RGATE,WGATE,WPCEN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{IN}	Input leakage current	-10		+10	µA	V_{IN}=GND to V_{CC}

Input Signals: SHIFT2X,RAWDATA,RLL/$\overline{MFM}$,WSCLK,$\overline{HS}$,SC/$\overline{COAST}$,$\overline{OPTICAL}$,WDATA,$\overline{EARLY}$, $\overline{LATE}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{IH}	Input high current	-0.1			mA	V_{IH}= 2.40 V*
I_{IL}	Input low currrent			-1.0	mA	V_{IL}=0.40V*

* Internal pullup resistor (10Kohm).

Input Signal: VF2, VF1, VF0

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Voltage input high	0.8V_{CC}			V	
V_{IT}	Voltage input 3-st volt	0.4V_{CC}		0.6V_{CC}	V	
V_{IL}	Voltage input low			0.2V_{CC}	V	
I_{IH}	Input high current	0.2		0.7	mA	V_{IH}=4.4 V, *
I_{IL}	Input low current	-0.2		-0.7	mA	V_{IL}=0.6 V, *
I_{IZ}	Input high Z current	-50.0		+50.0	µA	V_{IN} tristated, *, **

* Internal pullup and pulldown resistors (10Kohm). I_{IZ} tristate driver leakage current tolerance 50 µA.

**Allowable leakage of the tristate driver. Leakage greater than this will pull the input level out of the tristate band. This parameter is guaranteed by forcing voltages at the edge of the tristate band and measuring a tolerance greater than or equal to the I_{iz} specification.

Input Signal: VF2, VF1, VF0

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{RISE}	Rise time			25.0	nsec	0.2 V_{CC} to 0.8 V_{CC}; *
t_{FALL}	Fall time			25.0	nsec	0.8 V_{CC} to 0.2 V_{CC}; *

* Internal pullup and pulldown resistors (10Kohm). I_{IZ} tristate driver leakage current tolerance 50 µA.

Input Signal: XTALIN*

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Voltage input high	2.0			V	$f \leq 20.0$ MHz
V_{IL}	Voltage input low			0.8	V	$f \leq 20.0$ MHz
V_{IH}	Voltage input high	3.0			V	$f > 20.0$ MHz
V_{IL}	Voltage input low			0.4	V	$f > 20.0$ MHz

* Externally generated oscillator; XTALOUT open

Power Supply Currents: V_{CC}

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{CCA}	5v active current		25	35	mA	V_{CC} = 5.25; *
I_{CCS}	5v static current		6	10	mA	V_{CC} = 5.25; **

* I_{CCA} measured as follows : Highest current draw is at 15 Mbit/sec during a write operation, with WSCLK programmed to 14 MHz and the VF pins programmed to one of the Adaptive Window Shift states. Idle currents will be several mamps lower.

** I_{CCS} measured as follows: During the Reset Test Mode, pull XTALIN high after the required number of XTALIN clocks. Follow by grounding WGATE, RGATE, WPCEN; all other pins floating.

Power Supply Voltage: V_{CC}

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{PRD}	Power reset inactive	4.1			V	*
V_{PRA}	Power reset active			2.6	V	**

* At this level V_{CC} level and above, the power-qualified reset is guaranteed to be inactive.

** At this level V_{CC} level and below, the power-qualified reset is guaranteed to be active.

MOS Outputs:WCLK, RCLK, RDATA, DRUN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OH}	Output high volt	2.4			V	I_{OH}=-20μA
V_{OL}	Output low volt			0.4	V	I_{OL}=+20μA
t_{RISE}	Rise time			7.0	nsec	0.8 to 2.0 V; *
t_{FALL}	Fall time			4.0	nsec	2.0 to 0.8 V; *

* Specified with a maximum external load of 20 pF; intended for high impedence MOS receivers, whose input threshold requirement is TLL compatible (i.e. 2.0/0.8V V_{IH}/V_{IL})

TTL Outputs:WPCDATA

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OH}	Output high volt	2.4			V	I_{OH}=-400μA
V_{OL}	Output low volt			0.4	V	I_{OL}=+2.0mA
t_{RISE}	Rise time			7.0	nsec	0.8 to 2.0 V; *
t_{FALL}	Fall time			4.0	nsec	2.0 to 0.8 V; **

* Specified with 20 pF/20 kΩ load to V_{SS}; intended for TLL receivers

**Specified with 20 pF load to V_{SS}/2 kΩ load to V_{CC}; intended for TLL receivers

6.4 Analog Signals (Crystal Oscillator)

Input: XTALIN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LKX}	Input leakage currents	-100		+100	nA	$V_{IN}/V_{OUT}=V_{IBIAS}$
V_{IBIAS}	Input bias volt	1.0		1.8	V	XTALOUT floating

Leakage measured after the internal Power-On Reset has timed out.

Output: XTALOUT

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{OLS}	Short circuit sink current	4.5		18	mA	V_{CC}=+5; XTALIN=2.5V,XTALOUT=5V
I_{OHS}	Short circuit source current	-1.6		-9.4	mA	V_{CC}=+5; XTALIN,XTALOUT=0
R_{BO}	Operating bias resistance	1.1		5.6	Mohm	*
R_{BS}	Startup bias resistance	8		70	Kohm	**

*Measured after the internal Power Qualified Reset has timed out, R_{BO} is the feedback resistance between XTALIN and XTALOUT. With Vcc=5V, XTALOUT=0V, R_{BO} is modelled as a resistance combination with the measured leakage resistance, $R_{LKX} = V_{IBIAS}/I_{LKX}$. With XTALIN=$V_{IBIAS}$, XTALOUT = 0V, I_{LKX} measured at the XTALIN input is given by $V_{IBIAS}(1/R_{BO} + 1/R_{LKX})$ for leakage to GND, or by $V_{IBIAS}(1/R_{BO} + 1/R_{LKX})-5/R_{LKX}$ for leakage to Vcc. After measuring I_{LKX}, R_{BO} may be computed.

**Measured during the internal Power Qualified Reset, R_{BS} is the internal parallel resistor combination of R_{BO} and an additional resistor activated during Power Qualified Reset. R_{BS} is modelled as a parallel resistance to the measured leakage resistance $R_{LKX} = V_{IBIAS}/I_{LKX}$. To ensure that PQR is active, the supply should be set at 2.5V. At this supply setting, measure V_{IBIAS}. With XTALIN=V_{IBIAS}, XTALOUT = 0V, and Vcc=2.5V, I_{LKX} measured at the XTALIN input is given by $V_{IBIAS}(1/R_{BS} + 1/R_{LKX})$ for leakage to GND, or by $V_{IBIAS}(1/R_{BS} + 1/R_{LKX})-2.5/R_{LKX}$ for leakage to Vcc.

6.5 Phase-Locked Loop

Filter Input/Output: PUMP, VCON

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS*
I_{LKV}	VCON leakage current			100	nA	VCON=V_{CC}, *
I_{LKP}	PUMP leakage current	-100		100	nA	PUMP =V_{CC}/GND, *
I_{CLP}	PUMP clamp current	4		15	mA	VCON/PUMP=V_{CC}, **
V_{CAP}	PUMP clamp act threshold	2.7		3.9	V	$I_{PUMP} \geq$ 2.5 mA, **
V_{CDP}	PUMP clamp deact thrsh'd	.55		1.15	V	I_{PUMP} < 2.5 mA, **
I_{CLN}	VCON clamp current	1.3		4.5	mA	VCON=GND, **
V_{CLN}	VCON clamp threshold	.5		.95	V	I_{VCON} = -1µA, **
R_{PVC}	Pump-VCON comp res	2.2	3	5	Kohm	†
R_{PV0}	Pump-VCON BAND0 res		∝		ohm	†
R_{PV1}	Pump-VCON BAND1 res		∝		ohm	†
R_{PV2}	Pump-VCON BAND2 res	4.0	6	9.8	Kohm	†
R_{PV3}	Pump-VCON BAND3 res	2.3	3.5	5.6	Kohm	†
R_{PVV}	Pump-VCON Vlock res	531	627	1381	ohm	‡

* High impedence is guaranteed by placing the device in the Reset Test Mode to open the PUMP to the VCON resistor, tristate the Charge Pump, and disable the PUMP clamp. Leakage on VCON is not measured to V_{CC}, as there is a low voltage clamp on this pin.

** The PUMP clamp will activate, pulling PUMP low, when VCON rises above the PUMP clamp activation threshold voltage. The PUMP clamp is latched until VCON falls below the clamp deactivation threshold. The VCON clamp will activate, keeping VCON above ground, when VCON falls below the VCON clamp threshold. Both clamp currents/voltages should be measured after tristating the Charge Pump by disabling the RAWDATA input in phase lock, and selecting BAND0 or BAND1 to open the internal resistance betweeen PUMP and VCON.

† Measured during phase lock, this is the internal filter resistance between PUMP and VCON. The measurement should be made in the correct band with PUMP =1.5 V and VCON = 2.0 V.

‡ Measured during velocity lock, this is the internal filter resistance between PUMP and VCON. The measurement may be made in any band with PUMP = 1.5 V and VCON = 2.0V

Filter Input/Output: LPF

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LKL}	Leakage current	-10		10	µA	*
R_{LPC}	LPF-GND comp res		∝		ohm	**
R_{LP0}	LPF-GND BAND0 res		∝		ohm	**
R_{LP1}	LPF-GND BAND1 res	1.5	2.8	4.8	Kohm	**
R_{LP2}	LPF-GND BAND2 res	300	525	950	ohm	**
R_{LP3}	LPF-GND BAND3 res	75	150	250	ohm	**

* Tristate on LPF is guaranteed by setting VF0/=00 or zz.

** This in the internal filter resistance between LPF and GND. The measurement should be made in the correct band with LPF=2.0 V.

27

Charge Pump: PUMP

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS*
I_{PLP}	Comp/BAND0-2 pmp cur	40		200	µA	phase lock
I_{PLV}	Comp/BAND0-2 pmp cur	80		400	µA	velocity lock
I_{PHP}	BAND3 pump current	80		400	µA	phase lock
I_{PHV}	BAND3 pump current	160		800	µA	velocity lock
R_{PB}	Pump cur symmetry ratio	.95		1.05		I_{up}:I_{down}
R_{KDVP}	Vlock-Plock pmp gain ratio	1.9		2.1		K_D Vlock:Plock
R_{KDH1}	Hi-lo band pump gain ratio	1.9		2.1		K_{D3}:K_{D2}

* Currents are for the measured VCON voltages found at the frequency extremes of the specified frequency bands, and are specified as magnitudes. Pump current is related to VCON approximately by $I \cong \beta (V_{CON} - Vt)^2$.

VCO: VCON

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
V_{CON}	VCO N-Channel control volt	.9		2.4	V	*
K_{OM}	Comp VCO gain	150		450	%/V	5Mbit MFM, **
K_{OR}	Comp VCO gain	150		450	%/V	7.5Mbit RLL, **
K_{O0}	BAND0 VCO gain	150		500	%/V	**
K_{O1}	BAND1 VCO gain	50		450	%/V	**
K_{O2}	BAND2 VCO gain	50		450	%/V	**
K_{O3}	BAND3 VCO gain	50		450	%/V	**
K_{OLM}	Comp open loop gain	15		45	%mA/V	MFM, †
K_{OLR}	Comp open loop gain	15		45	%mA/V	RLL, †
K_{OL0}	BAND0 open loop gain	10		45	%mA/V	†
K_{OL1}	BAND1 open loop gain	10		50	%mA/V	†
K_{OL2}	BAND2 open loop gain	10		50	%mA/V	†
K_{OL3}	BAND3 open loop gain	30		79	%mA/V	†

* This is the voltage developed by the filter and charge pump used to drive the internal VCO. The VCON voltage will be within this range for each of the four K_O settings in Table 1.

** The VCO frequency is proportional to the square of the voltage, V_{CON}, on the VCON input. VCO gain is given by % $(\Delta f / f_{AVE})$ $(1/\Delta V_{CON})$, or 4000 $(f2 - f1) / (f2 + f1)$ where $f2$ and $f1$ are the frequencies at $V_{CON} \pm$ 25mV respectively. The gains are specified for the V_{CON}'s found at the frequency extremes of the frequency bands. (i.e., at 5 and 7.5 MHz for BAND0).

† The open loop gain is given as a product of K_O and the average Charge Pump current. Specifically, $K_{O1} = K_O I_{AVE} = 2000\ (f2 - f1)\ (I2+I1)/\ (f2 + f1)$ where I2 and I1 are the Charge Pump currents found at the V_{CON} voltages determine $f2$ and $f1$, respectively.

7.0 TIMING CHARACTERISTICS

The following timings have been, where applicable, expressed in terms of the data rate by T = 1/(2x NRZ data frequency), for data frequencies in the range of 5 to 15 MBit/sec.

Several timings are referenced using a phase relationship of input signals called NULL phases. These phases should be such that there is zero phase error at the Phase Detector and zero net charge transfer on the PUMP pin. When the PLL is acquiring data in velocity lock mode, for a given set of conditions there is one phase of RAWDATA with respect to VCOIN which results in zero net current on PUMP. This phase is called NULLV (denoted ΘV).

The equivalent phase relationship found when the PLL is tracking data in phase detection mode is called NULLP(denoted Θp). When the PLL is tracking the crystal reference, the corresponding NULL, NULLX (denoted Θx), refers to the equivalent phase between XTALIN and the VCO.

All timings are measured with input levels of 2.4V V_{IH} and .4V V_{IL}, Ta = 0 °C to 70 °C; V_{SS} = 0V, V_{CC} = 5 V + 0.25 V. Closed loop PLL timings will be guaranteed to within ±1ns for power supply ripple of no more than 30mV peak to peak.

Transition times are measured at the 2.0 V crossing for high going transitions, and at the 0.8 V crossing for low going. Any deviations from these criteria will be specified.

27

7.1 Disk Drive Raw Read Data

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{RDH}	RAWDATA pulse width high	15			nsec	
t_{RCL}	RAWDATA pulse width low	15			nsec	
t_{RDT}	RAWDATA period	T			nsec	MFM mode, *
t_{RDT}	RAWDATA period	2T			nsec	RLL mode, *

* This timing is intended to indicate that two consecutive bit shifts, in a direction such that a minimum interval is created, can be tolerated up to just under T/2ns each without recycle failure in the phase or data detectors.

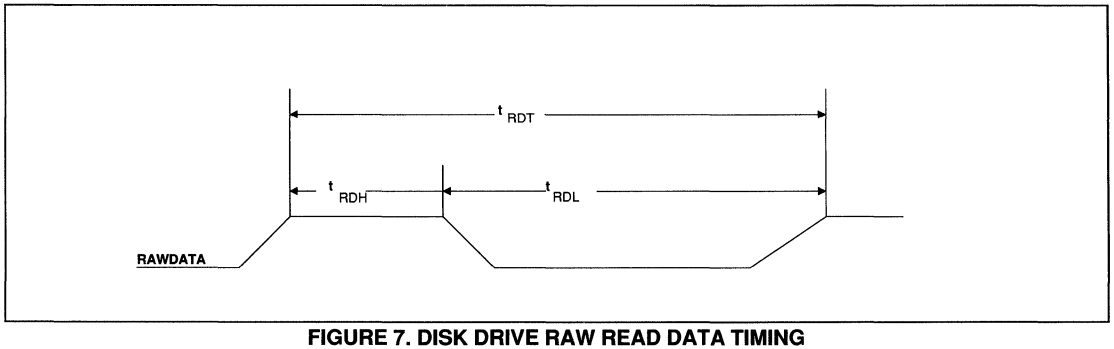


FIGURE 7. DISK DRIVE RAW READ DATA TIMING

7.2 Disk Drive
Raw Read Data Frequency Detector

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{DRL}	DRUN low freq threshold	2.50T	2.625T	2.75T	nsec	MFM mode, *
t_{DRH}	DRUN high freq threshold	1.188T	1.313T	1.438T	nsec	MFM mode, *
t_{DR}	DRUN threshold	4T		5T	nsec	RLL mode, **

* DRUN is guaranteed to be high for RAWDATA frequencies greater than t_{DRL} but less that t_{DRH}. For frequencies less than t_{DRL}, DRUN will not remain high, and for those greater than t_{DRH} DRUN behavior is not specified. DRUN low pulse widths will always reflect the pulse periods on RAWDATA for those periods which cause DRUN to drop. Thus the minimum will typically be 2.625T nsec.

** DRUN mInimum low pulse widths will be typically T nsec.

7.3 Read Data Conditioner

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS*
t_{RDP}	RDATA pulse width		T		nsec	
t_{RCP}	RCLK pulse width		T		nsec	
t_{RCS}	RDATA setup to RCLK	T/2-6.6	T/2	T/2+6.6	nsec	
t_{RCH}	RDATA hold from RCLK	T/2-6.6	T/2	T/2+6.6	nsec	

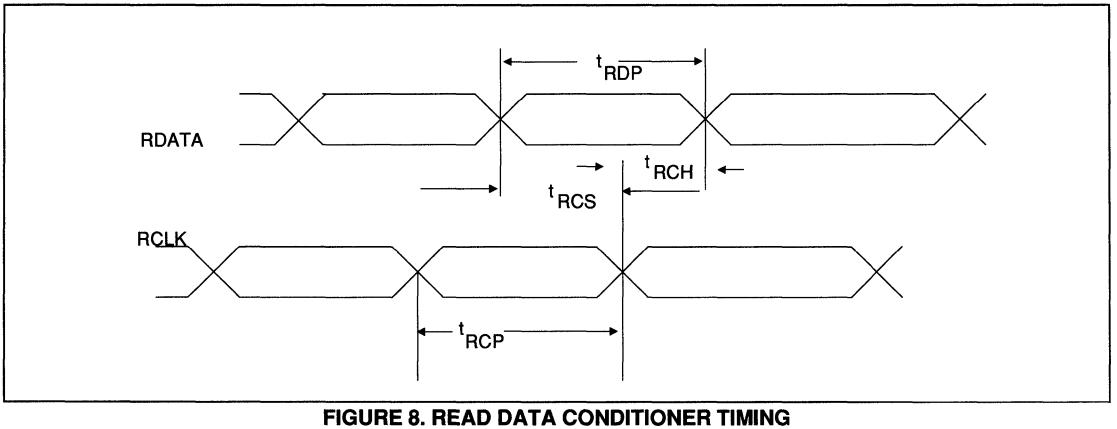


FIGURE 8. READ DATA CONDITIONER TIMING

7.4 Read Data Detector (Percentage Window Shift)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{DDW}	Data Detect Window	T-1	T	---	nsec	
t_{DWC}	DD Center Window	x/2-1	x/2	x/2+1	nsec	x = T_{DDW}, *
t_{DWSE1}	DD Window Shift Early 1X	-T/16-1	T/16	-T/16+1	nsec	SHIFT2X=GND
t_{DWSL1}	DD Window Shift Late 1X	T/16-1	T/16	T/16+1	nsec	SHIFT2X=GND
t_{DWSE2}	DD Window Shift Early 2X	-T/8-1	T/8	-T/8+1	nsec	SHIFT2X=V_{CC}
t_{DWS12}	DD Window Shift Late 2X	T/8-1	T/8	T/8+1	nsec	SHIFT2X=V_{CC}

* Window centering, t_{DWC}, is not a function of window loss and is thus correctly specified in terms of t_{DDW}.

7.5 Read Data Detector (Adaptive Window Shift)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{WS}	AWS Accuracy			5	%/Δns	**

** The accuracy is specified as the error in the gain (slope), 36/N, as given by equation 4 from Table 2. The t_{WS} error is determined by multiplying the difference in T_{WSCLK} from 153.2 ns. For example, if the required T_{WSCLK} is 160.2 ns, then the maximum t_{WS} error will be the 0.05x(160.2 -153.2)=350ps. If the required T_{WSCLK} were 150.2 ns, the maximum error would be 0.05x(150.2-153.2)ns=-150ps.

7.6 Phase-Frequency Detector

7.6.1 Phase Lock Mode

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{PDW}	Phase Detect Window		T		nsec	*
t_{PWC}	Phase Centering Window	x/2-1	x/2	x/2+1	nsec	$x=T_{PDW}$, *

* The phase detection window must be equal to T. Any apparent gain or loss in the window must be due to tester inaccuracy and/or statistical error in the measurement. Phase window centering is not a function of window size, and is thus correctly specified in terms of T_{PDW}.

27

7.6.2 Velocity Lock Mode (MFM)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{VDW}	Velocity Lock Detect Window		4T		nsec	
t_{VWE}	Velocity Lock Early Window		2T		nsec	
t_{VWL}	Velocity Lock Late Window		2T		nsec	

7.6.3 Velocity Lock Mode (RLL)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{VDW}	Velocity Lock Detect Window		6T		nsec	
t_{VWE}	Velocity Lock Early Window		3T		nsec	
t_{VWL}	Velocity Lock Late Window		3T		nsec	

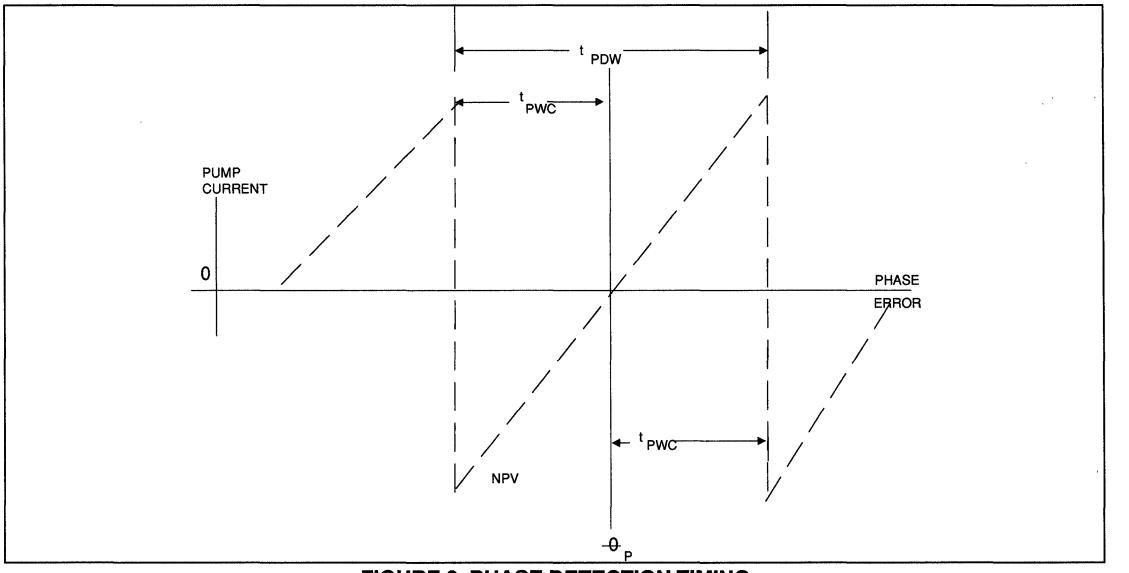


FIGURE 9. PHASE DETECTION TIMING

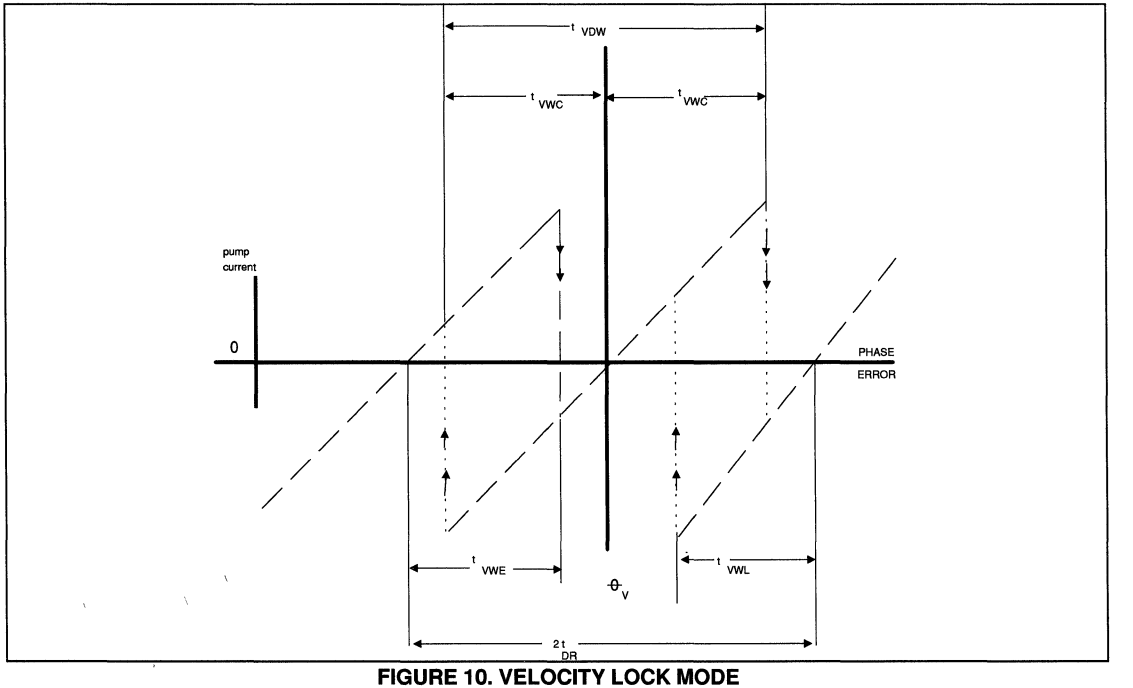


FIGURE 10. VELOCITY LOCK MODE

7.7 Write Data Conditioner

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{WCS}	WD setup to WCLK	8			nsec	*
t_{WCH}	WD hold from WCLCK	3			nsec	*
t_{PCE1}	Early precomp 1X	T/16-1	T/16	T/16+1	nsec	**, SHIFT2X=GND
t_{PCL1}	Late precomp 1X	T/16-1	T/16	T/16+1	nsec	**, SHIFT2X=GND
t_{PCE2}	Early precomp 2X	T/8-1	T/8	T/8+1	nsec	**, SHIFT2X=VCC
t_{PCL2}	Late precomp 2X	T/8-1	T/8	T/8+1	nsec	**, SHIFT2X=VCC
t_{PCP}	WPCDATA high	T-10	T		nsec	***, SHIFT2X=GND
t_{WPD}	WDATA to WPCDATA	.5T		2.75T+50	nsec	

* Timings are for WDATA, $\overline{EARLY}$, $\overline{LATE}$, and SHIFT2X.

** Differential measurement of rising edge of precompensated WPCDATA versus non-precompensated WPCDATA.

*** Measured for early and late precompensated WPCDATA.

27

7.8 TTL XTALIN Input Clock, WCLK Output

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{XS}	Crystal startup		1	2	msec	
t_{XP}	XTALIN freq @ TTL levels			20	MHz	40/60% Duty Cycle
t_{WCD}	WCLK duty cycle	45		55	%	*

* WCLK duty cycle is specified for the high phase, at any voltage between 0.8-2.0 V. This guarantees the worst case duty cycle seen at the input of a receiver, whose input threshold is specified to be within this voltage range. See the Output Driver section of the DC Electrical Characteristics above for load limitations.

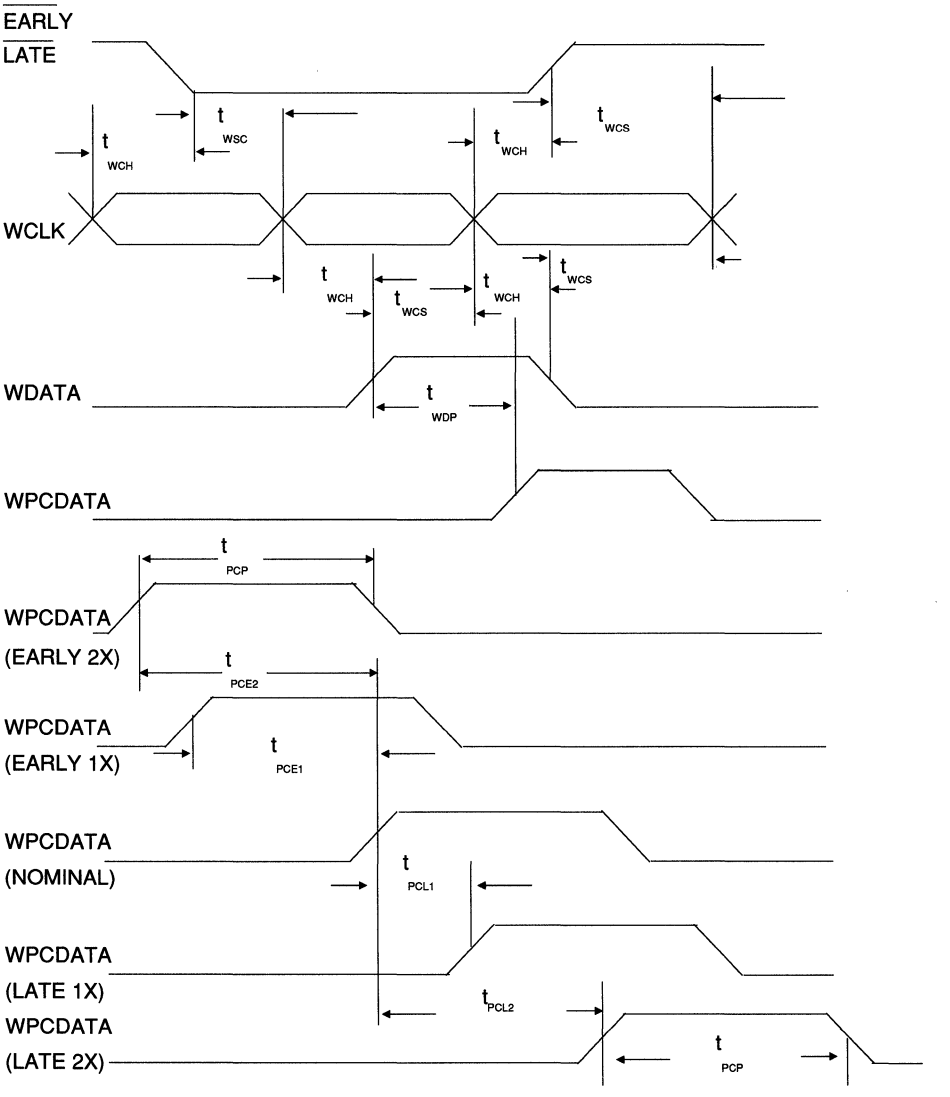


FIGURE 11. WRITE DATA CONDITIONER TIMINGS

7.9 Delay Line

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{DRC}	Delay-Locked Loop Time Constant		.4	1.5	msec	*

* This is the time required for the DDL to acquire the XTALIN frequency. It should be used in conjunction with t_{XS} to determine the time from power up to device ready.

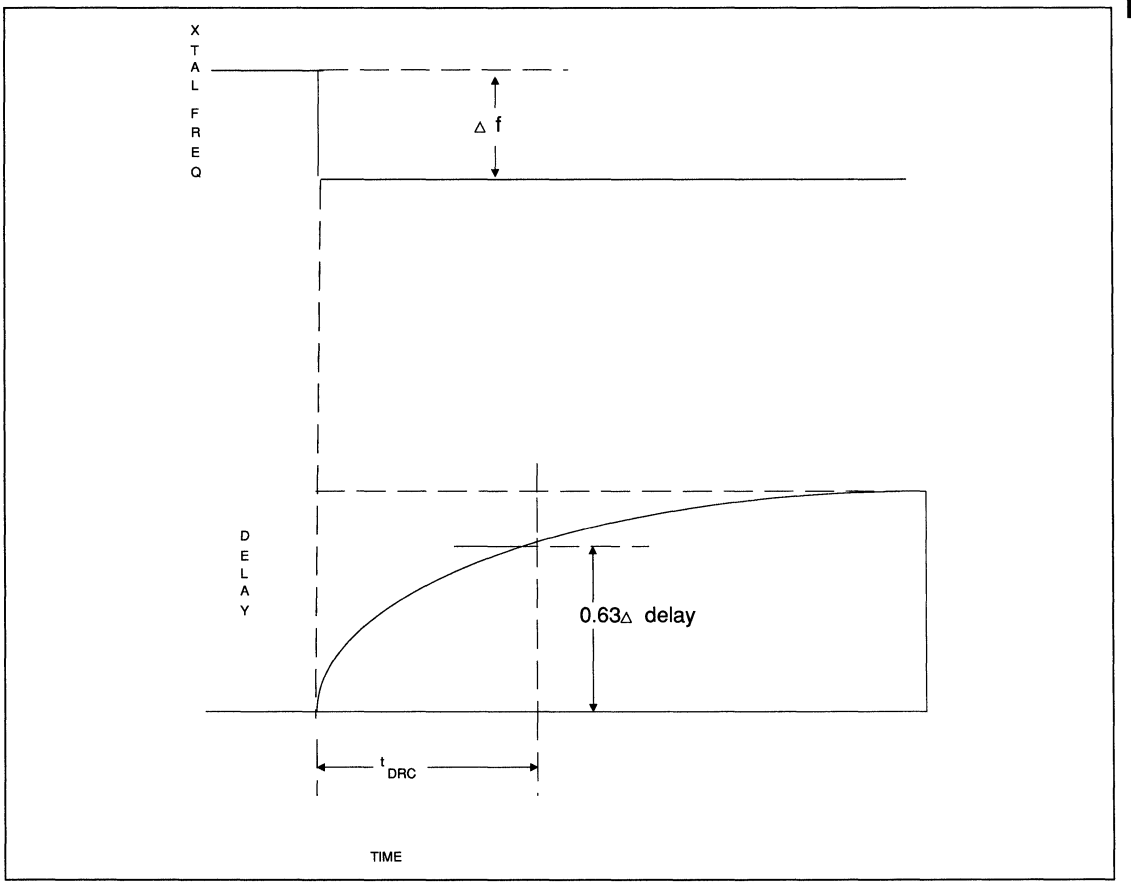
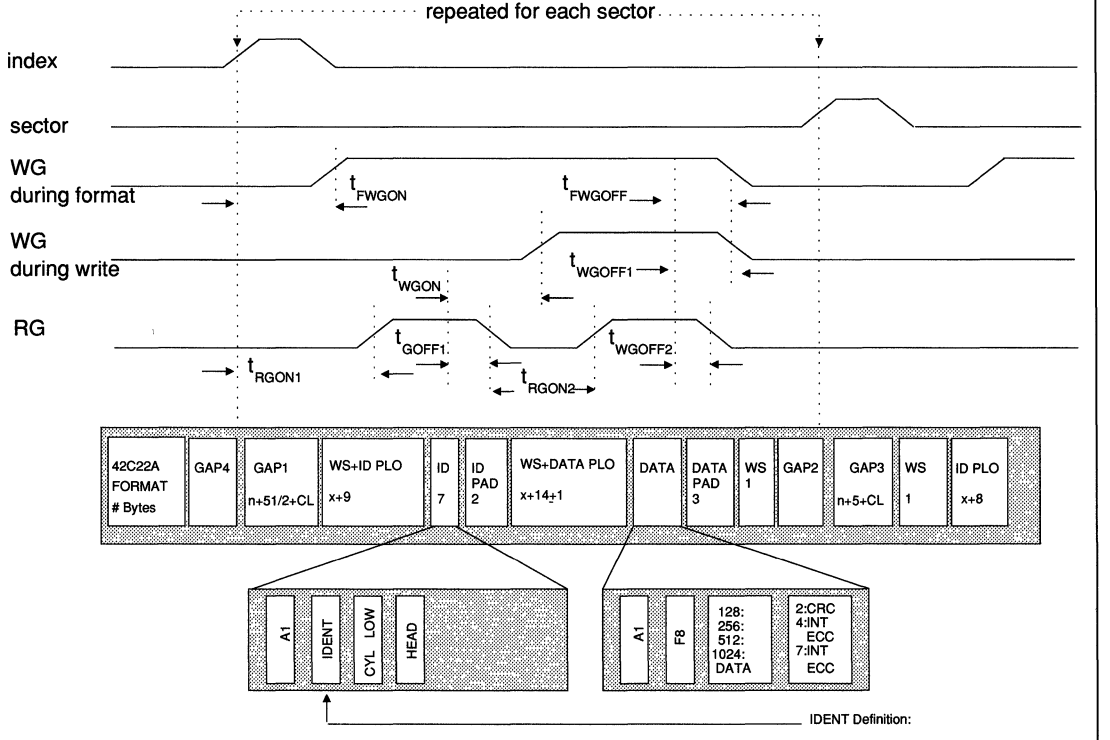


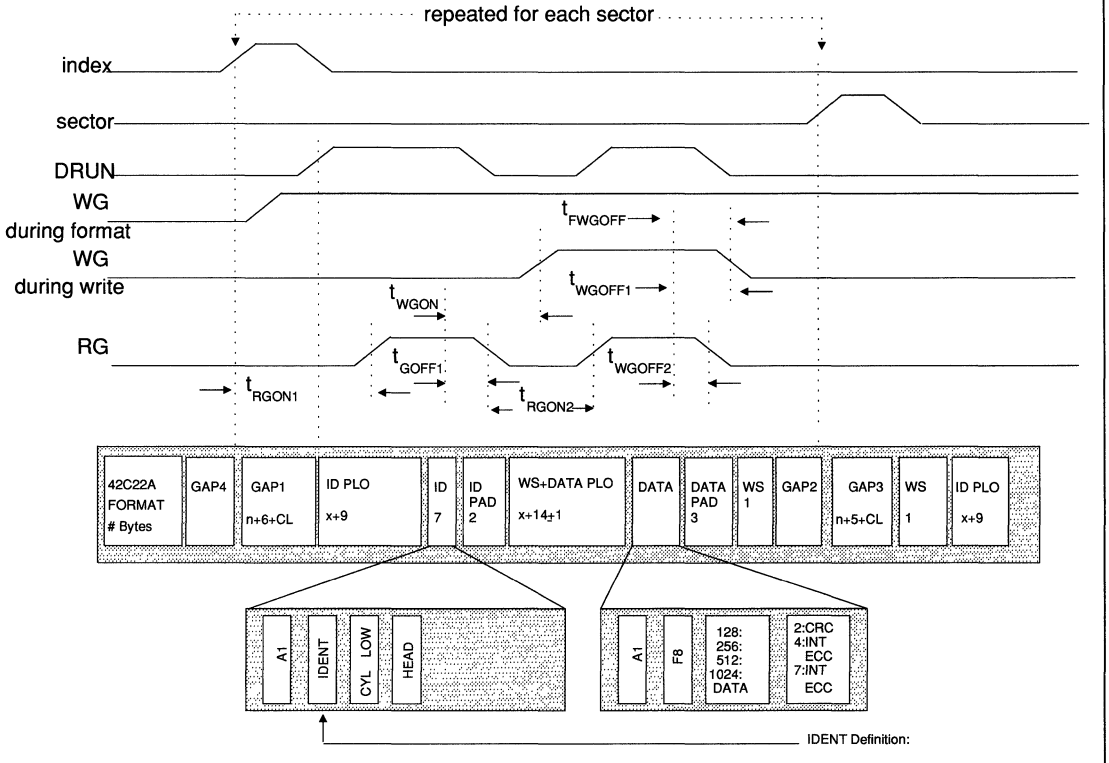
FIGURE 12. DELAY LINE TIMING



NOTES:

1. n=contents of Sector Number Register during Format command.
2. CL=controller latency. 0≤CL≤1 byte times.
3. x=contents of PLO register. ID PLO Length is programmable during Format command. DATA PLO Length is programmable during Write command. Data PLO Length is 11 during Format. Data PLO Length is 12±1 during write if x=0.
4. t_{WGON}=17±1 bit times with respect to RD in.
5. t_{WGOFF1}=28 bit times with respect to WD out.
6. t_{RGOFF1}=9±1 bit times with respect to RD in.
7. t_{RGOFF2}=9±1 bit times with respect to RD in.
8. t_{RGON1}=z+CL byte times with respect to INDEX/SECTOR (SCT). Sector is tied to DRUNSCT always. z=contents of internal GAP register.
9. t_{RGON2}=35±1 bit times with respect to RD in.
10. GAP2= speed tolerance + comined ENDEC delays + other GAP requirements (i.e. SERVO) GAP2 Length= (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad)
11. t_{FWGON}=n+51/2+CL byte times with respect to INDEX/SECTOR. n=contents of Sector Number Register during Format. t_{WGOFF}=20 bit times with respect to WD out.

FIGURE 13. HARD SECTOR FORMAT w/WG PULSE OPTION



NOTES:

1. n=contents of Sector Number Register during Format command.
2. CL=controller latency. 0≤CL≤1 byte times.
3. x=contents of PLO register. ID PLO Length is programmable during Format command.
   DATA PLO Length is programmable during Write command. Data PLO Length is 11 during Format. Data PLO Length is 12±1 during write if x=0.
4. t_{WGON}=17±1 bit times with respect to RD in.
5. t_{WGOFF1}=28 bit times with respect to WD out.
6. t_{RGOFF1}=9±1 bit times with respect to RD in.
7. t_{RGOFF2}=9±1 bit times with respect to RD in.
8. t_{RGON1}=19±1 bit times with respect to DRUN. SECTOR is tied to DRUNSCT during Format and DRUN is tied to DRUNSCT during Read and Write.
9. t_{RGON2}=35±1 bit times with respect to RD in.
10. GAP2= speed tolerance + comined ENDEC delays + other GAP requirements (i.e. SERVO)
    GAP2 Length= (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad)

FIGURE 14. HARD SECTOR FORMAT w/ SOFT SECTOR R/W

8.0 PRODUCT COMPATIBILITY

The following is a matrix of the features for each of the data separators from Western Digital's family of devices.

Market Number	**WD10C 20A**	**WD10C 21A**	**WD10C 20B**	**WD10C 22B**	**WD10C 23**
CMOS	3 µSM	3 µSM	3 µSM	3 µSM	1.25 µDM
min ext componts	15	15	14	14	3
ext delay line	√	√			
int delay line			√	√	√
ext VCO	√	√	√	√	
int VCO					√
MFM encoding	√		√	√	√
RLL encoding		√		√	√
5 Mbit	√	√	√	√	√
7.5 Mbit		√		√	√
10 Mbit				√	√
15 Mbit					√
var frequency					√
soft sector	√	√	√	√	√
hard sector					√
write precomp	ext dly	ext dly	± 12.5 %	± 12.5 %	*
window shift	ext dly	ext dly	± 12.5 %	± 12.5 %	**
adapt win centering					√

TABLE 4. PRODUCT COMPATIBILITY FOR DATA SEPARATORS

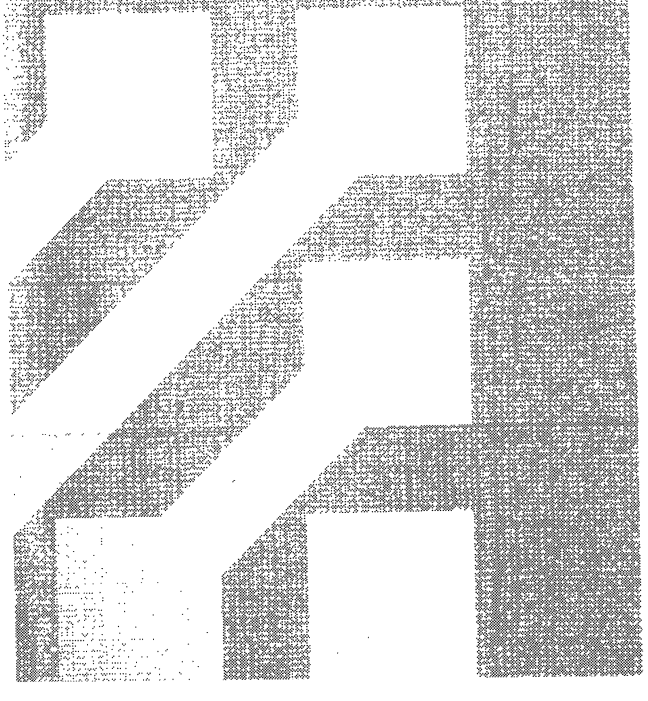
* ± 12.5 % / ± 6.25 %

** ± WIN / 2

WD33C92A

Enhanced SCSI Bus

Interface Controller



WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

The 33C92A is a MOS/VLSI device which is implemented in Western Digital's CMOS process. It operates from a single 5 volt supply and is available in either a 44-pin chip carrier or a 48-pin dual-in-line package. All inputs and outputs are TTL-compatible.

1.1 Features

- Implements full SCSI bus features: arbitration, disconnect, reconnect, parity generation/checking on both data ports, soft reset, and synchronous data transfers.
- Synchronous offset selectable from 1 to 12 bytes, with selectable transfer period up to 5 Mbytes/s. ANSI spec compatibility guaranteed to 4 Mbytes/s.
- Compatible with most microprocessors through an 8-bit data bus; supports both multiplexed and non-multiplexed address/data bus systems. Host bus data parity checking and generation is an optional feature.
- Can be used as host adapter (SCSI Initiator) or peripheral adapter (SCSI Target).
- Data transfer options include programmed I/O, single-byte DMA, burst (multibyte) DMA, or direct bus access (WD bus) transfers.
- Burst data transfers up to 4096 bytes.
- Programmable timeout for selection and reselection.
- "Combination" commands greatly reduce interrupt-handling responsibilities.
- Special "Translate Address" command performs the Logical-to-Physical address translation.
- Single +5V supply.
- Available in 44-pin chip carrier or 48-pin DIP.
- Low-power CMOS design.
- Compatible with single-ended or differential external drivers.

2.0 DESCRIPTION

The 33C92A is intended for use in systems which interface to the SCSI (Small Computer System Interface) Bus. The 33C92A can operate in both the initiator (typically, a host computer system) and the target (typically, a peripheral device) SCSI bus roles.

When used in the host system, the 33C92A interfaces to both the host bus and the SCSI bus. To perform a SCSI operation, the host processor must issue a command to the 33C92A to select the desired Target. The 33C92A then arbitrates for the SCSI bus and selects the peripheral unit. If it fails to get the bus because of a device with higher priority, it continues trying, notifying the host when it has succeeded by generating an interrupt. At this point, the 33C92A is operating in the initiator role. When the peripheral requests a SCSI command from the host, the 33C92A receives the request and generates another interrupt to the host. The host responds to this interrupt by issuing a "Transfer Info" command and supplying SCSI command bytes to the 33C92A. The 33C92A transfers the SCSI command to the peripheral, and then waits for the next bus phase request. This process continues until all SCSI information including data, status, and messages have been transferred.

The 33C92A also offers high-level Select-and-Transfer commands, eliminating the interrupt handling otherwise required between each SCSI bus phase.

When the 33C92A is used in a peripheral system, it interfaces with a local processor and the SCSI bus just as it does when used as a host adapter. In this environment, the 33C92A will operate primarily in a Target role. The Target-role command set enables the 33C92A to request each SCSI bus phase individually or to sequence the SCSI bus phases automatically through the use of combination commands.

The 33C92A has an internal microcontroller, a register task file, and SCSI interface logic. This architecture supports both tight control of the protocol for non-standard SCSI implementations, as well as a hands-free mode for standard SCSI applications.

3.0 33C92A PINOUT

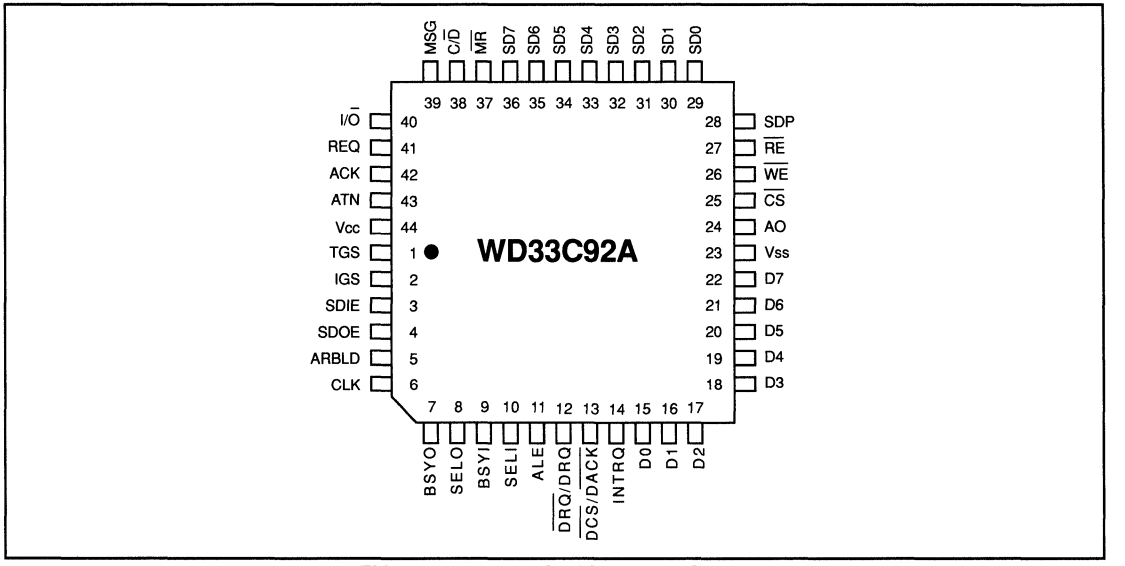


FIGURE 1. 44-PIN QUAD PIN DIAGRAM

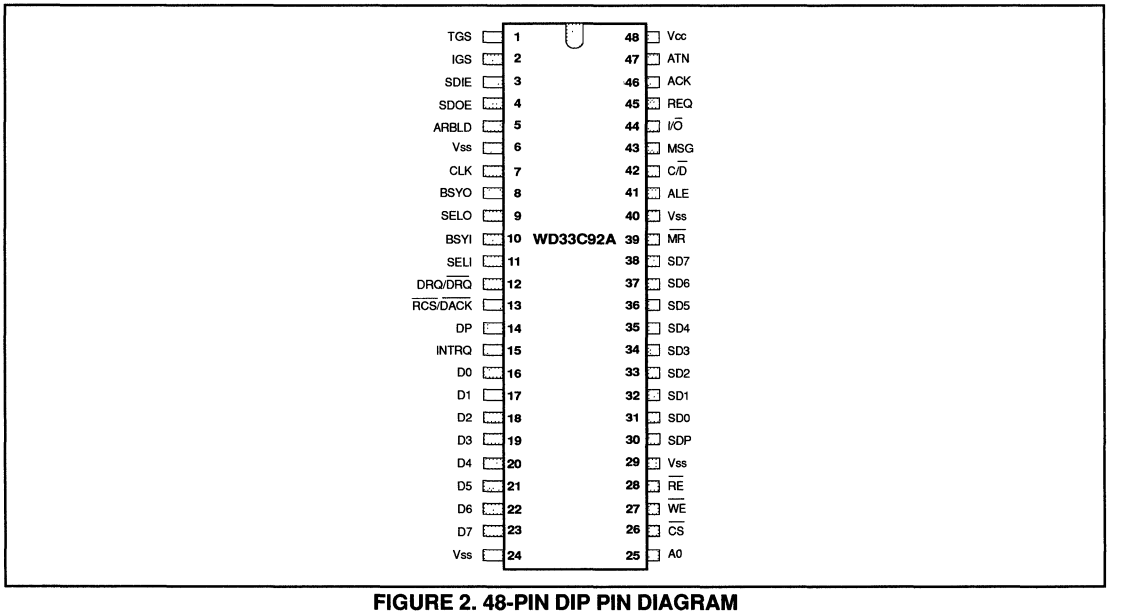


FIGURE 2. 48-PIN DIP PIN DIAGRAM

4.0 PIN DESCRIPTIONS

4.1 Processor/DMA Interface

NAME	I/O	FUNCTION
CLK	I	8-20 MHz square wave clock.
MR-	I	Reset is an active-low input which forces the 33C92A into an idle state. All SCSI outputs are tristated.
INTRQ	O	Interrupt Request to external microprocessor. Indicates command completion/termination or a need to service the SCSI interface. This bit is reset when the SCSI STATUS register is read.
RE-	I/O	Read enable is an active-low input which is used with CS- to read a register. In WD Bus mode, it is used as an output to read data from a sector buffer. Also used for DMA transfers. (TRI-STATE)
WE-	I/O	Write enable is an active-low input which is used with CS- to write a register. In WD Bus mode, it is used as an output to write data to a sector buffer. Also used for DMA transfers. (TRI-STATE)
CS-	I	Chip Select is an active-low input which qualifies RE- and WE- when accessing a register. This signal must be inactive during a DMA cycle (DACK- active in DMA/burst mode or DRQ active in WD Bus mode).
A0	I	Address pin used to access the internal registers for non-multiplexed address/data busses (i.e. the ALE pin is grounded). The address of the desired register is loaded into the ADDRESS register during a write cycle with A0=0. The selected register is then accessed when A0=1.
ALE	I	Address Latch Enable is used for multiplexed address/data busses to load the address of the desired 33C92A register from the data bus. If indirect addressing is to be used, the ALE pin should be grounded. See the description of the ADDRESS register for a complete discussion of direct and indirect addressing.
DACK- (RCS-)	I/O	DMA acknowledge input used for interfacing to an external DMA controller (e.g. 8237). When DACK- is low, all bus transfers are to/from the DATA register regardless of the contents of the ADDRESS register. In WD Bus mode, this pin functions as a RAM chip select output to allow the 33C92A to access a sector buffer. RE- and WE- are outputs when RCS- is active. Since this pin can be an open drain output, a pullup resistor may be required when operating in WD Bus mode.
DRQ-	I/O	Data request is an output when interfacing to (DRQ) an external DMA controller and an input when in WD Bus mode. When used with an external DMA controller, DRQ- and DACK- form the handshake for the data-byte transfers. In Burst mode, DRQ- remains low as long as there is data to transfer. In WD Bus mode, the 33C92A performs burst transfers while DRQ is high, and when DRQ is low, data transfers are inhibited, RCS- is false, and the RE- and WE- outputs are disabled. Since this pin can be an open drain output, a pullup resistor may be required when operating in DMA or Burst mode.
D7-D0	I/O	Processor data bus.
DP	I/O	Data Parity, used only for checking/generating parity during data transfers.

4.2 SCSI Interface

NAME	I/O	FUNCTION
ATN	I/O	ATN is an output in the initiator role and an input in the target role. It is used to indicate the ATTENTION condition.
REQ	I/O	REQ is an input in the initiator role and an output in the target role. It indicates a request for a REQ/ACK data transfer.
ACK	I//O	ACK is an output in the initiator role and an input in the target role. It indicates an acknowledgement for a REQ/ACK data transfer handshake.
MSG	I/O	MSG is an input in the initiator role and an output in the target role. It is asserted during a MESSAGE phase.
C/D-	I/O	C/D- is an input in the initiator role and an output in the target role. It is used to indicate whether CONTROL or DATA information is on the SCSI data bus.
I/O-	I/O	I/O- is an input in the initiator role and an output in the target role. It controls the direction of data movement on the SCSI data bus with respect to an Initiator.
SD7 | SD0	I/O	SCSI data bus.
SDP	I/O	SCSI data bus parity signal.
BSYI	I	BSYI signals the 33C92A that SCSI BSY- is asserted.
BSYO	O	The 33C92A asserts BSYO to assert the SCSI BSY- signal.
SELI	I	SELI signals the 33C92A that SCSI SEL- is asserted.
SELO	O	The 33C92A asserts SELO to assert the SCSI SEL-signal.
SDIE	O	Enables SCSI data bus receivers.
SDOE	O	Enables SCSI data bus drivers.
ARBLD	O	Latches the decoded port number into an external register just prior to the SCSI bus arbitration process.
IGS	O	The 33C92A asserts IGS when operating as an Initiator. IGS enables the SCSI drivers for ATN and ACK.
TGS	O	The 33C92A asserts TGS when operating as a Target.TGS enables the SCSI drivers for REQ, MSG, C/D- and I/O-.

5.0 33C92A BLOCK DIAGRAM

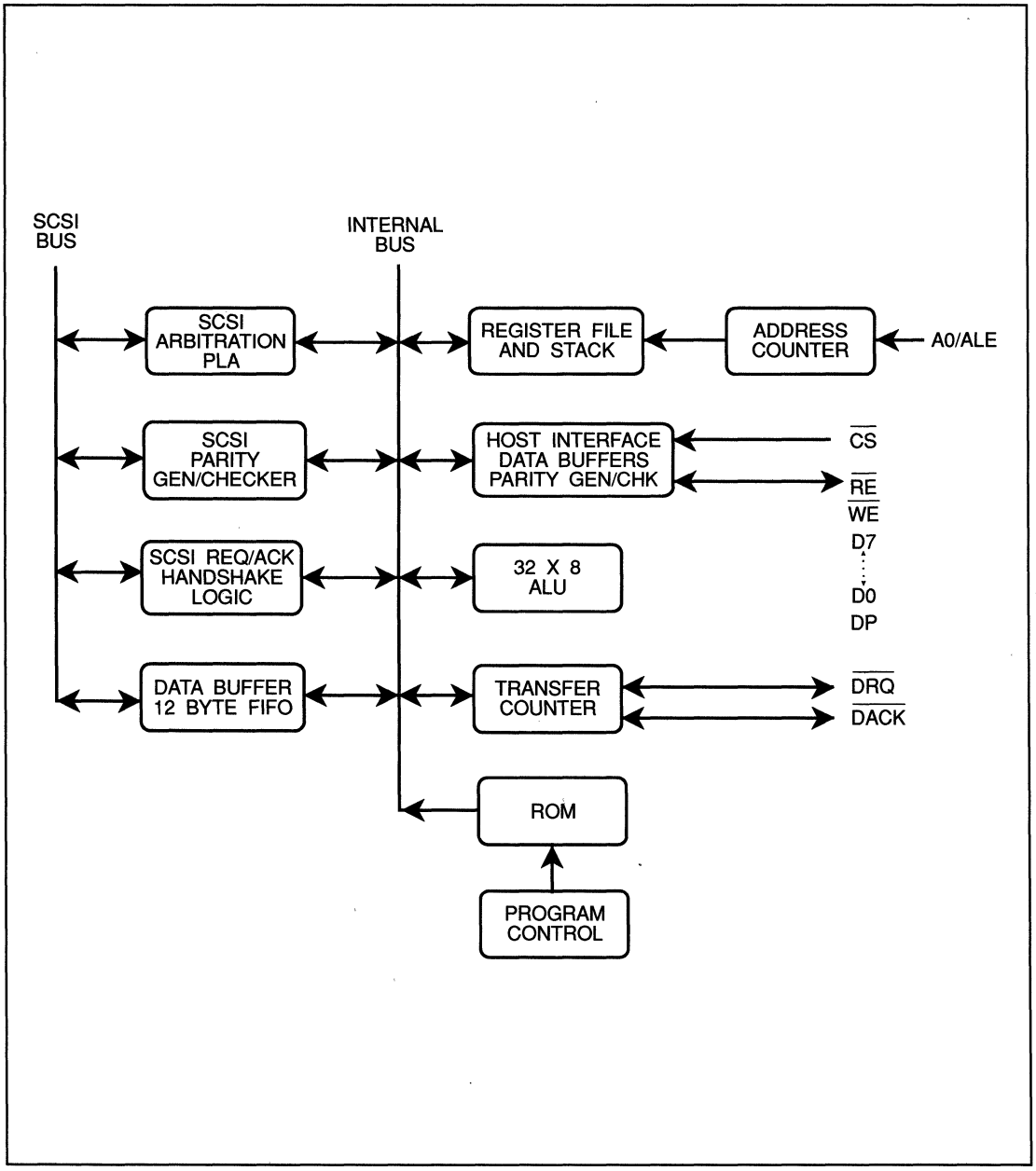


FIGURE 3. 33C92A BLOCK DIAGRAM

6.0 33C92A REGISTERS

6.1 Register Map

A0	R/W	REGISTER ACCESSED	ADDRESS (HEX)
0	R	AUXILIARY STATUS REGISTER	XX
0	W	ADDRESS REGISTER	XX
1	R/W	OWN ID REGISTER /CDB SIZE 00	00
1	R/W	CONTROL REGISTER	01
1	R/W	TIMEOUT PERIOD REGISTER	02
1	R/W	TOTAL SECTORS REGISTER /CDB 1ST	03
1	R/W	TOTAL HEADS REGISTER /CDB 2ND	04
1	R/W	TOTAL CYLINDERS REGISTER(MSB)/CDB 3RD	05
1	R/W	TOTAL CYLINDERS REGISTER(LSB)/CDB 4TH	06
1	R/W	LOGICAL ADDRESS(MSB) /CDB 5TH	07
1	R/W	LOGICAL ADDRESS(2ND) /CDB 6TH	08
1	R/W	LOGICAL ADDRESS(3RD) /CDB 7TH	09
1	R/W	LOGICAL ADDRESS(LSB) /CDB 8TH	0A
1	R/W	SECTOR NUMBER REGISTER /CDB 9TH	0B
1	R/W	HEAD NUMBER REGISTER /CDB 10TH	0C
1	R/W	CYLINDER NUMBER(MSB) REGISTER/CDB 11TH	0D
1	R/W	CYLINDER NUMBER(LSB) REGISTER/CDB 12TH	0E
1	R/W	TARGET LUN REGISTER	0F
1	R/W	COMMAND PHASE REGISTER	10
1	R/W	SYNCHRONOUS TRANSFER REGISTER	11
1	R/W	TRANSFER COUNT REGISTER (MSB)	12
1	R/W	TRANSFER COUNT REGISTER (2ND BYTE)	13
1	R/W	TRANSFER COUNT REGISTER (LSB)	14
1	R/W	DESTINATION ID REGISTER	15
1	R/W	SOURCE ID REGISTER	16
1	R	SCSI STATUS REGISTER	17
1	R/W	COMMAND REGISTER	18
1	R/W	DATA REGISTER	19

NOTES:

1. All unused bits of a defined register are reserved and must be zero.

2. Reading an undefined or unavailable register results in an all-ones data bus output.

3. Register addresses are determined by the ADDRESS register bits AR7 through AR0.

4. When using a multiplexed address/data bus with ALE, the A0 pin is ignored and the ADDRESS register is loaded with ALE. In this mode, the AUXILIARY STATUS register is mapped at hex 1F.

5. See section 6.3 for a description of how reset affects the internal registers.

6.2 Register Descriptions

6.2.1 Auxiliary Status Register

The AUXILIARY STATUS register is a read-only register which contains general status information not directly associated with the interrupt condition. The AUXILIARY STATUS register may be accessed at any time, except during DMA accesses (DACK- asserted in DMA/Burst mode or DRQ asserted in WD bus mode).

7	6	5	4	3	2	1	0
INT	LCI	BSY	CIP	0	0	PE	DBR

Bit 0 DBR-DATA BUFFER READY

DATA BUFFER READY is used during programmed I/O to indicate to the processor whether or not the DATA register is available for reading or writing. During Send or Transfer commands which transmit data over the SCSI bus, the DBR bit is set when the 33C92A is ready to take a byte from the host; the bit is reset when the processor writes the byte to the DATA register. During Receive or Transfer commands which receive data over the SCSI bus, the DBR is set when a byte is received; it is reset when the processor reads the byte from the DATA register.

Bit 1 PE-PARITY ERROR

PARITY ERROR status indicates that even parity was detected on a data byte received during an information transfer. Parity is checked on data received from the host bus during transfers out to the SCSI bus and is checked on data received from the SCSI bus during transfers out to the host bus.

Detection of a parity error will set the PE status bit regardless of the state of the HHP or HSP bits in the CONTROL register. The PE bit is cleared when a new command is issued.

Bit 2,3 Not Used

Not used bits are zero.

Bit 4 CIP-COMMAND IN PROGRESS

COMMAND IN PROGRESS, when set, indicates that the 33C92A is interpreting the last command entered into the COMMAND register and therefore this register is unavailable. When this bit is reset, a command may be written to the COMMAND register.

Bit 5 BSY-BUSY

BUSY indicates that a Level II command is currently executing and therefore only the COMMAND register (when CIP = 0), the DATA register, and the AUXILIARY STATUS register are accessible by the host. A Level II command may not be written to the COMMAND register when this bit is one.

Bit 6 LCI-LAST COMMAND IGNORED

LAST COMMAND IGNORED indicates that a command was issued by the host just prior to or concurrent with a pending interrupt, and therefore the command will be ignored.

Bit 7 INT-INTERRUPT PENDING

INTERRUPT PENDING indicates that the INTRQ pin is asserted. The host should read the SCSI STATUS register to clear INTRQ prior to issuing any commands.

6.2.2 Address Register

The ADDRESS register is a write-only register which contains the address of the register to be accessed. Registers in the 33C92A may be accessed in one of two ways:

- Direct addressing (multiplexed address/data busses). In direct addressing, the falling edge of the ALE signal is used to latch the address into the ADDRESS register. The A0 pin should be connected to ground when using this method. The ALE is typically then followed by the CS- and WE- or RE- signals that access the selected register. Also, in direct addressing, the AUXILIARY STATUS register is located at address 1F hex.
- Indirect addressing (separate address/data busses). In indirect addressing, the register

access is performed in two separate cycles. This method is enabled by attaching ALE to ground. First, the ADDRESS register is loaded by performing a write of the desired address to the 33C92A (WE- and CS- asserted) with A0=0. Then the register is accessed by asserting CS- and WE- or RE-, with A0=1. Also, following every access with A0=1, the ADDRESS register will automatically increment to point at the next register, with the exception of the following locations: AUXILIARY STATUS register, DATA register, and the COMMAND register. In indirect addressing, the AUXILIARY STATUS register is accessed by performing a read (CS- and RE- asserted) with A0=0.

6.2.3 Own ID/CDB Size Register

The OWN ID/CDB SIZE register, in its first mode, contains both the encoded ID of the 33C92A on the SCSI bus and several control bits that are used to initially configure the device during the "Reset" command. These bits control 'advanced feature' selection, host bus parity enable, and selection of the divisor for the input clock. In its second mode (when advanced features are enabled, see 7.3), this register is used during the combination commands to specify the SCSI CDB size if the command group is unknown to the 33C92A.

In the first mode, this register (as defined below) is sampled and becomes effective only after a "Reset" command is issued to the device. This register must be initialized, and a "Reset" command must then be issued, following a hardware reset to set the SCSI bus ID, the clock divisor, and the operating modes before any other commands are issued.

In the second mode, bits 3-0 of this register are used during the Select-and-Transfer and Wait-for-Select commands to specify the SCSI Command Descriptor Block size if it is not a group 0, group 1, or group 5 command. This mode is enabled only when advanced features are enabled (see 7.3).

7	6	5	4	3	2	1	0
FS1	FS0	0	EHP	EAF	ID2	ID1	ID0

Bit 0-2 IDn-SCSI ID Bits 0-2

SCSI ID Bits 0-2 set the SCSI bus ID number that the 33C92A will use during arbitration and selection.

Bit 3 EAF-ENABLE ADVANCED FEATURES

ENABLE ADVANCED FEATURES, when set to one, causes the 33C92A to enable certain advanced features (see section 7.3). When this bit is zero, those features are disabled.

Bit 4 EHP-ENABLE HOST PARITY

ENABLE HOST PARITY, when set to one, enables odd parity checking on the host bus; the PE bit in the AUXILIARY STATUS register will indicate parity errors detected on the host bus, and the HHP bit in the CONTROL register will be used. When this bit is zero, no checking is performed on the host bus; the PE bit is not set when a parity error is detected on the host bus, and the HHP bit must be set to zero. NOTE: Parity is always generated on the host data parity bit (DP), regardless of the state of this bit.

Bit 5 Not Used

Not used bits are zero.

Bit 6-7 FSn-FREQUENCY SELECT 0-1

FREQUENCY SELECT 0-1 select the divisor that is applied to the input clock. The resulting clock is used for data transfer timing and for SCSI bus arbitration timing. The table below shows input clock frequency ranges and the corresponding divisors. The correct divisor for the input clock must be used, or SCSI bus timing specifications may not be met.

INPUT CLOCK FREQUENCY (MHZ)	FS1	FS0	RESULTING DIVISOR
8-10	0	0	2
12-15	0	1	3
16-20	1	0	4
xx	1	1	undefined

Note that an 11 MHZ clock rate should not be used, as the resulting SCSI bus clear delay may violate SCSI specifications. The formula for computing the maximum SCSI data transfer rate is:

MAXIMUM SCSI TRANSFER RATE =
INPUT CLOCK FREQUENCY/CLOCK DIVISOR[MByte/sec]

6.2.4 Control Register

The CONTROL register is used to enable/disable certain functions, such as response to parity errors and the SCSI attention condition, interrupt handling, and data transfer modes.

7	6	5	4	3	2	1	0
DM2	DM1	DM0	HHP	EDI	IDI	HA	HSP

Bit 0 HSP-HALT on SCSI PARITY ERROR

The HALT on SCSI PARITY ERROR bit enables the 33C92A to immediately terminate a Receive or Transfer command if a parity error is detected on an incoming SCSI data byte. In the Initiator role, termination due to a SCSI parity error causes the ACK pin to be left in the active state in order to inhibit any additional data transfers (REQs) by the Target; this facilitates error handling with the Target. Synchronous data transfers check parity every 4096 bytes, or at the end of the remaining transfer count, whichever is less. Asynchronous transfers check parity on every byte.

Bit 1 HA-HALT on ATTENTION

The HALT on ATTENTION bit (in Target mode only) enables the 33C92A to terminate a Send or Receive command if the ATN input is asserted. This normally indicates that the Initiator detected a parity error while receiving data from the 33C92A. The ATN input is tested before the start of a data transfer, every 4096 bytes if the transfer count is greater than 4096, and after the end of the transfer. These rules apply to bothsynchronous and asynchronous transfers.

Bit 2 IDI-INTERMEDIATE DISCONNECT INTERRUPT

The INTERMEDIATE DISCONNECT INTERRUPT bit, when set, enables the 33C92A to generate an 85H interrupt and complete a Select-and-Transfer command if the Target disconnects according to the defined SCSI protocol. When this bit is reset, no interrupt is generated by a valid disconnect. This feature, when used with the Resume SAT command, provides support for overlapped SCSI operations. IDI is also used to select execution options in Target mode Combination commands that serve to reduce host system overhead. Refer to Section 7 for more details.

Bit 3 EDI-ENDING DISCONNECT INTERRUPT

When the ENDING DISCONNECT INTERRUPT bit is set, the 16H interrupt which normally follows the COMMAND COMPLETE message during the execution of a Select-and-Transfer command will be suppressed until the Target disconnects from the SCSI bus. EDI is also used in the Target mode Combination commands to enable chaining between those commands, resulting in reduced host system overhead. Refer to Section 7 for more details.

Bit 4 HHP-HALT on HOST PARITY ERROR

The HALT on HOST PARITY ERROR bit enables the 33C92A to immediately terminate a Send or Transfer command if a parity error is detected on an incoming host data byte. Host parity errors are checked according to the rules for checking SCSI parity errors. However, a halt on a host parity error will not hold the ACK signal asserted when an error occurs. Host parity checking is performed at the same intervals as SCSI parity checking.

Bit 5-7 DMx-DMA MODE SELECT

DMA MODE SELECT bits 2-0 are used to select the DMA mode of operation, which describes the host bus transfer mode used during Data In or Data Out phases. The following table describes the different DMA modes, and the state of these bits to select them:

6.2.4.1 DMA Mode Selected

DM2	DM1	DM0	DMA MODE SELECTED
0	0	0	POLLED MODE, or no DMA enabled. All data phase transfers are performed by polling for DBR in the AUXILIARY STATUS register, and then writing (reading) the data to (from) the DATA register.
0	0	1	BURST MODE selects a demand-mode DMA interface. In this mode, the DRQ- signal will be active as long as there is data/space in the internal FIFO to allow the transfer to continue. The DMA controller responds by asserting DACK- and RE-/WE- as long as DRQ- is active.
0	1	0	WD-BUS MODE is selected when the 33C92A is connected to a WD Bus. This mode also can be called Direct Buffer Access (DBA) mode. In this mode, the 33C92A acts as a bus master, and all data access signals reverse their direction: The DRQ- output signal becomes the DRQ input, which enables the 33C92A to drive the buffer bus control signals. The DACK- output signal becomes the RCS- input, which is asserted as a chip select for the buffer. The RE- and WE- inputs become outputs which drive the read and write functions of the RAM buffer. As long as the DRQ signal is asserted, transfers will continue in a burst manner, until the transfer is complete or the decides to pause the transfer by negating the DRQ signal; one more transfer may occur after this transition, and then the DACK-, RE-, and WE- signals are negated.
1	0	0	DMA MODE is selected when the 33C92A is to be used with a DMA controller in single-byte transfer mode. In this mode, DRQ- is asserted and then negated, and the DMA controller responds by asserting DACK- and WE- or RE-, for each data byte transferred to/from the 33C92A.

28

6.2.5 Timeout Period Register

The TIMEOUT PERIOD register is an 8-bit register containinga preset value which determines the timeout period for Select and Reselect commands. This value may be calculated as a function of the input clock frequency and the desired timeout period, as shown in the following equation:

register value = Tper * Ficlk/80

Where:

Tper = the desired timeout period in milliseconds

Ficlk = the input clock frequency at the MCK pin in Megahertz (with no divisor applied).

The constant '80' scales the units of the equation, as is based on the internal timeout cycle time. The user should round the resulting 'register value' up to the next integral value to ensure that the user's minimum timeout requirement is met.

The timeout period specifies how long the 33C92A will wait for a response (indicated by assertion of the BSY- signal) after it has begun the selection phase (assert SEL- and negate BSY-) before terminating the command. The timeout function can be disabled by loading the TIMEOUT PERIOD register with zero.

The following twelve registers are used exclusively by the Translate Address and/or "combination" commands. The function of each register is determined by the type of command issued.

6.2.6 Total Sectors Register/CDB 1st Byte

Translate Address:
The TOTAL SECTORS register should be set to the total number of sectors per track prior to issuing a Translate Address command.

Select-and-Transfer:
This register should be loaded with the first byte of the COMMAND DESCRIPTOR BLOCK before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the first byte of the received CDB in this register.

6.2.7 Total Heads Register/CDB 2nd Byte

Translate Address:
This register holds the total number of heads during a Translate Address command.

Select-and-Transfer:
This register should be loaded with the second byte of the CDB before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the second byte of the received CDB in this register.

6.2.8 Total Cylinders Register/CDB 3rd and 4th Bytes

Translate Address:
This is a 16-bit register which holds the total number of cylinders.

Select-and-Transfer:
This register should be loaded with the third and fourth bytes of the CDB before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the third and fourth bytes of the received CDB in this register.

6.2.9 Logical Address Register/CDB 5th-8th Bytes

Translate Address:
The LOGICAL ADDRESS register is a 32-bit register which should be loaded with the logical address to be translated prior to issuing the Translate Address command.

Select-and-Transfer:
For six byte CDBs, only the first two bytes of this register are loaded with the fifth and sixth bytes of the CDB. For ten and twelve byte CDBs, this register is loaded with the fifth, sixth, seventh, and eighth bytes of the CDB.

Wait-for-Select-and-Receive:
The 33C92A will store the fifth, sixth, seventh (if any), and eighth (if any) bytes of the received CDB in this register.

6.2.10 Sector Number Register/CDB 9th Byte

Translate Address:
This register will contain the resulting sector number following a Translate Address command.

Select-and-Transfer:
This register should be loaded with the ninth byte of a ten or twelve byte CDB before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the ninth byte of a ten or twelve byte received CDB in this register.

6.2.11 Head Number Register/CDB 10th Byte

Translate Address:
The HEAD NUMBER register contains the resulting head number following a Translate Address command. If automatic compensation for spare sectors on a disk is to be performed by the WD33C92A, then the number of spare sectors per cylinder must be written into this register before issuing the Translate Address

command. It should be noted that when compensation is used, the maximum number of cylinders allowed is 4096, and the maximum number of heads is 15. An initial value of zero in this register indicates that no compensation is to be performed.

Select-and-Transfer:
This register should be loaded with the tenth byte of a ten or twelve byte CDB before issuing a Select- and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the tenth byte of a ten or twelve byte received CDB in this register.

6.2.12 Cylinder Number Register/CDB 11th and 12th Bytes

Translate Address:
The CYLINDER NUMBER register is a 16-bit register which contains the resulting cylinder number following execution of the Translate Address command. When a Translate Address command involving automatic compensation for spare sectors is issued (i.e. the HEAD NUMBER register initially contains a nonzero value), then this register must be loaded with total number of sectors per cylinder (total sectors/track * total heads - total spare sectors/cyl) before issuing the command.

Select-and-Transfer:
This register should be loaded with the eleventh and twelfth bytes of a twelve byte CDB before issuing aSelect-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the eleventh and twelfth bytes of a twelve byte received CDB in this register.

Send-Status-and-Command-Complete:
The CDB11 register is used to specify the returned status byte to be sent during a Send-Status-and-Command-Complete command. The CDB12 register is used to determine the type of Command-Complete message sent by the 33C92A. If bit 0 of the CDB12 register is set to one, then a linked Command Complete message will be sent during command execution. In this case, bit 1 of the CDB12 register is used as a FLAG bit to determine whether a 0A hex (FLAG=0) or a 0B hex (FLAG=1) Linked Command Complete message is sent. If bit 0 is zero, then a simple Command Complete message (00 hex) is sent.

6.2.13 Target Lun Register

The TARGET LUN register is used to hold both the Logical Unit Number (LUN) and Target status information during various 33C92A commands and sequences. During a Select-and-Transfer or Reselect-and-Transfer command, the contents of this register (along with the SOURCE ID register) are used to generate and check the IDENTIFY messages which are transferred across the SCSI bus. In addition, the TARGET LUN register is used to hold the Target Status byte received during a Select-and-Transfer command.

During Wait-for-Select-and-Receive commands, this register may hold the image of the Identify message received from the Initiator. If the TLV bit is zero, there was no Identify message received. If the TLV bit is one, then a valid Identify message was received. The DOK bit will then indicate whether of not the Initiator has enabled disconnects.

During Reselect-and-Transfer commands, this register is used to set the LUN to be used in the Identify message sent to the Initiator after Selection phase. The TLV and DOK bits are not used.

In advanced mode, during Select-and-Transfer commands, this register is used to handle reselection by an unexpected Target. In this mode, this register will hold the logical unit number of the reselecting target. The TLV and DOK bits will be set to zero.

7	6	5	4	3	2	1	0
TLV	DOK	0	0	0	TL2	TL1	TL0

Bit 0-2 TLx-Target LUN

The Target Logical Unit Numbers bits 0-2.

Bit 3-5 Not Used

Not used bits are zero.

Bit 6 DOK-Disconnects OK

Disconnects permitted.

Bit 7 TLV-TARGET LUN Valid

TARGET LUN Valid.

6.2.14 Command Phase Register

The COMMAND PHASE register is used during combination commands to indicate which phases of these multi-phase commands have been completed. Thus, if the command has terminated abnormally, the processor can read this register to determine the cause of the termination and how to respond to it. This register is also used to resume combination commands by loading this register with a value that indicates the next desired or expected bus phase, and reissuing the command. Refer to the description of the specific commands for details regarding the various command phases and resume values.

7	6	5	4	3	2	1	0
0	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Bit 0-6 CPx-COMMAND PHASE bits0-6

Bit 7 Not Used.
Not used bits are zero.

6.2.15 Synchronous Transfer Register

The SYNCHRONOUS TRANSFER register is used to select between synchronous and asynchronous transfers, and is also used to define the maximum transfer rate. For information phases other than a "data" transfer phase, or when the selected offset is zero (OF3=OF2=OF1=OF0=0), asynchronous transfers will occur. Values greater than zero define a synchronous transfer mode and the offset is determined as shown below. This offset determines the effective FIFO depth for synchronous data transfers, and is typically determined by negotiation with the other SCSI device (as defined in the SCSI standard). The Transfer Period control bits select the minimum transfer period for both synchronous and asynchronous SCSI transfers and, if WD-Bus mode is used, the transfer period and the width of the RE-/WE- strobes for host transfers. The period is defined in terms of the internal clock cycle time; the frequency of this clock is determined by the divisor selected in the OWN ID register.

7	6	5	4	3	2	1	0
0	TP2	TP1	TP0	OF3	OF2	OF1	OF0

Bit 0-3 OFx-OFFSET bit 0-3

OFFSET bits 0-3 are used to select the desired offset according to the following:

3	2	1	0	SELECTED OFFSET
0	0	0	0	0(= Asynchronous data
0	0	0	1	1 phase transfers)
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	Undefined
1	1	1	x	Undefined

Bit 4-6 TPx-TRANSFER PERIOD bits 0-3

The TRANSFER PERIOD bits are used to select the desired transfer period according to the following table:

6	5	4	SCSI/Bus Transfer Period	(SCSI REQ/ACK* & Bus RE-/WE-
0	0	x	8 cycles	4 cycles
0	1	0	2 cycles	1 cycles
0	1	1	3 cycles	1 cycles
1	0	0	4 cycles	2 cycles
1	0	1	5 cycles	3 cycles
1	1	0	6 cycles	4 cycles
1	1	1	7 cycles	4 cycles

*synchronous pulse width & pulse width

The 'cycle' referred to above is the period of the internal data transfer clock after the divisor chosen in the OWN ID register is applied. This period is calculated by the following formula:

cycle = divisor (from OWN ID)(nsec) / 2 * input clock frequency (MHz)

Bit 7 Not Used.

Not used bits are zero.

6.2.16 Transfer Count Register

The TRANSFER COUNT register is a 24-bit register containing a preset value for the internal transfer counter. This preset value is loaded into the internal transfer counter when a Send, Receive, or Transfer command is issued. This counter is used to define command completion by decrementing as each data byte is transferred over the SCSI bus and causing a "successful completion" interrupt when the counter reaches zero. In Combination commands, this register specifies the number of bytes to be transferred during a Data phase.

The counter function can be disabled by loading the TRANSFER COUNT register with zeros prior to issuing a command or by setting the SINGLE-BYTE TRANSFER bit in the COMMAND register concurrent with issuing the command. If the counter is disabled, the Send, Receive, or Transfer command will be completed when a single byte has been transferred.

After the completion of any successful transfer, the TRANSFER COUNT register will be zero. This includes commands issued in Single Byte Transfer mode.

When a transfer is interrupted by a halt on error condition, a SCSI bus phase change, or an abort, the TRANSFER COUNT register will contain the number of bytes NOT successfully transferred to/from the SCSI bus, including clearing the internal FIFO of any bytes left in the FIFO (see DATA register). This FIFO clearing process may cause the TRANSFER COUNT register to differ with the user's DMA controller count, because some bytes may have been transferred into the FIFO, but not to the SCSI bus; therefore, the TRANSFER COUNT should be used to determine the actual number of bytes transferred to/from the SCSI bus.

6.2.17 Destination ID Register

The DESTINATION ID register contains the encoded SCSI bus ID of the device which is to be selected or reselected when a Reselect or Select command is issued. This register also contains control bits that affect the operation of certain combination commands.

7	6	5	4	3	2	1	0
SCC	DPD	0	0	0	DI2	DI1	DI0

Bit 0-2 DIx-DESTINATION ID bits 0-2

DESTINATION ID bits 0-2.

Bit 3-5 Not Used.

Not used bits are zero.

Bit 6 DPD-DATA PHASE DIRECTION,

DATA PHASE DIRECTION, when advanced features are enabled (see 7.3), is used to specify the expected direction of the SCSI data phase, when it occurs. This allows the 33C92A to verify the direction during Select-and-Transfer commands before beginning the transfer. When this bit is zero, the expected direction is out (to the Target). When this bit is one, the expected direction is in (from the Target). An unexpected information phase error will occur if the direction does not match the setting of this bit.

Bit 7 SCC-SELECT COMMAND CHAIN

SELECT COMMAND CHAIN is used only when the Reselect-and-Transfer command is issued with EDI=1. This bit selects which command is chained to when the data transfer is completed. When this bit is zero, a Send-Status-and-Command-Complete command begins executing. When this bit is one, a Send-Disconnect-Message command begins executing.

6.2.18 Source ID Register

The SOURCE ID register is used to report the SCSI bus ID of the device that has selected or reselected the 33C92A. It also contains bits that enable and control response to selection and reselection.

7	6	5	4	3	2	1	0
ER	ES	DSP	0	SIV	SIV	SIV	SIV

Bit 7 ER-ENABLE RESELECTION

ENABLE RESELECTION, when set to one, enables the 33C92A to respond to a

reselection by another device on the SCSI bus. When this bit is zero, any reselection is ignored.

Bit 6 ES-ENABLE SELECTION

ENABLE SELECTION, when set to one, enables the 33C92A to respond to a selection by another device on the SCSI bus. When this bit is zero, any selection is ignored.

Bit 5 DSP-DISABLE SELECT PARITY

DISABLE SELECT PARITY, when set to one, causes the 33C92A to ignore the bus parity when responding to selection or reselection. When this bit is zero, any selection or reselection with a parity error is ignored.

Bit 4 Not Used.

Not used bits are zero.

Bit 3 SIV-SOURCE ID VALID

SOURCE ID VALID is set to one after the 33C92A is selected or reselected if the other SCSI bus device asserted its own bus ID bit (in addition to the bus ID bit of the 33C92A) during the select/reselect phase. This bit is zero if only the bus ID bit of the 33C92A was asserted.

Bit 2-0 SIx-SOURCE ID Bits 2-0

SOURCE ID Bits 2-0 are valid only if the SIV bit is set to one. These bits indicate the SCSI bus ID of the device that selected or reselected the 33C92A.

6.2.19 SCSI Status Register

The SCSI STATUS register is a read-only register which indicates the cause of the most recent INTRQ assertion. INTRQ is asserted whenever a condition occurs within the 33C92A that requires intervention by the host; for example:

- the 33C92A has been reset;
- the command completed successfully;
- the bus phase changed;
- an error occurred.

Once INTRQ has been asserted, the contents of this register will not change until after the SCSI STATUS register has been read or until the 33C92A has been reset.

7	6	5	4	3	2	1	0
SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0

Bit 0-3 SSx-SCSI STATUS bits 0-3

SCSI STATUS bits 0-3 are status qualifiers whose meaning depends upon which upper (4-7) status bit is set.

Bit 4-7 SSx-SCSI STATUS bits 4-7

SCSI STATUS bits 4-7 define the type of interrupt that occurred. The possible codes are defined in the following table:

STATUS CODE	GROUP MEANING
0000 xxxx	The 33C92A is in a reset state.
0001 xxxx	A 33C92A command has completed successfully.
0010 xxxx	A 33C92A command has paused or was aborted by an Abort command.
0100 xxxx	A 33C92A command has been terminated prematurely due to an error or other unexpected condition.
1000 xxxx	An event on the SCSI bus requires service.

All other Status Code groups are currently not used and are reserved for future use.

In the following tables, the 'STATE' column indicates the current state in which the Status Code can occur. Also, the MCI field refers to the signals that define a SCSI bus information transfer phase: MSG, C/D, and I/O. A bit set to one indicates that the signal is asserted on the SCSI bus. A zero indicates negation. Whenever one of these Status Codes occurs, the REQ signal is asserted on the SCSI bus. The following table summarizes the meaning of the MCI field:

MCI CODE	MEANING
000	Data Out phase
001	Data In phase
010	Command phase
011	Status phase
100	Unspecified Info Out phase
101	Unspecified Info In phase
110	Message Out phase
111	Message In phase

6.2.19.1 Reset State Interrupts

STATUS CODE	STATE	SPECIFIC MEANING
0000 0000	DTI	33C92 Reset. The device has been reset, or a Reset command has executed successfully with no advanced features enabled. The new state of the 33C92A is disconnected.
0000 0001	DTI	33C92A Reset. The device has successfully completed a Reset command with advance features enabled. The new state of the 33C92A is disconnected.

6.2.19.2 Successful Completion Interrupts

STATUS CODE	STATE	SPECIFIC MEANING
0001 0000	D	A Reselect command completed successfully. The new state of the 33C92A is connected as a Target.
0001 0001	D	A Select command completed successfully. The new state of the 33C92A is connected as an Initiator.
0001 0010	-	Reserved for future use.
0001 0011	DT	A Receive, Send, Reselect-and-Transfer, Wait-for-Select-and-Receive, Send-Status-and-Command-Complete, or a Send-Disconnect-Message command completed successfully (ATN is not asserted).
0001 0100	DT	A Receive, Send, Reselect-and-Transfer, Wait-for-Select-and-Receive, Send-Status-and-Command-Complete, or a Send-Disconnect-Message command completed successfully (ATN is asserted).
0001 0101	DT	A Translate Address command completed successfully.
0001 0110	D I	A Select-and-Transfer command completed successfully.
0001 0111	-	Reserved for future use.
0001 1MCI	I	A Transfer (non-MESSAGE IN phase) command completed successfully. MCI defines the new information type (SCSI bus phase) being requested.

6.2.19.3 Paused Or Aborted Interrupts

STATUS CODE	STATE	SPECIFIC MEANING
0010 0000	I	A Transfer Info (MESSAGE-IN phase) command has paused with ACK asserted. This allows the host to examine the message before accepting it.
0010 0001	I	A Save-Data-Pointer message was received during a Select-and-Transfer command. The host should save its current data buffer pointer.
0010 0010	D	A Select or Reselect command was aborted.
0010 0011	T	A Receive or Send command was halted by an error or was aborted (ATN is not asserted).
0010 0100	T	A Receive or Send command was halted by an error, assertion of ATN, or was aborted (ATN is asserted).
0010 0101	D	Reserved for future use.
0010 0110	-	Reserved for future use.
0010 0111	D	The 33C92A has been reselected during a Select-and-Transfer (with IDI=0) by a Target that does not match the SCSI bus ID loaded into the DESTINATION ID register, or the following Identify message did not match the LUN loaded into the TARGET LUN register. ACK has been left asserted following the Identify message, and the bus ID and LUN of the reselecting Target are available in the SOURCE ID and TARGET LUN registers. (Advanced Mode only)
0010 1MCI	I	A Transfer command was aborted. MCI define the new information type (SCSI bus phase) being requested.

6.2.19.4 Terminated Interrupts

STATUS CODE	STATE	SPECIFIC MEANING
0100 0000	DTI	An invalid command was issued.
0100 0001	I	An unexpected disconnect (SCSI bus free) by the Target caused a command to terminate. The new state of the 33C92A is disconnected.
0100 0010	D	A timeout occurred during a Select or Reselect command. The state of the 33C92A is disconnected.
0100 0011	TI	A parity error caused a command to terminate ATN is not asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100 0100	TI	A parity error caused a command to terminate (ATN is asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100 0101	DT	The Logical Address exceeded the disk boundaries.
0100 0110	D	A Target whose SCSI bus device ID does not match the bus ID set in the DESTINATION ID register has reselected the 33C92A during a Select-and-Transfer command (with IDI=0). This interrupt occurs when the 33C92A is not in Advanced Mode. The new state of the 33C92A is connected as an Initiator.
0100 0111	I	A status byte with bad parity was received during a Select-and-Transfer command. ACK is asserted.
0100 1MCI	I	An unexpected information phase was requested. MCI define the SCSI bus phase which is requested.This is typically caused by a phase change before the Transfer Counthas reached zero, or an unexpected phase sequence occurred during a Select-and-Transfer command.

6.2.19.5 Service Required Interrupts

STATUS CODE	STATE	SPECIFIC MEANING
1000 0000	D	The 33C92A has been reselected. The new state of the 33C92A is connected as an Initiator. No Identify message transfer has yet occurred.
1000 0001	D	The 33C92A has been reselected in Advanced Mode. The SCSI bus ID of the Target may be read from the SOURCE ID register. The Identify message from the Target may be read from the DATA register. The ACK signal is left asserted. The new state of the 33C92A is connected as an Initiator.
1000 0010	D	The 33C92A has been selected (no ATN assertion). The new state of the 33C92A is connected as a Target.
1000 0011	D	The 33C92A has been selected (ATN was asserted). The new state of the 33C92A is connected as a Target.
1000 0100	T	The ATN signal has been asserted.
1000 0101	I	A disconnect has occurred. The new state of the 33C92A is disconnected.
1000 0110	-	Reserved for future use.
1000 0111	T	The Wait-for-Select-and-Receive command has paused because the first byte of the incoming CDB is not a known command group. The OWN ID register must be loaded with the CDB length,and the command resumed. The CDB1 register may be examined to determine the SCSI command group from the opcode. The new state of the 33C92A is connected as a Target. (Advanced Mode only)
1000 1MCI	I	The REQ signal has been asserted following connection or when the 33C92A is in the Initiator state and no command is executing. The information phase type should be examined. MCI define the information phase (SCSI bus phase) which is being requested.

6.2.20 Command Register

The COMMAND register is used to issue the 33C92A commands. This register should never be loaded when the CIP or INT bits (in AUXILIARY STATUS) are set to one, and a Level II command should never be loaded when the BSY bit is set to one.

The SINGLE-BYTE TRANSFER (SBT) bit in the COMMAND register is only used during information transfer type commands. When this bit is set in conjunction with one of these commands, the transfer counter is disabled and exactly one byte is to be transferred, regardless of the value in the TRANSFER COUNT register. The previous contents of the TRANSFER COUNT register are not preserved.

Refer to the COMMANDS section for a description of the commands and their corresponding command codes.

7	6	5	4	3	2	1	0
SBT	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Bit 0-6 CCx-COMMAND CODE bits 0-6

COMMAND CODE bits 0-6.

Bit 7 SBT-SINGLE-BYTE TRANSFER

SINGLE-BYTE TRANSFER bit.

6.2.21 Data Register

The DATA register is used to transfer data bytes between the host and the SCSI bus during the SCSI information transfer phases (command, data, status, or message phase). It may be accessed by the processor during any type of information phase (simple Level II commands) or via the DMA/WD interface during a SCSI Data In phase or Data Out phase (simple and combination Level II commands).

The DATA register is actually a port for the host interface into the internal twelve byte FIFO of the 33C92A. The FIFO is used for all transfers (synchronous and asynchronous) between the SCSI bus and the host bus, for both DMA and processor access transfers. If the 33C92A is to be halted for any reason (through ABORT, for example), then data transfers with this FIFO must continue until an interrupt occurs. This must be done so that the FIFO is returned to a ready state for subsequent transfers, and to flush incoming data to the host bus.

The DATA register is accessed by the processor during a data phase when the CONTROL register DMA mode select bits are all reset (=0), and when the DBR bit in the AUXILIARY STATUS register is true. The processor writes (reads) the DATA register by loading the ADDRESS register with a hex value of 19 and asserting the WE- (RE-) and CS- pins. This access also occurs during non-data phases.

When the CONTROL register DMA mode select bits are set for DMA mode or BURST mode, the DMA interface is enabled. In this case, the DATA register is written (read) when the DACK- and WE-(RE-) pins are asserted in response to the assertion by the 33C92A of the DRQ- pin.

When the WD BUS is selected by the DMA mode select bits, the RCS- pin functions as an external buffer chip select and the WE- and RE- pins become outputs, allowing the 33C92A to automatically transfer data between its DATA register and the external buffer. In this mode, bus control can be returned to the external processor or any other device by negating the DRQ pin.

6.3 Reset Conditions

6.3.1 Hardware Reset

The following results occur when the 33C92A is reset by the assertion of the MR- signal:

- The AUXILIARY STATUS register is reset to zero. The INT bit (and the INTRQ pin) is set to one when the hardware reset completes.
- The OWN ID register is reset to zero.
- Advanced mode is disabled.
- The ES, ER, and DSP bits in the SOURCE ID register are reset to zero.
- The SCSI STATUS register is reset to zero.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The internal clock divider circuit is set to divide by two.
- The following host accessible registers are NOT affected by the MR- signal:
  - Registers 01 hex through 15 hex;

- SOURCE ID (16 hex) register bits 0-3;
- COMMAND register (18 hex);

The SCSI Soft Reset may be implemented by using the SCSI bus reset signal to cause a reset of the 33C92A (for example, OR the host power on reset signal with the received SCSI bus reset (RST) signal). The host may examine the registers that are not affected by the MR- signal to recover from the SCSI reset condition.

6.3.2 Software Reset

The following results occur when the 33C92A executes the Reset command:

- The DBR bit in the AUXILIARY STATUS register is reset to zero. The INT bit (and INTRQ pin) is set to one when the Reset command is complete.
- All SCSI bus signals are reset to the negated state.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The OWN ID register is interpreted and the clock divisor, host parity, and advanced mode are configured.
- Registers 01 hex through 16 hex are reset to zero. The COMMAND register (18 hex) is also reset to zero.
- The SCSI STATUS register is set as commanded by the EAF bit in the OWN ID register.

7.0 COMMANDS

7.1 Command List

COMMAND CODE (HEX)	COMMAND	VALID STATES	LEVEL
00	Reset	D,T,I	I
01	Abort	D,T	I
02	Assert ATN	I	I
03	Negate ACK	I	I
04	Disconnect	T,I	I
05	Reselect	D	II
06	Select-with-ATN	D	II
07	Select-without-ATN	D	II
08	Select-with-ATN-and-Transfer	D,I	II
09	Select-without-ATN-and-Transfer	D,I	II
0A	Reselect-and-Receive-Data	D,T	II
0B	Reselect-and-Send-Data	D,T	II
0C	Wait-for-Select-and-Receive	D,T	II
0D	Send-Status-and-Command-Complete	T	II
0E	Send-Disconnect-Message	T	II
0F	Set IDI	D,T,I	I
10	Receive Command	T	II
11	Receive Data	T	II
12	Receive Message Out	T	II
13	Receive Unspecified Info Out	T	II
14	Send Status	T	II
15	Send Data	T	II
16	Send Message In	T	II
17	Send Unspecified Info In	T	II
18	Translate Address	D,T	II
20	Transfer Info	I	II

33C92A States:
D = Disconnected
T = Connected as a Target
I = Connected as an Initiator

Command Levels:
I = Level I command
II = Level II command

7.2 33C92A Command Types

There are two basic types of 33C92A commands: Level I and Level II. Level I commands may be issued while a Level II command is in progress (indicated by an AUXILIARY STATUS of BSY=1,CIP=0) and, except for the "Abort" and "Reset" commands, do not generate an interrupt upon their completion. Level II command execution will always result in an interrupt. If a Level II command is issued while another Level II command is executing, unpredictable results may occur.

There are two types of Level II commands. 'Simple' Level II commands are associated with a single operation or phase (for example, selection or information transfer). 'Combination' Level II commands combine multiple phases into a single 33C92A command to minimize interrupt overhead. The Initiator combination commands 'expect' certain SCSI bus phases at certain times during a sequence. These expected phases are based on common sequences performed by a Target on the SCSI bus; any deviation causes an interrupt. Target combination commands can be chained together to further minimize interrupt overhead by creating longer phase sequences.

NOTE: When using command chaining, care must be taken to ensure that all commands in the chain are initialized prior to issuing the command.

The 33C92A will be in one of three "states" during operation: Disconnected, Connected as a Target, or Connected as an Initiator. Certain commands are valid only in particular states as indicated in the COMMAND LIST. An attempt to issue a Level II command which is invalid for the present 33C92A state will cause an "invalid command" interrupt. Level I commands issued in invalid states will be ignored.

7.3 Advanced Mode Features

The 33C92A has several new features included which add new functions to the original 33C92 design. Some of these features cause the 33C92A to be incompatible with the 33C92. These features have been grouped together under the heading of 'Advanced Mode' features. These features are disabled when the 33C92A is reset by the MR- signal (hardware reset). They must be enabled by the host by issuing the 'Reset' command with the 'Enable Advanced Features' (EAF) bit set in the OWN ID register. The host can determine if advanced features have been enabled (thereby implying that a 33C92A is installed) by examining the SCSI STATUS register after issuing the 'Reset' command.

The features enabled by this bit are described in the subsections below.

7.3.1 Unexpected Reselection

When in normal (33C92) mode, a reselection when idle (ER=1) or when disconnected during a Select-and-Transfer command (and the Target bus ID does not match the DESTINATION ID register) causes an immediate interrupt after the reselection handshake is complete. In Advanced Mode, the 33C92A will continue to the Message In phase to fetch the Identify message. If the 33C92A was idle, the SCSI STATUS register will be set to 81 hex, and the Identify message will be in the DATA register. If the 33C92A was executing a Select-and-Transfer command, the SCSI STATUS register will be set to 27 hex, and the Identify message will be in the TARGET LUN register. In either case, the SOURCE ID register will contain the SCSI bus ID of the reselecting Target, and the ACK signal remains asserted so that the Identify message may be rEjected.

7.3.2 Unknown SCSI Command Groups

When a SCSI Command Descriptor Block is transferred on the SCSI bus, the command length in bytes is determined by the group code, which is found in bits 7-5 of the first command byte, or opcode. Group 0 (opcodes 00 to 1F hex), group 1 (opcodes 20 to 3F hex), and group 5 (opcodes A0 to BF hex) commands are defined by the SCSI standard (X3.131-1986) as six, ten, and twelve byte commands, respectively. All other command groups are undefined by that standard. In normal mode, the 33C92A will assume that these undefined groups are six byte commands when executing Select-and-Transfer or Wait-for-Select-and-Receive commands. In Advanced Mode, the following events will occur:

Select-and-Transfer:

When loading the CDB into the CDB registers prior to issuing the command, the host also loads the expected command length into the OWN ID register. The 33C92A uses this value to make sure the correct number of bytes are then transferred in the command phase.

Wait-for-Select-and-Receive

When receiving the CDB from the Initiator, the 33C92A will check the first CDB byte as soon as it is received. If the group is undefined, an interrupt will occur so that the host can examine the first command byte in the CDB 1ST register, and then load the TOTAL command length into the OWN ID register. The SCSI STATUS register is set to 87 hex, and the COMMAND PHASE register is set to 31 hex, when this interrupt occurs. After the interrupt, the 33C92A will only accept a Resume Wait-for-Select-and-Receive command, Abort, Disconnect, or Reset command. All other commands are invalid; during the interrupt processing, the 33C92A will continue to transfer the first six bytes of the command into its internal FIFO.

7.3.3 Data Phase Direction

During a Select-and-Transfer command in normal mode, the Data phase direction is determined solely by the Target; if this direction does not match the direction expected by the host, the 33C92A will not detect this error but expects that the transfer will continue. In Advanced Mode, the DPD bit in the DESTINATION ID register is compared with the state of the I/O signal on the SCSI bus. If the expected and actual directions do not match, an interrupt will occur with 'unexpected phase' status in the SCSI STATUS register.

7.4 Level I Commands

7.4.1 Reset (00 hex)

The Reset command performs a similar function to the hardware reset caused by asserting the MR- pin except that the OWN ID register is sampled for information concerning the operating configuration of the 33C92A. The 33C92A is also initialized as described in the RESET CONDITIONS section. The Reset command may be executed in any 33C92A state and will force the 33C92A into the Disconnected state, aborting any previously issued command in progress. Upon completion of the Reset command, an interrupt is generated the SCSI STATUS will be 00 hex or 01 hex, depending on the contents of the OWN ID register.

7.4.2 Abort (01 Hex)

The Abort command is valid in the Disconnected and Connected-as-Target states. The Abort command has different effects depending on the state and the command that is currently executing, as described below:

Disconnected State

In the Disconnected state, the Abort command may be used to halt an attempted Select, Select-and-Transfer, Reselect, or Reselect-and-Transfer command. If the Abort command is issued following a Select or Reselect command and the WD33C92A has won arbitration, the WD33C92A releases the SCSI bus by removing the Bus ID bits while SEL- is asserted and checking for a negated BSY- signal. If, after at least 200 us, there is no BSY- response, the WD33C92A goes to a Bus Free condition, and a "paused/aborted" interrupt is generated. If there is a response within this time period, then a "successful completion" interrupt will result instead. If the WD33C92A has not yet won arbitration, it will immediately abort the Select or Reselect command. The abort command will also terminate a Wait-for-Select-and-Receive command, if selection has not already begun. Once selected, the WD33C92A will ignore any abort attempts, and the command will finish normally.

Target State

When the WD33C92A is in a Connected-as-a-Target state, the Abort command may be used to abort Receive, Send, or the data phase portion of a Target combination command.
When issuing an Abort in the Connected-as-a-Target state, the following rules apply:

1. When a Abort command is issued to abort a Send or Reselect-and-Send command, the local processor must not service any data request (DBR, DRQ, etc.) from the WD33C92A until an interrupt from the WD33C92A occurs. This is required to allow the FIFO to clear; the Abort processing will not complete until the FIFO contents are flushed to the SCSI bus. The WD33C92A removes the data request at an arbitrary time during the Abort command processing and the data request is not valid once the Abort command is written to the COMMAND register.

2. When a Abort command is issued to abort a Receive or Reselect-and-Receive command, the local processor must CONTINUE to service any data request (DBR, DRQ, etc.) from the WD33C92A until an interrupt from the WD33C92A occurs. This is required to allow the FIFO to clear; the Abort processing will not complete until the FIFO contents are flushed to the local processor.

After the Abort command is processed and the local processorhas received the interrupt indicating this, the TRANSFER COUNT register contains the number of bytes that were not successfully transferred with the SCSI bus. The WD33C92A remains in the Connected-as-a-Target state. The WD33C92A is now ready to receive any appropriate Target mode command, including a resume of the command that was aborted.

7.4.3 Disconnect (04 hex)

The Disconnect command may be used in either the Target or the Initiator connected states. In the Target role, the Disconnect command is the normal procedure for disconnecting from the SCSI bus following the information transfer phase. In the Initiator role, Disconnect can be used to release the bus following a timeout condition. The Disconnect command causes the immediate release of all bus signals and, in Target mode, returns the SCSI bus to the Bus Free phase. If the Disconnect command is issued during an active Level II command, the Level II command is immediately terminated and the 33C92A transitions to the Disconnected state.

7.4.4 Assert ATN (02 hex)

The Assert ATN command is only valid when Connected as an Initiator. It is normally used to allow the Initiator to inform a Target that it has a message pending (The Target is expected to respond by performing a Message Out Phase). ATN is automatically negated:

- before the last byte of a Transfer Info command issued in response to the Message Out phase;
- when the Identify message out is transferred to the Target during a Select-and-Transfer command;
- when a SCSI Bus Free phase occurs.

The Select-with-ATN and Select-with-ATN-and-Transfer commands will cause the 33C92A to automatically assert ATN prior to the release of SEL- providing the bus arbitration is won.

7.4.5 Negate ACK (03 hex)

The Negate ACK command causes ACK to be negated. It may be used:

- When Connected as an Initiator following Message-In Transfer Info commands.
- After the 33C92A has detected a parity error on any received information and the HALT on SCSI PARITY ERROR (HSP) bit is set.
- After unexpected reselection in advanced mode.
- After a Save-Data-Pointer message is received during a Select-and-Transfer command.
- Host parity errors do not affect the ACK signal. For all other Initiator transfers, ACK negation is automatic.

In the case of a Message-In transfer, incoming messages may be rejected and the Initiator may indicate its intent to send either a "MESSAGE REJECT" or a "MESSAGE PARITY ERROR" Message by issuing the Assert ATN command prior to issuing the Negate ACK command. If the incoming message is to be accepted, only the Negate ACK command should be issued.

During non-Message-In transfers, if the Transfer command is terminated by a parity error, the Assert ATN command can again be issued prior to Negate ACK, this time indicating the Initiator's intent to send an "INITIATOR DETECTED ERROR" Message.

7.4.6 Set IDI (0F hex)

The Set IDI command is used in the Initiator role to support overlapped SCSI operations. If a SCSI command is executing via a Select-and-Transfer command, then the Set IDI command may be used to set the IDI bit in the CONTROL register, which then causes an interrupt to occur upon a Target disconnection. This ability allows the IDI bit to be left reset when the first SCSI operation is started, which may reduce the number of 33C92A interrupts, yet also allows a second operation to be started when needed without waiting for the first operation to be completed.

7.5 Simple Level II Commands

7.5.1 Select-with-ATN (06 hex)

Select-with-ATN is valid only in the Disconnected state and when issued will cause the 33C92A to select a Target. Before issuing this command, the SCSI Bus ID of the Target device should be written into the DESTINATION ID register. When the Select-with-ATN command is issued, the 33C92A begins bus arbitration. If the 33C92A is selected or reselected by another device during the arbitration, the Select-with-ATN command is aborted and a "service required" interrupt (8x hex) is generated.

Should the 33C92A win the arbitration, SEL- and ATN are asserted, the Target and Initiator Bus IDs are placed on the SCSI data bus, and then BSY- is deasserted. At this time, a timeout sequence whose length is determined by the value in the TIMEOUT PERIOD register begins. If BSY- is not asserted by the Target before a timeout occurs, the 33C92A begins its selection abort sequence (as described in the Abort command description), and if there is no Target response the Select-with-ATN command is terminated and a "terminated" interrupt is generated. If the Target responds before the timeout period has elapsed or before the selection abort sequence is complete, the 33C92A negates the SEL-signal, putting the 33C92A in a Connected-as-an-Initiator state. A "successful completion" interrupt indicates that the Select-with-ATN command has been completed successfully.

If the 33C92A does not win the arbitration or there is no response from the Target and the timeout feature is disabled, the Select-with-ATN command can be aborted with an Abort command. When the Abort command is successfully executed under these circumstances, the 33C92A is disconnected from the bus and a "paused/aborted" interrupt is generated.

7.5.2 Select-without-ATN (07 hex)

The Select-without-ATN command is identical to the Select-with-ATN command except that ATN is not set during the Selection Phase.

7.5.3 Reselect (05 hex)

The Reselect command is identical to the Select-without-ATN command except that the I/O signal is asserted upon completion of the Arbitration Phase. Successful completion of the Reselect command results in the 33C92A being Connected as a Target.

7.5.4 Receive (10-13 hex)

There are four Receive commands which are distinguished from each other only by the state of three SCSI interface signals and the type of data that is transferred. These commands, consisting of the Receive Command, Receive Data, Receive Message Out, and Receive Unspecified Info Out commands are valid only in the Connected-as-a-Target state. The type of the Receive command selected determines the state of the I/O-, C/D-, and MSG outputs during the command according to the following chart (1=asserted):

Receive Command Type	OP Code	MSG	C/D	I/O
Receive Command	10	0	1	0
Receive Data	11	0	0	0
Receive Message Out	12	1	1	0
Receive Unspecified Info Out	13	1	0	0

The Receive commands are information transferring commands and are therefore dependent on the SBT bit in the COMMAND register for determination of a successful completion. In addition to a termination caused by reset (via either a Reset command being issued or assertion of the MR-pin), a Receive command completion or termination will occur under any of these conditions:

1. The internal transfer counter is disabled (SBT=1 or the TRANSFER COUNT register is loaded with zero) and a single byte has been read from the DATA register.
2. The counter has decremented to zero (with SBT=0) indicating that the specified number of bytes have been transferred.
3. A parity error has been detected on one of the received data bytes (and HSP=1).
4. The ATN pin is asserted (and HA=1).
5. The Abort command is issued.
6. A Disconnect command is issued.

When the Receive command is completed as a result of receiving the correct number of bytes, a "successful completion" interrupt will be generated. If a parity error has caused termination, a "terminated" interrupt will instead be generated. In this case, the TRANSFER COUNT register will contain the number of bytes yet to be transferred. After any completion or termination of the Receive commands except those due to a subsequent Disconnect command or reset, the 33C92A is in the Connected-as-a-Target state.

As data transfer commands, the Receive commands are dependent on the DMA mode select bits in the CONTROL register for the DATA register accessing mode. These bits determine whether the DATA register accesses will be handled by the processor or through a DMA/WD interface. When the processor is required to read the DATA register (i.e. DMA mode select bits=0), it must monitor the DBR status bit (in AUXILIARY STATUS) to determine when a byte is available for reading. During Receive commands, this status bit will be reset when a byte is read from the DATA register and set when a byte is loaded into the DATA register via the SCSI interface. DBR is also reset when a Receive command is issued.

All information transfers involving other than data information are asynchronous. However, if the information phase involves data transfers, the SYNCHRONOUS TRANSFER register will be evaluated. In this case, any selected offset other than zero results in synchronous transfers. The minimum Transfer Period for both types of transfers is determined by the transfer period bits in this same register.

7.5.5 Send (14-17 hex)

As in the case of the Receive commands, there are four Send commands which are distinguished only by the state of the I/O-,C/D-, and MSG pins and the type of data that is transferred. The four Send commands, also valid in the Connected-as-a-Target state only, are the Send Status, Send Data, Send Message In, and Send Unspecified Info In commands. The SCSI pin states during the Send commands are determined by the particular command as follows (asserted=1):

Send Command Type	OP Code	MSG	C/D	I/O
Send Status	14	0	1	1
Send Data	15	0	0	1
Send Message In	16	1	1	1
Send Unspecified Info In	17	1	0	1

The Send commands are also information transferring commands and as such are also dependent upon the SBT bit in the COMMAND register for command completion. In addition to that caused by reset (via either a Reset command being issued or assertion of the MR- pin), a Send command completion or termination will occur under any of these conditions:

1. The internal transfer counter is disabled (SBT=1 or the TRANSFER COUNT register is loaded with zero) and a single byte has been read from the DATA register.
2. The counter has decremented to zero (with SBT=0) indicating that the specified number of bytes have been transferred
3. A parity error has been detected on one of the data bytes from the host (and HHP=1).
4. The ATN pin is asserted (and HA=1).
5. The Abort command is issued.
6. A Disconnect command is issued. The 33C92A remains Connected-as-a-Target following the Send command completion/termination unless the Disconnect command or reset was used to force a termination.

During a Send command, DATA register accessing is controlled by the DMA mode select bits in the CONTROL register. When these bits are set to the appropriate mode, loading of the DATA register is accomplished by a DMA controller or through the WD-Bus interface. If the DMA mode select bits are zero, the processor must poll the AUXILIARY STATUS register and can write to the DATA register only when the DATA BUFFER READY bit is set (DBR=1). Send commands cause the DBR bit to be reset every time the processor loads a byte into the DATA register and set when a byte is transferred from the DATA

register onto the SCSI data bus. The DBR bit will also be set upon issuing a Send command.

As in the case of Receive commands, synchronous transfers will occur only when data transfers are involved and an offset other than zero is selected.

7.5.6 Transfer Info (20 hex)

The Transfer Info command is valid only when Connected as an Initiator and is used to send and receive data, command, status, and message information.

The first REQ assertion following connection as an Initiator results in a "service required" interrupt. The processor should examine the SCSI STATUS register to determine the type and direction of information transfer requested by the Target, and then issue a Transfer Info command in response. While an Initiator, the 33C92A will also generate an interrupt each time the Target device requests a new type of information transfer phase.

As in the case of the Send and Receive commands, when completion of the Transfer Info command depends upon the internal transfer counter, the processor should load the TRANSFER COUNT register prior to issuing this command. The DMA mode select bits in the CONTROL register, the offset and transfer period bits in the SYNCHRONOUS TRANSFER register, and the SBT bit in the COMMAND register are used during Transfer Info commands just as they are during the Send and Receive commands. However, for processor access of the DATA register during Transfer Info commands (when the DMA mode select bits are zero or the bus phase is other than Data phase), behavior of the DATA BUFFER READY (DBR) status bit is determined by the direction of information transfer as defined by the I/O- pin. When the transfer is from Initiator to Target, the DBR bit is reset by writing to the DATA register and is set when the byte is transferred from the DATA register onto the SCSI data bus. When the transfer is from Target to Initiator, DBR is set when a byte is received over the SCSI data bus and transferred into the DATA register and is reset by reading the DATA register. DBR is also reset whenever a Transfer Info command is issued.

There are several causes of a Transfer Info command completion/termination in addition to a reset. Just as for a Send or Receive command, the Transfer Info command can be terminated by issuing a subsequent Disconnect command, causing an immediate disconnect but no interrupt.

A Transfer Info command will either complete or pause when the specified number of bytes (either a single byte or multiple bytes as defined by the SINGLE-BYTE TRANSFER bit in the COMMAND register) has been sent or received. The 33C92A generates a "successful completion" interrupt only after receiving another REQ from the Target during non-Message-In information phases but generates a "paused/aborted" interrupt for Message-In phases without waiting for an additional REQ (Note that when the completed Transfer Info command was a Message-In transfer phase, the ACK pin will be left asserted by the 33C92A in the last REQ/ACK cycle of the command, and the processor is required to issue a Negate ACK or an Assert ATN followed by a Negate ACK command to accept or reject the message).

If a parity error is detected on a data byte received from the SCSI bus (and HSP=1) or on a data byte byte received from the host (and HHP=1), then the 33C92A will terminate the command and, for SCSI parity errors, will leave ACK asserted (to also halt the Target). In this case a "terminated" interrupt is generated. Finally, a negation of the BSY- signal (i.e. the Target suddenly disconnects) or a transition in the I/O-, C/D-, and/or MSG pins during a Transfer command will also terminate the command and generate a "terminated" interrupt.

If a parity error is detected on a received byte but parity error command termination is disabled (HSP=0 or HHP=0, as appropriate), the 33C92A will still set the PARITY ERROR status bit in the AUXILIARY STATUS register but will not terminate the command as a result of this error.

7.5.7 Translate Address (18 hex)

The Translate Address command performs a logical-address to physical-address translation. Certain SCSI commands involve a logical address which may be up to 32 bits in length. When a command is detected which requires address translation, the processor can load the logical address into the 33C92A LOGICAL ADDRESS register and then issue the Translate Address command to have the 33C92A do the conversion. Upon receiving a "successful completion" interrupt, the processor can read the CYLINDER NUMBER, HEAD NUMBER, and SECTOR NUM-

BER registers to extract the logical address. The disk parameters contained in the TOTAL SECTORS, TOTAL HEADS, and TOTAL CYLINDERS registers must also be valid before issuing a Translate Address command.

If automatic compensation for spare sectors is to be performed by the WD33C92A, then the number of spare sectors per cylinder and total number of sectors per cylinder must also be loaded, respectively, into the HEAD NUMBER and CYLINDER NUMBER registers. A "terminated" interrupt will occur if any division operation performed during this command results in an overflow.

7.6 Combination Level II Commands

7.6.1 Select-and-Transfer (08 and 09 hex)

The Select-and-Transfer commands greatly reduce the host or local processor interrupt-handling burden by enabling the 33C92A's internal microprocessor to manage the low-level SCSI protocol, resulting in as few as one interrupt per SCSI operation. Select-and-Transfer commands are used when in an Initiator role, and typically consist of at least the following SCSI phases:

1. Selection of a Target device.
2. Sending of a command.
3. Reception of status information.
4. Reception of a COMMAND COMPLETE Message.

These commands optionally consist of a Data Transfer phase and additional Message Transfer phases.

The 33C92A will update the COMMAND PHASE register as the Select-and-Transfer command executes. Upon completion or termination of the command, the local processor can read this register to determine where the SCSI operation stopped.

The two Select-and-Transfer commands differ from each other only by whether or not the ATN pin is asserted during the Selection phase. The ability to assert ATN during Selection supports the SCSI Message Protocol which calls for an IDENTIFY Message Out phase following the Selection. When executing a Select W/ATN-and-Transfer commands, the 33C92A expects the Target to request a Message Out phase immediately following selection, whereas for a Select W/O ATN-and-Transfer command, it expects the Target to directly enter Command phase. The Select-and-Transfer commands, moreover, support Group 0 (6-byte CDB), Group 1 (10-byte CDB), and Group 5 (12-byte CDB) SCSI commands.

When a Select-and-Transfer command is issued, the 33C92A arbitrates for the bus and selects a Target just as during a Select command. If the Target does not respond before a timeout occurs, the Select-and-Transfer command halts and a "terminated" interrupt is generated. Failure to complete the Selection phase is also indicated by the fact that the COMMAND PHASE register contains all zeros. If the Selection is successful, no interrupt is generated, but the COMMAND PHASE register will be set to a hex 10.

After completing the Selection phase, the 33C92A begins an information transfer phase. If ATN has been asserted (i.e. a Select W/ATN-and-Transfer command was issued), the 33C92A expects the Target to respond with a Message Out phase. If the first information phase request is other than a Message Out request, the 33C92A will terminate the command and generate a "terminated" interrupt. However, when the Target does request a Message Out phase, the 33C92A will respond by automatically sending an IDENTIFY Message. This single byte message is of the binary form: 1r000ttt, where r=1 if the ENABLE RESELECTION bit in the SOURCE ID register is equal to 1, and ttt is the encoded Target LOGICAL UNIT NUMBER contained in the TARGET LUN register. Once the IDENTIFY Message has been sent, the 33C92A will set the COMMAND PHASE register to hex 20.

Following the Message Out phase (or Selection phase when ATN was not asserted during Selection), a Command phase is expected by the 33C92A. Again, and throughout the entire Select-and-Transfer command execution, if the Target requests an unexpected information phase type, the 33C92A terminates the command and generates a "terminated" interrupt. If the Command phase is requested in this situation, the 33C92A will extract the SCSI command from the internal COMMAND DESCRIPTOR BLOCK registers and send the 6-, 10-, or 12-bytes of command information as determined by its evaluation of the SCSI command code in the CDB1 register. The

COMMAND PHASE register is set to hex 30 before the first Command byte is sent and then increments with each byte transferred, so that for a 12-byte CDB command the COMMAND PHASE register will contain hex 3C when all bytes of the CDB have been transferred.

After the Command phase, the 33C92A expects either a Data In phase, Data Out phase, Status phase, or Message In phase. If the Target is requesting a Message In phase, a pending disconnection is assumed. The 33C92A therefore expects to receive either a Save-Data-Pointer message (hex 02) or a Disconnect message (hex 04). If either message is incorrect, or if a different message is received, a "terminated" interrupt will be generated to alert the processor of that fact and to allow the message to be read from the DATA register. A "terminated" interrupt will also be generated if the Target disconnects before sending the Disconnect message. When a correct Save-Data-Pointer message is received, a "paused/aborted" interrupt is generated and the Select-and-Transfer command terminated to allow the processor to save the SCSI data pointer. However, if a Disconnect message is received, the COMMAND PHASE register will be updated to hex 42 and command execution continues.

When the actual Target-disconnection does occur, the COMMAND PHASE register is updated to hex 43 and if the IDI bit is set, the WD33C92A terminates the Select-and-Transfer command by generating an 85H interrupt. However, if the IDI bit is reset, then instead the WD33C92A sits in an idle state, waiting for the Target to reconnect. If a different Target device Reselects the 33C92A, a "terminated" interrupt is generated. However, if the original Target Reselects the 33C92A, no interrupt is generated and the COMMAND PHASE register is set to hex 44.

Following the original Target Reselection, the 33C92A expects a Message In phase which should consist of the Target sending an IDENTIFY Message. This single-byte message should be of the binary form: 10000ttt, where ttt is the Target LUN. If the data received by the 33C92A is different or the Target LUN specified in this byte does not match the contents of the TARGET LUN register, a "terminated" interrupt is generated and the Message byte may be examined by the processor. A correct IDENTIFY Message In phase results in the COMMAND PHASE register being updated to hex 45.

After the IDENTIFY Message is received from the Target or immediately after the Command Out phase (when there is no disconnection), a Data In phase, Data Out phase, or Status phase should occur. If the TRANSFER COUNT register contains any non-zero value, then the 33C92A will expect a Data Transfer phase. If Advanced Features are enabled, then the DPD bit will be examined to verify the correct data direction. If the data direction is incorrect, then a "terminated" interrupt is generated. In this phase, the 33C92A will use the TRANSFER COUNT register to determine the number of bytes to be transferred, and all host-side DATA register accesses will be accomplished via the method selected by the DMA mode select bits in the CONTROL register. When the internal counter reaches zero, the Data Transfer phase is complete and the COMMAND PHASE register is set to hex 46.

Any number of disconnection/reconnection cycles may occur during the Data Transfer phase so long as they are accomplished according to the defined message protocol. The COMMAND PHASE register will cycle through the disconnect phases (41-45) with each disconnection and subsequent reconnection until all of the data has been transferred and the Data Transfer phase is complete.

A Status phase is expected by the 33C92A following the Data Transfer phase (or instead of the Data Transfer phase when the TRANSFER COUNT register contains a value of zero). At the start of the Status phase, the COMMAND PHASE register is loaded with hex 47. Upon completion of the Status phase, the COMMAND PHASE register will be updated to hex 50, and the received status byte is stored in the TARGET LUN register where it can be read upon completion of the command.

Following completion of the status-byte transfer, a Message In phase is expected. The 33C92A expects the Target to send a COMMAND COMPLETE Message (hex 00) to indicate that the SCSI command operation has been completed. After the 33C92A receives this COMMAND COMPLETE Message, the COMMAND PHASE register advances to hex 60, and if the EDI bit is reset, a "successful completion" interrupt is generated. The processor should then read the TARGET LUN register to examine the Target status. An additional interrupt will then occur when the SCSI bus goes to the Bus Free state, or when

another REQ is asserted to begin an information transfer phase (as in SCSI linked commands). If the EDI bit is set, the "successful completion" interrupt will be suppressed until the Target disconnects from the SCSI bus.

At any time during execution of the Select-and-Transfer commands, an abnormal or unexpected condition will cause the 33C92A to terminate the command, set the appropriate status qualifiers, and generate a "terminated" interrupt. If the termination occurred during an information transfer phase, the 33C92A will be left in a Connected-as-an-Initiator state (unless termination was due to a sudden Target disconnection). Command termination during any other phase will result in the 33C92A being in a Disconnected state. Transfer commands may be used to handle the exception by transferring messages with the Target.

The following table summarizes the possible values that the COMMAND PHASE register can take during the Select-and-Transfer commands, and their meanings relative to command termination:

COMMAND PHASE	MEANING
00	No SCSI bus device has been selected. The 33C92A is in the disconnected state.
10	The Target has been selected. The 33C92A is now in the connected as an Initiator state.
20	An Identify message has been sent to the Target.
30	Command phase has started, no bytes transferred.
3x	Command phase, x bytes have been transferred.
41	Save-Data-Pointer message received.
42	Disconnect message received, bus not free.
43	Target has disconnected (SCSI bus free) following a successful transfer of a Disconnect message. The 33C92A is now in the disconnected state.
44	The 33C92A has been reselected by the Target whose SCSI bus ID matches the value in the DESTINATION ID register. The 33C92A is now in the connected as an Initiator state.
45	The 33C92A has received an Identify message from the Target whose Logical Unit Number matches the value in the TARGET LUN register.
46	The number of bytes specified in the TRANSFER COUNT register have been transferred to/from the Target during a Data Out/In phase.
47	The Target has begun a Receive Status phase.
50	The 33C92A has successfully received a Status byte from the Target and stored it in the TARGET LUN register.
60	The 33C92A has successfully received a Command Complete message from the Target.

A "Resume Select-and-Transfer" command is assumed whenever a normal "Select-and-Transfer" command is issued while the 33C92A is in the Connected-As-An-Initiator state. When the "Resume" is issued, the 33C92A examines the COMMAND PHASE register to determine where to restart the Select-and-Transfer command execution. This feature, in conjunction with the INTERMEDIATE DISCONNECT INTERRUPT enabled, allows support of multi-threaded or overlapped I/O on the SCSI bus.

The following table briefly describes the valid settings of the COMMAND PHASE register when resuming a Select-and-Transfer command:

COMMAND PHASE	MEANING
10	Resume after Target selection is complete.
20	Resume after Identify message out. Command phase is expected; an implied Negate ACK occurs.
30	Resume when Command phase has begun (REQ asserted).
41	Resume after Command phase or after Save-Data-Pointer message. Data, Status, or Message In phases are expected. An implied Negate ACK occurs.
42	Resume to complete Disconnect Message In; an implied Negate ACK occurs.
44	Resume after reselection by a Target.
45	Resume to transfer more data in a data transfer phase. May expect Status or Message In as well. An implied Negate ACK occurs.
46	Resume after the data has has been completed, expecting Status phase or a Save-Data-Pointer/Disconnect Message In phase. An implied Negate ACK does NOT occur.
50	Resume to complete a Status phase; an implied Negate ACK occurs.
60	Resume to complete a Command Complete message from the Target; an implied Negate ACK occurs.

7.6.2 Reselect-and-Transfer (0A and 0B hex)

The Reselect-and-Transfer commands include the Reselect-and-Receive-Data and the Reselect-and-Send-Data commands. These commands cause the 33C92A to execute certain common SCSI bus phase sequences as a Target following a Reselection phase. These phases are determined by which command is sent, and the setting of two bits: the EDI bit in the CONTROL register; and the SCC bit in the DESTINATION ID register. The SCSI bus phase sequences are summarized below.

Refer to the command descriptions of the Send-Status-and-Command-Complete and Send-Disconnect-Message commands for details on those sequences.

1. Reselect-and-Receive command, EDI=0, and SCC=don't care:

   - Reselection phase;
   - Send Identify Message In;
   - Receive Data Out phase;
   - Completion interrupt.

2. Reselect-and-Send command, EDI=0, and SCC=don't care:

   - Reselection phase;
   - Send Identify Message In;
   - Send Data In phase;
   - Completion interrupt.

3. Reselect-and-Receive command, EDI=1, and SCC=0:

   - Reselection phase;
   - Send Identify Message In;
   - Receive Data Out phase;
   - Chain to Send-Status-and-Command Complete;

4. Reselect-and-Send command, EDI=1, and SCC=0:

   - Reselection phase;
   - Send Identify Message In;
   - Send Data In phase;
   - Chain to Send-Status-and-Command-Complete;

5. Reselect-and-Receive command, EDI=1, and SCC=1:

   - Reselection phase;
   - Send Identify Message In;
   - Receive Data Out phase;
   - Chain to Send-Disconnect-Message;

6. Reselect-and-Send command, EDI=1, and SCC=1:

   - Reselection phase;
   - Send Identify Message In;
   - Send Data In phase;
   - Chain to Send-Disconnect-Message;

If the reselection attempt times out during a Reselect-and-Transfer command, ATN is asserted and HA=1, or if a parity error is detected on a incoming data byte (and HSP=1 or HHP=1, depending on data direction), the command will be terminated and the appropriate status will be set. In this case, the COMMAND

PHASE register should be evaluated to determine the last successfully completed phase. If none of these conditions occurs, all phases complete normally, and if EDI=0, then a "successful completion" interrupt would be generated at this point. However, if EDI=1, no interrupt is generated and command chain occurs (as described above).

The following table summarizes the possible values that the COMMAND PHASE register can take during the Reselect-and-Transfer commands, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No SCSI bus device has been reselected. The 33C92A is in the disconnected state.
10	The 33C92A has successfully reselected the Initiator. The 33C92A is now in the connected as a Target state.
20	The Identify message has been successfully sent to the Initiator.
46	The requested data transfer has been completed.

A "Resume Reselect-and-Transfer" command is assumed whenever a normal "Reselect-and-Transfer" command is issued while the 33C92A is in the Connected-as-a-Target state. When the "Resume" is issued, the 33C92A examines the COMMAND PHASE register to determine where to restart the Reselect-and-Transfer command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Reselect-and-Transfer command:

COMMAND PHASE	MEANING
10	Resume after Initiator reselection is complete; start with Identify Message Out.
20	Resume after Identify message out; start with data transfer phase. If TRANSFER COUNT is zero, no data transfer phase occurs. In either case, a chain to another combination command can occur if enabled.

7.6.3 Wait-for-Select-and-Receive (0C hex)

The Wait-for-Select-and-Receive causes the 33C92A to idle until it is selected by an Initiator, at which time the 33C92A will enter the Target mode and message and command information will automatically be requested. As an option, the 33C92A may be programmed to disconnect when a SCSI read command is received while executing a Wait-for-Select-and-Receive command. Use of this command therefore eliminates the interrupts which normally occur after selection and after each subsequent SCSI bus phase, and results in very short bus-connect time during SCSI read commands.

If ATN was asserted by the Initiator during the selection phase, the 33C92A will first execute an implied "Receive Message Out" command to get the Identify message from the Initiator, before continuing on with the implied "Receive Command" to receive the SCSI command information. The SCSI command information (CDB) will be stored in the CDB registers (hex addresses 03 to 0E), and if a valid IDENTIFY message is received, it will be saved in the TARGET LUN register (hex address 0F). The number of command bytes requested by the 33C92A is determined by the SCSI group code in the first byte of the CDB.

After the 33C92A is selected and receives all valid command and message information, a "successful completion" interrupt will normally be generated to allow the local processor to read out and interpret the SCSI CDB. However, by setting the EDI bit prior to issuing a Wait-for-Select-and-Receive command, the 33C92A is enabled to perform an automatic disconnect when a SCSI read command is received. Therefore, when EDI=1 and the 1st CDB byte received contains a 6-, 10-, or 12-byte read command code, then the 33C92A will temporarily suppress the interrupt and chain to begin execution of a Send-Disconnect-Message command. An interrupt will then be generated after completion of this command, which normally would indicate a transition to the bus free condition. Refer to the Send-Disconnect-Message command description for more details.

If during execution the message or command information received from the Initiator is invalid, the implied receive command will be terminated and the appropriate status reported. In this case, the COMMAND PHASE register should be read to determine which phase of the Wait-for-Select-and-Receive command was last completed before the error condition occurred. A COMMAND PHASE hex value of hex 10 indicates that the 33C92A was successfully selected. A hex value of 20 indicates that a message was received from the Initiator, and when the 33C92A begins receiving command bytes, the COMMAND PHASE is set to hex 30 and increments with each byte received (to a maximum of 3C for a 12-byte CDB command).

The following table summarizes the possible values that the COMMAND PHASE register can take during the Wait-for-Select-and-Receive command, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	The 33C92A has not been selected. The 33C92A is in the disconnected state.
10	The 33C92A has been successfully selected by the Initiator. The 33C92A is now in the connected as a Target state.
20	The Identify message has been successfully received from the Initiator.
30	The 33C92A has begun command phase by setting the SCSI bus phase signals and asserting REQ.
31	The 33C92A has transferred 1 command byte from the Initiator. The SCSI STATUS may indicate the need for the host to load the command size into the OWN ID register.
3x	The 33C92A has transferred x command bytes from the Initiator.

A "Resume Wait-for-Select-and-Receive" command is assumed whenever a normal "Wait-for-Select-and-Receive" command is issued while the 33C92A is in the Connected-as-a-Target state. When the "Resume" is issued, the 33C92A examines the COMMAND PHASE register to determine where to restart the Wait-for-Select-and-Receive command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Wait-for-Select-and-Receive command:

COMMAND PHASE	MEANING
10	Resume after selection by the Initiator is complete; start with Identify Message Out if ATN is asserted, otherwise, start with command phase.
20	Resume after a message out; check the received message in the TARGET LUN register for a valid Identify message.
30	Resume after Identify message out. Start with command phase.
31	Resume after the 33C92A has transferred 1 command byte from the Initiator. This resume point is used only when an unknown group code has been detected in Advanced Mode, and the command size has been loaded into the OWN ID register.

7.6.4 Send-Status-and-Command-Complete (0D hex)

The Send-Status-and-Command-Complete command is valid in the Target role, and is used to complete a SCSI operation by transferring the appropriate status information to the Initiator prior to disconnection from the SCSI bus. This command also supports linked SCSI operations by optionally allowing a linked command-complete message to be sent after the status is transferred. Linked command complete messages are controlled by the CDB12 register with bits that correspond to the standard linked command control bits in the CDB.

Before a Send-Status-and-Command-Complete command is issued, the CDB11 register must be loaded with a status byte which will then be transferred across the SCSI bus. Also, the link control bits from the current CDB must be loaded into the CDB12 register to ensure that the correct sequence occurs.

The bits used by the 33C92A are identical in meaning to the SCSI standard link control bits. The host processor may simply load the control byte from the current SCSI command into CDB12 to get the correct function. As the command execution progresses, the COMMAND PHASE register will be updated to indicate the last phase completed.

The possible sequences caused by this command are as follows:

1. CDB12 bit0=0, bit1=don't care: The status byte in CDB11 is sent, followed by a Command Complete message (00 hex). A "successful completion" interrupt now occurs.

2. CDB12 bit0=1, bit1=0: The status byte in CDB11 is sent, followed by a Linked Command Complete message (0A hex). A chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to fetch the next CDB from the Initiator. 33C92A command execution proceeds as described for that command.

3. CDB12 bit0=1, bit1=1: The status byte in CDB11 is sent, followed by a Linked Command Complete with Flag message (0B hex). A chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to fetch the next CDB from the Initiator. 33C92A command execution proceeds as described for that command.

A Send-Status-and-Command-Complete command may be terminated by ATN asserted when HA=1, or when a Disconnect or Reset command is issued.

The following table summarizes the possible values that the COMMAND PHASE register can take during the Send-Status-and-Command-Complete command, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No operation occurred; typically, ATN was found to be asserted.
50	Status phase transfer completed.
60	Command Complete message transfer completed.
61	Linked Command Complete message transfer completed.

A "Resume Send-Status-and-Command-Complete" command is assumed whenever a normal "Send-Status-and-Command-Complete" command is issued while the 33C92A is in the Connected-as-a-Target state. When the "Resume" is issued, the 33C92A examines the COMMAND PHASE register to determine where to restart the Send-Status-and-Command-Complete command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Send-Status-and-Command-Complete command:

COMMAND PHASE	MEANING
50	Resume after status phase. Start with command complete message. May chain to command fetch if commanded to do so.

7.6.5 Send-Disconnect-Message (0E hex)

The Send-Disconnect-Message command is a Target-role command which may be used to disconnect from the SCSI bus at any time during a SCSI command sequence. This command consists of sending a Disconnect message byte, followed by physical disconnection from the bus (SCSI bus free). An interrupt is generated only after transition to bus free occurs. As an option, a Save-Data-Pointer message will automatically be sent before the Disconnect message whenever the IDI bit is set prior to issuing this command.

The COMMAND PHASE register is updated during execution of the Send-Disconnect-Message command to indicate bus phase status. After a Save-Data-Pointer message is sent, the COMMAND PHASE will be set to 41H. After the Disconnect message transfer, this register will be updated to 42H, and after disconnection the COMMAND PHASE register will contain a 43H.

A Send-Disconnect-Message command may be terminated by ATN asserted when HA=1, or when a Disconnect or Reset command is issued.

The following table summarizes the possible values that the COMMAND PHASE register can take during the Send-Disconnect-Message, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No operation occurred; typically, ATN was found to be asserted.
41	The Save-Data-Pointer message was transferred.
42	The Disconnect message was transferred.
43	The bus free state occurred after the Disconnect message was transferred. The 33C92A is now in the disconnected state.

8.0 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Ambient temperature under bias	$0^{o}C$ to $70^{o}C$
Storage temperature	-55^{o} C to 125^{o} C
Voltage on any pin with respect to GND	-0.5 to 7 Volts
Power dissipation	190 mW
Input Static Discharge Protection	2000 V pin to pin

NOTE
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

8.2 Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating temperature range	0^{o} to 70^{o} C
V_{CC}	+5 Volts $\pm$ 0.25 V
V_{SS}	0 Volts

28

8.3 DC Operating Characteristics

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage	---	10	µA	V_{IN} = .4 to VCC
I_{OL}	Output Leakage (inactive)	---	50	µA	V_{OUT} = .4 to VCC
V_{IH}	Input High Voltage	2.0	---	V	
V_{IL}	Input Low Voltage	---	0.8	V	
V_{OH}	Output High Voltage	2.4	---	V	I_O = -400 µA
V_{OL1}	Output Low Voltage (TGS, IGS)	---	0.4	V	I_O = 7.0 mA
V_{OL2}	Output Low Voltage (all others)	---	0.4	V	I_O = 4.0 mA
I_{CC}	Supply Current	---	36	mA	T_A = +25°C

9.0 TIMING CHARACTERISTICS

Timing characteristics are valid over the entire operating temperature (0 to 70 deg. C) and voltage (4.75 to 5.25 Volts) ranges. All pins are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, except for SCSI bus pins, which are referenced to 1.5 volts. All outputs are assumed to have a load capacitance of 50 picofarads.

Many of the timing parameters that follow are defined in terms of an internal clock cycle time that is determined by the input clock and the clock divisor selected in the OWN ID register. This cycle time is calculated as follows:

Tcyc =Tcp * DIVISOR/ 2

where:

Tcyc is the internal clock cycle time;
Tcp is the period of the clock at the CLK input;
DIVISOR is the clock divisor selected in the OWN ID register.

For example, with a 16MHz clock input to the 33C92A, the clock divisor selected would be 4. Therefore, the value of Tcyc would be:

Tcyc = 62.5 nsec * 4/ 2 = 125 nsec

9.1 Processor/DMA Interface

9.1.1 CLK

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tcp	CLOCK PERIOD	50	125	ns
tch	CLOCK HIGH	20		ns
tcl	CLOCK LOW	20		ns

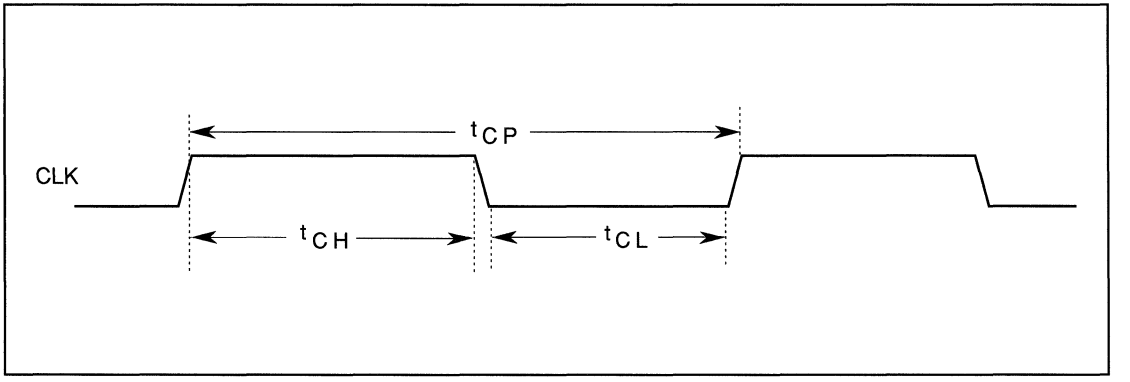


FIGURE 4. CLOCK TIMING

9.1.2 MR-

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tmr	MR- PULSE WIDTH	1		µs

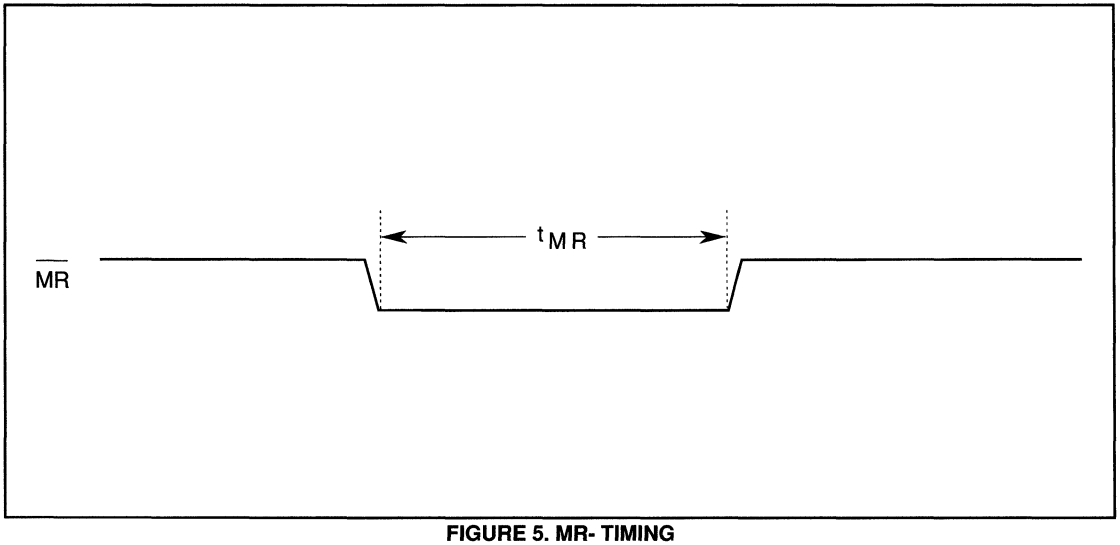


FIGURE 5. MR- TIMING

9.1.3 Processor Write (Indirect Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tavwl	A0 VALID TO WE- LOW	0		ns
tclwl	CS- LOW TO WE- LOW	0		ns
twe	WE- PULSE WIDTH	120		ns
tdvwh	DATA VALID TO WE- HIGH	70		ns
twhai	WE- HIGH TO A0 INVALID	0		ns
twhch	WE- HIGH TO CS- HIGH	0		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
twhwl	WE- HIGH TO WE- OR RE- LOW	100		ns

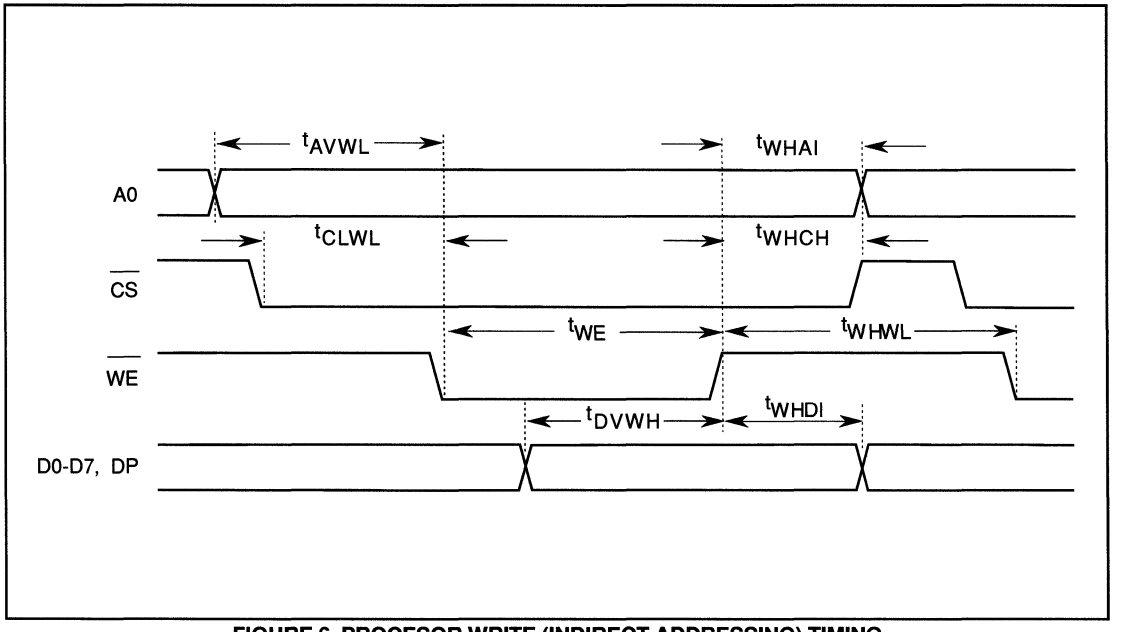


FIGURE 6. PROCESOR WRITE (INDIRECT ADDRESSING) TIMING

9.1.4 Processor Read (Indirect Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tavrl	A0 VALID TO RE- LOW	0		ns
tclrl	CS- LOW TO RE- LOW	0		ns
tre	RE- PULSE WIDTH	180	10000	ns
trldv	RE- LOW TO DATA VALID	---	180	ns
trhch	RE- HIGH TO CS- HIGH	0		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
trhrl	RE- HIGH TO RE- OR WE- LOW	100		ns
trhai	RE- HIGH TO A0 INVALID	0		ns

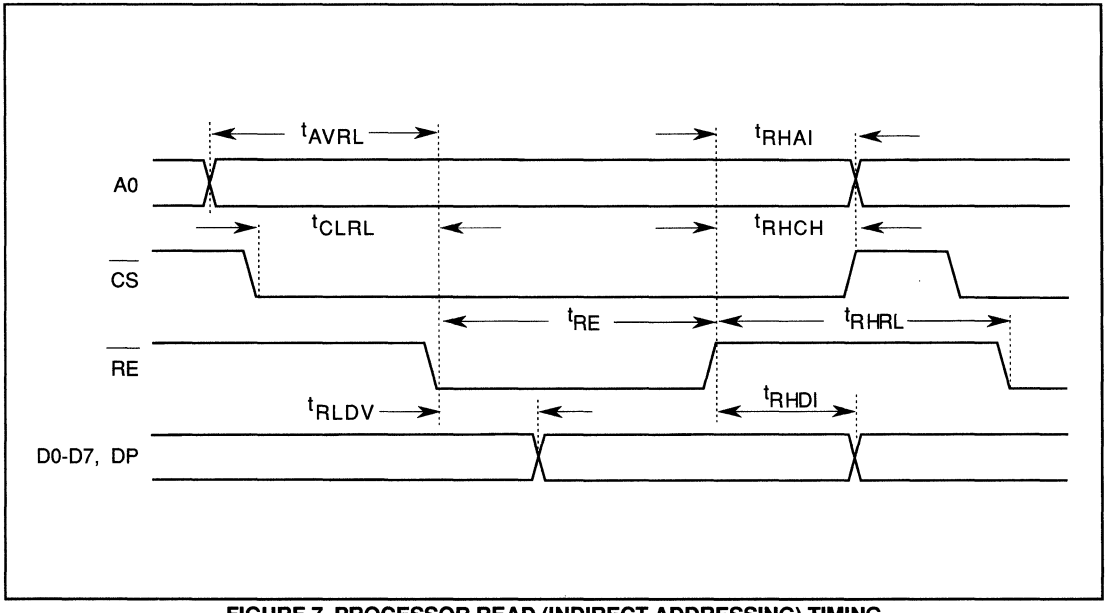


FIGURE 7. PROCESSOR READ (INDIRECT ADDRESSING) TIMING

9.1.5 Processor Write (Direct Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
taval	ADDR VALID TO ALE LOW	40		ns
talai	ALE LOW TO ADDR INVALID	0		ns
talwl	ALE LOW TO WE- LOW	90		ns
tclwl	CS- LOW TO WE- LOW	0		ns
twe	WE- PULSE WIDTH	120		ns
tdvwh	DATA VALID TO WE- HIGH	70		ns
twhch	WE- HIGH TO CS- HIGH	0		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
twhwl	WE- HIGH TO WE- OR RE- LOW	100		ns
tahal	ALE HIGH TO ALE LOW	---	1	µs

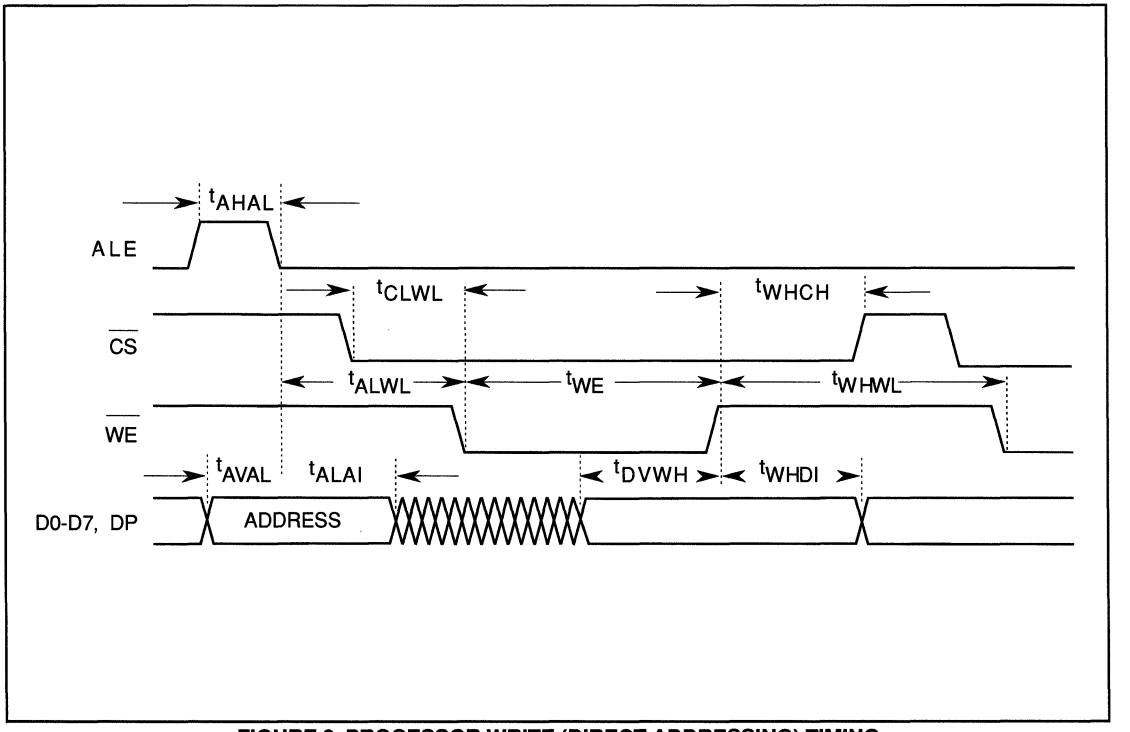


FIGURE 8. PROCESSOR WRITE (DIRECT ADDRESSING) TIMING

9.1.6 Processor Read (Direct Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
taval	ADDR VALID TO ALE LOW	40		ns
talai	ALE LOW TO ADDR INVALID	0		ns
talrl	ALE LOW TO RE- LOW	30		ns
tclrl	CS- LOW TO RE- LOW	0		ns
tre	RE- PULSE WIDTH	180	10000	ns
trldv	RE- LOW TO DATA VALID		180	ns
trhch	RE- HIGH TO CS- HIGH	0		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
trhrl	RE- HIGH TO RE- OR WE- LOW	100		ns
tahal	ALE HIGH TO ALE LOW		1	µs

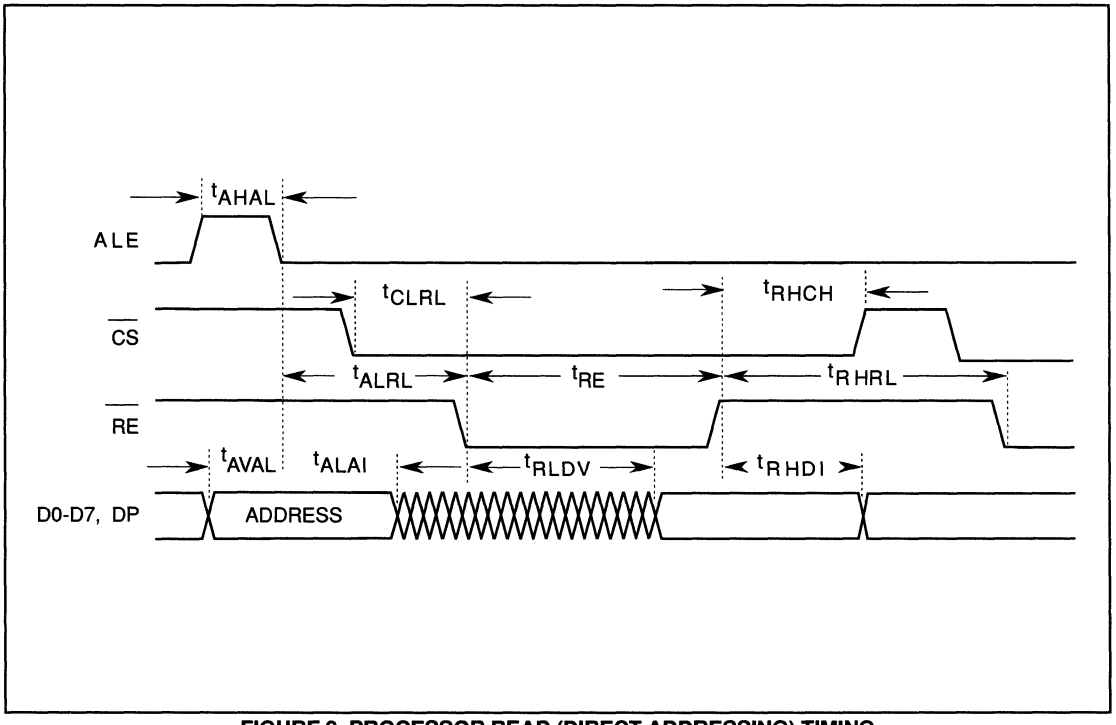


FIGURE 9. PROCESSOR READ (DIRECT ADDRESSING) TIMING

9.1.7 DMA Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlwl	DACK- LOW TO WE- LOW	0		ns
tdlqh	DACK- LOW TO DRQ- HIGH		75	ns
twr	WE- PULSE WIDTH	50		ns
twhwl	WE- HIGH TO WE- LOW	100		ns
tdvwh	DATA VALID TO WE- HIGH	25		ns
twhdh	WE- HIGH TO DACK- HIGH	0		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
tdhql	DACK- HIGH TO DRQ- LOW	0		ns

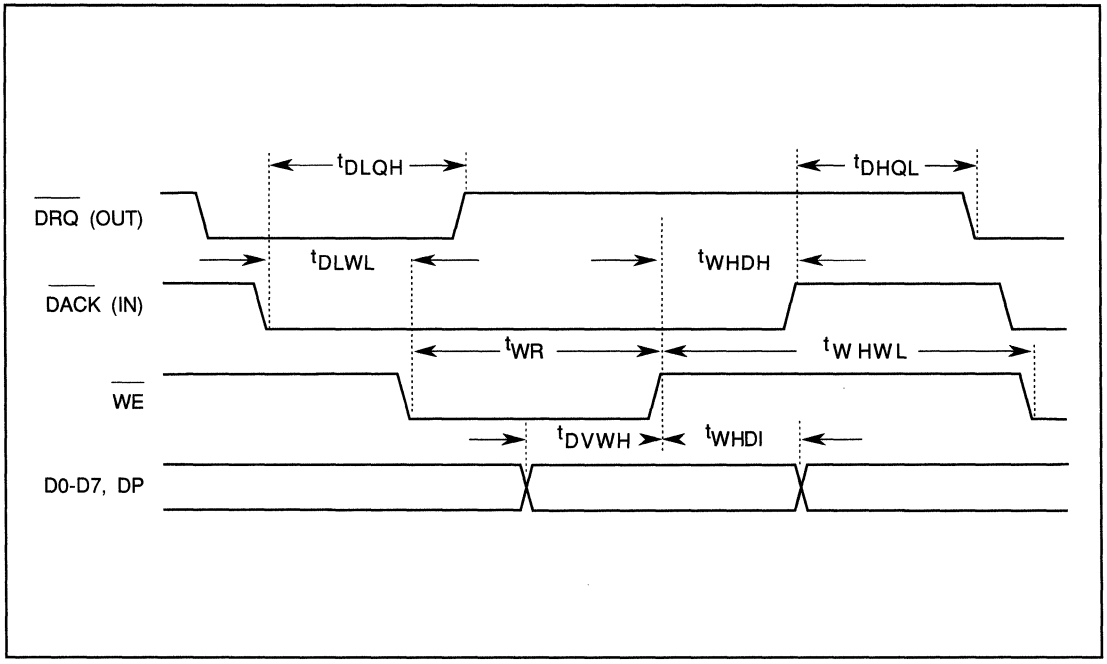


FIGURE 10. DMA WRITE

9.1.8 DMA Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlrl	DACK- LOW TO RE- LOW	0		ns
tdlqh	DACK- LOW TO DRQ- HIGH		75	ns
trd	RE- PULSE WIDTH	80		ns
trhrl	RE- HIGH TO RE- LOW	100		ns
trldv	RE- LOW TO DATA VALID		70	ns
trhdh	RE- HIGH TO DACK- HIGH	0		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
tdhql	DACK- HIGH TO DRQ- LOW	0		ns

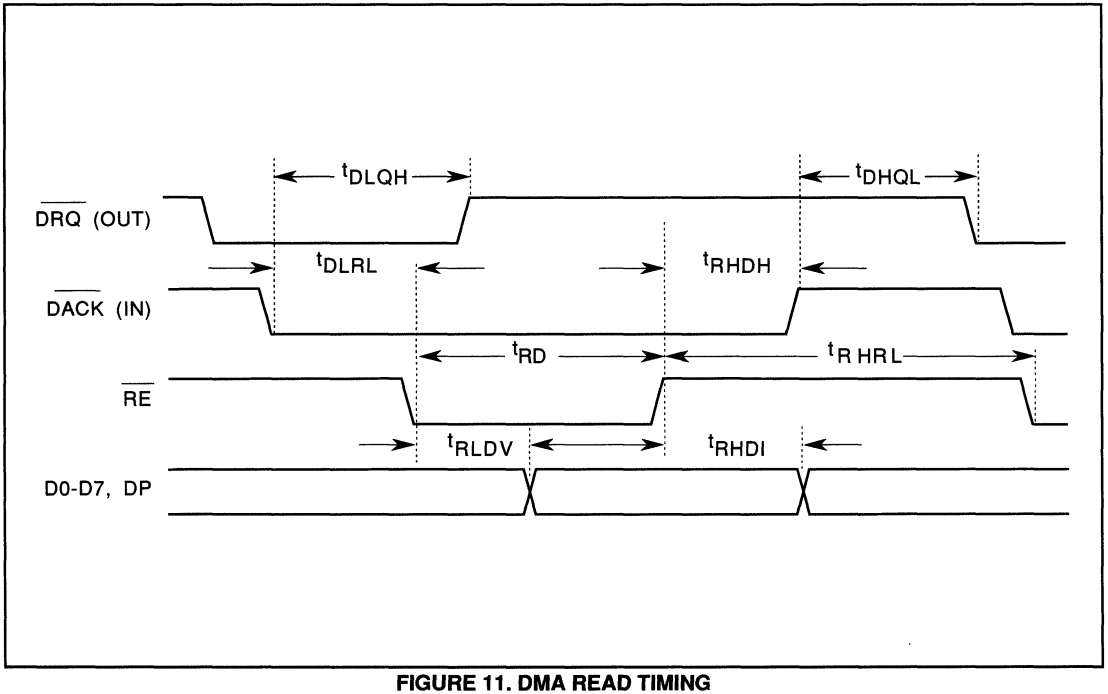


FIGURE 11. DMA READ TIMING

9.1.9 Bus Buffer Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tqhsl	DRQ HIGH TO RCS- LOW	0	40	ns
tslwv	RCS- LOW TO WE- VALID	-5	20	ns
two	WE- PULSE WIDTH	1-20ns		Tcyc
twldv	WE- LOW TO DATA VALID		50	ns
twhdi	WE- HIGH TO DATA INVALID	10		ns
twhwl	WE- HIGH TO WE- LOW	1-20ns		Tcyc
tqlsh	DRQ LOW TO RCS- HIGH	8	10	Tcyc
tshwi	RCS- HIGH TO WE- INVALID		100	ns
twhsh	WE- HIGH TO RCS- HIGH	0		ns
tslwl	RCS- LOW TO WE- LOW	60		ns
tqlwl	DRQ LOW TO WE- LOW (1)	0		ns
tslql	RCS- LOW TO DRQ LOW (2)		100	ns

(1) Guarantees that only one more byte will be transferred.

(2) Guarantees that only one byte will be transferred.

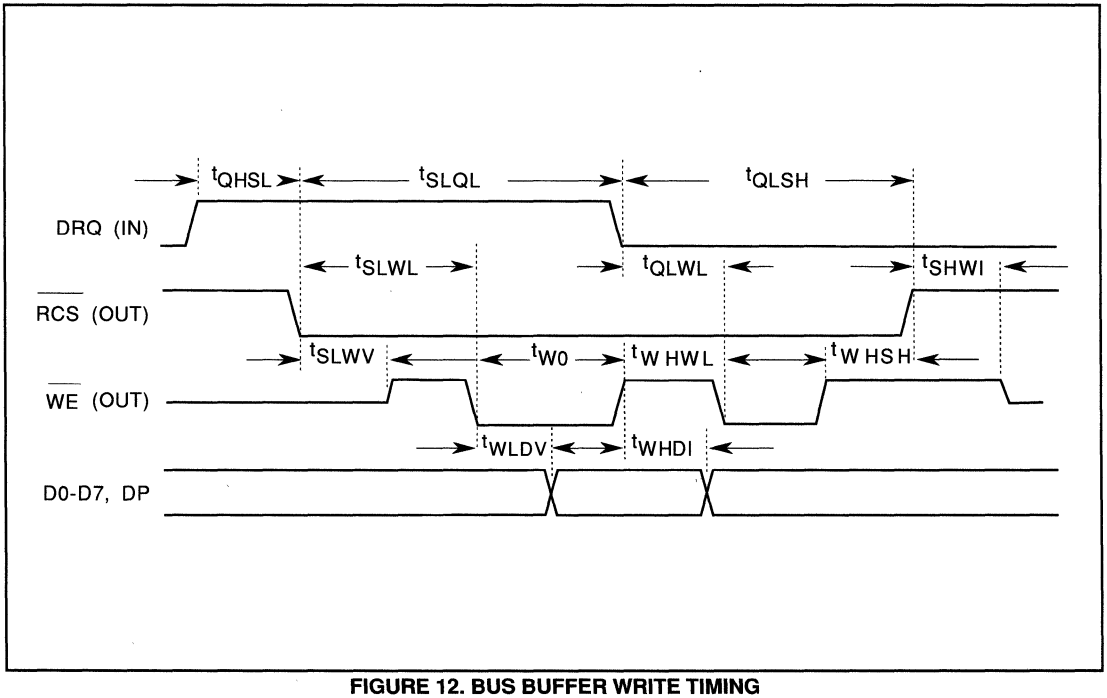


FIGURE 12. BUS BUFFER WRITE TIMING

9.1.10 Bus Buffer Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tqhsl	DRQ HIGH TO RCS- LOW	0	40	ns
tslrv	RCS- LOW TO RE- VALID	-5	20	ns
tro	RE- PULSE WIDTH	1-20ns		Tcyc
tdvrh	DATA VALID TO RE- HIGH	20		ns
trhdi	RE- HIGH TO DATA INVALID	0		ns
trhrl	RE- HIGH TO RE- LOW	1-20ns		Tcyc
tqlsh	DRQ LOW TO RCS- HIGH	8	10	Tcyc
tshri	RCS- HIGH TO RE- INVALID		100	ns
trhsh	RE- HIGH TO RCS- HIGH	0		ns
tslrl	RCS- LOW TO RE- LOW	60		ns
tqlrl	DRQ LOW TO RE- LOW (1)	0		ns
tslql	RCS- LOW TO DRQ LOW (2)		100	ns

(1) Guarantees that only one more byte will be transferred.

(2) Guarantees that only one byte will be transferred.

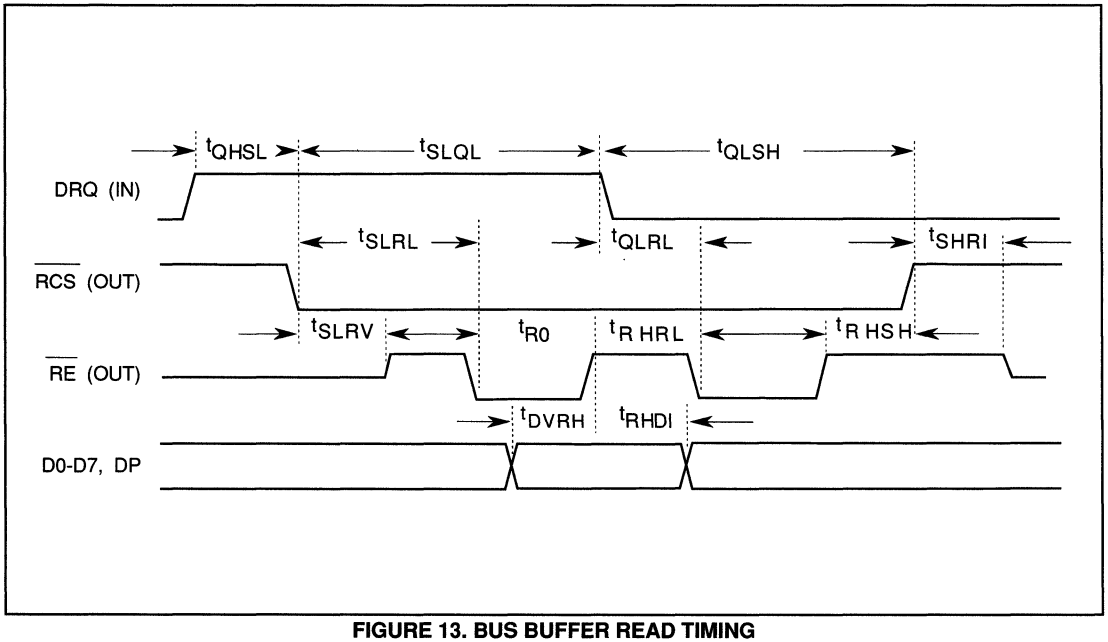


FIGURE 13. BUS BUFFER READ TIMING

9.1.11 Burst DMA Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlwl	DACK- LOW TO WE- LOW	0		ns
twlqh	WE- LOW TO DRQ- HIGH		75	ns
twr	WE- PULSE WIDTH	50		ns
twhwl	WE- HIGH TO WE- LOW	80		ns
tdvwh	DATA VALID TO WE- HIGH	25		ns
twhdh	WE- HIGH TO DACK- HIGH	0		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
tqhql	DRQ- HIGH TO DRQ- LOW	0.5		Tcyc

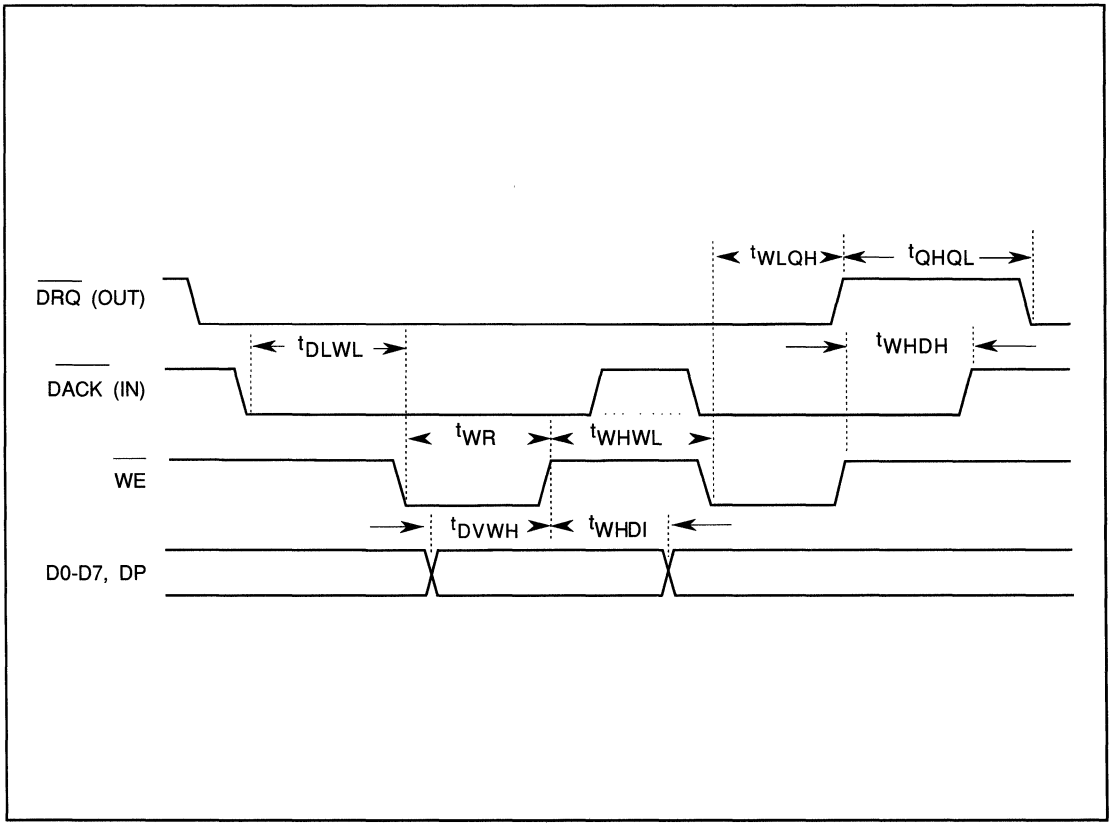


FIGURE 14. BURST DMA WRITE TIMING

9.1.12 Burst DMA Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlrl	DACK- LOW TO RE- LOW	0		ns
trlqh	RE- LOW TO DRQ- HIGH		75	ns
trd	RE- PULSE WIDTH	80		ns
trhrl	RE- HIGH TO RE- LOW	80		ns
trldv	RE- LOW TO DATA VALID		50	ns
trhdh	RE- HIGH TO DACK- HIGH	0		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
tqhql	DRQ- HIGH TO DRQ- LOW	0.5		Tcyc

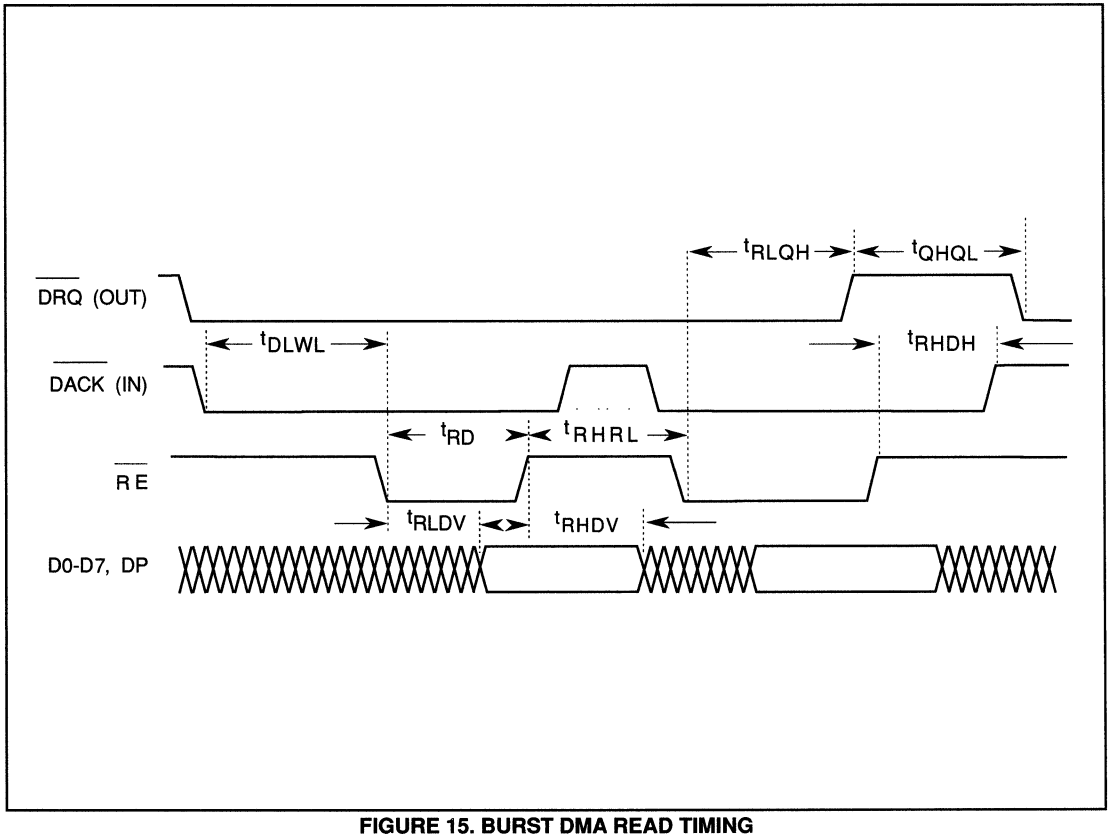


FIGURE 15. BURST DMA READ TIMING

9.1.13 INTRQ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tihrl	INTRQ HIGH TO RE- LOW	0		ns
tri	RE- PULSE WIDTH	180		ns
trhil	RE- HIGH TO INTRQ LOW	0	100	ns
tilih	INTRQ LOW TO INTRQ HIGH	100		ns

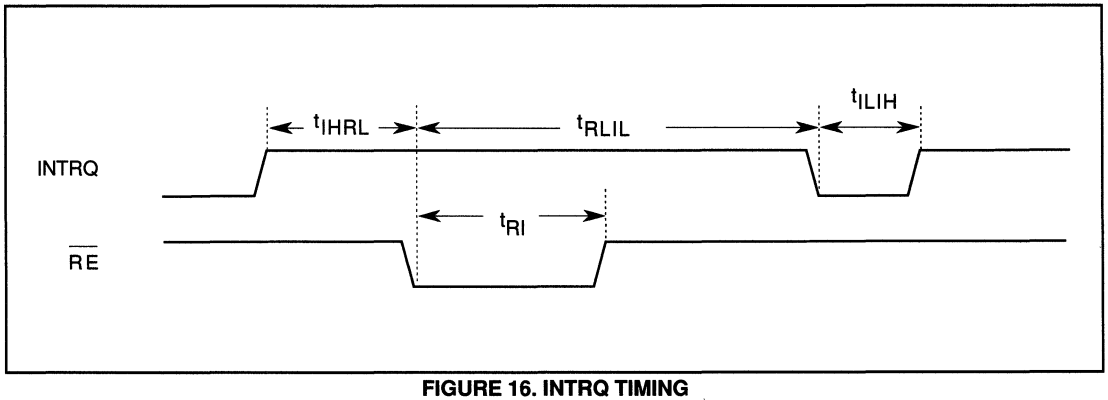


FIGURE 16. INTRQ TIMING

9.2 SCSI Interface

9.2.1 Arbitration

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tblel	BSYI, SELI LOW TO SDIE LOW	4		Tcyc
telio	SDIE LOW TO BUS ID OUT	1		Tcyc
tioah	BUS ID OUT TO ARBLD HIGH	1		Tcyc
tahdf	ARBLD HIGH TO DATA FLOAT	1		Tcyc
tdfeh	DATA FLOAT TO SDIE, SDOE HIGH	1		Tcyc
tblbh	BSYI, SELI LOW TO BSYO HIGH	12	17	Tcyc
tbheh	BSYO HIGH TO SDIE, SDOE HIGH	0	200	ns
tbhsh	BSYO HIGH TO SELO HIGH	2.2		µs

28

NOTE:
I/O* = I/O, C/D, MSG, REQ; ATN* = ATN, ACK

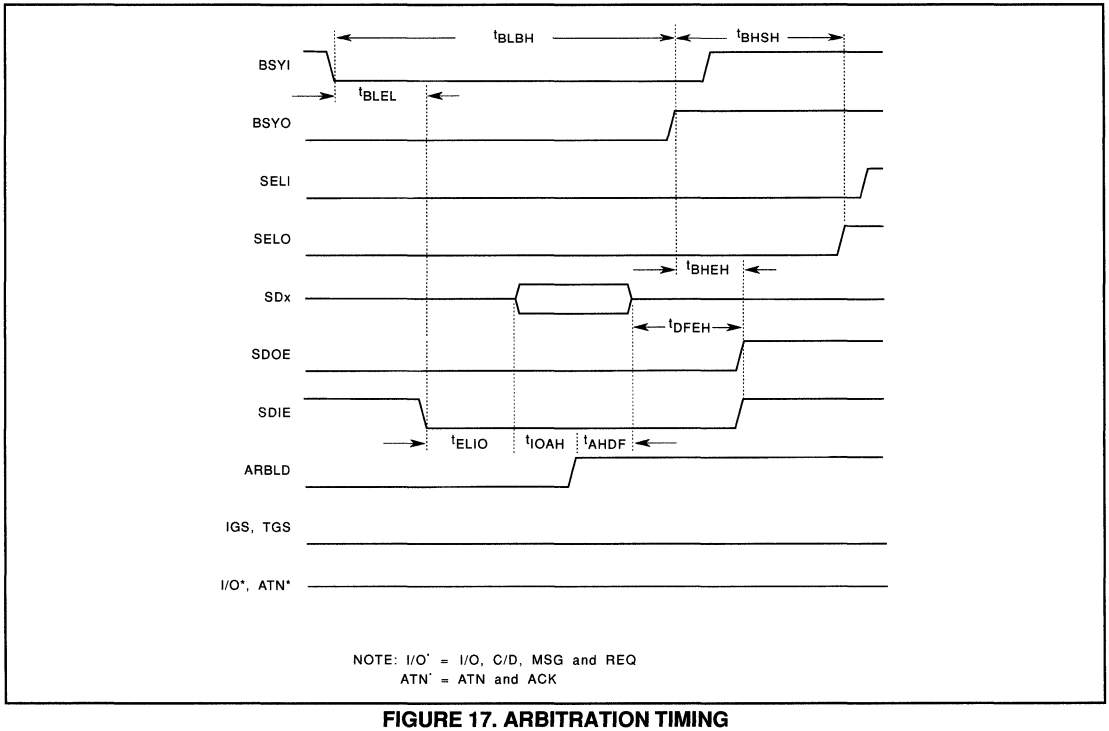


FIGURE 17. ARBITRATION TIMING

9.2.2 Selection (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshel	SELO HIGH TO SDIE LOW	1.2		µs
teloo	SDIE LOW TO "OR-ED" ID OUT	100		ns
tovgh	"OR-ED" ID OUT VALID TO IGS HIGH	100		ns
taogh	ATN, ACK OUT TO IGS HIGH	100		ns
tghav	IGS HIGH TO ATN VALID	400		ns
tavbl	ATN, ACK VALID OUT TO BSYO LOW	100		ns
tblbv	BSYO LOW TO BSY HIGH VALID	400		ns
tbhsl	BSYI HIGH TO SELO LOW	100		ns

NOTE:
I/O* = I/O, C/D, MSG, REQ; SDIE* = SDIE, ARBLD

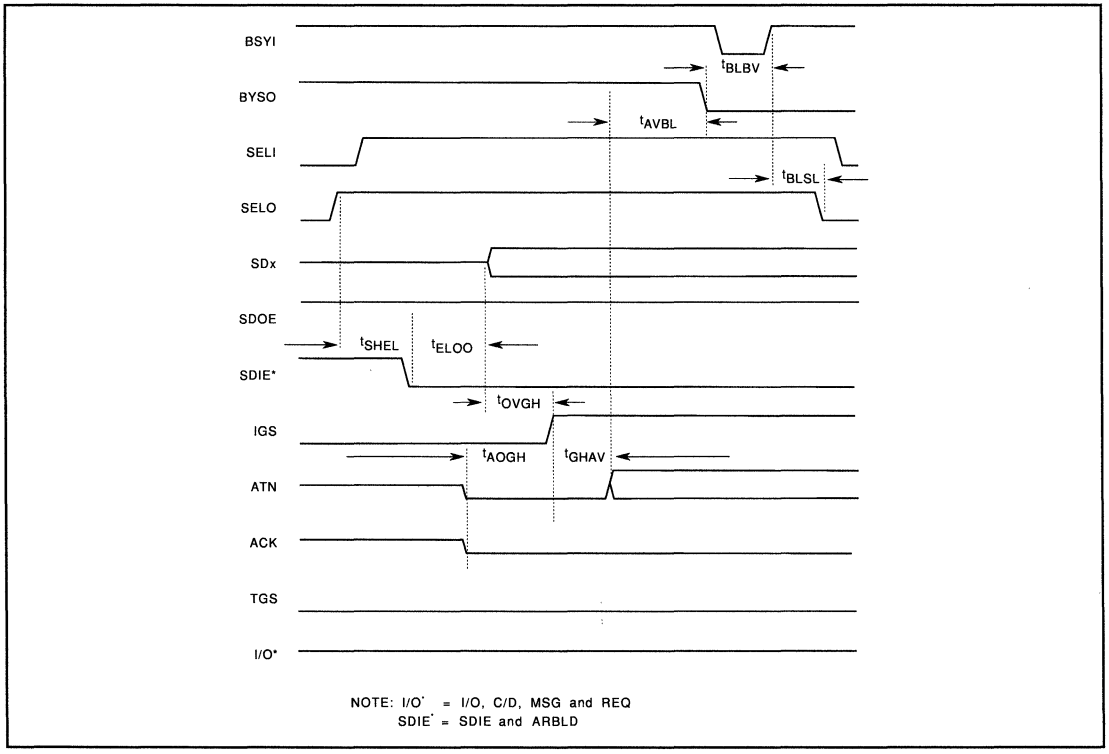


FIGURE 18. SELECTION (INITIATOR) TIMING

9.2.3 Selection (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshbl	SELI HIGH TO BSYI LOW	0		ns
tivbl	"OR-ED" ID VALID IN TO BSYI LOW	0		ns
tblbh	SELI HIGH, ID VALID, BSYI LOW TO BSYO HIGH	0.4	200	µs
tbhoi	BSYO HIGH TO "OR-ED" ID INVALID IN	0		ns
tbhsl	BSYO HIGH TO SELI LOW	0		ns
tavsl	ATN VALID IN TO SELI LOW	0		ns
tslio	SELI LOW TO I/O OUT	100		ns
tivgh	I/O OUT VALID TO TGS HIGH	100		ns

NOTE:
I/O* = I/O, C/D, MSG, REQ; SDOE* = SDOE, ARBLD

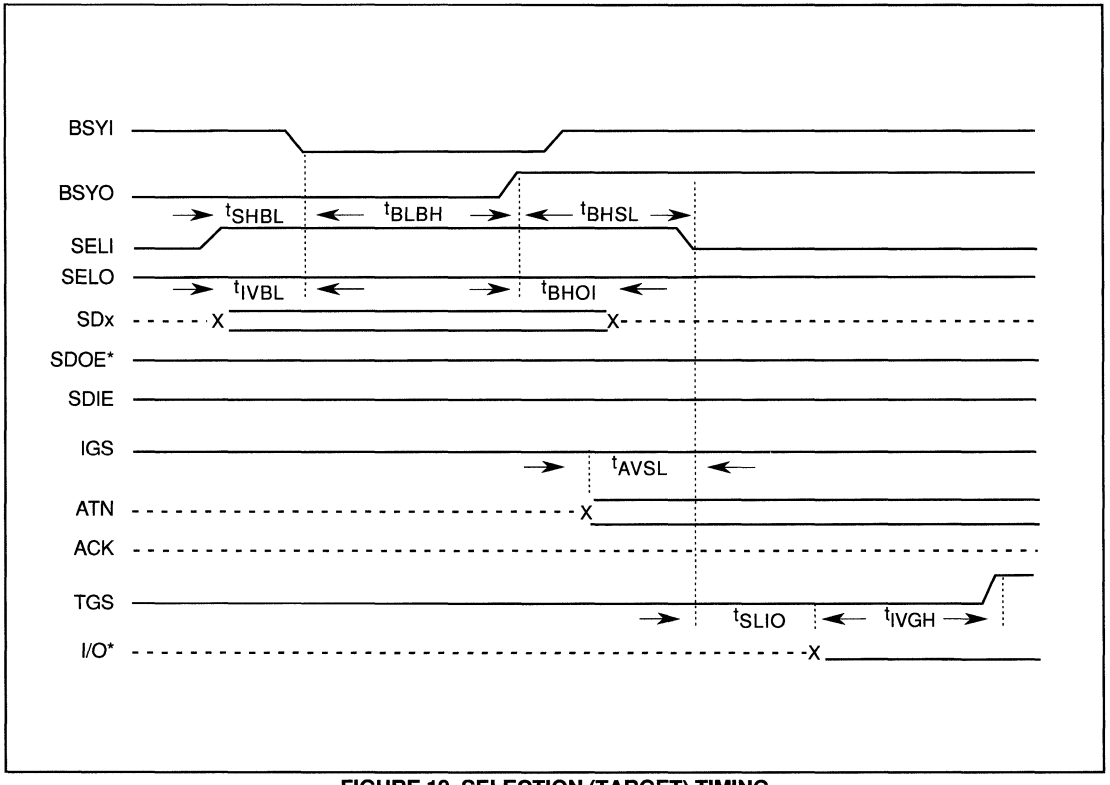


FIGURE 19. SELECTION (TARGET) TIMING

9.2.4 Reselection (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshel	SELO HIGH TO SDIE LOW	1.2		µs
teloo	SDIE LOW TO "OR-ED" ID OUT	100		ns
tovgh	"OR-ED" ID OUT VALID TO TGS HIGH	0		ns
tilgh	I/O, C/D OUT TO TGS HIGH	100		ns
tghih	TGS HIGH I/O HIGH	400		ns
tivbl	I/O, C/D OUT VALID TO BSYO LOW	100		ns
tblbv	BSYO LOW TO BSYI HIGH VALID	400		ns
tbhbh	BSYI HIGH TO BSYO HIGH	0		ns
tbhsl	BSYO HIGH TO SELO LOW	100		ns

NOTE:
C/D* = C/D, MSG, REQ; ATN* = ATN, ACK; SDIE* = SDIE, ARBLD

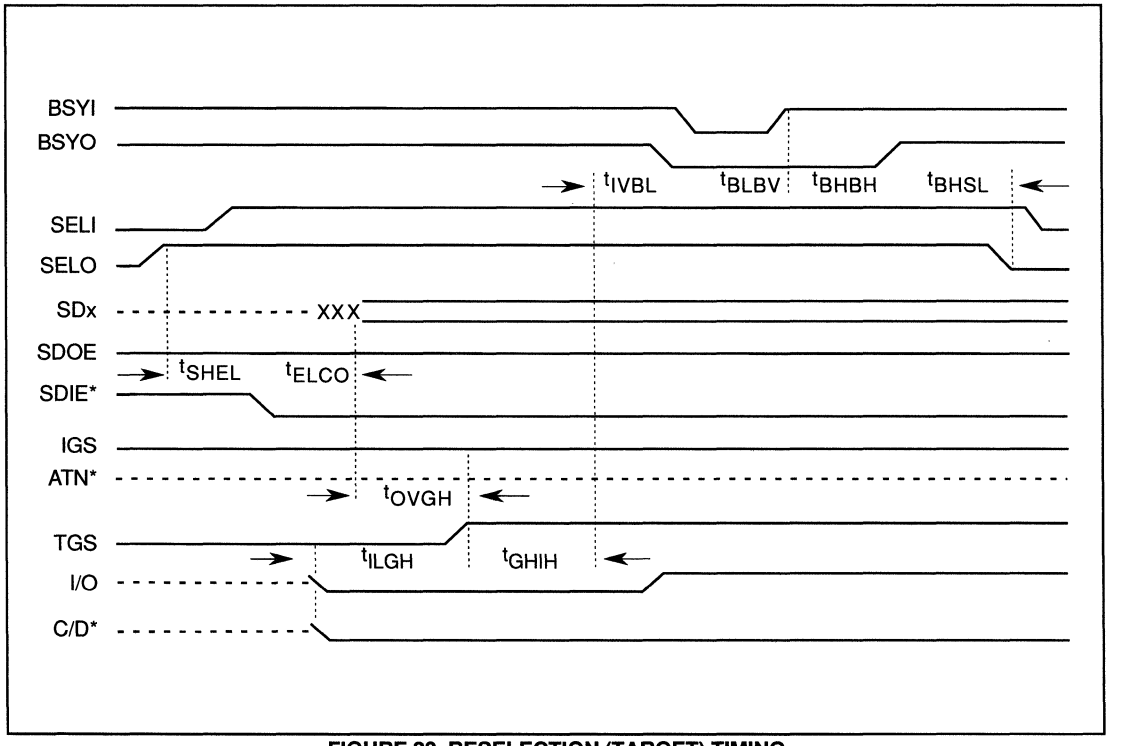


FIGURE 20. RESELECTION (TARGET) TIMING

9.2.5 Reselection (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshbl	SELI HIGH TO BSYI LOW	0		ns
tivbl	"OR-ED" ID VALID IN TO BSYI LOW	0		ns
tihbl	I/O IN HIGH TO BSYI LOW	0		ns
tblal	SELI HIGH, ID VALID, BSYI LOW TO ATN LOW	0		ns
tghao	IGS HIGH TO ATN OUT	100		ns
talgh	ATN LOW TO IGS HIGH	400		ns
tihbh	IGS HIGH TO BSYO HIGH	100		ns
tblbh	BSYI LOW TO BSYO HIGH	0.4	200	ns
tbhoi	BSYO HIGH TO "OR-ED" INVALID IN	0		ns
tbhsl	BSYO HIGH TO SELI LOW	0		ns
tslbl	SELI LOW TO BSYO LOW	0		ns

NOTE:
ATN* = ATN, ACK; SDOE* = SDOE, ARBLD, SELO; C/D* = C/D, MSG, REQ

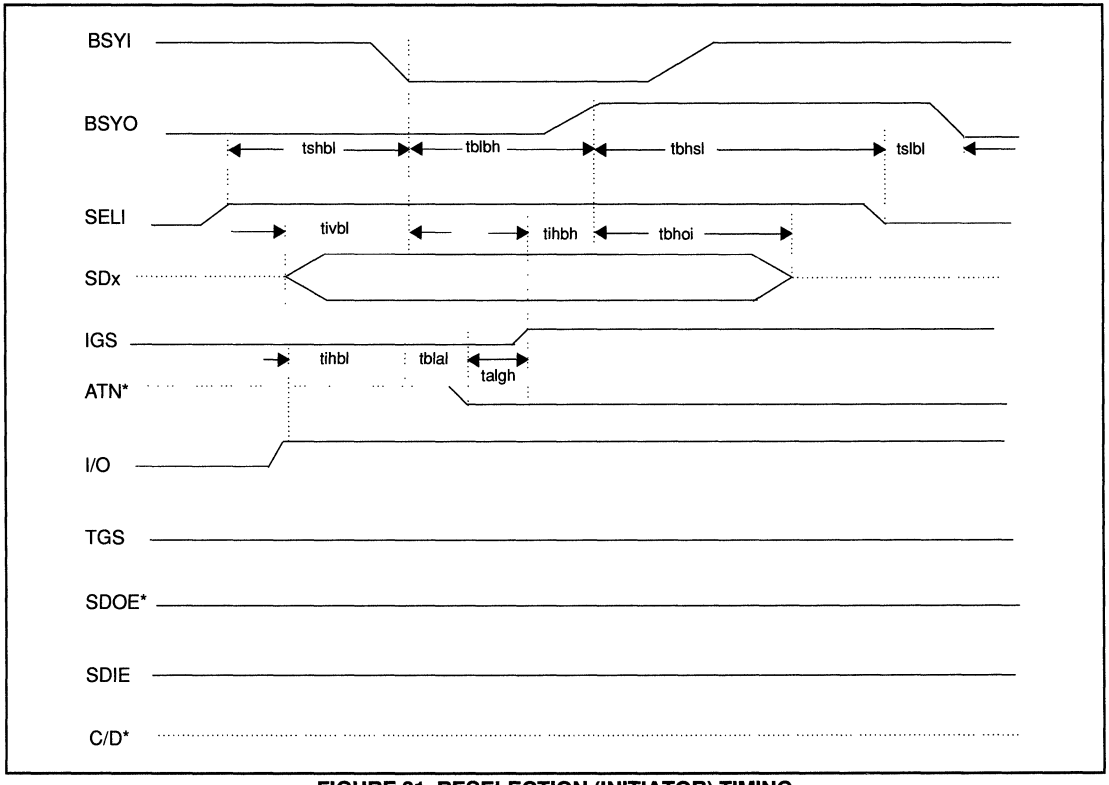


FIGURE 21. RESELECTION (INITIATOR) TIMING

9.2.6 Asynchronous Information Transfer In (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslpc	SELI LOW TO PHASE CHANGE IN	0		ns
tihol	I/O IN HIGH TO SDOE LOW, DATA BUS TRISTATE	0	125	ns
tdtih	DATA BUS TRISTATE TO SDIE HIGH	-10		ns
tpcrh	PHASE CHANGE IN TO REQ IN HIGH	350		ns
tdvrh	DATA VALID IN TO REQ IN HIGH	0		ns
trhah	REQ IN HIGH TO ACK OUT HIGH	0	175	ns
tahrl	ACK OUT HIGH TO REQ IN LOW	0		ns
trlal	REQ IN LOW TO ACK OUT LOW	0	175	ns
tahdi	ACK OUT HIGH TO DATA INVALID IN	0		ns
talpc	ACK OUT LOW TO PHASE CHANGE IN	0		ns

NOTE:
C/D* = C/D, MSG

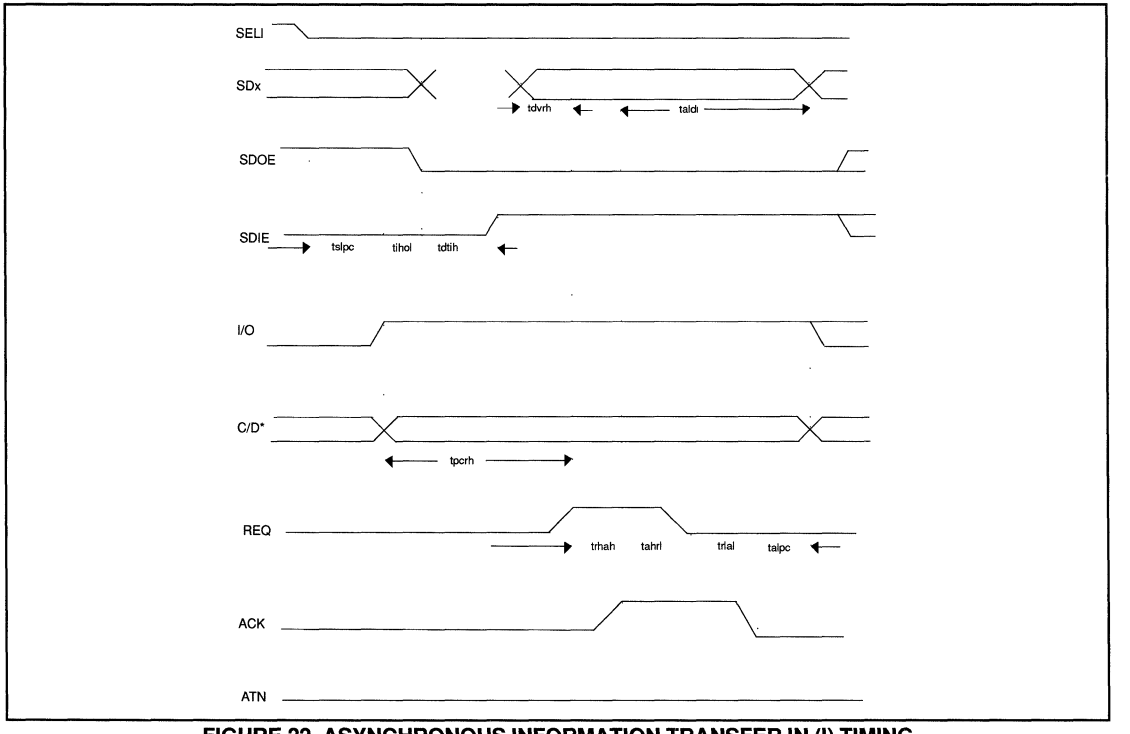


FIGURE 22. ASYNCHRONOUS INFORMATION TRANSFER IN (I) TIMING

9.2.7 Asynchronous Information Transfer In (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslpc	SELI LOW TO PHASE CHANGE OUT	100		ns
tihil	I/O OUT HIGH TO SDIE LOW	0		ns
tiloh	SDIE LOW TO SDOE HIGH, DATA OUT	30		ns
tdvrh	DATA OUT VALID TO REQ OUT HIGH	80		ns
tpcrh	PHASE CHANGE OUT TO REQ OUT HIGH	500		ns
trhah	REQ OUT HIGH TO ACK IN HIGH	0		ns
tahrl	ACK IN HIGH TO REQ OUT LOW	0	175	ns
tahdi	ACK IN HIGH TO DATA OUT INVALID	0		ns
trlal	REQ OUT LOW TO ACK IN LOW	0		ns
talpc	ACK IN LOW TO PHASE CHANGE OUT	100		ns

28

NOTE: C/D* = C/D, MSG

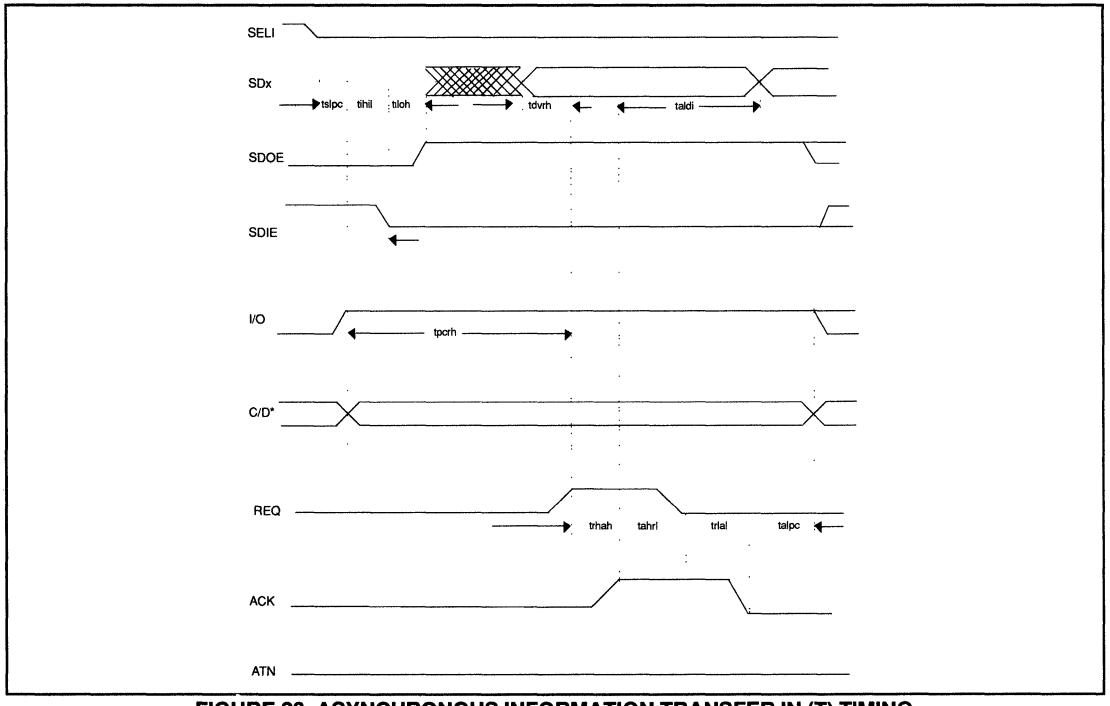


FIGURE 23. ASYNCHRONOUS INFORMATION TRANSFER IN (T) TIMING

9.2.8 Asynchronous Information Transfer Out (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslpc	SELI LOW TO PHASE CHANGE IN	0		ns
tilil	I/O IN LOW TO SDIE LOW	0		ns
tiloh	SDIE LOW TO SDOE HIGH, DATA OUT	30		ns
tpcrh	PHASE CHANGE IN TO REQ IN HIGH	350		ns
trhah	REQ IN HIGH TO ACK OUT HIGH	0	175	ns
tdvah	DATA OUT VALID TO ACK OUT HIGH	80		ns
tahrl	ACK OUT HIGH TO REQ IN LOW	0		ns
trlal	REQ IN LOW TO ACK OUT LOW	0	175	ns
trldi	REQ IN LOW TO DATA OUT INVALID	0		ns
talpc	ACK OUT LOW TO PHASE CHANGE IN	0		ns

NOTE:
C/D* = C/D, MSG

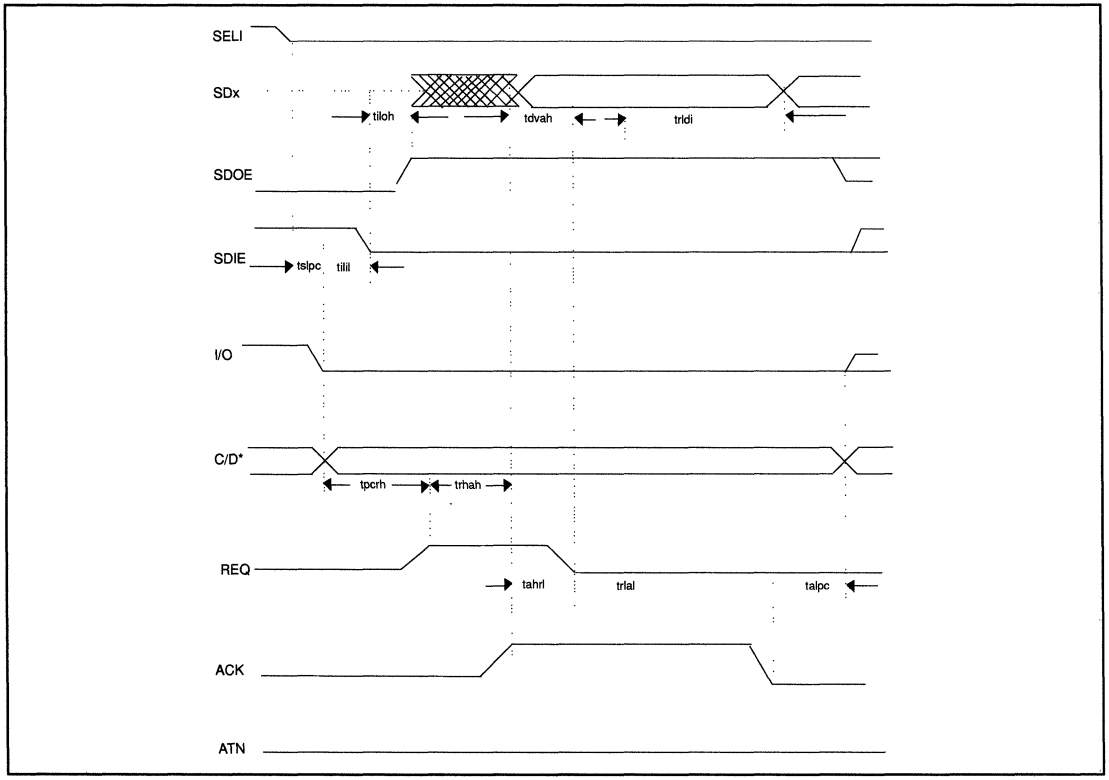


FIGURE 24. ASYNCHRONOUS INFORMATION TRANSFER OUT(I) TIMING

9.2.9 Asynchonous Information Transfer Out (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslpc	SELI LOW TO PHASE CHANGE OUT	100		ns
tilol	I/O OUT LOW TO SDOE LOW DATA BUS TRISTATE	0	125	ns
tdtih	DATA BUS TRISTATE TO SDIE HIGH	-10		ns
tpcrh	PHASE CHANGE OUT TO REQ OUT HIGH	500		ns
trhah	REQ OUT HIGH TO ACK IN HIGH	0		ns
tdvah	DATA IN VALID TO ACK IN HIGH	0		ns
tahrl	ACK IN HIGH TO REQ OUT LOW	0	175	ns
trldi	REQ OUT LOW TO DATA IN INVALID	0		ns
trlal	REQ OUT LOW TO ACK IN LOW	0		ns
talpc	ACK IN LOW TO PHASE CHANGE OUT	0		ns

NOTE:
C/D* = C/D, MSG

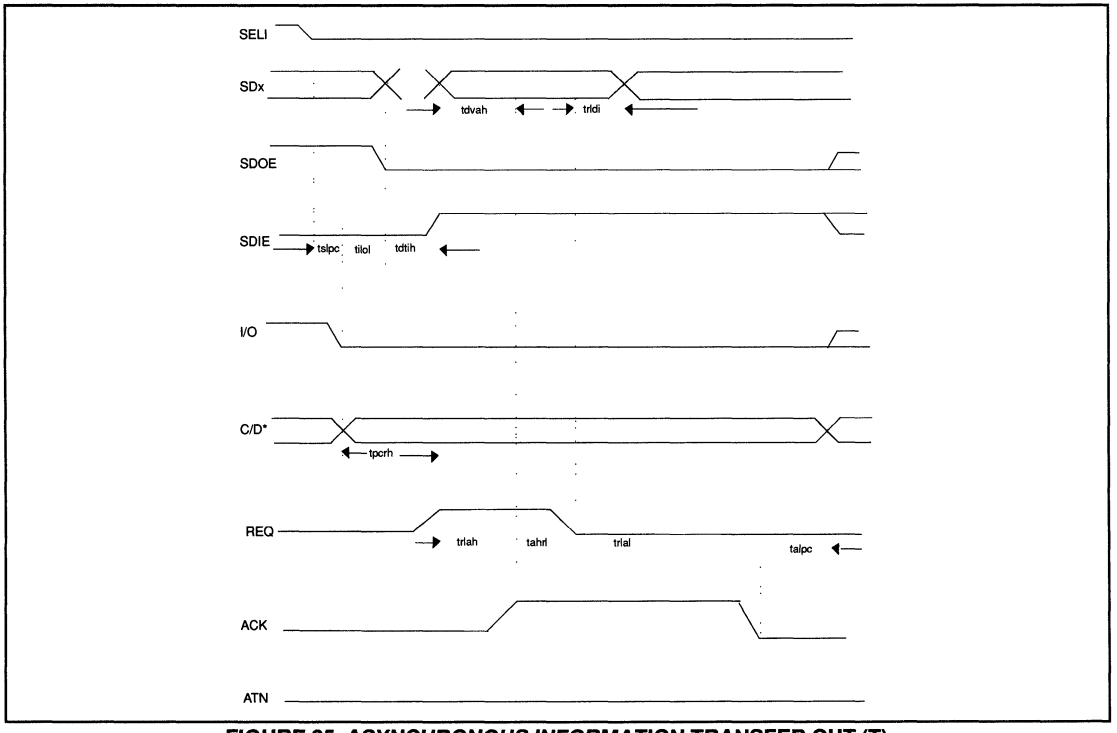


FIGURE 25. ASYNCHRONOUS INFORMATION TRANSFER OUT (T)

9.2.10 Synchronous Information Transfer In (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrh	DATA VALID IN TO REQ IN HIGH	0		ns
trhdi	REQ IN HIGH TO DATA INVALID IN	45		ns
trhrl	REQ IN HIGH TO REQ IN LOW	50		ns
trlrh	REQ IN LOW TO REQ IN HIGH	50		ns
tahal	ACK OUT HIGH TO ACK OUT LOW	1-15ns		Tcyc
talah	ACK OUT LOW TO ACK OUT HIGH	1-15ns		Tcyc
talpc	ACK OUT LOW TO PHASE CHANGE IN	0		ns

PARAMETERS tslpc, tihol, tdtih, and tpcrh ALSO APPLY (see 9.2.6).

NOTE:
C/D* = C/D, MSG

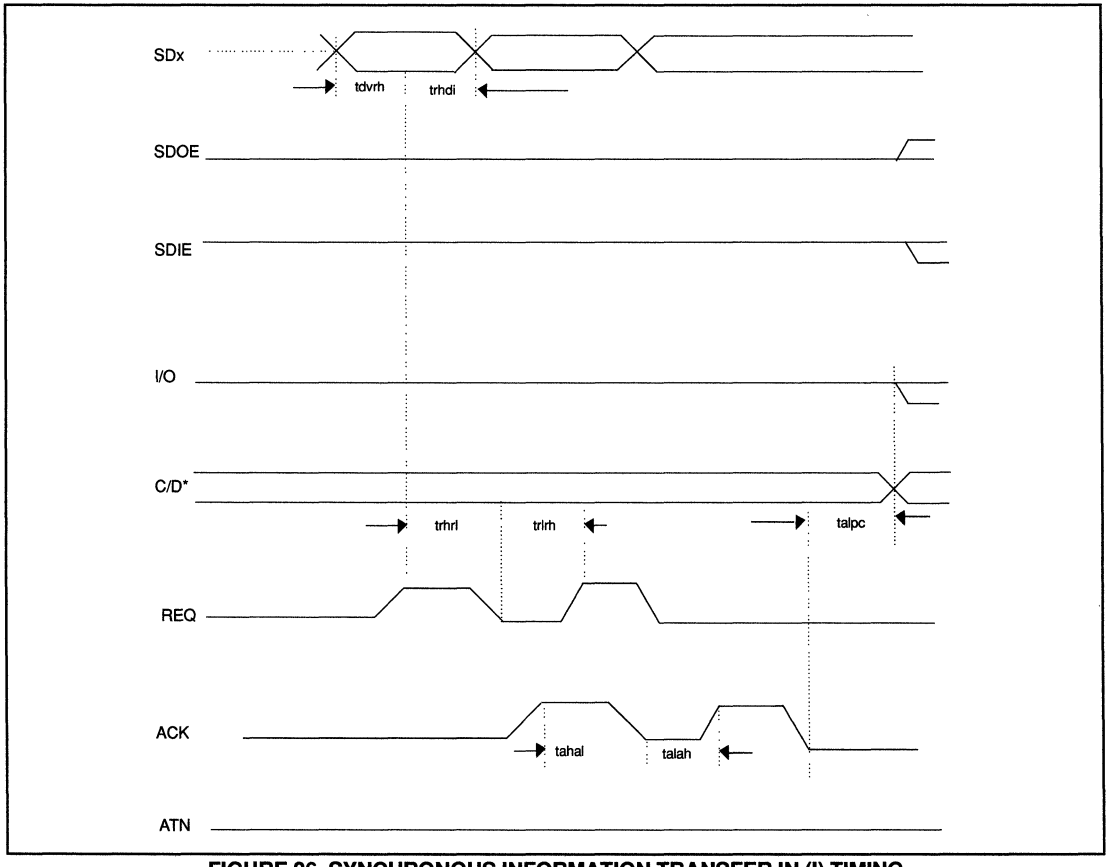


FIGURE 26. SYNCHRONOUS INFORMATION TRANSFER IN (I) TIMING

9.2.11 Synchronous Information Transfer In (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrh	DATA VALID OUT TO REQ OUT HIGH	75		ns
trhdi	REQ OUT HIGH TO DATA INVALID OUT	115		ns
trhrl	REQ OUT HIGH TO REQ OUT LOW	1-15ns		Tcyc
trlrh	REQ OUT LOW TO REQ OUT HIGH	1-15ns		Tcyc
tahal	ACK IN HIGH TO ACK IN LOW	50		ns
talah	ACK IN LOW TO ACK IN HIGH	50		ns
talpc	ACK IN LOW TO PHASE CHANGE OUT	0		ns

PARAMETERS tslpc, tihil, tiloh, and tpcrh ALSO APPLY (see 9.2.7).

NOTE:
C/D* = C/D, MSG

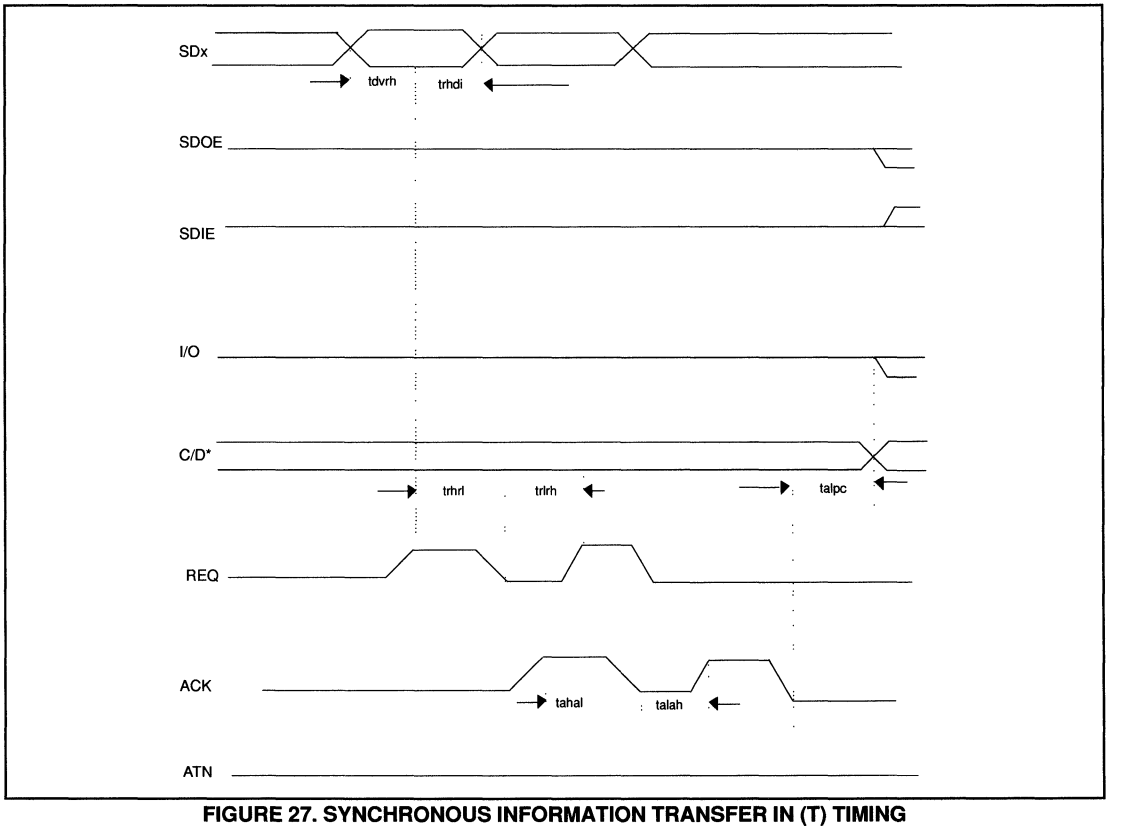


FIGURE 27. SYNCHRONOUS INFORMATION TRANSFER IN (T) TIMING

9.2.12 Synchronous Information Transfer Out (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvah	DATA VALID OUT TO ACK OUT HIGH	75		ns
tahdi	ACK OUT HIGH TO DATA INVALID OUT	115		ns
trhrl	REQ IN HIGH TO REQ IN LOW	50		ns
trlrh	REQ IN LOW TO REQ IN HIGH	50		ns
tahal	ACK OUT HIGH TO ACK OUT LOW	1-15ns		Tcyc
talah	ACK OUT LOW TO ACK OUT HIGH	1-15ns		Tcyc
talpc	ACK OUT LOW TO PHASE CHANGE IN	0		ns

PARAMETERS tslpc, tiloh, tilil, and tpcrh ALSO APPLY (see 9.2.8).

NOTE:
C/D* = C/D, MSG

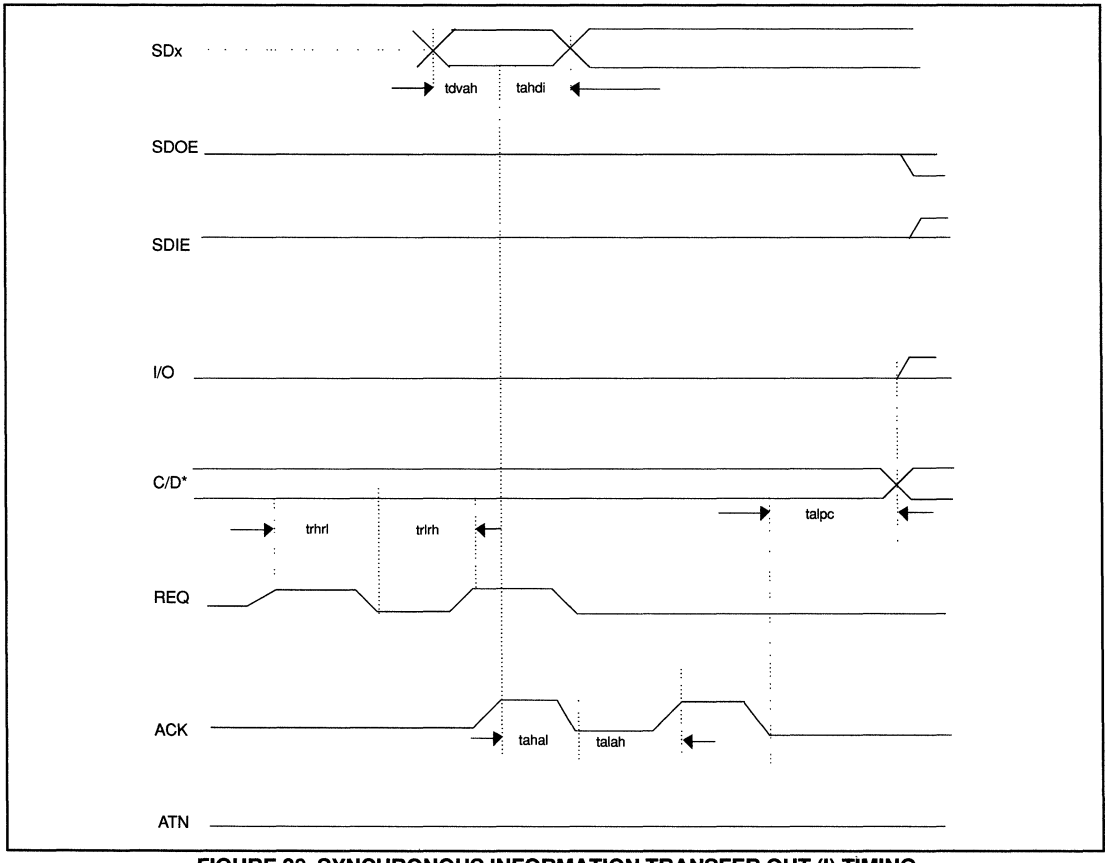


FIGURE 28. SYNCHRONOUS INFORMATION TRANSFER OUT (I) TIMING

9.2.13 Synchronous Information Transfer Out (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvah	DATA VALID IN TO ACK IN HIGH	0		ns
tahdi	ACK IN HIGH TO DATA INVALID IN	45		ns
trhrl	REQ OUT HIGH TO REQ OUT LOW	1-15ns		Tcyc
trlrh	REQ OUT LOW TO REQ OUT HIGH	1-15ns		Tcyc
tahal	ACK IN HIGH TO ACK IN LOW	50		ns
talah	ACK IN LOW TO ACK IN HIGH	50		ns
talpc	ACK IN LOW TO PHASE CHANGE OUT	0		ns

PARAMETERS tslpc, tilol, tdtih, and tpcrh ALSO APPLY (see 9.2.9).

NOTE:
C/D* = C/D, MSG

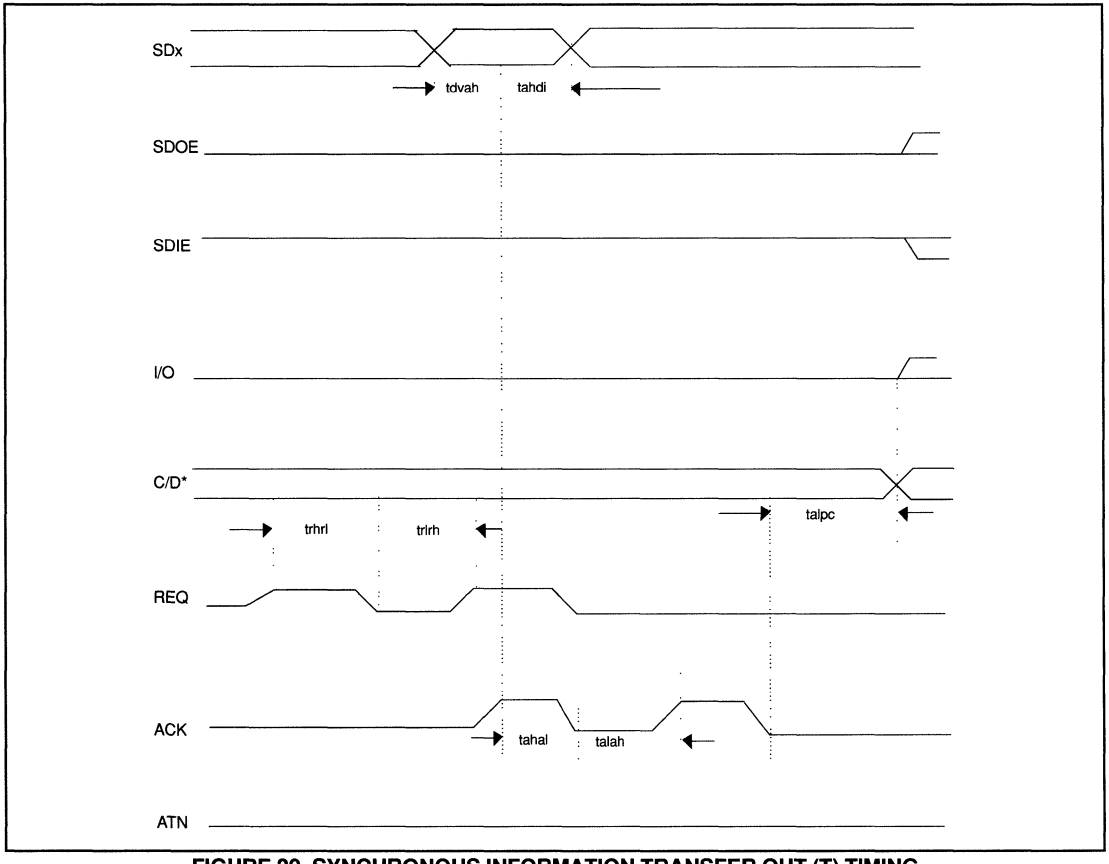


FIGURE 29. SYNCHRONOUS INFORMATION TRANSFER OUT (T) TIMING

9.2.14 Arbitration To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshbl	SELI HIGH TO BSYO, SDOE, ARBLD LOW		8+120ns|	Tcyc

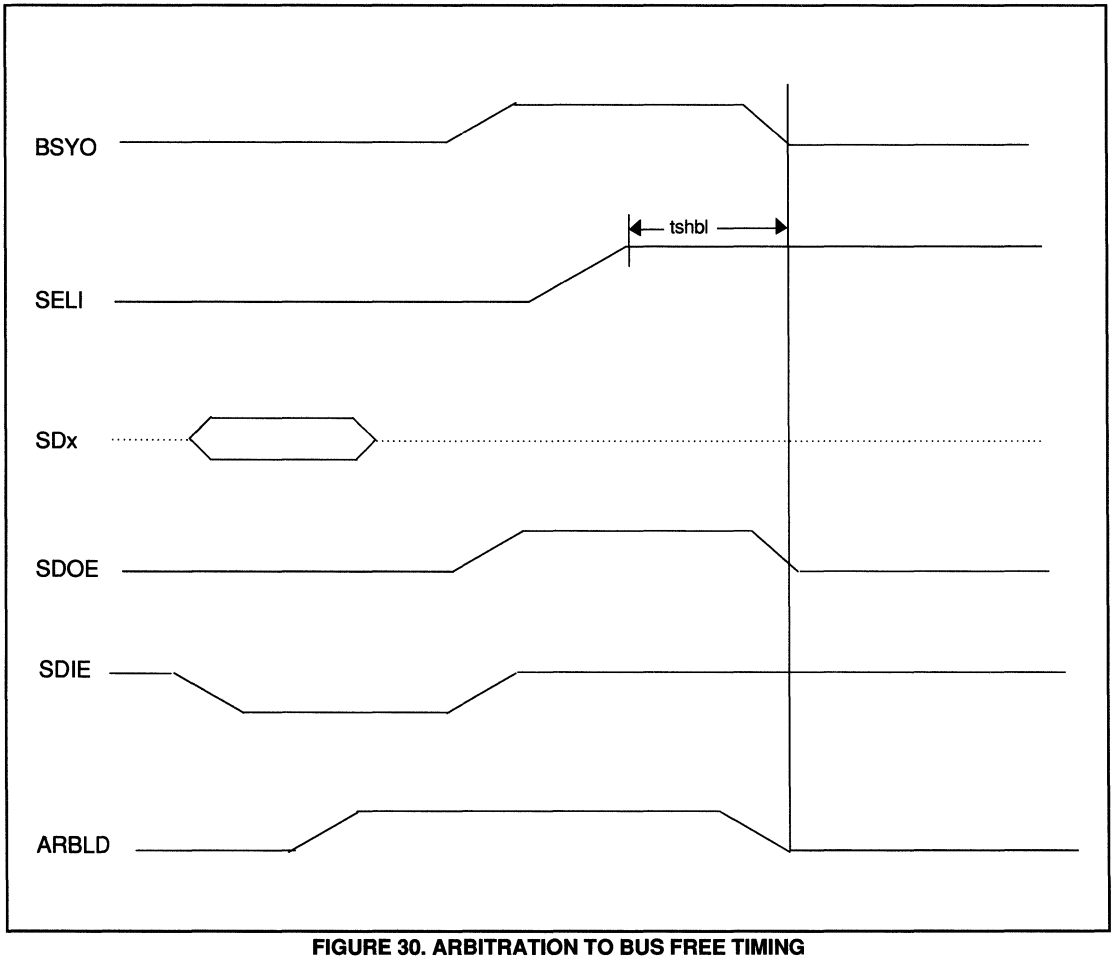


FIGURE 30. ARBITRATION TO BUS FREE TIMING

9.2.15 Selection (Initiator) Or Reselection (Target) To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
ttadc	TIMEOUT OR ABORT TO DATA BUS CLEARED*	0		ns
tdcsl	DATA BUS CLEARED* TO SELO LOW	200		µs
tslih	SELO LOW TO SDIE HIGH, SDOE LOW		8+120ns	Tcyc
tsldt	SELO LOW TO DATA BUS TRISTATE		8+120ns	Tcyc
tslgl	SELO LOW TO gs LOW, cntl TRISTATE		8+120ns	Tcyc

* SDx logic low, causing logic low on SCSI data bus.

NOTE:
gs = IGS (INITIATOR) or TGS (TARGET)
cntl = ATN, ACK (INIT) or I/O, C/D, MSG, and REQ (TARGET)

28

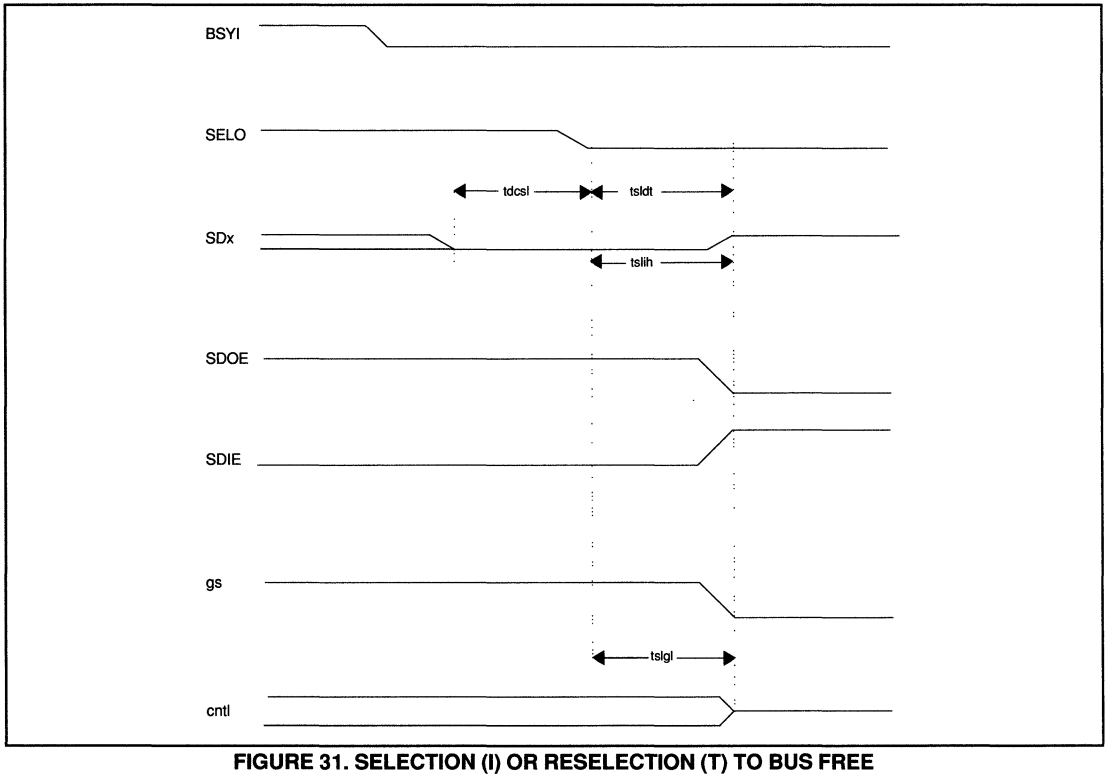


FIGURE 31. SELECTION (I) OR RESELECTION (T) TO BUS FREE

9.2.16 Connected-as-an-Initiator To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tblih	BSYI LOW TO SDIE HIGH, SDOE LOW		8+120ns	Tcyc
tbldt	BSYI LOW TO DATA BUS TRISTATE		8+120ns	Tcyc
tblgl	BSYI LOW TO IGS LOW, ATN TRISTATE		8+120ns	Tcyc

NOTE:
ATN* = ATN, ACK

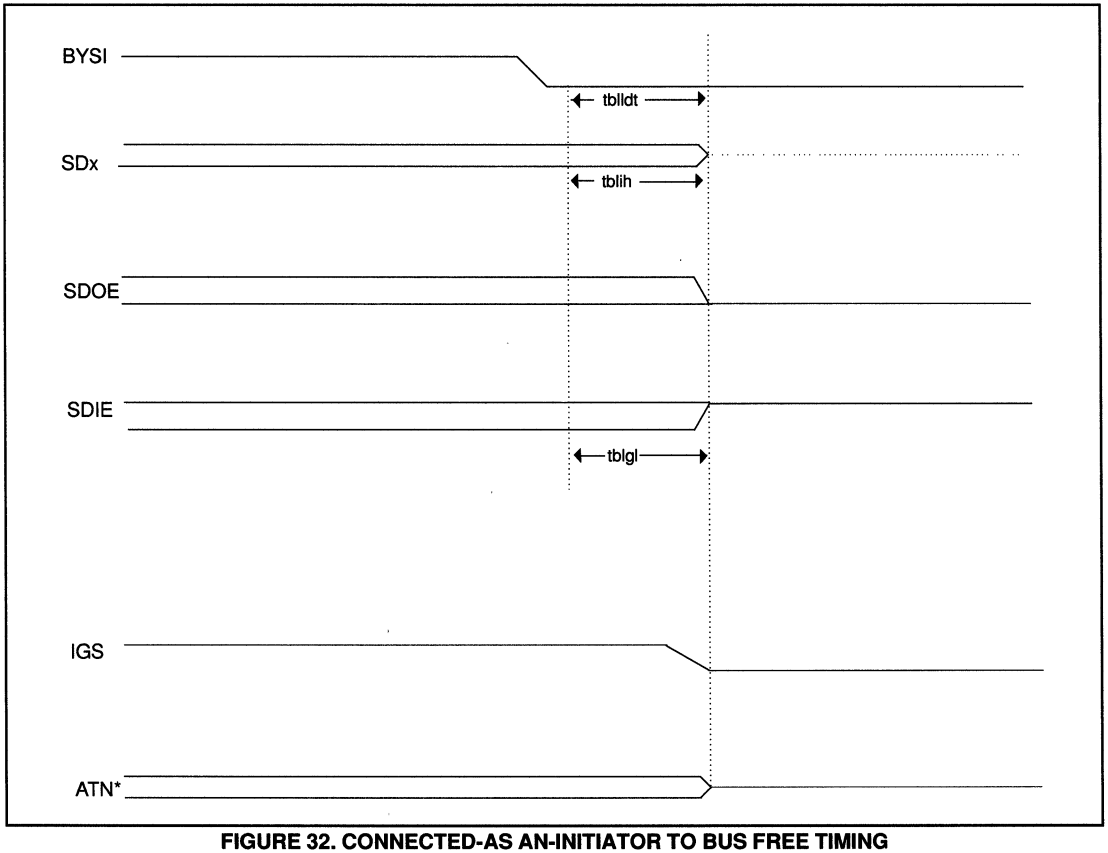


FIGURE 32. CONNECTED-AS AN-INITIATOR TO BUS FREE TIMING

9.2.17 Connected-as-a-Target To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tblih	BSYO LOW TO SDIE HIGH, SDOE LOW		8+120ns	Tcyc
tbldt	BSYO LOW TO DATA BUS TRISTATE		8+120ns	Tcyc
tblgl	BSYO LOW TO TGS LOW, I/O TRISTATE		8+120ns	Tcyc

NOTE:
I/O* = I/O, C/D, MSG, REQ

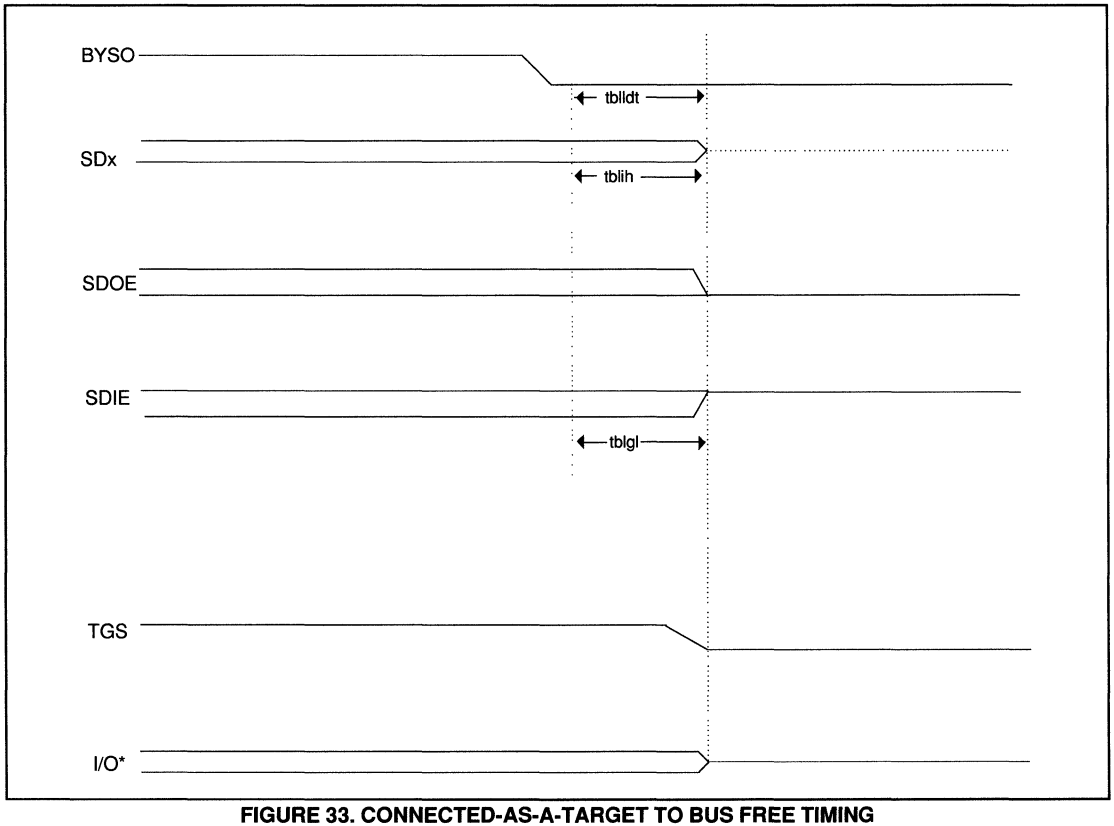


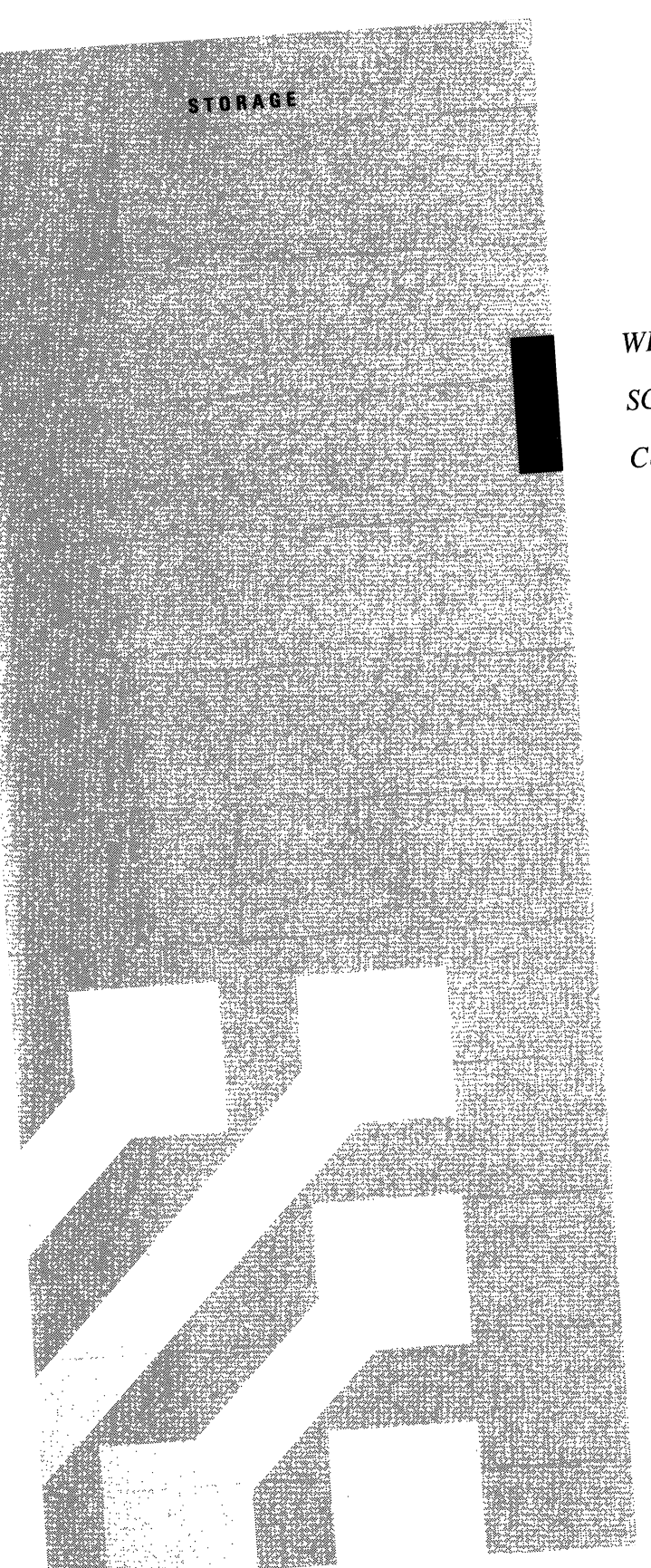
FIGURE 33. CONNECTED-AS-A-TARGET TO BUS FREE TIMING

STORAGE

WD33C93A

SCSI Bus Interface Controller

29



WESTERN DIGITAL

WD33C93A SCSI Bus Interface Controller

FEATURES

- Implements full SCSI bus features: arbitration, disconnect, reconnect, parity generation/checking on both data ports, soft reset, and synchronous data transfers.
- Asynchronous Data transfers up to 2.5 Mb/sec
- Synchronous Data transfers up to 5.0 Mb/sec
- Synchronous offset selectable from 1 to 12 bytes.
- Compatible with most microprocessors through an 8-bit data bus; supports both multiplexed and non-multiplexed address/data bus systems. Host bus data parity checking and generation is an optional feature.
- Can be used as host adapter (SCSI Initiator) or peripheral adapter (SCSI Target).
- Local host data transfer options include programmed I/0, single byte DMA, burst (multibyte) DMA, or direct bus access (WD bus) transfers.
- Includes 48-ma drivers for direct connection to the SCSI bus.
- 24 bit transfer counter.
- Programmable timeout for selection and reselection.
- Internal Microcontroller
- "Combination" commands greatly reduce interrupt-handling responsibilities.
- Special "Translate Address" command performs the Logical-to-Physical addressed translation.
- Single +5V supply.
- Available in 44-pin chip carrier or 40-pin DIP.
- Low power CMOS design.

DESCRIPTION

The WD33C93A is a MOS/VLSI device which is implemented in Western Digital's CMOS process. It operates from a single 5 volt supply and is available in either a 44-pin chip carrier or a 40-pin dual-in-line package. All inputs and outputs are TTL-compatible.

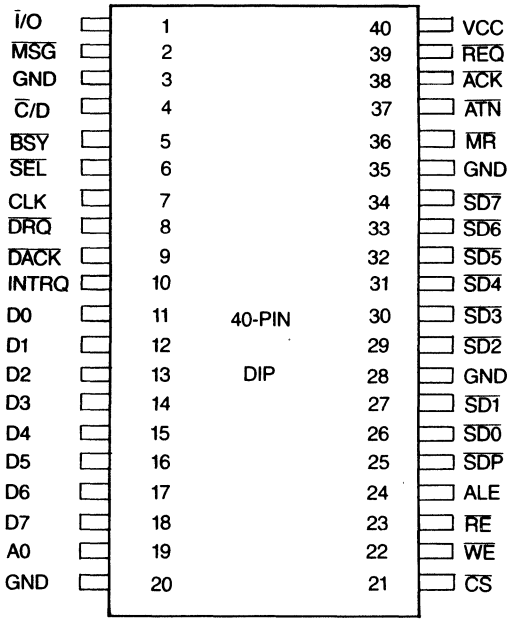
The WD33C93A is intended for use in systems which interface to the SCSI (Small Computer System Interface) Bus. The WD33C93A can operate in both the Initiator (typically, a host computer system) and the Target (typically, a peripheral device) SCSI bus roles.

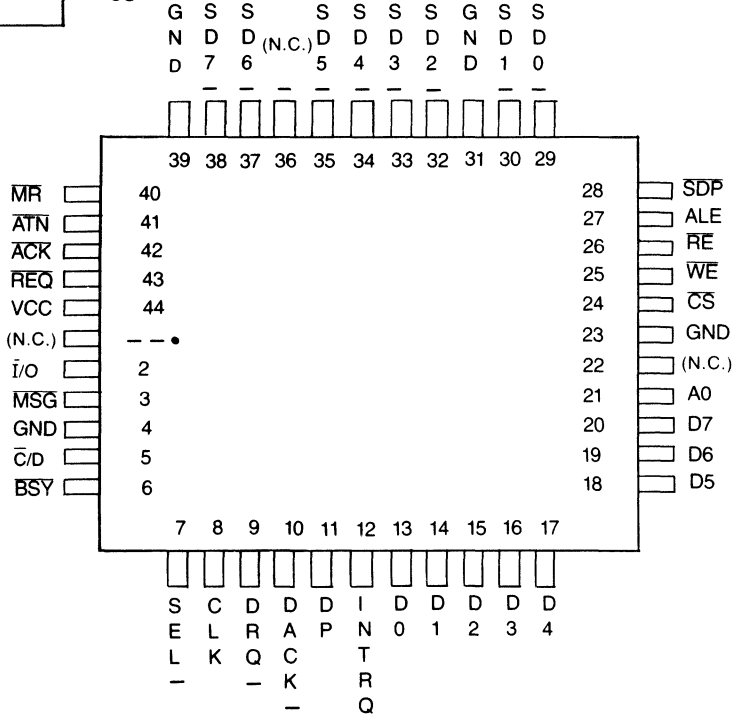
When used in the host system, the WD33C93A interfaces to both the host bus and to the SCSI bus. To perform a SCSI operation, the host processor must issue a command to the WD33C93A to select the desired Target. The WD33C93A then arbitrates for the SCSI bus and selects the peripheral unit. If it fails to get the bus because of a higher priority bus device, it continues trying, notifying the host when it has succeeded by generating an interrupt. At this point, the WD33C93A is operating in the initiator role. When the peripheral requests a SCSI command from the host, the WD33C93A receives the request and generates another interrupt to the host. The host responds to this interrupt by issuing a "Transfer Info" command and supplying SCSI command bytes to the WD33C93A. The WD33C93A transfers the SCSI command to the peripheral, and then waits for the next bus phase request. This process continues until all SCSI information including data, status, and messages have been transferred.

The WD33C93A also offers high level Select-And-Transfer commands, which may be used to eliminate the interrupt-handling which is otherwise typically required between each SCSI bus phase.

When the WD33C93A is used in a peripheral system, it interfaces with a local processor and the SCSI bus just as it does when used as a host adapter. In this environment, the WD33C93A will operate primarily in a Target role. The Target-role command set enables the WD33C93A to request each SCSI bus phase individually, or the special combination commands may be used for automatic SCSI bus phase sequencing.

The WD33C93A has an internal microcontroller, a register task file, and SCSI interface logic. This architecture supports both tight control of the protocol for non-standard SCSI implementations, as well as a hands-free mode for standard SCSI applications.





NOTE: Pin labeled N.C. should be left not connected.

4. PIN DESCRIPTIONS

4.1 PROCESSOR/DMA INTERFACE

DIP (40 PIN)	PLCC (44 PIN)	NAME	I/O	FUNCTION
7	8	CLK	I	8–16 MHz square wave clock.
36	40	$\overline{MR}$	I	Reset is an active low input which forces the WD33C93A into an idle state. All SCSI signals are forced to the negated state.
10	12	INTRQ	O	Interrupt Request to external microprocessor. Used to indicate command completion/termination or a need to service the SCSI interface. This bit is reset when the SCSI Status register is read.
23	26	$\overline{RE}$	I/O	Read enable is an active low input which is used with CS- to read a WD33C93A register. In WD Bus mode, it is used as an output to read data from a sector buffer. (Tri-State)
22	25	$\overline{WE}$	I/O	Write enable is an active low input which is used with CS- to write a WD33C93A register. In WD Bus mode, it is used as an output to write data to a sector buffer. (Tri-State)
21	24	$\overline{CS}$	I	Chip Select is an active low input which is used to qualify RE- and WE- when accessing a register. This signal must be inactive during a DMA cycle (DACK- active in DMA/burst mode, or DRQ active in WD Bus mode).
19	21	AO	I	Address pin used to access the internal registers for non-multiplexed address/data busses (i.e., the ALE pin is grounded). The address of the desired register is loaded into the Address register during a write cycle with A0 = 0. The selected register is then accessed when A0 = 1.
24	27	ALE	I	Address Latch Enable is used for multiplexed address/data busses to load the address of the desired WD33C93A register from the data bus. If indirect addressing is to be used, the ALE pin should be grounded. See the description of the Address register for a complete discussion of direct and indirect addressing.
9	10	$\overline{DACK}$/($\overline{RCS}$)	I/O	DMA acknowledge input used for interfacing to an external DMA controller. When DACK is low, all bus transfers are to/from the Data register regardless of the contents of the ADDRESS register. In WD Bus mode, this pin functions as a RAM chip select output to allow the WD33C93A to access a sector buffer. RE- and WE- are outputs when RCS- is active. Since this pin can be an open drain output, a pullup resistor is required when operating in WD Bus mode.
8	9	$\overline{DRQ}$/ (DRQ)	I/O	Data request is an output when interfacing to an external DMA controller, and an input when in WD Bus mode. When used with an external DMA controller, DRQ- and DACK- form the handshake for the data-byte transfers. In Burst mode, DRQ- remains low as long as there is data to transfer. In WD Bus mode, the WD33C93A performs burst transfers while DRQ is high, and when DRQ is low, data transfers are inhibited, RCS- is false, and the RE- and WE- outputs are disabled. Since this pin can be an open drain output, a pullup resistor is required when operating in DMA or Burst mode.
18-11	17-13	D7-D0	I/O	Host processor data bus.
	11	DP	I/O	Data Parity, used only for checking/generating host data bus parity during data transfers. (odd)

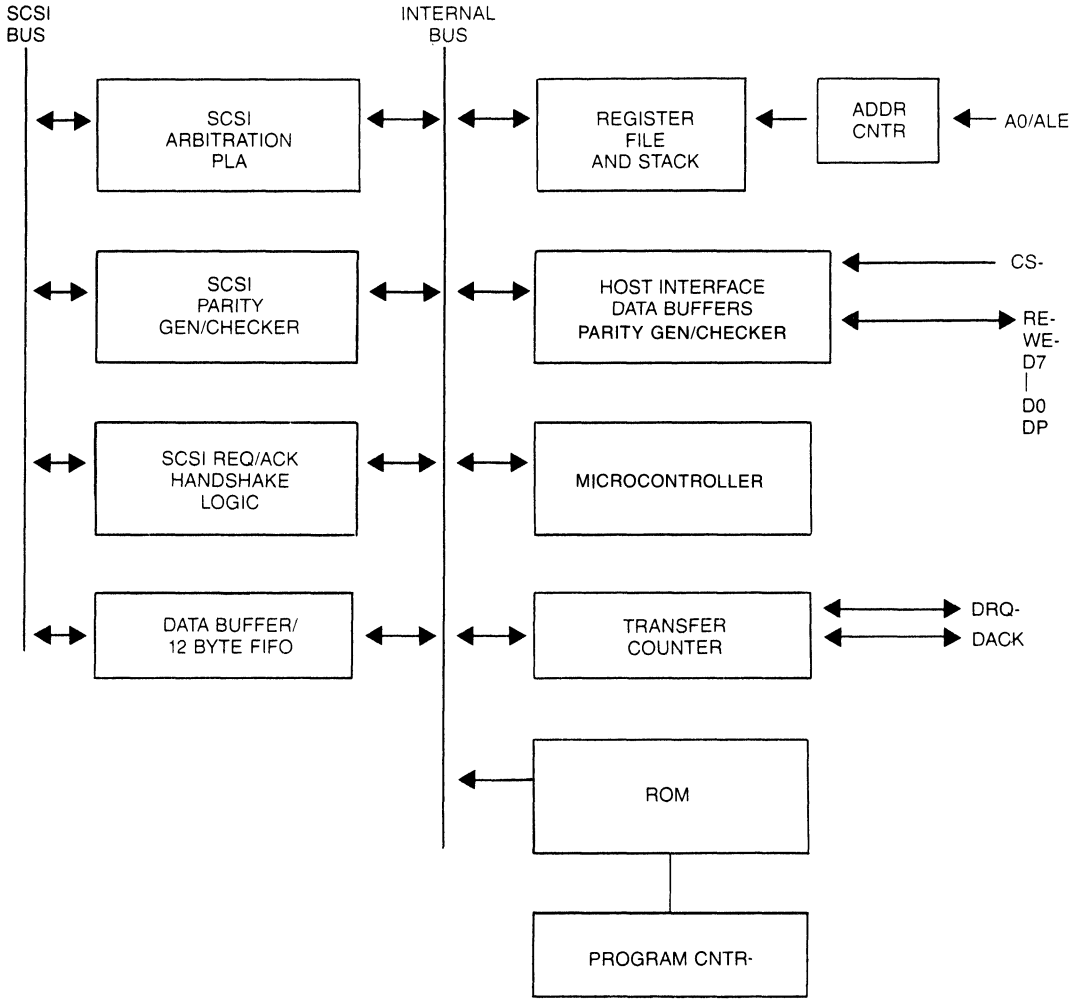
29

4.2 SCSI INTERFACE

Note: All pins have open-drain output drivers.

DIP (40 PIN)	PLCC (44 PIN)	NAME	I/O	FUNCTION
39	43	$\overline{REQ}$	I/O	REQ- is an input in the initiator role and an output in the target role. It indicates a request for a REQ/ACK data transfer.
38	42	$\overline{ACK}$	I/O	ACK- is an output in the initiator role and an input in the target role. It is used to indicate an acknowledgement for a REQ/ACK data transfer handshake.
37	41	$\overline{ATN}$	I/O	ATN- is an output in the initiator role and an input in the target role. It is used to indicate the SCSI Attention condition.
2	3	$\overline{MSG}$	I/O	MSG- is an input in the initiator role and an output in the target role. It is asserted during a Message phase.
4	5	$\overline{C}$/D	I/O	C/D- is an input in the initiator role and an output in the target role. It is used to indicate whether Control or Data information is on the SCSI data bus.
1	2	$\overline{I/O}$	I/O	I/O- is an input in the initiator role and an output in the target role. It controls the direction of data movement on the SCSI data bus with respect to an Initiator.
5	6	$\overline{BSY}$	I/O	BSY- is asserted when the WD33C93A is attempting to arbitrate for the SCSI bus or when connected as a Target.
6	7	$\overline{SEL}$	I/O	SEL- is asserted when the WD33C93A is attempting to select or reselect another SCSI device.
N/A	28	$\overline{SDP}$	I/O	SCSI data bus parity signal. (odd)
34–26	38–29	$\overline{SD7}$–$\overline{SD0}$	I/O	SCSI data bus.

5 WD33C93A BLOCK DIAGRAM



6. WD33C93A REGISTERS

6.1 REGISTER MAP

A0	R/W	REGISTER ACCESSED		ADDRESS (Hex)
0	R	AUXILIARY STATUS		XX
0	W	ADDRESS REGISTER		XX
1	R/W	OWN ID REGISTER	/CDB SIZE	00
1	R/W	CONTROL REGISTER		01
1	R/W	TIMEOUT PERIOD REGISTER		02
1	R/W	TOTAL SECTORS REGISTER	/CDB 1ST	03
1	R/W	TOTAL HEADS REGISTER	/CDB 2ND	04
1	R/W	TOTAL CYLINDERS REGISTER (MSB)	/CDB 3RD	05
1	R/W	TOTAL CYLINDERS REGISTER (LSB)	/CDB 4TH	06
1	R/W	LOGICAL ADDRESS (MSB)	/CDB 5TH	07
1	R/W	LOGICAL ADDRESS (2ND)	/CDB 6TH	08
1	R/W	LOGICAL ADDRESS (3RD)	/CDB 7TH	09
1	R/W	LOGICAL ADDRESS (LSB)	/CDB 8TH	0A
1	R/W	SECTOR NUMBER REGISTER	/CDB 9TH	0B
1	R/W	HEAD NUMBER REGISTER	/CDB 10TH	0C
1	R/W	CYLINDER NUMBER REGISTER (MSB)	/CDB 11TH	0D
1	R/W	CYLINDER NUMBER REGISTER (LSB)	/CDB 12TH	0E
1	R/W	TARGET LUN REGISTER		0F
1	R/W	COMMAND PHASE REGISTER		10
1	R/W	SYNCHRONOUS TRANSFER REGISTER		11
1	R/W	TRANSFER COUNT REGISTER (MSB)		12
1	R/W	TRANSFER COUNT REGISTER (2ND BYTE)		13
1	R/W	TRANSFER COUNT REGISTER (LSB)		14
1	R/W	DESTINATION ID REGISTER		15
1	R/W	SOURCE ID REGISTER		16
1	R	SCSI STATUS		17
1	R/W	COMMAND REGISTER		18
1	R/W	DATA REGISTER		19
1	R	AUXILIARY STATUS	(DIRECT ADDRESSING MODE)	1F

NOTES:
1. All unused bits of a defined register are reserved and must be zero.
2. Reading an undefined or unavailable register results in an all-ones data bus output.
3. Register addresses are determined by the Address register bits AR0 thru AR7.
4. When using a multiplexed address/data bus with ALE, the A0 pin is ignored and the Address register is loaded with ALE. In this mode, the Auxiliary Status register is mapped at Hex 1F.
5. See section 6.3 for a description of how reset affects the internal registers.

6.2 REGISTER DESCRIPTIONS

6.2.1 AUXILIARY STATUS REGISTER (Address Hex IF)

The Auxiliary Status register is a read-only register which contains general status information not directly associated with the interrupt condition. The Auxiliary Status register may be accessed at any time, except during DMA accesses (DACK- asserted in DMA/Burst mode, or DRQ asserted in WD bus mode).

7	6	5	4	3	2	1	0
INT	LCI	BSY	CIP	0	0	PE	DBR

Bit 0 DBR Data Buffer Ready is used during programmed I/0 to indicate to the processor whether or not the Data register is available for reading or writing. During Send or Transfer commands which transmit data over the SCSI bus, the DBR bit is set when the WD33C93A is ready to take a byte from the host; the bit is reset when the processor writes the byte to the DATA register. During Receive or Transfer commands which receive data over the SCSI bus, the DBR is set when a byte is received; it is reset when the processor reads the byte from the DATA register.

Bit 1 PE Parity Error status indicates that even parity was detected on a data byte received during an information transfer. Parity is checked on data received from the host bus during transfers out to the SCSI bus, and is checked on data received from the SCSI bus during transfers out to the host bus. Detection of a parity error will set the PE status bit regardless of the state of the HHP or HSP bits in the Control register. The PE bit is cleared when a new command is issued.

Bit 2 Not used, will be zero.

Bit 3 Not used, will be zero.

Bit 4 CIP COMMAND IN PROGRESS, when set, indicates that the WD33C93A is interpreting the last command entered into the Command register and therefore this register is unavailable. When this bit is reset, a command may be written to the Command register.

Bit 5 BSY BUSY indicates that a Level II command is currently executing and therefore only the Command register (when CIP = 0), the DATA register, and the Auxiliary Status register are accessible by the host. A Level II command may not be written to the Command register when this bit is one.

Bit 6 LCI LAST COMMAND IGNORED indicates that a command was issued by the host just prior to or concurrent with a pending interrupt, and therefore the command will be ignored and this status set.

Bit 7 INT INTERRUPT PENDING indicates that the Intrq pin is asserted. The host should read the SCSI Status register to clear Intrq prior to issuing any commands.

6.2.2 ADDRESS REGISTER [Address XX Hex]

The Address register is a write-only register which contains the address of the register to be accessed. Registers in the WD33C93A may be accessed in one of two ways:

- Direct addressing (multiplexed address/data busses). In direct addressing, the falling edge of the ALE signal is used to latch the address into the ADDRESS register. The ALE is typically then followed by the CS- and WE- or RE- signals that access the selected register. Also, in direct addressing, the AUXILIARY STATUS register is located at address 1F Hex.
- Indirect addressing (separate address/data busses). In indirect addressing, the register access is performed in two separate cycles. This method is enabled by attaching ALE to ground. First, the Address register is loaded by performing a write of the desired address to the WD33C93A (WE- and CS- asserted) with A0 = 0. Then the register is accessed by asserting CS- and WE- or RE-, with A0 = 1. Also, following every access with A0 = 1, the Address register will automatically increment to point at the next register, with the exception of the following locations: Auxiliary Status register, Data register, and the Command register. In indirect addressing, the Auxiliary Status register is accessed by performing a read (CS- and RE- asserted) with A0 = 0.

6.2.3 OWN ID/CDB SIZE REGISTER [Address 00 Hex]

The Own ID/CDB Size register, in its first mode, contains both the encoded ID of the WD33C93A on the SCSI bus and several control bits that are used to initially configure the device during the "Reset" command. These bits control 'advanced feature' selection, host bus parity enable, and selection of the input clock division. In its second mode (when advanced features are enabled, see 7.3), this register is used during the combination commands to specify the SCSI CDB size if the command group is unknown to the WD33C93A.

In the first mode, this register (as defined below) is sampled and becomes effective only after a "Reset" command is issued to the device. This register must be initialized, and then a "Reset" command issued, to set the SCSI bus ID, the clock divisor, and the operating modes before any other commands are issued.

In the second mode, bits 3-0 of this register are used during the Select-and-Transfer and Wait-for-Select commands to specify the SCSI Command Descriptor Block size if it is not a group 0, group 1, or group 5 command. This mode is enabled only when advanced features are enabled (see 7.3).

OWN ID/CDB SIZE REGISTER

7	6	5	4	3	2	1	0
FS1	FS0	0	EHP	EAF	ID2	ID1	ID0

Bit 0–2 IDn SCSI ID Bits 0–2 set the SCSI bus ID number that the WD33C93A will use during arbitration and selection.

Bit 3 EAF ENABLE ADVANCED FEATURES, when set to one, causes the WD33C93A to enable certain advanced features (see section 7.3). When this bit is zero, those features are disabled.

Bit 4 EHP ENABLE HOST PARITY, when set to one, enables odd parity checking on the host bus; the PE bit in the Auxiliary Status register will indicate parity errors detected on the host bus, and the HHP bit in the Control register will be used. When this bit is zero, no checking is performed on the host bus; the PE bit is not set when a parity error is detected on the host bus, and the HHP bit must be set to zero.

NOTE: Parity is always generated on the host data parity bit (DP), regardless of the state of this bit.

Bit 5 Not used, will be zero.

Bit 6–7 FSn FREQUENCY SELECT 0–1 select the divisor that is applied to the input clock. The resulting clock is used for data transfer timing and for SCSI bus arbitration timing. The table below shows input clock frequency ranges and the corresponding divisors. The correct divisor for the input clock must be used, or SCSI bus timing specifications may not be met.

INPUT CLOCK FREQUENCY (MHZ)	FS1	FS0	RESULTING DIVISOR
8–10	0	0	2
12–15	0	1	3
16	1	0	4
xx	1	1	undefined

Note that an 11 MHZ clock rate should not be used, as the resulting SCSI bus clear delay may violate SCSI specifications. The formula for computing the maximum SCSI data transfer rate is:

$$\text{MAXIMUM SCSI TRANSFER RATE} = \frac{\text{INPUT CLOCK FREQUENCY}}{\text{CLOCK DIVISOR}} \text{ [MByte/sec]}$$

29

6.2.4 CONTROL REGISTER [Address 01 Hex]

The CONTROL register is used to enable/disable certain functions, such as response to parity errors and the SCSI attention condition, interrupt handling, and data transfer modes.

BIT	7	6	5	4	3	2	1	0
	DM2	DM1	DM0	HHP	EDI	IDI	HA	HSP

Bit 0 HSP The HALT on SCSI PARITY ERROR bit enables the WD33C93A to terminate a Receive or Transfer command if a parity error is detected on an incoming SCSI data byte. In the Initiator role, termination due to a SCSI parity error causes the ACK- pin to be left in the active state in order to inhibit any additional data transfers (REQs) by the Target; this facilitates error handling with the Target. Synchronous data transfers check parity every 4096 bytes, or at the end of the remaining transfer count, whichever is less. Asynchronous transfers check parity on every byte.

Bit 1 HA The HALT on ATTENTION bit (in Target mode only) enables the WD33C93A to terminate a Send or Receive command if the ATN- input is asserted. This normally indicates that the Initiator detected a parity error while receiving data from the WD33C93A. The ATN- input is tested before the start of a data transfer, every 4096 bytes if the transfer count is greater than 4096, and after the end of the transfer. These rules apply to both synchronous and asynchronous transfers.

Bit 2 IDI The Intermediate Disconnect Interrupt bit, when set, enables the WD33C93A to generate an 85H disconnect interrupt and suspends a Select-and-Transfer command if the Target disconnects according to the defined SCSI protocol. When this bit is reset, no interrupt is generated by a valid disconnect. This feature, when used with the Resume SAT command, provides support for overlapped SCSI operations. IDI is also used to select execution options in Target mode combination commands that serve to reduce host system overhead. Refer to Section 7 for more details.

Bit 3 EDI When the Ending Disconnect Interrupt bit is set, the 16H interrupt which normally follows the Command Complete message during the execution of a Select-And-Transfer command will be suppressed until the Target disconnects from the SCSI bus. EDI is also used in the Target mode combination commands to enable chaining between those commands, resulting in reduced host system overhead. Refer to Section 7 for more details.

Bit 4 HHP The Halt on Host Parity Error bit enables the WD33C93A to immediately terminate a Send or Transfer command if a parity error is detected on an incoming host data byte. Host parity errors are checked according to the rules for checking SCSI parity errors. However, a halt on a host parity error will not hold the ACK- signal asserted when an error occurs. Host parity checking is performed at the same intervals as SCSI parity checking.

Bit 5–7 DMx DMA Mode Select bits 2-0 are used to select the DMA mode of operation, which describes the host bus transfer mode used during Data In or Data Out phases. The following table describes the different DMA modes, and the state of these bits to select them:

DM2	DM1	DM0	DMA MODE SELECTED
0	0	0	Polled I/0 Mode, or no DMA enabled. All data phase transfers are performed by polling for DBR in the Auxiliary Status register, and then writing (reading) the data to (from) the Data register.
0	0	1	Burst Mode selects a demand-mode DMA interface. In this mode, the DRQ- signal will be active as long as there is data/space in the internal FIFO to allow the transfer to continue. The DMA controller responds by asserting DACK- and RE-/WE- as long as DRQ- is active.
0	1	0	WD Bus Mode should be selected when the WD33C93A is connected to a WD Bus. This mode is also referred to as Direct Buffer Access (DBA) mode. In this mode, the WD33C93A acts as a bus master, and all data access signals reverse their direction: The DRQ- signal become the DRQ input, which enables the WD33C93A to drive the buffer bus control signals. The DACK- signal becomes the RCS- output, which is asserted as a chip select for the buffer. RE- and WE- become outputs which drive the read and write functions of the external FIFO/RAM buffer. As long as the DRQ signal is asserted, transfers will continue in a burst manner, until the transfer is complete or the host/local up decides to pause the transfer by negating the DRQ signal; after negating DRQ, one more transfer may occur before the RCS-, RE-, and WE- signals are negated.
1	0	0	DMA Mode is selected when the WD33C93A is to be used with a DMA controller in single-type transfer mode. In this mode, DRQ- is asserted and then negated, and the DMA controller responds by asserting DACK- and WE- or RE-, for each data byte transferred to/from the WD33C93A.

6.2.5 TIMEOUT PERIOD REGISTER [Address 02 Hex]

The Timeout Period register is an 8-bit register containing a preset value which determines the timeout period for Select and Reselect commands. This value may be calculated as a function of the input clock frequency and the desired timeout period, as shown in the following equation:

$$\text{register value} = \frac{\text{Tper} * \text{Ficlk}}{80\text{d}}$$

Where:

Tper = the desired timeout period in milliseconds;
Ficlk = the input clock frequency at the CLK pin in Megahertz (with no divisor applied).
d = decimal

The constant '80' scales the units of the equation, as is based on the internal timeout cycle time. The user should round the resulting 'register value' up to the next integral value to ensure that the user's minimum timeout requirement is met.

The timeout period specifies how long the WD33C93A will wait for a response (indicated by assertion of the BSY- signal) after it has begun the selection phase (assert SEL- and negate BSY-) before terminating the command. The timeout function can be disabled by loading the Timeout Period register with zero.

NOTE: The following twelve registers are used exclusively by the Translate Address and/or "combination" commands. The function of each register is determined by the type of command issued.

6.2.6 TOTAL SECTORS REGISTER/ CDB 1ST BYTE [Address 03 Hex]

Translate Address: The Total Sectors register should be set to the total number of sectors per track prior to issuing a Translate Address command.

Select-and-Transfer: This register should be loaded with the first byte of the Command Descriptor Block before issuing a Select-And-Transfer command.

Wait-For-Select-And-Receive: The WD33C93A will store the first byte of the received CDB in this register.

6.2.7 TOTAL HEADS REGISTER/ CDB 2ND BYTE [Address 04 Hex]

Translate Address: This register holds the total number of heads during a Translate Address command.

Select-And-Transfer: This register should be loaded with the second byte of the CDB before issuing a Select-And-Transfer command.

Wait-For-Select-And-Receive: The WD33C93A will store the second byte of the received CDB in this register.

6.2.8 TOTAL CYLINDERS REGISTER/ CDB 3RD AND 4TH BYTES [Address 05, 06 Hex]

Translate Address: This is a 16-bit register which holds the total number of cylinders.

Select-And-Transfer: This register should be loaded with the third and fourth bytes of the CDB before issuing a Select-And-Transfer command.

Wait-For-Select-And-Receive: The WD33C93A will store the third and fourth bytes of the received CDB in this register.

6.2.9 LOGICAL ADDRESS REGISTER/ CDB 5TH-8TH BYTES [Address 07, 08, 09, 0A Hex]

Translate Address: The Logical Address register is a 32-bit register which should be loaded with the logical address to be translated prior to issuing the Translate Address command.

Select-And-Transfer: For six byte CDBs, only the first two bytes of this register are loaded with the fifth and sixth bytes of the CDB. For ten and twelve byte CDBs, this register is loaded with the fifth, sixth, seventh, and eighth bytes of the CDB.

Wait-For-Select-And-Receive: The WD33C93A will store the fifth, sixth, seventh (if any), and eighth (if any) bytes of the received CDB in this register.

6.2.10 SECTOR NUMBER REGISTER/CDB 9TH BYTE [Address 0B Hex]

Translate Address: This register will contain the resulting sector number following a Translate Address command.

Select-And-Transfer: This register should be loaded with the ninth byte of a ten or twelve byte CDB before issuing a Select-and-Transfer command.

Wait-For-Select-And-Receive: The WD33C93A will store the ninth byte of a ten or twelve byte received CDB in this register.

6.2.11 HEAD NUMBER REGISTER CDB 10TH BYTE [Address 0C Hex]

Translate Address: The Head Number register contains the resulting head number following a Translate Address command. If automatic compensation for spare sectors on a disk is to be performed by the WD33C93A, then the number of spare sectors per cylinder must be written into this register before issuing the Translate Address command. It should be noted that when compensation is used, the maximum number of cylinders allowed is 4096, and the maximum number of heads is 15. An initial value of zero in this register indicates that no compensation is to be performed.

Select-And-Transfer: This register should be loaded with the tenth byte of a ten or twelve byte CDB before issuing a Select-And-Transfer command.

Wait-For-Select-And-Receive: The WD33C93A will store the tenth byte of a ten or twelve byte received CDB in this register.

6.2.12 CYLINDER NUMBER REGISTER/CDB 11TH AND 12TH BYTES [Address 0D, 0E, Hex]

Translate Address: The Cylinder Number register is a

16-bit register which contains the resulting cylinder number following execution of the Translate Address command. When a Translate Address command involving automatic compensation for spare sectors is issued (i.e. the Head Number register initially contains a non-zero value), then this register must be loaded with total number of sectors per cylinder (total sectors/track * total heads — total spare sectors/cyl) before issuing the command.

Select-And-Transfer: This register should be loaded with the eleventh and twelfth bytes of a twelve byte CDB before issuing a Select-and-Transfer command.

Wait-For-Select-And-Receive: The WD33C93A will store the eleventh and twelfth bytes of a twelve byte received CDB in this register.

Send-Status-And-Command-Complete: The CDB11 register is used to specify the returned status byte to be sent during a Send-Status-And-Command-Complete command. The CDB12 register is used to determine the type of Command-Complete message sent by the WD33C93A. If bit 0 of the CDB12 register is set to one, then a linked Command Complete message will be sent during command execution. In this case, bit 1 of the CDB12 register is used as a FLAG bit to determine whether a 0A Hex (FLAG = 0) or a OB Hex (FLAG = 1) Linked Command Complete message is sent. If bit 0 is zero, then a simple Command Complete message (00 Hex) is sent.

6.2.13 TARGET LUN REGISTER [Address 0F Hex]

The Target LUN register is used to hold both the Logical Unit Number (LUN) and Target status information during various WD33C93A commands and sequences. During a Select-And-Transfer or Reselect-And-Transfer command, the contents of this register (along with the Source ID register) are used to generate and check the Identify messages which are transferred across the SCSI bus. In addition, the Target LUN register is used to hold the Target Status byte received during a Select-And-Transfer command.

BIT	7	6	5	4	3	2	1	0
	TLV	DOK	0	0	0	TL2	TL1	TL0

During Wait-For-Select-And-Receive commands, this register may hold the image of the Identify message received from the Initiator. If the TLV bit is zero, there was no Identify message received. If the TLV bit is one, then a valid Identify message was received. The DOK bit will then indicate whether or not the Initiator has enabled disconnects.

During Reselect-And-Transfer commands, this register is used to set the LUN to be used in the Identify message sent to the Initiator after Selection phase. The TLV and DOK bits are not used.

In advanced mode, during Select-And-Transfer commands, this register is used to handle reselection by an unexpected Target. In this mode, this register will hold the image of the Identify message received from the Target. In this case, the TLV bit is one, since the Target always sends the Identify message.

6.2.14 COMMAND PHASE REGISTER [Address 10 Hex]

The Command Phase register is used during combination commands to indicate which phases of these multi-phase commands have been completed. Thus, if the command has terminated abnormally, the processor can read this register to determine the cause of the termination and how to respond to it. This register is also used to resume combination commands by loading this register with a value that indicates the next desired or expected bus phase, and reissuing the command. Refer to the description of the specific commands for details regarding the various command phases and resume values.

6.2.15 SYNCHRONOUS TRANSFER REGISTER [Address 11 Hex]

The Synchronous Transfer register is used to select between synchronous and asynchronous transfers, and is also used to define the maximum transfer rate. For information phases other than a "data" transfer phase, or when the selected offset is zero (OF3 – OF0 = 0), asynchronous transfers will occur. Values greater than zero define a synchronous transfer mode and the offset is determined as shown below. This offset determines the effective FIFO depth for synchronous data transfers, and is typically determined by negotiation with the other SCSI device (as defined in the SCSI standard). The Transfer Period control bits select the minimum transfer period for both synchronous and asynchronous SCSI transfers and, if WD-Bus mode is used, the transfer period and the width of the RE-/WE- strobes for host transfers. The period is defined in terms of the internal clock cycle time; the frequency of this clock is determined by the divisor selected in the OWN ID register.

BIT	7	6	5	4	3	2	1	0
	0	TP2	TP1	TP0	OF3	OF2	OF1	OF0

Bit 0–3 OFx The OFFSET bits are used to select the desired offset according to the following:

OF3	OF2	OF1	OF0	SELECTED OFFSET
0	0	0	0	Note 1
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	0	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	12
1	1	1	X	12

Note 1* — Asynchronous data phase transfers

Bit 4-6 TPx The TRANSFER PERIOD bits are used to select the desired transfer period according to the following table:

TP2	TP1	TP0	SCSI/WD-BUS TRANSFER PERIOD	(SCSI REQ/ACK synchronous pulse width and WD-BUS RE-/WE- pulse width)
0	0	X	8 cycles	(4 cycles)
0	1	0	2 cycles	(1 cycle)
0	1	1	3 cycles	(1 cycle)
1	0	0	4 cycles	(2 cycles)
1	0	1	5 cycles	(3 cycles)
1	1	0	6 cycles	(4 cycles)
1	1	1	7 cycles	(4 cycles)

The 'cycle' referred to above is the period of the internal data transfer clock after the divisor chosen in the OWN ID register is applied. This period is calculated by the following formula:

$$\text{CYCLE } (\mu s) = \frac{\text{DIVISOR (from OWN ID)}}{2 * \text{INPUT CLOCK FREQUENCY (MHZ)}}$$

6.2.16 TRANSFER COUNT REGISTER [Address 12, 13, 14 Hex]

The Transfer Count register is a 24-bit register containing a preset value for the internal transfer counter. This preset value is loaded into the internal transfer counter when a Send, Receive, or Transfer command is issued. This counter is used to define command completion by decrementing as each data byte is transferred over the SCSI bus and causing a successful completion interrupt when the counter reaches zero. In combination commands, this register specifies the number of bytes to be transferred during a Data phase.

The counter function can be disabled by loading the Transfer Count register with zeroes prior to issuing a command or by setting the Single-Byte Transfer bit in the Command register concurrent with issuing the command. If the counter is disabled, the Send, Receive, or Transfer command will be completed when a single byte has been transferred.

After the completion of any successful transfer, the Transfer Count register will be zero. This includes commands issued in Single Byte Transfer mode.

When a transfer is interrupted by a halt on error condition, a SCSI bus phase change, or an abort, the Transfer Count register will contain the number of bytes NOT successfully transferred to/from the SCSI bus, including clearing the internal FIFO of any bytes left in the FIFO (see DATA register). This FIFO clearing process may cause the Transfer Count register to differ with the user's DMA controller count, because some bytes may have been transferred into the FIFO, but not to the SCSI bus; therefore, the Transfer Count should be used to determine the actual number of bytes transferred to/from the SCSI bus.

6.2.17 DESTINATION ID REGISTER [Address 15 Hex]

The Destination ID register contains the encoded SCSI bus ID of the device which is to be selected or reselected when a Reselect or Select command is issued. This register also contains control bits that affect the operation of certain combination commands.

BIT	7	6	5	4	3	2	1	0
	SCC	DPD	0	0	0	DI2	DI1	DI0

Bit 0–2 Destination ID bits DI0-DI2 contains the encoded SCSI bus ID of the device which is to be selected or reselected when a Reselect or a Select command is issued.

Bit 6 DPD DATA PHASE DIRECTION, when advanced features are enabled (see 7.3), is used to specify the expected direction of the SCSI data phase. This allows the WD33C93A to verify the direction during Select-And-Transfer commands before beginning the transfer. When this bit is zero, the expected direction is out (to the Target). When this bit is one, the expected direction is in (from the Target). An unexpected information phase error will occur if the direction does not match the setting of this bit.

Bit 7 SCC SELECT COMMAND CHAIN is used only when the Reselect-And-Transfer command is issued with EDI = 1. This bit selects which command is chained to when the data transfer is completed. When this bit is zero, a Send-Status-and-Command-Complete command begins executing. When this bit is one, a Send-Disconnect-Message command begins executing.

29

6.2.18 SOURCE ID REGISTER [Address 16 Hex]

The SOURCE ID register is used to report the SCSI bus ID of the device that has selected or reselected the WD33C93A. It also contains bits that enable and control response to selection and reselection.

BIT	7	6	5	4	3	2	1	0
	ER	ES	DSP	0	SIV	SI2	SI1	SI0

Bit 0–2 SIx Source ID Bits 2–0 are valid only if the SIV bit is set to one. These bits indicate the SCSI bus ID of the device that selected or reselected the WD33C93A.

Bit 3 SIV Source ID Valid is set to one after the WD33C93A is selected or reselected if the other SCSI bus device asserted its own bus ID bit (in addition to the bus ID bit of the WD33C93A) during the select/reselect phase. This bit is zero if only the bus ID bit of the WD33C93A was asserted.

Bit 4 Not used, will be zero.

Bit 5 DSP Disable Select Parity, when set to one, causes the WD33C93A to ignore the bus parity when responding to selection or reselection. When this bit is zero, any selection or reselection with a parity error is ignored.

Bit 6 ES Enable Selection, when set to one, enables the WD33C93A to respond to a selection by another device on the SCSI bus. When this bit is zero, any selection is ignored.

Bit 7 ER Enable Reselection, when set to one, enables the WD33C93A to respond to a reselection by another device on the SCSI bus. When this bit is zero, any reselection is ignored.

6.2.19 SCSI STATUS REGISTER [Address 17 Hex]

The SCSI Status register is a read-only register which indicates the cause of the most recent interrupt request assertion. Interrupt request is asserted whenever a condition occurs within the WD33C93A that requires intervention by the host; for example:

- the WD33C93A has been reset;
- the command completed successfully;
- the bus phase changed;
- an error occurred.

Once interrupt request has been asserted, the contents of this register will not change until after the SCSI STATUS register has been read or until the WD33C93A has been reset.

BIT	7	6	5	4	3	2	1	0
	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0

Bit 0–3 SSx SCSI Status bits 0–3 are status qualifiers whose meaning depends upon which upper (4–7) status bit is set.

Bit 4–7 SSx SCSI Status bits 4–7 define the type of interrupt that occurred. The possible codes are defined in the following table:

STATUS	CODE	GROUP MEANING
0000	xxxx	The WD33C93A is in a reset state.
0001	xxxx	A WD33C93A command has completed successfully.
0010	xxxx	A WD33C93A command has paused or was aborted by an Abort command.
0100	xxxx	A WD33C93A command has been terminated prematurely due to an error or other unexpected condition.
1000	xxxx	An event on the SCSI bus requires service.

All other Status Code groups are currently not used and are reserved for future use.

In the following tables, the 'State' column indicates the current state from which the Status Code can occur. Also, the MCI field refers to the signals that define a SCSI bus information transfer phase: MSG, C/D, and I/O. A bit set to one indicates that the signal is asserted on the SCSI bus. A zero indicates negation. Whenever one of these Status Codes occurs, the REQ signal is asserted on the SCSI bus. The table below summarizes the meaning of the MCI field:

MCI CODE	MEANING
000	Data Out phase
001	Data In phase
010	Command phase
011	Status phase
100	Unspecified Info Out phase
101	Unspecified Info In phase
110	Message Out phase
111	Message In phase

RESET STATE INTERRUPTS

STATUS	CODE	STATE*	SPECIFIC MEANING
0000	0000	D, T, I	WD33C93 Reset. The device has been reset, or a Reset command has executed successfully with no advanced features enabled. The new state of the WD33C93A is disconnected.
0000	0001	D, T, I	WD33C93A Reset. The device has successfully completed a Reset command with advanced features enabled. The new state of the WD33C93A is disconnected.

* D = Disconnected
T = Connected as a Target
I = Connected as an Initiator

29

SUCCESSFUL COMPLETION INTERRUPTS

STATUS	CODE	STATE*	SPECIFIC MEANING
0001	0000	D	A Reselect command completed successfully. The new state of the WD33C93A is connected as a Target.
0001	0001	D	A Select command completed successfully. The new state of the WD33C93A is connected as an Initiator.
0001	0010		Reserved for future use.
0001	0011	D, T	A Receive, Send, Reselect-And-Transfer, Wait-For-Select-And-Receive, Send-Status-And-Command-Complete, or a Send-Disconnect-Message command completed successfully (ATN- is not asserted).
0001	0100	D, T	A Receive, Send, Reselect-And-Transfer, Wait-For-Select-And-Receive, Send-Status-And-Command-Complete, or a Send-Disconnect-Message command completed successfully (ATN- is asserted).
0001	0101	D, T	A Translate Address command completed successfully.
0001	0110	D, I	A Select-And-Transfer command completed successfully.
0001	0111		Reserved for future use.
0001	1MCI	I	A Transfer (non-Message IN phase) command completed successfully. MCI defines the new information type (SCSI bus phase) being requested.

PAUSED OR ABORTED INTERRUPTS

STATUS	CODE	STATE*	SPECIFIC MEANING
0010	0000	I	A Transfer Info (Message-In phase) command has paused with ACK- asserted. This allows the host to examine the message before accepting it.
0010	0001	I	A Save Data Pointers message was received during a Select-And-Transfer command. The host should save its current data buffer pointer.
0010	0010	D	A Select or Reselect command was aborted.
0010	0011	T	A Receive or Send command has halted by an error or was aborted (ATN- is not asserted).
0010	0100	T	A Receive or Send command has halted by an error or ATN- asserted, or was aborted (ATN- is asserted).
0010	0101	D	An Abort was issued while the WD33C93A was in the process of being selected or reselected.
0010	0110		Reserved for future use.
0010	0111	D	The WD33C93A has been reselected during a Select-And-Transfer (with IDI = 0) by a Target that does not match the SCSI bus ID loaded into the Destination ID register; or the following Identify message did not match the LUN loaded into the Target LUN register. ACK- has been left asserted following the Identify message, and the bus ID and LUN of the reselecting Target are available in the Source ID and Target LUN registers. (Advanced Mode only)
0010	1MCI	I	A Transfer command was aborted. MCI define the new information type (SCSI bus phase) being requested.

* D = Disconnected
T = Connected as a Target
I = Connected as an Initiator

TERMINATED INTERRUPTS

STATUS	CODE	STATE*	SPECIFIC MEANING
0100	0000	D, T, I	An invalid command was issued.
0100	0001	I	An unexpected disconnect (SCSI bus free) by the Target caused a command to terminate. The new state of the WD33C93A is disconnected.
0100	0010	D	A timeout occurred during a Select or Reselect command. The state of the WD33C93A is disconnected.
0100	0011	T, I	A parity error caused a command to terminate (ATN- is not asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100	0100	T, I	A parity error caused a command to terminate (ATN- is asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100	0101	D, T	The Logical Address exceeded the disk boundaries.
0100	0110	D	A Target whose SCSI bus device ID does not match the bus ID set in the Destination ID register has reselected the WD33C93A during a Select-And-Transfer command (with IDI = 0). This interrupt occurs when the WD33C93A is not in Advanced Mode. The new state of the WD33C93A is connected as an Initiator.
0100	0111	I	An incorrect status byte (i.e. the status byte has a parity error) was received during a Select-And-Transfer command. The Data Register can be read to observe the status byte in error.
0100	1MCI	I	An unexpected information phase was requested. MCI define the SCSI bus phase which is requested. This is typically caused by a phase change before the Transfer Count has reached zero, or an unexpected phase sequence occurred during a Select-And-Transfer command.

* D = Disconnected
T = Connected as a Target
I = Connected as an Initiator

SERVICE REQUIRED INTERRUPTS

STATUS	CODE	STATE*	SPECIFIC MEANING
1000	0000	D	The WD33C93A has been reselected. The new state of the WD33C93A is connected as an Initiator. No Identify message transfer has yet occurred.
1000	0001	D	The WD33C93A has been reselected in Advanced Mode. The SCSI bus ID of the Target may be read from the Source ID register. The Identify message from the Target may be read from the Data register. The ACK- signal is left asserted. The new state of the WD33C93A is connected as an Initiator.
1000	0010	D	The WD33C93A has been selected (no ATN- assertion). The new state of the WD33C93A is connected as a Target.
1000	0011	D	The WD33C93A has been selected (ATN- was asserted). The new state of the WD33C93A is connected as a Target.
1000	0100	T	The ATN- signal has been asserted.
1000	0101	I	A disconnect has occurred. The new state of the WD33C93A is disconnected.
1000	0110		Reserved for future use.
1000	0111	T	The Wait-For-Select-And-Receive command has paused because the first byte of the incoming CDB is not a known command group. The Own ID register must be loaded with the CDB length, and the command resumed. The CDB1 register may be examined to determine the SCSI command group from the opcode. The new state of the WD33C93A is connected as a Target. (Advanced Mode only)
1000	1MCI	I	The REQ signal has been asserted following connection or when the WD33C93A is in the Initiator state and no command is executing. The information phase type should be examined. MCI define the information phase (SCSI bus phase) which is being requested.

* D = Disconnected
T = Connected as a Target
I = Connected as an Initiator

6.2.20 COMMAND REGISTER [Address 18 Hex]

The Command register is used to issue the WD33C93A commands. Since the WD33C93A expects the SCSI Status to have been read before the host can issue a valid command, a command should not be loaded into the Command register within seven microseconds (independent of input clock frequency) from the last SCSI Status read to avoid the command being ignored (indicated by the LCI bit in the Auxiliary Status register). Also, this register should never be loaded when the CIP or INT bits (in Auxiliary Status) are set to one, and a Level II command should never be loaded when the BSY bit is set to one.

The Single-Byte Transfer (SBT) bit in the Command register is only used during information transfer type commands. When this bit is set in conjunction with one of these commands, the transfer counter is disabled and exactly one byte is to be transferred, regardless of the value in the Transfer Count register.

Refer to the Commands section for a description of the commands and their corresponding command codes.

BIT	7	6	5	4	3	2	1	0
	SBT	CC6	CC5	CC4	CC3	CC2	CC1	CC0

6.2.21 DATA REGISTER [Address 19 Hex]

The DATA register is used to transfer data bytes between the host and the SCSI bus during the SCSI information transfer phases (command, data, status, or message phase). It may be accessed by the processor during any type of information phase (simple Level II commands) or via the DMA/WD BUS interface during a SCSI Data In phase or Data Out phase (simple and combination Level II commands).

The DATA register is actually a port for the host interface into the interval twelve byte FIFO of the WD33C93A. The FIFO is used for all transfers (synchronous and asynchronous) between the SCSI bus and the host bus, for both DMA and processor access transfers. If the WD33C93A is to be halted for any reason (through ABORT, for example), then data transfers with this FIFO must continue until an interrupt occurs. This must be done so that the FIFO is returned to a ready state for subsequent transfers, and to flush incoming data to the host bus.

The DATA register is accessed by the host processor during a data phase when the CONTROL register DMA mode select bits are all reset (= 0), and when the DBR bit in the Auxiliary Status register is true. The processor writes (reads) the DATA register by loading the Address register with a Hex value of 19 and asserting the WE- (RE-) and CS- pins. This access also occurs during non-data phases.

When the Control register DMA mode selects bits are set for DMA mode or Burst mode, the DMA interface is enabled. In this case, the DATA register is written (read) when the DACK- and WE- pins are asserted in response to the assertion by the WD33C93A of the DRQ- pin.

When the WD-BUS is selected by the DMA mode select bits, the RCS- pin functions as an external buffer chip select and the WE- and RE- pins become outputs, allowing the WD33C93A to automatically transfer data between its DATA register and the external buffer. In this mode, bus control can be returned to the external processor or any device by negating the DRQ pin.

6.3 RESET CONDITIONS

6.3.1 HARDWARE RESET

The following results occur when the WD33C93A is reset by the assertion of the MR- signal:

- The LCI and PE bits in the Auxiliary Status register are reset to zero. The DBR bit in the Auxiliary Status Register is reset to zero. The BSY and CIP are reset to zero, and the INT bit (and INTRQ pin) is set to one when the hardware reset is complete.
- The Own ID register is reset to zero.
- Advanced mode is disabled.
- The ES, ER, and DSP bits in the Source ID register are reset to zero.
- The SCSI Status register is reset to zero.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The internal clock divider circuit is set to divide by two.
- The following host accessible registers are NOT affected by the MR- signal:
  - Registers 01 Hex through 15 Hex;
  - Source ID (16 Hex) register bits 0–3;
  - Command register (18 Hex).

NOTE: The SCSI Soft Reset may be implemented by using the SCSI bus reset signal to cause a reset of the WD33C93A (for example, OR the host power on reset signal with the received SCSI bus reset (RST) signal). The host may examine the registers that are not affected by the MR- signal to recover from the SCSI reset condition.

6.3.2 SOFTWARE RESET

The following results occur when the WD33C93A executes the Reset command:

- The DBR bit in the Auxiliary Status register is reset to zero. The INT bit (and INTRQ pin) is set to one when the Reset command is complete.
- All SCSI bus signals are reset to the negated state.
- The internal FIFO, internal transfer counter, offsets, and state machines are cleared.
- The Own ID register is interpreted and the clock divisor, host parity, and advanced mode are configured.
- Registers 01 Hex through 16 Hex are reset to zero. The Command register (18 Hex) is also reset to zero.
- The SCSI Status register is set as commanded by the EAF bit in the Own ID register.

7. COMMANDS
7.1 COMMAND LISTS

COMMAND CODE (Hex)	COMMAND	VALID STATES	LEVEL
00	Reset	D,T,I	I
01	Abort	D,T,I	I
02	Assert ATN	I	I
03	Negate ACK	I	I
04	Disconnect	T,I	I
05	Reselect	D	II
06	Select-With-ATN	D	II
07	Select-Without-ATN	D	II
08	Sel w/ATN-And-Transfer	D,I	II
09	Sel w/o ATN-And-Transfer	D,I	II
0A	Reselect-And-Receive Data	D	II
0B	Reselect-And-Send Data	D	II
0C	Wait-For-Select-And-Receive	D	II
0D	Send-Status-And-Command-Complete	T	II
0E	Send-Disconnect-Message	T	II
0F	Set IDI	D,T,I	I
10	Receive Command	T	II
11	Receive Data	T	II
12	Receive Message Out	T	II
13	Receive Unspecified Info Out	T	II
14	Send Status	T	II
15	Send Data	T	II
16	Send Message In	T	II
17	Send Unspecified Info In	T	II
18	Translate Address	D,T	II
20	Transfer Info	I	II

WD33C93A valid states:
D = Disconnected
T = Connected as a Target
I = Connected as an Initiator

Command Levels:
I = Level I command
II = Level II command

7.2 WD33C93A COMMAND TYPES

There are two basic types of WD33C93A commands: Level I and Level II. Level I commands may be issued while a Level II command is in progress (indicated by an Auxiliary Status of BSY = 1, CIP = 0) and, except for the "Abort" and "Reset" commands, do not generate an interrupt upon their completion. Level II command execution will always result in an interrupt. If a Level II command is issued while another Level II command is executing, unpredictable results may occur.

There are two types of Level II commands. 'Simple' Level II commands are associated with a single operation or phase (for example, selection or information transfer). 'Combination' Level II commands combine multiple phases into a single WD33C93A command to minimize interrupt overhead. The Initiator combination commands 'expect' certain SCSI bus phases at certain times during a sequence.These expected phases are based on common sequences performed by a Target on the SCSI bus; any deviation causes an interrupt. Target combination commands can also be chained together to minimize interrupt overhead by creating longer phase sequences.

NOTE: When using command chaining, care must be taken to ensure that all commands in the chain are initialized prior to issuing the command.

The WD33C93A will be in one of three "states" during operation: Disconnected, Connected as a Target, or Connected as an Initiator. Certain commands are valid only in particular states as indicated in the Command List. An attempt to issue a Level II command which is invalid for the present WD33C93A state will cause an "invalid command" interrupt. Level I commands issued in invalid states will be ignored.

7.3 ADVANCED MODE FEATURES

The WD33C93A has several new features included which add new functions to the original WD33C93 design. Some of these features cause the WD33C93A to be incompatible with the WD33C93. These features have been grouped together under the heading of 'Advanced Mode' features. These features are disabled when the WD33C93A is reset by the MR- signal (hardware reset). They must be enabled by the host by issuing the 'Reset' command with the 'Enable Advanced Features' (EAR) bit set in the Own ID register. The host can determine if advanced features have been enabled (thereby implying that a WD33C93A is installed) by examining the SCSI status register after issuing the 'Reset' command.

The features enabled by this bit are described below.

7.3.1 UNEXPECTED RESELECTION:

When in normal mode, a reselection when idle (ER = 1) or when disconnected during a Select-And-Transfer command (and the Target bus ID does not match the Destination ID register) causes an immediate interrupt after the reselection handshake is complete. In Advanced Mode, the WD33C93A will continue to the Message In phase to fetch the Identify message. If the WD33C93A was idle, the SCSI status register will be set to 81 Hex, and the Identify message will be in the Data register. If the WD33C93A was executing a Select-And-Transfer command, the SCSI status register will be set to 27 Hex, and the Identify message will be in the Target LUN register. In either case, the Source ID register will contain the SCSI bus ID of the reselecting Target, and the ACK signal remains asserted so that the Identify message may be rejected.

7.3.2 UNKNOWN SCSI COMMAND GROUPS

When a SCSI Command Descriptor Block is transferred on the SCSI bus, the command length in bytes is determined by the group code, which is found in bits 7–5 of the first command byte, or opcode. Group 0 (opcodes 00 to 1F Hex), group 1 (opcodes 20 to 3F Hex), and group 5 (opcodes A0 to BF Hex) commands are defined by the SCSI standard (X3.131–1986) as six, ten, and twelve byte commands, respectively. All other command groups are undefined by that standard. In normal mode, the WD33C93A will assume that these undefined groups are six byte commands when executing Select-And-Transfer or Wait-For-Select-And-Receive commands. In Advanced Mode, the following events will occur:

- **Select-And-Transfer:** When loading the CDB into the CDB registers prior to issuing the command, the host also loads the expected command length into the OWN ID register. The WD33C93A uses this value to make sure the correct number of bytes are then transferred in the command phase.
- **Wait-For-Select-And-Receive:** When receiving the CDB from the Initiator, the WD33C93A will check the first CDB byte as soon as it is received. If the group is undefined, an interrupt will occur so that the host processor can examine the first command byte in the CDB 1ST register, and then load the Total command length into the Own ID register. The SCSI status register is set to 87 Hex, and the Command Phase register is set to 31 Hex, when this interrupt occurs.

After the interrupt, the WD33C93A will only accept a Resume Wait-For-Select-And-Receive command, Abort, Disconnect, or Reset command. All other commands are invalid; during the interrupt processing, the WD33C93A will continue to transfer the first six bytes of the command into its internal FIFO.

7.3.3 DATE PHASE DIRECTION

During a Select-And-Transfer command in normal mode, the Data phase direction is determined solely by the Target; if this direction does not match the direction expected by the host, the WD33C93A will not detect this error but expects that the transfer will continue. In Advanced Mode, the DPD bit in the Destination ID register is compared with the state of the I/O signal on the SCSI bus. If the expected and actual directions do not match, an interrupt will occur with 'unexpected phase' status in the SCSI status register.

7.4 LEVEL I COMMANDS

7.4.1 RESET (00 HEX)

The Reset command performs a similar function to the hardware reset caused by asserting the MR- pin except that the Own ID register is sampled for information concerning the operating configuration of the WD33C93A. The WD33C93A is also initialized as described in the RESET CONDITIONS section. The Reset command may be executed in any WD33C93A state and will force the WD33C93A into the Disconnected state, aborting any previously issued command in progress. Upon completion of the Reset command, an interrupt is generated the SCSI STATUS will be 00 Hex or 01 Hex, depending on the contents of the OWN ID register.

7.4.2 ABORT (01 HEX)

The Abort command is valid in any WD33C93A state: Disconnected, Target, or Initiator. The Abort command has different effects depending on the state and the command that is currently executing, as described below:

Disconnected State: In the Disconnected state, the Abort command may be used to halt an attempted Select, Select-and-Transfer, Reselect, or Reselect-and-Transfer command. If the Abort command is issued following a Select or Reselect command and the WD33C93A has won arbitration, the WD33C93A releases the SCSI bus by removing the Bus ID bits while SEL- is asserted and checking for a negated BSY- signal. If, after at least 200 µS, there is no BSY- response, the WD33C93A goes to a Bus Free condition, and a "paused/aborted" interrupt is generated. If there is a response within this time period, then a "successful completion" interrupt will result instead. If the WD33C93A has not yet won arbitration, it will immediately abort the Select or Reselect command.

Target State: When the WD33C93A is in a Connected as a Target state, the Abort command may be used to abort RECEIVE, SEND, or the data phase portion of a Target combination command. When issuing an Abort in the Connected as a Target state, the following rules apply:

1. When an Abort command is issued to abort a SEND or Reselect-and-SEND command, the local processor must not service any data request (DBR, DRQ, etc.) from the WD33C93A until an interrupt from the WD33C93A occurs. This is required to allow the FIFO to clear; the Abort processing will not complete until the FIFO contents are flushed to the SCSI bus. The WD33C93A removes the data request at an arbitrary time during the Abort command processing and the data request is not valid once the Abort command is written to the COMMAND register.

2. When an Abort command is issued to abort a RECEIVE or Reselect-and-RECEIVE command, the local processor must CONTINUE to service any data request (DBR, DRQ, etc.) from the WD33C93A until an interrupt from the WD33C93A occurs. This is required to allow the FIFO to clear; the Abort processing will not complete until the FIFO contents are flushed to the local processor.

After the Abort command is processed and the local processor has received the interrupt indicating this, the TRANSFER COUNT register contains the number of bytes that were not successfully transferred with the SCSI bus. The WD33C93A remains in the connected as a Target state. The WD33C93A is now ready to receive any appropriate Target mode command, including a resume of the command that was aborted.

Initiator State: When the WD33C93A is in a connected as an Initiator state, the Abort command may be used to abort TRANSFER INFO, TRANSFER PAD, Select, or Select-and-TRANSFER command. When issuing an Abort in the connected as an Initiator state, the local processor must continue to service any data request (DBR, DRQ, etc.) from the WD33C93A until an interrupt from the WD33C93A occurs. This is required to allow the FIFO to clear; the Abort processing will not complete until the FIFO contents are flushed to the data destination.

After the Abort command is processed and the local processor has received the interrupt indicating this, the TRANSFER COUNT register contains the number of bytes that were not successfully transferred with the SCSI bus. The WD33C93A remains in the connected as an Initiator state. The WD33C93A is now ready to receive any appropriate Initiator mode command, including a resume of the command that was aborted.

29

7.4.3 DISCONNECT (04 HEX)

The Disconnect command may be used in either the Target or the Initiator connected states. In the Target role, the Disconnect command is the normal procedure for disconnecting from the SCSI bus following the information transfer phase. In the Initiator role, Disconnect can be used to release the bus following a timeout condition. The Disconnect command causes the immediate release of all bus signals and, in Target mode, returns the SCSI bus to the Bus Free phase. If the Disconnect command is issued during an active Level II command, the Level II command is immediately terminated and the WD33C93A transitions to the Disconnected state.

7.4.4 ASSERT ATN (02 HEX)

The Assert ATN command is only valid when Connected as an Initiator. It is normally used to allow the Initiator to inform a Target that it has a message pending (the Target is expected to respond by performing a Message Out Phase).

ATN- is automatically negated:

- before the last byte of a Transfer Info command issued in response to the Message Out phase;
- when the Identify message out is transferred to the Target during a Select-and-Transfer command;
- when a SCSI Bus Free phase occurs.

The Select-with-ATN and Select-with-ATN-and-Transfer commands will cause the WD33C93A to automatically assert ATN- prior to the release of SEL- providing the bus arbitration is won.

7.4.5 NEGATE ACK (03 HEX)

The Negate Ack command causes ACK- to be negated. It is used when Connected as an Initiator following Message-In type Transfer Info commands, or when the WD33C93A has detected a parity error on any received information and the Halt on SCSI Parity Error (HSP) bit is set. Host parity errors do not affect the ACK- signal. For all other Initiator transfers, ACK- negation is automatic.

In the case of a Message-In transfer, incoming messages may be rejected and the Initiator may indicate its intent to send either a "Message Reject" or a "Message Parity Error" Message by issuing the Assert ATN command prior to issuing the Negate Ack command. If the incoming message is to be accepted, only the Negate Ack command should be issued.

During non-Message-In transfers, if the Transfer command is terminated by parity error, the Assert ATN command can again be issued prior to Negate ACK, this time indicating the Initiator's intent to send an "Initiator Detected Error" Message.

7.4.6 SET IDI (0F HEX)

The Set IDI command is used in the Initiator role to support overlapped SCSI operations. If a SCSI command is executing via a Select-and-Transfer command, then the Set IDI command may be used to set the IDI bit in the Control register, which then causes an interrupt to occur upon a Target disconnection. This ability allows the IDI bit to be left reset when the first SCSI operation is started, which may reduce the number of WD33C93A interrupts, yet also allows a second operation to be started when needed without waiting for the first operation to be completed.

7.5 SIMPLE LEVEL II COMMANDS

7.5.1 SELECT-WITH-ATN (06 HEX)

Select-with-ATN is valid only in the Disconnected state and when issued will cause the WD33C93A to select a Target. Before issuing this command, the SCSI Bus ID of the Target device should be written into the Destination ID register. When the Select-with-ATN command is issued, the WD33C93A begins bus arbitration. If the WD33C93A is selected or reselected by another device during the arbitration, the Select-with-ATN command is aborted and a "service required" interrupt (8x Hex) is generated.

Should the WD33C93A win the arbitration, SEL- and ATN- are asserted, the Target and Initiator Bus IDs are placed on the SCSI data bus, and then BSY- is deasserted. At this time, a timeout sequence whose length is determined by the value in the Timeout Period register begins. If BSY- is not asserted by the Target before a timeout occurs, the WD33C93A begins its selection abort sequence (as described in the Abort command description), and if there is no Target response the Select-with-ATN command is terminated and a "terminated" interrupt is generated. If the Target responds before the timeout period has elapsed or before the selection abort sequence is complete, the WD33C93A negates the Sel- signal, putting the WD33C93A in a Connected-as-an-Initiator state. A "successful completion" interrupt indicates that the Select-with-ATN command has been completed successfully.

If the WD33C93A does not win the arbitration or there is no response from the Target and the timeout feature is disabled, the Select-with-ATN command can be aborted with an Abort command. When the Abort command is successfully executed under these circumstances, the WD33C93A is disconnected from the bus and a "paused/aborted" interrupt is generated.

7.5.2 SELECT-WITHOUT-ATN (07 HEX)

The Select-without-ATN command is identical to the Select-with-ATN command except that ATN- is not set during the Selection Phase.

7.5.3 RESELECT (05 HEX)

The Reselect command is identical to the Select-without-ATN command except that the I/O signal is asserted upon completion of the Arbitration Phase. Successful completion of the Reselect command results in the WD33C93A being Connected as a Target.

7.5.4 RECEIVE (10–13 HEX)

There are four RECEIVE commands which are distinguished from each other only by the state of three SCSI interface signals and the type of data that is transferred. These commands, consisting of the Receive Command, Receive Data, Receive Message Out, and Receive Unspecified Info Out commands are valid only in the Connected-as-a-Target state. The type of Receive command selected determines the state of the I/O-, C/D-, and MSG- outputs during the command according to the following chart below (1 = asserted).

The Receive commands are information transferrring commands and are therefore dependent on the SBT bit in the Command register for determination of a successful completion. In addition to a termination caused

RECEIVE COMMAND TYPE	OPCODE	MSG	C/D	I/O
Receive Command	10	0	1	0
Receive Data	11	0	0	0
Receive Message Out	12	1	1	0
Receive Unspecified Info Out	13	1	0	0

by reset (via either a Reset command being issued or assertion of the MR- pin), a Receive command completion or termination will occur under any of these conditions: (1) The internal transfer counter is disabled (SBT = 1 or the Transfer Count register is loaded with zero) and a single byte has been read from the Data register; (2) The counter has decremented to zero (with SBT = 0) indicating that the specified number of bytes have been transferred; (3) A parity error has been detected on one of the received data bytes (and HSP = 1); (4) The ATN- pin is asserted (and HA = 1); (5) The Abort command is issued; or (6) A Disconnect command is issued.

When the Receive command is completed as a result of receiving the correct number of bytes, a "successful completion" interrupt will be generated. If a parity error has caused termination, a "terminated" interrupt will instead be generated. In this case, the Transfer Count register will contain the number of bytes yet to be transferred. After any completion or termination of the Receive commands except those due to a subsequent Disconnect command or reset, the WD33C93A is in the Connected-as-a-Target state.

As data transfer commands, the Receive commands are dependent on the DMA mode select bits in the Control register for the Data register accessing mode. These bits determine whether the Data register accesses will be handled by the processor or through a DMA/WD interface. When the processor is required to read the Data register (i.e. DMA mode select bits = 0), it must monitor the DBR status bit (in Auxiliary Status) to determine when a byte is available for reading. During Receive commands, this status bit will be reset when a byte is read from the Data register and set when a byte is loaded into the Data register via the SCSI interface. DBR is also reset when a Receive command is issued.

All information transfers involving other than data information are asynchronous. However, if the information phase involves data transfers, the Synchronous Transfer register will be evaluated. In this case, any selected offset other than zero results in synchronous transfers. The minimum Transfer Period for both types of transfers is determined by the transfer period bits in this same register.

7.5.5 SEND (14–17 HEX)

As in the case of the RECEIVE commands, there are four Send commands which are distinguished only by the state of the I/O-, C/D-, and MSG- pins and the type of data that is transferred. The four Send commands, also valid in the Connected-as-a-Target state only, are the Send Status, Send Data, Send Message In, and Send Unspecified Info In commands. The SCSI pin states during the Send commands are determined by the particular commands as follows shown in the chart below (asserted = 1).

The Send commands are also information transferring commands and as such are also dependent upon the SBT bit in the Command register for command completion. In addition to that caused by reset (via either a Reset command being issued or assertion of the MR- pin), a Send command completion or termination will occur under any of these conditions: (1) The internal transfer counter is disabled (SBT = 1 or the Transfer Count register is loaded with zero) and a single byte has been read from the Data register; (2) The counter has decremented to zero (with SBT = 0) indicating that the specified number of bytes have been transferred; (3) A parity error has been detected on one of the data bytes from the host (and HHP = 1); (4) The ATN- pin is asserted (and HA = 1); (5) The Abort command is issued; or (6) A Disconnect command is issued. The WD33C93A remains Connected-As-A-Target following the Send command completion/termination unless the Disconnect command or reset was used to force a termination.

During a Send command, Data register accessing is controlled by the DMA mode select bits in the Control register. When these bits are set to the appropriate mode, loading of the Data register is accomplished by a DMA controller or through the WD-Bus interface. If the DMA mode select bits are zero, the processor must poll the Auxiliary Status register and can write to the Data register only when the Data Buffer Ready bit is set (DBR = 1). Send commands cause the DBR bit to be reset every time the processor loads a byte into the Data register and set when a byte is transferred from the Data register onto the SCSI data bus. The DBR bit will also be set upon issuing a Send command.

As in the case of Receive commands, synchronous transfers will occur only when data transfers are involved and an offset other than zero is selected.

7.5.6 TRANSFER (20 HEX)

Transfer Info is used to send and receive data, command, status, and message information.

SEND	COMMAND TYPE	OPCODE	MSG	C/D	I/O
Send	Status	14	0	1	1
Send	Data	15	0	0	1
Send	Message In	16	1	1	1
Send	Unspecified Info In	17	1	0	1

The first Req- assertion following connection as an Initiator results in a "service required" interrupt. The processor should examine the SCSI Status register to determine the type and direction of information transfer requested by the Target, and then issue a Transfer Info command in response. While an Initiator, the WD33C93A will also generate an interrupt each time the Target device requests a new type of information transfer phase.

As in the case of the Send and Receive commands, when the Transfer Info command completion is to be dependent upon the internal transfer counter, the processor should load the Transfer Count register prior to issuing this command. The DMA mode select bits in the Control register, the offset and transfer period bits in the Synchronous Transfer register, and the SBT bit in the Command register are used during Transfer Info commands just as they are during the Send-And-Receive commands. However, for processor access of the Data register during Transfer Info commands (when the DMA mode select bits are zero, or the bus phase is other than Data phase), behavior of the Data Buffer Ready (DBR) status bit is determined by the direction of information transfer as defined by the I/O- pin. When the transfer is from Initiator to Target, the DBR bit is reset by writing to the Data register and is set when the byte is transferred from the Data register onto the SCSI data bus. When the transfer is from Target to Initiator, DBR is set when a byte is received over the SCSI data bus and transferred into the Data register and is reset by reading the Data register. DBR is also reset whenever a Transfer Info command is issued.

There are several causes of a Transfer Info command completion/termination in addition to a reset. Just as for a Send or Receive command, the Transfer Info command can be terminated by issuing a subsequent Disconnect or Abort command. The Abort command will cause a "paused/aborted" interrupt to be generated after execution (leaving the WD33C93A in a connected state), while the Disconnect command causes an immediate disconnect and does not generate an interrupt.

A Transfer Info command will be either completed or paused when the specified number of bytes (either a single byte or multiple bytes as defined by the Single-Byte Transfer bit in the Command register) have been sent or received. The WD33C93A generates a "successful completion" interrupt only after receiving another REQ- from the Target during non-Message In information phases, but generates a "paused/aborted" interrupt for Message-In phases without waiting for an additional REQ- (Note that when the completed Transfer Info command was a Message-In transfer phase, the ACK- pin will be left asserted by the WD33C93A in the last REQ-ACK cycle of the command, and the processor is required to issue a negate ACK or an Assert ATN followed by a Negate ACK command to accept or reject the message respectively).

If a parity error is detected on a data byte received from the SCSI bus (and HSP = 1), or on a data byte received from the host (and HHP = 1), then the WD33C93A will terminate the command and, for SCSI parity errors, will leave ACK- asserted (to also halt the Target). In this case a "terminated" interrupt is generated. Finally, negation of the BSY- signal (i.e. the Target suddenly disconnects) or a transition in the I/O-, C/D-, and/or MSG- pins during a Transfer command will also terminate the command and generate a "terminated" interrupt.

If a parity error is detected on a received byte but parity error command termination is disabled (HSP = 0 or HHP = 0, as appropriate), the WD33C93A will still set the Parity Error status bit in the Auxiliary Status register but will not terminate the command as a result of this error.

7.5.7 TRANSLATE ADDRESS (18 HEX)

The Translate Address Command is used to perform a logical-to physical-address translation. Certain SCSI commands involve a logical address which may be up to 32 bits in length. When a command is detected which requires address translation, the processor can reload the logical address into the WD33C93A Logical Address register and then issue the Translate Address command to have the WD33C93A do the conversion. Upon receiving a "successful completion" interrupt, the processor can read three WD33C93A registers to extract the Cylinder Number, Head Number, and Sector Number corresponding to the logical address. The disk parameters contained in the Total Sectors, Total Heads, and Total Cylinders registers must also be valid before issuing a Translate Address command.

If automatic compensation for spare sectors is to be performed by the WD33C93A, then the number of spare sectors per cylinder and total number of sectors per cylinder must also be loaded in the Head Number and Cylinder Number registers respectively. A "terminated" interrupt will occur if any division operation performed during this command results in an overflow.

7.6 COMBINATION LEVEL II COMMANDS

7.6.1 SELECT-AND-TRANSFER (08 AND 09 HEX)

The Select-And-Transfer commands are capable of greatly reducing the host or local processor interrupt-handling burden by enabling the WD33C93A's internal microprocessor to manage the low-level SCSI protocol.

This results in as few as one interrupt per SCSI operation. Select-And-Transfer commands are used when in an Initiator role, and typically consist of at least the following SCSI phases: (1) Selection of a Target device; (2) Sending of a command; (3) Reception of status information; and (4) Reception of a Command Complete Message. These commands optionally consist of a Data Transfer phase and additional Message Transfer phases. During execution of a Select-And-Transfer command, the Command Phase register will be updated to indicate which bus phases of the SCSI operation have been completed, so that upon completion or termination of the command, the WD33C93A may be interrogated to find out where the SCSI operation was stopped.

The two Select-And-Transfer commands are distinguished from each other only by whether or not the ATN- pin is asserted during the Selection phase. Select-And-Transfer commands directly support Group 0 (6-byte CDB), Group 1 (10-byte CDB), and Group 5 (12-byte) SCSI commands. In addition, the ability to have ATN- asserted during Selection supports the SCSI Message Protocol which calls for an Identify Message Out phase following the Selection. When the Select w/Atn-And-Transfer commands is issued, the WD33C93A expects the first information phase request from the Target to be a Message Out phase, whereas for a Select w/o Atn-and-Transfer command, the first information phase request is expected to be a Command Out phase.

When a Select-And-Transfer command is issued, the WD33C93A arbitrates for the bus and selects a Target just as during a Select command. If the Target does not respond before a timeout occurs, the Select-And-Transfer command is terminated and a "terminated" interrupt is generated. Failure to complete the Selection phase is also indicated by the fact that the Command Phase register contains all zeroes. If the Selection is successful, no interrupt is generated, but the Command Phase register will be set to a Hex 10.

After completing the Selection phase, the WD33C93A begins an information transfer phase. If ATN- has been asserted (i.e. a Select w/Atn-And-Transfer command was issued), the WD33C93A expects the Target to respond with a Message Out phase. If the first information phase request is other than a Message Out request, the WD33C93A will terminate the command and generate a "terminated" interrupt. However, when the Target does request a Message Out phase, the WD33C93A will respond by automatically sending an Identify Message. This single byte message is of the binary form: 1r000ttt, where r = 1 if the Enable Reselect bit in the Source ID register is equal to 1, and ttt is the encoded Target Logical Unit Number contained in the Target LUN register. Once the Identify Message has been sent, the WD33C93A will set the Command Phase register to Hex 20.

Following the Message Out phase (or Selection phase when ATN- was not asserted during Selection), a Command phase is expected by the WD33C93A. Again, and throughout the entire Select-And-Transfer command execution, if the Target requests an unexpected information phase type, the WD33C93A terminates the command and generates a "terminated" interrupt. If the Command phase is requested in this situation, the WD33C93A will extract the SCSI command from the internal Command Descriptor Block registers and send 6, 10, or 12 bytes of command information as determined by its evaluation of the SCSI command code in the CDB1 register. The Command Phase register is set to Hex 30 before the first Command byte is sent and then increments with each byte transferred, so that for a 12-byte CDB command the Command Phase register will contain Hex 3C when all bytes of the CDB have been transferred.

After the Command phase, the WD33C93A expects either a Data In phase, Data Out phase, Status phase, or Message In phase. If the Target is requesting a Message In phase, a pending disconnection is assumed. The WD33C93A therefore expects to receive either a Save Data Pointer Message (Hex 02) or a Disconnect Message (Hex 04). If either message is incorrect, or if a different message is received, a "terminated" interrupt will be generated to alert the processor of that fact and to allow the message to be read from the Data register. A "terminated" interrupt will also be generated if the Target disconnects before sending the Disconnect message. When a correct Save Data Pointer message is received, a "paused/aborted" interrupt is generated and the Select-And-Transfer command terminated to allow the processor to save the SCSI data pointers. However, if a Disconnect message is received, the Command Phase register will be updated to Hex 42 and command execution continues.

When the actual Target-disconnection does occur, the Command Phase register is updated to Hex 43 and if the IDI bit is set, the WD33C93A terminates the Select-And-Transfer command by generating an 85H interrupt. However, if the IDI bit is reset, then instead the WD33C93A sits in an idle state, waiting for the Target to reconnect. If a different Target device Reselects the WD33C93A, a "terminated" interrupt is generated. However, if the original Target Reselects the WD33C93A, no interrupt is generated and the Command Phase register is set to Hex 44.

Following the original Target Reselection, the WD33C93A expects a Message In phase which should consist of the Target sending an Identify Message. This single-byte message should be of the binary form: 10000ttt, where ttt is the Target Lun. If the data received by the WD33C93A is different or the Target Lun specified in this byte does not match the contents of the Target Lun register, a "terminated" interrupt is generated and the Message byte may be examined by the processor. A correct Identify Message In phase results in the Command Phase register being updated to Hex 45.

After the Identify Message is received from the Target or immediately after the Command Out phase (when there is no disconnection), a Data In phase, Data Out phase,

or Status phase should occur. If the Transfer Count register contains any non-zero value, then the WD33C93A will expect a Data Transfer phase. If Advanced Features are enabled, then the DPD bit will be examined to verify the correct data direction. If the data direction is incorrect, then a "terminated" interrupt is generated. In this phase, the WD33C93A will use the Transfer Count register to determine the number of bytes to be transferred, and all host-side Data register accesses will be accomplished via the method selected by the DMA mode select bits in the Control register. When the internal counter reaches zero, the Data Transfer phase is complete and the Command Phase register is set to Hex 46.

Note that any number of disconnection/reconnection cycles may occur during the Data Transfer phase so long as they are accomplished according to the defined message protocol. The Command Phase register will cycle through the disconnect phases (41-45) with each disconnection and subsequent reconnection until all of the data has been transferred and the Data Transfer phase is complete.

A Status phase is expected by the WD33C93A following the Data Transfer phase (or instead of the Data Transfer phase when the Transfer Count register contains a value of zero). At the start of the Status phase, the Command Phase register is loaded with Hex 47. Upon completion of the Status phase, the Command Phase register will be updated to Hex 50, and the received status byte is stored in the Target Lun register where it can be read upon completion of the command.

Following completion of the status-byte transfer, a Message In phase is expected. The WD33C93A expects the Target to send a Command Complete Message (Hex 00) to indicate that the SCSI command operation has been completed. After the WD33C93A receives this Command Complete Message, the Command Phase register advances to Hex 60, and if the EDI bit is reset, a "successful completion" interrupt is generated. The processor should then read the Target Lun register to examine the Target status. An additional interrupt will then occur when the SCSI bus goes to the Bus Free state, or when another REQ- is asserted to begin an information transfer phase (as in SCSI linked commands). If the EDI bit is set, the "successful completion; interrupt will be suppressed until the Target disconnects from the SCSI bus.

At any time during execution of the Select-And-Transfer commands, an abnormal or unexpected condition will cause the WD33C93A to terminate the command, set the appropriate status qualifiers, and generate a "terminated" interrupt. If the termination occurred during an information transfer phase, the WD33C93A will be left in a Connected-as-an-Initiator state (unless termination was due to a sudden Target disconnection). Command termination during any other phase will result in the WD33C93A being in a Disconnected state. Transfer

COMMAND PHASE	MEANING
00	No SCSI bus device has been selected. The WD33C93A is in the disconnected state.
10	The Target has been selected. The WD33C93A is now in the connected as an Initiator state.
20	An Identify message has been sent to the Target.
30	Command phase has started, no bytes transferred.
3x	Command phase, x bytes have been transferred.
41	Save Data Pointer message received.
42	Disconnect message received, bus not free.
43	Target has disconnected (SCSI bus free) following a successful transfer of a Disconnect message. The WD33C93A is now in the disconnected state.
44	The WD33C93A has been reselected by the Target whose SCSI bus ID matches the value in the DESTINATION ID register. The WD33C93A is now in the connected as an Initiator state.
45	The WD33C93A has received an Identify message from the Target whose Logical Unit Number matches the value in the TARGET LUN register.
46	The number of bytes specified in the TRANSFER COUNT register have been transferred to/from the Target during a Data Out/In phase.
47	The Target has begun a Receive Status phase.
50	The WD33C93A has successfully received a Status byte from the Target and stored it in the TARGET LUN register.
60	The WD33C93A has successfully received a Command Complete message from the Target.

COMMAND PHASE	MEANING
10	Resume after Target selection is complete.
20	Resume after Identify message out. Command phase is expected; an implied Negate ACK occurs.
30	Resume when Command phase has begun (REQ- asserted).
41	Resume after Command phase or after Save Data Pointer message. Data, Status, or Message In phases are expected. An implied Negate ACK occurs.
42	Resume to complete Disconnect Message In; an implied Negate ACK occurs.
44	Resume after reselection by a Target.
45	Resume to transfer more data in a data transfer phase. May expect Status or Message In as well. An implied Negate ACK occurs.
46	Resume after the data phase has been completed, expecting Status phase or a Save Data Pointer/Disconnect Message In phase. An implied Negate ACK does not occur.
50	Resume to complete a Status phase; an implied Negate ACK occurs.
60	Resume to complete a Command Complete message from the Target; an implied Negate ACK occurs.

commands may be used to handle the exception by transferring messages with the Target.

The following table summarizes the possible values that the Command Phase register can take during the **Select-And-Transfer** commands, and their meanings relative to command termination:

A "Resume Select-And-Transfer" command is assumed whenever a normal "Select-And-Transfer" command is issued while the WD33C93A is in the Connected-Initiator state. When the "Resume" is issued, the WD33C93A examines the Command Phase Register to determine where to restart the Select-And-Transfer command execution. This feature, in conjunction with the Intermediate Disconnect Interrupt enabled, allows support of multi-threaded or overlapped I/O on the SCSI bus.

The table above briefly describes the valid settings of the Command Phase register when resuming a Select-And-Transfer command:

7.6.2 RESELECT-AND-TRANSFER (0A AND 0B HEX)

The Reselect-And-Transfer commands include the Reselect-and-Receive Data and the Reselect-and-Send Data commands. These commands cause the WD33C93A to execute certain common SCSI bus phase sequences as a Target following a Reselection phase. These phases are determined by which command is sent, and the setting of two bits: the EDI bit in the Control Register; and the SCC bit in the Destination ID register. The SCSI bus phase sequences are summarized below. Refer to the command descriptions of the Send-Status-And-Command-Complete and Send-Disconnect-Message commands for details on those sequences.

(1) Reselect-and-Receive command, EDI = 0, and SCC = don't care:
- Reselection phase;
- Send Identify Message In;
- Receive Data Out phase;
- Completion interrupt.

(2) Reselect-and-Send command, EDI = 0, and SCC = don't care:
- Reselection phase;
- Send Identify Message In;
- Receive Data In phase;
- Completion interrupt.

(3) Reselect-and-Receive command, EDI = 1, and SCC = 0:
- Reselection phase;
- Send Identify Message In;
- Receive Data Out phase;
- Chain to Send-Status-and-Command Complete.

(4) Reselect-and-Send command, EDI = 1, and SCC = 0:
- Reselection phase;
- Send Identify Message In;
- Receive Data In phase;
- Chain to Send-Status-And-Command Complete.

(5) Reselect-and-RCV command, EDI = 1, and SCC = 1:
- Reselection phase;
- Send Identify Message In;
- RCV Data Out phase;
- Chain to Send-Disconnect-Message.

(6) Reselect-and-Send command, EDI = 1, and SCC = 1:

- Reselection phase;
- Send Identify Message In;
- Send Data In phase;
- Chain to Send-Disconnect-Message.

If the reselection attempt times out during a Reselect-And-Transfer command, ATN- is asserted and HA = 1, or if a parity error is detected on an incoming data byte (and HSP = 1 or HHP = 1, depending on data direction), the command will be terminated and the appropriate status will be set. In this case, the Command Phase register should be evaluated to determine the last successfully completed phase. If none of these conditions occurs, all phases complete normally, and if EDI = 0, then a "successful completion" interrupt would be generated at this point. However, if EDI = 1, no interrupt is generated and command chain occurs (as described above).

COMMAND PHASE	MEANING
00	No SCSI bus device has been reselected. The WD33C93A is in the disconnected state.
10	The WD33C93A has successfully reselected the Initiator. The WD33C93A is now in the connected as a Target state.
20	The Identify message has been successfully sent to the Initiator.
46	The requested data transfer has been completed.

The following table summarizes the possible values that the Command Phase register can take during the Reselect-And-Transfer commands, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

A "Resume Reselect-And-Transfer" command is assumed whenever a normal "Reselect-And-Transfer" command is issued while the WD33C93A is in the Connected as a Target state. When the "Resume" is issued, the WD33C93A examines the Command Phase Register to determine where to restart the Reselect-And-Transfer command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the Command Phase register when resuming a Reselect-And-Transfer command:

COMMAND PHASE	MEANING
10	Resume after Initiator reselection is complete; start with Identify Message Out.
20	Resume after Identify Message Out; start with data transfer phase. If Transfer Count is zero, no data transfer phase occurs. In either case, a chain to another combination command can occur if enabled.

7.6.3 WAIT-FOR-SELECT-AND-RECEIVE (0C HEX)

The Wait-For-Select-And-Receive causes the WD33C93A to idle until it is selected by an Initiator, at which time the WD33C93A will enter the Target mode and message and command information will automatically be requested. As an option, the WD33C93A may be programmed to disconnect when a SCSI read command is received while executing a Wait-For-Select-And-Receive command. Use of this command therefore eliminates the interrupts which normally occur after selection and after each subsequent SCSI bus phase, and results in very short bus-connect time during SCSI read commands.

If ATN- was asserted by the Initiator during the selection phase, the WD33C93A will first execute an implied "Receive Message Out" command to get the Identify message from the Initiator, before continuing on with the implied "Receive Command" to receive the SCSI command information. The SCSI command information (CDB) will be stored in the CDB registers (Hex addresses 03 to 0E), and if a valid Identify message is received, it will be saved in the Target Lun register (Hex address 0F). The number of command bytes requested by the WD33C93A is determined by the SCSI group code in the first byte of the CDB.

After the WD33C93A is selected and receives all valid command and message information, a "successful completion" interrupt will normally be generated to allow the local processor to read out and interpret the SCSI CDB. However, by setting the EDI bit prior to issuing a Wait-For-Select-And-Receive command, the WD3?C93A is enabled to perform an automatic disconnect when a SCSI read command is received. There-

fore, when EDI=1 and the 1st CDB byte received contains a 6, 10 or 12 byte read command code, then the WD33C93A will temporarily suppress the interrupt and chain to begin execution of a Send-Disconnect-Message command. An interrupt will then be generated after completion of this command, which normally would indicate a transition to the bus free condition. Refer to the Send-Disconnect-Message command description for more details.

If during execution the message or command information received from the Initiator is invalid, the implied receive command will be terminated and the appropriate status reported. In this case, the Command Phase register should be read to determine which phase of the Wait-For-Select-And-Receive command was last completed before the error condition occurred. A Command Phase Hex value of Hex 10 indicates that the WD33C93A was successfully selected. A Hex value of 20 indicates that a message was received from the Initiator, and when the WD33C93A begins receiving command bytes, the Command Phase is set to Hex 30 and increments with each byte received (to a maximum of 3C for a 12-byte CDB command).

The following table summarizes the possible values that the Command Phase register can take during the Wait-For-Select-And-Receive command, and their meanings relative to command termination. See other command descriptions for additonal values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	The WD33C93A has not been selected. The WD33C93A is in the disconnected state.
10	The WD33C93A has been successfully selected by the Initiator. The WD33C93A is now in the connected as a Target state.
20	The Identify message has been successfully received from the Initiator.
30	The WD33C93A has begun command phase by setting the SCSI bus phase signals and asserting REQ-.
31	The WD33C93A has transferred 1 command byte from the Initiator. The SCSI Status may indicate the need for the host to load the command size into the OWN ID register.
3x	The WD33C93A has transferred x command bytes from the Initiator.

A "Resume Wait-For-Select-And-Receive" command is assumed whenever a normal "Wait-For-Select-And-Receive" command is issued while the WD33C93A is in the Connected as a Target state. When the "Resume" is issued, the WD33C93A examines the Command Phase Register to determine where to restart the Wait-For-Select-And-Receive command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the Command Phase register when resuming a Wait-For-Select-And-Receive command:

COMMAND PHASE	MEANING
10	Resume after selection by the Initiator is complete; start with Identify Message Out if ATN is asserted, otherwise, start with command phase.
20	Resume after a message out; check the received message in the Target Lun register for a valid Identify message.
30	Resume after Identify message out. Start with command phase.
31	Resume after the WD33C93A has transferred 1 command byte from the Initiator. This resume point is used only when an unknown group code has been detected in Advanced Mode, and the command size has been loaded into the Own ID register.

7.6.4 SEND-STATUS-AND-COMMAND-COMPLETE (0D HEX)

The Send-Status-And-Command-Complete command is valid in the Target role, and is used to complete a SCSI operation by transferring the appropriate status information to the Initiator prior to disconnection from the SCSI bus. This command also supports linked SCSI operations by optionally allowing a linked command-complete message to be sent after the status is transferred. Linked command complete messages are controlled by the CDB12 register with bits that correspond to the standard linked command control bits in the CDB.

Before a Send-Status-And-Command-Complete command is issued, the CDB11 register must be loaded with a status byte which will then be transferred across the SCSI bus. Also, the link control bits from the current CDB must be loaded into the CDB12 register to ensure that the correct sequence occurs. Note that the bits used by the WD33C93A are identical in meaning to the SCSI standard link control bits. The host processor may simply load the control byte from the current SCSI command into CDB12 to get the correct function. As the command execution progresses, the Command Phase register will be updated to indicate the last phase completed.

The possible sequences caused by this command are as follows:

(1) CDB12 bit0 = 0, bit1 = don't care: The status byte in CDB11 is sent, followed by a Command Complete message (00 Hex). A "successful completion" interrup now occurs.

(2) CDB12 bit0 = 1, bit1 = 0: The status byte in CDB11 is sent, followed by a Linked Command Complete message (0A Hex). A chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to fetch the next CDB from the Initiator. WD33C93A command execution proceeds as described for that command.

(3) CDB12 bit0 = 1, bit1 = 1: The status byte in CDB11 is sent, followed by a Linked Command Complete with Flag message (0B Hex). A chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to fetch the next CDB from the Initiator. WD33C93A command execution proceeds as described for that command.

A Send-Status-And-Command-Complete command may be terminated by ATN- asserted when HA = 1, or when a Disconnect or Reset command is issued. In addition, it may be aborted on a SCSI bus-phase boundary by issuing an Abort command.

The following table summarizes the possible values that the Command Phase register can take during the Send-Status-and-Command-Complete command, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No operation occurred; typically, ATN- was found to be asserted.
50	Status phase transfer completed.
60	Command Complete message transfer completed.
61	Linked Command Complete message transfer completed.

A "Resume Send-Status-And-Command-Complete" command is assumed wheneve a normal "Send-Status-And-Command-Complete" command is issued while the WD33C93A is in the Connected as a Target state. When the "Resume" is issued, the WD33C93A examines the Command Phase Register to determine where to restart the Send-Status-And-Command-Complete command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the Command Phase register when resuming a Send-Status-And-Command-Complete command:

COMMAND PHASE	MEANING
50	Resume after status phase. Start with command complete message. May chain to command fetch if commanded to do so.

7.6.5 SEND-DISCONNECT-MESSAGE (0E HEX)

The Send-Disconnect-Message command is a Target-role command which may be used to disconnect from the SCSI bus at any time during a SCSI command sequence. This command consists of sending a Disconnect message byte, followed by physical disconnection from the bus (SCSI bus free). An interrupt is generated only after transition to bus free occurs. As an option, a Save Data Pointers message will automatically be sent before the Disconnect message whenever the IDI bit is set prior to issuing this command.

The Command Phase register is updated during execution of the Send-Disconnect-Message command to indicate bus phase status. After a Save Data Pointers message is sent, the Command Phase will be set to 41H. After the Disconnect message transfer, this register will be updated to 42H, and after disconnection the Command Phase register will contain a 43H.

A Send-Disconnect-Message command may be terminated by ATN- asserted when HA = 1, or when a Disconnect or Reset command is issued. In addition, it may be aborted on a SCSI bus-phase boundary by issuing an Abort command.

The following table summarizes the possible values that the Command Phase Register can take during the Send-Disconnect-Message, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No operation occurred; typically, ATN- was found to be asserted.
41	The Save Data Pointer message was transferred.
42	The Disconnect message was transferred.
43	The bus free state occurred after the Disconnect message was transferred. The WD33C93A is now in the disconnected state.

29

8. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to GND	−0.5V to +7.0V
Operating temperature	0 to 70 degrees C
Storage temperature	−55 to +125 degrees C
Power dissipation	500 mW
Input Static Discharge Protection	1200 V pin to pin

DC OPERATING CHARACTERISTICS

Ta = 0 to 70 deg. C
VCC = +5V +/− .25V, GND = 0V

SYMBOL	CHARACTERISTICS	MIN	MAX	UNITS	CONDITIONS
IIL	INPUT LEAKAGE		10	uA	VIN = .4 TO VCC
IOL1	SCSI OUTPUT LEAKAGE (INACTIVE)		50	uA	VOUT = .5 TO VCC
IOL2	OUTPUT LEAKAGE (TRI-STATE)		10	uA	VOUT = .4 TO VCC
VIH	INPUT HIGH VOLTAGE	2.0		V	
VIL	INPUT LOW VOLTAGE		0.8	V	
VIHYS	SCHMITT TRIGGER INPUT HYSTERISIS (ALL SCSI PINS)	0.2		V	
VOH	OUTPUT HIGH VOLTAGE	2.4		V	IO = −400 uA
VOL1	SCSI OUTPUT LOW VOLTAGE		0.5	V	IO = 48.0 mA
VOL2	OUTPUT LOW VOLTAGE (ALL OTHERS)		0.4	V	IO = 4.0 mA
ICC	SUPPLY CURRENT		20	mA	Ta = +25 deg. C

9. TIMING CHARACTERISTICS

Timing characteristics are valid over the entire operating temperature (0 to 70 deg. C) and voltage (4.75 to 5.25 Volts) ranges, and are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts. All outputs are assumed to have a load capacitance of 50 picofarads.

Many of the SCSI bus timing parameters that follow are defined in terms of an internal clock cycle time that is determined by the input clock and the clock divisor selected in the OWN ID register. This cycle time is calculated as follows:

$$Tcyc = \frac{Ticlk * DIVISOR}{2}$$

Where:

Tcyc is the internal clock cycle time;

Ticlk is the period of the clock at the MCK input;

DIVISOR is the clock divisor selected in the OWN ID register.

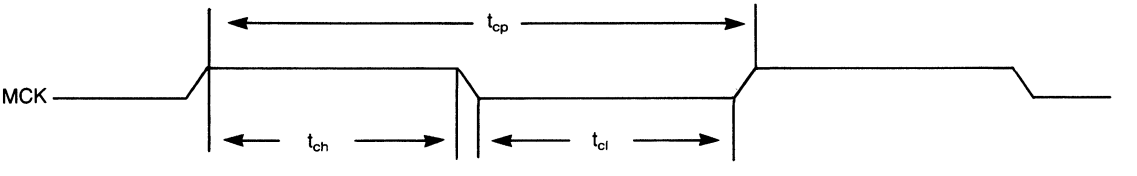
For example, with a 16MHz clock input to the WD33C93A, the clock divisor selected would be 4. Therefore, the value of Tcyc would be:

$$Tcyc = \frac{62.5\ nsec * 4}{2} = 125\ nsec$$

9.1 PROCESSOR/DMA INTERFACE

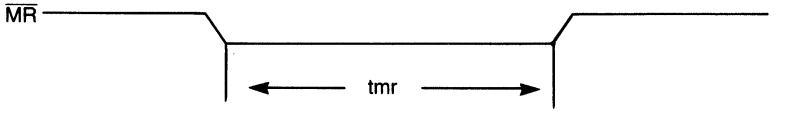
9.1.1 CLK

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{cp}	CLOCK PERIOD	62.5	125	ns
t_{ch}	CLOCK HIGH	28		ns
t_{cl}	CLOCK LOW	28		ns



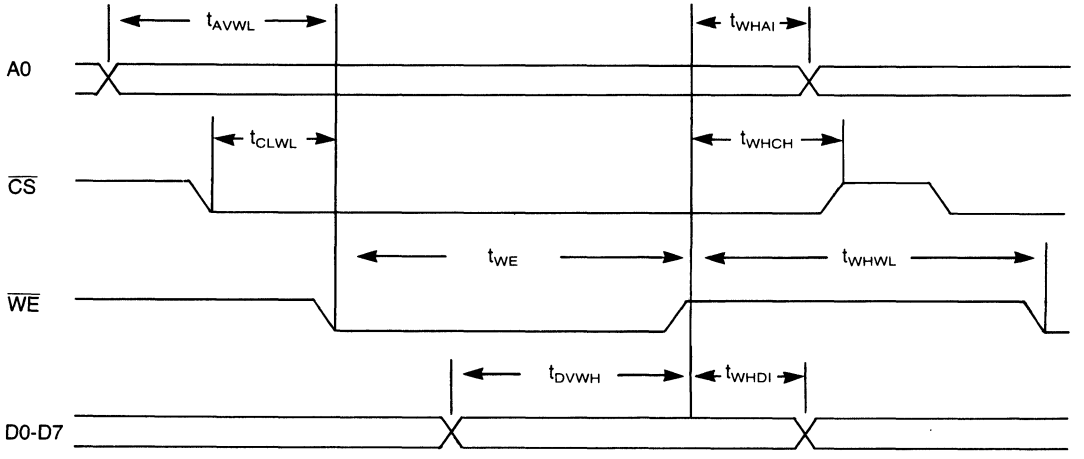
9.1.2 $\overline{MR}$

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tmr	$\overline{MR}$ PULSE WIDTH	1		us



9.1.3 PROCESSOR WRITE — INDIRECT ADDRESSING MODE

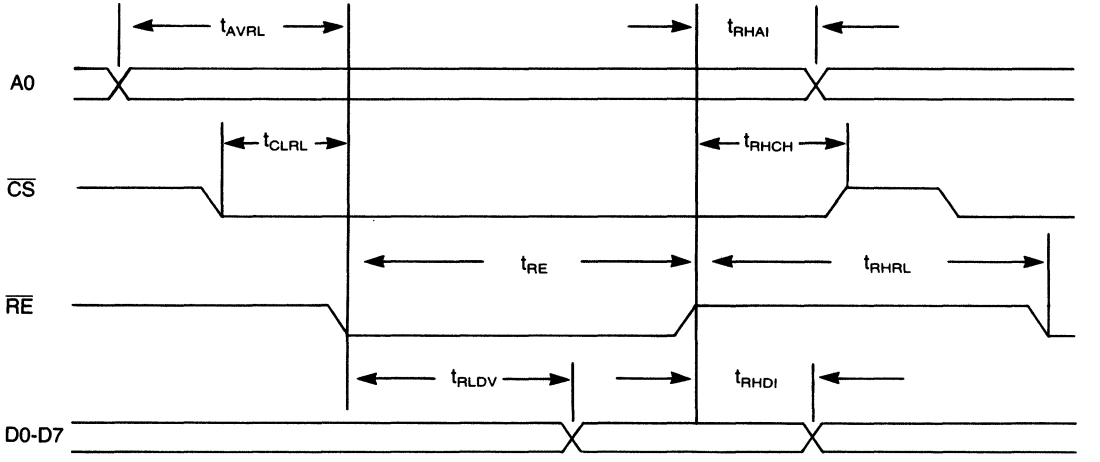
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{avwl}	ADDR VALID TO $\overline{WE}$ LOW	0		ns
t_{clwl}	$\overline{CS}$ LOW TO $\overline{WE}$ LOW	0		ns
t_{we}	$\overline{WE}$ PULSE WIDTH	120		ns
t_{dvwh}	DATA VALID TO WE HIGH	70		ns
t_{whai}	$\overline{WE}$ HIGH TO ADDR. INVALID	0		ns
t_{whch}	$\overline{WE}$HIGH TO $\overline{CS}$ HIGH	0		ns
t_{whdi}	$\overline{WE}$ HIGH TO DATA INVALID	0		ns
t_{whwl}	$\overline{WE}$ HIGH TO $\overline{WE}$ OR $\overline{RE}$ LOW	100		ns



29

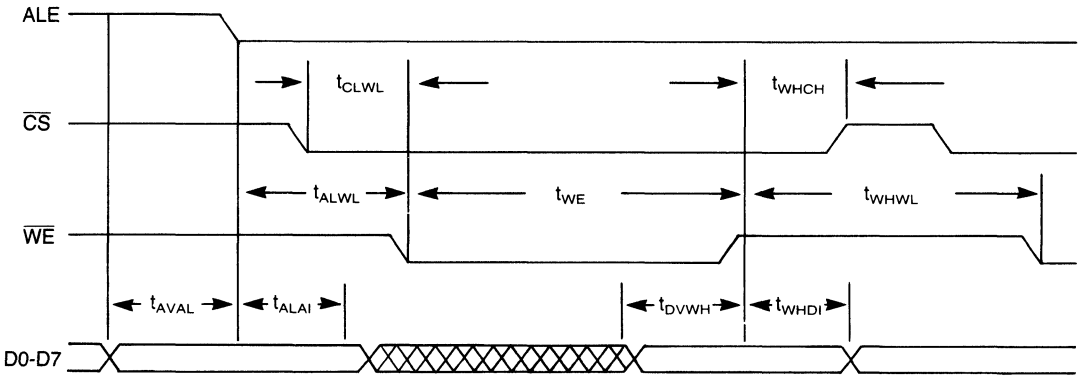
9.1.4 PROCESSOR READ — INDIRECT ADDRESSING MODE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{avrl}	ADDR VALID TO $\overline{RE}$ LOW	0		ns
t_{clrl}	$\overline{CS}$ LOW TO $\overline{RE}$ LOW	0		ns
t_{re}	$\overline{RE}$ LOW TO DATA VALID	180	10000	ns
t_{rldv}	$\overline{RE}$ PULSE WIDTH LOW TO DATA VALID	180	180	ns
t_{rhch}	$\overline{RE}$ HIGH TO $\overline{CS}$ HIGH	0		ns
t_{rhdi}	$\overline{RE}$ HIGH TO DATA INVALID	10	40	ns
t_{rhrl}	$\overline{RE}$ HIGH TO $\overline{RE}$ OR $\overline{WE}$ LOW	100		ns
t_{rhai}	$\overline{RE}$ HIGH TO A0 INVALID	0		ns



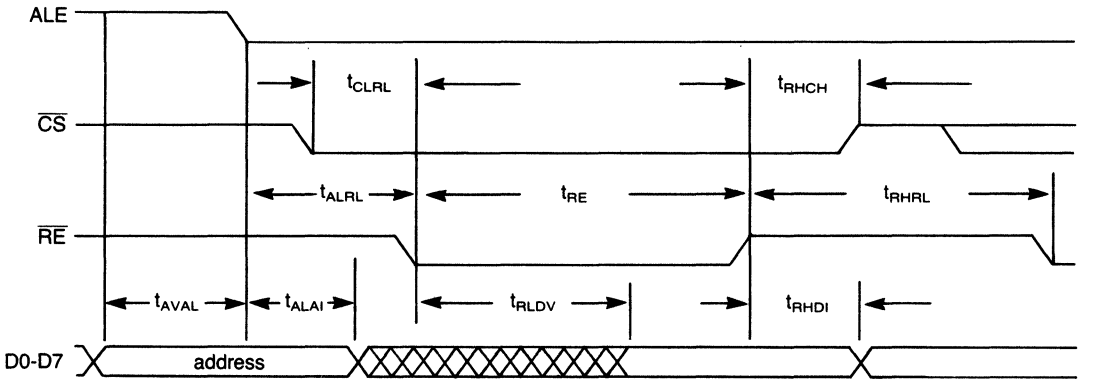
9.1.5 PROCESSOR WRITE — DIRECT ADDRESSING MODE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{aval}	ADDR VALID TO $\overline{ALE}$ LOW	40		ns
t_{alai}	ALE LOW TO ADDR INVALID	0		ns
t_{alwl}	ALE LOW TO $\overline{WE}$ LOW	90		ns
t_{clwl}	$\overline{CS}$LOW TO $\overline{WE}$ LOW	0		ns
t_{we}	$\overline{WE}$ PULSE TO $\overline{WE}$ HIGH	120		ns
t_{dvwh}	DATA VALID TO $\overline{WE}$ HIGH	70		ns
t_{whch}	$\overline{WE}$ HIGH TO $\overline{CS}$ HIGH	0		ns
t_{whdi}	$\overline{WE}$ HIGH TO DATA INVALID	0		ns
t_{whwl}	$\overline{WE}$ HIGH TO $\overline{WE}$ OR $\overline{RE}$ LOW	100		ns



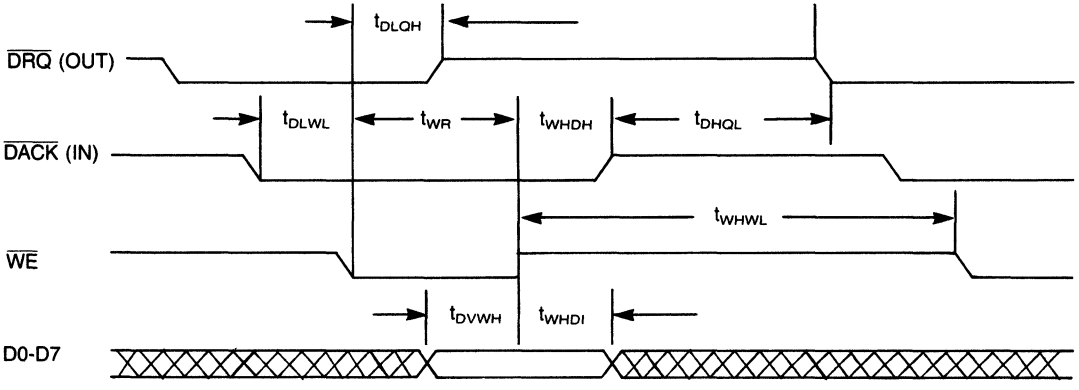
9.1.6 PROCESSOR READ – DIRECT ADDRESSING MODE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{aval}	ADDR VALID TO $\overline{ALE}$ LOW	40		ns
t_{alai}	ALE LOW TO ADDR INVALID	0		ns
t_{alrl}	ALE LOW TO $\overline{RE}$ LOW	30		ns
t_{clrl}	$\overline{CS}$ LOW TO $\overline{RE}$ LOW	0		ns
t_{re}	$\overline{RE}$ PULSE WIDTH	180	10000 ns	
t_{rldv}	$\overline{RE}$ LOW TO DATA VALID		180	ns
t_{rhch}	$\overline{RE}$ HIGH TO $\overline{CS}$ HIGH	0		ns
t_{rhdi}	$\overline{RE}$ HIGH TO DATA INVALID	10	40	ns
t_{rhrl}	$\overline{RE}$ HIGH TO $\overline{RE}$ OR $\overline{WE}$ LOW	100		ns



9.1.7 DMA WRITE

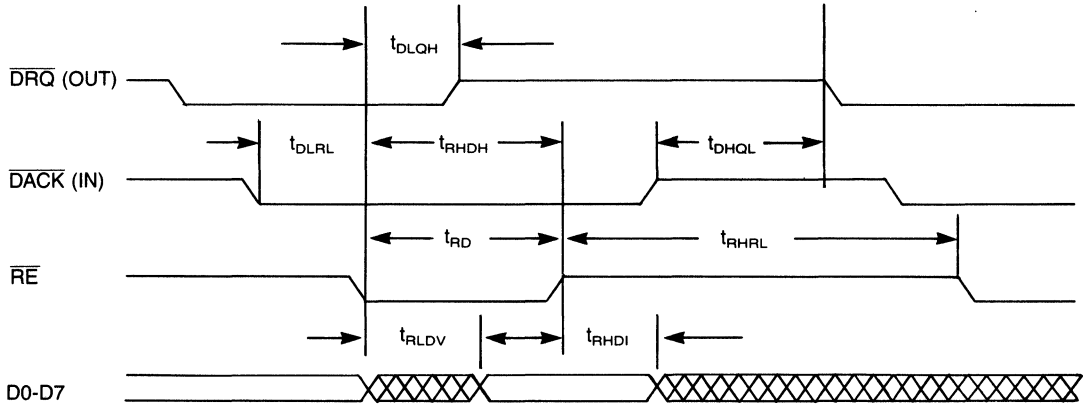
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dlwl}	$\overline{DACK}$ LOW TO $\overline{WE}$ LOW	0		ns
t_{dlqh}	$\overline{DACK}$, $\overline{WR}$ LOW TO $\overline{DRQ}$ HIGH	40	90	ns
t_{wr}	$\overline{WE}$ PULSE WIDTH	50		ns
t_{whwl}	$\overline{WE}$ HIGH TO $\overline{WE}$ LOW	100		ns
t_{dvwh}	DATA VALID TO $\overline{WE}$ HIGH	25		ns
t_{whdh}	$\overline{WE}$ HIGH TO DACK HIGH	0		ns
t_{whdi}	$\overline{WE}$ HIGH TO DATA INVALID	0		ns
t_{dhql}	$\overline{DACK}$ HIGH TO $\overline{DRQ}$ LOW	30		ns



NOTE: External load on $\overline{DRQ}$ & $\overline{DACK}$ is assumed to be 1KΩ.

9.1.8 DMA READ

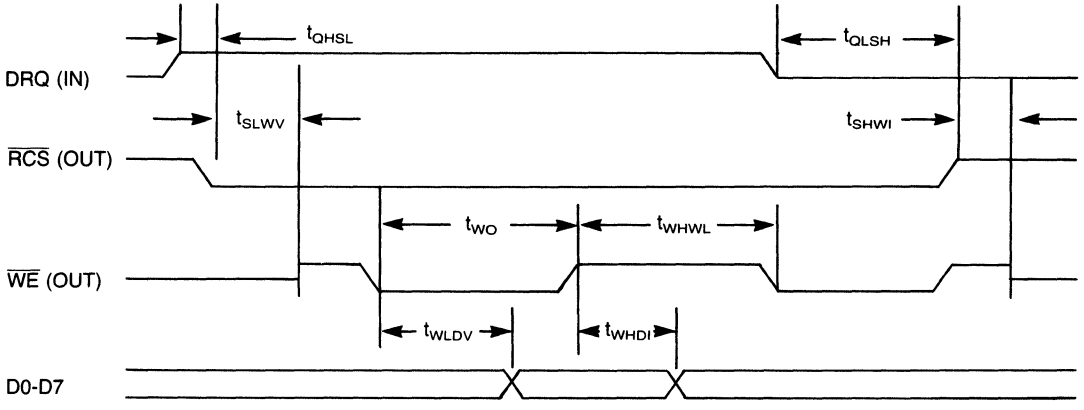
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dlrl}	$\overline{DACK}$ LOW TO $\overline{RE}$ LOW	0		ns
t_{dlqh}	$\overline{DACK}$, $\overline{RE}$ LOW TO $\overline{DRQ}$ HIGH	40	90	ns
t_{rd}	$\overline{RE}$ PULSE WIDTH	80		ns
t_{rhrl}	$\overline{RE}$ HIGH TO $\overline{RE}$ LOW	100		ns
t_{rldv}	$\overline{RE}$ LOW TO DATA VALID		70	ns
t_{rhdh}	$\overline{RE}$ HIGH TO $\overline{DACK}$ HIGH	0		ns
t_{rhdi}	$\overline{RE}$ HIGH TO DATA INVALID	5	40	ns
t_{rhdl}	$\overline{DRQ}$ HIGH TO $\overline{DRQ}$ LOW	100		ns
t_{dhql}	$\overline{DACK}$ HIGH TO $\overline{DRQ}$ LOW	30		ns



NOTE: External load on $\overline{DRQ}$ & DACK is assumed to be 1KΩ.

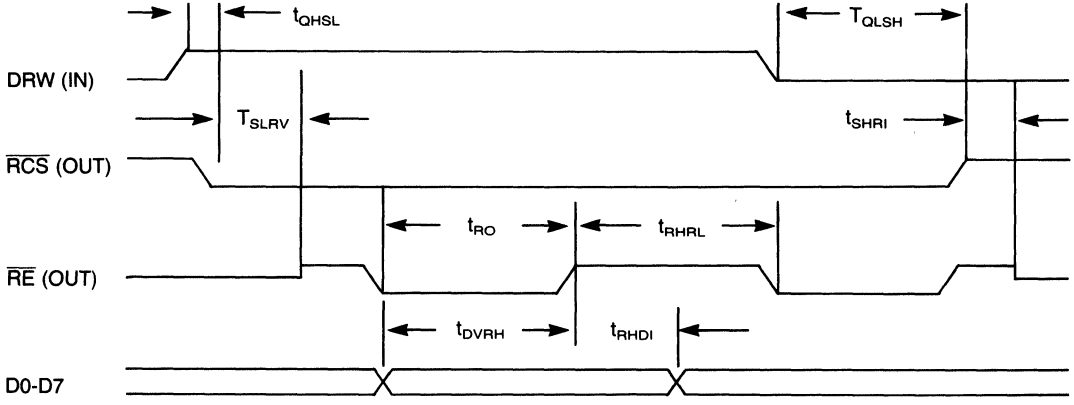
9.1.9 WD-BUS BUFFER WRITE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{qhsl}	DRQ HIGH TO $\overline{RCS}$ LOW	0		ns
t_{slwv}	$\overline{RCS}$ LOW TO $\overline{WE}$ VALID	0	20	ns
t_{wo}	$\overline{WE}$ PULSE WIDTH	Tcyc-20		ns
t_{wldv}	$\overline{WE}$ LOW TO DATA VALID		50	ns
t_{whdi}	$\overline{WE}$ HIGH TO $\overline{WE}$ LOW	30		ns
t_{whwl}	$\overline{WE}$ HIGH TO $\overline{WE}$ LOW	Tcyc-20		ns
t_{qlsh}	DRQ LOW TO $\overline{RCS}$ HIGH	8*Tcyc	10*Tcyc	ns
t_{shwi}	$\overline{RCS}$ HIGH TO $\overline{WE}$ INVALID	0	100	ns



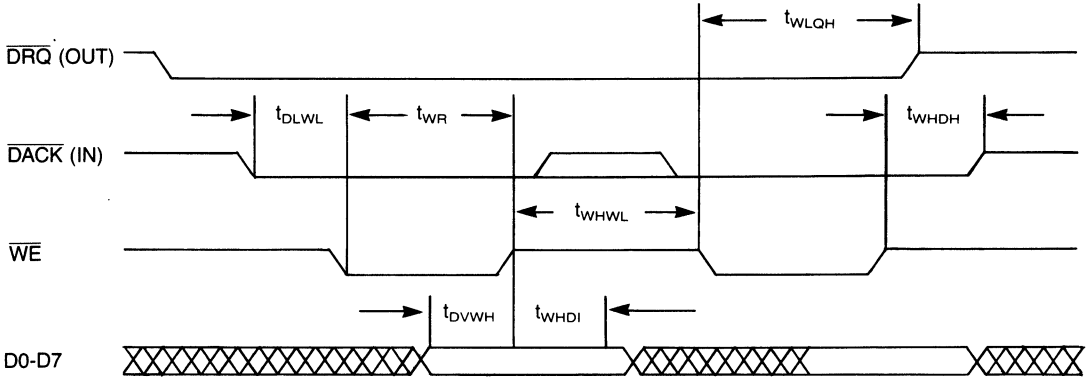
9.1.10 WD-BUS BUFFER READ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{qhsl}	DRQ HIGH TO $\overline{RCS}$ LOW	0		ns
t_{slrv}	$\overline{RCS}$ LOW TO $\overline{RE}$ VALID	0	20	ns
t_{ro}	$\overline{RE}$ PULSE WIDTH	Tcyc-20		ns
t_{dvrh}	DATA VALID TO $\overline{RE}$ HIGH	10		ns
t_{rhdi}	$\overline{RE}$ HIGH TO DATA INVALID	10		ns
t_{rhrl}	$\overline{RE}$ HIGH TO $\overline{RE}$ LOW	TCYC-20		ns
t_{qlsh}	DRQ LOW TO $\overline{RCS}$ HIGH	8*Tcyc	10*Tcyc	ns
t_{shri}	$\overline{RCS}$ HIGH TO $\overline{RE}$ INVALID	0	100	ns



9.1.11 BURST DMA WRITE

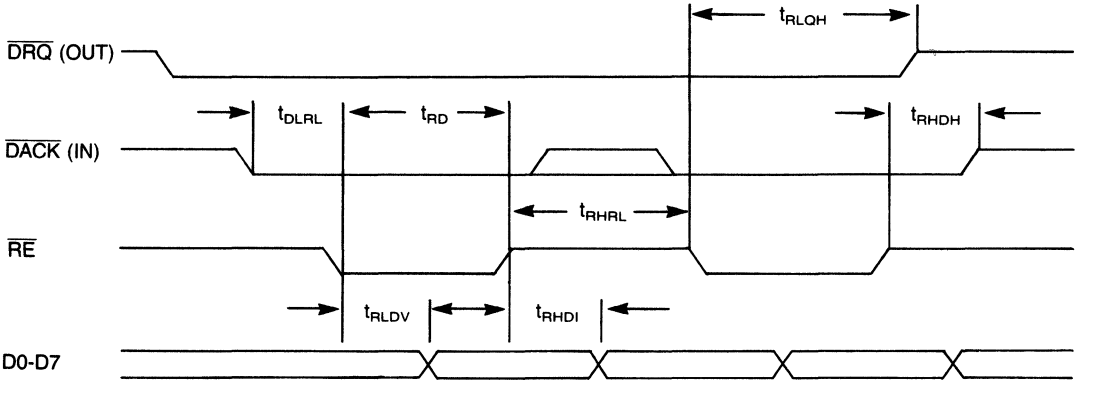
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dlwl}	$\overline{DACK}$ LOW TO $\overline{WE}$ LOW	0		ns
t_{wlqh}	$\overline{WE}$ LOW TO $\overline{DRQ}$ HIGH		75	ns
t_{wr}	$\overline{WE}$ PULSE WIDTH	50		ns
t_{whwl}	$\overline{WE}$ HIGH TO $\overline{WE}$ LOW	80		ns
t_{dvwh}	$\overline{DATA\ VALID\ TO}$ WE HIGH	25		ns
t_{whdh}	$\overline{WE}$ HIGH TO $\overline{DACK}$ HIGH	0		ns
t_{whdi}	$\overline{WE}$ HIGH TO DATA INVALID	0		ns



29

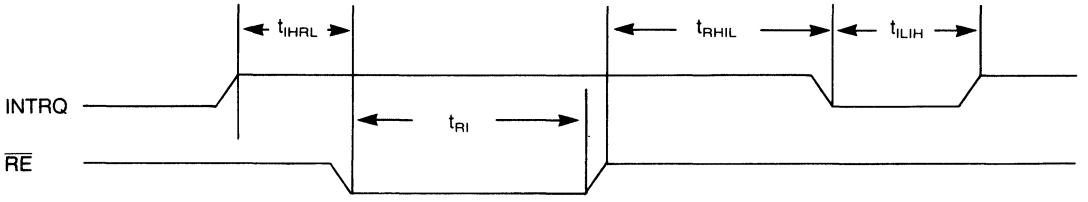
9.1.12 BURST DMA READ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dlrl}	$\overline{DACK}$ LOW TO $\overline{RE}$ LOW	0		ns
t_{rlqh}	$\overline{RE}$ LOW TO $\overline{DRQ}$ HIGH		75	ns
t_{rd}	$\overline{RE}$ PULSE WIDTH	80		ns
t_{rhrl}	$\overline{RE}$ HIGH TO $\overline{RE}$ LOW	80		ns
t_{rldv}	$\overline{RE}$ LOW TO DATA VALID		50	ns
t_{rhdh}	$\overline{RE}$ HIGH TO $\overline{DACK}$ HIGH	0		ns
t_{rhdi}	$\overline{RE}$ HIGH TO DATA INVALID	5	40	ns



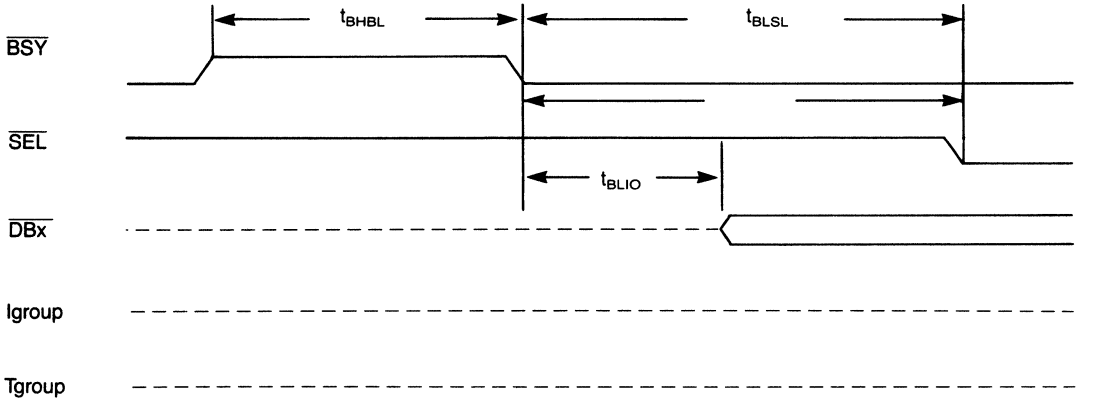
9.1.13 INTRQ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{ihrl}	INTRQ HIGH TO $\overline{RE}$ LOW	0		ns
t_{ri}	$\overline{RE}$ PULSE WIDTH	180		ns
t_{rhil}	$\overline{RE}$ HIGH TO INTRQ LOW	0	100	ns
t_{ilih}	INTRQ LOW TO INTRQ HIGH	100		ns



9.2 SCSI INTERFACE
9.2.1 ARBITRATION

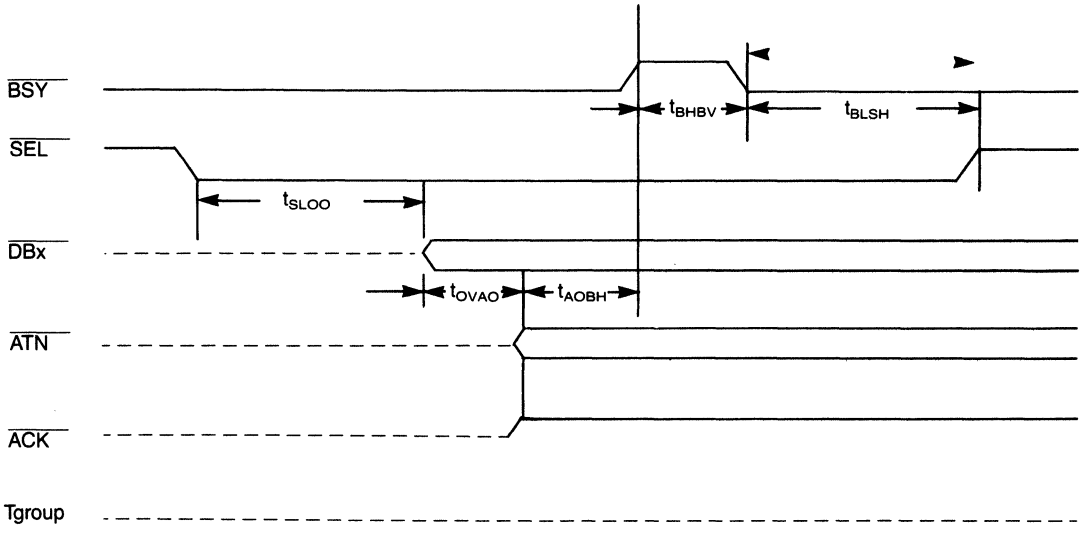
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{bhbl}	$\overline{BSY}$, $\overline{SEL}$ IN HIGH TO $\overline{BSY}$ OUT LOW	12*Tcyc	16*Tcyc	ns
t_{blio}	$\overline{BSY}$ OUT LOW TO BUS ID OUT	−50	50	ns
t_{blsl}	$\overline{BSY}$ OUT LOW TO $\overline{SEL}$ OUT LOW	2.2		us



NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$
Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$

9.2.2 SELECTING A TARGET (AS AN INITIATOR)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{sloo}	$\overline{SEL}$ OUT LOW TO "OR-ED" ID OUT	1.2		us
t_{ovao}	"OR-ED" ID OUT VALID TO $\overline{ACK}$, $\overline{ATN}$ OUT	100		ns
t_{aobh}	$\overline{ACK}$, $\overline{ATN}$ OUT VALID TO $\overline{BSY}$ OUT HIGH	100		ns
t_{bhbv}	$\overline{BSY}$ OUT HIGH TO $\overline{BSY}$ IN LOW VALID	400		ns
t_{blsh}	$\overline{BSY}$ IN LOW TO $\overline{SEL}$ OUT HIGH	100		ns

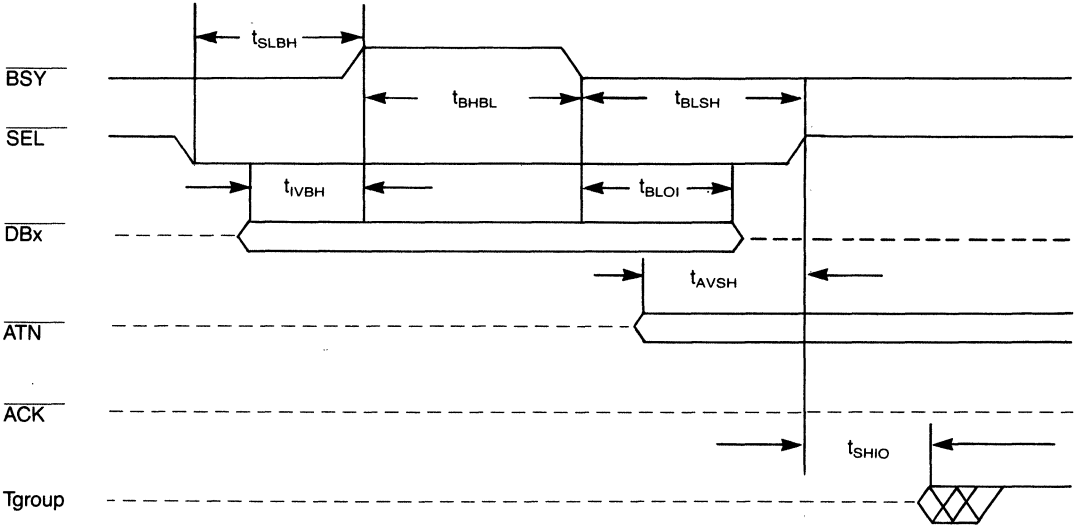


NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$

29

9.2.3 RESPONSE TO SELECTION (AS A TARGET)

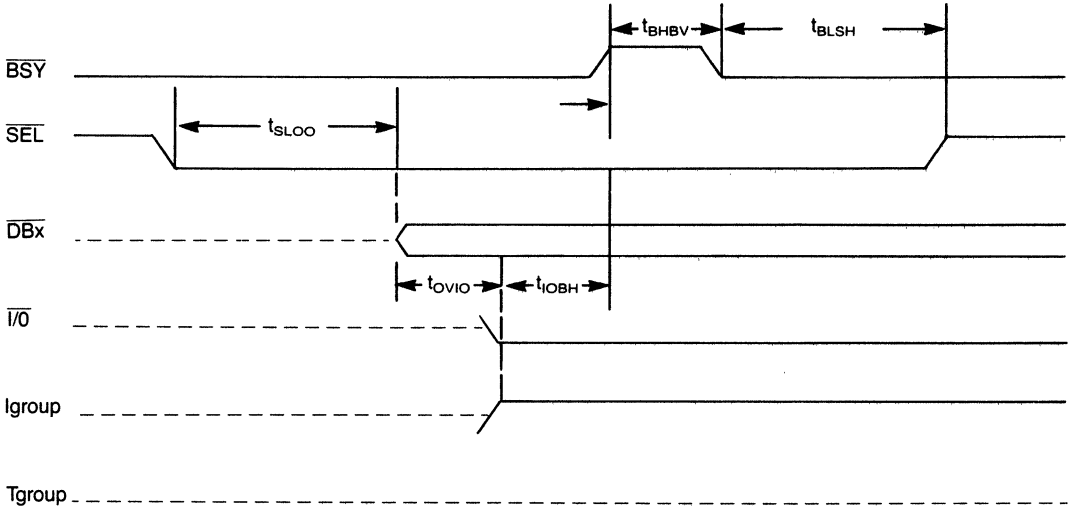
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{slbh}	$\overline{SEL}$ IN LOW TO $\overline{BSY}$ IN HIGH	0		ns
t_{ivbh}	"OR-ED" ID VALID IN TO $\overline{BSY}$ IN HIGH	0		ns
t_{bhbl}	$\overline{SEL}$ LOW, ID VALID, $\overline{BSY}$ HIGH TO $\overline{BSY}$ LOW	0.4	200	us
t_{bloi}	$\overline{BSY}$ OUT LOW TO "OR-ED" ID INVALID IN	0		ns
t_{blsh}	$\overline{BSY}$ OUT LOW TO $\overline{SEL}$ IN HIGH	0		ns
t_{avsh}	$\overline{ATN}$ VALID IN TO $\overline{SEL}$ IN HIGH	0		ns
t_{shio}	$\overline{SEL}$ IN HIGH TO Tgroup OUT	100		ns



NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$

9.2.4 RESELECTING AN INITIATOR (AS A TARGET)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{sloo}	$\overline{SEL}$ OUT LOW TO "OR-ED" ID OUT	1.2		us
t_{ovio}	"OR-ED" ID VALID TO I/O and Tgroup OUT VALID	100		ns
t_{iobh}	I/O and Tgroup OUT VALID TO $\overline{BSY}$ OUT HIGH	100		us
t_{bhbv}	$\overline{BSY}$ OUT HIGH TO $\overline{BSY}$ IN LOW VALID	400		ns
t_{blsh}	$\overline{BSY}$ IN LOW TO $\overline{SEL}$ OUT HIGH	100		ns

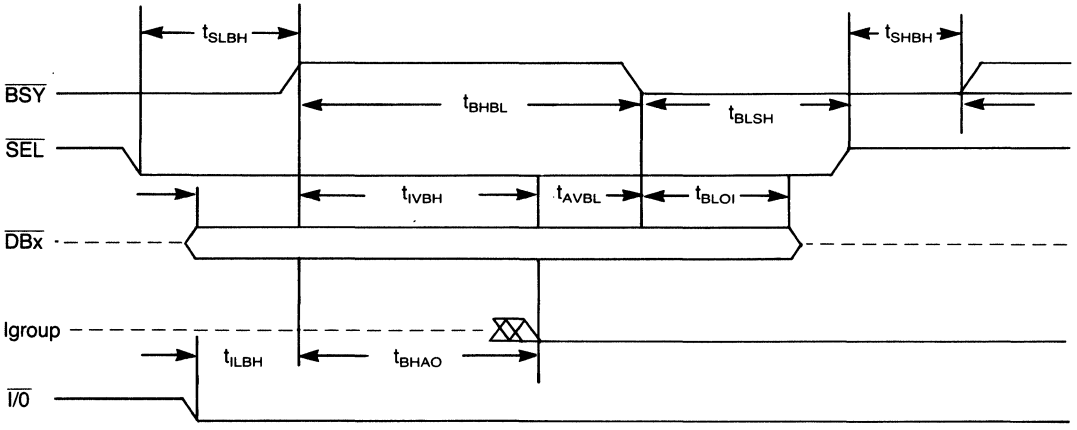


NOTE: Tgroup = signals driven by a Target = $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$
Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$

29

9.2.5 RESPONSE TO RESELECTION (AS AN INITIATOR)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{slbh}	$\overline{SEL}$ IN LOW TO $\overline{BSY}$ IN HIGH	0		ns
t_{ivbh}	"OR-ED" ID VALID IN TO $\overline{BSY}$ IN HIGH	0		ns
t_{ilbh}	$\overline{I/O}$ IN LOW TO $\overline{BSY}$ IN HIGH	0		ns
t_{bhao}	$\overline{SEL}$ LOW, ID VALID, $\overline{BSY}$ HIGH TO Igroup OUT	100		ns
t_{avbl}	Igroup VALID OUT TO $\overline{BSY}$ OUT LOW	100		ns
t_{bhbl}	$\overline{BSY}$ IN HIGH TO $\overline{BSY}$ OUT LOW	0.4	200	us
t_{bloi}	$\overline{BSY}$ OUT LOW TO "OR-ED" INVALID IN	0		ns
t_{blsh}	$\overline{BSY}$ OUT LOW TO $\overline{SEL}$ IN HIGH	0		ns
t_{shbh}	$\overline{SEL}$ IN HIGH TO $\overline{BSY}$ OUT HIGH	0		ns

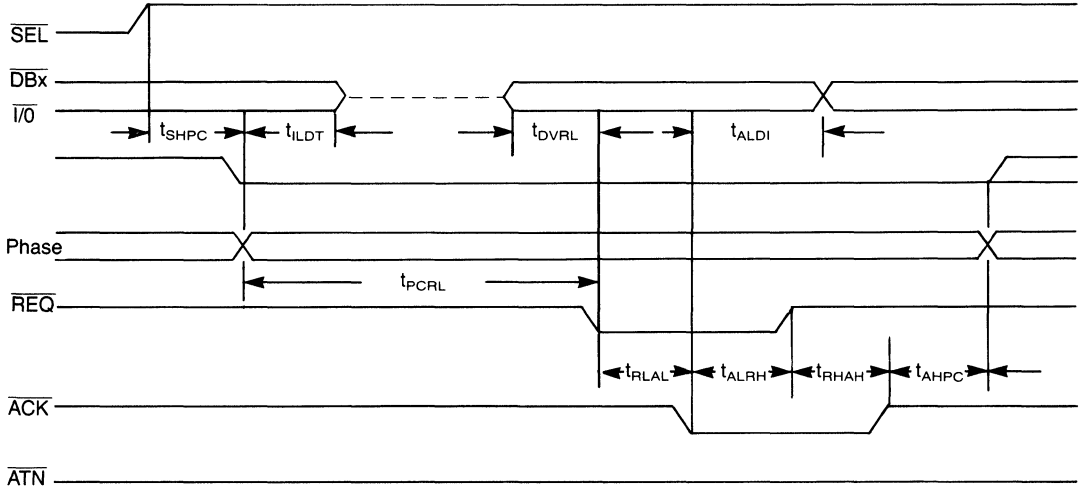


NOTE: Tgroup = signals driven by a Target = $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$
Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$

*** $\overline{BSY}$ will still be driven low by the reselecting target.

9.2.6 RECEIVE ASYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS AN INITIATOR)

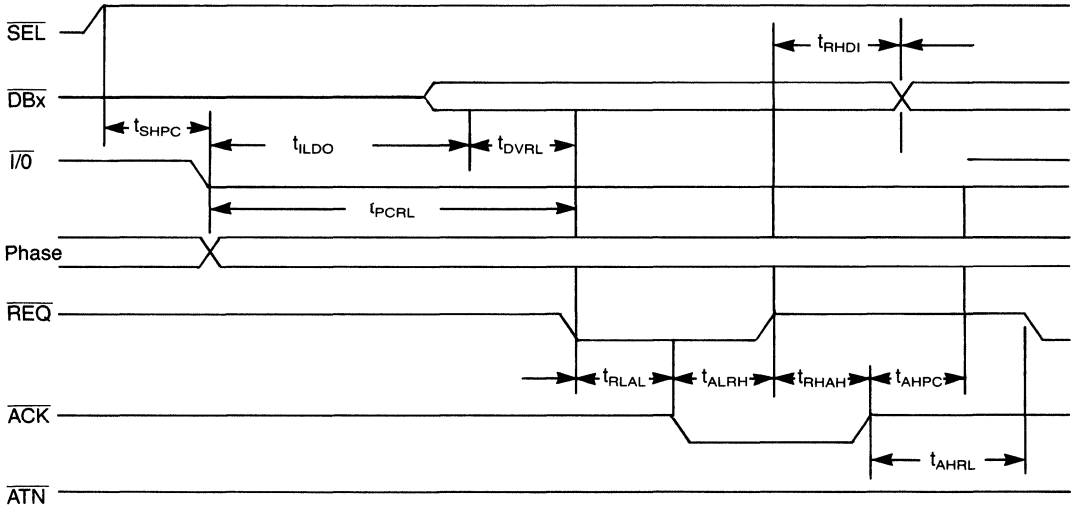
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{shpc}	$\overline{SEL}$ IN HIGH TO PHASE CHANGE IN	0		ns
t_{ildt}	$\overline{I/O}$ IN LOW TO DATA BUS TRISTATE	0	125	ns
t_{pcrl}	PHASE CHANGE IN TO $\overline{REQ}$ IN LOW	400		ns
t_{dvrl}	DATA VALID IN TO $\overline{REQ}$ IN LOW	0		ns
t_{rlal}	$\overline{REQ}$ IN LOW TO $\overline{ACK}$ OUT LOW	0	175	ns
t_{aldi}	$\overline{ACK}$ OUT LOW TO DATA INVALID IN	0		ns
t_{alrh}	$\overline{ACK}$ OUT LOW TO $\overline{REQ}$ IN HIGH	0		ns
t_{rhah}	$\overline{REQ}$ IN HIGH TO $\overline{ACK}$ OUT HIGH	0	175	ns
t_{ahpc}	$\overline{ACK}$ OUT HIGH TO PHASE CHANGE IN	0		ns



NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

9.2.7 SEND ASYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS A TARGET)

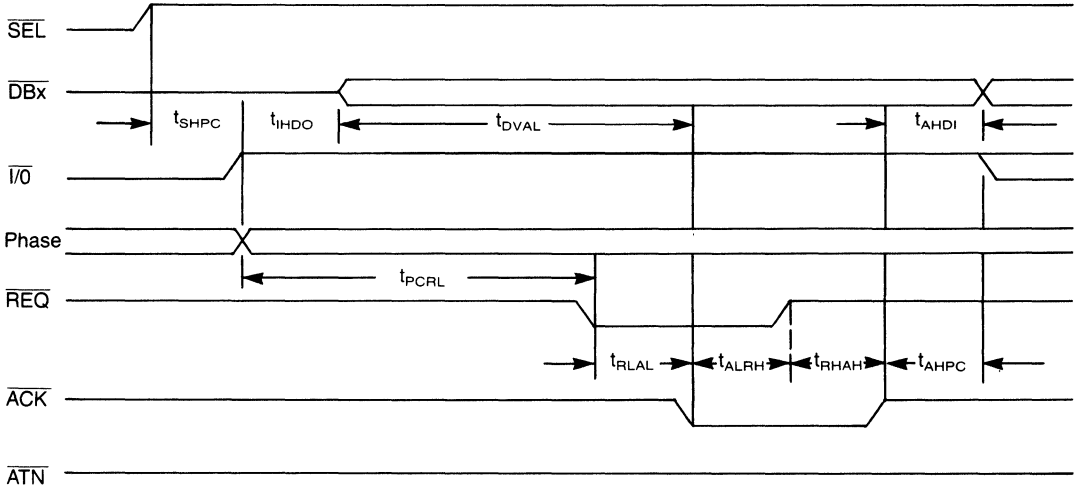
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{shpc}	$\overline{SEL}$ IN HIGH TO PHASE CHANGE OUT	100		ns
t_{ildo}	$\overline{I/O}$ OUT LOW TO DATA OUT	800		ns
t_{dvrl}	DATA OUT VALID TO $\overline{REQ}$ OUT LOW	55		ns
t_{pcrl}	PHASE CHANGE OUT TO $\overline{REQ}$ OUT LOW	500		ns
t_{rlal}	$\overline{REQ}$ OUT LOW TO $\overline{ACK}$ IN LOW	0		ns
t_{alrh}	$\overline{ACK}$ IN LOW TO $\overline{REQ}$ OUT HIGH	0	175	ns
t_{rhdi}	$\overline{REQ}$ OUT HIGH TO DATA OUT INVALID	0		ns
t_{rhah}	$\overline{REQ}$ OUT HIGH TO $\overline{ACK}$ IN HIGH	0		ns
t_{ahpc}	$\overline{ACK}$ IN HIGH TO PHASE CHANGE OUT	100		ns
t_{ahrl}	$\overline{ACK}$ IN HIGH TO $\overline{REQ}$ OUT LOW	0	175	ns



NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

9.2.8 SEND ASYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS AN INITIATOR)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{shpc}	$\overline{SEL}$ IN HIGH TO PHASE CHANGE IN	0		ns
t_{ihdo}	$\overline{I/O}$ IN HIGH TO DATA OUT	0		ns
t_{pcrl}	PHASE CHANGE IN TO $\overline{REQ}$ IN LOW	400		ns
t_{rlal}	$\overline{REQ}$ IN LOW TO $\overline{ACK}$ OUT LOW	0	175	ns
t_{dval}	DATA OUT VALID TO $\overline{ACK}$ OUT LOW	55		ns
t_{alrh}	$\overline{ACK}$ OUT LOW TO $\overline{REQ}$ IN HIGH	0		ns
t_{rhah}	$\overline{REQ}$ IN HIGH TO $\overline{ACK}$ OUT HIGH	0	175	ns
t_{ahdi}	$\overline{ACK}$ OUT HIGH TO DATA OUT INVALID	0		ns
t_{ahpc}	$\overline{ACK}$ OUT HIGH TO PHASE CHANGE IN	0		ns

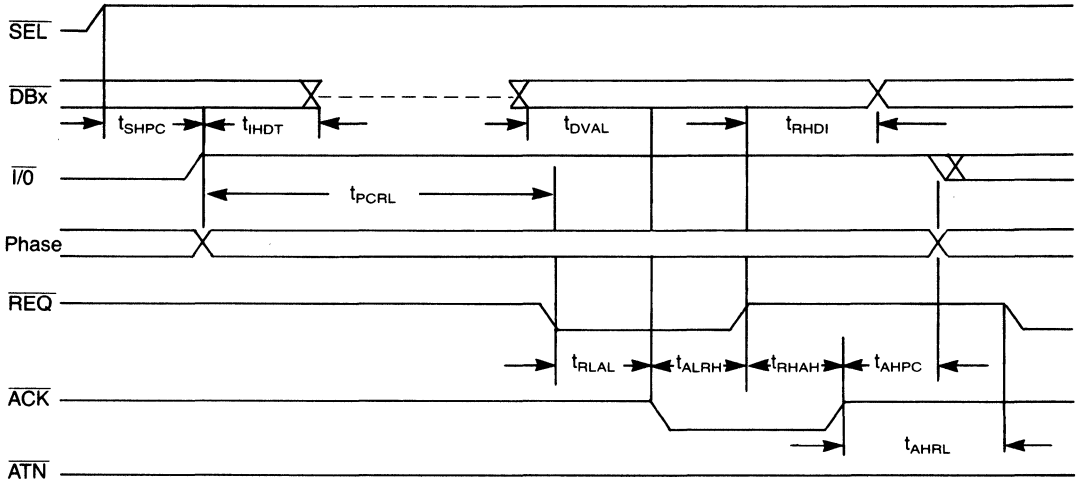


NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

29

9.2.9 RECEIVE ASYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS AN TARGET)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{shpc}	$\overline{SEL}$ IN HIGH TO PHASE CHANGE OUT	100		ns
t_{ihdt}	$\overline{I/O}$ OUT HIGH TO DATA BUS TRISTATE		0	ns
t_{pcrl}	PHASE CHANGE TO $\overline{REQ}$ OUT LOW	500		ns
t_{rlal}	$\overline{REQ}$ OUT LOW TO $\overline{ACK}$ IN LOW	0		ns
t_{dval}	DATA IN VALID TO $\overline{ACK}$ IN LOW	5		ns
t_{alrh}	$\overline{ACK}$ IN LOW TO $\overline{REQ}$ OUT HIGH	0	175	ns
t_{rhdi}	$\overline{REQ}$ OUT HIGH TO DATA IN INVALID	0		ns
t_{rhah}	$\overline{REQ}$ OUT HIGH TO $\overline{ACK}$ IN HIGH	0		ns
t_{ahpc}	$\overline{ACK}$ IN HIGH TO PHASE CHANGE OUT	0		ns
t_{ahrl}	$\overline{ACK}$ IN HIGH TO $\overline{REQ}$ OUT LOW	0	175	ns

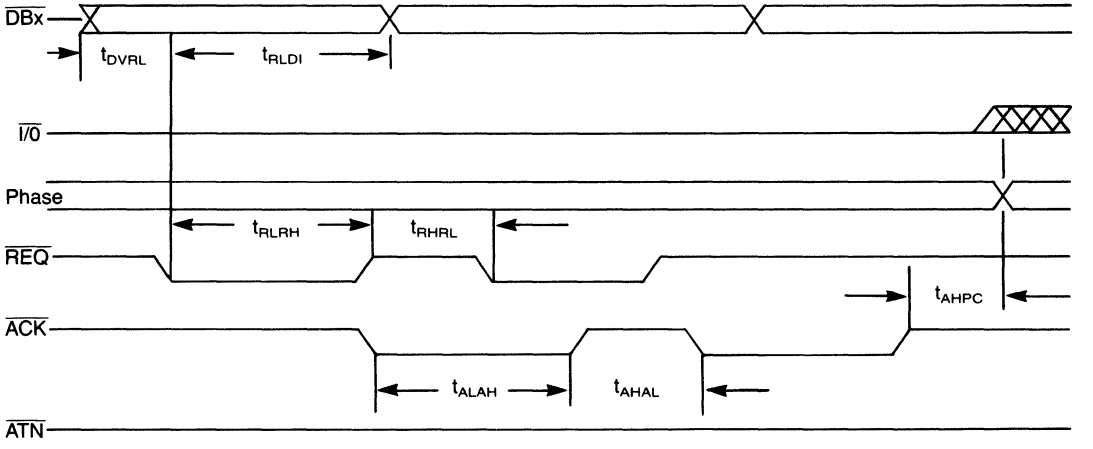


NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

9.2.10 RECEIVE SYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS AN INITIATOR)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dvrl}	DATA VALID IN TO $\overline{REQ}$ IN LOW	0		ns
t_{rldi}	$\overline{REQ}$ IN LOW TO DATA INVALID	45		ns
t_{rlrh}	$\overline{REQ}$ IN LOW TO $\overline{REQ}$ IN HIGH	50		ns
t_{rhrl}	$\overline{REQ}$ IN HIGH TO REQ IN LOW	50		ns
t_{alah}	$\overline{ACK}$ OUT LOW TO $\overline{ACK}$ OUT HIGH	Tcyc-10		ns
t_{ahal}	$\overline{ACK}$ OUT HIGH TO $\overline{ACK}$ OUT LOW	Tcyc-25		ns
t_{ahpc}	$\overline{ACK}$ OUT HIGH TO PHASE CHANGE	0		ns

PARAMETERS tshpc, tildt, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 9.2.6.



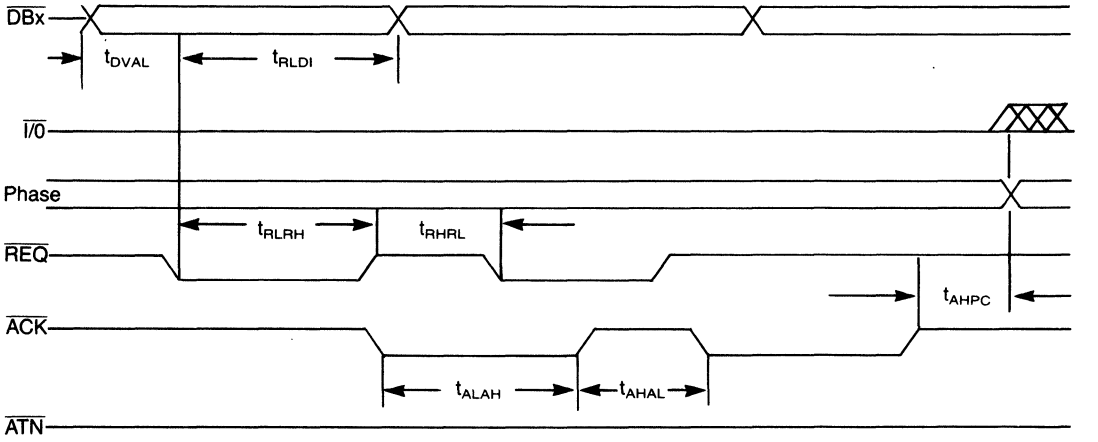
NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

29

9.2.11 SEND SYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS A TARGET)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dvrl}	DATA VALID OUT TO $\overline{REQ}$ OUT LOW	55		ns
t_{rldi}	$\overline{REQ}$ OUT LOW TO DATA INVALID OUT	100		ns
t_{rlrh}	$\overline{REQ}$ OUT LOW TO $\overline{REQ}$ OUT HIGH	Tcyc-10		ns
t_{rhrl}	$\overline{REQ}$ OUT HIGH TO $\overline{REQ}$ OUT LOW	Tcyc-25		ns
t_{alah}	$\overline{ACK}$ IN LOW TO $\overline{ACK}$ IN HIGH	50		ns
t_{ahal}	$\overline{ACK}$ IN HIGH TO $\overline{ACK}$ IN LOW	50		ns
t_{ahpc}	$\overline{ACK}$ IN HIGH TO PHASE CHANGE OUT	0		ns

PARAMETERS tshpc, tildt, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN SUBSECTION 9.2.7.

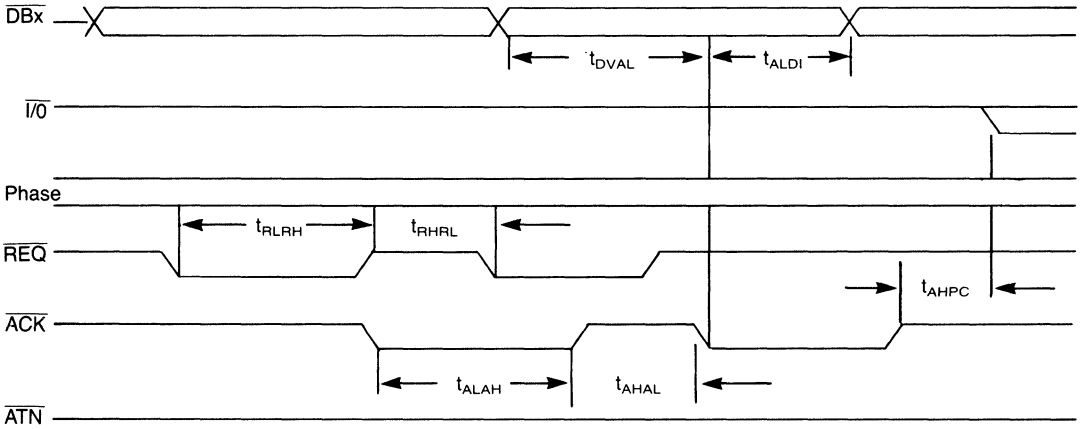


NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

9.2.12 SEND SYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS AN INITIATOR)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dval}	DATA VALID OUT TO $\overline{ACK}$ OUT LOW	55		ns
t_{aldi}	$\overline{ACK}$ OUT LOW TO DATA INVALID OUT	100		ns
t_{rlrh}	$\overline{REQ}$ IN LOW TO $\overline{REQ}$ IN HIGH	50		ns
t_{rhrl}	$\overline{REQ}$ IN HIGH TO $\overline{REQ}$ IN LOW	50		ns
t_{alah}	$\overline{ACK}$ OUT LOW TO $\overline{ACK}$ OUT HIGH	Tcyc-10		ns
t_{ahal}	$\overline{ACK}$ OUT HIGH TO $\overline{ACK}$ OUT LOW	Tcyc-25		ns
t_{ahpc}	$\overline{ACK}$ OUT HIGH TO PHASE CHANGE	0		ns

PARAMETERS tshpc, tildt, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 9.2.8.



NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

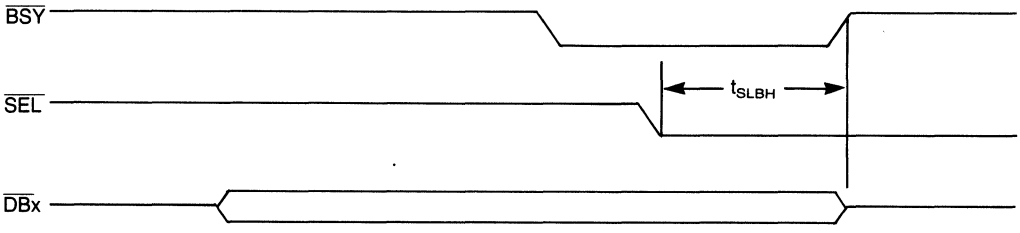
9.2.13 RECEIVE SYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS A TARGET)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{dval}	DATA VALID IN TO $\overline{ACK}$ IN LOW	0		ns
t_{aldi}	$\overline{ACK}$ IN LOW TO DATA INVALID	45		ns
t_{rlrh}	$\overline{REQ}$ OUT LOW TO $\overline{REQ}$ OUT HIGH	Tcyc-10		ns
t_{rhrl}	$\overline{REQ}$ OUT HIGH TO $\overline{REQ}$ OUT LOW	Tcyc-25		ns
t_{alah}	$\overline{ACK}$ IN LOW TO $\overline{ACK}$ IN HIGH	50		ns
t_{ahal}	$\overline{ACK}$ IN HIGH TO $\overline{ACK}$ IN LOW	50		ns
t_{ahpc}	$\overline{ACK}$ IN HIGH TO PHASE CHANGE OUT	0		ns

PARAMETERS t_{shpc}, t_{ildt}, and t_{pcrl} ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN SUBSECTION 9.2.9.

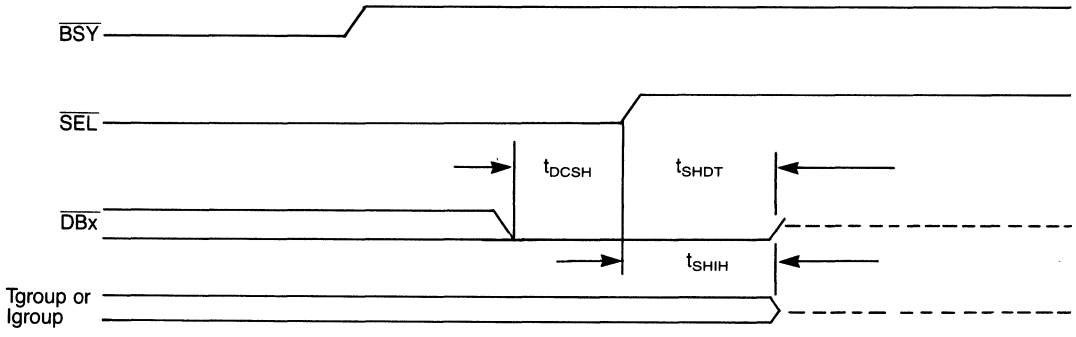
9.2.14 ARBITRATION TO BUS FREE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{slbh}	$\overline{SEL}$ IN LOW TO $\overline{BSY}$ HIGH, DATA TRI-STATE		8*Tcyc +75	ns



9.2.15 SELECTION (AS AN INITIATOR) OR RESELECTION (AS A TARGET) TO BUS FREE (SELECTION TIMEOUT)

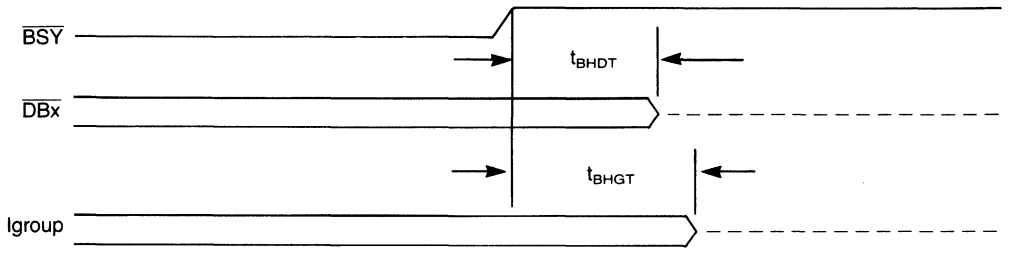
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{tadc}	TIMEOUT OR ABORT TO DATA BUS CLEARED	0		ns
t_{dcsh}	DATA BUS CLEARED TO $\overline{SEL}$ OUT HIGH	200		us
t_{shdt}	$\overline{SEL}$ OUT HIGH TO DATA BUS TRISTATE		800	ns
t_{shih}	$\overline{SEL}$ OUT HIGH TO cntl TRISTATE		800	ns



NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$
Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$

9.2.16 CONNECTED-AS-AN-INITIATOR TO BUS FREE

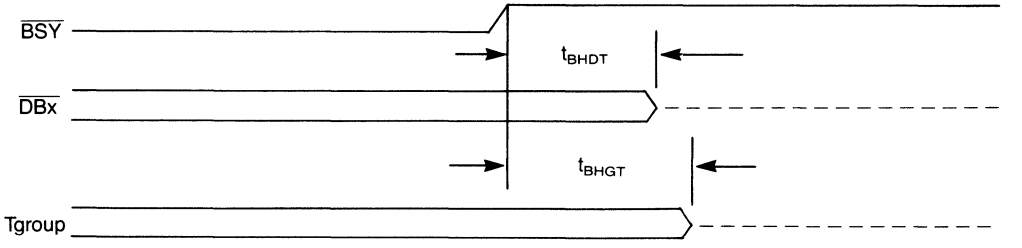
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{bhdt}	$\overline{BSY}$ IN HIGH TO DATA BUS TRISTATE		8*Tcyc +75ns	ns
t_{bhgt}	$\overline{BSY}$ IN HIGH TO Igroup TRISTATE		8*Tcyc +75ns	ns



NOTE: Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$

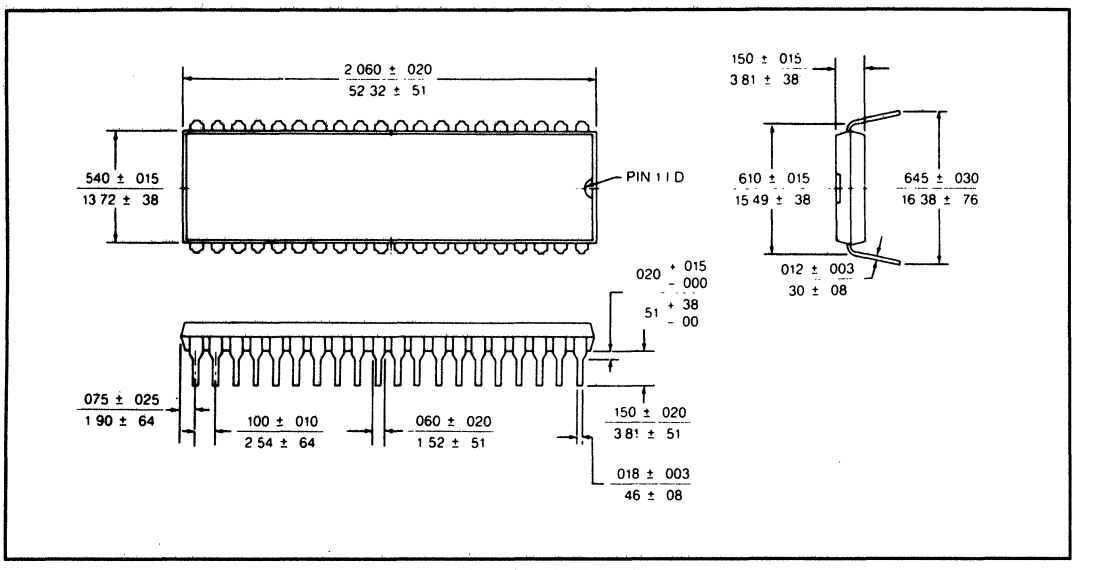
9.2.17 CONNECTED-AS-A-TARGET TO BUS FREE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{bhdt}	$\overline{BSY}$ OUT HIGH TO DATA BUS TRISTATE	8*Tcyc +75ns	ns	
t_{bhgt}	$\overline{BSY}$ OUT HIGH TO Tgroup TRISTATE		8*Tcyc +75ns	ns

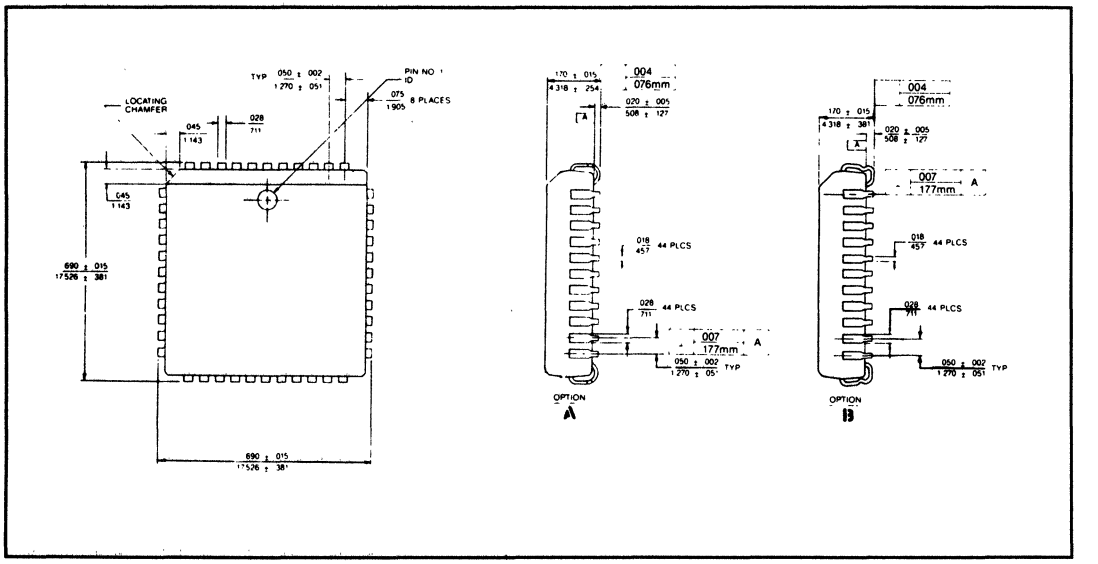


NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$

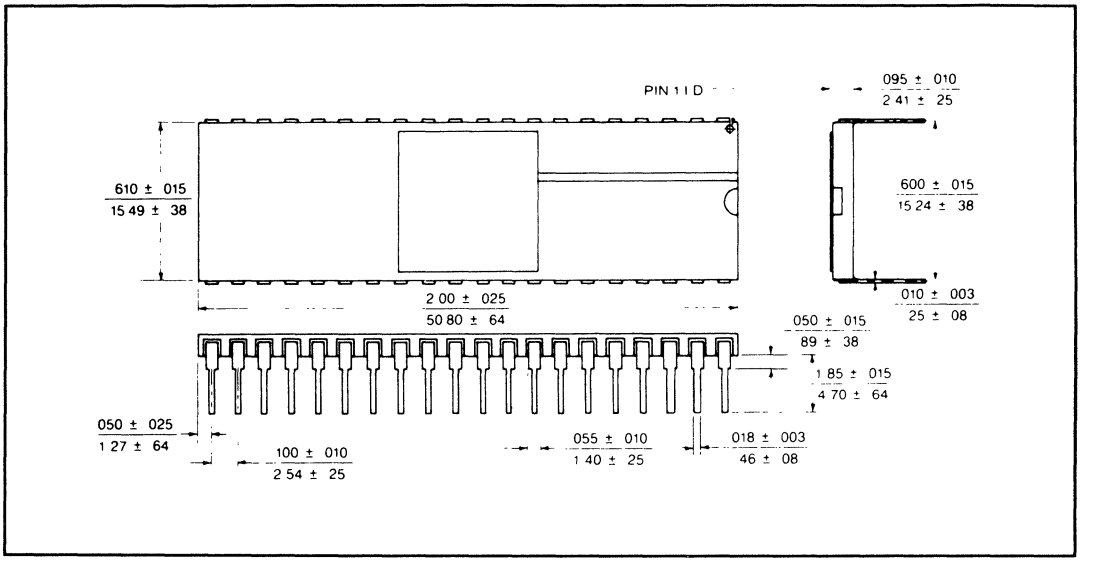
PACKAGE DIAGRAMS



40 LEAD PLASTIC "PL"
WD33C93A



44 LEAD PLASTIC "JM"
WD33C93A



40 LEAD CERAMIC "AL"
WD33C93A

29

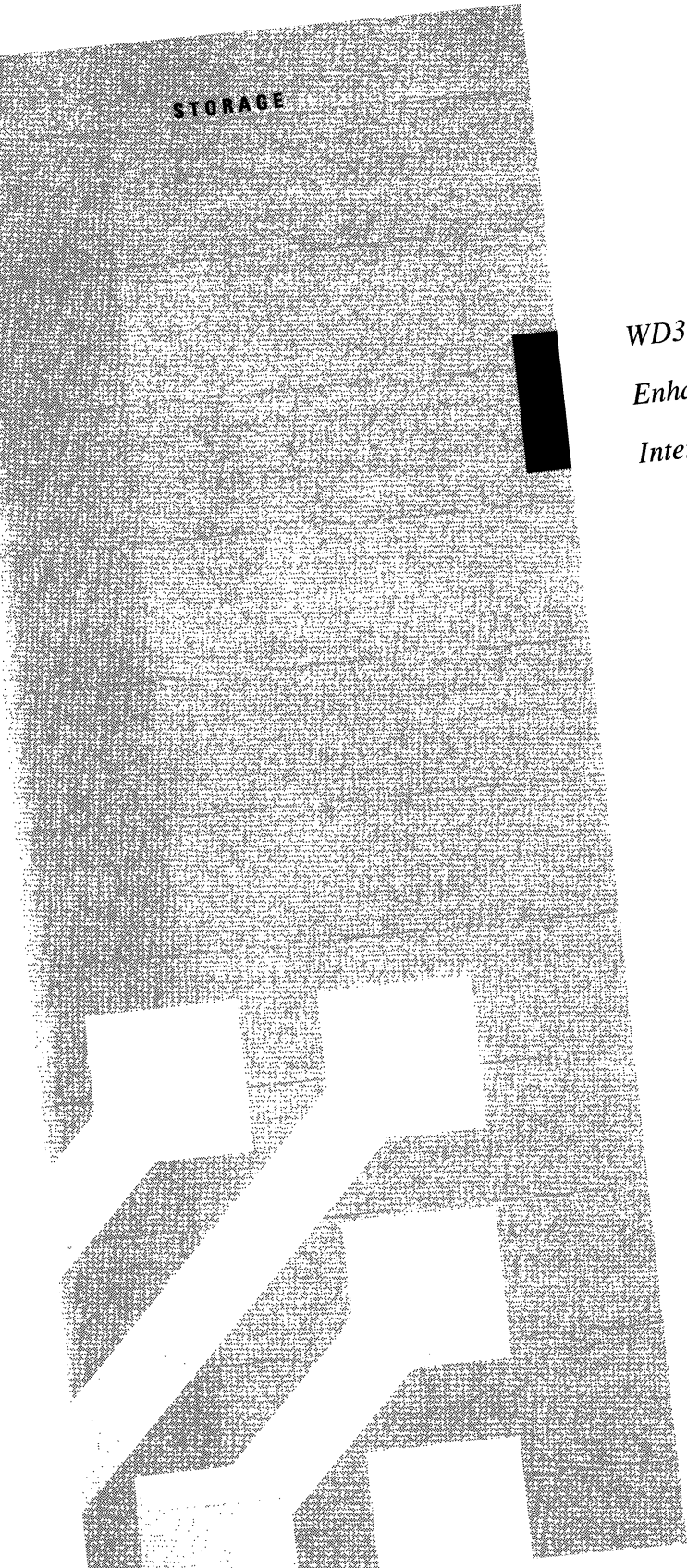
STORAGE

WD33C93B

Enhanced SCSI Bus

Interface Controller

30



WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

1.1 DESCRIPTION

The 33C93B, a MOS/VLSI device implemented in Western Digital's CMOS process, operates from a single 5 Volt supply and is available in either a 44-pin chip carrier or a 40-pin dual-in-line package. All inputs and outputs are TTL compatible.

The 33C93B is intended for use in systems which interface to the Small Computer System Interface (SCSI) Bus. The 33C93B can operate in both the initiator (typically, a host computer system) and the target (typically, a peripheral device) SCSI bus roles.

When used in the host system, the 33C93B interfaces to both the host bus and the SCSI bus. To perform a SCSI operation, the host processor issues a command to the 33C93B to select the desired target. The 33C93B then arbitrates for the SCSI bus and selects the peripheral unit. If it fails to get the bus because of a device with higher priority, it continues trying and notifies the host when it has succeeded by generating an interrupt. At this point, the 33C93B is operating in the initiator role. When the peripheral requests a SCSI command from the host, the 33C93B receives the request and generates another interrupt to the host. The host responds to this interrupt by issuing a "Transfer Info" command and supplying SCSI command bytes to the 33C93B. The 33C93B transfers the SCSI command to the peripheral and then waits for the next bus phase request. This process continues until all SCSI information including data, status, and messages have been transferred.

The 33C93B also offers high-level Select-and-Transfer commands which eliminate the interrupt handling otherwise required between each SCSI bus phase.

When the 33C93B is used in a peripheral system, the 33C93B operates primarily in a target role. It interfaces with a local processor and the SCSI bus in this environment just as it does when used in a host adapter. The target-role command set enables the 33C93B to request each SCSI bus phase individually or to sequence the SCSI bus phases automatically through the use of combination commands.

The 33C93B has an internal microcontroller, a register task file, and SCSI interface logic. This architecture supports both tight control of the protocol for non-standard SCSI implementations, as well as a hands-free mode for standard SCSI applications.

1.2 FEATURES

- ❑ Implements full SCSI bus features: arbitration, disconnect, reconnect, parity generation and checking on both data ports, soft reset, and synchronous data transfers.
- ❑ Includes 48 mA drivers for direct connection to the SCSI bus.
- ❑ Operates in both initiator and target roles.
- ❑ Synchronous offset selectable from one to twelve bytes.
- ❑ Programmable timeout for selection and reselection.
- ❑ Support for SCSI-2 features:
  - Synchronous transfer rates up to 10 Mbytes/s for Fast SCSI transfers; up to 5 Mbyte/s for standard SCSI transfers.
  - Select-and-Transfer, Reselect-and-Transfer, and Wait-for-Select-and-Receive commands provide support for queue tag messages and target routine identify messages.
- ❑ Special "Translate Address" command performs the Logical-to-Physical address mapping.
- ❑ "Combination" commands greatly reduce interrupt-handling responsibilities.
- ❑ Compatible with most microprocessors through an 8-bit data bus; supports both multiplexed and non-multiplexed address/data bus systems. Host bus data parity checking and generation is an optional feature.
- ❑ Burst data transfers up to 4096 bytes.
- ❑ Data transfer options include programmed I/O, single-byte DMA, burst (multibyte) DMA, or direct bus access (WD bus) transfers.
- ❑ Single +5 V supply.
- ❑ Available in 44-pin chip carrier or 40-pin DIP.
- ❑ Low-power CMOS design.

30

1.3 DIFFERENCES BETWEEN THE 33C93A AND 33C93B

The 33C93B delivers the same functionality as the 33C93A as well as additional features to support SCSI-2 and improve system performance. Unless the device is configured with the RAF bit in the OWN ID register set, the 33C93B is completely backward compatible to the 33C93A; consequently, in most applications, it may replace the 33C93A with no modification to the hardware or the firmware.

The 33C93B has grouped several recently added features of the 33C93A with two 33C93B-only enhancements into a mode enabled by configuring the device with the RAF bit set. Section 4.3.2 describes this new mode. The first two features---the loading of the microcode revision on a soft reset condition and the aborting of a target Receive command upon the detection of the SCSI Attention condition or of a parity error---existed in the 33C93A design. The 33C93B design has added to this mode the ability to detect possible data corruption and unexpected disconnects from the SCSI bus when operating as a target.

To support SCSI-2, the combination commands Select-and-Transfer, Reselect-and-Transfer, and Wait-for-Select-and-Receive optionally send or receive Queue-tag messages at appropriate points in the SCSI bus sequence. The host via two bits in the DESTINATION ID register and the newly added QUEUE TAG register provides information which the first two commands use to generate and check these messages. Wait-for-Select-and-Receive, through the same locations, relays information to the host regarding the type of Queue-tag message received, including whether the initiator sent a message or not, and the actual queue tag.

These commands also support the LUNTAR bit in the Identify message. By setting the corresponding bit in the TARGET LUN register, the host enables the Select-and-Transfer and Reselect-and-Transfer commands to send an Identify message for a target routine. In the case of Select-and-Transfer, setting this bit also enables the 33C93B to accept automatically an Identify message with the LUNTAR bit set. The host also has the option to let the Wait-for-Select-and-Receive command receive a target routine Identify message and proceed to the next phase or to interrupt the host so that it may reject the message when the application does not support target routines.

The last new feature pertaining to SCSI-2 relates to Fast SCSI. When the 33C93B has an input clock between 16 MHz and 20 MHz, by controlling the Fast SCSI Select (FSS) bit in the SYNCHRONOUS TRANSFER register, the host can select between normal synchronous transfers which reach a maximum transfer rate of 5 MB/s and Fast synchronous transfers with a peak rate of 10 MB/s on both the SCSI and host DMA interfaces.

The final addition to the 33C93B is the FIFO Full/Empty (FFE) bit in the AUXILIARY STATUS register to be used primarily during polled I/O transfers. As its name suggests, this bit reflects the full or empty state of the FIFO depending on the direction of the transfer. If the host is writing data to the FIFO, the 33C93B sets this bit when the FIFO is empty, indicating that the host may write up to twelve bytes to the FIFO without having to poll the DBR bit before writing each byte. Similarly, when the host is reading data from the FIFO, the 33C93B sets this bit when the FIFO is full, indicating that the host may read the DATA register twelve times without polling DBR before each read. Some restrictions do apply when using this bit, and they are described in Section 3.1.22.

2.0 PIN DESCRIPTIONS

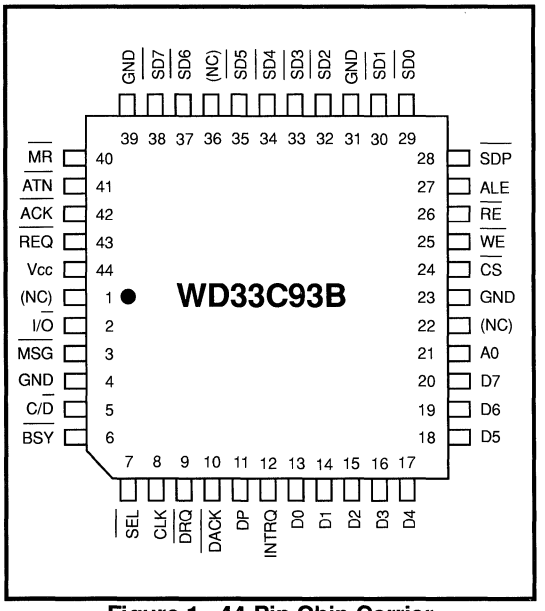


Figure 1. 44-Pin Chip Carrier

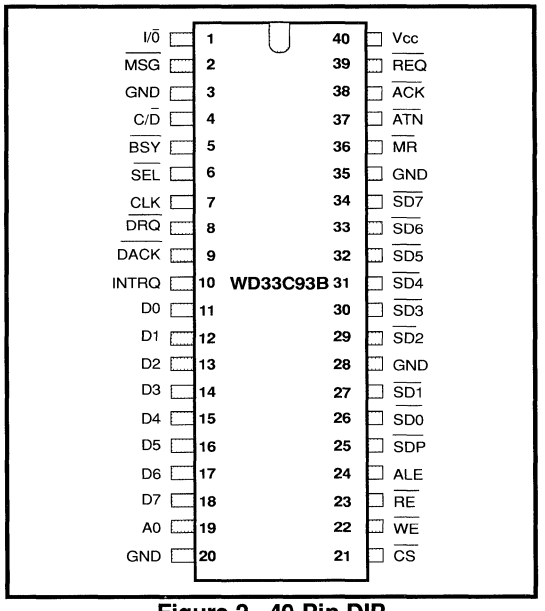


Figure 2. 40-Pin DIP

2.1 PROCESSOR/DMA INTERFACE

NAME	I/O	FUNCTION
CLK	I	8-20 MHz square wave clock
MR-	I	Reset is an active-low input which forces the 33C93B into an idel state and forces all SCSI signals to the negated state.
INTRQ	O	Interrupt Request to the external microprocessor indicates a command completion/termination or a need to service the SCSI interface. Reading the SCSI STATUS register clears this bit.
RE-	I/O	Read Enable is an active-low input used with CS- to read a register or with DACK- to access the DATA register in DMA mode. In WD Bus mode, it is used as an output to read data from a sector buffer. (TRI-STATE).
WE-	I/O	Write Enable is an active-low input used with CS- to write a register or with DACK- to access the DATA register in DMA mode. In WD Bus mode, it is used as an output to write data to a sector buffer. (TRI-STATE)
CS-	I	Chip Select is an active-low input which qualified RE- and WE- when accessign a register. This signal must be inactive during a DMA cycle (DACK- active in DMA and Burst DMA mode or DRQ active in WD Bus mode).
A0	I	Address Pin A0 is used to access the internal registers for non-multiplexed address/data busses (i.e.; the ALE pin is grounded). The address of the desired register is loaded into the address register during a write cycle with A0=0. The selected register is then accessed when A0=1.

NAME	I/O	FUNCTION
ALE	I	Address Latch Enable is used for multiplexed address/data busses to load the address of the desired 33C93B register from the data bus. For indirect addressing, the ALE pin should be grounded. See the description of the ADDRESS register for a complete discussion of direct and indirect addressing.
DACK- (RCS-)	I/O	DMA Acknowledge is an active-low input used for (RCS-) interfacing to an external DMA controller (e.g. 8237). When DACK- is low, all bus transfers are to or from the DATA register regardless of the contents of the ADDRESS register. In WD Bus mode this pin, an open-drain output, functions as a RAM Chip Select to the sector buffer. RE- and WE- are outputs when RCS- is active. Regardless of the host DMA mode selected, this pin should be pulled via external circuitry (e.g. a pullup resistor) to an inactive state and should not be left floating.
DRQ-	I/O	Data Request is an active-low output when used for interfacing to an external DMA controller and an active-high input when in WD Bus mode. In the first application, DRQ- and DACK- form the handshake for the DMA data transfers. In Burst mode, DRQ- remains low so long as there is data to transfer; in Single-byte DMA mode, DRQ- toggles for each byte. Since this pin is an open drain output, a pullup resistor may be required when operating in these modes. In WD Bus mode, this pin becomes the DRQ input. A high level on this pin enables the 33C93B to perform burst transfers; a low level inhibits transfers by deasserting RCS-and disabling the RE- and WE- outputs.
D7 - D0	I/O	Processor data bus.
DP	I/O	Data Parity is used only for checking and generating parity during data transfers.

2.2 SCSI INTERFACE

NAME	I/O	FUNCTION
ATN-	I/O	ATN- is an output in the initiator role and an input in the target role. Its assertion indicates the ATTENTION condition.
REQ-	I/O	REQ- is an input in the initiator role and an output in the target role. It indicates a request for a data transfer.
ACK-	I/O	ACK- is an output in the initiator role and an input in the target role. It indicates an acknowledgement of a data transfer.
MSG-	I/O	MSG- is an input in the initiator role and an output in the target role. The target asserts this signal when requesting message information.
C/D-	I/O	C/D- is an input in the initiator role and an output in the target role. It specifies whether CONTROL or DATA information is on the SCSI data bus.
I/O-	I/O	I/O- is an input in the initiator role and an output in the target role. It controls the direction of data movement on the SCSI data bus with respect to an initiator.
SD7-	I/O	SCSI data bus.
SD0-	I/O	SCSI data bus.
SDP-	I/O	SCSI data bus parity signal.
BSY-	I/O	BSY- is asserted when the 33C93B is attempting to arbitrate for the SCSI bus or when connected as a target.
SEL-	I/O	SEL- is asserted when the 33C93B is attempting to select or reselect another SCSI device.

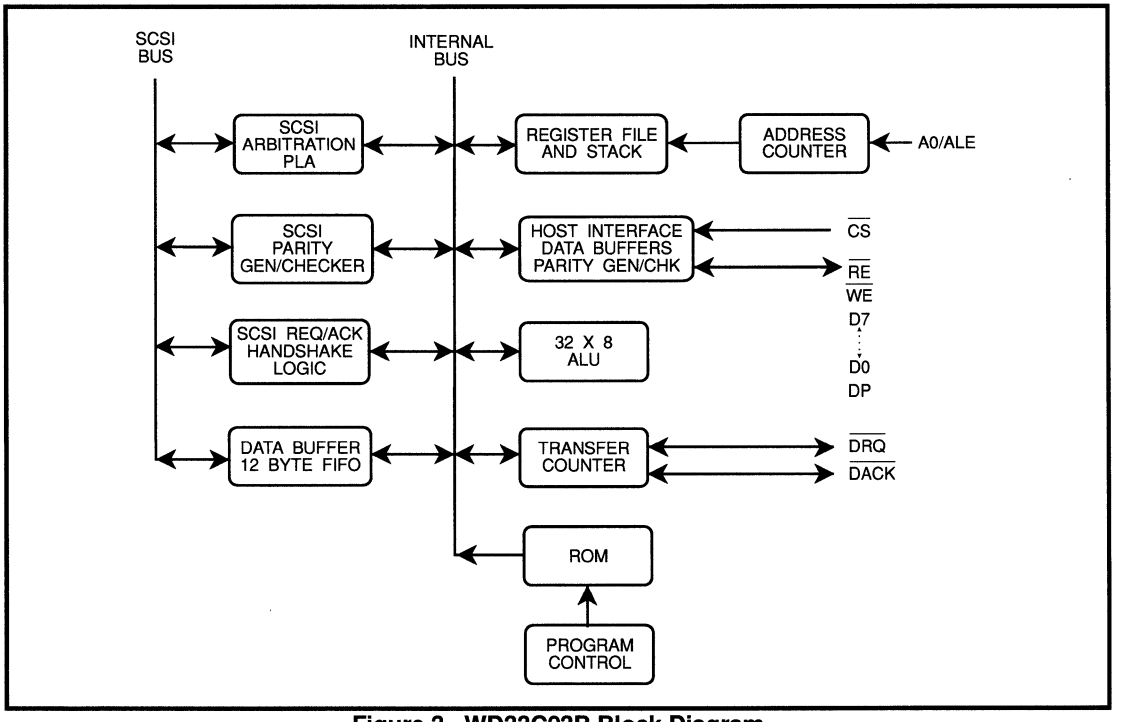


Figure 3. WD33C93B Block Diagram

3.0 WD33C93B REGISTERS

REGISTER MAP				
A0	**R/W**	**REGISTER ACCESSED**		**ADDRESS (HEX)**
0	R	Auxiliary Status Register		XX
0	W	Address Register		XX
1	R/W	Own ID Register	/CDB Size	00
1	R/W	Control Register		01
1	R/W	Timeout Period Register		02
1	R/W	Total Sectors Register	/CDB 1st	03
1	R/W	Total Heads Register	/CDB 2nd	04
1	R/W	Total Cylinders Register (MSB)	/CDB 3rd	05
1	R/W	Total Cylinders Register (LSB)	/CDB 4th	06
1	R/W	Logical Address (MSB)	/CDB 5th	07
1	R/W	Logical Address (2nd)	/CDB 6th	08
1	R/W	Logical Address (3rd)	/CDB 7th	09
1	R/W	Logical Address (LSB)	/CDB 8th	0A
1	R/W	Sector Number Register	/CDB 9th	0B
1	R/W	Head Number Register	/CDB 10th	0C
1	R/W	Cylinder Number (MSB) Register	/CDB 11th	0D
1	R/W	Cylinder Number (MSB) Register	/CDB 12th	0E
1	R/W	Target LUN Register		0F
1	R/W	Command Phase Register		10
1	R/W	Synchronous Transfer Register		11
1	R/W	Transfer Cound Register (MSB)		12
1	R/W	Transfer Cound Register (2nd Byte)		13
1	R/W	Transfer Cound Register (LSB)		14
1	R/W	Destination ID Register		15
1	R/W	Source ID Register		16
1	R	SCSI Status Register		17
1	R/W	Command Register		18
1	R/W	Data Register		19
1	R/W	Queue Tage Register		1A

NOTE: 1. All unused bits of a defined register are reserved and must be zero.
2. Reading an undefined or unavailable register results in an all-ones data bus output.
3. Register addresses are determined by the ADDRESS register bist AR7 through AR0.
4. When using a multiplexed address/data bus with ALE, the A0 pin is ignored, and the ADDRESS register is loaded with ALE. In this mode, the AUXILIARY STATUS register is mapped at 1F hex.
5. See section 3.2 for a description of how reset affects the internal registers.

3.1 REGISTER DESCRIPTIONS

3.1.1 Auxiliary Status Register

The AUXILIARY STATUS register, a read-only register, contains general status information not directly associated with the interrupt condition. The host may access the AUXILIARY STATUS register at any time except during DMA accesses. (DACK- asserted in DMA/Burst mode or RCS- asserted in WD bus mode).

7	6	5	4	3	2	1	0
INT	LCI	BSY	CIP	O	FFE	PE	DBR

Bit 0 DBR-DATA BUFFER READY
DATA BUFFER READY indicates to the processor whether or not the DATA register is available for reading or writing. During a Send command or a Transfer Info command which transmits data over the SCSI bus, the 33C93B sets this bit when ready to take a byte from the host; it resets this bit when the processor writes the byte to the DATA register. During a Receive command or a Transfer Info command which receives data over the SCSI bus, the 33C93B sets DBR when it receives a byte and resets DBR when the processor reads the byte from the DATA register.

Bit 1 PE-DATA BUFFER READY
PARITY ERROR status indicates that the 33C93B received a byte with even parity during a transfer. SCSI parity checking is always enabled; host parity checking is enabled via the EHP bit in the OWN ID register Detection of a parity error will set the PE status bit regardless of the state of the HHP or HSP bits in the CONTRO register. Issuing a command clears the PE bit.

Bit 2 FFE -DATA BUFFER READY
FIFO FULL/EMPTY indicates when the FIFO is full or empty depending on the direction of the transfer. (see 3.1.22)

Bit 4 CIP -DATA BUFFER READY
COMMAND IN PROGRESS indicates that the 33C93B is interpreting the last command entered into the COMMAND register which is therefore unavailable.

Bit 5 BSY-BUSY
BUSY indicates that a Level II command is currently executing, so the host may only access the COMMAND register (when CIP = 0),the DATA register, and the AUXILIARY STATUS register. When this bit is set, the host should not issue a Level II command.

Bit 6 LCI -DATA BUFFER READY
LAST COMMAND IGNORED indicates that the 33C93B ignored a command because the host issued it just prior to or concurrent with a pending interrupt.

Bit 7 INT-DATA BUFFER READY
INTERRUPT PENDING reflects the state of the INTRQ pin. When set, the host should read the SCSI STATUS register to clear INTRQ prior to issuing any commands.

30

3.1.2 Address Register

The ADDRESS register, a write-only register, holds the address of the register to be accessed. Registers in the 33C93B may be accessed in one of two ways:

- Direct addressing (multiplexed address/data busses). In this mode, the falling edge of the ALE signal latches the contents of the host data bus into the ADDRESS register. The CS- and WE- or RE- signals typically follow to access the selected register. When using direct addressing, the A0 pin should be connected to ground, and the AUXILIARY STATUS register is located at address 1F hex.
- Indirect addressing (separate address/data busses). This method, enabled by tying ALE to ground, requires two separate cycles for a register access. The first cycle loads the desired address into the ADDRESS register by writing (CS- and WE- asserted) to the 33C93B with A0=0.The second cycle, with A0=1, then reads (CS- and RE- asserted) or writes (CS- and WE- asserted) the selected register. Every cycle with A0=1 increments the ADDRESS register except when accessing the DATA or COMMAND registers. In indirect

addressing, the AUXILIARY STATUS register is accessed by performing a read (CS- and RE- asserted) with A0=0.

3.1.3 Own ID/CDB Size Register

The OWN ID/CDB SIZE register, in its first mode, contains information which the Soft Reset command uses to configure the device. Following a hardware reset, the host, before issuing any other command, must initialize this register and issue the Reset command to set the clock divisor and the SCSI bus ID of the device and to enable various sets of features and host bus parity checking.

In the second mode, bits 3-0 of this register specify the SCSI CDB size if the command group is unknown (i.e. not a group 0, group 1, or group 5 SCSI command) to the 33C93B during the Select-and-Transfer and Wait-for-Select commands. This mode is enabled only when advanced features (see 4.3.1) have been selected.

7	6	5	4	3	2	1	0
FS1	FS0	0	EHP	EAF	ID2	ID1	ID0

Bit 0-2 IDn- SCSI ID BITS
SCSI ID Bits 0-2 set the SCSI bus ID that the 33C93B uses during arbitration and selection.

Bit 3 EAF-ENABLE ADVANCED FEATURES
ENABLE ADVANCED FEATURES, when set, enables functions described in section 4.3.1.

Bit 4 EHP-ENABLE HOST PARITY
ENABLE HOST PARITY enables odd parity checking on the host bus. The PE bit in the AUXILIARY STATUS register will then also indicate parity errors detected on the host bus, and the HHP bit in the CONTROL register will have effect during transfers. When host parity is disabled, the PE bit is not set when a parity error occurs on the host bus,and the HHP bit must be set to zero. NOTE: Parity is always generated on the host data parity bit (DP), regardless of the state of this bit.

Bit 5 RAF-REALLY ADVANCED FEATURES
REALLY ADVANCED FEATURES, when set, enables features described in section 4.3.2.

Bit 6-7 FSn-FREQUENCY SELECT
FREQUENCY SELECT 0-1 select the divisor that is applied to the input clock. The divided clock is used for data transfer timing and for SCSI bus arbitration timing. The table below shows input clock frequency ranges and their corresponding divisors. An incorrect divisor for the input clock may result in violation of SCSI bus timing specifications.

INPUT CLOCK FREQUENCY (MHz)	FS1	FS0	RESULTING DIVISOR
8-10	0	0	2
12-15	0	1	3
16-20	1	0	4
XX	1	1	Undefined

Note that a clock rate between 10 MHz and 12 MHz should not be used, as the resulting SCSI bus clear delay may violate SCSI specifications. The formula for computing the maximum SCSI data transfer rate is given in Section 6.

3.1.4 Control Register

The CONTROL register consists of option bits which affect response to parity errors and to the SCSI attention condition, suppress interrupts, allow command chaining, and select the mode of DMA transfer.

7	6	5	4	3	2	1	0
DM2	DM1	DM0	HHP	EDI	IDI	HA	HSP

Bit 0 HSP-HALT on SCSI PARITY ERROR
The HALT on SCSI PARITY ERROR bit enables the 33C93B to terminate a Receive or Transfer Info command if a parity error occurs on an incoming SCSI data byte. Asynchronous transfers check

parity on every byte; synchronous data transfers check parity on 4096-byte boundaries in most cases. In the initiator role, the 33C93B responds to a SCSI parity error by leaving the ACK- pin asserted to inhibit any additional data transfers (REQs) by the target and to facilitate error handling with the target. If Immediate Halts are enabled, a SCSI parity error during a synchronous Receive or Reselect-and-Receive command will abort the transfer before the 4096-byte boundary.

Bit 1 HA-HALT on ATTENTION
The HALT on ATTENTION bit (target mode only) enables the 33C93B to terminate a Send or Receive command if the initiator asserts ATN-. The 33C93B normally tests for the ATN-condition before the start of a data transfer, on 4096 byte boundaries, and after the end of the transfer. If the Immediate Halt feature is enabled, an Abort command will be issued upon recognition of the ATN-condition. These rules apply to both synchronous and asynchronous transfers.

Bit 2 IDI-INTERMEDIATE DISCONNECT INTERRUPT
The INTERMEDIATE DISCONNECT INTERRUPT bit, when set in the initiator role, causes the 33C93B to terminate a Select-and-Transfer command and generate an 85 hex interrupt upon a proper target disconnect. When this bit is reset, a valid disconnect will not cause the 33C93B to generate an interrupt, and command execution proceeds. This feature, when used with the Resume SAT command, provides support for overlapped SCSI operations. In the target role, the IDI bit selects combination command execution options. Refer to Section 4 for more details.

Bit 3 EDI-ENDING DISCONNECT INTERRUPT
The ENDING DISCONNECT INTERRUPT bit, when set, delays the 16 hex interrupt which normally follows receipt of the Command-Complete message during a Select-and-Transfer command until after the target disconnects, replacing the 85 hex interrupt. This bit also enables chaining between certain target-role combination commands to reduce host system overhead. Refer to Section 4 for more details.

Bit 4 HHP-HALT on HOST PARITY ERROR
The HALT on HOST PARITY ERROR bit allows the 33C93B to terminate a Send or Transfer command if a parity error occurs on an incoming host data byte. The 33C93B checks for host parity errors according to the sames rules it uses when checking for SCSI parity errors. However, a host parity error will not leave the ACK- signal asserted.

Bit 5-7 DMx-DMA MODE SELECT
The DMA MODE SELECT bits 2-0 select the host bus transfer mode to be used during a Data phase. The following table describes the different DMA modes and specifies the state of these bits to select each mode:

DM2	DM1	DM0	DMA MODE SELECTED
0	0	0	POLLED I/O MODE or no DMA enabled. The host must poll for DBR in the AUXILIARY STATUS register and then, depending on the direction of the transfer, read or write the DATA register.
0	0	1	BURST MODE or demand-mode DMA. In this mode, the DRQ- signal will remain active so long as data or space exists in the internal FIFO to allow the transfer to continue. The DMA controller responds by asserting DACK- and pulsing RE- or WE- to transfer the data.
0	1	0	WD-BUS MODE or Direct Buffer Access (DBA) mode. In this mode, the 33C93B acts as a bus master, and all data access signals reverse their directions. The DRQ- pin becomes the DRQ input, which when high, enables the 33C93B to drive the buffer control signals. The DACK- pin becomes the RCS- output and serves as a chip select for the buffer. The RE- and WE- pins become outputs which drive the read and write functions of the RAM buffer. Transfers will continue in a burst manner until the transfer is complete or until the external buffer logic pauses the transfer by negating the DRQ signal. One transfer may occur after DRQ drops and then the DACK-, RE-, and WE- signals will tristate.
1	0	0	DMA MODE or Single-byte DMA. In this mode,a DRQ-/DACK- handshake occurs for each byte.The DMA controller transfers the byte by asserting WE- or RE- while asserting DACK-.

3.1.5 Timeout Period Register

The TIMEOUT PERIOD register stores a user-selected, 8-bit value which determines the timeout period for selection and reselection attempts. The timeout period specifies how long the 33C93B will wait for a response (i.e. assertion of the BSY- signal) after it has begun the Selection phase (asserted SEL- and negated BSY-) before terminating the command. Loading this register with zero disables the timeout feature. For a desired timeout period, the register value depends upon the input clock frequency, as shown in the following equation:

$$\text{register value} = \frac{\text{Tper} * \text{Ficlk}}{80}$$

where Tper = the desired timeout period in milliseconds; Ficlk = the input clock frequency at the MCK pin in megahertz (with no divisor applied).

The constant '80' scales the units of the equation, as it is based on the internal timeout cycle time. The user should round the resulting 'register value' up to the next integral value to ensure that the minimum timeout requirement is met.

3.1.6 Command Descriptor Block Registers

The COMMAND DESCRIPTOR BLOCK registers hold the SCSI command bytes to be sent during Command phase of a Select-and-Transfer command and the command bytes received during the Command phase of a Wait-for-Select-and-Receive command.

The Send-Status-and-Command-Complete command uses the contents of the CDB11 register as the returned status and determines the type of the Command-Complete message to send from the contents of the CDB12 register. Bit 0 of CDB12 selects whether the command sends a simple Command-Complete message bit 0=0) or a Linked-

Command-Complete message (bit 0=1). In the latter case, bit 1 of CDB12, the FLAG bit, specifies whether a 0A hex (FLAG=0) or a 0B hex (FLAG=1) message is sent.

3.1.7 Total Sectors Register

The TOTAL SECTORS register stores an 8-bit value specifying the total number of sectors per track for the Translate Address command.

3.1.8 Total Heads Register

The TOTAL HEADS register stores an 8-bit value specifying the total number of heads for the Translate Address command.

3.1.9 Total Cylinders Register

The TOTAL CYLINDERS register stores a 16-bit value specifying the total number of cylinders for the Translate Address command.

3.1.10 Logical Address Register

The LOGICAL ADDRESS register stores the 32-bit logical address to be translated by the Translate Address command.

3.1.11 Sector Number Register

The SECTOR NUMBER register will contain the resulting physical sector number following a Translate Address command.

3.1.12 Head Number Register

The HEAD NUMBER register contains the resulting head number following a Translate Address command.

If the host desires the 33C93B to compensate for spare sectors on the disk, this register should contain the number of spare sectors per cylinder prior to issuing the Translate Address command. A value of zero indicates no compensation. With compensation, the maximum number of cylinders allowed is 4096, and the maximum number of heads is 15.

3.1.13 Cylinder Number Register

The CYLINDER NUMBER register contains a 16-bit value specifying the resulting cylinder number following a Translate Address command.

If the host desires the 33C93B to compensate for spare sectors on the disk, the Translate Address command expects this register to contain the number of sectors per cylinder after allowing for the spares, i.e. (sectors/track * heads - spares/cylinders).

3.1.14 Target LUN Register

The TARGET LUN register holds the Logical Unit Number (LUN) and other target status information during various 33C93B commands and sequences.

The Select-and-Transfer commands use the contents of this register and the SOURCE ID register to generate and check Identify messages. In addition, these commands also store the returned status byte from the target in this register. For proper operation of the Select-and-Transfer commands, the host should not set the TLV bit in this register.

In advanced mode, the Select-and-Transfer commands, in the event of an unexpected reselection, place the logical unit number (TRN=0) or the target routine number (TRN=1) of a reselecting target in this register. The TLV and DOK bits will be zero.

The Wait-for-Select-and-Receive command places a copy of a received Identify message in this register. If the TLV bit is zero, the initiator did not send a valid Identify message. If the TLV bit is one, the initiator sent a valid Identify message, and the DOK bit will then indicate whether or not the initiator has enabled disconnects. The Wait-for-Select-and-Receive command will accept an Identify message with the TRN bit set only if the host issues the command with the SBT bit in the COMMAND register set.

The Reselect-and-Transfer commands use only the LUN portion and the TRN bit of this register to generate the Identify message. The TLV and DOK bits are not used.

7	6	5	4	3	2	1	0
TLV	DOK	TRN	0	0	TL2	TL1	TL0

3.1.15 Command Phase Register

The COMMAND PHASE register indicates which phases of a combination command have completed. Thus, if the command has terminated abnormally, the processor can read this register to determine the cause of the termination and decide how to respond to it.

When resuming a combination command, the contents of this register specify from which point to restart the command. Refer to the description of the specific commands for details regarding the various command phases and resume values.

7	6	5	4	3	2	1	0
0	CP6	CP5	CP4	CP3	CP2	CP1	CP0

3.1.16 Synchronous Transfer Register

The contents of the SYNCHRONOUS TRANSFER register specify the maximum transfer rate and the transfer mode for a SCSI data phase.

For information phases other than a Data phase or when the selected offset is zero (OF3=OF2=OF1=OF0=0), the 33C93B performs asynchronous transfers. A non-zero offset value, which should be twelve or less, selects synchronous data transfers and determines the effective FIFO depth. This value is typically determined through negotiation (as defined in the SCSI standard) with the other SCSI device.

The Transfer Period control bits select the minimum transfer period for both synchronous and asynchronous SCSI data transfers and, in WD-Bus mode, the transfer period and the width of the RE-/WE- strobes for host transfers; for non-data transfers, the transfer period defaults to six periods. The period is defined in terms of the internal clock cycle time, which depends upon the input clock, the divisor selected in the OWN ID register, and the setting of the FSS bit.

The FSS bit has effect only when operating with an input clock frequency of 16-20 MHz, i.e. the divisor set to 4. Setting this bit enables Fast SCSI transfers, doubling the maximum transfer rate for synchronous transfers. For example, with a 20 MHz input clock and a transfer period of 2, the normal maximum transfer rate (FSS=0) would be 5 MB/s; the Fast SCSI transfer rate (FSS=1) would be twice this value or 10 MB/s. The FSS bit does not affect the rate of asynchronous transfers.

7	6	5	4	3	2	1	0
FSS	TP2	TP1	TP0	OF3	OF2	OF1	OF0

Bit 0-3 OFx - OFFSET

The OFFSET bits specifies the desired offset according to the following table:

3	2	1	0	SELECTED OFFSET
0	0	0	0	0 Note 1
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	Undefined
1	1	1	X	Undefined

Note 1 - Asynchronous data phase transfers.

Bit 4-6 TPx - TRANSFER PERIOD

The TRANSFER PERIOD bits select the desired desired transfer period according to the following table:

6	5	4	SCSI/WD-BUS TRANSFER PERIOD	(SCSI REQ/ACK Synchronous Pulse Width and WD-BUS RE- /WE- Pulse Width
0	0	X	8 cycles	(4 cycles)
0	1	0	2 cycles	(1 cycle)
0	1	1	3 cycles	(1 cycle)
1	0	0	4 cycles	(2 cycles)
1	0	1	5 cycles	(3 cycles)
1	1	0	6 cycles	(4 cycles)
1	1	1	7 cycles	(4 cycles)

The 'cycle' referred to above is the period of the internal data transfer clock. For asynchronous transfers or for synchronous transfer when the input clock frequency is less than 16 MHz, it is calculated as follows:

$$\text{CYCLE } (\mu s) = \frac{\text{DIVISOR (from OWN ID)}}{2 * \text{INPUT CLOCK FREQUENCY (MHz)}}$$

30

For synchronous transfers when the input clock frequency is 16 MHz or greater, the cycle time is calculated as follows:

$$\text{CYCLE } (\mu s) = \frac{2}{(\text{FSS}+1) * \text{INPUT CLOCK FREQUENCY (MHz)}}$$

Bit 7 FSS - FAST SCSI SELECT

The FAST SCSI SELECT bit under the conditions mentioned above enables the doubling of the internal clock frequency resulting in a synchronous transfer rate up to 10 MB/s.

3.1.17 Transfer Count Register

The TRANSFER COUNT register, a 24-bit register, stores a preset value for the internal transfer counter. A Send, Receive, or Transfer Info command causes the 33C93B to load this preset value into the internal transfer counter, which then decrements as each data byte is transferred over the SCSI bus and causes a "successful completion" interrupt when it reaches zero.

Loading the TRANSFER COUNT register with zeros prior to issuing these command or issuing the command with the SINGLE-BYTE TRANSFER bit set in the COMMAND register disables the counter function. If the counter is disabled, the Send, Receive, or Transfer Info command will complete when a single byte has been transferred.

In combination commands, this register specifies the number of bytes to be transferred during a Data phase. A zero value indicates the lack of a Data phase.

After the completion of any successful transfer, including commands issued in Single Byte Transfer mode, the TRANSFER COUNT register will be zero.

When a transfer halts because of an error condition, a SCSI bus phase change, or an abort, the TRANSFER COUNT register will contain the number of bytes NOT successfully transferred over the SCSI bus, including any bytes present in the FIFO at the time of the interruption. The FIFO clearing

process may cause the TRANSFER COUNT register to differ with the host DMA controller count, because some bytes may have been transferred into the FIFO but not to the SCSI bus.

3.1.18 Destination ID Register

The DESTINATION ID register stores the encoded SCSI bus ID of the device to be selected or reselected when a Select or Reselect command is issued. This register also contains control bits that affect the operation of certain combination commands.

7	6	5	4	3	2	1	0
SCC	DPD	DF	TG1	TG0	DI2	DI1	DI0

Bit 3-4 TGx - TAG MESSAGE
The TAG MESSAGE bits select which tag message code to send during Select-and-Transfer and identify which tag message code was received by the Wait-for-Select-and-Receive command. In addition, the Reselect-and-Transfer commands send a Simple-Queue Tag message following the Identify message if either of these bits are set.

4	3	MESSAGE RECEIVED OR SENT
0	0	No Message
0	1	SIMPLE QUEUE TAG (20H)
1	0	HEAD OF QUEUE TAG (21H)
1	1	ORDERED QUEUE TAG (22H)

Bit 5 DF -DISABLE FEATURE
DISABLE FEATURE, when set, disables Data phase direction checking in advanced mode and inhibits the normally automatic link from Send-Status-and-Command-Complete to the command fetch portion of Wait-for-Select-and-Receive when a Linked-Command-Complete message is sent.

Bit 6 DPD - DATA PHASE DIRECTION
DATA PHASE DIRECTION, when advanced features are enabled (see 4.3.1), specifies the expected direction of the SCSI Data phase of a Select-and-Transfer command. When this bit is zero, the expected direction is out (to the target), and when this bit is one, the expected direction is in (from the target). An unexpected data phase error will occur if the actual direction does not match the setting of this bit.

Bit 7 SCC - SELECT COMMAND CHAIN
SELECT COMMAND CHAIN selects which command will follow a Reselect-and-Transfer command when chaining is enabled (EDI=1). When this bit is zero, a Send-Status-and-Command-Complete command will follow; when this bit is one, a Send-Disconnect-Message command follows.

3.1.19 Source ID Register

The SOURCE ID register is used to report the SCSI bus ID of the device that has selected or reselected the 33C93B. It also contains bits that enable and control response to selection and reselection.

7	6	5	4	3	2	1	0
ER	ES	DSP	0	SIV	SI2	SI1	SI0

Bit 2-0 SIx - SOURCE ID
SOURCE ID Bits 2-0, valid only if the SIV bit is set, indicate the SCSI bus ID of the device that selected or reselected the 33C93B.

Bit 3 SIV - SOURCE ID VALID
SOURCE ID VALID is set to one when the 33C93B is selected or reselected and the other SCSI bus device asserted its own bus ID bit during the Selection/Reselection phase. This bit is zero if only the bus ID bit of the 33C93B was asserted.

Bit 5 DSP DISABLE SELECT PARITY
DISABLE SELECT PARITY, when set, causes the 33C93B to ignore the bus parity when responding to selection or reselection.

Bit 6 ES - ENABLE SELECTION
ENABLE SELECTION, when set, allows the 33C93B to respond to selection by another device on the SCSI bus.

Bit 7 ER - ENABLE RESELECTION
ENABLE RESELECTION, when set, allows the 33C93B to respond to reselection by another device on the SCSI bus.

3.1.20 SCSI Status Register

The SCSI STATUS register, a read-only register, holds a value which indicates the cause of the most recent INTRQ assertion. The 33C93B asserts INTRQ whenever a condition occurs that requires intervention by the host. For example,

- the 33C93B has been reset;
- the command completed successfully;
- the bus phase changed;
- an error occurred.

After assertion of INTRQ, the contents of this register will not change until the host reads the register or until the 33C93B has been reset.

7	6	5	4	3	2	1	0
SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0

Bit 0-3 SSx - SCSI STATUS
SCSI STATUS bits 0-3 are status qualifiers with meanings that depend upon the upper (4-7) status bits.

Bit 4-7 SSx - SCSI STATUS
SCSI STATUS bits 4-7 define the type of interrupt that occurred. The following table describes the various types:

30

STATUS	CODE	GROUP MEANING
0000	xxxx	The 33C93B is in a reset state.
0001	xxxx	A 33C93B command has completed successfully.
0010	xxxx	A 33C93B command has paused or was aborted.
0100	xxxx	A 33C93B command has been terminated prematurely due to an error or other unexpected condition.
1000	xxxx	An event on the SCSI bus requires service.

All other Status Code groups are currently not used and are reserved for future use.

In the following tables, the 'STATE' column indicates the state---Disconnected, Target, or Initiator--from which the Status Code can occur. The MCI field refers to the signals that define a SCSI bus information transfer phase: MSG-, C/D-, and I/O-. A bit set to one indicates that the signal is asserted on the SCSI bus; a zero indicates negation. Whenever one of these Status Codes occurs, the REQ- signal is asserted on the SCSI bus. The table on the right summarizes the meaning of the MCI field:

MCI CODE	MEANING
000	Data Out phase
001	Data In phase
010	Command phase
011	Status phase
100	Unspecified Info Out phase
101	Unspecified Info In phase
110	Message Out phase
111	Message In phase

RESET STATE INTERRUPTS			
STATUS	**CODE**	**STATE**	**SPECIFIC MEANING**
0000	0000	DT1	33C93 Reset. The device has been hard reset, or a Reset command has executed successfully with no advanced features enabled. The new state of the 33C93B is disconnected.
0000	0001	DT1	33C93B Reset. The device has successfully completed a Reset command with advanced features enabled. The new state of the 33C93B is disconnected.

SUCCESSFUL COMPLETION INTERRUPTS			
STATUS	**CODE**	**STATE**	**SPECIFIC MEANING**
0001	0000	D	A Reselect command completed successfully. The new state of the 33C93B is connected as a target.
0001	0001	D	A Select command completed successfully. The new state of the 33C93B is connected as an initiator.
0001	0010	-	Reserved for future use.
0001	0011	T	A Receive, Send, Reselect-and-Transfer, Wait- for-Select-and-Receive, Send-Status-and- Command-Complete, or Send-Disconnect-Message command completed successfully (ATN- is not asserted).
0001	0100	T	A Receive, Send, Reselect-and-Transfer, Wait-for-Select-and-Receive, or Send-Status-and- Command-Complete command completed successfully (ATN- is asserted).
0001	0101	DT	A Translate Address command completed successfully.
0001	0110	I	A Select-and-Transfer command completed successfully.
0001	0111	-	Reserved for future use.
0001	1MCI	I	A Transfer Info (non-Message-In phase) command completed successfully. MCI defines the new information type (SCSI bus phase) requested.

PAUSED OR ABORTED INTERRUPTS			
STATUS	**CODE**	**STATE**	**SPECIFIC MEANING**
0010	0000	I	A Transfer Info (Message In phase) command has paused with ACK- asserted, giving the host the opportunity to reject the message.
0010	0001	I	A Save-Data-Pointer message was received during a Select-and-Transfer command. The host should save its current data buffer pointer.
0010	0010	D	A Select, Reselect, or Wait-for-Select-and- Receive command aborted.
0010	0011	T	A Receive or Send command aborted, or a Wait- for-Select-and-Receive detected an error in the Identify message. (ATN- is not asserted).
0010	0100	T	A command aborted or halted due to assertion of ATN-, or a Wait-for-Select-and-Receive detected an error in the Identify message. (ATN- is asserted).
0010	0101	T	A transfer has aborted because of a violation of the data transfer protocol, possibly corrupting the data.
0010	0110	I	An I/O process with a queue tag which does not match the value in the QUEUE TAG register reselected the 33C93B. ACK- has been left asserted.
0010	0111	I	A target whose SCSI bus ID does not match the ID in the DESTINATION ID register reselected the 33C93B or the following Identify message did not match the LUN in the TARGET LUN register. ACK- has been left asserted following the Identify message, and the bus ID and LUN of the reselecting target are available in the SOURCE ID and TARGET LUN registers. This status only occurs when executing a Select-and-Transfer in advanced mode.
0010	1MCI	-	Reserved for future use.

TERMINATED INTERRUPTS			
STATUS	**CODE**	**STATE**	**SPECIFIC MEANING**
0100	0000	DTI	An invalid command was issued.
0100	0001	TI	An unexpected disconnect occurred. The new state of the 33C93B is disconnected.
0100	0010	D	A timeout occurred during a Select or Reselect command. The state of the 33C93B is disconnected.
0100	0011	TI	A parity error caused a command to terminate (ATN- is not asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100	0100	T	A parity error caused a command to terminate (ATN- is asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100	0101	DT	A Translate Address command did not complete successfully. The Logical Address exceeded the disk boundaries.
0100	0110	I	A target whose SCSI bus device ID does not match the bus ID set in the DESTINATION ID register has reselected the 33C93B during a Select-and-Transfer command. This interrupt occurs when the 33C93B is not in advanced mode. The state of the 33C93B is connected as an initiator.
0100	0111	I	A status byte with a parity error was received during Select-and-Transfer.
0100	1MCI	I	An unexpected information phase was requested. MCI defines the SCSI bus phase requested. This interrupt typically occurs when the phase changes before the Transfer Count reaches zero during a Transfer Info command or when an unexpected phase sequence occurs during a Select-and-Transfer command.

SERVICE REQUIRED INTERRUPTS			
STATUS	**CODE**	**STATE**	**SPECIFIC MEANING**
1000	0000	D	The 33C93B has been reselected. The new state of the 33C93B is connected as an initiator.
1000	0001	D	The 33C93B has been reselected in advanced mode. The Identify message from the target must be read from the DATA register. The ACK- signal is asserted. The new state of the 33C93B is connected as an initiator.
1000	0010	D	The 33C93B has been selected (ATN- was not asserted). The new state of the 33C93B is connected as a target.
1000	0011	D	The 33C93B has been selected (ATN- was asserted). The new state of the 33C93B is connected as a target.
1000	0100	T	The ATN- signal has been asserted.
1000	0101	TI	The target has disconnected. The new state of the 33C93B is disconnected.
1000	0110	-	Reserved for future use.
1000	0111	T	The Wait-for-Select-and-Receive command has paused because the first byte of the incoming CDB is not of a known command group. The host can examine the CDB1 register to determine from the opcode the number of command bytes expected. The new state of the 33C93B is connected as a target. (Advanced mode only)
1000	1MCI	I	The REQ signal has been asserted while the 33C93B was in an idle initiator state. The information phase type should be examined. MCI defines the information phase (SCSI bus phase) requested.

30

3.1.21 Command Register

The COMMAND register is used to issue the 33C93B commands. The host should never write to this register when the CIP or INT bits (in AUXILIARY STATUS) are set and should never issue a Level II command when the BSY bit is set.

The SINGLE-BYTE TRANSFER (SBT) bit in the COMMAND register affects the information transfer commands by disabling the TRANSFER COUNT register and specifying that only one byte is to be transferred. The previous contents of the TRANSFER COUNT register are not preserved.

The SBT bit also affects the Wait-for-Select-and-Receive command. Normally, this command does not accept as valid an Identify message with the LUNTAR bit (bit 5) set, which occurs when the initiator wishes to communicate with a target routine. Issuing the command with the SBT bit set allows it to accept an Identify message for a target routine.

Refer to the COMMANDS section for a description of the commands and their corresponding command codes.

7	6	5	4	3	2	1	0
SBT	CC6	CC5	CC4	CC3	CC2	CC1	CC0

3.1.22 Data Register

The DATA register provides an interface between the internal twelve byte FIFO and the host. During any type of information phase, the host may access this register with the processor, and during a SCSI Data phase, the host may also access this register through the DMA/WD interface.

The processor, except in one case, should only access the DATA register when the DBR bit in the AUXILIARY STATUS register is true. The exception occurs when the 33C93B is reselected while operating in advanced mode: the processor must retrieve the Identify message from the target by reading the DATA register.

The FFE bit in the AUXILIARY STATUS register enables the host to avoid polling DBR in some cases. This bit, when the host writes to the FIFO, acts as a FIFO empty indicator; thus, when set, the host can safely write up to eleven bytes to the FIFO without polling for DBR between each write. Similarly, when the transfer direction is to the host, the FFE bit indicates the FIFO full condition, and the processor can safely read twelve bytes from the FIFO without checking for DBR before each read. In both cases, the host should consider the FFE bit valid only when DBR is set.

Two exceptions do exist, however, both when writing to the DATA register. First, after the initial setting of the FFE and DBR bits in response to a Transfer Info or Send command, the host may write twelve bytes to the FIFO without causing a FIFO overrun. Second, because the 33C93B splits a Transfer Info command into two separate transfers when responding to a message out phase, the host must not write the last message byte to the DATA register until the 33C93B specifically requests that byte. For instance, if the host wishes to send a (five-byte) Synchronous Data Transfer Request message, the first set of writes should contain only the first four bytes of the message. The host must then poll for DBR before writing the final byte.

The processor normally should not access the DATA register during a Data phase unless the host has selected polled I/O mode by setting all of the DMA MODE SELECT bits in the CONTROL register to zero. In exceptional cases, such as aborting a transfer, the host may wish to switch to polled I/O accesses. In this case, the processor may access the DATA register but must guarantee that the DMA interface is inactive, i.e. DACK- inactive in the DMA and Burst DMA modes and RCS- deasserted in WD Bus mode.

3.1.23 Queue Tag Register

The QUEUE TAG register holds the second byte of the Tag messages associated with the Select-and-Transfer, Reselect-and-Transfer, and Wait-for-Select-and-Receive commands.

The Select-and-Transfer and Reselect-and-Transfer commands send the contents of this register as the second byte of the Tag message during the Tag message out phase.

The Select-and-Transfer and Wait-for-Select-and-Receive commands place the received queue tag byte into this register during the Tag message in phase. The Select-and-Transfer commands, furthermore, compare the received byte with the previous contents of the register and generate an interrupt in the case of a mismatch.

3.2 RESET CONDITIONS

3.2.1 Hardware Reset

A hard reset, caused by assertion of the MR- signal, will result in the following conditions:

- The AUXILIARY STATUS register is reset to zero. The INT bit (and the INTRQ pin) is set to one when the hardware reset completes.
- The OWN ID register is reset to zero.
- Advanced mode is disabled.
- The ES, ER, and DSP bits in the SOURCE ID register are reset to zero.
- The SCSI STATUS register is reset to zero.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The internal clock divider circuit is set to divide by two.

The hard reset does NOT affect the following host accessible registers:

- Registers 01 hex through 15 hex;
- SOURCE ID (16 hex) register bits 0-3;
- COMMAND register (18 hex);

NOTE: The SCSI Soft Reset may be implemented by using the SCSI bus reset signal to reset the 33C93B (for example, OR the host power on reset signal with the received SCSI bus reset (RST-) signal). The host may examine the registers that are not affected by the MR- signal to recover from the SCSI reset condition.

3.2.2 Software Reset

A soft reset, caused by executing the Reset command, will result in the following conditions:

- The DBR bit in the AUXILIARY STATUS register is reset to zero. The INT bit (and INTRQ pin) is set to one when the Reset command is complete.
- All SCSI bus signals are reset to the negated state.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The OWN ID register is interpreted and the clock divisor, host parity, and operating mode are configured.
- Registers 01 hex through 16 hex are reset to zero. The COMMAND register (18 hex) is also reset to zero.
- The SCSI STATUS register is set as commanded by the EAF bit in the OWN ID register.

4.0 COMMANDS

4.1 COMMAND LIST

COMMAND CODE (HEX)	COMMAND	VALID	LEVEL
00	Reset	D, T, I	I
01	Abort	D, T	I
02	Assert ATN	I	I
03	Negate ACK	I	I
04	Disconnect	T, I	I
05	Reselect	D	II
06	Select-with-ATN	D	II
07	Select-without-ATN	D	II
08	Select-with-ATN-and-Transfer	D I	II
09	Select-without-ATN-and-Transfer	D I	II
0A	Reselect-and-Receive-Data	D, T	II
0B	Reselect-and-Send-Data	D, T	II
0C	Wait-for-Select-and-Receive	D, T	II
0D	Sedn-Status-and-Command-Complete	T	II
0E	Send-Disconnect-Message	T	II
0F	Set IDI	D, T, I	I
10	Receive Command	T	II
11	Receive Data	T	II
12	Receive Message Out	T	II
13	Receive Unspecified Info Out	T	II
14	Send Status	T	II
15	Send Data	T	II
16	Send Message In	T	II
17	Send Unspecified Info In	T	II
18	Translate Address	D, T	II
20	Transfer Info	I	II

33C93B States:
D = Disconnected
T = Connected as a target
I = Connected as an initiator

Command Levels:
I = Level I command
II = Level II command

4.2 33C93B COMMAND TYPES

The 33C93B command set consists of two types of commands: Level I and Level II commands. Level I commands, except for the Reset and Abort commands, do not generate interrupts upon their completion; Level II commands always terminate with an interrupt. The host may issue a Level I command while a Level II command is executing. Issuing a Level II command while another Level II command is executing will cause unpredictable behavior of the part.

The 33C93B operates in one of three "states" at any one time: disconnected, connected as a target, or connected as an initiator. In each state, the 33C93B recognizes only certain commands as valid, as indicated in the command list above. An attempt to issue a Level II command invalid for the present 33C93B state will cause an "invalid command" interrupt. Level I commands issued in invalid states will be ignored.

There are two types of Level II commands. 'Simple' Level II commands perform a single operation (e.g. selection) or single phase (e.g. Command phase). 'Combination' Level II commands combine multiple phases into a single 33C93B command to minimize interrupt overhead.

The initiator combination commands expect the target to follow common SCSI bus phase sequences. Any deviation causes an interrupt.

The EDI and IDI bits in the CONTROL register and the SCC bit in the DESTINATION ID register enable and control chaining of target combinations command. Linking commands further decreases interrupt overhead by creating longer phase sequences. When using command chaining, the host must initialize all commands in the chain prior to starting the sequence.

4.3 33C93B SPECIFIC FEATURES

The 33C93B incorporates two sets of features, both of which cause it to be incompatible with the original 33C93 design and one which causes it to be incompatible with the 33C93A device. Both the 33C93A and 33C93B implement the 'advanced mode' features. Both devices, moreover, implement two features included in the 'really advanced' set of functions; however, in this mode, the 33C93B also generates additional interrupts, described below, making it incompatible with the 33C93A.

Upon completion of a hardware reset, both sets of features are disabled. The host enables them by soft resetting the 33C93B with the EAF and RAF bits in the OWN ID register set appropriately. An advanced mode reset results in a 01 hex being loaded into the SCSI STATUS register instead of the 00 hex which normally results from a reset. This difference gives the host a method to deduce that a 33C93B is installed as opposed to a 33C93.

4.3.1 Advanced Mode Features

UNEXPECTED RESELECTION: When in normal (33C93) mode, a reselection when idle (ER=1) or a reselection during a Select-and-Transfer command by an target whose ID does not match the one in the DESTINATION ID register causes an interrupt immediately after the reselection handshake finishes. In advanced mode, the 33C93B will continue to the Message In phase to fetch the Identify message. If the 33C93B was idle, the SCSI STATUS register will be set to 81 hex, and the Identify message will be in the DATA register. If the 33C93B was executing a Select-and-Transfer command, the SCSI STATUS register will be set to 27 hex, and the logical unit number will be in the TARGET LUN register. In both cases, the SOURCE ID register will contain the SCSI bus ID of the reselecting target, and the ACK signal remains asserted so that the Identify message may be rejected if desired.

Any message other than a valid Identify message will result in an unexpected message in phase interrupt. If the unexpected reselection occurs during a Select-and-Transfer command, a parity error will cause an unexpected message in phase interrupt only if the halt-on-SCSI-parity-error feature is enabled. If reselected from an idle state, the 33C93B will halt on a parity error regardless of the setting of the HSP bit. The host can retrieve the byte with the Transfer Info command.

UNKNOWN SCSI COMMAND GROUPS: The length of a SCSI Command Descriptor Block is determined by the group code, found in bits 7-5 of the first command byte. The SCSI standard (X3.131-1986) defines Group 0 (opcodes 00 to 1F hex), group 1 (opcodes 20 to 3F hex), and group 5 (opcodes A0 to BF hex) commands respectively as six, ten, and twelve byte commands. All other

command groups are undefined by that standard. In normal mode, the 33C93B assumes a length of six bytes for these undefined groups when executing a Select-and-Transfer or Wait-for-Select-and-Receive command. In advanced mode, the 33C93B behaves as follows:

- Select-and-Transfer: When sending a command from an unknown group, the host must load the expected command length into the CDB SIZE register before issuing the Select-and-Transfer. The 33C93B uses this value to make sure the correct number of bytes are transferred in the Command phase.
- Wait-for-Select-and-Receive: When receiving the CDB from the initiator, the 33C93B examines the first CDB byte to determine the command group. An undefined group results in an interrupt with the SCSI STATUS register set to 87 hex and the COMMAND PHASE register set to 31 hex. The host may examine the byte, available in the CDB 1ST register, to determine the TOTAL command length, which it then places into the CDB SIZE register, before resuming the Wait-for-Select-and-Receive command.

  After this interrupt, the 33C93B will only accept a Resume Wait-for-Select-and-Receive, Abort, Disconnect, or Reset command. All other commands are invalid. While the host processes the interrupt, the 33C93B continues to transfer the first six bytes of the SCSI command into its internal FIFO.

DATA PHASE DIRECTION: Normally during a Select-and-Transfer command, the target solely determines the direction of the Data phase. The 33C93B will not detect a mismatch between this direction and the one expected by the host and will proceed with the transfer. In advanced mode, the 33C93B compares the DPD bit in the DESTINATION ID register with the state of the I/O- signal on the SCSI bus. If the expected and actual directions do not match, an interrupt will occur with an 'unexpected phase' status in the SCSI STATUS register. Setting the DF bit in the DESTINATION ID register disables this feature.

4.3.2 Really Advanced Features

MICROCODE REVISION: The 33C93B will load the revision number of the microcode into the CDB1 register during the reset sequence when really advanced features are enabled.

IMMEDIATE HALT: The 33C93B normally checks for parity errors during a synchronous transfer and for the attention condition during both asynchronous and synchronous transfer on 4096-byte boundaries. With really advanced features enabled, the 33C93B continuously checks for these conditions and upon detecting one issues an Abort command.

PROTOCOL ERROR: The 33C93B, if it detects a possible transfer corruption caused by noise on the REQ- and ACK- signals, will abort a Send or Receive command and generate a 25 hex interrupt. The detection scheme can not catch all possible failures due to the nature of the SCSI transfer protocols; however, this feature does provide some protection against data integrity faults.

UNEXPECTED BUS FREE INTERRUPTS: The 33C93B will generate either an 85 hex interrupt or a 41 hex interrupt in the event that a glitch on the SEL- signal causes the device to disconnect from the SCSI bus.

4.4 LEVEL I COMMANDS

4.4.1 Reset (00 hex)

The Reset command initializes the 33C93B according to the contents of the OWN ID register and as described in the RESET CONDITIONS section. The host may issue the Reset command while in any state, forcing the 33C93B into a disconnected state; any command executing at that time will terminate. Upon completion of the Reset command, the 33C93B will generate an interrupt with the SCSI STATUS register containing a 00 hex or a 01 hex depending upon the contents of the OWN ID register at the time of the reset.

4.4.2 Abort (01 hex)

The Abort command is valid in the disconnected and connected-as-a-target states. The Abort command has different effects depending on the current state and the command that is currently executing, as described below:

- Disconnected State: In this state, the Abort command will halt a selection or reselection attempt of a Select, Select-and-Transfer, Reselect, or Reselect-and-Transfer command or will halt the Wait-for-Select-and-Receive command before selection. Aborting a selection or reselection attempt before the 33C93B has won arbitration immediately returns the 33C93B to an idle state and generates a "paused/aborted" interrupt. If the 33C93B has already won arbitration, the Abort command causes the 33C93B to remove the Bus ID bits from the SCSI bus while maintaining assertion of SEL-. If the target does not respond within at least 200 us by asserting BSY-, the 33C93B will go to a Bus Free condition and generate a "paused/aborted" interrupt. If the target does respond within this time period, a "successful completion" interrupt will result instead.

  The Abort command, in addition, will terminate a Select- and-Transfer command if the target has disconnected from the bus. The 33C93B will generate an 85 hex interrupt and will be in the Disconnected state. If the target is still connected at the time the Abort command is recognized, the command will be ignored.

- Target State: In this state, the Abort command will terminate a Receive or Send command or the Data phase portion of a Reselect-and-Transfer command. The following rules apply when issuing an Abort:

  - During a Send or Reselect-and-Send command, the 33C93B removes the data request (DRQ-, DBR, etc.) at an arbitrary time during the abort procedure. The host must NOT service any data request once it has written the Abort command to the COMMAND register until the 33C93B generates an interrupt. Abort processing will not complete until the contents of the FIFO are flushed to the SCSI bus.
  - During a Receive or Reselect-and-Receive command, the host must CONTINUE to service any data request from the 33C93B. Abort processing will not complete until the contents of the FIFO are flushed to the host.

  After completion of the Abort command, the TRANSFER COUNT register contains the number of bytes that were not transferred across the SCSI bus. The 33C93B remains in the connected-as-a-target state and will accept any target mode command, including a resume of the aborted command.

4.4.3 Disconnect (04 hex)

The Disconnect command, valid in the initiator and target states, immediately terminates an active Level II command, causes the immediate release of all bus signals, and returns the 33C93B to a disconnected state. In the target role, the Disconnect command is the normal procedure for disconnecting from the SCSI bus following the information transfer phase. In the initiator role, this command can be used to release the bus following a timeout condition.

30

4.4.4 Assert ATN (02 hex)

The Assert ATN command, valid only when connected as an initiator, allows the initiator to inform the target that it has a message pending. The target should respond with a Message Out Phase. ATN- is automatically negated:

- before the last byte of a Transfer Info command issued in response to the Message Out phase;
- when the Identify message out is transferred to the target during a Select-and-Transfer command;
- when a SCSI Bus Free phase occurs.

The Select-with-ATN and Select-with-ATN-and-Transfer commands will cause the 33C93B to assert ATN- automatically prior to the release of SEL-.

4.4.5 Negate ACK (03 hex)

The Negate ACK command causes the 33C93B to release ACK- which for some reason it has held active. Holding ACK- active allows the host to respond to information it has just received before the target continues the current phase or proceeds to the next one. The 33C93B, therefore, does not

negate ACK- before generating an interrupt in the following cases:

- after successful completion of a Message-In Transfer Info command;
- after detection of a parity error on any received SCSI information when the HALT on SCSI PARITY ERROR (HSP) bit is set;
- after unexpected reselection in advanced mode;
- after reception of a save-data-pointer message during a Select-and-Transfer command;
- after reselection by a process with a queue tag which differs from the contents of the QUEUE TAG register; and
- after reception of a status byte with a parity error during a Select-and-Transfer command.

ACK- negates automatically for all initiator transfers other than Message In transfers. Host parity errors, moreover, do not affect the ACK- signal.

Before completing a Message In phase, the initiator, upon examining the message, may decide to reject it and send a "MESSAGE REJECT" message to the target or, upon detecting a parity error in the message, may decide to send a "MESSAGE PARITY ERROR" message to the target. Similarly, if a parity error causes a transfer command to terminate, the initiator may wish to send an "INITIATOR DETECTED ERROR" message to the target. In all cases, the initiator signals its intent to send a message by asserting ATN before issuing the Negate ACK command.

4.4.6 Set IDI (0F hex)

The Set IDI command provides support for overlapped SCSI operations in the initiator role. The host may start a SCSI operation with the IDI bit reset, allowing the 33C93B to handle target disconnects and reconnects and thus minimizing the interrupt handling overhead. When it wishes to start a second operation, the host issues the Set IDI command so that if the current target disconnects and releases the SCSI bus, the 33C93B will produce an interrupt. The host may now start the second operation without having had to wait for the first operation to complete.

4.5 SIMPLE LEVEL II COMMANDS

4.5.1 Select-with-ATN (06 hex)

Select-with-ATN, valid only in the disconnected state, instructs the 33C93B to select a target. Before issuing this command, the host should write the SCSI Bus ID of the target device into the DESTINATION ID register. The Select-with-ATN command causes the 33C93B to begin bus arbitration. If another device selects or reselects the 33C93B during arbitration, the Select-with-ATN command aborts and a "service required" interrupt (8x hex) will occur.

Should the 33C93B win the arbitration, it asserts SEL- and ATN-, places the target and initiator Bus IDs on the SCSI data bus, and then deasserts BSY-. At this time, a timeout sequence begins, its length determined by the value in the TIMEOUT PERIOD register. If the target does not respond with BSY- within the allotted time, the 33C93B begins a selection abort sequence as described in the Abort command description. If the target has not responded by the end of this sequence, the Select-with-ATN command terminates. If the target responds before the timeout period has elapsed or before the selection abort sequence completes, the 33C93B negates the SEL- signal, enters the connected-as-an-initiator state, and generates a "successful completion" interrupt.

A successful abort of Select-with-ATN, either through a timeout or through the Abort command, leaves the 33C93B disconnected from the SCSI bus and results in a "paused/aborted" interrupt.

4.5.2 Select-without-ATN (07 hex)

The Select-without-ATN command is identical to the Select-with- ATN command except that ATN- is not set during the Selection Phase.

4.5.3 Reselect (05 hex)

The Reselect command is identical to the Select-without-ATN command except that the I/O- signal is asserted upon completion of the Arbitration Phase. Successful completion of the Reselect command results in the 33C93B being connected as a target.

4.5.4 Receive (10-13 hex)

The four Receive commands---Receive Command, Receive Data, Receive Message Out, and Receive Unspecified Info Out---differ from each other only by the state of the C/D- and MSG- pins and the type of data that is transferred. These commands, valid only in the target role, correspond to those SCSI information phases where the I/O- pins is not asserted; the type of the Receive command selected determines the state of the C/D- and MSG- outputs according to the following chart (1=asserted):

RECEIVE	COMMAND TYPE	OP-CODE	MSG	C/D	I/O
Receive	Command	10	0	1	0
Receive	Data	11	0	0	0
Receive	Message Out	12	1	1	0
Receive	Unspecified Info Out	13	1	0	0

A Receive command will complete or terminate under any of the following conditions:

- The host has read the specified number of bytes from the DATA register;
- The 33C93B detects a parity error on one of the received data bytes when Halt-on-SCSI-Parity is enabled;
- The 33C93B detects ATN- when Halt-on-ATN is enabled;
- The 33C93B detects a transfer protocol error;
- The host aborts the Receive command;
- The host issues a Disconnect command; or
- The 33C93B resets because of a Reset command or assertion of MR-.

Any conclusion of a Receive command, except those due to a Disconnect command or a Reset, leaves the 33C93B in a connected-as-a-target state and the number of bytes not yet transferred in the TRANSFER COUNT register.

In the case of a Receive Data command, the 33C93B evaluates the contents of the SYNCHRONOUS TRANSFER register. Any offset other than zero selects synchronous transfers. The minimum transfer period applies to both synchronous and asynchronous transfers. The 33C93B also examines the CONTROL register to determine what mode of data transfer will occur on the host interface.

In all other cases, asynchronous transfers occur on the SCSI bus, and polled I/O transfers occur on the host interface.

4.5.5 Send (14-17 hex)

The four Send commands---Send Status, Send Data, Send Message, and Send Unspecified Info---like the four Receive commands, differ from each other only by the state of the C/D- and MSG- pins and the type of data that is transferred. These commands, valid only in the connected-as-a-target state, correspond to those SCSI phases where the I/O- pin is asserted; the type of Send command selected determines the state of the C/D- and MSG- outputs according to the following chart (1=asserted):

30

SEND	COMMAND TYPE	OP-CODE	MSG	C/D	I/O
Send	Status	14	0	1	1
Send	Data	15	0	0	1
Send	Message In	16	1	1	1
Send	Unspecified Info Out	17	1	0	1

A Send command will complete or terminate under any of the following conditions:

- The initiator has acknowledged receipt of the specified number of bytes;
- The 33C93B detects a parity error on one of the received data bytes when Halt-on-Host-Parity is enabled;
- The 33C93B detects ATN- when Halt-on-ATN is enabled;
- The 33C93B detects a transfer protocol error;
- The host aborts the Receive command;
- The host issues a Disconnect command; or
- The 33C93B resets because of a Reset command or assertion of MR-.

Any conclusion of a Send command, except those due to a Disconnect command or a Reset, leaves the 33C93B in a connected- as-a-target state and the number of bytes not yet transferred in the TRANSFER COUNT register.

In the case of the Send Data command, the 33C93B evaluates the contents of the SYNCHRONOUS TRANSFER register. Any offset other than zero selects synchronous transfers. The minimum transfer period applies to both synchronous and asynchronous transfers. The 33C93B also examines the CONTROL register to determine what mode of data transfer will occur on the host interface.

In all other cases, asynchronous transfers occur on the SCSI bus, and polled I/O transfers occur on the host interface.

4.5.6 Transfer Info (20 hex)

The Transfer Info command allows the host to send and receive data, command, status, and message information when operating in the connected-as-an-initiator state.

The first REQ- assertion following connection as an initiator results in a "service required" interrupt. The processor should examine the SCSI STATUS register to determine the type and direction of information transfer requested by the target, and then issue a Transfer Info command in response. The 33C93B will also generate an interrupt each time the target device requests a new type of information transfer phase.

The processor either should initialize the TRANSFER COUNT register prior to issuing this command or issue the command with the SBT bit in the COMMAND register set. Also, if responding to a request for a Data phase, the processor should set the DMA mode select bits in the CONTROL register and specify the offset and transfer period in the SYNCHRONOUS TRANSFER register before issuing the Transfer Info command.

Behavior of the DBR status bit during Transfer Info depends upon the direction of the transfer. When the bytes move from the initiator to the target, i.e. an out phase, the DBR bit is set whenever the FIFO can accept additional data from the host. When the transfer proceeds in the opposite direction, DBR set indicates that the FIFO contains data available for the host to read.

The Transfer Info command normally terminates or pauses after the specified number of bytes has been sent or received. For a non- Message-In transfer, the 33C93B will generate a "successful completion" interrupt after the target asserts REQ- to begin a new phase. For a message-in transfer, the 33C93B does not wait for the next phase but instead leaves ACK- asserted and generates a "paused/aborted" interrupt. The processor can then assert ATN- if it intends to reject the message before negating ACK-.

The Transfer Info command may terminate for a number of different reasons which are listed below:

- The host issues a Disconnect command;
- The 33C93B resets in response to the assertion of MR- or the Reset command;
- The target negates the BSY- signal;
- The target unexpectedly changes phase, i.e. before the specified number of bytes have been transferred; or
- The incoming data has a parity error and the corresponding halt-on-parity-error bit is set.

The Disconnect command, the hard and soft resets, and the negation of BSY- will leave the 33C93B in a idle, disconnected state, and in these cases, the value in the TRANSFER COUNT register will not accurately reflect the number of bytes that did not transfer across the SCSI interface. Except for the issuance of the Disconnect command, these occurrences will result in an interrupt.

The 33C93B checks for a parity error on each byte it receives; however, for synchronous transfers, the internal microcontroller will not recognize an error until the transfer reaches a 4096- byte boundary. The response to the parity error, furthermore, depends upon the direction of the transfer. If the parity error occurs on received SCSI data, the 33C93B will halt the SCSI interface, leaving ACK- asserted to halt the target, and generate a "terminated" interrupt once the host has flushed any remaining bytes from the FIFO. Similarly, if the error occurs on data received on the host interface, the 33C93B will halt the host interface and generate a "terminated" interrupt after any bytes remaining in the FIFO are flushed to the SCSI bus; the ACK-

signal, however, will not remain asserted. In both cases, the TRANSFER COUNT register will indicate the number of bytes that did not successfully transfer to or from the target.

If it detects a parity error but the appropriate halt-on-parity- error bit is not set, the 33C93B will indicate the error by setting the PARITY ERROR bit in the AUXILIARY STATUS register but will not terminate the Transfer Info command.

An unexpected phase change will cause a "terminated" interrupt, and as in the case of a parity error, the TRANSFER COUNT register contains the number of bytes yet to be transferred. If an unexpected phase change occurs during a SCSI synchronous transfer, the host should test the PARITY ERROR bit in the AUXILIARY STATUS register, as the phase change most likely occurred before the internal microcontroller recognized the parity error. In the asynchronous case, the 33C93B stops on the byte with the error; therefore, it will always detect a parity error before a phase change in this mode.

4.5.7 Translate Address (18 hex)

The Translate Address Command performs a logical-address to physical-address translation to facilitate processing of certain SCSI commands involving logical addresses up to 32 bits in length. To perform this mapping, the processor first loads the logical address into the LOGICAL ADDRESS register, the disk parameters into the TOTAL CYLINDER NUMBER, TOTAL HEAD NUMBER, and TOTAL SECTOR NUMBER registers, and zeros into the HEAD NUMBER and CYLINDER NUMBER registers. It then issues the Translate Address command, and upon receiving a "successful completion" interrupt, reads the CYLINDER NUMBER, HEAD NUMBER, and SECTOR NUMBER registers to obtain the logical address.

The Translate Address command can also compensate for spare sectors. To use this feature, the host, instead of zeroing the HEAD NUMBER and CYLINDER NUMBER registers, should load the number of spare sectors per cylinder into the HEAD NUMBER register and the logical number of sectors per cylinder into the CYLINDER NUMBER register prior to issuing the command.

An overflow during any calculation will result in a "terminated" interrupt.

4.6 COMBINATION LEVEL II COMMANDS

4.6.1 Select-and-Transfer (08 and 09 hex)

The Select-and-Transfer commands greatly reduce the host or local processor interrupt-handling burden by enabling the 33C93B's internal microprocessor to manage the low-level SCSI protocol. Use of these command may result in as few as one interrupt per SCSI operation. Select-and-Transfer commands, used when in an initiator role, typically consist of at least the following SCSI phases: an Arbitration phase, a Selection phase, a Command phase, a Status phase, and a Command-Complete Message phase. These commands optionally include Data and additional Message In phases.

30

The Select-and-Transfer commands expect the target to follow a certain sequence of SCSI bus phases, and any deviation from this expected protocol results in a "terminated" interrupt. As the different phases complete, the 33C93B updates the COMMAND PHASE register, so upon termination of the command, the host processor may examine this register to identify the cause of the termination and the state of the SCSI operation.

The two Select-and-Transfer commands differ from each other only by whether or not the 33C93B asserts ATN- pin during the Selection phase. The ability to assert ATN- during Selection supports the SCSI message protocol which calls for an Identify Message Out phase following the selection. When executing a Select-with-ATN-and-Transfer command, the 33C93B expects the target to request a Message Out phase immediately following selection, whereas for a Select-without-ATN-and-Transfer command, it expects the target to begin the Command phase once selection completes.

The 33C93B begins the Select-and-Transfer command by arbitrating for the bus and selecting a target just as during a Select command. If the target does not respond before a timeout occurs, the Select-and-Transfer command halts and generates an interrupt. Failure to complete the Selection phase is also indicated by the fact that the COMMAND PHASE register contains all zeros. If

the selection is successful, no interrupt is generated, and the COMMAND PHASE register will be set to a 10 hex.

After completing the Selection phase, the 33C93B begins a Message Out phase if ATN- has been asserted or a Command phase if not. When the target requests a Message Out phase, the 33C93B responds by automatically sending an Identify message byte, which it generates by exclusive-ORing the contents of the TARGET LUN register with 80 hex if the ENABLE RESELECTION bit in the SOURCE ID register is reset or with C0 hex if the bit is set. After it has sent the Identify message, the 33C93B will set the COMMAND PHASE register to 20 hex.

Normally, bit 6 of the Identify message mirrors the state of the ENABLE RESELECTION bit; however, the host may occasionally wish to allow the 33C93B to respond to a reselection attempt but not enable target disconnects during another SCSI operation. Setting both the ENABLE RESELECTION bit and the DOK bit of the TARGET LUN register allows the 33C93B to respond to reselection but results in an Identify message byte which does not enable target disconnects.

Following the Identify message out, if bits 3 or 4 of the DESTINATION ID register specify a tag message and if ATN- is asserted, the 33C93B expects the target to request the first byte of a tag message. It responds to this request by sending the selected tag message code and incrementing the COMMAND PHASE register. The 33C93B now expects the target to ask for the second byte and services this request by sending the contents of the QUEUE TAG register and incrementing the COMMAND PHASE register to 22 hex.

The 33C93B expects a Command phase to follow the Message Out phase or, if ATN- is not asserted during selection, the Selection phase. The 33C93B obtains the SCSI command from the internal COMMAND DESCRIPTOR BLOCK registers and sends either six, ten, or twelve bytes of command information depending on the first byte of the SCSI command. The Select-and-Transfer commands support Group 0 (6-byte CDB), Group 1 (10-byte CDB), and Group 5 (12-byte CDB) SCSI commands. The length of any other command defaults to six bytes unless advanced mode is enabled (see 7.3.1). The COMMAND PHASE register, set to 30 hex before the first Command byte is sent, increments with each byte transferred, so for a twelve-byte CDB command, the COMMAND PHASE register will contain 3C hex when all bytes of the CDB have been transferred.

After the Command phase, the 33C93B anticipates a Data phase if the TRANSFER COUNT register contains a non-zero value, a Status phase if this register contains zero, or, in either case, a Message In phase if the ENABLE RESELECTION bit is set and the DOK bit is not. The 33C93B assumes a pending disconnection if the target requests a Message In phase. Thus, when enabled, the 33C93B expects to receive either a Save-Data-Pointer message (02 hex) or a Disconnect message (04 hex). If a message byte has a parity error and the HSP bit is set or if the target sends an unsupported message, the 33C93B will generate a "terminated" interrupt, alerting the processor of this fact and allowing it to retrieve the message byte via the Transfer Info command.

Reception of a correct Save-Data-Pointer message results in a "paused/aborted" interrupt, terminating the Select-and-Transfer command with the COMMAND PHASE register set to 41 hex. The processor can then save the SCSI data pointer before resuming the Select-and-Transfer command.

A Disconnect message, on the other hand, will not cause an interrupt; instead, command execution continues with the COMMAND PHASE register set to 42 hex and with Bus Free as the next expected phase. The 33C93B updates the COMMAND PHASE register to 43 hex when the target actually disconnects and, if the IDI bit is set, suspends the Select-and-Transfer command with an 85 hex interrupt. If, however, the IDI bit is reset, the 33C93B sits in an idle state, waiting for the target to reconnect. Reselection by the original target generates no interrupt and increments the COMMAND PHASE register to 44 hex; reselection by a different target will cause a "terminated" interrupt. In advanced mode, this interrupt will not occur until the 33C93B has also received the Identify message from the target and placed the logical unit number in the target LUN register.

Following the original target reselection, the 33C93B expects an Identify Message In phase from the target. This single-byte message should be of the binary form: 10r00ttt, where r and ttt

match the corresponding bits in the TARGET LUN register. Successful completion of this phase results in the COMMAND PHASE register being updated to 45 hex or 70 hex depending upon whether or not the 33C93B expects a tag message, deduced from the settings of the TG0 and TG1 bits of the DESTINATION ID register.

The target, in the latter case, should send a Simple Queue tag message immediately after the Identify message. Upon receiving and validating the message byte, the 33C93B increments the COMMAND PHASE register and awaits the second message byte from the target. When it receives this byte, the 33C93B sets the COMMAND PHASE to 45 hex and then compares the byte to the contents of the QUEUE TAG register. If the two values match, command execution proceeds; if the two values differ, the 33C93B stores the received byte in the QUEUE TAG register, generates a "Different Process Reselected" interrupt (26 hex) and terminates the Select-and-Transfer command.

The 33C93B anticipates a data phase immediately after the Command phase or after successfully receiving the proper messages after reselection. To handle the Data phase, the Select-and-Transfer command effectively performs a Transfer Info command. The contents of the TRANSFER COUNT register determines the number of bytes to transfer; the value in the SYNCHRONOUS TRANSFER register specifies the type and minimum period of the transfers on the SCSI interface; and the DMA mode select bits in the CONTROL register specify the protocol to follow on the host interface.

Any number of disconnection/reconnection cycles may occur during the data transfer so long as the target follows the defined message protocol. The COMMAND PHASE register will cycle through the disconnect phases (41-45,70,71) with each disconnection and subsequent reconnection until all of the data has been transferred, at which point it is set to 46 hex. During the data transfer, a disconnection will cause an interrupt regardless of the setting of the IDI bit to allow the host to reinitialize the external DMA controller.

The start of the Status phase, assuming the transfer count has reached zero, advances the COMMAND PHASE register to 47 hex. If the status byte has no parity error or if the HSP bit is not set, the internal microcontroller places the byte in the TARGET LUN register and updates the COMMAND PHASE register to 50 hex. If the byte contains an error, a 27 hex interrupt will occur, and the command will terminate with ACK- asserted.

The 33C93B expects the target to send a Command-Complete message (00 hex) to indicate that the SCSI operation has completed. Upon receiving this message, the 33C93B sets the COMMAND PHASE register to 60 hex, and if the EDI bit is reset, generates "successful completion" interrupt. The processor should then read the TARGET LUN register to examine the target status. Another interrupt will occur when the SCSI bus goes to the Bus Free state or when the target again asserts REQ- to begin a new information transfer phase (as in SCSI linked commands). Setting the EDI bit suppresses the "successful completion" interrupt until the target disconnects from the SCSI bus.

The following table summarizes the possible values that the COMMAND PHASE register can assume during the Select-and-Transfer commands and their meanings relative to command termination:

COMMAND PHASE	MEANING
00	No SCSI bus device has been selected. The 33C93B is in the disconnected state.
10	The target has been selected. The 33C93B is now in the connected-as-an-initiator state.
20	An Identify message has been sent to the target.
21	The Tag message code has been sent to the target.
22	The Queue tag has been sent to the target.
30	Command phase has started, no bytes transferred.
3X	Command phase, x bytes have been transferred.
41	Save-Data-Pointer message received.
42	Disconnect message received, bus not free.
43	Target has disconnected (SCSI Bus Free) following a successful transfer of a Disconnect message. The 33C93B is now in the disconnected state.
44	The 33C93B has been reselected by the target with a SCSI bus ID which matches the value in the DESTINATION ID register. The 33C93B is now in the connected as an initiator state.
45	The 33C93B has received an matching Identify message and, if expected, a matching Tag message from the target.
46	The number of bytes specified in the TRANSFER COUNT register have been transferred to or from the target during the Data phase.
47	The target has begun a Receive Status phase.
50	The 33C93B has successfully received a Status byte from the target and stored it in the TARGET LUN register.
60	The 33C93B has successfully received a Command-Complete message from the target.
70	The 33C93B has received an Identify message from the target, and the Logical Unit Number matches the value in the TARGET LUN register. A tag message is expected.
71	The 33C93B has received a Simple-Queue Tag message.

The host processor may resume a Select-and-Transfer sequence by issuing the command when the 33C93B is in the Connect-as-an- initiator state. When resuming the Select-and-Transfer, the 33C93B examines the COMMAND PHASE register to determine where to restart execution of the command. This feature, in conjunction with the INTERMEDIATE DISCONNECT INTERRUPT enabled, supports multi-threaded or overlapped I/O on the SCSI bus.

The following table briefly describes the valid settings of the COMMAND PHASE register when resuming a Select-and-Transfer command:

COMMAND PHASE	MEANING
10	Resume after target selection is complete.
20	Resume after Identify message out. Command or message phases are expected; an implied Negate ACK occurs.
22	Resume after Tag message out. Command phase is expected; an implied Negate ACK occcurs.
30	Resume when Command phase has begun (REQ- asserted).
41	Resume after Command phase or after a Save-Data-Pointer message. Data, Status, or Message In phases are expected. An implied Negate ACK occurs.
42	Resume to complete Disconnect Message In; an implied Negate ACK occurs.
44	Resume after reselection by a target. An Identify Message In expected.
45	Resume to transfer more data in a data transfer phase. May expect Status or Message In as well. An implied Negate ACK occurs.
46	Resume after the Data phase has completed, expecting Status phase or a Save-Data-Pointer/Disconnect Message In phase. An implied Negate ACK does NOT occur.
50	Resume to complete a Status phase; an implied Negate ACK occurs.
60	Resume to complete a Command Complete message from the target; an implied Negate ACK occurs.
70	Resume to receive a Simple-Queue Tag message. An implied Negate ACK occurs.

4.6.2 Reselect-and-Transfer (0A and 0B hex)

The Reselect-and-Transfer commands consist of the Reselect-and- Receive-Data and the Reselect-and-Send-Data commands. These commands cause the 33C93B to execute certain common SCSI bus phase sequences as a target following a Reselection phase. These phases, determined by which command is sent and the setting of the EDI bit in the CONTROL register and the SCC bit in the DESTINATION ID register, are summarized below. Refer to the descriptions of the Send-Status-and-Command-Complete and Send- Disconnect-Message commands for details on those sequences.

- Reselect-and-Receive command, EDI=0, and SCC=don't care:
  - Reselection phase;
  - Send Message In;
  - Receive Data Out phase;
  - Completion interrupt.
- Reselect-and-Send command, EDI=0, and SCC=don't care:
  - Reselection phase;
  - Send Message In;
  - Send Data In phase;
  - Completion interrupt.
- Reselect-and-Receive command, EDI=1, and SCC=0:
  - Reselection phase;
  - Send Message In;
  - Receive Data Out phase;
  - Chain to Send-Status-and-Command-Complete
- Reselect-and-Send command, EDI=1, and SCC=0:
  - Reselection phase;
  - Send Message In;
  - Send Data In phase;
  - Chain to Send-Status-and-Command-Complete;

- Reselect-and-Receive command, EDI=1, and SCC=1:
  - Reselection phase;
  - Send Message In;
  - Receive Data Out phase;
  - Chain to Send-Disconnect-Message;
- Reselect-and-Send command, EDI=1, and SCC=1:
  - Reselection phase;
  - Send Message In;
  - Send Data In phase;
  - Chain to Send-Disconnect-Message;

The Message In phase consists of an Identify message and, if bits 3 and 4 in the DESTINATION ID register are not both zero, a Simple-Queue Tag message. The commands send the contents of the QUEUE TAG register as the second byte of the Tag message.

If the reselection attempt times out during a Reselect-and-Transfer command, if ATN- is asserted and HA=1, or if a parity error is detected on a incoming data byte (and HSP=1 or HHP=1, depending on data direction), the command will terminate with the appropriate status. In this case, the COMMAND PHASE register will indicate the last successfully completed phase. If these conditions do not occur and all phases complete normally, the command will end with a "successful completion" interrupt at this point if EDI=0. However, if EDI=1, no interrupt is generated and command chaining occurs (as described above).

The following table summarizes the possible values that the COMMAND PHASE register can assume during the Reselect-and- Transfer commands and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No SCSI bus device has been reselected. The 33C93B is in the disconnected state.
10	The 33C93B has successfully reselected the initiator. The 33C93B is now in the connected as a target state.
20	The Identify message has been successfully sent to the initiator.
46	The requested data transfer has been completed.

The host processor may resume a Reselect-and-Transfer sequence by issuing the command when the 33C93B is operating in the connected-as-a-target state. When resuming, the 33C93B examines the COMMAND PHASE register to determine where to restart the Reselect-and-Transfer command. This feature in conjunction with the capability to chain to other combination commands allows longer SCSI bus sequences to be performed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Reselect-and-Transfer command:

COMMAND PHASE	MEANING
10	Resume after initiator reselection is complete; start with Identify Message Out.
20	Resume after Identify message out; start with data transfer phase. If TRANSFER COUNT is zero, no data transfer phase occurs. In either case, a chain to another combination command can occur if enabled.

4.6.3 Wait-for-Select-and-Receive (0C hex)

The Wait-for-Select-and-Receive causes the 33C93B to idle until it is selected by an initiator, at which time the 33C93B will enter the target mode and automatically request message and command information. Optionally, the 33C93B will then disconnect if it receives a SCSI read command. Use of this command therefore eliminates the interrupts which normally occur after selection and after each subsequent SCSI bus phase and minimizes bus-connect time during SCSI read commands.

If the initiator asserts ATN- during the Selection phase, the 33C93B first executes an implied "Receive Message Out" command to get the Identify message and the Tag message, if any, from theinitiator. The 33C93B stores the Identify message byte in the TARGET LUN register; it encodes the Tag message code into bits 3 and 4 of the DESTINATION ID register and places the queue tag into the QUEUE TAG register. Normally, the Wait-for-Select-and- Receive command rejects an Identify message with the LUNTAR bit (bit 5) set; however, issuing this command with the SBT bit in the COMMAND REGISTER set allows the 33C93B to accept an Identify message for a target routine.

The 33C93B executes an implied "Receive Command" following the Selection phase or Identify Message In phase and stores the SCSI command information in the CDB registers. It determines the number of command bytes to request from the SCSI group code in the first byte of the CDB.

At this point, a "successful completion" interrupt normally will occur to allow the local processor to interpret the SCSI CDB. However, by setting the EDI bit prior to issuing a Wait-for-Select-and-Receive command, the host enables the 33C93B to perform an automatic disconnect when it receives a SCSI read command. Thus, when EDI=1 and the 1st CDB byte received contains a six, ten, or twelve byte read command code, the 33C93B will suppress the interrupt and chain to the Send-Disconnect-Message command. Completion of this sequence causes an interrupt and normally indicates a transition to the bus free condition. Refer to the Send-Disconnect-Message command description for more details.

If the message or command information received from the initiator is invalid, the Wait-for-Select-and-Receive command will be terminated and the appropriate status reported. As usual, the COMMAND PHASE register will indicate which phases of the command completed before the error condition occurred.

The following table summarizes the possible values that the COMMAND PHASE register can assume during the Wait-for-Select-and-Receive command and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	The 33C93B has not been selected. The 33C93B is in the disconnected state.
10	The 33C93B has been successfully selected by the initiator. The 33C93B is now in the connected-as-a- target state.
20	The 33C93B has received a message byte (Identify) from the initiator. The TARGET LUN register holds the byte.
21	The 33C93B has received a message byte (Tag code) from the initiator. The QUEUE TAG register contains the byte.
22	The 33C93B has received a message byte (Queue Tag) from the initiator. The QUEUE TAG register contains the byte.
30	The 33C93B is ready to begin Command phase. The SCSI bus phase lines and REQ- have not been asserted.
31	The 33C93B has transferred one command byte from the initiator. The SCSI STATUS may indicate the need for the host to load the command size into the OWN ID register.
3x	The 33C93B has transferred x command bytes from the initiator.

A "paused/aborted" interrupt in conjunction with command phases 20 and 21 indicate that the respective message byte was not valid. A parity error in the Identify message results in the appropriate interrupt and the COMMAND PHASE register set to 10 hex. This combination allows the host to retry the transfer by merely reissuing the command to resume the operation from the proper phase. A parity error in the other two message bytes results in a command phase of 21 or 22, indicating which byte contained the error.

The host processor may resume the Wait-for-Select-and-Receive command by issuing the command when the 33C93B is operating in the connected-as-a-target state. When resuming this command, the 33C93B examines the COMMAND PHASE register to determine where to restart the Wait-for-Select-and-Receive command. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Wait-for-Select-and-Receive command:

COMMAND PHASE	MEANING
10	Resume after selection by the initiator is complete. Start with Identify Message Out if ATN is asserted; otherwise, start with Command phase.
20	Resume after a Message Out; check the received message in the TARGET LUN register for a valid Identify message.
21	Resume after Identify message verified. Start with Tag Message Out if ATN is asserted; otherwise, start with Command phase.
30	Resume after Identify Message Out. Start with Command phase.
31	Resume after the 33C93B has transferred one command byte from the initiator. This resume point is used only when an unknown group code has been detected in advanced mode and the command size has been loaded into the OWN ID register.

4.6.4 Send-Status-and-Command-Complete (0D hex)

The Send-Status-and-Command-Complete command, valid in the target role, combines the Status and the Command-Complete Message phases used to complete a SCSI operation into one command. This command also supports linked SCSI operations by optionally sending a Linked-Command-Complete message after the transferring the status byte. Bits in the CDB12 register corresponding to the standard linked command control bits in the CDB control the choice of Linked-Command-Complete messages.

Before issuing this command, the host loads the status byte into the CDB11 register and the link control bits from the current CDB into the CDB12 register. Note that the bits used by the 33C93B are identical in meaning to the SCSI standard link control bits. Consequently, the host processor may simply load the control byte from the current SCSI command into CDB12 to obtain the correct function. As the command execution progresses, the COMMAND PHASE register will update to indicate the last phase completed.

The possible sequences caused by this command are as follows:

- CDB12 bit0=0, bit1=don't care: The status byte in CDB11 is sent, followed by a Command Complete message (00 hex), followed by a transition to bus free. A "successful completion" interrupt now occurs.
- CDB12 bit0=1, bit1=0: The status byte in CDB11 is sent, followed by a Linked-Command-Complete message (0A hex). If the DF bit in the DESTINATION ID register is not set, a chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to obtain the next CDB from the initiator. 33C93B command execution proceeds as described for that command.
- CDB12 bit0=1, bit1=1: The status byte in CDB11 is sent, followed by a Linked-Command-Complete-with-Flag message (0B hex). If the DF bit in the DESTINATION ID register is not set, a chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to obtain the next CDB from the initiator. 33C93B command execution proceeds as described for that command.

Assertion of ATN- when HA=1, assertion of MR-, or execution of a Disconnect or Reset command will terminate this command.

The following table summarizes the possible values that the COMMAND PHASE register can assume during the Send-Status-and-Command-Complete command and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No operation occurred; typically, ATN- was found to be asserted.
50	Status phase transfer completed.
60	Command Complete message transfer completed.
61	Linked Command Complete message transfer completed.

The host processor may resume the Send-Status-and-Command-Complete command by loading the appropriate value into the COMMAND PHASE register prior to issuing the command. This feature, in conjunction with the capability to chain to other combination commands, allows for a single command to invoke longer SCSI bus sequences.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Send-Status-and-Command-Complete command:

COMMAND PHASE	MEANING
50	Resume after status phase. Start with command complete message. May chain to command fetch if selected to do so.

4.6.5 Send-Disconnect-Message (0E hex)

The Send-Disconnect-Message command, a target-mode command, instructs the 33C93B to send a Disconnect message and then to deassert the BSY- signal, causing a logical disconnection of the device from the SCSI bus. Also, a Save-Data-Pointer message will precede the Disconnect message if the host sets the IDI bit prior to issuing this command.

Assertion of ATN- when HA=1, assertion of MR-, or execution of a Disconnect or Reset command will terminate this command. The following table summarizes the possible values that the COMMAND PHASE register can assume during the Send-Disconnect-Message and their meanings relative to command termination.

COMMAND PHASE	MEANING
00	No operation occurred; typically, ATN- was found to be asserted.
41	The Save-Data-Pointer message was transferred.
42	The Disconnect message was transferred.
43	The bus free state occurred after the Disconnect message was transferred. The 33C93B is now in the disconnected state.

5.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to GND ..... -0.5 V to +7.0 V
Operating temperature ..... 0° to 70° C
Storage temperature ..... -55° to +125° C
Power dissipation ..... 500 mW
Input Static Discharge Protection ..... 1200 V pin to pin

DC OPERATING CHARACTERISTICS ..... Ta = 0° to 70° C,
..... VCC = +5 V ± - 0.25 V, GND = 0 V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
IIL	INPUT LEAKAGE		10	uA	VIN = .4 to VCC
IOL1	SCSI OUTPUT LEAKAGE (INACTIVE)		50	uA	VOUT = .5 to VCC
IOL2	OUTPUT LEAKAGE (TRI-STATE)		10	uA	VOUT = .4 to VCC
VIH	INPUT HIGH VOLTAGE	2.0		V	
VIL	INPUT LOW VOLTAGE		0.8	V	
VIHYS	SCHMITT TRIGGER INPUT HYSTERESIS (ALL SCSI PINS)	0.3		V	
VOH	OUTPUT HIGH VOLTAGE	2.4		V	IO = -400 uA
VOL1	SCSI OUTPUT LOW VOLTAGE (1)		0.5	V	IO = 48.0 mA
VOL2	OUTPUT LOW VOLTAGE (ALL OTHERS)		0.4	V	IO = 4.0 mA
ICC	SUPPLY CURRENT)		36	mA	Ta = +25° C

(1) REQ- and ACK- will sink 57 mA at 0.5 volts.

6.0 TIMING CHARACTERISTICS

Timing characteristics are valid over the entire operating temperature (0 to 70° C) and voltage (4.75 to 5.25 Volts) ranges, and are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts. All outputs are assumed to have a load capacitance of 50 picofarads. Additionally, open-drain outputs DRQ- and DACK- are tested with 10 mA current source pull-ups as loads.

The SCSI asynchronous timings, furthermore, assume that the minimum assertion and deassertion times specified for the chosen transfer period have been met. For example, with a transfer period of four, the 33C93B, acting as a target, will assert REQ- for at least 200 ns. If the initiator takes more than 200 ns from the leading edge of REQ- to assert ACK-, then the 33C93B will release REQ- within 175 ns. However, if the initiator responds with ACK- within 200 ns of REQ-, the 33C93B may not meet the 175 ns maximum.

These timings, moreover, apply only during a burst and assume that the FIFO has space or data available to allow the burst to continue. For instance, the time from the REQ- in low to ACK- out low for the first byte of a new phase or of a 4096-byte burst will depend on the time needed by the 33C93B and possibly the host microprocessor to respond to the new phase or to set up for the next 4096-byte block. Clearly, the 33C93B can not meet the175 ns timing in these situations. In addition, the internal microcontroller controls the handshaking of messages bytes, like the Identify and Disconnect messages, during execution of the combination commands, and again, in these cases, the 33C93B will not meet the asynchronous transfer timings given in the following tables.

Many of the timing parameters that follow are defined in terms of an internal clock cycle time Tcyc. The cycle time depends upon the input clock frequency, the clock divisor selected, and, for synchronous transfers and if the input clock frequency is 16 MHz or greater, the setting of the FSS bit in the SYNCHRONOUS TRANSFER register. Section 6.2.16 provides the details on calculating Tcyc for a given set of these parameters. For normal SCSI transfers, the resulting clock has a frequency from 4 MHz to 5 MHz; for fast SCSI transfers, the frequency falls in the range from 8 MHz to 10 MHz. For non-transfer timings, such as those pertaining to arbitration and bus release, Tcyc corresponds to the value for normal SCSI transfers.

6.1 PROCESSOR/DMA INTERFACE

6.1.1 CLK

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tcp	CLOCK PERIOD	50	125	ns
tch	CLOCK HIGH	20		ns
tcl	CLOCK LOW	20		ns

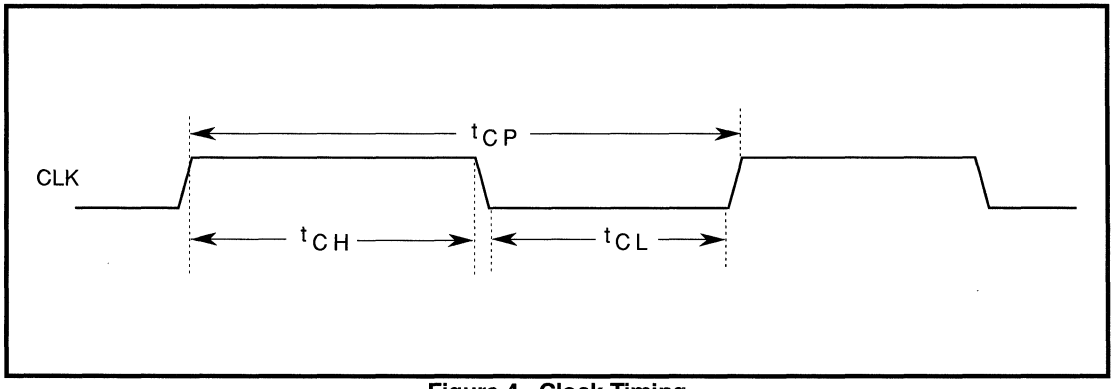


Figure 4. Clock Timing

6.1.2 MR-

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tmr	MR- PULSE WIDTH	1		us

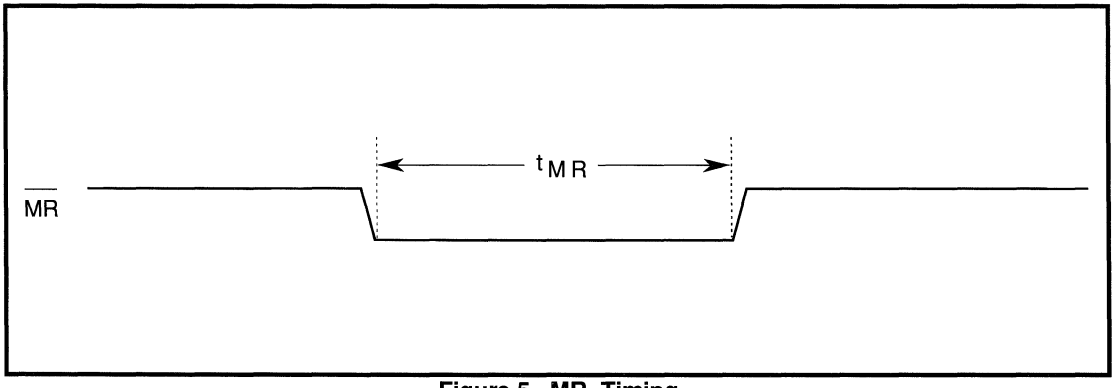


Figure 5. MR- Timing

6.1.3 Processor Write (Indirect Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tavwl	A0 VALID TO WE- LOW	0		ns
tclwl	CS- LOW TO WE- LOW	0		ns
twe	CS- LOW, WE- LOW TIME	120		ns
tdvwh	DATA VALID TO WE- HIGH	70		ns
twhai	WE- HIGH TO A0- INVALID	0		ns
twhch	WE- HIGH TO CS- HIGH	-5		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
twhw1	WE- HIGH TO WE- OR RE- LOW	100		ns

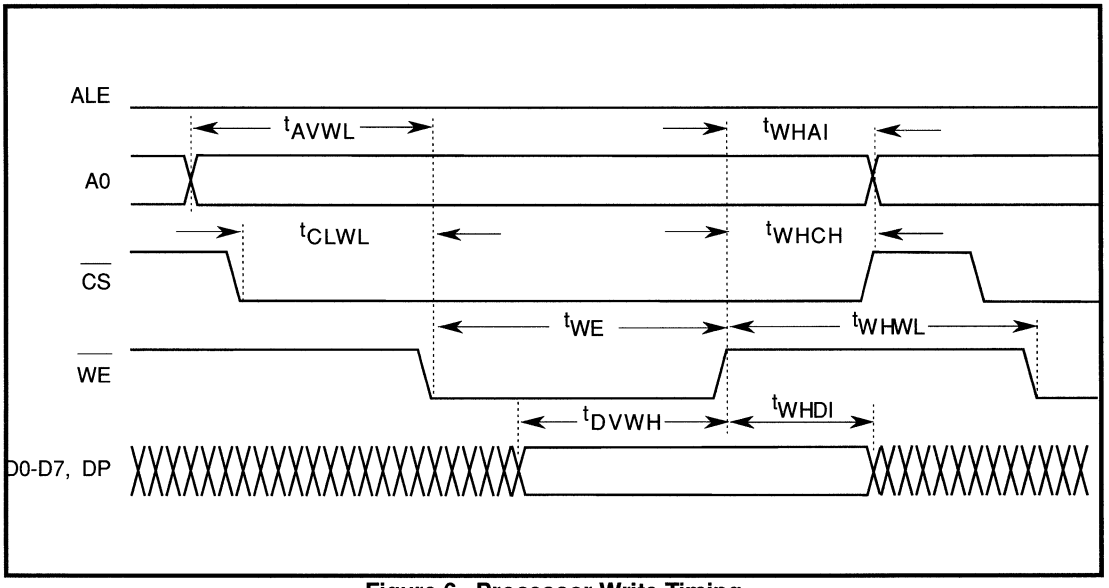


Figure 6. Processor Write Timing

6.1.4 Processor Read (Indirect Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tavrl	A0 VALID TO RE- LOW	0		ns
tclrl	CS- LOW TO RE- LOW	0		ns
tre	CS- LOW, RE- LOW TIME	180	10000	ns
trldv	RE- LOW TO DATA VALID		162	ns
trhch	RE- HIGH TO CS- HIGH	-5		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
trhrl	RE- HIGH TO RE- OR WE- LOW	100		ns
trhai	RE- HIGH TO A0 INVALID	0		ns

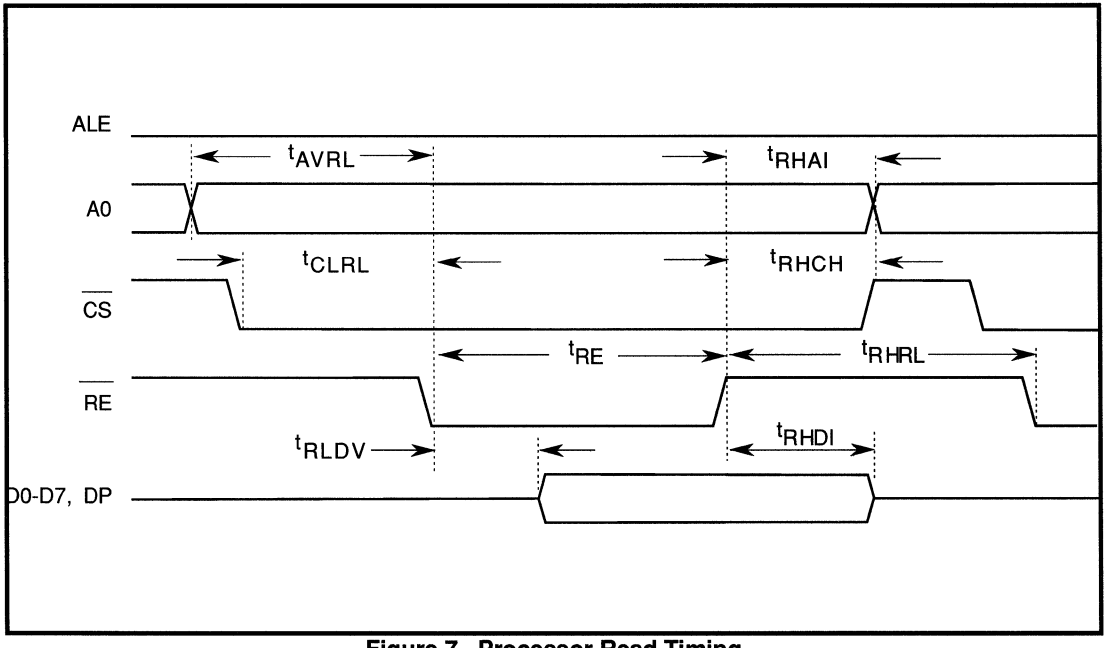


Figure 7. Processor Read Timing

6.1.5 Processor Write (Direct Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
taval	ADDR VALUE TO ALE LOW	40		ns
talai	ALE LOW TO ADDR INVALID	0		ns
talwl	ALE LOW TO WE- LOW	90		ns
tclwl	CS- LOW TO WE- LOW	0		ns
twe	CS- LOW, TO WE- LOW TIME	120		ns
tdvwh	DATA VALID TO WE- HIGH	70		ns
twhch	WE- HIGH TO CS- HIGH	-5		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
twhwl	WE- HIGH TO WE- OR RE- LOW	100		ns
tahal	ALE HIGH TO ALE LOW	40	1000	ns

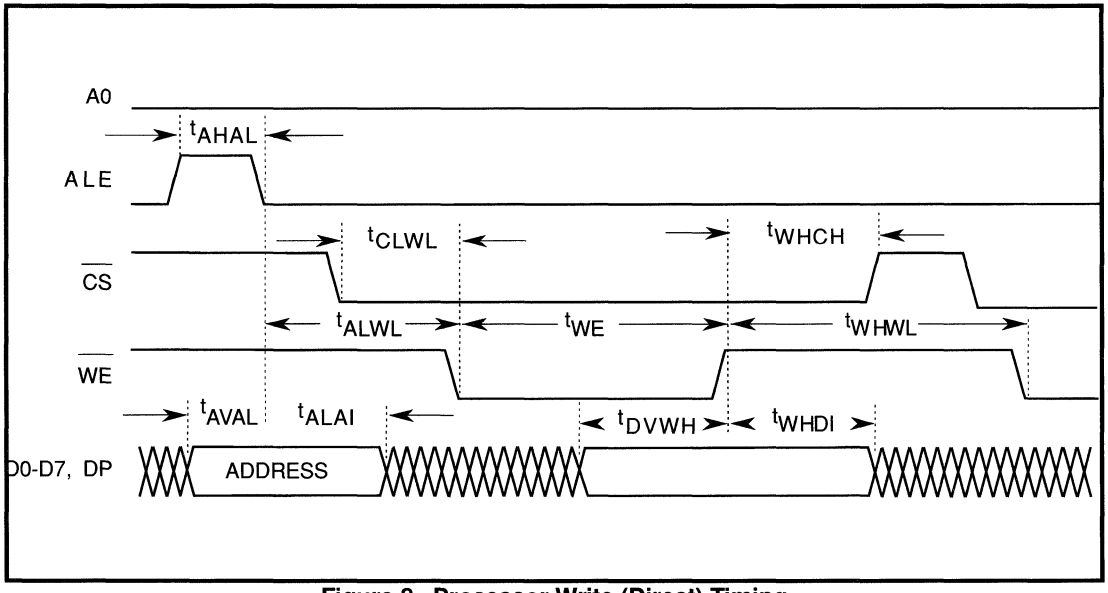


Figure 8. Processor Write (Direct) Timing

30

6.1.6 Processor Read (Direct Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
taval	ADDR VALID TO ALE LOW	40		ns
talai	ALE LOW TO ADDR INVALID	0		ns
talrl	ALE LOW TO RE- LOW	30		ns
tclrl	CS- LOW TO RE- LOW	0		ns
tre	CS- LOW, RE- LOW TIME	180	10000	ns
trldv	RE- LOW TO DATA VALID		162	ns
trhch	RE- HIGH TO CS- HIGH	-5		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
trhrl	RE- HIGH TO RE- OR WE- LOW	100		ns
tahal	ALE HIGH TO ALE LOW	40	1000	ns

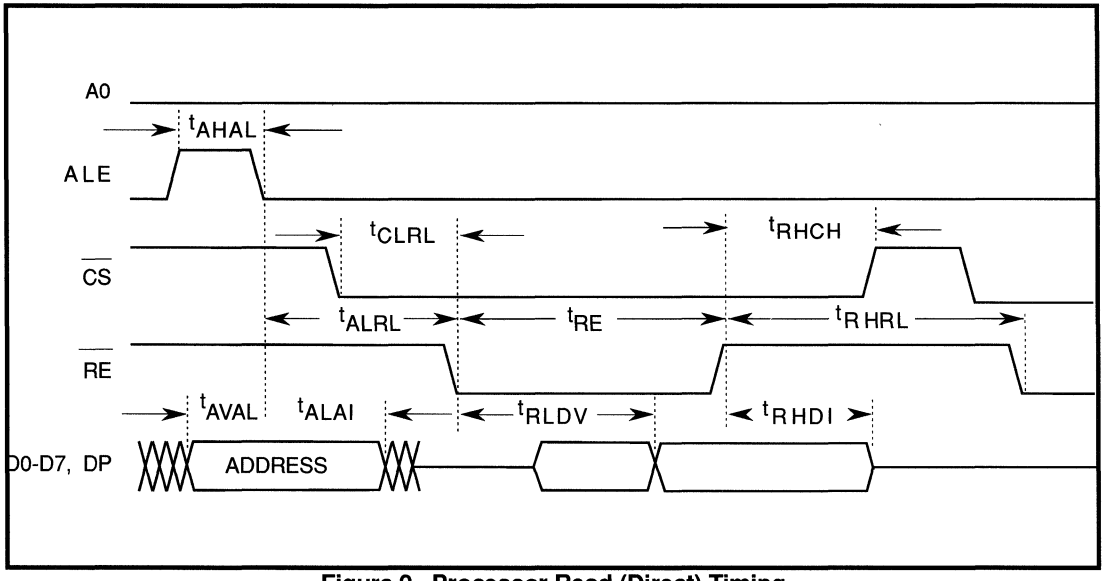


Figure 9. Processor Read (Direct) Timing

6.1.7 DMA Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlwl	DACK- LOW TO WE- LOW	0		ns
tdlqh	DACK- LOW TO DRQ- HIGH		75	ns
twr	WE- PULSE WIDTH	50		ns
twhwl	WE- HIGH TO WE- LOW	100		ns
tdvwh	DATA VALID TO WE- HIGH	25		ns
twhdh	WE- HIGH TO DACK- HIGH	0		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
tdhql	DACK- HIGH TO DRQ- LOW	0		ns

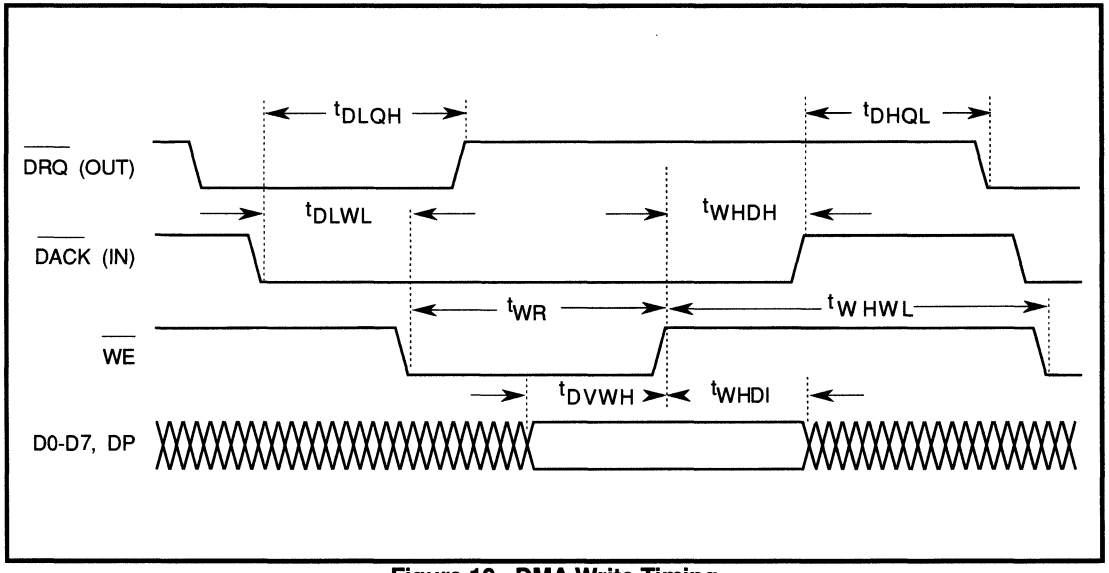


Figure 10. DMA Write Timing

6.1.8 DMA Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlrl	DACK- LOW TO RE- LOW	0		ns
tdlqh	DAKC- LOW TO DRQ- HIGH		75	ns
trd	RE- PULSE WIDTH	80		ns
trhrl	RE- HIGH TO RE- LOW	100		ns
trldv	RE- LOW TO DATA VALID		70	ns
trhdh	RE- HIGH TO DACK- HIGH	0		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
tdhql	DACK- HIGH TO DRQ- LOW	0		ns

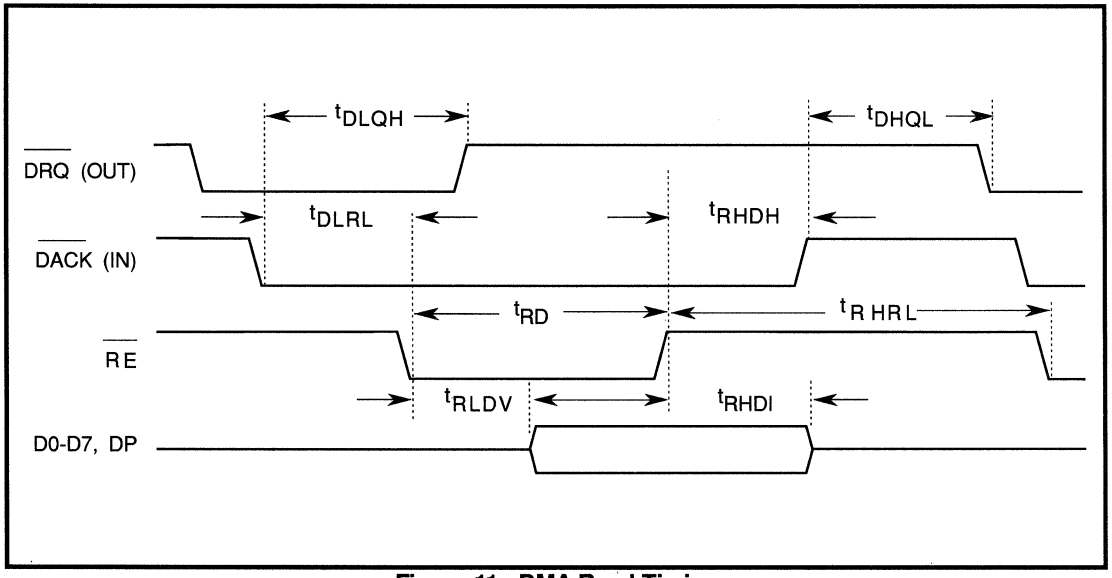


Figure 11. DMA Read Timing

6.1.9 WD-BUS Buffer Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tqhsl	DRQ HIGH TO RCS- LOW	0	40	ns
tslwv	RCS- LOW TO WE- VALID	-5	20	ns
two	WE- PULSE WIDTH (1)	1-10ns		Tcyc
twhwl	WE- HIGH TO WE- LOW (A)	1-10ns		Tcyc
twldv	WE- LOW TO DATA VALID		20	ns
twhdi	WE- HIGH TO DATA INVALID	1-		ns
tqlsh	DRQ LOW TO RCS- TRISTATE	8	10	Tcyc
tshwi	RCS- TRISTATE TO WE- INVALID		100	ns
twhsh	WE- HIGH TO RCS- TRISTATE	0		ns
tslwl	RCS- LOW TO WE- LOW	60		ns
twlql	WE- LOW TO DRQ LOW (2)		55	ns
tslql	RCS- LOW TO DRQ LOW (3)		75	ns

(1) Two + Twhwl = 2*Tcyc

(2) Guarantees that only one more byte will be transferred.

(3) Guarantees that only one byte will be transferred.

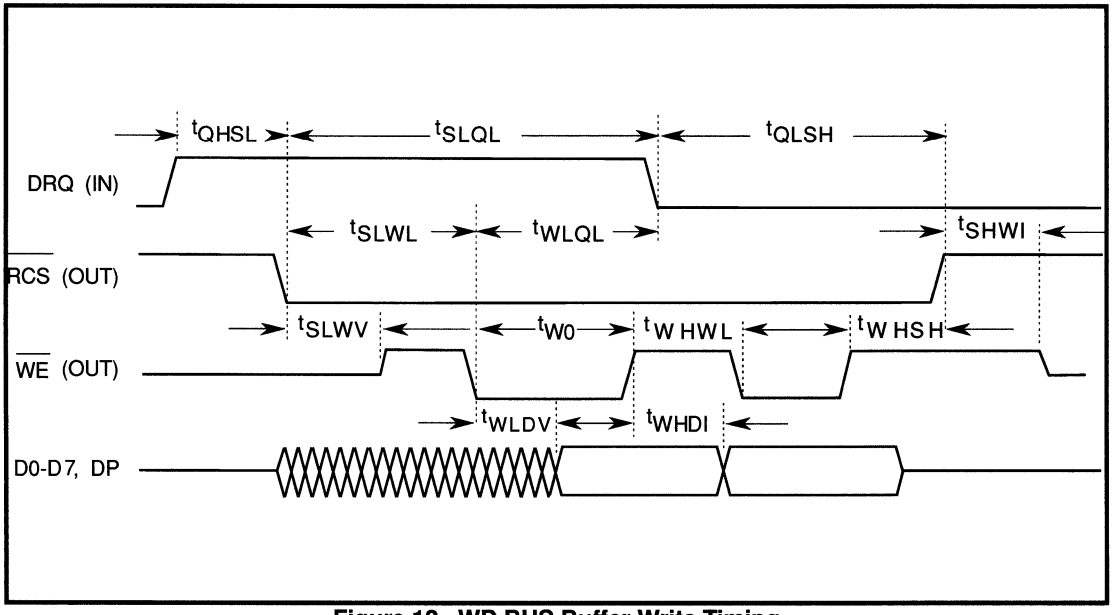


Figure 12. WD BUS Buffer Write Timing

6.1.10 WD-BUS Buffer Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tqhsl	DRQ HIGH TO RCS- LOW	0	40	ns
tslrv	RCS- LOW TO RE- VALID	-5	20	ns
tro	RE- PULSE WIDTH (1)	1-10ns		Tcyc
trhrl	RE- HIGH TO RE- LOW (1)	1-10ns		Tcyc
tdvrh	DATA VALID TO RE- HIGH	20		ns
trhdi	RE- HIGH TO DATA INVALID	0		ns
tqlsh	DRQ LOW TO RCS- TRISTATE	8	10	Tcyc
tshri	RCS- TRISTATE TO RE- INVALID		100	ns
trhsh	RE- HIGH TO RCS- TRISTATE	0		ns
tslrl	RCS- LOW TO RE- LOW	60		ns
trlql	RE- LOW TO DRQ LOW (2)		55	ns
tslql	RCS- LOW TO DRQ LOW (3)		75	ns

(1) Tro + Trhrl = 2*Tcyc

(2) Guarantees that only one more byte will be transferred.

(3) Guarantees that only one byte will be transferred.

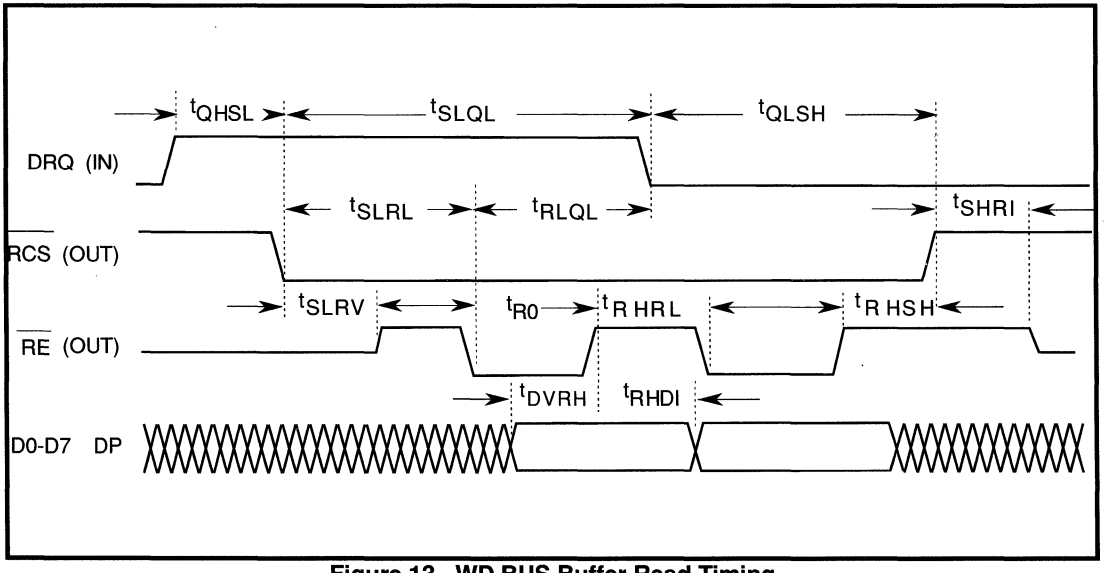


Figure 13. WD BUS Buffer Read Timing

6.1.11 Burst DMA Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlwl	DACK- LOW TO WE- LOW	0		ns
twlqh	WE- LOW TO DRQ- HIGH		50	ns
twr	WE- PULSE WIDTH	30		ns
twhwl	WE- HIGH TO WE- LOW	30		ns
tdvwh	DATA VALID TO WE- HIGH	18		ns
twhdh	WE- HIGH TO DACK- HIGH	0		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
tdhql	DACK- HIGH TO DRQ- LOW	0		ns

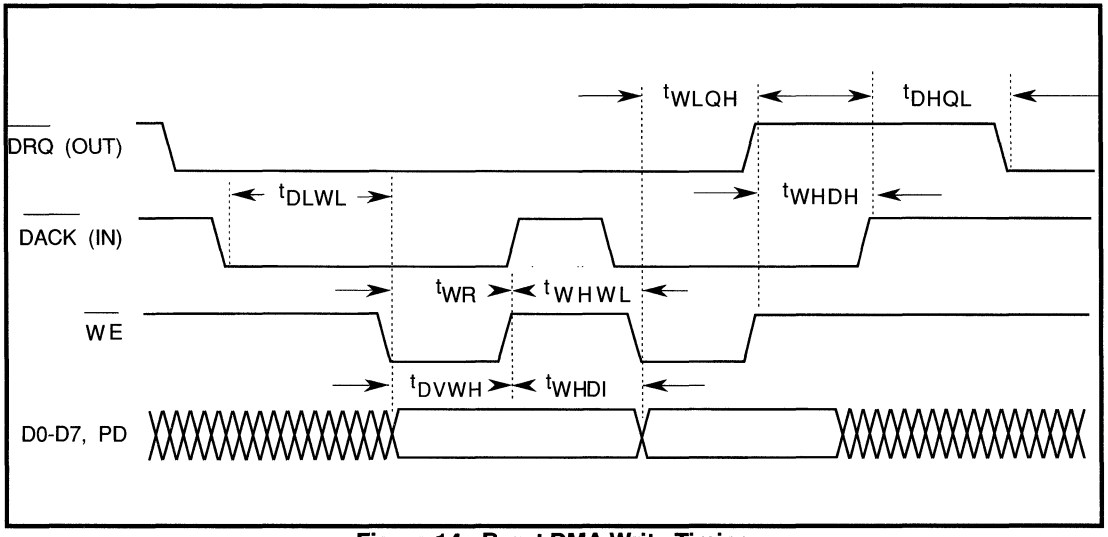


Figure 14. Burst DMA Write Timing

6.1.12 Burst DMA Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlrl	DACK- LOW TO RE- LOW	0		ns
tdldv	DACK- LOW TO DATA VALID	50		ns
trlqh	RE- LOW TO DRQ- HIGH		60	ns
trd	RE- PULSE WIDTH	30		ns
trhrl	RE- HIGH TO RE- LOW	30		ns
trhdv	RE- HIGH TO DATA VALID		80	ns
trhdh	RE- HIGH TO DACK- HIGH	0		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
tdhql	DACK- HIGH TO DRQ- LOW	0		ns

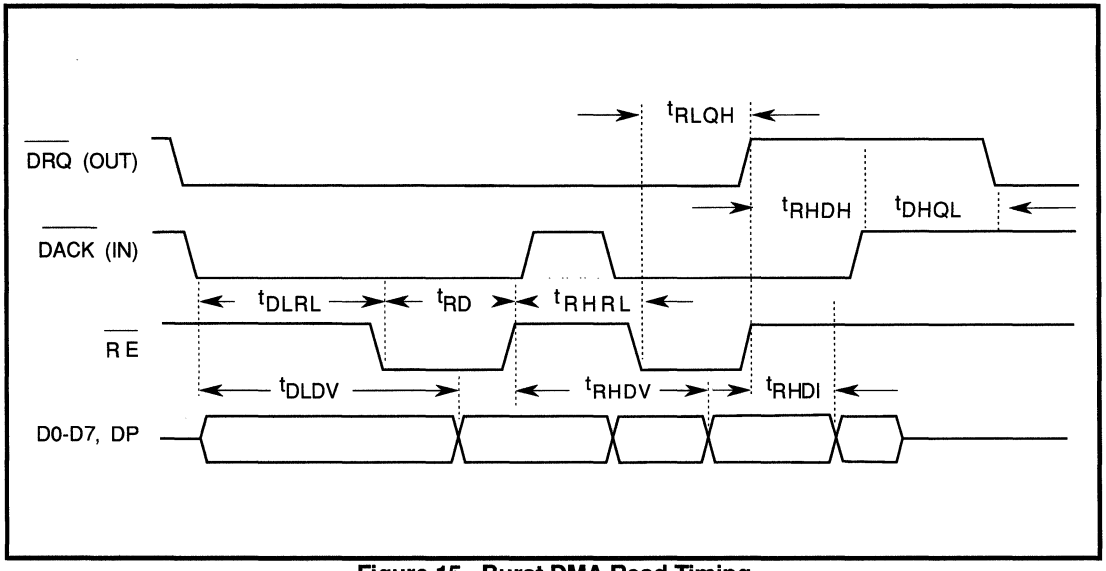


Figure 15. Burst DMA Read Timing

6.1.13 INTRQ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tihrl	INTRQ HIGH TO RE- LOW	0		ns
tri	RE- PULSE WIDTH	180		ns
trhil	RE- HIGH TO INTRQ LOW	0	100	ns
tilih	INTRQ LOW TO INTRQ HIGH	100		ns

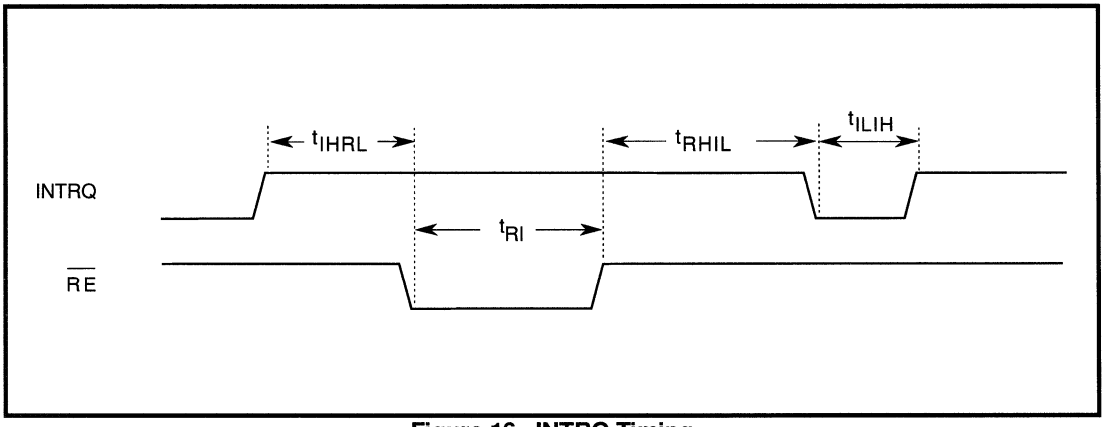


Figure 16. INTRQ Timing

6.2 SCSI INTERFACE

6.2.1 Arbitration

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tbhbl	BSY- , SEL- IN HIGH TO BSY- OUT LOW	12	16	cyc
tblio	BSY- OUT LOW TO BUS ID OUT	-50	50	ns
tblsl	BSY- OUT LOW TO SEL- OUT LOW	2.2		us

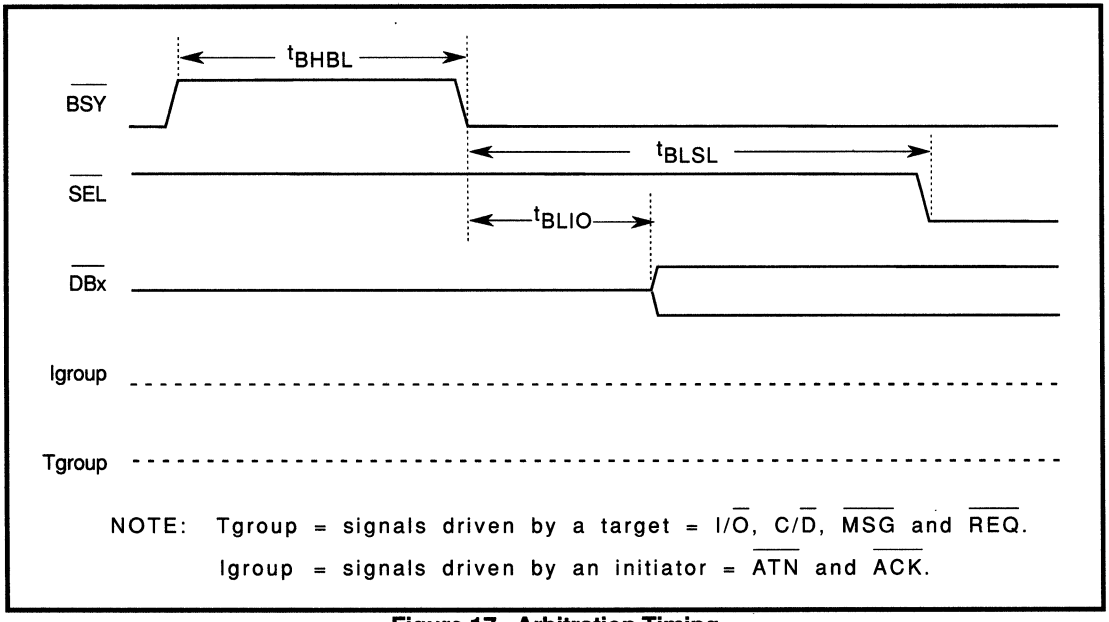


Figure 17. Arbitration Timing

6.2.2 Selecting A Target (As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tsloo	SEL- OUT LOW TO "OR-ED" ID OUT	1.2		us
tovao	"OR-ED" ID OUT VALID TO ACK- , ATN- OUT	100		ns
taobh	ACK- , ATN- OUT VALID TO BSY- OUT HIGH	100		ns
tbhbv	BSY- OUT HIGH TO BSY- IN LOW VALID	400		ns
tblsh	BSY- IN LOW TO SEL- OUT HIGH	100		ns

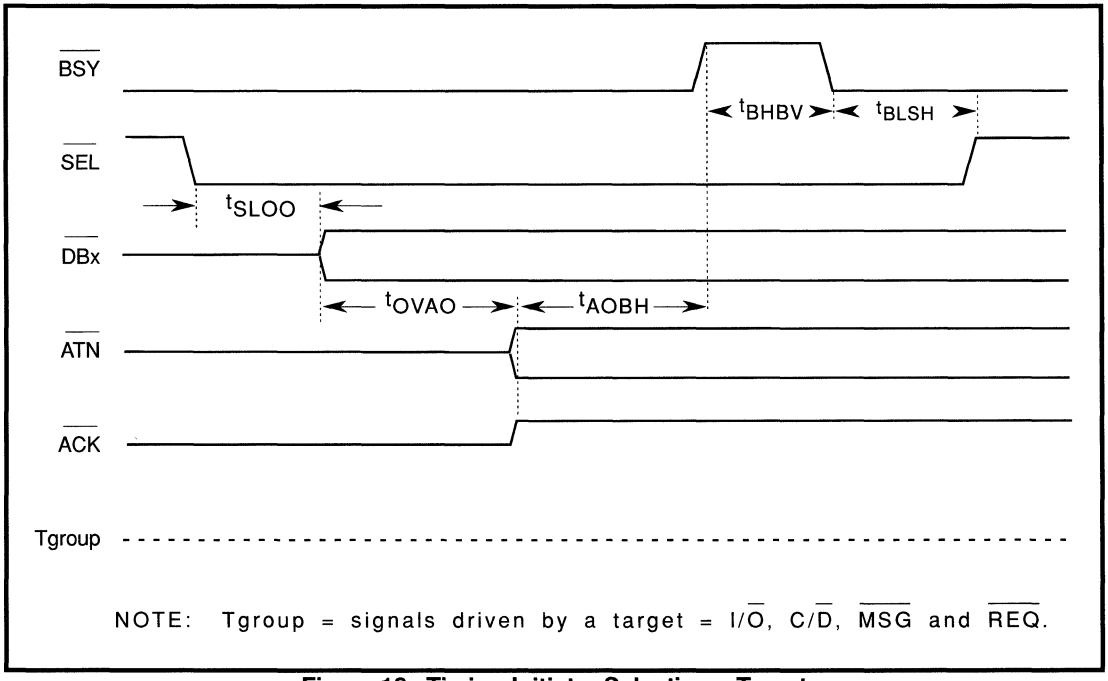


Figure 18. Timing-Initiator Selecting a Target

6.2.3 Response To Selection (As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslbh	SEL- IN LOW TO BSY- IN HIGH	0		ns
tivbh	"OR-ED" ID VALID IN TO BSY- IN HIGH	0		ns
tbhbl	SEL- LOW, ID VALID, BSY- HIGH TO BSY- OUT LOW	0.4	200	us
tbloi	BSY- OUT LOW TO "OR-ED" ID INVALID IN	0		ns
tblsh	BSY- OUT LOW TO SEL- IN HIGH	0		ns
tavsh	ATN- VALID IN TO SEL- IN HIGH	0		ns
tshio	SEL- IN HIGH TO Tgroup OUT	100		ns

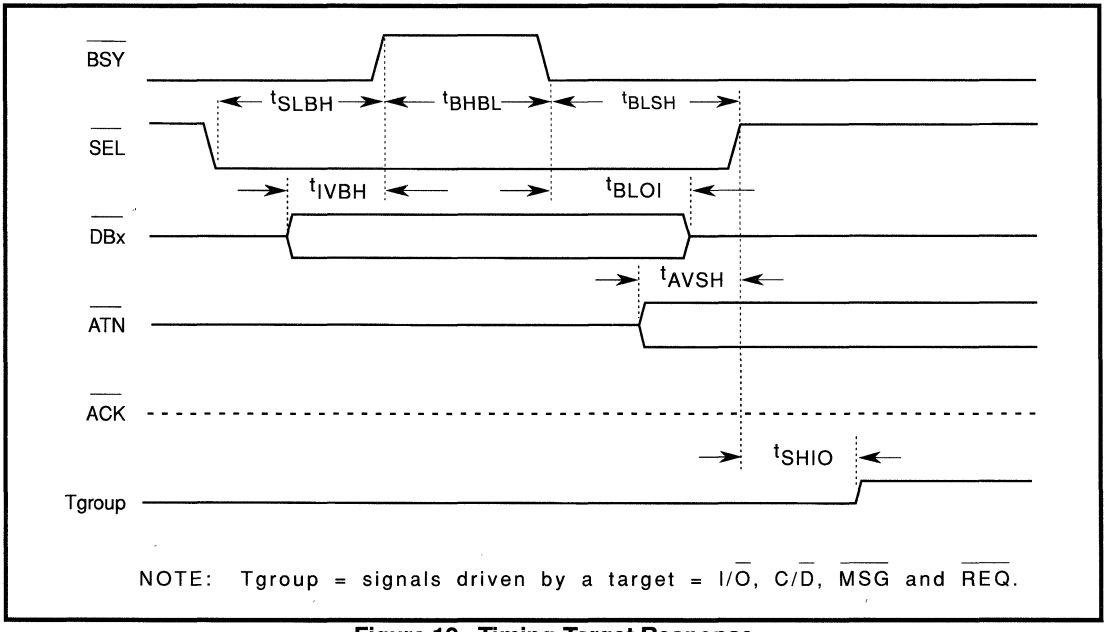


Figure 19. Timing-Target Response

6.2.4 Reselecting An Initiator (As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tsloo	SEL- OUT LOW TO "OR-ED" ID OUT	1.2		us
tovio	"OR-ED" ID OUT VALID TO I/O AND Tgroup OUT VALID	100		ns
tiobh	I/O AND Tgroup OUT VALID TO BSY- OUT HIGH	100		ns
tbhbv	BSY- OUT HIGH TO BSY- IN LOW VALID	400		ns
tblsh	BSY- IN LOW TO SEL- OUT HIGH	100		ns

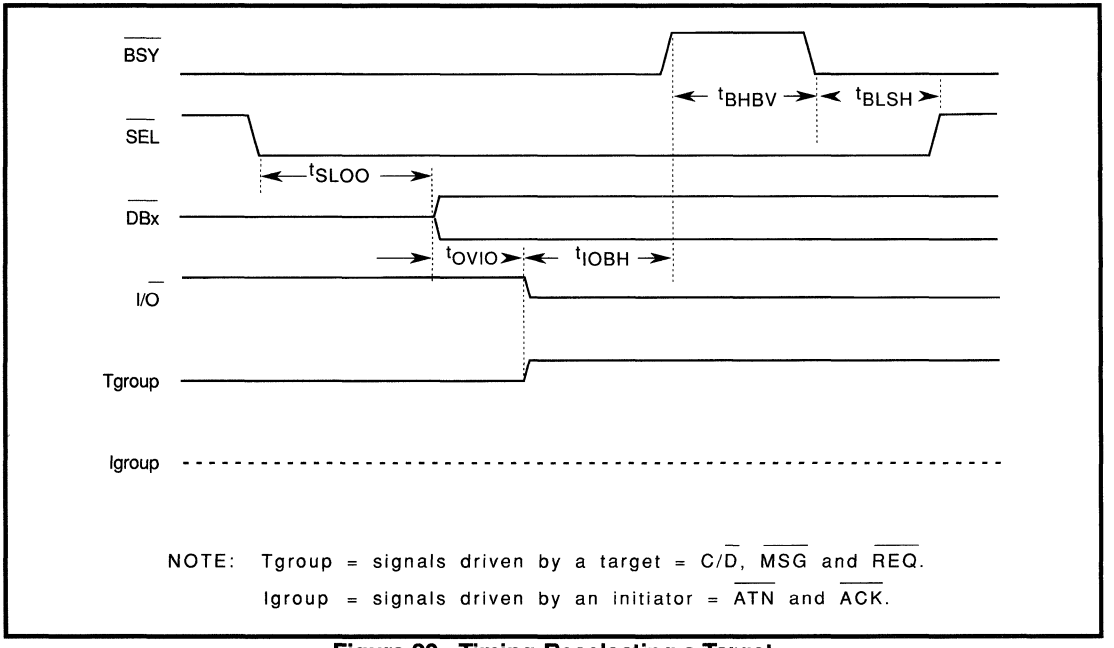


Figure 20. Timing-Reselecting a Target

6.2.5 Response To Reselection (As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslbh	SEL- IN LOW TO BSY- IN HIGH	0		ns
tivbh	"OR-ED" ID VALID IN TO BSY- IN HIGH	0		ns
tilbh	I/I- IN LOW TO BSY- IN HIGH	0		ns
tbhao	SEL- LOW, ID VALID, BSY- HIGH TO Igroup OUT	100		ns
tavbl	Igroup VALID OUT TO BSY- OUT LOW	100		ns
tbhbl	BSY- IN HIGH TO BSY- OUT LOW	0.4	200	ns
tbloi	BSY- OUT LOW TO "OR-ED" ID INVALID IN	0		ns
tblsh	BSY- OUT LOW TO SEL- IN HIGH	0		ns
tshbh	SEL- IN HIGH TO BSY- OUT HIGH	0		ns

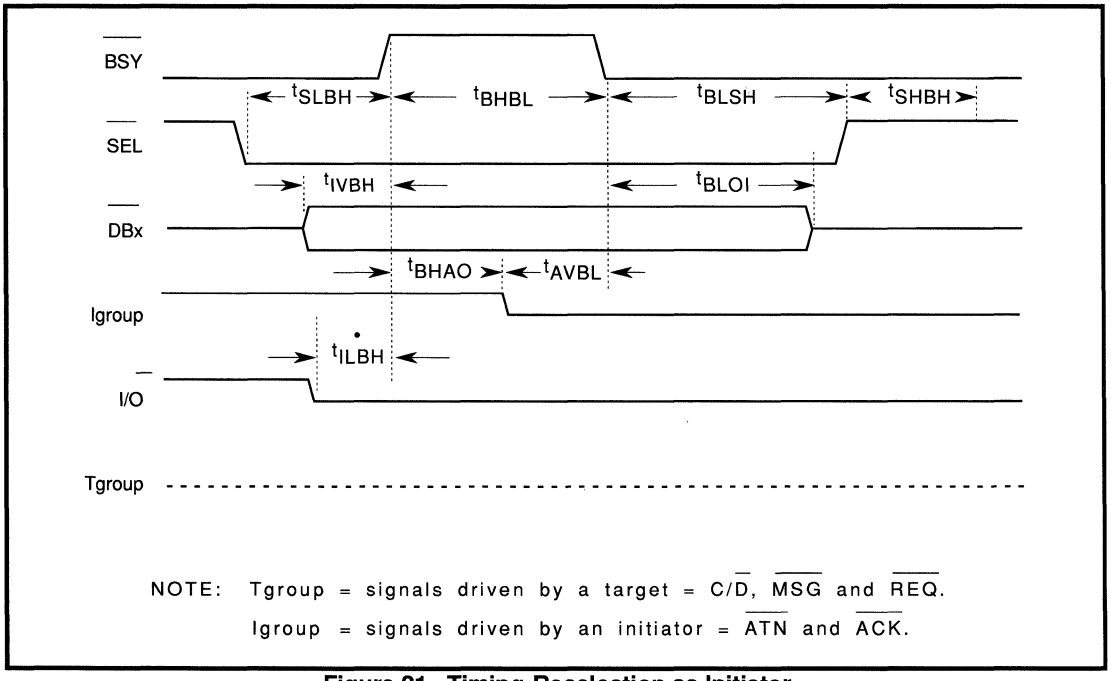


Figure 21. Timing-Reselection as Initiator

6.2.6 Receive Asynchronous Information Transfer In (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshpc	SEL- IN HIGH TO PHASE CHANGE IN	0		ns
tildt	I/O- IN LOW TO DATA BUS TRISTATE	0	125	ns
tpcrl	PHASE CHANGE IN TO REQ- IN LOW	400		ns
tdvrl	DATA VALID IN TO REQ- IN LOW	0		ns
trlal	REQ- IN LOW TO ACK- OUT LOW	0	175	ns
tadli	ACK- OUT LOW TO DATA INVALID IN	0		ns
talrh	ACK- OUT LOW TO REQ- IN HIGH	0		ns
trhah	REQ- IN HIGH TO ACK- OUT HIGH	0	175	ns
tahpc	ACK- OUT HIGH TO PHASE CHANGE IN	0		ns

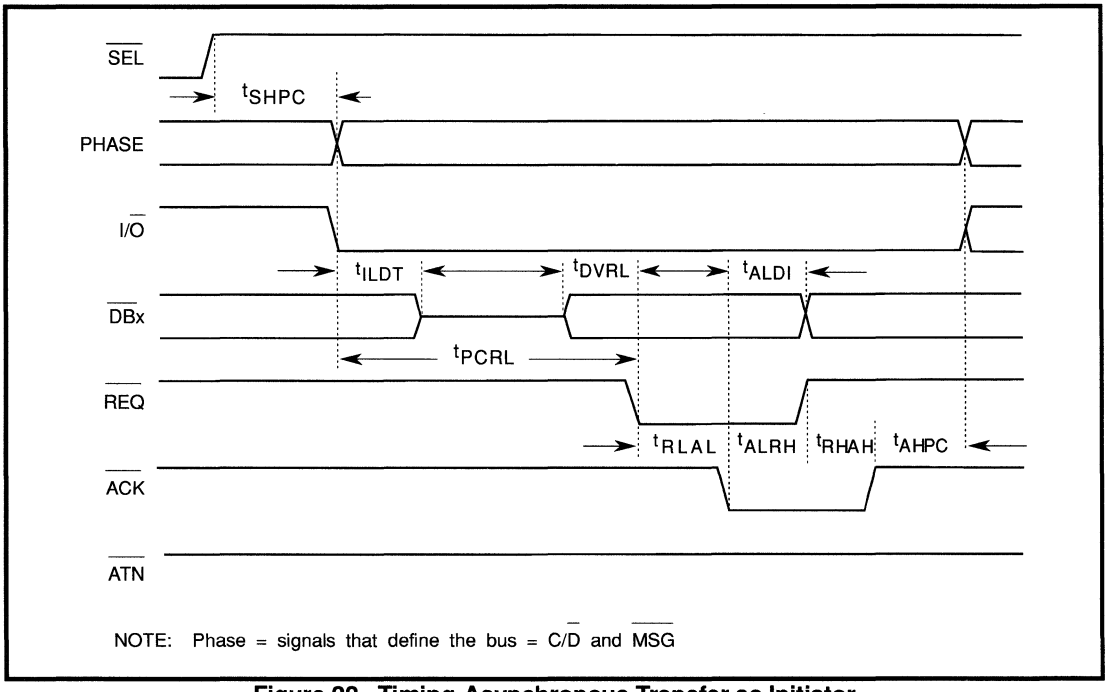


Figure 22. Timing-Asynchronous Transfer as Initiator

6.2.7 Send Asynchronous Information Transfer In (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshpc	SEL- IN HIGH TO PHASE CHANGE OUT	100		ns
tildo	I/O- OUT LOW TO DATA OUT	800		ns
tdvrl	DATA OUT VALID TO REQ- OUT LOW	55		ns
tpcrl	PHASE CHANGE OUT TO REQ- OUT LOW	500		ns
trlal	REQ- OUT LOW TO ACK- IN LOW	0		ns
talrh	ACK- IN LOW TO REQ- OUT HIGH	0	175	ns
taldi	ACK- IN LOW TO DATA OUT INVALID	0		ns
trhah	REQ- OUT HIGH TO ACK- IN HIGH	0		ns
tahpc	ACK- IN HIGH TO PHASE CHANGE OUT	100		ns
tahrl	ACK- IN HIGH TO REQ- OUT LOW	0	175	ns

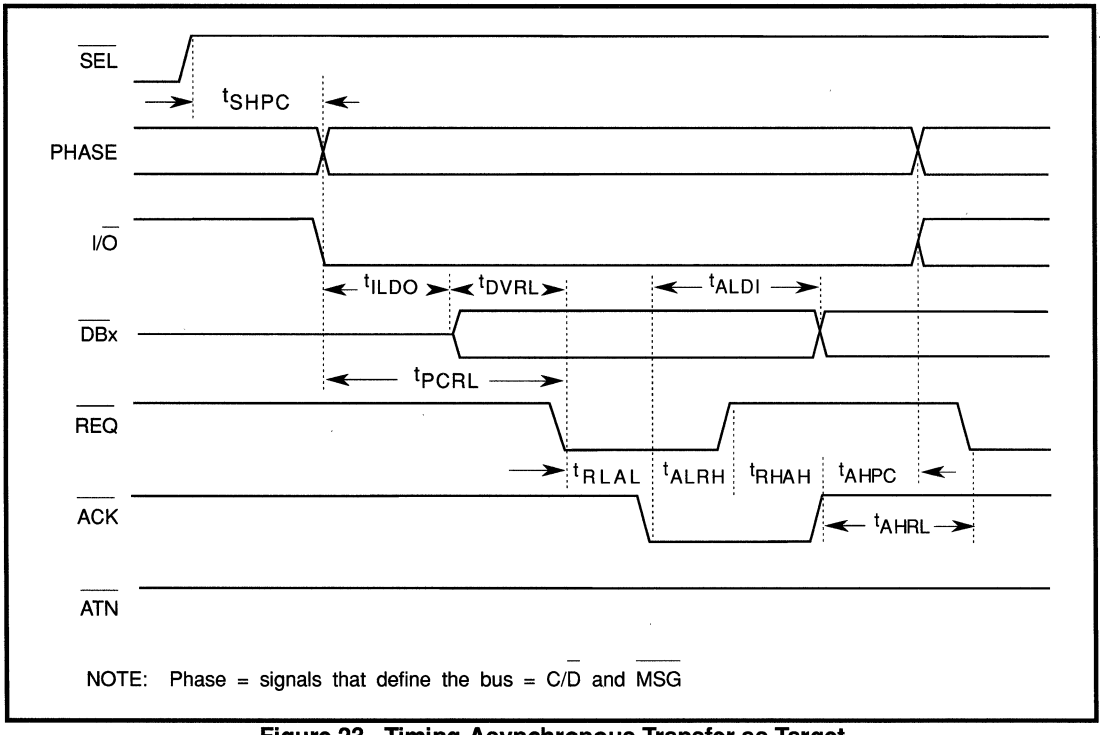


Figure 23. Timing-Asynchronous Transfer as Target

6.2.8 Send Asynchronous Information Transfer Out (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshpc	SEL- IN HIGH TO PHASE CHANGE IN	0		ns
tihdo	I/O- IN HIGH TO DATA OUT	0		ns
tpcrl	PHASE CHANGE IN TO REQ- IN LOW	400		ns
trlal	REQ- IN LOW TO ACK- OUT LOW	0	175	ns
tdval	DATA OUT VALID TO ACK- OUT LOW	55		ns
talrh	ACK- OUT LOW TO REQ- IN HIGH	0		ns
trhah	REQ- IN HIGH TO ACK- OUT HIGH	0	175	ns
trhdi	REQ- IN HIGH TO DATA OUT INVALID	0		ns
tahpc	ACK- OUT HIGH TO PHASE IN CHANGE	0		ns

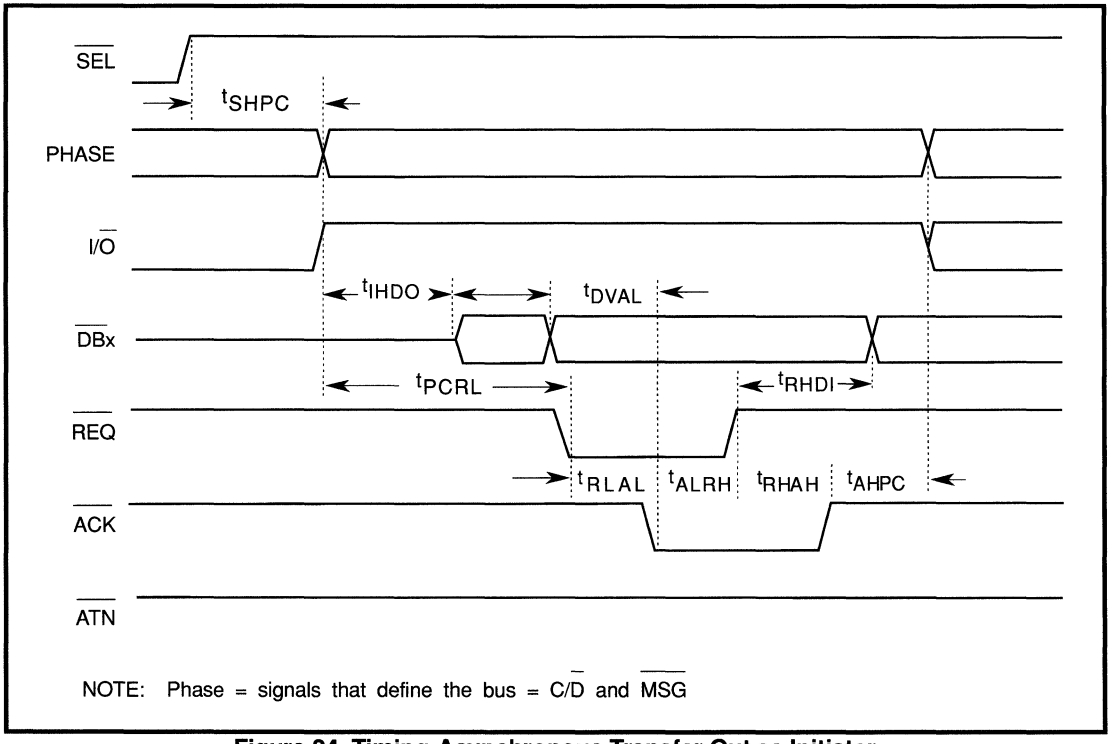


Figure 24. Timing-Asynchronous Transfer Out as Initiator

6.2.9 Receive Asynchronous Information Transfer Out (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshpc	SEL- IN HIGH TO PHASE CHANGE OUT	100		ns
tihdt	I/O- OUT HIGH TO DATA BUS TRISTATE		0	ns
tpcrl	PHASE CHANGE TO REQ- OUT LOW	500		ns
trlal	REQ- OUT LOW TO ACK- IN LOW	0		ns
tdval	DATA IN VALID TO ACK- IN LOW	0		ns
talrh	ACK- IN LOW TO REQ- OUT HIGH	0	175	ns
trhdi	REQ- OUT HIGH TO DATA IN INVALID	0		ns
trhah	REQ- OUT HIGH TO ACK- IN HIGH	0		ns
tahpc	ACK- IN HIGH TO PHASE CHANGE OUT	0		ns
tahrl	ACK- IN HIGH TO REQ- OUT LOW	0	175	ns

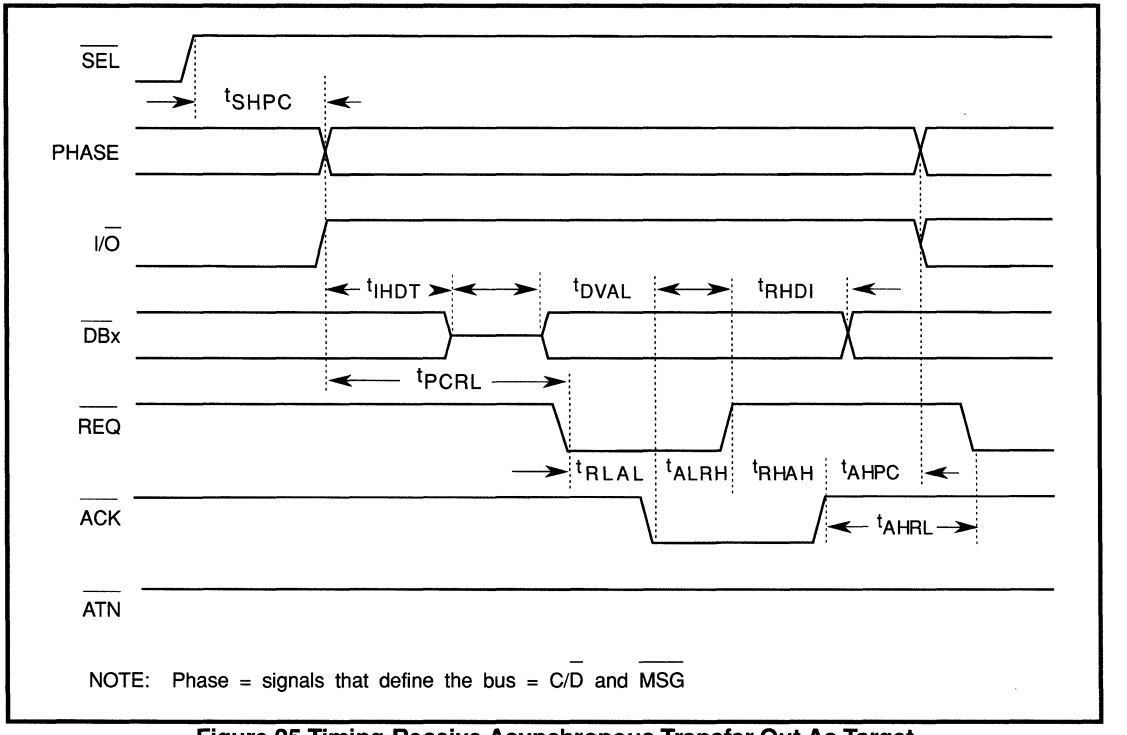


Figure 25.Timing-Receive Asynchronous Transfer Out As Target

6.2.10 Receive Synchronous Information Transfer In (5 and 10 Mb/s) (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrl	DATA VALID IN TO REQ- IN LOW	0		ns
trldi	REQ- IN LOW TO DATA INVALID	30		ns
trcyc	REQ- IN CYCLE TIME	100		ns
trlrh	REQ- IN LOW TO REQ- IN HIGH	30		ns
trhrl	REQ- IN HIGH TO REQ- IN LOW	30		ns
talah	ACK- OUT LOW TO ACK- OUT HIGH (1)	1-10ns		Tcyc
tahal	ACK- OUT HIGH TO ACK- OUT LOW (1)	1-10ns		Tcyc
tahpc	ACK- OUT HIGH TO PHASE CHANGE	0		ns

PARAMETERS tshpc, tildt, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 6.2.6.

(1) Tahal + Talah = 2*Tcyc

30

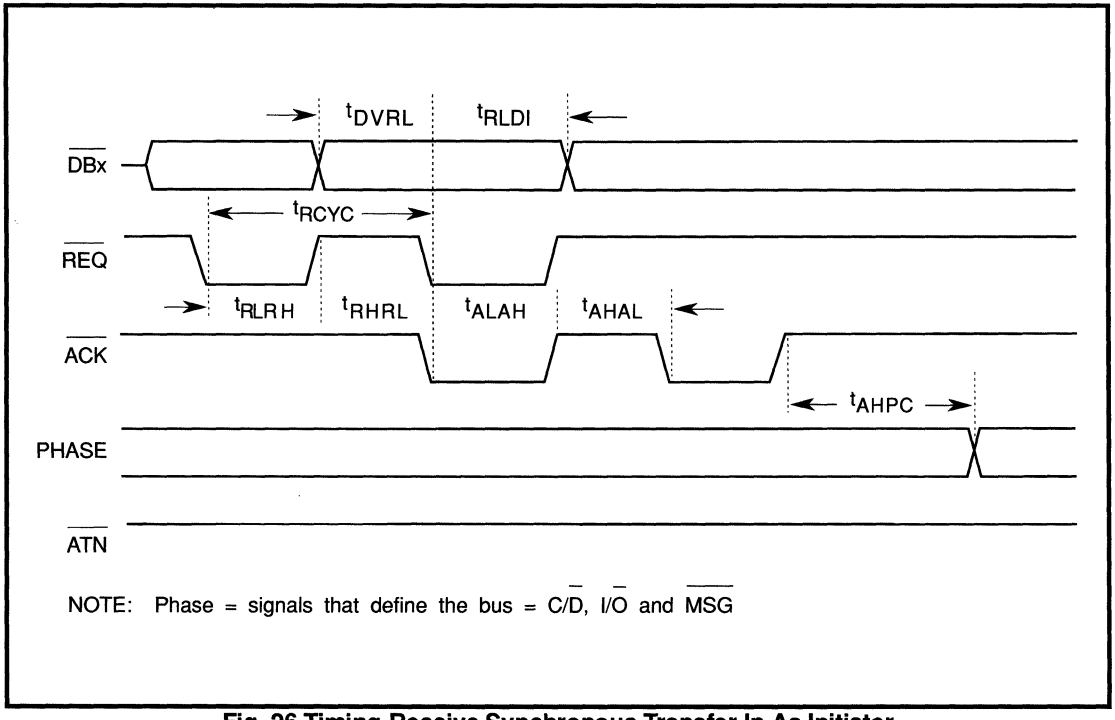


Fig. 26.Timing-Receive Synchronous Transfer In As Initiator

6.2.11a Send Synchronous Information Transfer In (5 Mb/s) (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrl	DATA VALID OUT TO REQ- OUT LOW	55		ns
trldi	REQ- OUT LOW TO DATA INVALID	100		ns
trlrh	REQ- OUT LOW TO REQ- OUT HIGH (1)	1-10ns		Tcyc
trhrl	REQ- OUT HIGH TO REQ- OUT LOW (1)	1-10ns		Tcyc
tacyc	ACK- IN CYCLE TIME	200		ns
talah	ACK- IN LOW TO ACK- IN HIGH	50		ns
tahal	ACK- IN HIGH TO ACK- IN LOW	50		ns
tahpc	ACK- IN HIGH TO PHAS CHANGE OUT	0		ns

PARAMETERS tshpc, tildo, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 6.2.7.

(1) Trhrl + Trlrh = 2*Tcyc

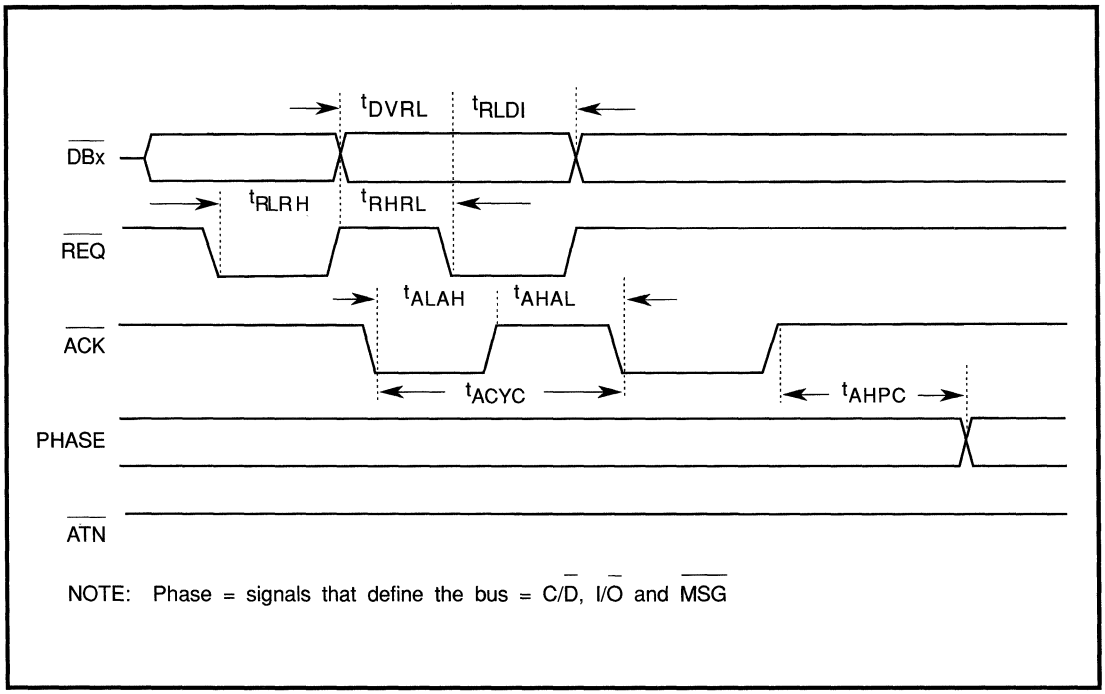


Figure 27. Timing-Send Synchronous Transfer In As Target

6.2.11b Send Synchronous Information Transfer In (10 Mb/s) (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrl	DATA VALID OUT TO REQ- OUT LOW	25		ns
rtrldi	REQ- OUT LOW TO DATA INVALIF	35		ns
trlrh	REQ- OUT LOW TO REQ- OUT HIGH (1)	1-10ns		Tcyc
trhrl	REQ- OUT HIGH TO REQ- OUT LOW (1)	1-10ns		Tcyc
tacyc	ACK- IN CYCLE TIME	100		ns
talah	ACK- IN LOW TO ACK- IN HIGH	30		ns
tahal	ACK- IN HIGH TO ACK- IN LOW	30		ns
tahpc	ACK- IN HIGH TO PHASE CHANGE OUT	0		ns

PARAMETERS tshpc, tildo, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 6.2.7.

(1) Trhrl + Trlrh = 2*Tcyc

30

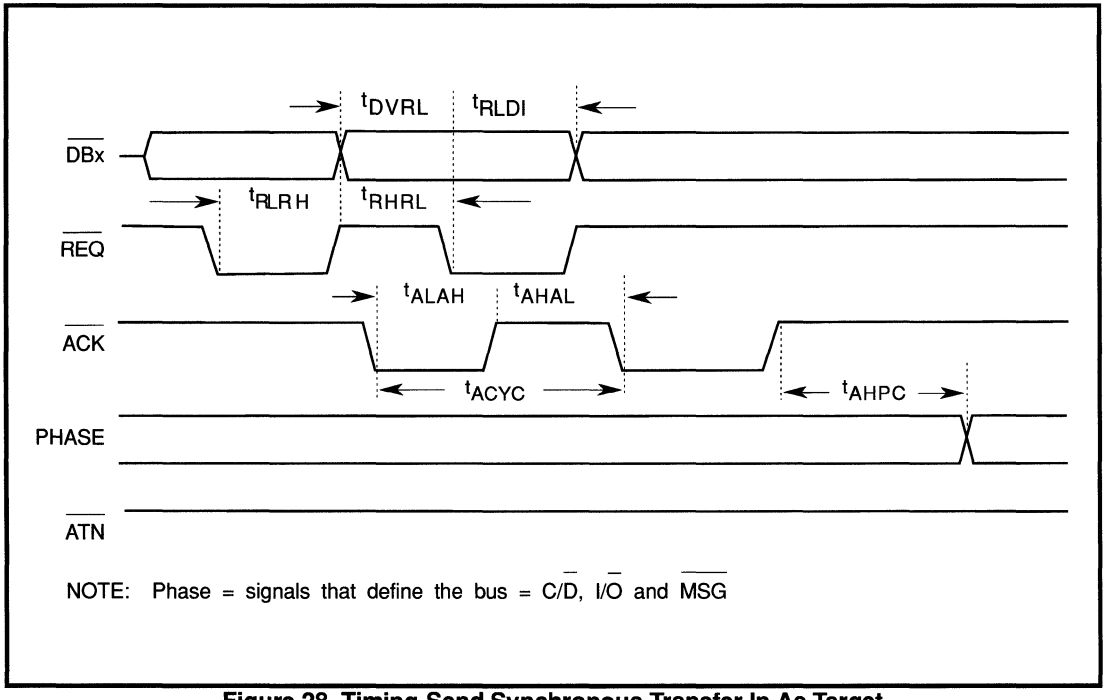


Figure 28. Timing-Send Synchronous Transfer In As Target

6.2.12a Send Synchronous Information Transfer Out (5 Mb/s) (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdval	DATA VALID OUT TO ACK- OUT LOW	55		ns
taldi	ACK- OUT LOW TO DATA INVALID	100		ns
trcyc	REQ- IN CYCLE TIME	200		ns
trlrh	REQ- IN LOW TO REQ- IN HIGH	50		ns
trhrl	REQ- IN HIGH TO REQ- IN LOW	50		ns
talah	ACK- OUT LOW TO ACK- OUT HIGH (1)	1-10ns		Tcyc
tahal	ACK- OUT HIGH TO ACK- OUT LOW (1)	1-10ns		Tcyc
tahpc	ACK- OUT HIGH TO PHASE CHANGE IN	0		ns

PARAMETERS tshpc, tihdo, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 6.2.8.

(1) Tahal + Talah = 2*Tcyc

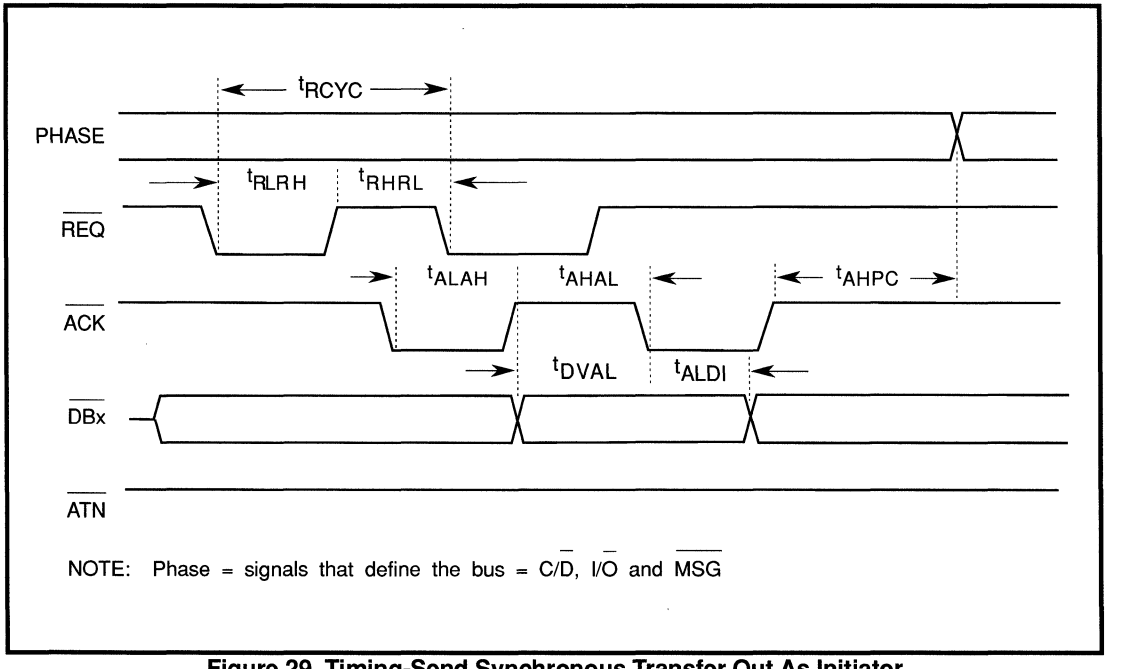


Figure 29. Timing-Send Synchronous Transfer Out As Initiator

6.2.12b Send Synchronous Information Transfer Out (10 Mb/s) (Acting As An Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdval	DATA VALID OUT TO ACK- OUT LOW	25		ns
taldi	ACK- OUT LOW TO DATA INVALID	35		ns
trcyc	REQ- IN CYCLE TIME	100		ns
trlrh	REQ- IN LOW TO REQ- IN HIGH	30		ns
trhrl	REQ- IN HIGH TO REQ- IN LOW	30		ns
talah	ACK- OUT LOW TO ACK- OUT HIGH (1)	1-10ns		Tcyc
tahal	ACK- OUT HIGH TO ACK- OUT LOW (1)	1-10ns		Tcyc
tahpc	ACK- OUT HIGH TO PHASE CHANGE IN	0		ns

PARAMETERS tshpc, tihdo, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 6.2.8.

(1) Tahal + Talah = 2*Tcyc

30

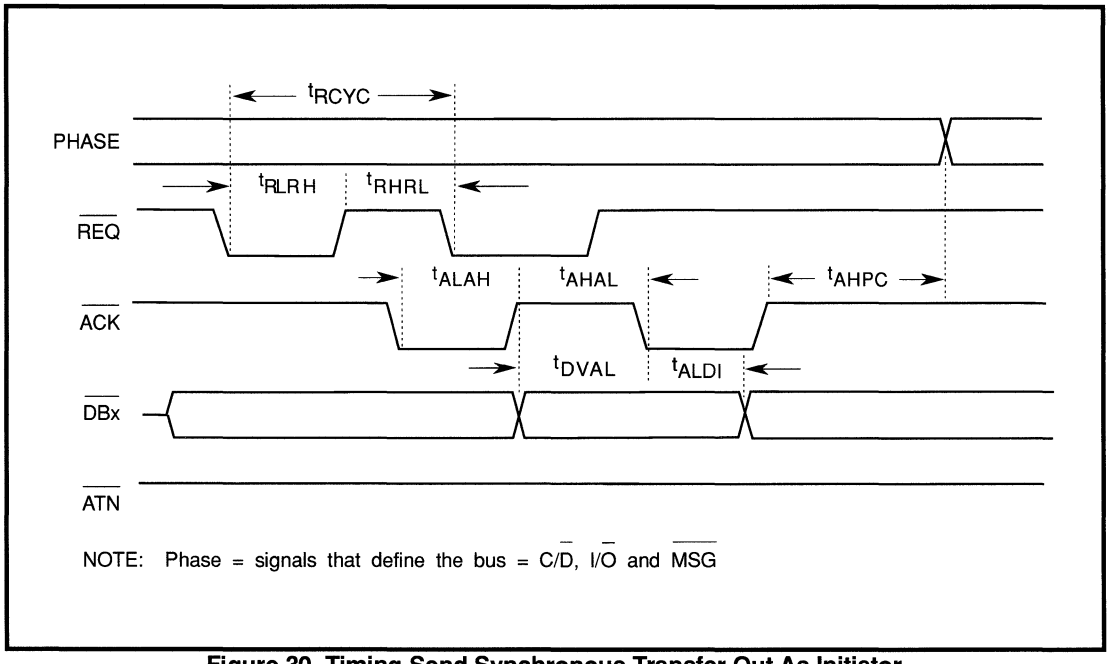


Figure 30. Timing-Send Synchronous Transfer Out As Initiator

6.2.13 Receive Synchronous Information Transfer Out (5 and 10 Mb/s) (Acting As A Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdval	DATA VALID IN TO ACK- IN LOW	0		ns
taldi	ACK- IN LOW TO DATA INVALID	30		ns
trlrh	REQ- OUT LOW TO REQ- OUT HIGH (1)	1-10ns		Tcyc
trhrl	REQ- OUT HIGH TO REQ- OUT LOW (1)	1-10ns		Tcyc
tacyc	ACK- IN CYCLE TIME	100		ns
talah	ACK- IN LOW TO ACK- IN HIGH	30		ns
tahal	ACK- IN HIGH TO ACK- IN LOW	30		ns
tahpc	ACK- IN HIGH TO PHASE CHANGE OUT	0		ns

PARAMETERS tshpc, tihdt, and tpcrl ARE ALSO APPLICABLE AND ARE IDENTICAL TO THOSE IN 6.2.9.

(1) Trhrl + Trlrh = 2*Tcyc

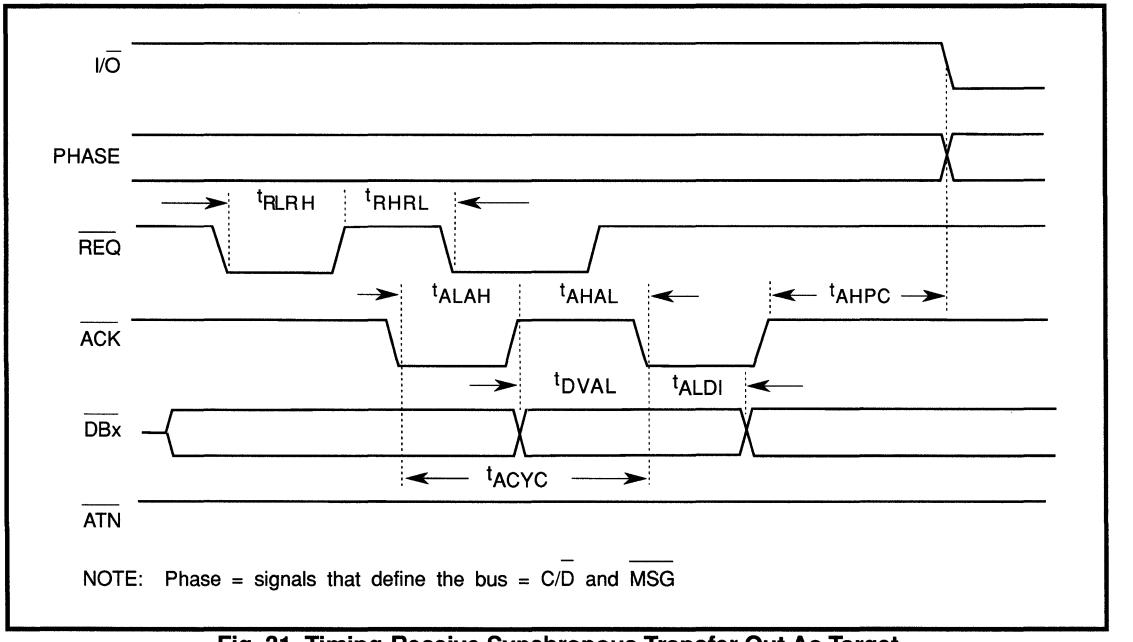


Fig. 31. Timing-Receive Synchronous Transfer Out As Target

6.2.14 Arbitration To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslbh	SEL- IN LOW TO BSY- HIGH, DATA TRI-STATE		6+50ns	Tcyc

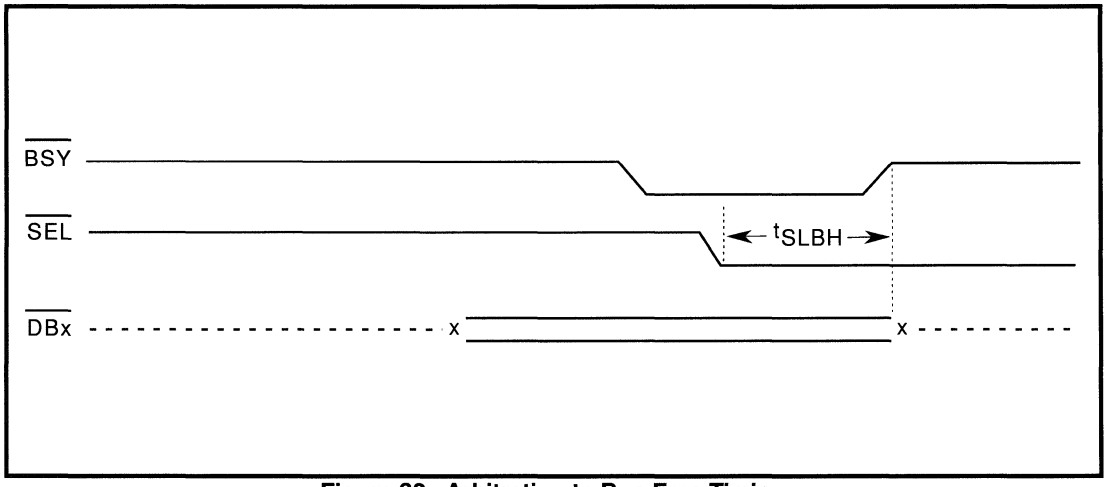


Figure 32. Arbitration to Bus Free Timing

6.2.15 Selection (As An Initiator) Or Reselection (As A Target) To Bus Free (Selection Timeout)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
ttadc	TIMEOUT OR ABORT TO DATA BUS CLEARED	0		ns
tdcsh	DATA BUS CLEARED TO SEL- OUT HIGH	201		us
tshdt	SEL- OUT HIGH TO DATA BUS TRISTATE		800	ns
tshih	SEL- OUT HIGH TO cntl TRISTATE		800	ns

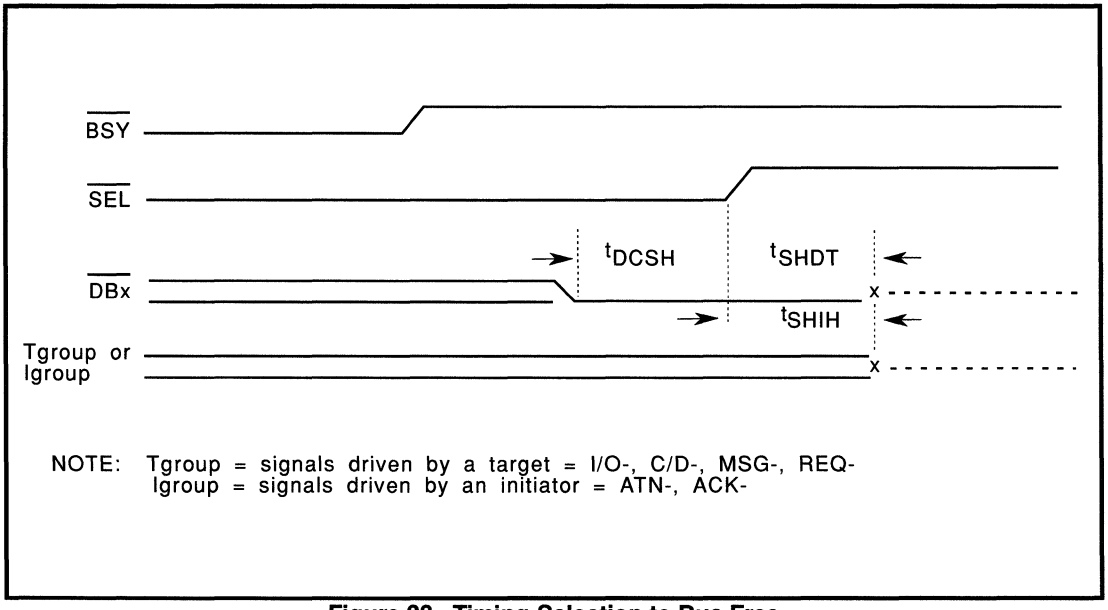


Figure 33. Timing-Selection to Bus Free

6.2.16 Connected-As-An-Initiator To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tbhdt	BSY- IN HIGH TO DATA BUS TRISTATE		8+75ns	Tcyc
tbhgt	BSY- IN HIGH TO Igroup TRISTATE		8+75ns	Tcyc

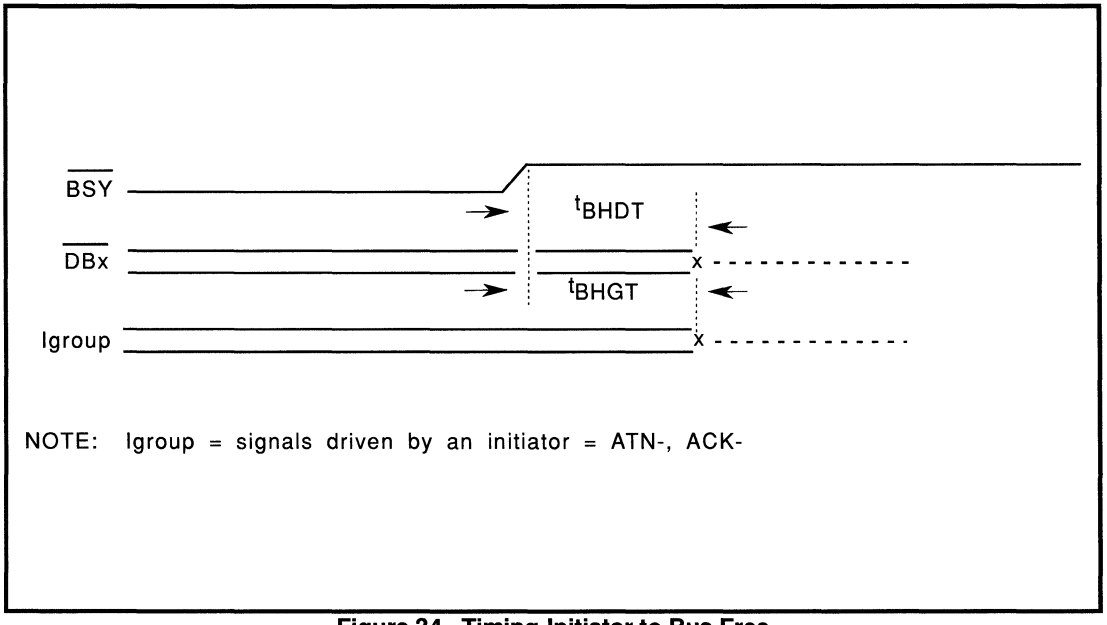


Figure 34. Timing-Initiator to Bus Free

6.2.17 Connected-As-A-Target To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tbhdt	BSY- OUT HIGH TO DATA BUS TRISTATE		8+75ns	Tcyc
tbhgt	BSY- OUT HIGH TO Tgroup TRISTATE		8+75ns	Tcyc

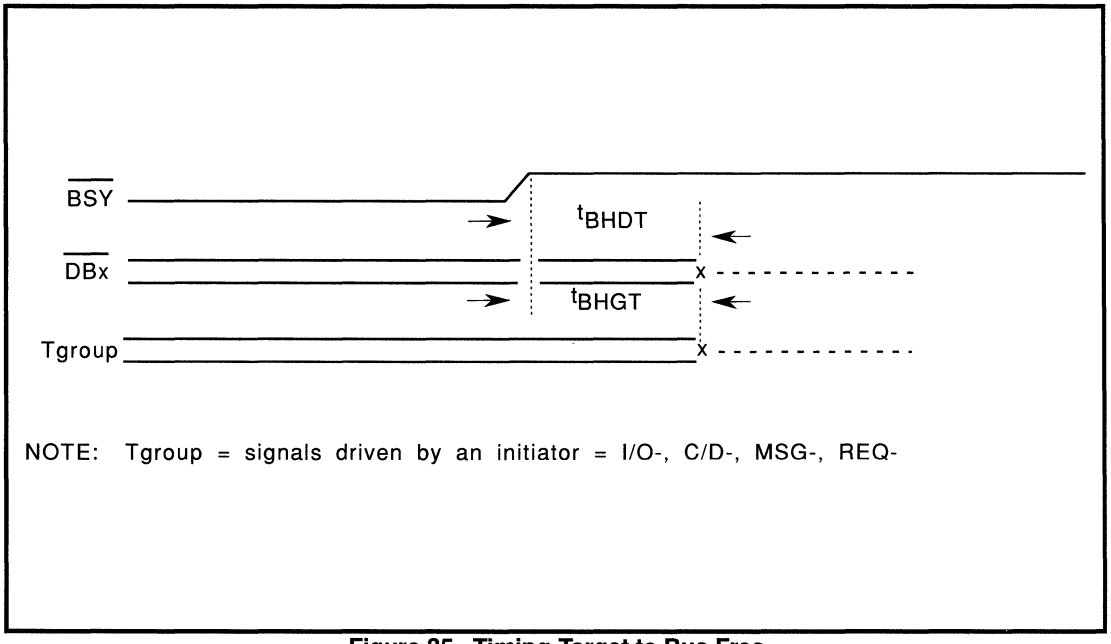


Figure 35. Timing-Target to Bus Free

STORAGE

WD37C65C

Floppy Disk Subsystem

Controller Device

31

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

The WD37C65C Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the host processor and the floppy disk drive. This "superchip" integrates the following functions: formatter/controller, data separation, write precompensation, data rate selection (to a maximum of 1Mbit per second), and clock generation. It also provides interface drivers and receivers for the floppy drive.

The WD37C65C is functionally compatible pin-for-pin with the WD37C65A/B. In addition the WD37C65C supports a power down mode for laptop and portable systems. Refer to Table 36 for a descripion of functional differences between the WD37C65A/B and the WD37C65C.

On the disk drive interface, the WD37C65C includes data separation designed to address high performance error rates on floppy disk drives. It contains all the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Write precompensation is included, in addition to the usual formatting, encoding/decoding, stepper motor control, and status sensing functions. All inputs are TTL compatible Schmitt Trigger line receivers, and outputs are high current, open drain, with 48 mA drivers which meet the ANSI specification.

The host interface supports an 8 or 12 MHz, 286 microprocessor bus without the use of wait states. The inputs are Schmitt Triggers. Output drive capability is 20 LSTTL loads, allowing direct interconnection to bus structures without the use of buffers or transceivers. For PC, PC AT and EISA applications, qualification of interrupt request and DMA request is provided.

Traditionally, data rate selection, drive selection, and stepper motor control have been output ports of the host processor architecture. In the WD37C65C, these functions are latched into registers addressed within the I/O mapping of the system. The WD37C65C has eight internal registers. The eight bit main status register contains status information about the WD37C65C and may be accessed any time. Another four status registers under system control also give various status and error information. The Control Register provides support logic that latches the two LSBs used to select the desired data rate that controls internal clock generation. The Operations Register replaces the standard latched port used in floppy subsystems. These registers are incorporated into the WD37C65C.

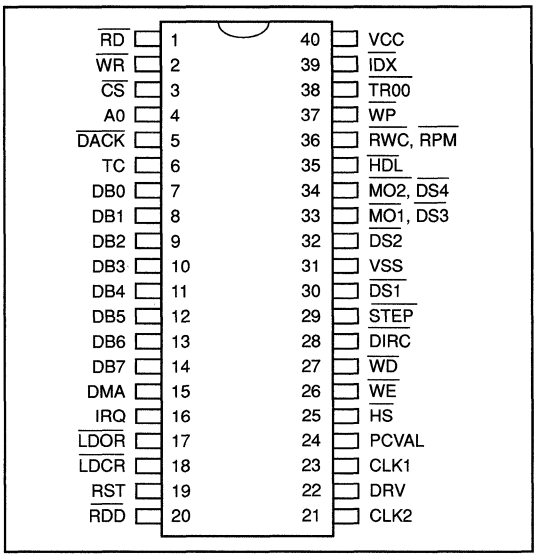
All Clock Generation: SCLK - Sampling Clock, WCLK-Write Clock, and MCLK - Master Clock, are included in the WD37C65C. XTAL oscillator circuits provide the necessary signals for internal timing when using the 44 pin PLCC. If the 40 pin DIP is used, the TTL level clock inputs must be provided. There are two oscillator inputs to the WD37C65C. The first at 32 MHz that handles all standard data rates (1MB/sec, 500, 250, and 125 kb/sec or 16MHz to handle 500, 250, and 125 Kb/sec). The second oscillator is at 9.6 MHz to support the 300 kb/sec data rate used in PC AT designs.

Some AT compatibles use two-speed disk drives. If a two-speed disk drive is used, the DRV input should be grounded along with the CLK2 input.

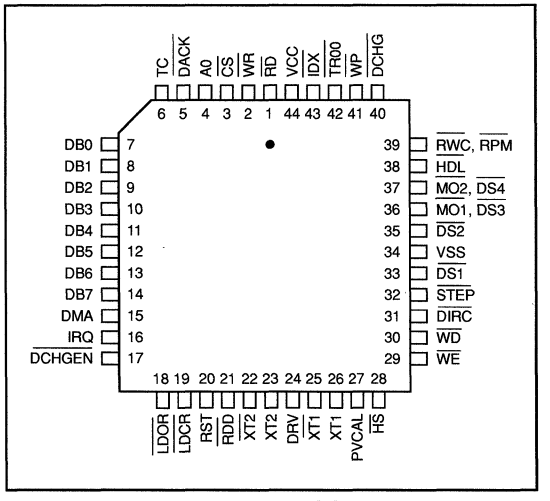
1.1 Features

- IBM PC AT compatible format (single and double density)
  - —Provides "on chip" floppy control and operations
  - —Provides required signal qualification to DMA channel when in PC AT mode
  - —BIOS compatible
  - —Supports dual speed spindle drives
- CMOS low power consumption (typically 300 mW at 32 MHz)
- Power down mode with low standby current (ICC = 100µA maximum)
- Address mark detection circuitry (internal to floppy disk controller)
- Multi-sector and multi-track transfer capability
- Direct floppy disk drive interface (no buffers needed)
  - —48 mA sink output drivers
  - —Schmitt Trigger line receivers
- Compatible with PD8080/85, PD8086, 8088, 80286, 80386SX, 80386, and PD780 (Z80) microprocessors
- On chip clock generation
- Two TTL clock inputs for 40-pin DIP
- Two XTAL oscillator circuits for 44-pin PLCC

- Automatic write precompensation
  - —Disable option
  - —Pin selectable inner track values of 125 or 187 nanoseconds
- Integrated high-performance DPLL data separator
  - —Industry standard error rates of 10<E-9
  - —Data rates of 125, 250, 300, 500 Kbits/second and 1Mbit/second
  - —Option to select 150 Kbits/second FM and 300 Kbits/second MFM data rates only
- Enhanced host interface
  - —20 LSTTL output drive capability
  - —TTL Schmitt trigger inputs
- User programmable track stepping rate and head load/unload times
- Supports four floppy or Micro Floppydisk drives with external decode logic
- Data transfer in DMA or non-DMA mode
- Parallel seek operation on a maximum of four drives
- Internal power up reset circuitry
- Single +5V DC power supply



40 PIN DIP



44 PIN PLCC

2.0 PIN DESCRIPTIONS

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1 /1	$\overline{RD}$	$\overline{READ}$	I	Control signal for transfer of data or status onto the data bus by the WD37C65C.
2/2	$\overline{WR}$	$\overline{WRITE}$	I	Control signal for latching data from the bus into the WD37C65C Buffer Register.
3/3	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	Selected when 0 (low) allowing $\overline{RD}$ or $\overline{WR}$ operation from the host.
4/4	A0	ADDRESS LINE	I	Address line selecting data (=1) or status (=0) information. (A0 = logic 0 during $\overline{WR}$ is illegal except in Power Down mode.)
5/5	$\overline{DACK}$	$\overline{DMA\ ACKNOWLEDGE}$	I	Used by the DMA controller to transfer data from the WD37C65C onto the bus. Logical equivalent to $\overline{CS}$ and A0=1. In Special or AT/EISA mode, this signal is qualified by DMAEN from the Operations Register.
6/6	TC	TERMINAL-COUNT	I	This signal indicates to WD37C65C that data transfer is complete. If DMA operational mode is selected for command execution, TC will be qualified by $\overline{DACK}$, but not in the programmed I/O execution. In AT/EISA or Special mode, qualification by $\overline{DACK}$ requires the Operations Register signal DMAEN to be logically true. Note also that in AT/EISA mode, TC will be qualified by $\overline{DACK}$, whether in DMA or non-DMA host operation. Programmed I/O in AT/EISA mode will cause an abnormal termination error at the completion of a command.
7-14/ 7-14	DB0 thru DB7	DATA BUS 0 thru DATA BUS 7	I/O	8-Bit, bi-directional, tri-state, data bus. D0 is the least significant bit (LSB). D7 is the most significant bit (MSB).
15/15	DMA	DIRECT MEMORY ACCESS	O	DMA request for byte transfers of data. In Special or AT/EISA mode, this pin is tri-stated, enabled by the DMAEN signal from the Operations Register. This pin is driven in the Base mode.
16/16	IRQ	INTERRUPT	O	Interrupt request indicating the completion of command execution or data transfer requests (in non-DMA mode). Normally driven in base mode. In Special or AT/EISA mode, this pin is tri-stated, enabled by the DMAEN signal from the Operations Register.

*Only in the PLCC version of the WD37C65C. Not connected in the DIP package.

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
/17	$\overline{\text{DCHGEN}}$*	$\overline{\text{DISK CHANGE ENABLE}}$	I	This input must be at Logic = 0 to enable $\overline{\text{DCHG}}$ input status at pin 40 to be placed on bit 7 of the data bus during a $\overline{\text{RD}}$ = 0 of $\overline{\text{LDCR}}$ = 0. It has Internal pull-up.
17/18	$\overline{\text{LDOR}}$	$\overline{\text{LOAD OPERATIONS REGISTER}}$	I	Address decode which enables the loading of the Operations Register. Internally gated with $\overline{\text{WR}}$ creates the strobe which latches the data bus into the Operations Register.
18/19	$\overline{\text{LDCR}}$	$\overline{\text{LOAD CONTROL REGISTER}}$	I	Address decode which enables loading of the Control Register. Internally gated with $\overline{\text{WR}}$ creates the strobe which latches the two LSBs from the data bus into the Control Register.
19/20	RST	RESET	I	Resets controller, placing microsequencer in idle. Resets device outputs. Puts device in Base mode, not PC AT or Special mode.
20/21	$\overline{\text{RDD}}$	$\overline{\text{READ DISK DATA}}$	I	This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of the encoded data.
21/	CLK2	CLOCK2	I	TTL level clock input used for non-standard data rates; is 9.6MHz for 300 kb/s, and can only be selected from the Control Register.
/22	$\overline{\text{XT2}}$	$\overline{\text{XTAL2}}$	0	XTAL oscillator drive output for 44 pin PLCC (See Figure 6). Should be left floating if TTL inputs used at pin 23.
/23	XT2	XTAL2	I	XTAL oscillator input used for non-standard data rates. It may be driven with a TTL level signal.
22/24	DRV	DRIVE TYPE	I	Drive type input indicates to the device that a twospeed spindle motor is used if logic is 0. In that case, the second clock input will never be selected and must be grounded.
23/	CLK1	CLOCK1	I	TTL level clock input is used to generate all internal timings for standard data rates. Frequency must be 16MHz ± 0.1% or 32MHz ± 0.1%, and may have 40/60 or 60/40 duty cycle.
/25	$\overline{\text{XT1}}$	$\overline{\text{XTAL1}}$	0	XTAL oscillator drive output for 44 pin PLCC (See Figure 6). Should be left floating if TTL inputs are used at pin 26.
/26	XT1	XTAL1	I	XTAL oscillator input requiring 16MHz or 32MHz crystal. This oscillator is used for all standard data rates, and may be driven with a TTL level signal.

*Only in the PLCC version of the WD37C65C. Not connected in the DIP package.

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
24/27	PCVAL	PRECOMPEN-SATIONVALUE	I	Precompensation value select input. This pin determines the amount of write precompensation used on the inner tracks of the diskette. Logic 1 = 125ns, Logic 0 = 187ns. If the defeat option is used, PCVAL is unimportant and precompensation is disabled.
25/28	$\overline{HS}$	HEAD SELECT	O	High current driver (HCD) output selects the head (side) of the floppy disk that is being read or written. Logic 1 = side 0. Logic 0 = side 1.
26/29	$\overline{WE}$	WRITE ENABLE	O	This HCD output becomes true, active low, just prior to writing on the diskette. This allows current to flow through the write head.
27/30	$\overline{WD}$	WRITE DATA	O	This HCD output is WRITE DATA. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
28/31	$\overline{DIRC}$	DIRECTION	O	This HCD output determines the direction of the head stepper motor. Logic 1 = outward motion. Logic 0 = inward motion.
29/32	$\overline{STEP}$	STEP PULSE	O	This HCD output issues an active low pulse for each track to track movement of the head.
30/33	$\overline{DS1}$	DRIVE SELECT 1	O	This HCD output, when active low, is DRIVE SELECT 1 in AT/EISA mode. It enables the interface to this disk drive. This signal comes from the Operations Register. In Base, or Special mode, this output is #1 of the four decoded Unit Selects, as specified in the device command syntax.
31/34	VSS	GROUND	--	Ground.
32/35	$\overline{DS2}$	DRIVE SELECT 2	0	This HCD output, when active low, is DRIVE SELECT 2 in AT/EISA mode, enables the interface to this disk drive. This signal comes from the Operations Register. In Base or the Special mode, this output is #2 of the four decoded Unit Selects as specified in the device command syntax.
33/36	$\overline{MO1}$, $\overline{DS3}$	MOTOR ON 1, DRIVE SELECT 3	0	This HCD output, when active low, is MOTOR ON enable for disk drive #1, in AT/EISA mode. This signal comes from the Operations Register. In the Base or Special mode, this output is #3 of the four decoded Unit Selects as specified in the device command syntax.

*Only in the PLCC version of the WD37C65C. Not connected in the DIP package.

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
34/37	$\overline{MO2}$, $\overline{DS4}$	$\overline{MOTOR\ ON\ 2}$, $\overline{DRIVE\ SELECT\ 4}$	0	This HCD output, when active low, is MOTOR ON enable for disk drive #2, in AT/EISA mode. This signal comes from the Operations Register. In the Base or Special mode, this output is #4 of the four decoded Unit Selects as specified in the device command syntax.
35/38	$\overline{HDL}$	$\overline{HEAD\ LOADED}$	O	This HCD output, when active low, causes the head to be loaded against the media in the selected drive.
36/39	$\overline{RWC}$, $\overline{RPM}$	$\overline{REDUCED\ WRITE\ CURRENT}$, $\overline{REVOLUTIONS\ PER\ MINUTE}$	O	This HCD output, when active low, causes a REDUCED WRITE CURRENT, when bit density is increased toward the inner tracks, becoming active when tracks >28 are accessed. This condition is valid for Base or Special mode, and is indicative of when write precompensation is necessary. In the AT/EISA mode, this signal will be active when CR0=1.
/40	$\overline{DCHG}$*	$\overline{DISK\ CHANGE}$	I	This Schmitt Trigger (ST) input senses status from the drive. Active low indicates that drive door is open or that the diskette has possibly changed since the last drive selection. It has internal pull-up.
37/41	$\overline{WP}$	$\overline{WRITE\ PROTECTED}$	I	This ST input senses status from the disk drive indicating active low when a diskette is WRITE PROTECTED.
38/42	$\overline{TR00}$	$\overline{TRACK\ 00}$	I	This ST input senses status from disk drive, indicating active low when the head is positioned over the outermost track, TRACK 00.
39/43	$\overline{IDX}$	$\overline{INDEX}$	I	This ST input senses status from the disk drive, indicating active low when the head is positioned over the beginning of a track marked by an index hole.
40/44	VCC	+5VDC	--	Input power supply.

*Only in the PLCC version of the WD37C65C. Not connected in the DIP package.

3.0 ARCHITECTURE

The WD37C65C Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the host processor and the floppy disk drive. This "superchip" integrates: formatter/controller, data separation, write precompensation, data rate selection, clock generation, drive interface drivers and receivers.

Figure 1 illustrates a block diagram of the WD37C65C Floppy Disk Subsystem Controller.

Figure 2 illustrates a typical WD37C65C system.

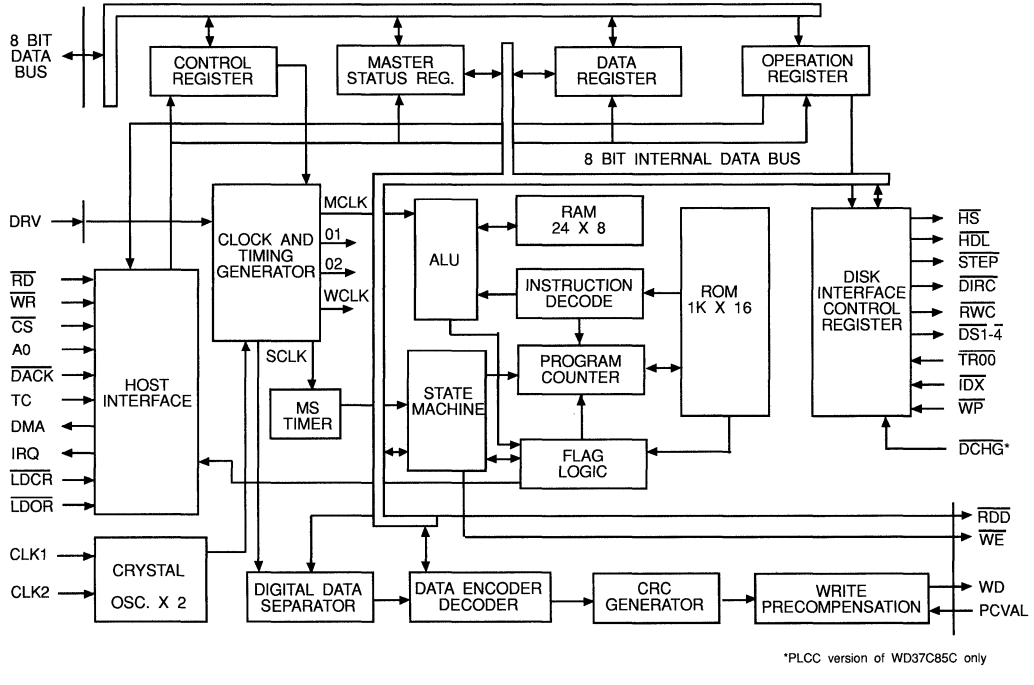


FIGURE 1. WD37C65C BLOCK DIAGRAM

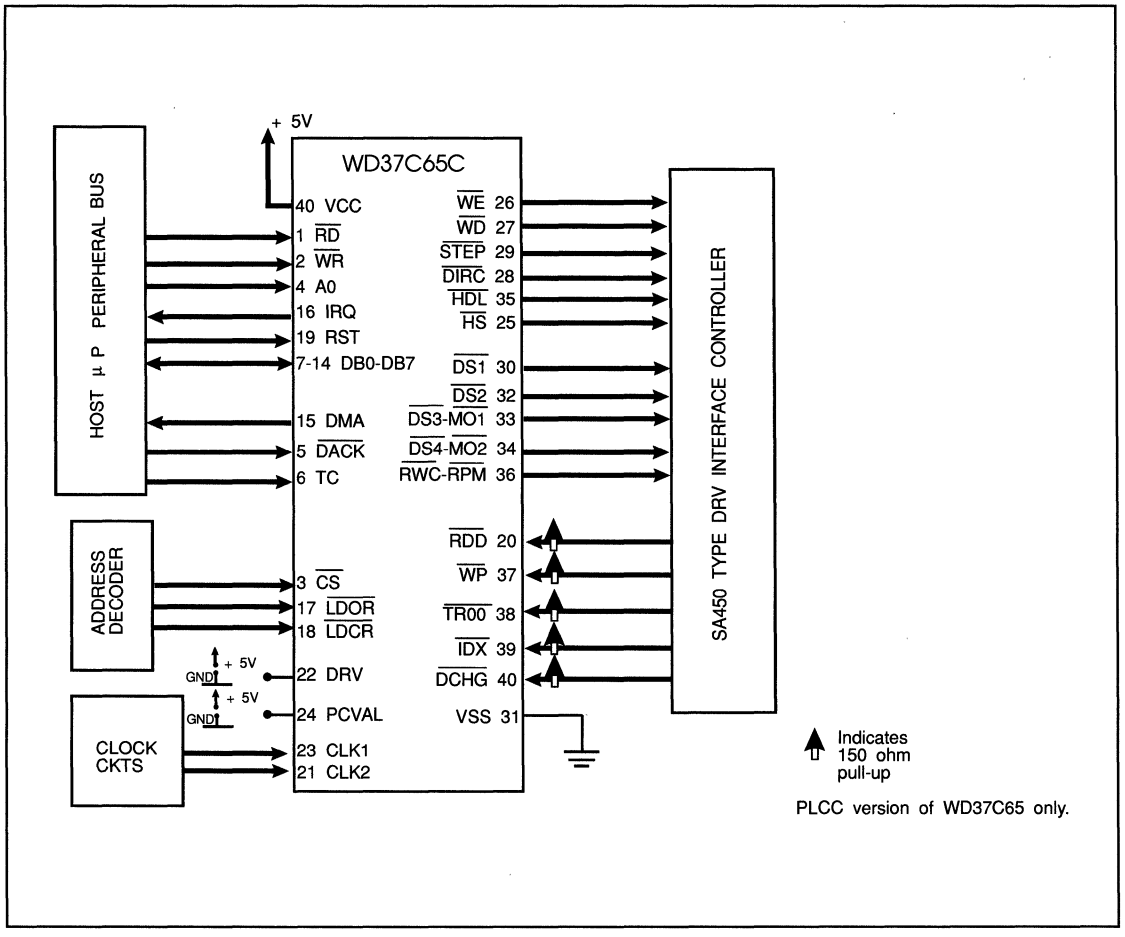


FIGURE 2. TYPICAL WD37C65 SYSTEM

4 .0 HOST INTERFACE

The host interface is the Host Microprocessor Peripheral Bus. This bus is composed of eight control signals and eight data signals. In the Special or AT/EISA modes, IRQ and DMA request are tri-stated and qualified by DMA enable which is provided by the Operations Register. The data bus, DMA, and IRQ outputs are designed to handle 20 LSTTL loading. Inputs are Schmitt Trigger receivers and can be hooked up to a bus or backplane without any additional buffering.

During the Command or Result phases, the Main Status Register must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data is read from or written into the Data Register, the CPU waits for 12 µs before reading the Main Status Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the WD37C65C. Many of the commands require multiple bytes. As a result, the Main Status Register must be read prior to each byte transfer to the WD37C65C. During the Result phase, Bits D6 and D7 in the Main Status Register must both be 1's (D6=1 and D7=1) before reading each byte from the Data Register. Note that this reading of the Main Status Register before each byte transfer to the WD37C65C is required only in the Command and Result phases, and not during the Execution phase. Note

also that DB6 and DB7 in the MSR can be polled instead of waiting 12µs.

During the Execution phase, the Main Status Register need not be read. If the WD37C65C is in the non-DMA Mode, then the receipt of each data byte (WD37C65C is reading data from the FDD) is indicated by an interrupt signal on pin 16 (IRQ=1). The generation of a Read signal (RD = 0) clears the interrupt and sends the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13 µs for the MFM mode and 27 µs for the FM mode), then it may poll the Main Status Register and bit D7 (RQM) functions as the Interrupt signal. If a Write Command is in process then the WR signal performs the reset to the Interrupt signal.

All timings mentioned above double for mini floppy data rates.

Note that in the non-DMA mode it is necessary to examine the Main Status Register to determine the cause of the interrupt since it could be a data interrupt or a command termination interrupt, either normal or abnormal. If the WD37C65C is in the DMA mode, no interrupt signals are generated during the Execution phase. The WD37C65C generates DMA's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both DACK=0 (DMA Acknowledge) and an RD=0 (Read signal). When the DMA Acknowledge signal goes low (DACK=0), the DMA Request is cleared (DMA= 0) If a Write Command has been issued, then a WR signal will appear instead of RD. After the Execution phase has been completed (Terminal Count has occurred) or the EOT sector read/written, then an Interrupt will occur (IRQ = 1). This signifies the beginning of the Result phase. When the first byte of data is read during the Result phase, the interrupt is automatically cleared (IRQ = 0).

Note that in PC AT usage, non-DMA Host transfers are not the normal procedure. If the user chooses to do so, the WD37C65C will successfully complete commands, but will always give abnormal termination error status since TC is qualified by an inactive DACK.

The RD or WR signals should be asserted while DACK is true. The CS signal is used in conjunction with RD and WR as a gating function during programmed I/O operations. CS has no effect durinq DMA operations. If the non-DMA mode is chosen, the DACK signal should be pulled up to Vcc. Note that during the Result phase all bytes shown in the Command Table must be read. The Read Data Command, for example, has several bytes of data in the Result phase. All seven bytes must be read in order to successfully complete the Read Data command. The WD37C65C will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result phase. The WD37C65C contains five Status Registers. The Main Status Register mentioned may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and may be read only afler completing a command. The particular command that has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the WD37C65C to form the Command phase, and are read out of the WD37C65C in the Result phase, must occur in the order shown in the Command Table. The command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phases is allowed. After the last byte of data in the Command phase is sent to the WD37C65C, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result phase, the command is automatically ended and the WD37C65C is ready for a new command.

5.0 CONTROL REGISTER

The Control Register is a write only register that is used to set the data transfer rate and disable write precompensation. It provides support logic that latches the two LSBs of the data bus upon receiving LDCR and WR. CS should not be active when this happens. These bits are used to select the desired data rate, which in turn controls the internal clock generation. Clock switchover is internally "deglitched," allowing continuous operation after changing data rates. If the Control Register is not used, the data rate is governed by the supplied clock or crystal. The frequency must be 64 times the desired MFM data rate. This implies a maximum data rate of 250 kb/s for a frequency of 16 MHz or a maximum data rate of 500 Kb/s for a frequency of 32 MHz, unless the Control Register is used. Switching of this clock must be "glitchless" or the device will need to be reset. Table 1 and Table 2 present the Control Register configuration for 16 MHz and 32 MHz frequencies, respectively.

The WD37C65C optionally supports 150 kb/s FM data transfer rate. The Control Register configuration is shown in Table 3. The 150 kb/s data rate can be selected by using a 9.6 MHz XTAL or TTL level clock input on pin 26 (44pin PLCC) or pin 23 (40 pin DIP). Only two data transfer rates can be selected with this configuration: 150 kb/s FM and 300 kb/s MFM.

CR1	CR0	DRV	Data Rate	Comments	RPM (AT/EISA mode)
0	0	x	500 K	MFM	1
0	0	x	250 K	FM	1
0	1	0	250 K	MFM	0
0	1	1	300 K	MFM,(9.6 MHz XTAL)	0
1	0	x	250 K	MFM, RST Default	1
1	0	x	125 K	FM, RST Default	1
1	1	x	125 K	FM	0

TABLE 1. CONTROL REGISTER CONFIGURATION - 16 MHZ

CR1	CR0	DRV	Data Rate	Comments	RPM (AT/EISAmode)
0	0	x	1 M	MFM	1
0	0	x	500 K	FM	1
0	1	0	500 K	MFM	0
0	1	1	300 K	MFM,(9.6 MHz XTAL)	0
1	0	x	500 K	MFM, RST Default	1
1	0	x	250 K	FM,MFM,RST Default	1

TABLE 2. CONTROL REGISTER CONFIGURATION - 32 MHz

In AT/EISA mode, write precompensation can be disabled by a logic high on bit 2 of the Control Register. (See Table 4).

CR1	CR0	DRV	Data Rate	Comments	RPM (AT/EISA mode)
0	0	x	300 K	MFM	1
0	0	x	150 K	FM	1

TABLE 3. CONTROL REGISTER CONFIGURATION - OPTIONS

Bit	Signal Name & Function	Reset Condition	Clock Qualifier
0	Data Rate	0	None
1	Data Rate	0	None
2	No Write Precompensation	0	None
3-7	Reserved	None	None

TABLE 4. CONTROL REGISTER CONFIGURATION - AT/EISA MODE

6.0 MASTER STATUS REGISTER

The Master Status Register is an eight-bit, read/write register that contains the status information of the FDC. It can be accessed at any time. The WD35C65C provides a write only register, called Master Status Register 1 (MSR1) which is used only to select power down mode. In power down mode the XTAL oscillator, controller circuitry and all linear circuitry are turned off so that the controller draws very low current. Normal operation is restored by asserting reset to the WD37C65C. See Master Status Register 1.

Only the Master Status Register may be read and used to facilitate the transfer of data between the processor and WD37C65C. The DIO and RQM bits in the Master Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last RD or WR during a Command or Result phase and the setting of DIO and RQM is 12 µs if 500 kb/s MFM data rate is selected. (If 250 kb/s MFM is selected, the delay is 24 µs. If 1 Mb/s is selected, the delay is 6 µs.) For this reason, everytime the Master Status Register is read, the CPU should wait 12 µs. The maximum time from the trailing edge of the last RD in the result phase to when DB4 (FDC busy) goes low is 12 µs.

The bits in the Master Status Register are listed in Table 6. The bits in Status Register 0 are listed in Table 7.The bits in Status Register 1 are listed in Table 8.The bits in Status Register 2 are listed in Table 9.The bits in Status Register 3 are listed in Table 10.

6.1 Master Status Register 1 (MSR1--Write Only)

The WD37C65C will enter power down mode, when bit 0 of MSR1 is set to logical "1" and the following conditions are met:

1. The RST pin to the FDC is inactive.
2. Bit 2 in the Operations Register is "SRST/= 1".
3. The WD37C65C is awaiting a command from the host.

The WD37C65C can also be programmed with external logic to automatically enter power down mode a few msec after the beginning of idle mode.

Normal operation is restored when the RST pin to the FDC is active and the FDC is reset. This in turn resets bit 0 of MSR1 register to logic 0.

The bits in the Master Status Register are listed in Table 6.

Bit	Signal Name & Function	Reset Condition	Clock Qualifier
0	Power down mode (PDM)	0	None
1-7	Reserved	None	None

TABLE 5. AT/EISA MODE. MASTER STATUS REGISTER 1 CONFIG.

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
DB0	FDD 0 BUSY	D0B	FDD number is 0 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB1	FDD 1 BUSY	D1B	FDD number 1 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB2	FDD 2 BUSY	D2B	FDD number 2 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB3	FDD 3 BUSY	D3B	FDD number 3 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB4	FDC BUSY	CB	A READ or WRITE command is in progress. FDC will not accept any other command.
DB5	EXECUTION MODE	EXM	This bit is set only during Execution phase in non-DMA mode. When DB5 goes low Execution phase has ended and Results Phase has started. It operates only during non-DMA mode of operation.
DB6	DATA INPUT	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO=1, then transfer is from Data Register to the processor. If DIO=0, then transfer is from the processor to Data Register.
DB7	REQUEST FOR MASTER	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and '"direction" to the processor.

TABLE 6. MASTER STATUS REGISTER BITS

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
D7	INTERRUPT CODE	IC	D7=0 and D6=0. Normal termination of command was completed and properly executed. D7=0 and D6=1. Abnormal termination of command, (AT). Execution of command was started but was not successfully completed.
D6	---	---	D7=1 and D6=0. Invalid command issue, (IC). Command which was issued was never started.
D5	SEEK END	SE	When the FDC completes the SEEK command, this flag is set to 1 (high).
†D4	EQUIPMENT CHECK	EC	If the Track 0 signal fails to occur after 77step pulses per Recalibrate Command, then this flag is set.
†D3	NOT READY	NR	Since drive Ready is always presumed true, this will always be a logic 0.
D2	HEAD SELECT	HS	This flag is used to indicate the state of the head at interrupt.
D1	UNIT SELECT 1	US1	This flag is used to indicate a Drive Unit Number at interrupt.
D0	UNIT SELECT 0	US0	This flag is used to indicate a Drive Unit Number at interrupt.

TABLE 7. STATUS REGISTER 0 BITS

BIT NO.	NAME	SYMBOL	DESCRIPTION
D7	END OF CYLINDER	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D6	---	---	Not used. This bit is always 0 (low).
D5	DATA ERROR	DE	When the FDC detects a *CRC error in either the ID field or the data field, this flag is set.
D4	OVERRUN	OR	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D3	---	---	Not used. This bit is always 0 (low).
D2	NO DATA	ND	During execution of READ DATA, WRITE DELETED DATA, or SCAN command, if the FDC cannot find the sector specified in the **IDR Register, this flag is set. During execution of the READ ID command, if the FDC cannot read the ID field without an error, then this flag is set. During execution of the READ A TRACK command, if the starting sector cannot be found, then this flag is set.
D1	NOT WRITEABLE	NW	During execution of WRITE DATA, WRITE DELETED DATA or FORMAT A TRACK commands, if the FDC detects a $\overline{WP}$ signal from the FDD, then this flag is set.
D0	MISSING ADDRESS MARK	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. At the same time the MD (Missing Address Mark in data field) of Status Register 2 is set.

TABLE 8. STATUS REGISTER 1 BITS

BIT NO.	NAME	SYMBOL	DESCRIPTION
D7	---	---	Not Used. This bit is always 0 (low).
D6	CONTROL MARK	CM	During execution of the READ DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D5	DATA ERROR	DD	If the FDC detects a CRC error in the data field, then this flag is set.
D4	WRONG CYLINDER	WC	This bit is related to the ND bit, and when the contents of * * *C on the medium is different from that stored in the IDR, this flag is set.
D3	SCAN EQUAL	SH	During execution of the SCAN command, if the condition of "equal" is satisfied, this flag is set.
D2	SCAN NOT	SN	During execution of the SCAN command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D1	BAD CYLINDER	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF, then this flag is set.
D0	MISSING ADDRESS MARK IN DATA FIELD	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.

TABLE 9. STATUS REGISTER 2 BITS

BIT NO.	NAME	SYMBOL	DESCRIPTION
†D7	---	---	Not used. Will always be logic 0.
D6	$\overline{\text{WRITE PROTECTED}}$	$\overline{\text{WP}}$	This bit is used to indicate the status of the $\overline{\text{WRITE PROTECTED}}$ signal from the FDD.
†D5	READY	RY	This bit will always be a logic 1. Drive is presumed to be ready.
D4	TRACK 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
†D3	$\overline{\text{WRITE PROTECTED}}$	$\overline{\text{WP}}$	This bit is used by the WD37C65C to indicate the status of the $\overline{\text{WRITE PROTECTED}}$ signal from the FDD.
D2	HEAD SELECT	HS	This bit is used to indicate the status of the Side Select signal to the FDD.
D1	UNIT SELECT 1	US1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D0	UNIT SELECT 2	US0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

TABLE 10. STATUS REGISTER 3 BITS

31

* CRC - Cyclic Redundancy Check
* * IDR - Internal Data Register
* * * C - Cylinder

† - Different from NEC765

7.0 DATA REGISTER

The eight-bit Data Register stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command.

The relationship between the Master Status Register and the Data Register and the signals RD, WR, and A0 are shown in Table 11.

A0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

TABLE 11. MASTER STATUS AND DATA REGISTERS RELATIONSHIPS

8.0 OPERATIONS REGISTER

The Operations Register provides support logic that latches the data bus upon receiving LDOR and WR. CS should not be active when this happens. The Operations Register replaces the typical latched port found in floppy subsystems used to control disk drive spindle motors and to select the desired disk drive. Table 12 represents the Operations Register.

NO.	SYMBOL	DESCRIPTION
OR0	DSEL	Drive Select, if low and MOEN1 = 1, then DS1 is active. If high and MOEN2 = 1, then DS2 is active, but only in the AT/EISA mode.
OR1	(x)	This must be a logic O for DS1 and DS2 to become active.
OR2	SRST	Soft reset, active low.
OR3	DMAEN	DMA enable, active in Special and AT/EISA modes. Qualifies DMA and IRQ outputs and DACK input.
OR4	MOEN1	Motor On enable, inverted output M01 is active only in AT/EISA mode.
OR5	MOEN2	Motor On enable, inverted output M02 is active only in AT/EISA mode.
OR6	(X)	Has no defined function. A spare.
OR7	(MSEL)	Mode Select. During a soft reset condition, may be used to select between Special mode (1) and AT/EISA mode (0).

TABLE 12. OPERATIONS REGISTER

9.0 BASE, SPECIAL, AND AT/EISA MODES

Base, Special, PC AT and EISA modes allow subtle differences which the user may find desirable. The Control Register may be used in any mode without altering functionality.

9.1 Base Mode

After a hardware reset, RST active, the WD37C65C will be held in soft reset, SRST active, with the normally driven signals, DMA request and IRQ request outputs tri-stated. Base mode may be initiated at this time by a chip access by the host. Although this may be any read or write, it is strongly recommended that the Base mode user's first chip access be a read of the Master Status Register. Once Base mode is entered, the soft reset is released, and IRQ and DMA are driven. Base mode prohibits the use of the Operations Register, hence there can be no qualifying by DMAEN and no soft resets. The Drive Select outputs, DS1 to DS4, offer a 1 of 4 decoding of the Unit Select bits resident in the command structure. Pin RWC represents Reduce Write Current and is indicative of when write precompensation is necessary.

9.2 Special Mode

Special mode allows use of the Operations Register for the DMAEN signal as a qualifier and to do a software driven device reset, SRST. To enter Special mode, the Operations Register is loaded with (1 X 0 0 X 0 X X), setting mode Select to a logic 1 disabling MOEN1 and MOEN2 and causing SRST to be active. Then a read of the Control Register address, LDCR and RD, places the device in Special mode. The DS1 through DS4 is again offered in this mode, as is RWC.

9.3 AT/EISA Modes

For AT/EISA compatibility, users write to the Operations Register, LDOR and WR; this action, performed after a hardware reset, or in the Base mode, initiates AT/EISA mode. AT/EISA mode can also be entered from Special mode by loading the Operations Register with (0 X 0 0 X 0 X X), setting Mode Select to a logic 0, disabling MOEN1 and MOEN2, and causing SRST to be active. Then a read of the Control Register address sets the device into AT/EISA mode. The DS outputs are replaced with the DSEL and MOEN signals buffered from the Operations Register. DMAEN and SRST are supported and compatible with the current BIOS. RWC pin function is now RPM so that users with two-speed drives may reduce spindle speed from a nominal 360 revolutions per minute to 300 revolutions per minute when active low. It can also be used to reduce write current when a slower data rate is selected for a given drive. Figure 3 illustrates the relationship among the three modes.

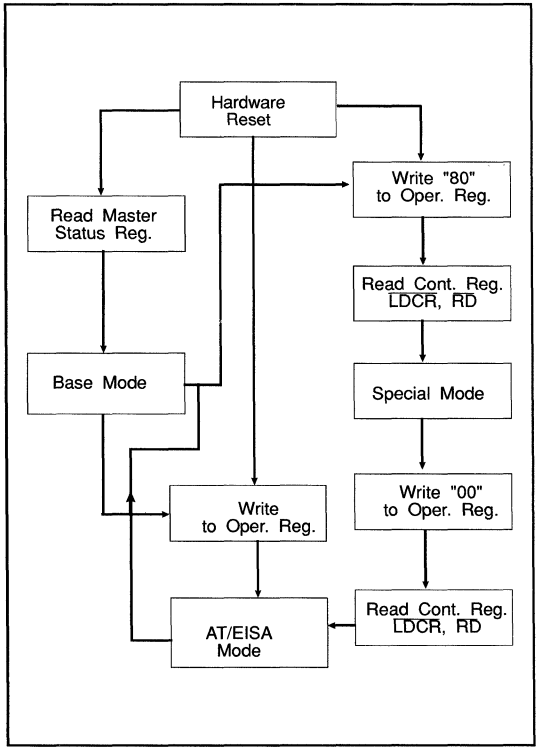


FIGURE 3. FLOW DIAGRAM BASE, SPECIAL & AT/EISA MODES

10.0 POLLING ROUTINE

After any reset the WD37C65C, (a hard RST or soft SRST), will automatically go into a Polling routine. In between commands (and between step pulses in the SEEK Command), the WD37C65C polls all four FDDs looking for a change in the Ready line from any of the drives. Since the drive is always presumed Ready, an interrupt will only be generated following a reset. This occurs because a reset forces Not Ready status, which then promptly becomes Ready. Note that in Special, AT/EISA modes, if DMAEN is not valid 1ms after reset goes inactive, then IRQ may be already set and pending when finally enabled onto the bus. The polling of the Ready line by the WD37C65C occurs continuously between commands. Each drive is polled every 1.024ms, except during the READ/WRITE commands. For mini-floppies, the polling rate is 2.048ms. The drive polling sequence is 1-2-4-3. Note that in the AT/EISA mode, the user will not see the polling at the Drive Select signals. Figure 4 illustrates the Drive Select Polling Timing.

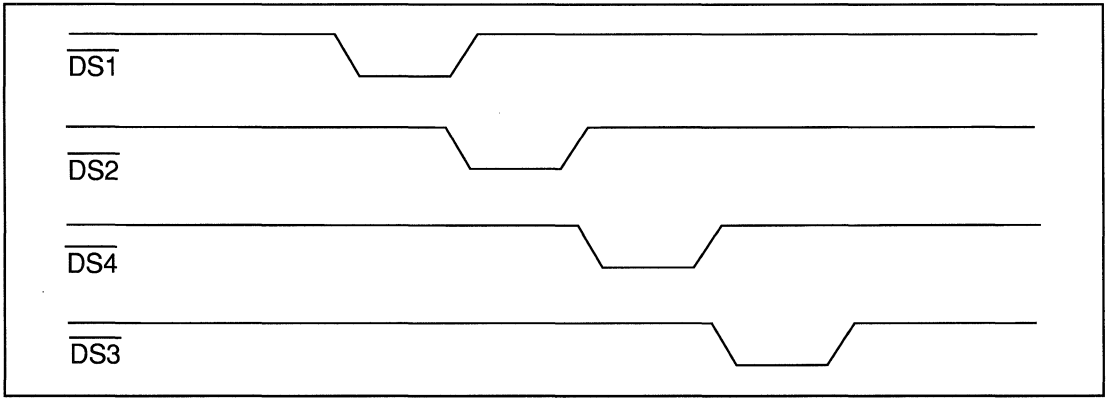


FIGURE 4. DRIVE SELECT POLLING TIMING

11.0 DEVICE RESETS

The WD37C65C supports both hardware reset (RST) pin (19) and a software reset (SRST) through use of the Operations Register. The RST pin will cause a device reset for the active duration. RST causes a default to Base mode, and selects 250kb MFM (or 125kb FM, code dependent) as the data rate (16 MHz input clock). The default data rate for a 32 MHz input clock is 500kb MFM. SRST will reset the microcontroller as did the RST, but will not affect the current data rate selection or the mode. RST, when active, will disable the high current driver outputs to the disk drive. RST and SRST will not affect the values set for the internal timers - HUT, HTL, and SRT.

If the XTAL oscillators are used, instead of the TTL driven clock inputs, the hardware RST active time requirement will be extended. The oscillator circuit is designed so that RST will bootstrap the circuit into guaranteed oscillation in a fixed amount of time. The extended reset time allows the growth of the oscillation to produce stable internal clock timing.

12.0 DATA SEPARATOR

The Data Separator is a WD92C32 Digital Phase Lock Loop Floppy Disk Data Separator (DPLL). It was designed to address high performance error rates on floppy disk drives, and to provide superior performance in terms of available bit jitter tolerance. It contains the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Figure 1 illustrates the WD92C32 used as the Data Separator in the WD37C65C system. Figure 5 illustrates the WD92C32 simplified block diagram. The bit jitter tolerance for the data separator is 60%, which guarantees an error rate of <10E-9.

13.0 WRITE PRECOMPENSATION

The WD37C65C maintains the standard first level algorithm to determine when write precompensation should be applied. The EARLY and LATE signals are used internally to select the appropriate delay in the write data pulse stream. The encoded WRITE DATA signal is synchronized to the 16 MHz or 32 MHz clock if this is the frequency on CLK1 pin (23), and clocked through a shift register. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexer gates the chosen bit to the output. The output data pulse width has a 25% duty cycle, i.e., one fourth of the bit cell period, and equal to one half the WCLK period.

When PCVAL pin (24) = 1, all data will be precompensated by ± 125ns, regardless of track number and data rate. However, this is only for MFM encoding. There is no write precompensation for FM. If PCVAL = 0, and if a track inside number 28 is accessed, then ± 187ns precompensation will be generated. For frequencies other than 16 MHz or 32 MHz on the CLK1 pin, the precompensation values will be two and three clock cycles respectively.

When the non-standard 300 kb/s data rate using CLK2 is chosen, the MFM precompensation will always be two clock cycles. For 9.6 MHz, this is ± 208ns. In this case, the PCVAL function is disabled.

Write precompensation can be disabled by bit 2 of the Control Register for the AT/EISA. The PCVAL input to WD37C65C is ignored if there is no write precompensation.

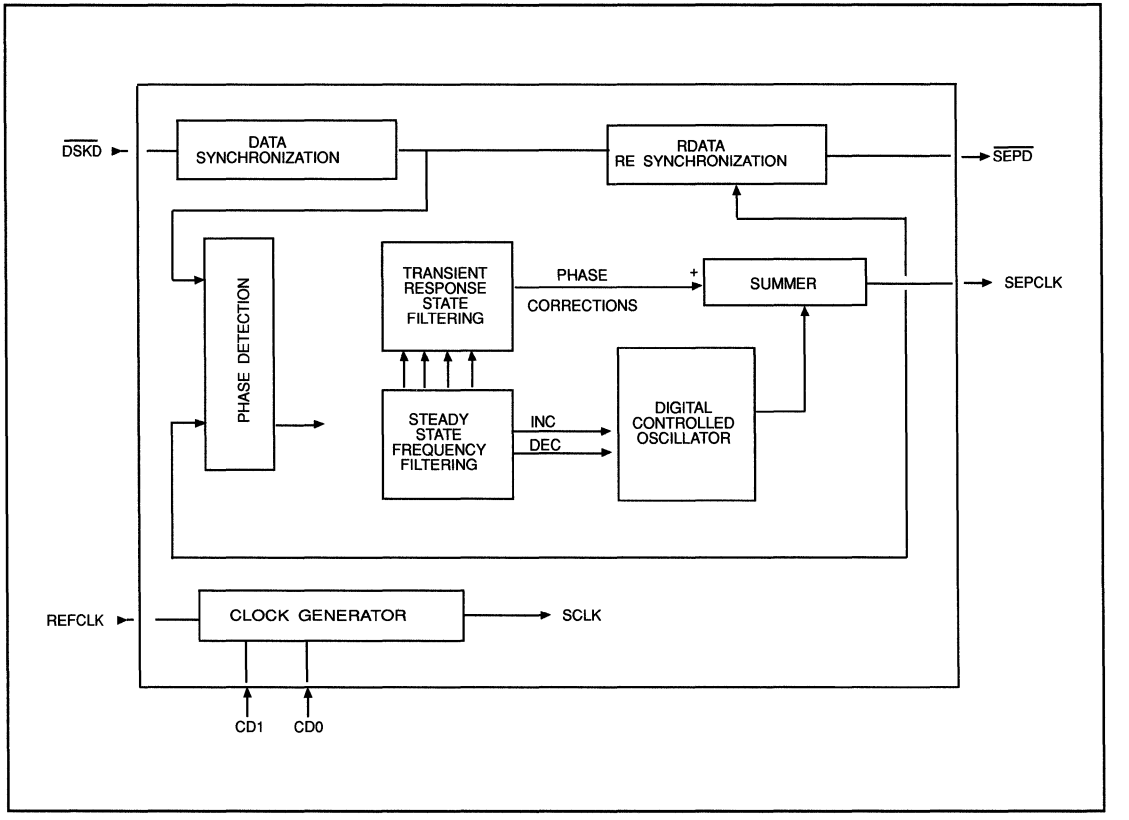


FIGURE 5. WD92C32 SIMPLIFIED BLOCK DIAGRAM

14.0 CLOCK GENERATION

This logical block provides all the clocks needed by the WD37C65C. They are: Sampling Clock (SCLK), Write Clock (WCLK), and the Master Clock (MCLK).

SCLK drives the WD92C32 Data Separator used during data recovery. This clock's frequency is always 32 times the selected data rate.

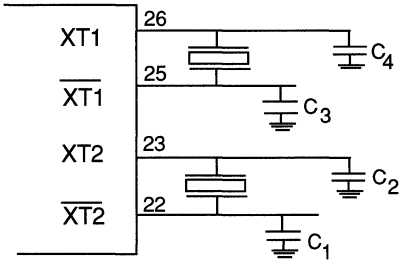
WCLK is used by the encoder logic to place MFM or FM on the serial WD-stream to the disk. WCLK always has a frequency two times the selected data rate.

MCLK is used by the microsequencer. MCLK and MCLK clock all latches in a two-phase scheme. One microinstruction cycle is four MCLK cycles. MCLK has a frequency equal to eight times the selected MFM data rate or 16 times the FM data rate. Table 13 presents the Clock Data Rate. Figure 6 illustrates the XTAL oscillator circuits for the 44 pin PLCC configuration.

In power down mode the XTAL oscillator and the clock circuitry are turned off.

DATA RATE	CODE	SCLK MHz	MCLK MHz	WCLK
1 Mb/s	MFM	32.0	8.0	2.0 MHz
500 kb/s	MFM	16.0	4.0	1.0 MHz
500 kb/s	FM	16.0	8.0	1.0 MHz
250 kb/s	FM	8.0	4.0	500 KHz
250 kb/s	MFM	8.0	2.0	500 KHz
125 kb/s	FM	4.0	2.0	250KHz
300 kb/s	MFM	9.6	2.4	600 KHz

TABLE 13. CLOCK DATA RATE



SERIES RESONANT
XT2

9.6 MHz ± 100 ppm
R series = 30 ohm max
C shunt = 10 pf max
C1 = 68 pf 5% mica
C2 = 56 pf 5% mica

SERIES RESONANT
XT1

16.0 MHz ± 100 ppm		32 MHz ± ppm	
R series	= 30 ohm max	R series	= 47.2 ohm
C shunt	= 10 pf max	C shunt	= 2 pf max
C3	= 47 pf 5% mica	C3	= 30 pf 5% mica
C4	= 15 pf 5% mica	C4	= 30 pf 5% mica

FIGURE 6. CRYSTAL OSCILLATOR CIRCUITS FOR 44 PIN PLCC

15.0 COMMAND PARAMETERS

The WD37C65C is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor. The results after execution of the command may also be a multibyte transfer back to the processor. The commands consist of three phases: Command phase, Execution phase, and the Result phase.

Command phase - The Floppy Disk Controller (FDC) receives all information required to perform a particular operation from the processor

Execution phase - The FDC performs the operation it was instructed to do.

Result phase - After completion of the operation, status and other housekeeping information are made available to the processor.

Table 14 lists the 15 WD37C65C commands.

READ DATA
READ DELETED DATA
WRITE DATA
WRITE DELETED DATA
READ A TRACK
READ ID
FORMAT A TRACK
SCAN EQUAL
SCAN LOW OR EQUAL
SCAN HIGH OR EQUAL
RECALIBRATE
SENSE INTERRUPT STATUS
SPECIFY
SENSE DRIVE STATUS
SEEK

TABLE 14. WD37C65C COMMANDS

Tables 15 through 29 are presented to show the required parameters and results for each command. Most commands require nine command bytes and return seven bytes during the result phase. The "W" to the left of each byte indicates a command phase byte to be written. An "R" indicates a result byte.

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to
	W	H	H	H	H	H	H	H	H	command execution. The four
	W	R	R	R	R	R	R	R	R	bytes are compared against
	W	N	N	N	N	N	N	N	N	header on floppy disk.
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after com-
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	mand execution.
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after com-
	R	R	R	R	R	R	R	R	R	mand execution.
	R	N	N	N	N	N	N	N	N	

TABLE 15. READ DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to
	W	H	H	H	H	H	H	H	H	command execution. The four
	W	R	R	R	R	R	R	R	R	bytes are compared against
	W	N	N	N	N	N	N	N	N	header on floppy disk.
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after com-
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	mand execution.
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after com-
	R	R	R	R	R	R	R	R	R	mand execution.
	R	N	N	N	N	N	N	N	N	

TABLE 16.READ DELETED DATA

31

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to
	W	H	H	H	H	H	H	H	H	command execution. The four
	W	R	R	R	R	R	R	R	R	bytes are compared against
	W	N	N	N	N	N	N	N	N	header on floppy disk.
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after com-
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	mand execution.
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after com-
	R	R	R	R	R	R	R	R	R	mand execution.
	R	N	N	N	N	N	N	N	N	

TABLE 17. WRITE DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to
	W	H	H	H	H	H	H	H	H	command execution. The four
	W	R	R	R	R	R	R	R	R	bytes are compared against
	W	N	N	N	N	N	N	N	N	header on floppy disk.
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after com-
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	mand execution.
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after com-
	R	R	R	R	R	R	R	R	R	mand execution.
	R	N	N	N	N	N	N	N	N	

TABLE 18. WRITE DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US1	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to
	W	H	H	H	H	H	H	H	H	command execution.
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system. FDD reads all data fields from index hole to EOT.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after com-
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	mand execution.
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after com-
	R	R	R	R	R	R	R	R	R	mand execution
	R	N	N	N	N	N	N	N	N	

TABLE 19. READ A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
EXECUTION										The first correct ID information on the cylinder is stored in Data Register.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information read during
	R	R	R	R	R	R	R	R	R	Execution Phase from floppy
	R	N	N	N	N	N	N	N	N	disk.

TABLE 20. READ ID

31

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	N	N	N	N	N	N	N	N	Bytes/Sector
	W	SC	SC	SC	SC	SC	SC	SC	SC	Sectors/Track
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	Gap 3
	W	D	D	D	D	D	D	D	D	Filler Byte
EXECUTION										Floppy Disk Controller (FDC) formats an entire track.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	In this case, the ID information
	R	R	R	R	R	R	R	R	R	has no meaning.
	R	N	N	N	N	N	N	N	N	

TABLE 21. FORMAT A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	STP	STP	STP	STP	STP	STP	STP	STP	
EXECUTION										Data compared between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution.
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 22. SCAN EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	STP	STP	STP	STP	STP	STP	STP	STP	
EXECUTION										Data compared between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 23. SCAN LOW OR EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to
	W	H	H	H	H	H	H	H	H	command execution.
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	STP	STP	STP	STP	STP	STP	STP	STP	
EXECUTION										Data compared between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after com-
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	mand execution.
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after com-
	R	R	R	R	R	R	R	R	R	mand execution.
	R	N	N	N	N	N	N	N	N	

TABLE 24. SCAN HIGH OR EQUAL

31

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
EXECUTION										Head retracted to Track zero.

TABLE 25. RECALIBRATE

The WD37C65C issues 77 step pulses, the same as the NEC765.

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	0	0	0	Command Codes
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information about the FDC
	R	PCN	PCN	PCN	PCN	PCN	PCN	PCN	PCN	at the end of seek operation

TABLE 26. SENSE INTERRUPT STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W W W	0 SRT HLT	0 SRT HLT	0 SRT HLT	0 SRT HLT	0 HUT HLT	0 HUT HLT	1 HUT HLT	1 HUT ND	Command Codes

TABLE 27. SPECIFY

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W W	0 X	0 X	0 X	0 X	0 X	0 HS	0 US1	0 US0	Command Codes
RESULTS	R	ST3	ST3	ST3	ST3	ST3	ST3	ST3	ST3	Status information about the FDC.

TABLE 28.SENSE DRIVE STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W W W	0 X NCN	0 X NCN	0 X NCN	0 X NCN	1 X NCN	1 HS NCN	1 US1 NCN	1 US0 NCN	Command Codes
EXECUTION										Head is positioned over proper cylinder on the diskette.

TABLE 29. SEEK

Table 30 defines, in alphabetical order, the symbols used in Command Tables 15 through 29.

SYMBOL	NAME	DESCRIPTION
A0	ADDRESS LINE 0	A0 controls selection of Main Status Register (A0=0) or Data Register (A0=1).
C	CYLINDER NUMBER	C stands for the current/selected cylinder (track) numbers 0 through 255 of the medium.
D	DATA	D stands for the data pattern which is going to be written into a sector.
D7 - D0	DATA BUS	8-bit DATA BUS, where D7 stands for a most significant bit, and D0 stands for a least significant bit.
DTL	DATA LENGTH	When N is defined as 00, DTL stands for the DATA LENGTH which users are going to read out or write into the sector.
EOT	END OF TRACK	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL	GAP LENGTH	GPL stands for the length of Gap 3. During the FORMAT Command, it determines the size of Gap 3.
H	HEAD ADDRESS	H stands for head number 0 or 1 as specified in the ID field.
HLT	HEAD LOAD TIME	HLT stands for the HEAD LOAD TIME in FDD (2 to 254ms in 2ms increments).
HS	HEAD SELECT	HS stands for a selected head number 0 or 1 and controls the polarity of pin 25 (in 40 pin DIP) or pin 28 (in 44 pin PLCC).
HUT	HEAD UNLOAD TIME	HUT stands for the HEAD UNLOAD TIME after a Read or Write operation has occurred (16 to 240ms in 16ms increments).
MF	FM or MFM	If MF is low, FM mode is selected. If it is high, MFM mode is selected.
MT	MULTITRACK	If MT is high, a MULITRACK operation is performed. If MT=1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N	NUMBER	N stands for the NUMBER of data bytes written in a sector.
NCN	NEW CYLINDER NUMBER	NCN stands for a NEW CYLINDER NUMBER which is going to be reached as a result of the Seek operation. Desired position of head.
ND	NON-DMA MODE	ND stands for operation in the NON-DMA MODE.
PCN	PRESENT CYLINDER	PCN stands for the cylinder number at the completion of the SENSE INTERRUPT STATUS Command. Position of head at present time.

TABLE 30. COMMAND SYMBOL DESCRIPTIONS

SYMBOL	NAME	DESCRIPTION
R	RECORD	R stands for the sector number which will be read or written.
R/W	READ/WRITE	R/W stands for either READ or WRITE signal.
SC	SECTOR	SC indicates the number of sectors per cylinder.
SK	SKIP	SK stands for SKIP Deleted Data Address mark.
SRT	STEP RATE TIME	SRT stands for the Stepping Rate for the FDD (1 to 16ms in 1ms increments). Stepping Rate applies to all drives. In 2's complement format, F(Hex)=1ms, E(Hex)=2ms, etc.
ST0 ST1 ST2 ST3	STATUS 0 STATUS 1 STATUS 2 STATUS 3	ST0-3 stands for one of four registers which store the STATUS information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0=0). ST0-3 may be read only after a command has been executed and contains information relevant to that particular command.
STP	---	During a SCAN operation, if STP=1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP=2, then alternate sectors are read and compared.
US0,US1	UNIT SELECT	US stands for a selected drive; binary encoded, 1 of 4.

TABLE 30. COMMAND SYMBOL DESCRIPTIONS (CONT'D)

16.0 COMMAND DESCRIPTIONS

16.1 Read Data

A set of nine byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number("R") stored in the ID Register(IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon MT (multitrack), MF (MFM/FM), and N (number of bytes/sector). Table 31 lists the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes /Sector N	Maximum Transfer Capacity (Bytes/Sector) Number of Sectors	Final Sector Read From Diskettes
0	0	00	(128)(26)=3,328	26 at Side 0 or
0	1	01	(256)(26)=6,656	26 at Side 1
1	0	00	(128)(52)=6,656	26 at Side 1
1	1	01	(256)(52)=13,312	
0	0	01	(256)(15)=3,840	15 at Side 0
0	1	02	(512)(15)=7,680	
1	0	01	(256)(30)=7,680	15 at Side 1
1	1	02	(512)(15)=15,360	
0	0	02	(512)(8)=4,096	8 at Side 1 or
0	1	03	(1024)(8)=8,192	8 at Side 1
1	0	02	(512)(16)=8,192	8 at Side 1
1	1	03	(1024)(16)=16,384	

TABLE 31. TRANSFER CAPACITY

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskene. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond DTL in the sector is not sent to the Data Bus. The FDC reads (internally) the complete sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read operation. When N is non-zero, then DTL has no meaning and should be set to FF hexidecimal.

At the completion of the Read Data command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify command) has elapsed. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in 'R'), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to 1 (high). If a CRC error occurs in the Data Field, the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data command, after reading all the data in the sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 µs in the FM mode, and every 13 µs in the MFM mode, or the FDC sets the OR (Overrun) flag in Status Register

1 to a 1 (high), and terminates the Read Data command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result phase is dependent upon the state of the MT bit and EOT byte. Table 32 shows the values for C, H, R, and N, when the processor terminates the command.

MT	HD	Final Sector Transferred to Procesor	ID Information at Result Phase C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
0	0	Equal to EOT	C+1	NC	R=0	NC
0	1	Less than EOT	NC	NC	R+1	NC
0	1	Equal to EOT	C+1	NC	R=0	NC
1	0	Less than EOT	NC	NC	R+1	NC
1	0	Equal to EOT	NC	LSB	R=0	NC
1	1	Less than EOT	NC	NC	R+1	NC
1	1	Equal to EOT	C+1	LSB	R=0	NC

TABLE 32. C, H, R, AND N VALUES

Notes:
NC (No Change): The same value as the one at the beginning of command execution.
LSB (Least Significant bit): The least significant bit of H is complemented.

16.2 Write Data

A set of nine bytes is required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the sector number stored in 'R' is incremented by one, and the next data field is written into. The FDC continues this 'Multisector Write Operation' until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data command for details:

- Transfer capacity
- EN (End of Cylinder) flag
- ND (No Data) flag
- Head Unload Time interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N ≠0

In the Write Data mode, data transfers between the processor and FDC via the data bus, must occur every 27 µs in the FM mode and every 13 µs in the MFM mode. If the time interval between data transfers is longer than this, then the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

16.3 Write Deleted Data

This command is the same as the Write Data command except a Deleted Data Address mark is written at the beginning of the data field instead of the normal Data Address mark.

16.4 Read Deleted Data

This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field (and SK = 0 [low]), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address mark and reads the next sector.

16.5 Read A Track

This command is similar to the Read Data command except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track.

The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multitrack or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID Address mark on the diskette after it senses the index hold for the second time, it sets the MA (Missing Address mark) flag in Status Register 1 to a 1 (high) and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

16.6 Read ID

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, then the MA (Missing Address mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

16.7 Format A Track

The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; Gaps, Address marks, ID fields and data fields, all per the IBM System 34 (double density) or System 3740 (single density) format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (gap length), and D (data pattern) which are supplied by the processor during the Command phase. The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (cylinder number), H (head number), R (sector number) and N (number of bytes/sector). This allows the diskette to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the WD37C65C for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the Interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by 1 after each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formaning continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

Table 33 shows the relationship between N, SC, and GPL for various sector sizes.

Format	Sector Size Bytes/sector	N	SC	GPL 1	GPL 2,3
8" Standard Floppy					
FM Mode	128	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5 1/4" Minifloppy					
FM Mode	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3 1/2" Sony Microfloppy					
FM Mode	128	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

TABLE 33. N, SC AND GPL RELATIONSHIP

Notes:
1. Suggested values of GPL in Read 0, Write commands to avoid splice point between data field and ID field of contiguous sections.
2. Suggested values of GPL in format command.
3. All values except sector size are hexadecimal.
4 In MFM mode FDC cannot perform a Read/Write/format operation with 126 bytes/sector. (N=00)

16.8 Scan Commands

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP -8 R), and the scan operation is continued. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high) and terminates the Scan command. The receipt of a Terminal Count signal from the processor or DMA controller durring the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and then to terminate the command. Table 34 shows the status of bits SH and SN under various conditions of Scan.

Command	Status Register 2 Bit 2=SN	Bit 3=SH	Comments
Scan Equal	0	1	$D_{FFD}=D$ Processor
Scan Equal	1	0	$D_{FFD}\neq D$ Processor
Scan Low or Equal	0	1	$D_{FFD}=D$ Processor
Scan Low or Equal	0	0	$D_{FFD}<D$ Processor
Scan Low or Equal	1	0	$D_{FFD}>D$ Processor
Scan Low or Equal	0	1	$D_{FFD}=D$ Processor
Scan High or Equal	0	0	$D_{FFD}>D$ Processor
Scan High or Equal	1	0	$D_{FFD}<D$ Processor

TABLE 34. STATUS OF BITS SH AND SN

If the FDC encounters a Deleted Data Address mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (Control mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address mark and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control mark) flag of Status Register 2 to a 1 (high) in order to show that a deleted sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read or the MT (Multitrack) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, the following will happen: sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the index hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA controller for comparison against the data read from the diskette. In order to avoid having the OR (Overrun) flag set in Status Register 1, it is necessary to have the data available in less than 27 µs (FM mode) or 13 µS (MFM mode). If an Overrun occurs, the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

16.9 Seek

The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent Present Cylinder Registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to a 1 (high), and step pulses are issued. (Step In)

PCN > NCN: Direction signal to FDD set to a 0 (low), and step pulses are issued. (Step Out)

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued NCN is compared against PCN, and when NCN = PCN, the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits D_0B-D_3B in the Main Status Register are set during the Seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the FDC is in the FDC Busy state; but during the Execution phase, it is in the non-busy state. While the FDC is in the non-busy state, another Seek command may be issued, and in this manner parallel Seek operations may be done on up to four drives at once. No other command can be issued as long as the FDC is in the process of sending step pulses to any drive.

If the time to write three bytes of Seek command exceeds 150 µS, the timing between the first two step pulses may be shorter than that set in the Specify command by as much as 1ms.

16.10 Recalibrate

The function of this command is to retract the Read/Write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and step pulses are issued. When the Track 0 signal goes high, the SE (Seek End) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 255 step pulses have been issued, (for the WD37C65

and the WD37C65A) or 77 step pulses (WD37C65B/C), the FDC sets the SE (Seek End) and EC (Equipment Check) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also applies to the Recalibrate command.

16.11 Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Cylinder command
   g. Write Deleted Data command
   h. Scan commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate command
4. During Execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an Execution phase in non-DMA mode, DB5 in the Main Status Register is high. Upon entering the Result phase, this bit gets cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by Reading/Writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command, when issued, resets the Interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

Seek End Bit 5	Interrupt Code Bit 6	Bit 7	Cause
0	1	1	Ready Line changed state, either polaritv
1	0	0	Normal Termination of Seek or Recalibrate command
1	1	0	Abnormal Termination of Seek or Recalibrate command

TABLE 35. INTERRUPT CAUSE

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no Result phase. When the disk drive has reached the desired head position, the WD37C65C will set the Interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives. See Figure 7.

The Specify command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240ms in increments of 16ms (01 = 16ms, 02 =32 ms . . . $0F_{16}$ = 240ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1ms, E = 2ms, D = 3ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2ms, 02 = 4ms, 03 = 6ms . . . 7F = 254ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 23). Times indicated above are for a 16MHz clock; if the clock was reduced to 8MHz, then all time intervals are increased by a factor of 2. If the clock was increased to 32 MHz, then all time intervals are decreased by half.

The choice of DMA or non-DMA operation is made by the ND (Non-DMA) bit. When this bit is high (ND = 1), the Non-DMA mode is selected; and when ND = 0, the DMA mode is selected.

16.12 Sense Drive Status

This command may be used by the processor to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

16.13 Invalid

If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status Register are both high (1), indicating to the processor that the WD37C65C is in the Result phase and the

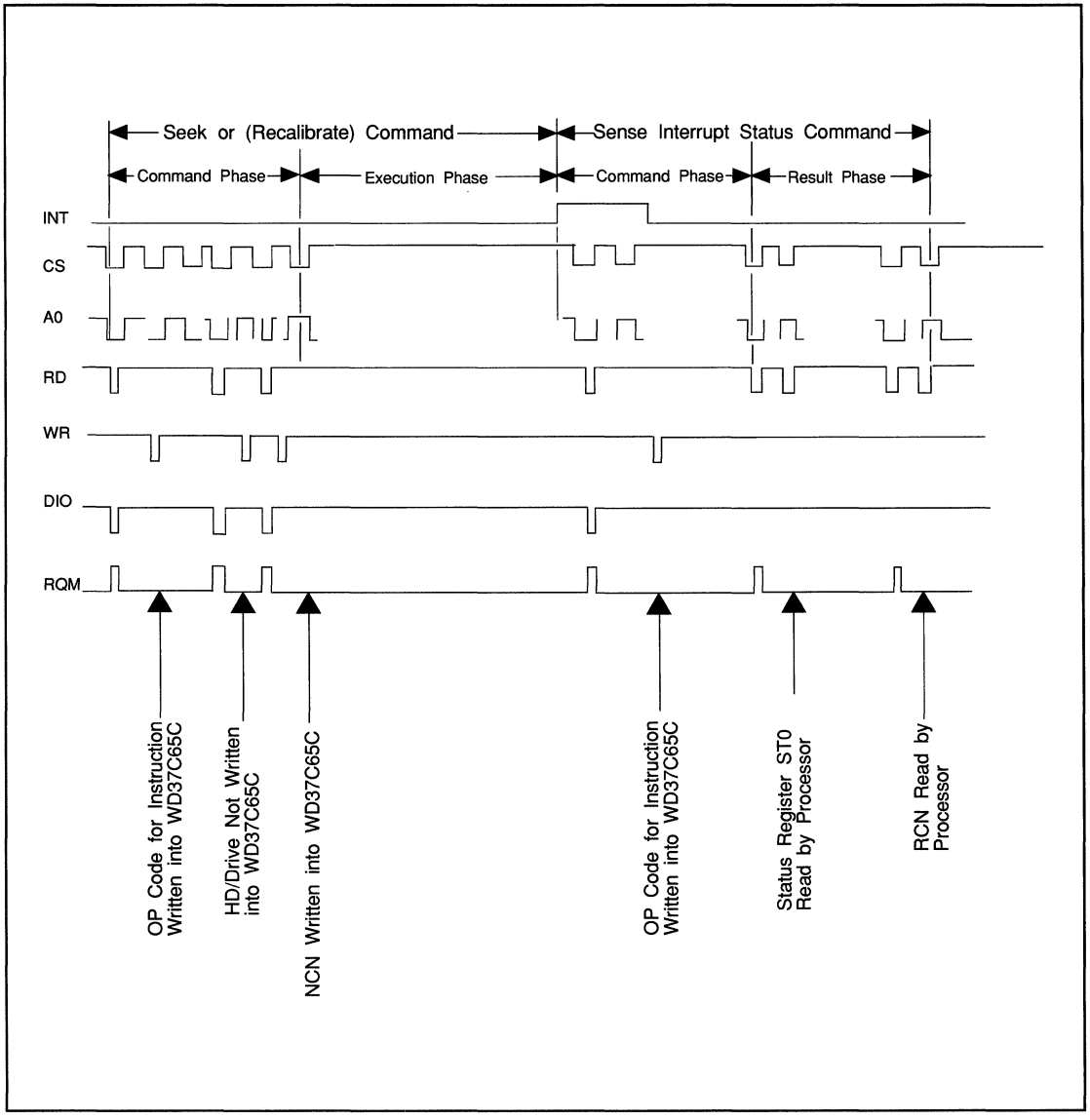


FIGURE 7. SEEK, RECALIBRATE, AND SENSE INTERRUPT

contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0, it will find an 80 hex, indicating an Invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt; otherwise the FDC will consider the next command to be an invalid command. In some applications, the user may wish to use this command as a No-Op command to place the FDC in a standby or No Operation state.

GAP4a	SYNC	IAM	GAP 1	SYNC	IDAM	C		S		C	GAP 2	SYNC	DATA AM	DATA	C	GAP 3	GAP4b
40x	6x		26x	6x		Y	H	E	N	R	11x	6x		1	R	1	
FF	00	FC	FF	00	FE	L	D	C	O	C	FF	00	FB or F8		C		

Index ⟵ Repeat N Times ⟶

FIGURE 8. WD37C65C FM MODE FORMAT

GAP4a	SYNC	IAM		GAP 1	SYNC	IDAM		C		S		C	GAP 2	SYNC	DATA AM		DATA	C	GAP 3	GAP4b
80x	12x	3x		50x	12x	3x		Y	H	E	N	R	22x	12x	3x	FB	1	R	1	
FF	00	C2	FC	FF	00	A1	FE	L	D	C	O	C	E	00	A1	F8		C		

Index ⟵ Repeat N Times ⟶

FIGURE 9. WD37C65C MFM MODE FORMAT

No.	WD37C65/A/B	WD37C65/C
1.	2 XTAL oscillators. - 16 MHz for standard data rate (up to 500kb/s MFM). - 9.6 MHz for non-standard rate. (300 kb/s PCAT)	2 XTAL oscillators. - 32 MHz for standard data rate (up to 1 Mb/s MFM) or 16 MHz for standard data rate (up to 500kb/s MFM). - 9.6 MHz for non-standard rate. (300 kb/s AT/EISA)
2.	Supports data rate up to 500 Kb/s.	Supports data rate up to 1 Mb/s
3.	Does not support power down mode.	Supports power down mode feature, standby ICC = 100 µA max.
4.	PCVAL pin for selecting the precomp values.	PCVAL pin for selecting the precomp values and a feature to disable write precomp.

TABLE 36. DIFFERENCES BETWEEN WD37C65/A/B AND WD37C65C

17.0 ELECTRICAL CHARACTERISTICS

17.1 Absolute Maximum Ratings

Operating Temperature	0°C (32°F) to 70°C (158°F)
Storage Temperature	-55°C (-67°F) to +125°C (257°F)
Voltage on any pin with respect to ground	-0.3V to VCC +0.3V
Supply Voltage with respect to ground	7V

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

17.2 Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to ground.

Operating temperature range (TA)	0°C (32°F) to 70°C (158F)
Power supply voltage (VCC)	+5V ± 10%

17.3 DC Operating Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS
VCC	+5VDC Power Supply	4.5	5.5	V
VIL	Input Low Voltage - Data Bus & XTOSC	---	0.8	V
VIH	Input High Volt - Data Bus & XTOSC	2.0	---	V
VILT	Input Low Threshold - Schmitt Trigger	0.8	1.1	V
VIHT	Input High Threshold - Schmitt Trigger	1.7	2.0	V
VHYS	Schmitt Trigger Hysterisis	0.45	---	V
VOL	Output Low- DBx,IRQ,DMA,; Io = 24.0mA	---	0.4	V
VOH	Output High - DBx,IRa,DMA,; Io = -5.0mA	2.8	---	V
VOLHC	Output Low - High Current; Io = 48.0mA	---	0.4	V
ILUL	Latch Up Current Low	40.0	---	mA

SYMBOL	PARAMETER	MIN	MAX	UNITS
ILUH	Latch Up Current High	-40.0	---	mA
ILL	Leakage Current Low	---	10.0	µA
ILH	Leakage Current High	---	-10.0	µA
ICC	Supply Current - 100 µA Source Loads	---	60.0	mA
ICCHL	Supply Current - 5.0 mA Source Loads	---	120.0	mA
ICCPDM	Supply Current in Power Down Mode	---	100.0	µA[1]
PD	Power Dissipation- ICC Max	---	600.0	mW[3]
PDHL	Power Dissipation - ICCHL Max	---	750.0	mW[2,3]
VPQR	Power Qualified Reset Threshold	2.8	4.35	V

Note 1. Vin = VCC or GND, Io = O mA.

Note 2. Includes DBx, IRQ and DMA; Io = -5.0 mA source loads.

Note 3. Includes open drain high current drivers at Vol = 0.4V.

18.0 AC TIMING CHARACTERISTICS

The following notes apply to all parameters presented in this section:

1. TA = 0°C (32°F) to 70°C (158°F)
2. VCC = +5V ± 10%
3. CL = 100 pf
4. CY = CLK1 or XT1 period
5. MCY = MCLK period, dependent on selected data rate
6. WCY = WCLK period, dependent on selected data rate

SYMBOL	PARAMETER	MIN	MAX	UNITS
tCY	Clock Period	31	---	nS
tPH	Clock Active (High or Low)	13.5	---	nS
tR	Clock Rise Time (Vin 0.8 to 2.0)	---	2	nS
tF	Clock Fall Time (Vin 2.0 to 0.8)	---	2	nS
tAR	A0,$\overline{CS}$,$\overline{DACK}$ Set Up Time to $\overline{RD}$ Low	0	---	nS
tRA	A0,$\overline{CS}$,$\overline{DACK}$ Hold Time to RD High	0	---	nS
tRR	$\overline{RD}$ Width	90	---	nS
tRD	Data Access Time From $\overline{RD}$ Low	---	90	nS
tDF	DB To Float Delay From $\overline{RD}$ High	10	65	nS
tAW	A0,$\overline{CS}$,$\overline{DACK}$,$\overline{LDCR}$,$\overline{LDOR}$, Set Up Time To $\overline{WR}$ Low	0	---	nS
tWA	A0,$\overline{CS}$,$\overline{DACK}$,$\overline{LDCR}$,$\overline{LDOR}$, Hold Time From $\overline{WR}$ High	0	---	nS
tWW	$\overline{WR}$ Width	60	---	nS
tDW	Data Set Up Time To $\overline{WR}$ High	80	---	nS
tWD	Data Hold Time From $\overline{WR}$ High	0	---	nS
tRI	IRQ Reset Delay Time From $\overline{RD}$ High			1MCY +150nS
tWI	IRQ Reset Delay Time From $\overline{WR}$ High			1MCY +150nS
tMCY	DMA Cycle Time	52		MCY
tAM	DMA Reset Delay Time From $\overline{DACK}$ Low	---	140	nS
tMA	$\overline{DACK}$ Delay Time From DMA High	0	---	nS
tAA	$\overline{DACK}$ Width	90	---	nS
tTC	TC Width	60	---	nS
tRST	Reset Width - TTL Driven CLK1	60	---	nS
tSRST	Reset Width - Software Reset	5	---	MCY
tRDD	$\overline{RDD}$ Active Time Low	40	---	nS
tWDD	$\overline{WD}$ Write Data Width Low	1/2 (TYP)	---	WCY
tDST	$\overline{DIRC}$ Hold & Set Up To $\overline{STEP}$ Low	4	---	MCY
tSTU	$\overline{DSX}$ Hold Time From $\overline{STEP}$ Low	20	---	MCY
tSTP	$\overline{STEP}$ Active Time Low	24	---	MCY
tSC	$\overline{STEP}$ Cycle Time	132	---	MCY
tSTD	$\overline{DIRC}$ Hold Time After $\overline{STEP}$	96	---	MCY
tIDX	$\overline{IDX}$ Index Pulse Width	2	---	MCY
tMR	$\overline{RD}$ Delay From DMA	0	---	nS

31

SYMBOL	PARAMETER	MIN	MAX	UNITS
tMW	$\overline{WR}$ Delay From DMA	0	---	nS
tMRW	$\overline{RD}$ Or $\overline{WR}$ Response From DMA High	---	48	MCY
tCA	Chip Access Delay From RST Low - TTL	32	---	MCY
tCAS	Chip Access Delay From tSRST Low	40	---	MCY
tXCA	Chip Access Delay From RST-OSC XT1 at 16 MHz	500	---	µS
tXTS	XT2 Access Delay After RST 9.6 MHz	1000	---	µS
tTCR	TC Delay From Last DMA Or IRQ, $\overline{RD}$	0	192	MCY
tTCW	TC Delay From DMA Or IRQ, $\overline{WR}$	0	384	MCY
Tcycle	Clock Cycle	60	---	nS
Tp-high	Clock High	25	---	nS
Tp-low	Clock Low	25	---	nS
Trise	Rise Time	---	5	nS; Vin .8 to 2.0
Tfall	Fall Time	---	5	nS; Vin 2.0 to .8

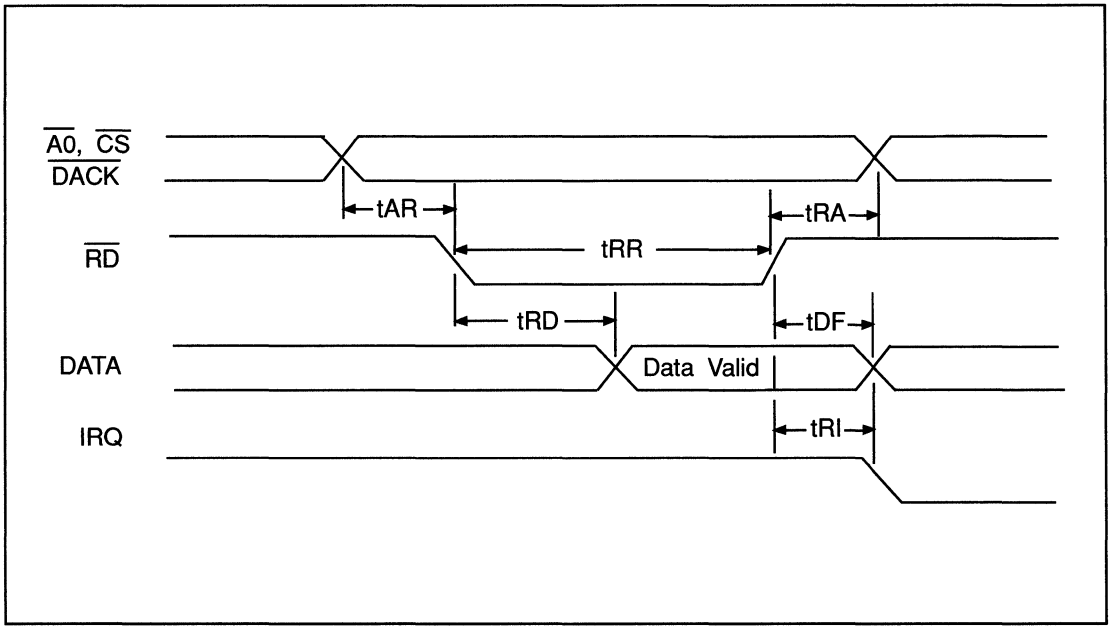


FIGURE 10. READ TIMING

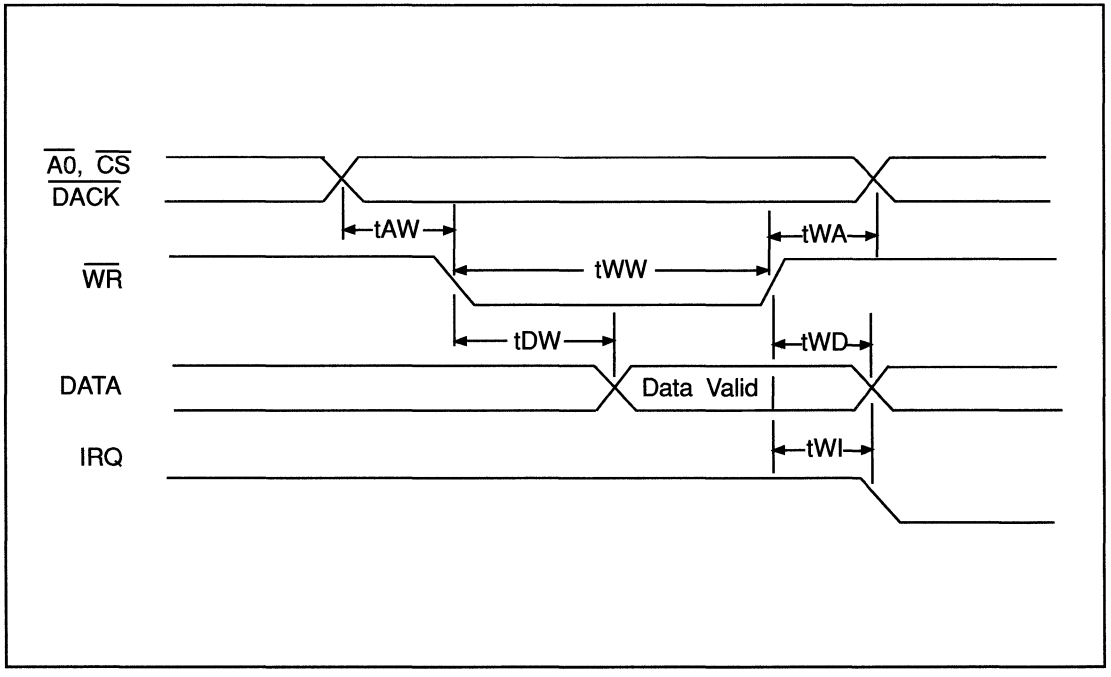


FIGURE 11. WRITE TIMING

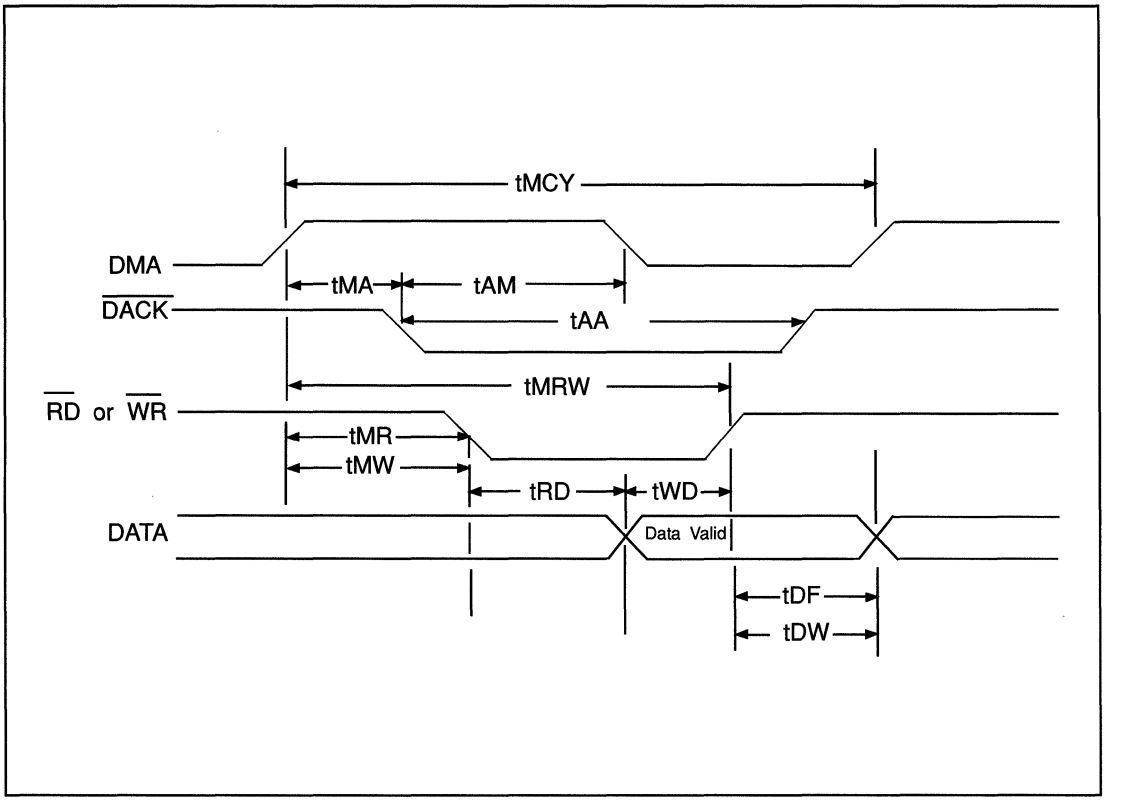


FIGURE 12. DMA TIMING

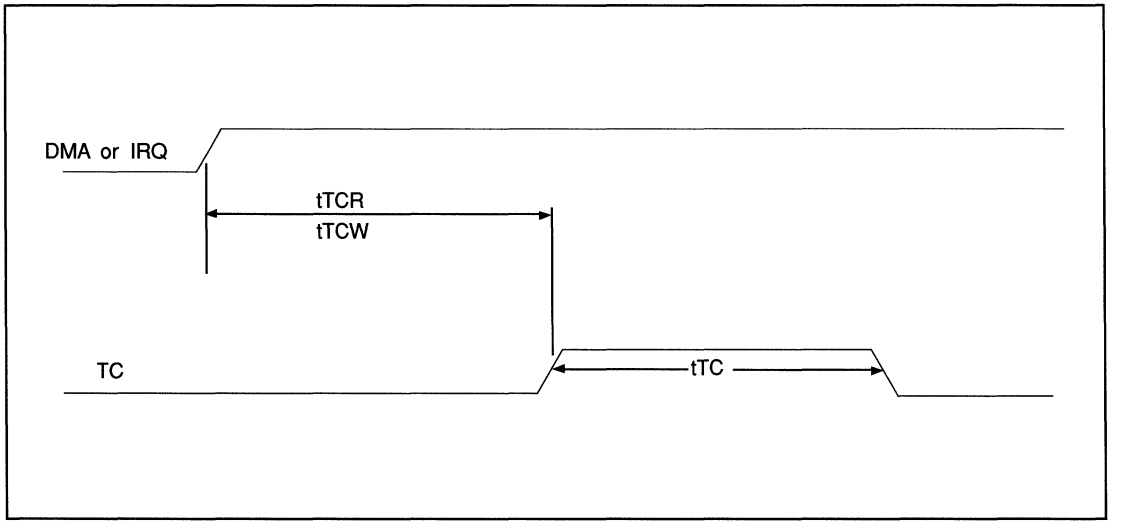


FIGURE 13. TERMINAL COUNT TIMING

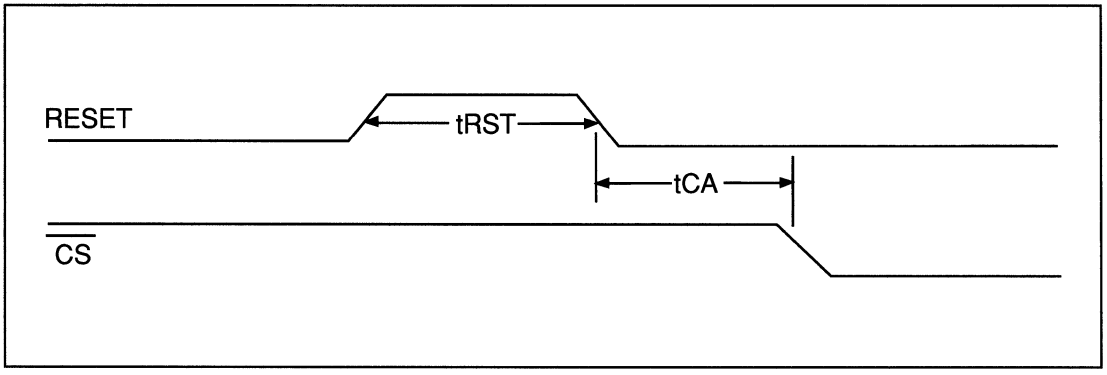


FIGURE 14. RESET TIMING

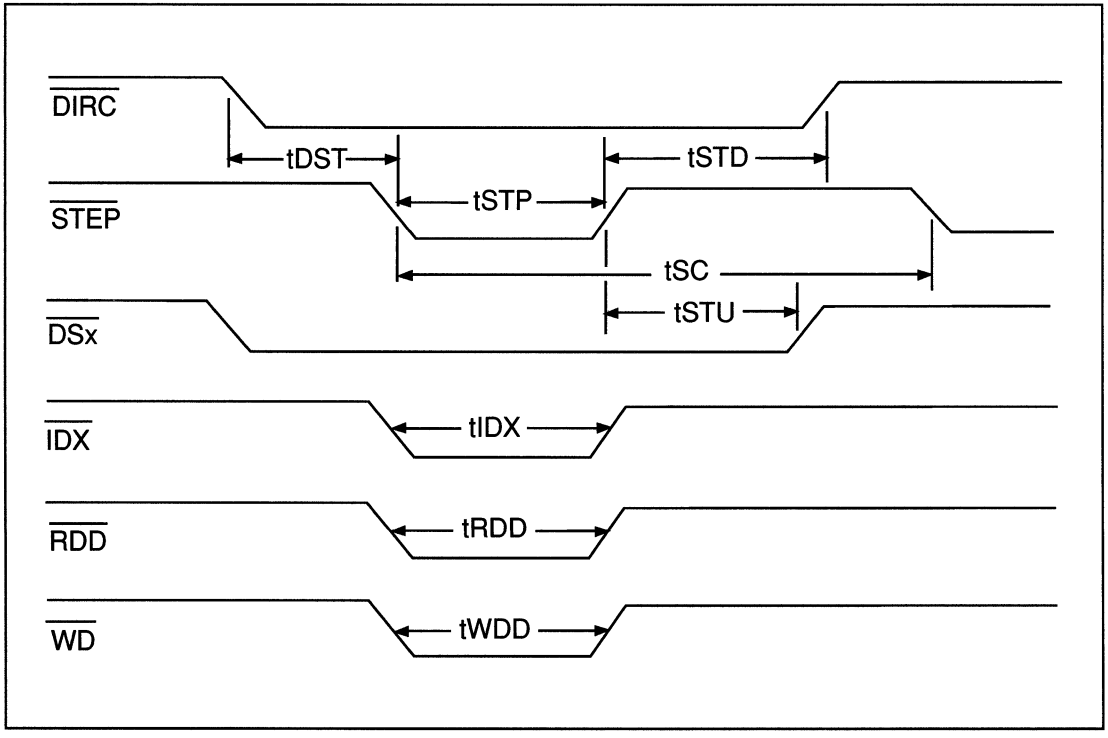


FIGURE 15. DISK DRIVE TIMING

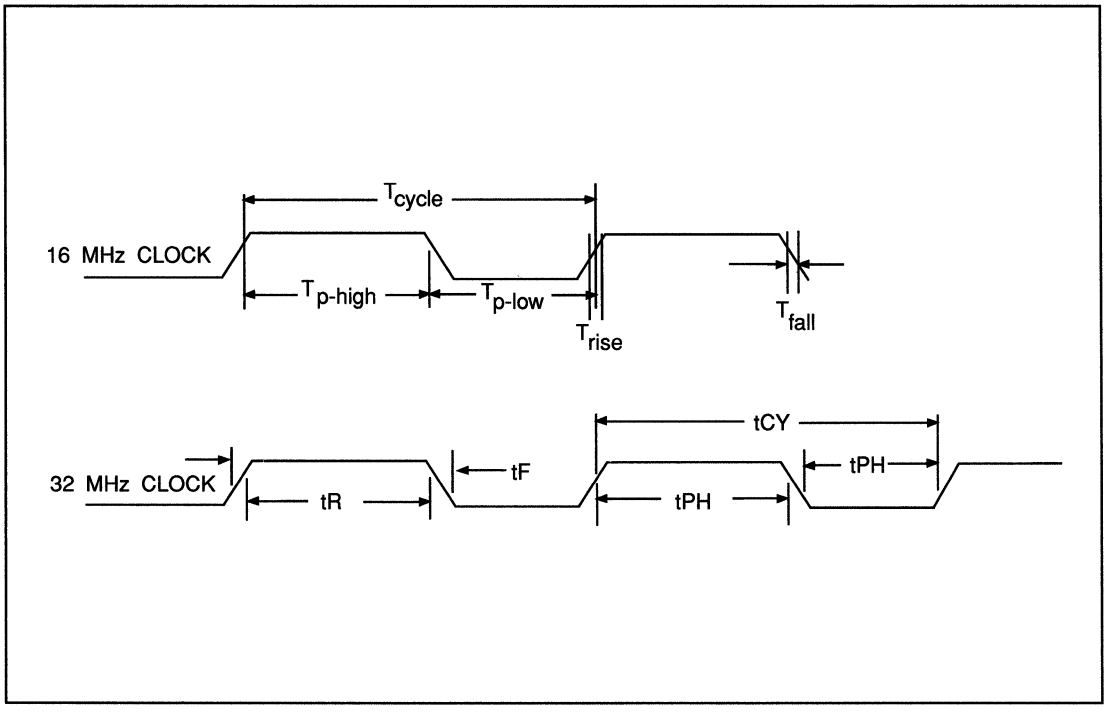


FIGURE 16. CLOCK TIMING

WD42C22A

Winchester Disk Subsystem Controller Device

WESTERN DIGITAL

TABLE OF CONTENTS

Section Title **Page**

Section Title **Page**

Section **Title** **Page**

Section **Title** **Page**

Section **Title** **Page**

32

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

Western Digital's WD42C22A integrates a high performance, low cost Winchester formatter/controller, host interface, a buffer manager, and CRC/ECC generator/checker in a single 84-pin LSI device. Operating from a single +5V power supply, the WD42C22A is implemented in a low power CMOS design and is available in an 84-pin PLCC (Figure 1). Figure 2 is a block diagram of the WD42C22A.

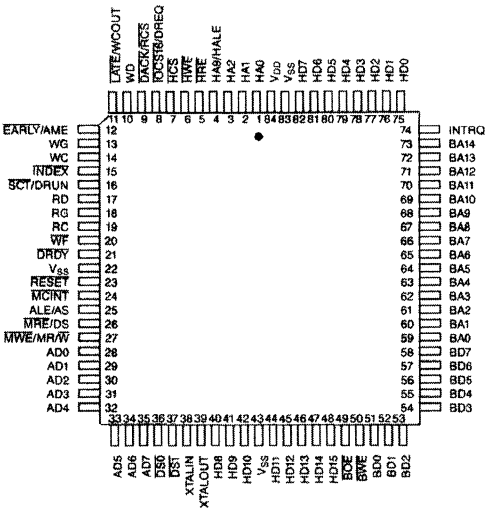


FIGURE 1. PIN DESIGNATION

1.1 FEATURES

- Enhanced host interface
  - IBM Personal Computer AT and XT port compatible
  - Supports AT speeds up to 12 MHz, 1 wait state I/O and 0 wait state memory using 120 nsec static RAM (SRAM)
  - Supports AT speeds up to 16 MHz, 1 wait state I/O and 0 wait state memory using 100 nsec SRAM
  - Selectable DMA or programmed I/O data transfers in all host interface modes
  - Host port slave mode compatible with ALE based peripherals such as the WD33C93 SBIC
  - Host transfer rates up to 4 Mwords/sec for AT and 4 MB/sec for XT
  - Internal 12 mA high current drivers for direct connection to the XT or AT system bus
- Advanced buffer manager
  - Supports 1:1 interleave **without** resorting to wait states
  - Direct interface for up to 32 KB of static RAM
  - Sustained RAM bandwidth up to 10 MB/sec
  - Pipelined host and disk address counters
  - Operates as either ring or scatter-gather buffer
  - Allows full track buffering and facilitates look ahead cacheing algorithms
- Adaptable disk controller
  - Software selectable MFM, RLL 2, 7, or NRZ disk interface
  - Software selectable 56 bit ECC, 32 bit ECC, or 16 bit CRC
  - Software selectable 5, 11, or 22 bit error correction span
  - Software selectable default sector lengths of 128, 256, 512, and 1024 bytes
  - User programmable sector size up to 2048 bytes
  - Software selectable 3 bit or 4 bit head number field
  - Reads and writes at 1:1 Interleave regardless of the formatted interleave
  - 15 Mbs data transfer rate for MFM and RLL
  - 20 Mbs data transfer rate for NRZ
  - Supports hard or soft sectored formats
  - Supports "zero latency" read operations
  - Internal defect management of sector and track level alternates
  - Able to read ESDI defect list
  - Supports sector servo schemes by disabling WRITE GATE over servo when formatting
  - Internal 48 mA drivers and Schmitt trigger input receivers for direct connection to the drive control cable

32

- Integrated support features
  - Programmable master/slave mode allows two Integrated Drive Electronics (IDE) disks on one connector
  - Supports both Intel-type(80xx) and Motorola-type(68xx) microcontrollers
  - Internal power-qualified reset to detect low V_{DD}
- Low power sleep mode

1.2 DESCRIPTION

1.2.1 ENHANCED HOST INTERFACE

The WD42C22A host interface port directly connects to the host system bus via internal 12 mA drivers. When operating in either AT or XT mode, all host control, data, and task file address lines directly connect to the WD42C22A. Mapping the device to the desired host system I/O addresses require external address decode logic. Integrated I/O port compatible AT and XT task file registers assure system compatibility.

To satisfy requirements for faster system bus rates and data transfers, the WD42C22A can operate in 12 MHz or 16 MHz, 1 wait state I/O channels (0 wait state memory) of 286 microprocessors. DMA or PIO data operations transfer at a rate of 4 Mwords/sec (AT mode) or 4 MB/sec (XT mode). In addition to traditional single

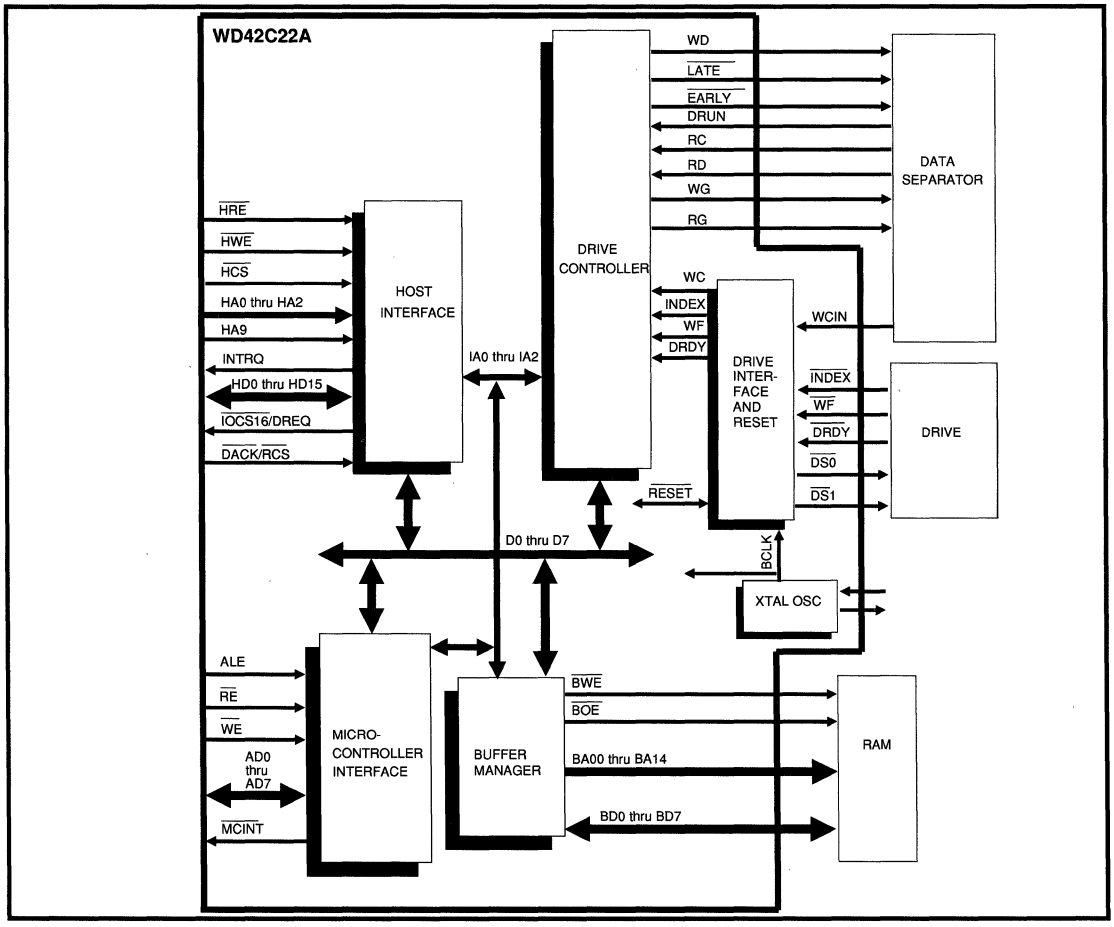


FIGURE 2. WD42C22A BLOCK DIAGRAM

mode DMA, burst mode DMA transfers are also available.

An alternative host mode, slave mode, allows communication between the microcontroller and a peripheral device through the host interface. The slave device transfers data to the buffer RAM by using a slave DMA scheme such as the WD-BUS mode in the WD33C93 SCSI bus interface controller (SBIC).

1.2.2 ADVANCED BUFFER MANAGEMENT

The WD42C22A contains an advanced buffer manager satisfying the interface requirements between a byte or word wide host interface bus and a high speed serial disk interface. Optimized for the block oriented data structures of a disk controller, the WD42C22A can manage multiple sector buffers up to 32 KB. Each sector buffer can be any size to 2055 bytes. Pipelined host and disk address counters enable sustained, simultaneous transfers on each port. Sufficient RAM buffer bandwidth is available to support 1:1 interleaved 20 Mb/sec disk transfers while simultaneously performing 16-bit host transfers at a rate in excess of 3 Mwords/sec. Achieving maximum RAM bandwidth requires using 70 nsec static RAM.

The pipelined structure of the buffer manager controls the buffer RAM in either a simple ring structure or a more advanced scatter-gather structure.

1.2.3 ADAPTABLE DISK CONTROLLER

The WD42C22A's versatile design makes the device adaptable for a wide variety of disk interface operations. A designer can select from three data formats, MFM, RLL 2,7, or NRZ. Disk data rates range up to 15 Mbits/sec with MFM and RLL 2,7 encoding, while NRZ data rates range up to 20 Mbits/sec. To support varied data format requirements, the WD42C22A operates in hard or soft sectored mode with programmable sector sizes to 2048 bytes and programmable ID PLO, data PLO, and GAP lengths.

Software selectable retry algorithms and 32 or 56-bit ECC polynomials enhance data integrity. Data integrity can further be ensured through the use of the device's built-in advanced defect management. The WD42C22A can be programmed to automatically detect the presence of a previously assigned defective sector and identify the location of the alternate sector. This allows access to alternate sectors without the typical additional rotational latency associated with defect handling.

With the pipelined architecture of the buffer manager, the designer can program the disk controller to execute "zero-latency" multiple sector read operations. In this mode of operation, the WD42C22A immediately commences data transfer to the RAM buffer upon encountering the first sector on the desired track. All subsequent sectors transfer to the buffer within a single rotational period. Host transfers begin upon location of the first requested sector within the buffer. Simultaneous host and disk transfers continue until all sectors are read from the drive. Zero-latency operation makes available an entire track of data to the host within one rotational period from the time the host requested the data. This differs from traditional implementations which read the entire track within one rotational period **AFTER** the first requested sector has been located. Zero latency read operations eliminate the typical one-half rotational period average latency required to locate the first sector in full track data transfers

The WD42C22A includes an internal power qualified reset circuit for power up and power down conditions. This circuit eliminates the need for costly external circuitry that traditionally performed this function.

The WD42C22A features a multiplexed address/data bus on the microcontroller interface port and supports both Intel (80XX) and Motorola (68XX) type microcontrollers. An internal circuit automatically determines the connected microcontroller and configures the ports for direct interfacing.

Internal 48 mA drivers and Schmitt triggers input receivers provide direct connection to the drive control cable. Programmable input polarities assist in integrated drive electronics (IDE) designs.

1.2.4 FLEXIBILITY OF APPLICATION

As a result of its level of integration, a designer can create a wide variety of products. In addition to traditional stand alone Winchester controller boards, the WD42C22A is ideal for multi-function

boards, direct system motherboards, and IDE applications. Special design considerations within the WD42C22A facilitate these applications.

1.2.5 TYPICAL APPLICATION

With an external microcontroller, buffer RAM, and a data separator such as the WD10C22B, the WD42C22A forms the basis of a Winchester disk controller product. For AT and XT applications, direct interfacing is available to the system bus. In these applications, the WD42C22A requires external address decoding to select the primary and secondary I/O address range of the WD42C22A. Other bus interfaces are supported via auxiliary bus controllers such as the WD33C93A SCSI Bus Interface Controller.

For ST506 (MFM) and ST412HP (RLL) applications, the WD42C22A directly connects to the WD10C22 data separator. (Like the WD42C22A, the WD10C22B supports both MFM and RLL encoding methods.) An external microcontroller implements interface specific control lines, e.g. the ST506's $\overline{\text{STEP}}$ and $\overline{\text{DIRECTION}}$ signals. For ESDI applications, the WD42C22A operates in NRZ mode.

1.2.6 PIN DESCRIPTIONS

This section lists the pin number, signal name, and function for all the WD42C22A's pins. The pin descriptions are arranged by functions. Table 1 describes the pin designations for the host interface. Table 2 describes the pin designations for the local microcontroller interface. Table 3 describes the pin designations for the buffer interface. Table 4 describes the pin designations for the drive interface.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1 2 3 4	HA0 HA1 HA2 HA9/ HALE	HOST ADDRESS 0 HOST ADDRESS 1 HOST ADDRESS 2 HOST ADDRESS 9/ HOST ALE	I I I I/O	Schmitt-triggered input. These four inputs are used to address the internal registers. Internal decoding of these address signals is a function of the AT/XT and HSMB mode bits. Port compatibility is maintained for both the AT and XT. In slave host mode HALE is used by the peripheral device to latch the address from HD0 through HD7.
5	$\overline{\text{HRE}}$	$\overline{\text{HOST READ ENABLE}}$	I/O	Schmitt-triggered input. $\overline{\text{HRE}}$ is asserted by the AT or XT with HCS to read an internal register or the FIFO. In slave mode, $\overline{\text{HRE}}$ is asserted when $\overline{\text{MRE}}$ is asserted. It can also be asserted by the slave peripheral in DMA mode.
6	$\overline{\text{HWE}}$	$\overline{\text{HOST WRITE ENABLE}}$	I/O	Schmitt-triggered input. $\overline{\text{HWE}}$ is asserted by the AT or XT with HCS to write an internal register or the FIFO. In slave mode, $\overline{\text{HRE}}$ is asserted when $\overline{\text{MRE}}$ is asserted. It is also asserted by the slave peripheral in DMA mode.
7	$\overline{\text{HCS}}$	$\overline{\text{HOST CHIP SELECT}}$	I/O	Schmitt-triggered input. $\overline{\text{HCS}}$ should be decoded from the AT or XT address bus and is used to qualify $\overline{\text{HRE}}$ and $\overline{\text{HWE}}$ for host accesses. In slave mode, HCS is asserted when the local microcontroller is accessing the slave device address space.
8	$\overline{\text{IOCS16}}$/ DREQ	$\overline{\text{I/O CHIP SELECT 16}}$/ DMA REQUEST	O	This output is programmable to function as the AT bus signal $\overline{\text{IOCS16}}$ when the PIO mode is selected or as a DMA Request signal (DREQ) in the DMA mode. This output is tri-stated at power-up and remains tri-stated until the interface mode is set by the local microcontroller. $\overline{\text{IOCS16}}$ is an open-drain ouput. DREQ is a tri-state output.
9	$\overline{\text{DACK}}$/ RCS	$\overline{\text{DMA ACKNOWLEDGE}}$/	I	Schmitt-triggered input. $\overline{\text{DACK}}$ is asserted by the host in response to the DREQ signal assertion in order to complete the DMA handshake. $\overline{\text{RCS}}$ is used in slave mode to qualify host data transfers to/from the FIFO.

TABLE 1. HOST INTERFACE PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
23	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	I/O	Open-drain output and Schmitt input, can be wire- ORed with an external reset. The WD42C22A resets all logic except the Task File when this input is asserted. On power-up, or when requested by the host, this output is asserted.
75 thru 82, 40, 41, 42, 44 thru 48	HD0 thru HD15	HOST DATA 0 thru HOST DATA 15	I/O	Schmitt-triggered inputs. These 16 pins are used during host 16-bit data transfers, and the lower eight bits (HD0-HD7) are used for byte-wide host data transfers as well as all command and status information transfers.
74	INTRQ	INTERRUPT REQUEST	I/O	INTRQ indicates to the AT or XT that a data blocktransfer is requested or a command has been completed. In slave host mode INTRQ is asserted by the slave peripheral device.
83	V_{SS}	GROUND		Ground.
84	V_{DD}	+5V		+5V

TABLE 1. HOST INTERFACE PIN DESCRIPTION (CONT'D)

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
22	V_{SS}	GROUND		Ground.
24	$\overline{MCINT}$	$\overline{\mu CONTROLER}$ INTERRUPT	O	This output is used as an interrupt signal in order to alert the local microcontroller it is necessary to check command parameters or status. For the XT mode, $\overline{MCINT}$ is asserted when the controller is selected.
25	ALE/AS	ADDRESS LATCH ENABLE/ ADDRESS STROBE	I	Schmitt-triggered input. ALE is used to latch the lower eight address bits from the multiplexed address/data lines (AD7-AD0). AS is used for this function when tied to a Motorola type microcontroller.
26	$\overline{MRE}$/DS	$\overline{\mu CONTROLLER}$ READ ENABLE /DATA STROBE	I	Schmitt-triggered input. $\overline{MRE}$ is asserted by the local microcontroller to read an internal register or the buffer. DS is used in Motorola type microcontrollers to enable the data transfer.
27	$\overline{MWE}$/ MR/W	$\overline{\mu CONTROLLER}$ WRITE ENABLE/ uC READ/WRITE	I	Schmitt-triggered input. $\overline{MWE}$ is asserted by the local microcontroller to write an internal register or the buffer. MR/W is used by Motorola type microcontrollers to set the direction of data transfers.
28 thru 35	AD0 thru AD7	ADDRESS/DATA 0 thru ADDRESS/DATA 7	I/O	Schmitt-triggered inputs. These multiplexed address/data lines are used to load the register/buffer address on the falling edge of ALE, and are used for data transfers between the local microcontroller.
43	V_{SS}	GROUND		Ground.

TABLE 2. LOCAL MICROCONTROLLER INTERFACE PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
38	XTALIN	CRYSTAL INPUT	I	Crystal oscillator input. The crystal frequency is twice the buffer data rate.
39	XTALOUT	CRYSTAL OUT	O	Crystal oscillator output.
49	$\overline{\text{BOE}}$	$\overline{\text{BUFFER}}$ OUTPUT $\overline{\text{ENABLE}}$	O	$\overline{\text{BOE}}$ is asserted by the chip to read data from the external SRAM buffer.
50	$\overline{\text{BWE}}$	$\overline{\text{BUFFER}}$ WRITE $\overline{\text{ENABLE}}$	O	$\overline{\text{BWE}}$ is asserted by the chip to write data into the external SRAM buffer.
51 thru 58	BD0 thru BD7	BUFFER DATA 0 thru BUFFER DATA 7	I/O	Schmitt-triggered. Buffer data bus, which connects directly to a static RAM.
59 thru 73	BA0 thru BA14	BUFFER ADDR 0 thru BUFFER ADDR 14	I/O	Buffer address bus, for direct connection to 32 KB of SRAM. In XT mode, also used to read jumper config-uration data in Read Configuration Mode. In input mode, there is a low current internal pulldown.

TABLE 3. BUFFER INTERFACE PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
10	WD	WRITE DATA	O	WD is the MFM/NRZ write data written to the disk. It is shifted out at a rate determined by write clock. MFM write data should be synchronized by a D flip flop clocked at 10 MHz (for 5 Mbs operation).
11	LATE/ WCOUT	LATE/ WCOUT	O O	LATE is used along with EARLY in the Write Precompensation circuitry to control the delay of WD. In NRZ mode WCOUT is write clock out which can be used to qualify WD in an ESDI application.
12	AME/ EARLY	ADDRESS MARK ENABLE/EARLY	O	In NRZ mode, this output is the Address Mark Enable signal for an ESDI drive. In MFM or RLL mode, this output is EARLY. EARLY and LATE are used in the Write Precompensation circuitry to control the delay of WD.
13	WG	WRITE GATE	O	WG is asserted when valid data is to be written to the disk. It enables write current to the head and is immediately de-asserted if a WRITE FAULT (WF) is detected.
14	WC	WRITE CLOCK	I	A clock used internally to control WD. (Up to 10 MHz for ST412, up to 15 MHz for ESDI).
15	INDEX	INDEX	I	Schmitt-triggered INDEX input for direct connection to the drive control cable.
16	SCT/ DRUN	SECTOR/ DATA RUN	I	Schmitt-triggered input. In hard sector mode, SCT is used to indicate the start of a sector. In soft sector NRZ mode, SCT indicates Address Mark Found. In soft sector MFM or RLL mode, DRUN indicates a sequence of MFM or RLL '0's or a sequence of MFM '1's has been detected.
17	RD	READ DATA	I	RD is MFM or NRZ read data from the drive. Data and clocks are separated internally for MFM data.
18	RG	READ GATE	O	RG is asserted to initiate a search for an address mark. It remains asserted until the end of the ID or data field.

TABLE 4. DRIVE INTERFACE PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
19	RC	READ CLOCK	I	RC is typically generated from an oscillator phase-locked to the read data.
20	$\overline{WF}$	$\overline{WRITE\ FAULT}$	I	Schmitt-triggered. $\overline{WRITE\ FAULT}$ input for direct connection to the drive control cable.
21	$\overline{DRDY}$	$\overline{DRIVE\ READY}$	I	Schmitt-triggered. $\overline{DRIVE\ READY}$ input for direct connection to the drive control cable.
36	$\overline{DS0}$	$\overline{DRIVE\ SELECT\ 0}$	O	High-current open-drain $\overline{DRIVE\ SELECT}$ outputs for direct connection to the drive control cable.
37	$\overline{DS1}$	$\overline{DRIVE\ SELECT\ 1}$	O	

TABLE 4. DRIVE INTERFACE PIN DESCRIPTION (CONT'D)

2.0 ARCHITECTURE

2.1 POWER-QUALIFIED RESET

This integrated function is used to reliably initialize flip-flops to a predictable state during the application of V_{DD}. It causes the $\overline{RESET}$ output signal to be asserted. It also forces a reset if the V_{DD} falls below a threshold.

2.2 DRIVE INTERFACE LOGIC

The drive interface contains high-current 48 mA drivers for direct connection of the drive select outputs to the drive control cable. Schmitt trigger input receivers connect the drive interface logic directly to the control cable inputs.

2.3 DRIVE CONTROLLER ORGANIZATION

The controller is composed of the following major sections:

- PLA Control
- CRC/ECC Logic
- MFM/RLL Decoding
- Address Mark Detector
- Buffer and DMA Control
- Task Register File

The controller is designed to operate with 2 clock inputs, READ CLOCK (RC) and WRITE CLOCK (WC). The PLA controller, processor interface, and buffer control sections use the write clock input. The clock inputs are used for MFM, RLL, or NRZ decoding. For a 10 Mbs data rate, the clock frequency is 10 MHz for a 10 Mbs data rate.

The controller reads or writes disk data to a 15 Mbs rate for MFM and RLL and 20 Mbs for NRZ. The RLL implementation is a (2,7,2,4,3) code based on the IBM 3370 code. The only difference lies in the assignments of the code words to the 7 different data streams possible. Error propagation for a single bit error is limited to 4 bits.

When programmed in the NRZ mode, the WD42C22A qualifies NRZ disk data using the Sector / Address Mark Detect signal, and also modifies the RG and WG signals to meet ESDI specifications.

In all modes, the length of the PLO sync and gap fields are software programmable. The ID PLO sync field length, the Gap1/Gap3 length, the Gap1/Gap3 data bytes and the ID CRC pad bytes are programmable during the format command. The data PLO sync field length and the data CRC/ECC pad bytes are programmable during the Write command.

Figure 3 is a block diagram of the drive controller section of the WD42C22A.

2.4 PROGRAMMABLE LOGIC ARRAY (PLA) CONTROLLER

The PLA controller interprets commands, e.g. write, read format, etc. This circuitry's operation is

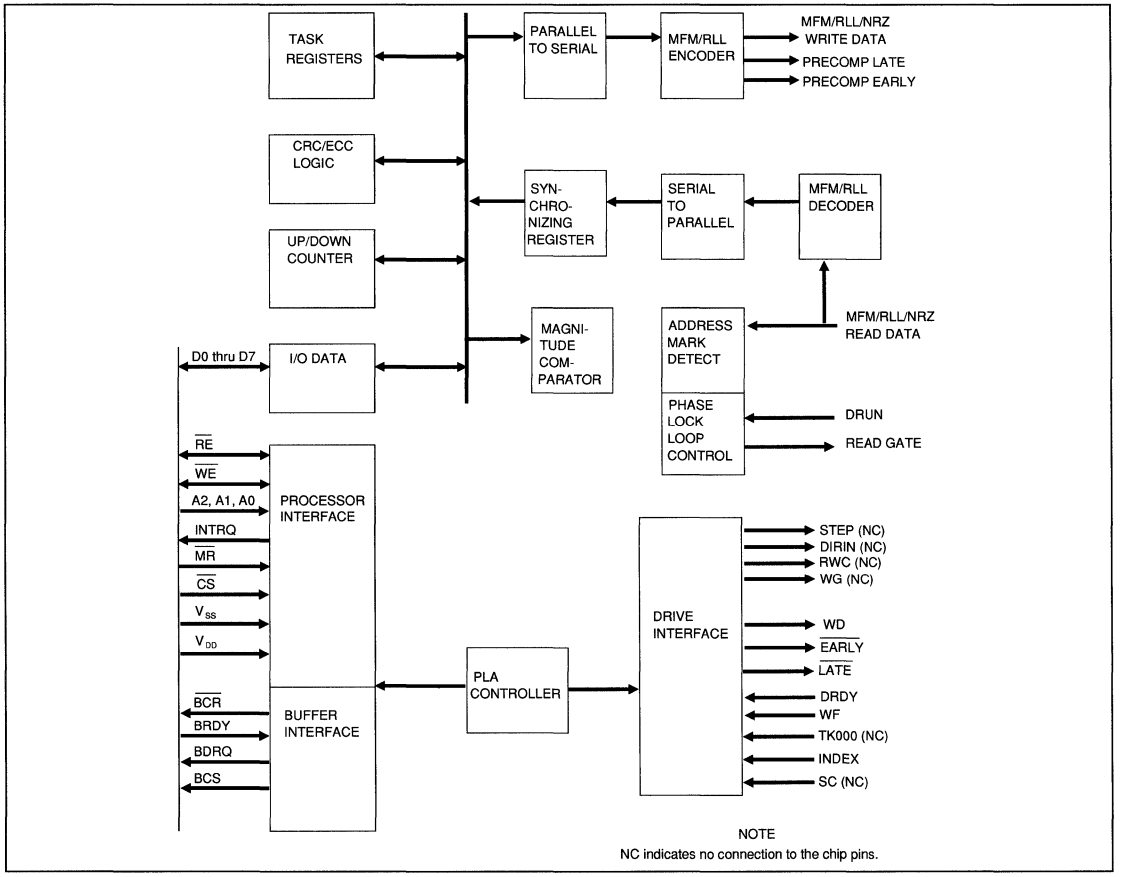


FIGURE 3. DRIVE CONTROLLER BLOCK DIAGRAM

synchronized with the WC input. The PLA controller is started when a command is written into the command register. It generates control signals and operates in a handshake mode when communicating with the MFM/RLL decoding block. The MFM/RLL decoding block uses the RC input which may be asynchronous to WC.

2.5 MAGNITUDE COMPARATOR

An 11-bit magnitude comparator calculated drive step direction and number of step pulses between present cylinder position and desired position in earlier Winchester controller versions. This comparator is **not** used in the WD42C22A. A separate high speed equivalence comparator is used to compare ID field bytes when searching for a sector ID field.

2.6 CRC/ECC GENERATOR AND CHECKER

The CRC/ECC generator computes and checks the cyclic redundancy check characters appended to the ID and data fields written on the disk. The CRC mode of operation, defined by the SDH register (bit 7 set to 0) provides a means of verifying the accuracy of the data read from the disk but does not attempt to correct it. (Bit 7 of the SDH register will not implement CRC mode for data fields when RLL mode is selected.) The CRC polynomial used is:

$$X^{16} + X^{12} + X^5 + 1$$

The CRC register is preset to all ones before computation starts.

If the CRC character being generated while reading the data does not equal the one previously written, an error exists. If there is a CRC failure in the ID field, an ID not found is indicated by setting bit 4 of the error register. If the failure is in the data field, bit 6 of the error register is set.

A 32 bit or 56 bit ECC polynomial may be selected instead of the CRC polynomial for the data field. The CRC/ECC selection is controller by bit 7 of the SDH register when the controller is in MFM or NRZ modes. CRC is selected when bit 7 of the SDH register is 0 in MFM or NRZ modes. ECC is selected when bit 7 of the SDH register is 1 in MFM or NRZ modes. Bit 2 in the set parameter command selects either the 32 bit or 56 bit polynomial. RLL mode defaults to the 56 bit polynomial. The CRC or 32 bit ECC options are **not** usable in RLL mode.

The ECC mode of operation (SDH bit 7 = 1) is only applicable to the data field. This feature built into the WD42C22A provides the user with the ability to detect and correct errors in the data field automatically.

The following is a summary of the parameters considered when ECC is used:

- 1. SDH register bit 7.
- 2. Read and write command bit 1 (L).
- 3. Compute correction command.
- 4. Set parameter command.
- 5. Error occurred, bit 0 of the status register.
- 6. On any ECC error the controller stops regardless of the T bit. (Refer to the read command description.)

The SDH register bit 7 must be equal to one to change from the CRC mode to the ECC mode, for MFM and NRZ only.

When an ECC error is detected, no attempt is made to correct it and bit 0 of the status register and bit 6 of the error register are set. The user now has two choices:

- 1. Ignore the error and make no attempt to correct it.
- 2. Use the compute correction command to determine the pattern and location of the error, and correct it within the user's program.

When implementing the compute correction command, use it before executing commands that alter the content of the ECC register. The read, write, scan, and format commands can alter the syndrome and make correction impossible. If the compution correction command determines that the error is uncorrectable, then the error bits in the status register and error register are set.

Although ECC generation starts with the first bit of the F8 byte in the data ID field, the actual ECC bytes produced for the sector are the same as if the A1 byte was included.

The 32-bit ECC polynomial is:

$$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 1$$

and is the same one used in the WD1002, WD1003, and WD1006 controller boards. The 32-bit ECC polynomial has an 11 bit maximum single burst correction span. The reverse 32-bit ECC polynomial is:

$$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^6 + X^4 + 1$$

The non-detection probability for the 32-bit ECC polynomial is:

2.3 (E-10), $r^{\dagger} = 516 \times 8$, $b^{\dagger} = 5$

and the miscorrection probability is:

1.57 (E-5), $r^{\dagger} = 516 \times 8$, $b^{\dagger} = 5$

The 56-bit ECC polynomial is:

$$X^{56} + X^{52} + X^{50} + X^{43} + X^{41} + X^{34} + X^{30} + X^{26} + X^{24} + X^8 + 1$$

The 56-bit ECC polynomial has a 22 bit maximum single burst correction span.

The reverse 56-bit ECC polynomial is:

$$X^{56} + X^{48} + X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^6 + X^4 + 1$$

† r represents record length. b represents error correction span.

The non-detection probability for the 56-bit ECC polynomial is:

$$1.39\ (E\text{-}17),\ r^{\dagger} = 519 \times 8,\ b^{\dagger} = 11$$

and the miscorrection probability is:

$$5.84\ (E\text{-}11),\ r^{\dagger} = 519 \times 8,\ b^{\dagger} = 11$$

The set parameter command selects the number of bits in the correction span, through the use of bit 0.

Read and write commands, with the L bit (bit 1) set to one, are referred to as read long and write long commands. With these commands, no ECC or CRC characters are generated or checked by the WD42C22A. In effect, the four or seven bytes are handled as an additional four or seven bytes of data which pass through the data buffer. With proper use of the write, read long, write long, and read commands, a diagnostic routine may be developed to test the accuracy of the error correction process.

For CRC/ECC calculations, the CRC/ECC register is initialized to all 1's. For CRC/ECC purposes only, the address mark byte has a value of "A1" and is included in the CRC/ECC calculations.

2.7 MFM/RLL ENCODING AND MFM/RLL DECODING

The MFM/RLL encoding section receives 8-bit parallel data and generates either MFM or RLL write data depending on the K option in the load parameter block command. This section operates with a write clock having a frequency of the desired bit rate. The write clock need not be synchronized to read clock (RC).

Data bytes are written to the drive most significant bit first. The MFM/RLL decoding section generates 8 bit binary data from MFM or RLL read data once an address mark has been detected. Table 5 lists the RLL coding rules followed by the controller.

NRZ Data				RLL Code Word Output	
First Bit		Last Bit		First Bit	Last Bit
1	1	X	X	1 0 0 0	X X X X
1	0	X	X	0 1 0 0	X X X X
0	1	1	X	0 0 1 0	0 0 X X
0	1	0	X	0 0 0 1	0 0 X X
0	0	0	X	1 0 0 1	0 0 X X
0	0	1	1	0 0 0 0	1 0 0 0
0	0	1	0	0 0 1 0	0 1 0 0

TABLE 5. RLL CODING RULES

When NRZ mode is selected, the MFM/RLL encode and decode logic is bypassed. NRZ read data is clocked in on the rising edge of Read Clock and NRZ write data is clocked out on the rising edge of WC.

2.8 ADDRESS MARK DETECTOR

An address mark is a unique 2 byte code placed at the beginning of each ID field or data field. A series of zero bytes always precedes each address mark. The address mark detector section begins searching for an address mark when synchronization has been lost after a series of zero bytes is detected. The detection of an address mark establishes resynchronization.

The address mark is composed of a 2 byte sequence. The first byte is used for resynchronization and the second byte specifies ID or data field. For the MFM mode, the first byte is an A1 (hex) byte with missing clock (data = A1, clock = 0A). The second byte is encoded with normal MFM rules. FF through FC and F7 through F4 specify the beginning of an ID field and F8 specifies the beginning of a data field.

In RLL mode, the first byte is a unique code which violates normal RLL coding rules but does not violate the 2,7 timing rule. The RLL address mark pattern is 1000 0000 1001 0000 (8090 hex). The second byte is encoded with normal RLL rules. FF through FC and F7 through F4 specify the

beginning of an ID field and F8 specifies the beginning of a data field.

In NRZ mode, an NRZ A1 byte establishes byte synchronization. When the WD42C22A is used to control an ESDI (NRZ) drive, the Sector Pulse (Address Mark Found) signal will qualify Read Data to prevent false address mark detection.

2.9 CONTROLLER TO DATA SEPARATOR INTERFACE

The read interface section generates READ GATE (RG) from signals sent by the PLA controller and by the DRUN input. In this system, raw read data from the drive is presented to the RD in put. RG is low when the controller is not inspecting read data. When a read command is started and a search begins for an address mark, DRUN from the data separator is examined. Since each address mark should be preceded by approximately 12 bytes of zeroes, RG is activated when a sequence of zeros is detected by DRUN and read data is examined until either an address mark is detected or a non-zero byte which is not an address mark is detected. If an address mark was detected, and it was preceded by at least 8 bytes of zeroes, read gate is held high and the ID or data field can be read.

If a non-zero non-address mark byte was detected, then read gate is dropped for at least 2 byte times, allowing the phase lock loop to resynchronize with WC, before inspecting DRUN input again. If the desired ID field was read, then the sector transfer can be made. If a data field was detected or if the ID bytes did not match, or if an address mark was not preceded by eight bytes of zeroes with six coming after RG on, then RG is lowered and DRUN is inspected again for a sequence of zeroes.

Figures 4 illustrates the PLL control sequence for the ID field. Figure 5 illustrates the PLL control sequence for the data field.

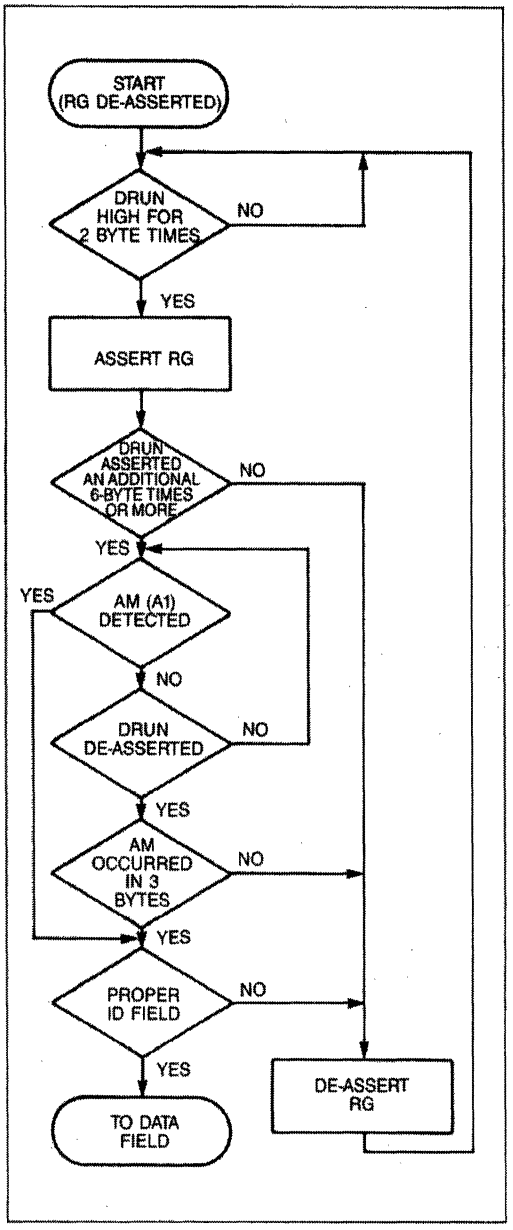


FIGURE 4. PLL CONTROL (ID FIELD)

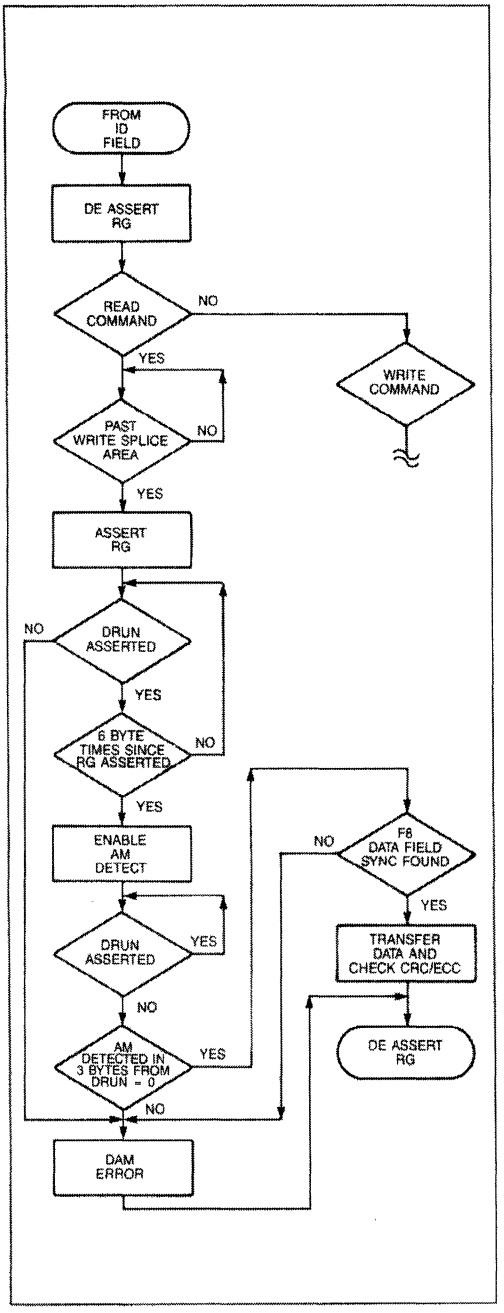


FIGURE 5. PLL CONTROL (DATA FIELD)

The write precompensation circuitry, in the controller to the drive interface, reduces the effects one bit has on another. There are two parts to write precompensation logic, reduced write current (RWC) and shifting of the bits as they are written. The RWC is **NOT** controlled by the drive controller. The local microcontroller should specify when the write current is reduced by asserting its own RWC cutput.

The shifting of the data bits is controlled by the $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ outputs. These two outputs should be used to delay the output as follows in Table 6:

$\overline{\text{EARLY}}$	$\overline{\text{LATE}}$	DELAY	
0		1	no delay
1		1	one unit delay
1		0	two units delay

TABLE 6. EARLY AND LATE DELAYS

32

The $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ outputs are generated according to the rules in Tables 7 (RLL) and 8 (MFM or NRZ).

RLL Coded Data Pattern			
Preceding Bits	**Comp. Bit**	**Following Bits**	**Precomp**
0 1 0 0	1	0 0 0 1	None
0 1 0 0	1	0 0 0 0	EARLY
X 0 0 0	1	0 0 0 X	None
1 0 0 0	1	0 0 1 0	None
0 0 0 0	1	0 0 1 0	LATE
0 1 0 0	1	0 0 1 0	None

TABLE 7. EARLY AND LATE GENERATION (RLL MODE)

MFM Coding - NRZ Data Pattern			
Preceding Bits	CompBit	Following Bits	Precomp
X X X 1	1	0 X X X	EARLY
X X X 0	1	1 X X X	LATE
X X 0 0	0	1 X X X	EARLY
X X 1 0	0	0 X X X	LATE

TABLE 8. EARLY AND LATE GENERATION (MFM - NRZ)

3.0 INTERFACE PORTS AND TASK FILES

3.1 HOST INTERFACE ORGANIZATION

The WD42C22A's host interface directly connects to the IBM XT or IBM AT system bus as well as the system bus of any XT or AT compatible. The WD42C22A has high current drivers which allow it to be directly connected to the system bus.

The register configuration for the host interface is dependent on the state of the AT/$\overline{XT}$ control bit in the interface control register which is written by the local microcontroller.

There is an additional slave host mode. In this mode, the microcontroller communicates to a peripheral device with up to 32 registers through the host interface. The slave device can transfer data between the buffer RAM by using a slave DMA scheme such as the WD-BUS mode in the SBIC.

The sequence that the microcontroller follows to transfer data between the buffer RAM and the host is defined under the buffer manager description.

3.2 XT HOST INTERFACE

To put the WD42C22A in the PC/XT compatible interface mode the local microcontroller resets the AT/$\overline{XT}$ control bit. In this mode, $\overline{HCS}$ should be active when I/O ports 320 (hex) through 323 (hex) are addressed. (XT I/O ports 320 through 323 are primary ports. XT I/O ports 324 through 327 are secondary ports. Unless otherwise noted, information regarding the primary ports is identical to information on secondary ports.) Table 9 lists the port descriptions for this mode.

HA9	HA2	HA1	HA0	READ PORT	WRITE PORT
X	X	0	0	Read data	Write data
X	X	0	1	Hardware status	Hardware reset
X	X	1	0	Drive configuration	Drive select
X	X	1	1	NOT USED	DMA and interrupt control

TABLE 9. XT PORT DESCRIPTIONS

3.2.1 READ DATA PORT (HA1 THRU HA0 = 0, READ)

The read data port is used to send data and status to the host processor. The data read from this port comes from the buffer RAM under the control of the buffer manager.

3.2.2 WRITE DATA PORT (HA1 THRU HA0 = 0, WRITE)

The write data port is used to send commands and data from the host to the drive controller. The data is written to the buffer RAM under the control of the buffer manager.

3.2.3 HARDWARE STATUS (HA1 THRU HA0 = 1, READ)

This port contains the controller hardware status. It can be read by the host at any time. Bit 7, bit 6, bit 2, and bit 1 are written by the local microcontroller. Bit 5, bit 4, bit 3, and bit 0 are controlled by internal logic. The bits are defined as follows:

Bit							
7	6	5	4	3	2	1	0
X	X	IRQ	DRQ	XBSY	C/D	I/O	REQ

3.2.3.1 BIT 5 - INTERRUPT REQUEST

This bit signifies that an interrupt is pending. IRQ reflects the state of the INTRQ output. The INTRQ pin is tri-stated and the IRQ status bit and internal interrupt flip-flop are reset when the host disables the interrupt or when the

WD42C22A is reset, either by the host or by asserting master reset.

3.2.3.2 BIT 4 DMA REQUEST

This bit signals that the WD42C22A is ready for a DMA transfer to take place. The direction of the transfer is determined by the I/O bit. This bit reflects the state of the DREQ output.

3.2.3.3 BIT 3 - XT BUSY

This bit indicates that the WD42C22A is busy executing a command and is unable to accept another command. This bit is set by during a reset.

3.2.3.4 BIT 2 - COMMAND / $\overline{\text{DATA}}$

This bit tells the host which type of transfer is expected at the read and write data ports. C/$\overline{D}$ set to 1 indicates that a command or status transfer is expected. C/$\overline{D}$ set to 0 indicates that a data transfer is expected.

3.2.3.5 BIT 1 - INPUT / $\overline{\text{OUTPUT}}$

This bit tells the host the direction of transfer for the two data ports. I/$\overline{O}$ set to 1 indicates an input (read) by the host and I/$\overline{O}$ set to 0 indicates an output (write) by the host.

3.2.3.6 BIT 0 - REQUEST

This bit is one of the handshaking signals between the host and WD42C22A. When transferring data between the WD42C22A's read data and write data ports by the host, assertion of this bit informs the host that the WD42C22A is ready for the transfer.

3.2.4 CONTROLLER RESET (HA1 THRU HA0 = 1, WRITE)

When this port is written, regardless of the data written, the RESET output is asserted if enabled. If the reset has been disabled by the local microcontroller, then writing to this port asserts $\overline{\text{MCINT}}$ and the local microcontroller is responsible for resetting the logic on the drive controller board.

3.2.5 DRIVE CONFIGURATION INFORMATION (HA1 THRU HA0 = 2, READ)

This register, when read, informs the host about the configuration of the drive(s) attached. This configuration information is written by the local microcontroller.

3.2.6 CONTROLLER SELECT (HA1 THRU HA0 = 2, WRITE)

When this port is written, regardless of the data written, the $\overline{\text{MCINT}}$ output is asserted to inform the local microcontroller that the controller board has been selected.

3.2.7 DMA AND INTERRUPT MASK (HA1 THRU HA0 = 3, WRITE)

This port enables or disables the DMA and interrupt to the host. When IRQEN is set to 1, then interrupts to the host are enabled. This bit is cleared when the WD42C22A is reset. The INTRQ line is tri-stated and the host interrupt is cleared when the interrupts are disabled. When DRQEN is set to 1, then DMA requests to the host are enabled. This bit is cleared when the WD42C22A is reset.

Bit							
7	6	5	4	3	2	1	0
X	X	X	X	X	X	IRQ EN	DRQ EN

3.3 AT HOST INTERFACE

To put the WD42C22A in the AT compatible interface mode, the AT/$\overline{\text{XT}}$ control bit is set by the local microcontroller. The $\overline{\text{HCS}}$ chip select should be active when I/O ports 1F0(hex) through 1F7(hex) and 3F6(hex) and 3F7(hex) are addressed for primary addressing and for I/O ports 170(hex) through 177(hex) and 376(hex) and 377(hex) for secondary addressing. Only address signals HA8 through HA3 and AEN need to be decoded to generate $\overline{\text{HCS}}$. Table 10 describes the ports for AT mode as follows:

ABSY	HA9	HA2	HA1	HA0	READ PORT	WRITE PORT
					AT TASK FILE COPY	
0	0	0	0	0	Read Data (16 bits)	Write Data (16 bits)
0	0	0	0	1	Host Error Register	Write Precomp Cylinder
0	0	0	1	0	Sector Count	Sector Count
0	0	0	1	1	Sector Number	Sector Number
0	0	1	0	0	Cylinder Number Low	Cylinder Number Low
0	0	1	0	1	Cylinder Number High	Cylinder Number High
0	0	1	1	0	SDH	SDH
0	0	1	1	1	Host Status Register	Host Command Register
1	0	X	X	X	Host Status Register	INVALID
					CONTROL PORTS	
X	1	1	1	0	Alternate Status Register	Fixed Disk Register
X	1	1	1	1	Digital Input Register	NOT USED

TABLE 10. AT MODE PORT DESCRIPTIONS

When port 0 is accessed the $\overline{\text{IOCS16}}$ output is asserted when in AT programmed I/O mode. All buffer data transfers are 16 bits. The ECC byte transfers in a long mode read or write are 8 bit transfers. All other register transfers are 8 bits.

Registers 1 through 7 are an identical copy of the drive controller task registers 1 through 7. These registers can be read or written by the host only when the ABSY status bit is not active. Any attempt by the host to read the AT task file copy while ABSY is active results in the host status register being read. The AT task file copy registers cannot be written by the host while ABSY is active.

3.3.1 ERROR REGISTER (HA9, HA2 THRU HA0 = 01, READ)

The error register is read only and contains the specific error status pertaining to a command. The meaning of the status register bits are as follows:

Bit							
7	6	5	4	3	2	1	0
BB	CRC/ ECC	0	IDNF	0	AC	TK0	DMNF

3.3.1.1 BIT 7 BAD BLOCK

A bad block address mark has been detected when trying to read or write that sector. The data field will not be read or written.

3.3.1.2 BIT 6 CRC/ECC DATA FIELD ERROR

An uncorrectable ECC error or a CRC error was detected in the data field.

3.3.1.3 BIT 5 RESERVED

Not used, forced to zero.

3.3.1.4 BIT 4 ID NOT FOUND

Occurs when cylinder, head, sector, size parameters with a correct ID field CRC cannot be found. For read and write sector commands, with

the retry disable bit reset, this bit indicates that after 10 index pulses, an auto-scan ID and auto-seek, and 10 more index pulses, no matching ID field was found. If the retry disable bit is set, then no matching ID field was found after 2 index pulses; no auto-scan or auto-seek is performed.

3.3.1.5 BIT 3 RESERVED

Not used, forced to zero.

3.3.1.6 BIT 2 ABORTED COMMAND

Set if command was started and one of the following conditions occurred:

- 1. Drive not ready
- 2. Write fault
- 3. Illegal command code.

3.3.1.7 BIT 1 TRACK 0 ERROR

This bit, when set, indicates an error detecting Track 0 during a restore.

3.3.1.8 BIT 0 DATA ADDRESS MARK NOT FOUND

Set if the first two bytes of the data field following an ID match are not A1 F8. This condition is checked for Read Sector commands only.

3.3.2 WRITE PRECOMP CYLINDER REGISTER (HA9, HA2 THRU HA0 = 01, WRITE)

This register is used to control the Reduce Write Current (RWC) signal going to the drive. RWC is turned on if the present position cylinder number is greater than or equal to the 4 times the write precomp cylinder number. If the write precomp cylinder number is 'FF' hex, then the RWC is never asserted.

3.3.3 SECTOR COUNT REGISTER (HA9, HA2 THRU HA0 = 02, READ/WRITE)

This register is used in read sector, write sector, and format commands to implement multiple sector handling with one command. A value of 1 indicates a single sector transfer, a value of 2 indicates a 2 sector transfer, and so forth. A value of 0 indicates a 256 sector transfer. Sector count is decremented and the sector number is incremented after each sector transfer between the buffer and host or drive.

3.3.4 SECTOR NUMBER REGISTER (HA9, HA2 THRU HA0 = 03, READ/WRITE)

The sector number register is used to hold the number of the desired sector for read and write commands. The sector number can range from 0 to 255.

3.3.5 CYLINDER NUMBER LOW AND HIGH REGISTERS (CYLINDER NUMBER LOW: HA9, HA2 THRU HA0 = 04, READ/WRITE. CYLINDER NUMBER HIGH: HA9, HA2 THRU HA0 = 05, READ/WRITE)

These registers specify the cylinder number for read, write, and format commands. The cylinder number may range in value from 0 to 2047. Cylinder number low register holds the 8 least significant bits of the desired cylinder number. Cylinder number high register holds the three most significant bits of the desired cylinder number in bits 0 through 2. Bits 3 through 7 are not normally used in disk controller boards. These bits are latched when writing to this register. This means that all 8 bits can be used to transfer information between the host and the local microcontroller.

3.3.6 SDH REGISTER (HA9, HA2 THRU HA0 = 06, READ/WRITE)

This register is used to specify the desired drive and head numbers and to specify CRC or ECC mode.

Bit							
7	6	5	4	3	2	1	0
CRC/0 ECC	SS	Drive	Head Number				

3.3.6.1 BIT 7 ECC/CRC SELECT

This bit is set for data field ECC mode. It is reset for data field CRC mode.

3.3.6.2 BIT 5 SECTOR SIZE

Bit 5 (SS0) is used to select sector size. If SS0 = 0, then the sector size is 256 bytes and if SS0 = 1, then the sector size is 512 bytes.

3.3.6.3 BIT 4 DRIVE SELECT

Bit 4 specifies the desired drive number. This bit also determines which of the two internal drive status registers are read when the host accesses the host status register or alternate status register. If DS = 0, the host receives drive zero status. If DS = 1, then the host receives drive one status.

3.3.6.4 BITS 3 THROUGH 0 HEAD NUMBER

Bits 3, 2, 1 and 0 specify the desired head number.

3.3.7 HOST STATUS REGISTER (HA9, HA2 THRU HA0 = 7, READ)

The status register reads only and reflects the status of the controller as well as the status of certain drive control lines. Some of the status bits are controlled by the local microcontroller. Drive status comes from two registers in the WD42C22A, one for each drive. Bit 4 of the SDH register in the AT task file copy controls which of the two registers is read when the host reads this port. Reading of the status register by the host resets INTRQ. The description of the status register bits follows:

Bit							
7	6	5	4	3	2	1	0
ABSY	RDY	WF	SC	DRQ	DWC	IDX	ERR

3.3.7.1 BIT 7 AT BUSY

This bit is active (=1) when the controller is accessing the disk. ABSY is activated by the start of a command (writing into the host command register). It is deactivated at end of all commands by the local microcontroller. This bit is also set during a reset.

3.3.7.2 BIT 6 DRIVE READY

This bit reflects the state of the DRDY drive status pin. Any command aborts if DRDY is low. This bit is written by the local microcontroller.

3.3.7.3 BIT 5 WRITE FAULT

This bit reflects the state of the WF drive status pin. Any command aborts if WF is high. This bit is written by the local microcontroller.

3.3.7.4 BIT 4 SEEK COMPLETE

This bit reflects the state of the SC signal coming from the drive. This bit is written by the local microcontroller.

3.3.7.5 BIT 3 DATA REQUEST

This bit is asserted when the host should be transferring data between the RAM buffer and host. This bit is controlled by the buffer manager.

3.3.7.6 BIT 2 DATA WAS CORRECTED

This bit indicates that an error in the data field was detected and corrected. The buffer contains corrected data. This bit is written by the local microcontroller.

3.3.7.7 BIT 1 INDEX

This bit reflects the state of the INDEX pin.

3.3.7.8 BIT 0 ERROR

This bit indicates that a non-recoverable error has occurred. The error register describes the error condition when this bit is active. This bit is written by the local microcontroller.

3.3.8 HOST COMMAND REGISTER (HA9, HA2 THRU HA0 = 7, WRITE)

The command to be executed is written into this register. Writing this register sets ABSY in the status register and asserts the $\overline{\text{MCINT}}$ pin going to the local microcontroller. The command latches in a register which the local microcontroller reads. Writing this register resets INTRQ.

3.3.9 ALTERNATE STATUS REGISTER (HA9, HA2 THRU HA0 = E, READ)

This register is the same as the host status register (7) but mapped at a different address. Refer to page 23 for the bit description.

3.3.10 FIXED DISK REGISTER (HA9, HA2 THRU HA0 = E, WRITE)

The fixed disk register is used by the host to control some of the internal functions of the WD42C22A. Bit 0 and bits 4 through bit 7 are reserved for future definition. These bits are currently not used in the AT protocol but they are implemented in the WD42C22A, i.e. the fixed disk register passes 8 bits between the host and the

local microcontroller. The host should write zeros to these bits in AT mode. The fixed disk register is coded as follows:

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	HS3EN	RST	$\overline{IEN}$	0

3.3.10.1 BIT 3 HEAD SELECT 3 ENABLE

When HS3EN = 1, then HEAD SELECT 3 is asserted by the local microcontroller. When HS3EN = 0, then RWC is asserted by the local microcontroller.

3.3.10.2 BIT 2 RESET

Writing a 1 to this bit resets the WD42C22A. The RESET output is asserted and remains asserted until this bit is written back to 0. This bit must be on for a minimum of 5.0 µsec. If reset has been disabled by the local microcontroller then writing a '1' to this bit only resets the WD42C22A. $\overline{RESET}$ is not asserted in this case. The WD42C22A asserts $\overline{MCINT}$ and the local microcontroller is responsible for resetting the drive controller board logic.

3.3.10.3 BIT 1 $\overline{INTERRUPT\ ENABLE}$

When $\overline{IEN}$ = 0, then the $\overline{INTRQ}$ output to the host is enabled. When $\overline{IEN}$ = 1, then the INTRQ output to the host is disabled. Disabling interrupts does NOT reset an existing interrupt but inhibits all further interrupts. Any interrupts pending when this bit is set causes the INTRQ output to be asserted. A system master reset does NOT affect the $\overline{IEN}$ bit but resets any existing interrupt. The internal power qualified reset sets $\overline{IEN}$ to 1. When interrupts are disabled, then the INTRQ pin is tri-stated.

3.3.11 DIGITAL INPUT REGISTER (HA9, HA2 THRU HA0 = F, READ)

The digital input register is used by the host to determine the state of $\overline{WRITE\ GATE}$ and the drive selects and head selects. Bit 5 is written by the local microcontroller when HS3EN (bit 3 of the fixed disk register) is set to zero. Bit 5 comes from bit 3 of the host SDH register with HS3EN set to one. Bits 0 through bit 4 also come from the host SDH register. When this register is read by the host, then HD7 (pin 82) is tri-stated. It is coded as follows:

Bit							
7	6	5	4	3	2	1	0
X	$\overline{WG}$	$\overline{HS3/RWC}$	$\overline{HS2}$	$\overline{HS1}$	$\overline{HS0}$	$\overline{DS2}$	$\overline{DS1}$

3.3.11.1 BIT 6 WRITE GATE ON

This bit reflects the state of the $\overline{WG}$ output pin.

3.3.11.2 BIT 5 HEAD SELECT 3/ REDUCE WRITE CURRENT

This bit reflects the state of the $\overline{HS3/RWC}$ drive control output. The $\overline{RWC}$ bit is written by the local microcontroller. $\overline{HS3}$ comes from the SDH register bit 3.

3.3.11.3 BIT 4, BIT 3, AND BIT 2 HEAD SELECTS

These bits reflect the states of the $\overline{HS2}$, $\overline{HS1}$, $\overline{HS0}$, and drive control outputs respectively. These bits are controlled by SDH register bits 2 through 0 respectively.

3.3.11.4 BIT 1 AND BIT 0 DRIVE SELECTS

These bits indicate which drive is currently being selected by the host. They are controlled by the SDH register bit 4.

ADB7	ADB6	ADB5	ADB4	ADB3	ADB2	ADB1	ADB0	READ PORT	WRITE PORT
DISK CONTROLLER TASK FILE									
0	0	0	X	X	X	X	X	BUS TRISTATE	NOT USED
0	0	1	0	0	0	0	0	INVALID	INVALID
0	0	1	0	0	0	0	1	Error Register	PLO Length
0	0	1	0	0	0	1	0	Sector Count	Sector Count
0	0	1	0	0	0	1	1	Sector Number	Sector Number
0	0	1	0	0	1	0	0	Cylinder Number Low	Cylinder Number Low
0	0	1	0	0	1	0	1	Cylinder Number High	Cylinder Number High
0	0	1	0	0	1	1	0	SDH	SDH
0	0	1	0	0	1	1	1	Status Register	Command Register
XT									
0	0	1	0	1	1	0	1	Hardware Status	Hardware Status
0	0	1	0	1	1	1	0	NOT USED	Drive Configuration
BUFFER MANAGER									
0	1	1	0	0	0	0	0	Host Buffer Pointer Low	Host Buffer Pointer Low
0	0	1	1	0	0	0	1	Host Buffer Pointer High	Host Buffer Pointer High
0	0	1	1	0	0	1	0	Host Transfer Count Low	Host Transfer Count Low
0	0	1	1	0	0	1	1	Host Transfer Count High	Host Transfer Count High
0	0	1	1	0	1	0	0	Disk Buffer Pointer Low	Disk Buffer Pointer Low
0	0	1	1	0	1	0	1	Disk Buffer Pointer High	Disk Buffer Pointer High
0	0	1	1	0	1	1	0	Microcontroller RAM Access	Microcontroller RAM Access
0	0	1	1	0	1	1	1	Buffer Status	Buffer Control
0	0	1	0	1	1	1	1	Auxilliary Buffer Status	Auxilliary Buffer Control

TABLE 11. LOCAL MICROCONTROLLER REGISTER MAP

3.4 SLAVE HOST INTERFACE

In slave mode, the WD42C22A host interface can be hooked up to a peripheral device such as the WD33C93 (SBIC). The microcontroller reads and writes the peripheral device through the WD42C22A using the ports as follows:.

ABSY	ADB7	ADB6	ADB5	ADB4	ADB3	ADB2	ADB1	ADB0	READ PORT	WRITE PORT
X	0	1	0	0	1	0	0	0	Bus tri-state	Slave address port for reads
X	0	1	0	0	1	0	1	0	Bus tri-state	Slave address port for writes
X	0	1	0	0	1	0	0	1	Slave read data	Slave write data

ABSY	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	READ PORT	WRITE PORT
MISC.										
X	0	0	1	1	1	0	0	0	Interface Status	Interface Control
X	0	0	1	1	1	0	0	1	Configuration Status Low	NOT USED
X	0	0	1	1	1	0	1	0	Configuration Status High	NOT USED
X	0	0	1	1	1	0	1	1	Drive Interface Status	Drive Interface Control
X	0	0	1	1	1	1	0	0	Alternate Sector Number	NOT USED
AT INTERFACE										
X	0	0	1	1	1	1	0	1	Drive 0 Status	Drive 0 Status
X	0	0	1	1	1	1	1	0	Drive 1 Status	Drive 1 Status
X	0	0	1	1	1	1	1	1	Fixed Disk Register	Digital Input Register
AT INTERFACE (TASK FILE COPY)										
1	0	1	0	0	0	0	0	1	Write Precomp Cylinder	Error Register
1	0	1	0	0	0	0	1	0	Sector Count	Sector Count
1	0	1	0	0	0	0	1	1	Sector Number	Sector Number
1	0	1	0	0	0	1	0	0	Cylinder Number Low	Cylinder Number Low
1	0	1	0	0	0	1	0	1	Cylinder Number High	Cylinder Number High
1	0	1	0	0	0	1	1	0	SDH	SDH
1	0	1	0	0	0	1	1	1	Command Register (from Host)	NOT USED
SLAVE HOST										
0	0	1	0	0	0	X	X	X	INVALID	INVALID
X	0	1	0	0	1	0	0	0	INVALID	Slave Address Port for reads
X	0	1	0	0	1	0	1	0	INVALID	Slave Address Port for writes
X	0	1	0	0	1	0	0	1	Slave Read Data	Slave Write Data
X	0	1	0	0	1	X	X	X	INVALID	NOT USED
X	0	1	0	1	X	X	X	X	INVALID	NOT USED
X	0	1	1	X	X	X	X	X	BUS TRISTATE	NOT USED
X	1	X	X	X	X	X	X	X	BUS TRISTATE	NOT USED

TABLE 11. LOCAL MICROCONTROLLER REGISTER MAP (CONT'D)

The slave peripheral connects to the WD42C22A using an ALE type interface. Register reads and writes are always 8-bit. The procedure to read or write a slave peripheral register is to first write the register number to the slave address port before the register contents are read or written. This address must always be written before each register access even when consecutively accessing the same register two or more times.

Data transfers between the peripheral device and the WD42C22A are WD-bus mode and can be either 8-bit or 16-bit and is controlled by the H16/8 bit (bit 1 of the auxilliary buffer control register).

The slave mode is enabled by the HSMB bit (bit 6 of the auxilliary buffer control register).

3.5 LOCAL MICROCONTROLLER INTERFACE ORGANIZATION

The local microcontroller controls the host interface mode (AT or XT) and controls the buffer manager and the drive controller. The local microcontroller is usually in a sleep state until it is told to do something by the assertion of the MCINT output. In the XT mode, MCINT is asserted when the controller is selected. In the AT mode, MCINT is asserted when the host writes to the command register. In slave host mode, MCINT is asserted when the slave peripheral device asserts its INTRQ signal. MCINT is also asserted at the end of each host or disk transfer regardless of the interface mode.

The local microcontroller can have either the Intel-type (8051) or the Motorola-type (68HC11) interface. The WD42C22A has a built-in M-Otorola-inTEL (MOTEL) circuit which can sense the processor interface type and can therefore be directly interfaced to either type processor.

Table 11 lists the register map for the local microcontroller.

3.6 DISK CONTROLLER TASK FILE (AD7 THRU AD0 = 20 THRU 27)

3.6.1 ERROR REGISTER (AD7 THRU AD0 = 21, READ)

The error register reads only and contains the specific error status pertaining to a command. The meaning of the status register bits are as follows:

Bit							
7	6	5	4	3	2	1	0
BB	CRC/ ECC	RIDF	IDNF	0	AC	0	DMNF

3.6.1.1 BIT 7 BAD BLOCK

A bad block address mark has been detected when trying to read or write that sector. The data field is not be read or written.

3.6.1.2 BIT 6 CRC/ECC DATA FIELD ERROR

A CRC error in the data field has been detected when in CRC mode. In ECC mode, data errors were detected in the data.

3.6.1.3 BIT 5 RELOCATION ID FOUND

This bit is set if a relocation ID is found after detecting the bad block mark in the desired sector's ID field. This bit is only valid if the R option is used in the set parameter command.

3.6.1.4 BIT 4 ID NOT FOUND

Occurs when cylinder, head, sector, size parameters with a correct ID field CRC cannot be found. For all commands, this bit is set after 10 index pulses if the ID is not found if T = 0. For all commands with the retry disable bit set, this bit indicates that after 2 index pulses no matching ID field was found.

3.6.1.5 BIT 3 RESERVED

Not used, forced to zero.

3.6.1.6 BIT 2 ABORTED COMMAND

Set if command was started and one of the following conditions occurred:

- 1. Drive not ready
- 2. Write fault
- 3. Illegal command code.

3.6.1.7 BIT 1 RESERVED

Not used in WD42C22A, forced to zero.

3.6.1.8 BIT 0 DATA ADDRESS MARK NOT FOUND

Set if the first two bytes of the data field following an ID match are not A1 F8. This condition is checked for read sector commands only.

3.6.2 PLO LENGTH REGISTER (AD7 THRU AD0 = 21, WRITE)

This register is used for two purposes:

- 1. To determine the length of the Data PLO sync field during write commands and to determine the length of the ID PLO sync field during format commands. The contents of this register regulates the PLO field size in all data coding modes.
- 2. To load a value in the internal GAP register. During the load parameter block command the

contents of the lower six bits of the PLO length register are transferred to the internal GAP register. In hard sector mode, this internal GAP register is used to control the delay between the INDEX or SECTOR pulse and the leading edge of READ GATE. This GAP register is altered by loading the desired GAP register value into the PLO length register and then issuing a load parameter block command.

3.6.3 SECTOR COUNT (AD7 THRU AD0 = 22, READ/WRITE)

Bit							
7	6	5	4	3	2	1	0
NUMBER OF SECTORS/GAP VALUE SECTOR WITH BAD BLOCK							

This register is used for three purposes:

- 1. The sector count register is used in read sector, write sector, and format commands to implement multiple sector handling with one command. A value of 1 indicates a single sector transfer, a value of 2 indicates a 2 sector transfer, and so forth. A value of 0 indicates a 256 sector transfer. Sector count decrements and sector number increments after each sector transfer to or from the buffer.
- 2. To load a value into the internal gap value register. During the load parameter block command the contents of this register are transferred into an internal gap value register. This gap value register specifies the data byte written into the gaps during format commands.
- 3. To specify to the microcontroller the sector number where a bad block bit was detected if relocation ID searches are enabled. If the R option is set in a set parameter command, then during read and write commands if a bad block is detected, the WD42C22A searches for a special ID field containing relocation information. When the command terminates due to a bad block, then the sector number of the sector with the bad block is returned to the microcontroller in this register. This is true whether or not the relocation information is detected.

3.6.4 SECTOR NUMBER REGISTER (AD7 THRU AD0 = 23, READ/WRITE)

Bit							
7	6	5	4	3	2	1	0
SECTOR NUMBER / GAP SIZE							

The sector number register has three uses:

- 1. To hold the number of the desired sector for read and write commands. The sector number can range from 0 to 255.
- 2. To control the Gap 1 and Gap 3 sizes during format commands. The sector number holds the number of gap bytes minus three for format (number of gap bytes minus six for NRZ mode).
- 3. To load a value into the internal pad value register. During the load parameter block command the contents of this register are transferred into an internal pad value register. This pad value register specifies the data byte written into the ID and DATA pads during format and write commands.

3.6.5 CYLINDER NUMBER REGISTERS (CYLINDER NUMBER LOW: AD7 THRU AD0 = 24, READ WRITE CYLINDER NUMBER HIGH: AD7 THRU AD0 = 25, READ/WRITE)

This register has two functions:

- 1. To specify the cylinder number for read, write, and format commands. The cylinder number may range in value from 0 to 2047.
- 2. The cylinder number register is used during a load parameter block command to specify the desired sector size if a non-standard sector size is desired and to specify the offset for a write ID command. To load the internal sector size register, load in the desired sector size into the cylinder registers. Next, issue a load parameter block command. Set U=1 to enable the programmable sector size or programmable write ID offset.

3.6.6 CYLINDER NUMBER REGISTERS (CYLINDER NUMBER LOW: AD7 THRU AD0 = 24, READ/WRITE CYLINDER NUMBER HIGH: AD7 THRU AD0 = 25, READ/WRITE)

Cylinder number low register holds the 8 least significant bits of the desired cylinder number or the 8 least significant bits of the desired sector size.

Cylinder number high register holds the three most significant bits (bits 0 through 2) of the desired cylinder number or the three most significant bits of the desired sector size. Bits three through seven of the cylinder number high register are not used and must be set to zero.

3.6.7 SDH REGISTER (AD7 THRU AD0 = 26, READ/WRITE)

This register is used to specify the desired drive and head numbers and to specify CRC or ECC mode. There are two SDH modes available, three or four bit head number. Three bit head mode is the default after a master reset. Setting the H bit in the set parameter command engages the four bit head mode.

3.6.7.1 SDH REGISTER, THREE BIT HEAD NUMBER

Bit							
7	6	5	4	3	2	1	0
CRC/ ECC	SS1	SS0	Drive #		Head #		

3.6.7.2 SDH REGISTER, FOUR BIT HEAD NUMBER

Bit							
7	6	5	4	3	2	1	0
CRC/ ECC	SS1	SS0	Drive #	Head #			

3.6.7.3 BIT 7 ECC/CRC SELECT

This bit is set for data field ECC mode. It is reset for data field CRC mode. In RLL mode, this bit is ignored. RLL mode always uses 7-byte ECC. The CRC/ECC flag bit is not written on the disk at format time. The bad block flag is written on the disk in its place.

3.6.7.4 BIT 6 AND BIT 5 SECTOR SIZE

Bits 6 and 5 contain sector size bits. These bits are written on the disk at format time. These bits should be 0 if programmable sector size is used. These bits are reserved for special flags in programmable sector size mode. The possible sector sizes and their selection codes are as follows:

SS1	SS0	Sector Size
0	0	256 byte data field
0	1	512 byte data field
1	0	1024 byte data field
1	1	128 byte data field

The sector sizes can be optionally specified to be any value between 100 and 2048 bytes by using the load parameter block command. The user is responsible for validating the effectiveness of the ECC for sector sizes over 1056 bytes.

3.6.7.5 BIT 4 AND BIT 3 DRIVE NUMBER (THREE BIT HEAD NUMBER) BIT 4 DRIVE NUMBER (FOUR BIT HEAD NUMBER)

Bits 4 and 3 specify the desired drive number in three bit head number mode. Only bit 4 specifies the drive number in four bit head number mode. The local microcontroller is responsible fortransferring these bits to the DS1 and DS0 output pins.

3.6.7.6 BIT 2, BIT 1, AND BIT 0 THREE BIT HEAD NUMBER BIT 3, BIT 2, BIT 1, AND BIT 0 FOUR BIT HEAD NUMBER

Bits 2, 1, and 0 specify the desired head number in the three bit mode. Bits 3, 2, 1, and 0 specify the desired head number in four bit mode. The local microcontroller is responsible for outputting these bits to the drive.

NOTE

These bits are written on the disk at format time. The SDH byte written in the ID field during a format command is NOT the same as the SDH register. The SDH format byte is shown as follows:

3.6.7.7 SDH ID FIELD FORMAT BYTE (THREE BIT HEAD MODE)

Bit							
7	6	5	4	3	2	1	0
Bad Block	SS1	SS0	0	0	Head #		

3.6.7.8 SDH ID FIELD FORMAT BYTE (FOUR BIT HEAD MODE)

Bit							
7	6	5	4	3	2	1	0
Bad Block	SS1	SS0	0	Head #			

3.6.8 STATUS REGISTER (AD7 THRU AD0 = 27, READ)

The status register is read only and reflects the status of the controller as well as the status of certain drive control lines. If command in progress (bit 1) is set then no other register reads are valid and none of the other register bits are valid. The status register contents are returned for any read and all writes are disabled. The description of the status register bits follows:

Bit							
7	6	5	4	3	2	1	0
0	RDY	WF	1	0	0	0	ERR

3.6.8.1 BIT 7 ALWAYS 0

This bit is always zero when the microcontroller has access to this status register.

3.6.8.2 BIT 6 DRIVE READY

This bit reflects the status of the DRDY. Any command aborts if DRDY is low.

3.6.8.3 BIT 5 WRITE FAULT

This bit reflects the state of the WF pin. Any command aborts if WF is high.

3.6.8.4 BIT 4 ALWAYS 1

This bit reflects the state of the SC input to the drive controller. This signal is internally tied to V_{DD}.

3.6.8.5 BIT 3 ALWAYS 0

This bit reflects the state of the BDRQ signal that goes between the drive controller and the buffer manager. It is always zero when the microcontroller has access to this status register.

3.6.8.6 BIT 2 NOT USED

Forced to 0

3.6.8.7 BIT 1 ALWAYS 0

This bit reflects the state of the command in progress signal in the drive controller. It is always zero when the microcontroller has access to this status register.

3.6.8.8 BIT 0 ERROR

This bit indicates that a non-recoverable error has occurred. The error register describes the error condition when this bit is asserted.

Drive ready and write fault bits reflect the state of their associated input pins. The states of these status register bits are latched at the end of the command and are unlatched after the first status register read. Reading the status register results in the disk controller interrupt being reset.

32

3.6.9 COMMAND REGISTER (AD7 THRU AD0 = 27, WRITE)

The command to be executed is written into this register. Writing this register sets the internal BUSY and CIP signals and causes the controller to start executing the desired command. Writing this register resets the disk controller interrupt (DCI bit in the interface status register).

3.7 XT INTERFACE PORTS

3.7.1 XT HOST HARDWARE STATUS (AD7 THRU AD0 = 2D, READ/WRITE)

Bits 7, bit 6, bit 2, and bit 1 of this register are written by the local microcontroller and read by the host. The other bits reflect the state of certain hardware signals. This register is readable and valid in all host modes.

Bit							
7	6	5	4	3	2	1	0
1	1	IRQ	DRQ	XBSY	C/$\overline{D}$	I/$\overline{O}$	REQ

3.7.1.1 BITS 6 AND 7 UNDEFINED

These bits are currently undefined in the XT protocol and read as 1.

3.7.1.2 BIT 5 INTERRUPT REGUEST

This bit reflects the state of the INTRQ output. This bit can NOT be written by the microcontroller.

3.7.1.3 BIT 4 DMA REQUEST

This bit reflects the state of the DREQ output. This bit can NOT be written by the microcontroller.

3.7.1.4 BIT 3 XT BUSY

This bit reflects the state of the internal XT BUSY flipflop. This bit is set by during a reset and is set when the WD42C22A is selected in XT mode. This bit can NOT be written by the microcontroller.

3.7.1.5 BIT 2 COMMAND / $\overline{\text{DATA}}$

This bit tells the host which type of transfer is expected at the read data and write data ports. C/$\overline{\text{D}}$ = 1 indicates that a command or status transfer is expected and C/$\overline{\text{D}}$ = 0 indicates that a data transfer is expected. This bit is written by the microcontroller.

3.7.1.6 BIT 1 INPUT / $\overline{\text{OUTPUT}}$

This bit tells the host the direction of transfer for the two data ports. I/$\overline{\text{O}}$ = 1 indicates an input (read) by the host and I/$\overline{\text{O}}$ = 0 indicates an output (write) by the host. This bit is written by the microcontroller.

3.7.1.7 BIT 0 REQUEST

This bit indicates the state of the internal host transfer enable. This bit is active when the buffer manager is transferring data between the RAM and the host. This bit can NOT be written by the microcontroller. This bit is identical to the DRQ in the drive zero status and drive one status registers used in AT mode.

3.7.2 HOST DRIVE CONFIGURATION (AD7 THRU AD0 = 2E, WRITE)

This register is used to write the drive configuration information that is read by the host.

3.7.3 BUFFER MANAGER REGISTERS (AD7 THRU AD0 = 30 THRU 37) HOST BUFFER POINTER LOW (AD7 THRU AD0 = 30, READ/WRITE) HOST BUFFER POINTER HIGH (AD7 THRU AD0 = 31, READ/WRITE)

Bit							
7	6	5	4	3	2	1	0
LEAST SIGNIFICANT BYTE OF HOST BUFFER POINTER							

Bit							
7	6	5	4	3	2	1	0
0	MOST SIGNIFICANT BITS OF HOST BUFFER POINTER						

The host buffer pointer low register contains the least significant byte of the host buffer pointer. The host buffer pointer high register contains the seven most significant bits of the host buffer pointer. The host buffer pointer is used as the base address for the internal host buffer counter. The contents of the host buffer pointer registers are transferred to the host buffer pointer counter under the control of the buffer control register.

When the AHBP bit is set in the control register, then the pointer register is transferred to the pointer counter when the transfer counter reaches zero. If the transfer count is already zero, then the transfer occurs immediately. This allows a pending transfer to be queued behind the current transfer. When the pointer is transferred to the counter, the AHBP buffer status bit resets.

3.7.4 HOST TRANSFER COUNT LOW (AD7 THRU AD0 = 32, READ/WRITE) HOST TRANSFER COUNT HIGH (AD7 THRU AD0 = 33, READ/WRITE)

The host transfer count low register contains the least significant byte of the host transfer count. The host transfer count high register contains the most significant bits of the host transfer count. The transfer count controls the number of bytes that are to be transferred on the host interface. The transfer count register is transferred to the internal transfer counter at the same time that the host buffer pointer register is transferred to the

host buffer pointer counter. The transfer counter is 12 bits long which gives a maximum transfer count of 4095 bytes.

Bit							
7	6	5	4	3	2	1	0
LEAST SIGNIFICANT BYTE OF HOST TRANSFER COUNT							

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	MS BITS OF HOST TRANSFER COUNT			

3.7.5 DISK BUFFER POINTER LOW (AD7 THRU AD0 = 34, READ/WRITE) DISK BUFFER POINTER HIGH (AD7 THRU AD0 = 35, READ/WRITE)

The disk pointer low register contains the least significant byte of the disk buffer pointer. The disk pointer high register contains the seven most significant bits of the disk buffer pointer. The disk buffer pointer is used as the base address for the internal disk buffer counter. The contents of the disk buffer pointer registers are transferred to the disk buffer pointer counter under the control of the buffer control register. When the ADBP bit is set in the control register, then the pointer is transferred to the counter when the drive controller sets DRQI to 1 (bit 1) in the interface status register (38 hex). This allows a pending transfer to be queued behind the current transfer. When the pointer register is transferred to the counter, the ADBP bit in the buffer status resets. If ADBP=0 when the drive controller sets DRQI to 1, then the drive controller stops transferring data to the buffer and discontinues the command until ADBP sets.

Bit							
7	6	5	4	3	2	1	0
LEAST SIGNIFICANT BYTE OF DISK BUFFER POINTER							

Bit							
7	6	5	4	3	2	1	0
0	MOST SIGNIFICANT BYTE OF DISK BUFFER POINTER						

3.7.6 MICROCONTROLLER RAM ACCESS PORT (AD7 THRU AD0 = 36, READ/WRITE)

This port is used by the local microcontroller to access the buffer RAM. Accesses to this port go through the drive controller's FIFO. These accesses are enabled by the MAC bit in the drive interface control register. The DRWB bit in the buffer manager control register controls the direction of the accesses.

3.7.7 BUFFER CONTROL REGISTER (AD7 THRU AD0 = 37, WRITE)

This register is used to control the buffer manager.

Bit			
7	6	5	4
AT/$\overline{XT}$	RDCFG	RXC	AHBP
3	2	1	0
HRWB	DRWB	BDEN	ADBP

3.7.7.1 BIT 7 AT / $\overline{XT}$ INTERFACE CONTROL

This bit, along with HSMB, in the auxilliary buffer control register, controls the host interface type. If AT/$\overline{XT}$ = 0, then the interface is XT type if HSMB = 0. If AT/$\overline{XT}$ = 1, then the interface is AT type if HSMB = 0. This bit has no meaning if HSMB = 1. The RESET input and the host soft reset does not affect this bit.

3.7.7.2 BIT 6 READ CONFIGURATION

When this bit is set, all buffer address outputs are placed in a medium impedence state with each buffer address pin having a 180 µA current source pulldown. The buffer manager should be idle when this mode is enabled. This mode is used to read configuration switch information. The microcontroller should wait 100 µsec after setting this bit before reading the configuration registers. This bit resets when $\overline{RESET}$ is asserted.

3.7.7.3 BIT 5 RESET TRANSFER COUNTER

When this bit is set, the internal transfer counter and the host FIFO pointers reset. This bit resets after the transfer counter and FIFO reset.

3.7.7.4 BIT 4 ARM HOST BUFFER POINTER

Writing a '1' to this bit, sets an internal latch. Writing a '0' to this bit has no effect. When this bit is set, then when the internal transfer counter reaches zero the host buffer pointer is transferred to the internal host buffer counter and the host transfer count is transferred to the internal transfer counter. This bit is reset by the WD42C22A after the host pointer and count registers are transferred. This bit resets when $\overline{\text{RESET}}$ is asserted.

3.7.7.5 BIT 3 HOST READ / $\overline{\text{WRITE}}$

This bit controls the direction of the host data transfers. It is used internally to control the direction of the FIFO. When HRWB = 0, then the host writes to the WD42C22A. When HRWB = 1, then the host reads from the WD42C22A.

3.7.7.6 BIT 2 DISK READ / $\overline{\text{WRITE}}$

This bit controls the direction of the disk or local microcontroller data transfers. It is used internally to control the direction of the disk FIFO. When DRWB = 0, then the disk controller or local microcontroller writes to the buffer RAM. When DRWB = 1, then the disk controller or local microcontroller reads from the buffer RAM. When the microcontroller accesses the buffer RAM, then this bit should be written before the ADBP bit is set.

3.7.7.7 BIT 1 BURST DMA ENABLE

When BDEN = 1 and HDMA = 1 in the auxilliary buffer control register, then burst DMA transfers are enabled on the host interface.

3.7.7.8 BIT 0 ARM DISK BUFFER POINTER

Writing a '1' to this bit, sets an internal latch. Writing a '0' to this bit has no effect. When this bit is set, then the disk buffer pointer is transferred to the internal disk buffer counter when the drive controller sets the BDRQ interrupt. This bit also enables the disk controller to continue to the next sector. This bit is reset by the WD42C22A after the pointer registers have been transferred. When the disk controller port is used by the local microcontroller to access the buffer RAM, then setting this bit resets the disk FIFO pointers and the next byte read or written by the microcontroller will be at the new address loaded into the disk buffer pointer.

3.7.8 BUFFER STATUS REGISTER (AD7 THRU AD0 = 37, READ)

This register reflects the status of the buffer manager logic.

Bit			
7	6	5	4
AT/$\overline{\text{XT}}$	RDCFG	RXC	AHBP
3	2	1	0
HRWB	DRWB	BDEN	ADBP

3.7.8.1 BIT 7 AT / $\overline{\text{XT}}$ INTERFACE MODE

This status bit reflects the state of the AT/$\overline{\text{XT}}$ control bit defined above.

3.7.8.2 BIT 6 READ CONFIGURATION

This bit reflects the state of the read configuration control bit defined in the buffer manager control register.

3.7.8.3 BIT 5 RESET TRANSFER COUNTER

This bit reflects the state of the RXC control bit defined in the buffer control register.

3.7.8.4 BIT 4 HOST BUFFER POINTER ARMED

This bit reflects the state of the AHBP control bit defined in the buffer control register.

3.7.8.5 BIT 3 HOST READ / $\overline{\text{WRITE}}$

This bit reflects the state of the HRWB control bit defined in the buffer control register.

3.7.8.6 BIT 2 DISK READ / $\overline{\text{WRITE}}$

This bit reflects the state of the DRWB control bit defined in the buffer control register.

3.7.8.7 BIT 1 BURST DMA ENABLE

This bit reflects the state of the BDEN control bit defined in the buffer control register.

3.7.8.8 BIT 0 DISK BUFFER POINTER ARMED

This bit reflects the state of the ADBP control bit defined in the buffer control register.

3.7.9 AUXILLIARY BUFFER CONTROL REGISTER (AD7 THRU AD0 = 2F, WRITE)

This register is used for additional control of the buffer manager and host interface.

Bit			
7	6	5	4
HDMA	HSMB	BCNT	IDD
3	2	1	0
DSEL	X	H16/$\overline{8}$	SCKS

3.7.9.1 BIT 7 HOST DMA

This bit controls the host data transfers to/from the buffer RAM. If HDMA = 1, then the data is transferred to the host via DMA regardless of the host interface selected. If HDMA = 0, the default, then data is transferred via programmed I/O.

3.7.9.2 BIT 6 HOST SLAVE / $\overline{\text{MASTER}}$

When HSMB = 0, the default, then the host is a master which drives the WD42C22A in either XT or AT type interface. When HSMB = 1, then the host is a slave device which is controlled by the local microcontroller. The slave device can be addressed in either ALE or indirect mode. The SBIC is an example of a device which can be connected to the WD42C22A. The ALE mode supports up to 32 registers in the slave device. Data transfers occur via WD-BUS mode if HDMA = 1 and is an 8-bit transfer if H16/$\overline{8}$ = 0 and a 16-bit if H16/$\overline{8}$ = 1. This bit resets upon power-up but not affected by $\overline{\text{RESET}}$.

3.7.9.3 BIT 5 BURST CONTINUOUS

This bit, along with the HDMA bit, and the BDEN bit in the buffer control register control the bursting of data during DMA transfers. If BCNT = 1, HDMA = 1, and BDEN = 1, then the WD42C22A DMAs data continuously as long as the FIFOs can keep up. If BCNT = 0, HDMA = 1, and BDEN = 1, then the WD42C22A DMAs data in 8-byte or 16-byte maximum length bursts, for 8 and 16 bit host data bus width, respectively.

3.7.9.4 BIT 4 INTELLIGENT DRIVE DECODE

When IDD = 1, then the controller is assumed to be on an intelligent drive. The HD0-15, INTRQ, and DREQ/$\overline{\text{IOCS16}}$ outputs are always tri-stated if the drive is not selected. If IDD = 0, the default, then the outputs are controlled normally. This bit resets upon power up but not affected by $\overline{\text{RESET}}$.

3.7.9.5 BIT 3 DRIVE SELECT

This bit is used when IDD = 1 to control drive selection. If AT/$\overline{\text{XT}}$ =1, then the drive is considered selected when SDH register bit 4 equals DSEL. If AT/$\overline{\text{XT}}$ = 0, then the drive is considered selected if DSEL = 1 and not selected if DSEL = 0. This bit resets upon power-up but is not affected by $\overline{\text{RESET}}$.

3.7.9.6 BIT 1 HOST 16 / $\overline{8}$ BIT

This bit controls the width of the data transfers on the host side. If H16/$\overline{8}$ = 0, then the host data transfers are 8-bit. If H16/$\overline{8}$ = 1, then the host data transfers are 16-bit. This bit resets upon power up but is not affected by $\overline{\text{RESET}}$.

3.7.9.7 BIT 0 SYNCHRONOUS CLOCK SWITCH

This bit is used to control the clocking of the drive controller so that ESDI drives can be changed or data rates can bae changed without the need for external clock deglitching. When SCKS = 1, the default, then the WD42C22A synchronously switches the drive controller to the internal buffer clock (BCLK). When SCKS = 0, the WD42C22A switches the drive controller back to WCLK. The switch occurs only if both clocks are present. The CKSRC status bit defined below indicates whether or not the switch occurred. When $\overline{\text{RESET}}$ is asserted, the buffer clock clocks the drive controller during the reset and SCKS is set. The microcontroller must switch the clock source to the WCLK input prior to ussuing any commands to the drive controller.

3.7.10 AUXILLIARY BUFFER STATUS REGISTER (AD7 THRU AD0 = 2F, READ)

This register gives additional status of the buffer manager and host interface.

3.7.10.1 BIT 7 HOST DMA

This bit reflects the state of the HDMA control bit defined in the auxilliary buffer control register.

3.7.10.2 BIT 6 HOST SLAVE / $\overline{\text{MASTER}}$

This bit reflects the state of the HSMB control bit defined in the auxilliary buffer control register.

3.7.10.3 BIT 5 BURST CONTINUOUS

This abit reflects the state of the BCNT control bit defined in the auxilliary buffer control register.

3.7.10.4 BIT 4 INTELLIGENT DRIVE DECODE

This bit reflects the state of the IDD control bit defined in the auxillary buffer control register.

3.7.10.5 BIT 3 DRIVE SELECT

This bit reflects the state of the DSEL control bit defined in the auxilliary buffer control register.

3.7.10.6 BIT 2 CLOCK SOURCE

This bit indicates the source of the drive controller clock. If CKSRC = 1 and SCKS = 1, then the drive controller is being clocked by the buffer clock (BCLK). If CKSRC = 0 and SCKS = 0, then the drive controller is clocked by WCLK. If CKSRC = 1 and SCKS = 0 or CKSRC = 0 and SCKS = 1, then the clock source is undefined. CKSRC should not be checked until at least 10 clock periods after the SCKS has been written. The slower of BCLK and WCLK should be used in determining this delay.

3.7.10.7 BIT 1 HOST 16 / $\overline{8}$ BIT

This bit reflects the state of the H16/$\overline{8}$ control bit defined in the auxilliary buffer control register.

3.7.10.8 BIT 0 SYNCHRONOUS CLOCK SWITCH

This bit reflects the state of the SCKS control bit defined in the auxilliary buffer control register.

3.7.11 INTERFACE STATUS REGISTER (AD7 THRU AD0 = 38, READ)

This register is used to indicate the status of the WD42C22A. The bits are defined as follows:

Bit			
7	**6**	**5**	**4**
MINT	DCGI	RSTI	FEI
3	**2**	**1**	**0**
DCI	HPRI	DRQI	CWSI

3.7.11.1 BIT 7 MICROCONTROLLER INTERRUPT

This bit is high if the $\overline{\text{MCINT}}$ output pin is asserted. $\overline{\text{MCINT}}$ is the logical OR of seven sources:

- 1.) A host SDH register write
- 2.) A host soft reset
- 3.) A FIFO error
- 4.) The disk controller interrupt signal
- 5.) The host transfer count interrupt flip-flop
- 6.) The disk controller BDRQ signal
- 7.) The command write/select interrupt flip-flop.

If any of the bits 6 through 0 are set, then the MCINT bit is high.

3.7.11.2 BIT 6 DRIVE CHANGE INTERRUPT

This bit sets when the host writes a new value to the SDH register bit 4 when AT mode is selected.

3.7.11.3 BIT 5 SOFT RESET INTERRUPT

This bit sets if the host initiates a soft reset. This bit resets by writing the proper bit in the interface control register.

3.7.11.4 BIT 4 FIFO ERROR INTERRUPT

This bit sets if a FIFO overrun or underrun condition occurs during host or disk transfers. It resets by writing the proper bit in the interface control register.

3.7.11.5 BIT 3 DISK CONTROLLER INTERRUPT

This bit reflects the state of the disk controller interrupt signal. This interrupt occurs at the end of a command. This bit resets either when the disk controller status (port 27 hex) is read or when the disk controller command (port 27 hex) register is written.

3.7.11.6 BIT 2 HOST POINTER READY INTERRUPT

This bit reflects the state of the host transfer count interrupt flip-flop. This interrupt sets when the host transfer counter reaches zero and the FIFO is empty if the host pointer is not armed. It is also set when the host pointer pipeline register is loaded into the host pointer counter. It resets by writing the proper bit in the interface control register.

3.7.11.7 BIT 1 DISK BDRQ INTERRUPT

This bit reflects the state of the disk controller BDRQ signal. It sets when the disk controller starts a transfer between the disk controller and the sector buffer. It resets by writing the proper bit in the interface control register. If ADBP=0 (bit 0) in the buffer control register (37 hex) when this bit first goes from 0 to 1 then DRQI and MCINT is not reset until after the microcontroller writes ADBP=1.

3.7.11.8 BIT 0 COMMAND WRITE / SELECT / SLAVE INTERRUPT

This bit informs the local microcontroller that a command has been written if the WD42C22A is in AT mode, that the WD42C22A has been selected if it is in XT mode, or that the slave host device has issued an interrupt (Asserts INTRQ. Slave interrupt only triggers on rising edge of INTRQ.) if in slave host mode. This bit resets by writing the proper bit in the interface control register.

3.7.12 INTERFACE CONTROL REGISTER (AD7 THRU AD0 = 38, WRITE)

This register is used to control various parts of the WD42C22A. The bits are defined as follows:

Bit			
7	**6**	**5**	**4**
SIRQ	RDCI	RSRI	RFEI
3	**2**	**1**	**0**
RBSY	RHRI	RDQI	RCWS

3.7.12.1 BIT 7 SET INTERRUPT

Writing a '1' to this bit generates a host interrupt if interrupts are enabled.

3.7.12.2 BIT 6 RESET DRIVE CHANGE INTERRUPT

Writing a '1' to this bit resets the host SDH write interrupt flip-flop.

3.7.12.3 BIT 5 RESET SOFT RESET INTERRUPT

Writing a '1' to this bit resets the soft reset interrupt flip-flop. In AT mode, the microcontroller must wait for the RST bit (2) in the FDR register (3F hex) to be reset by the host before this interrupt can be reset.

3.7.12.4 BIT 4 RESET FIFO ERROR INTERRUPT

Writing a '1' to this bit resets the FIFO error interrupt flip-flop.

3.7.12.5 BIT 3 RESET BUSY

Writing a '1' to this bit resets the BSY status bit in the hardware status register if XT mode is selected or it resets the ABSY status bit in the host status register if AT mode is selected. In AT mode, this bit should only be set at the very end of a command after the last DRQ is asserted to the host. Internal logic handles ABSY during buffer transfers to the host.

3.7.12.6 BIT 2 RESET HOST POINTER READY INTERRUPT

Writing a '1' to this bit resets the host pointer ready interrupt flip-flop.

3.7.12.7 BIT 1 RESET DISK BDRQ INTERRUPT

Writing a '1' to this bit resets the disk BDRQ interrupt flip-flop.

3.7.12.8 BIT 0 RESET COMMAND WRITE / SELECT /SLAVE INTERRUPT

Writing a '1' to this bit resets the command write/select/slave interrupt flip-flop.

3.7.13 CONFIGURATION REGISTER LOW (AD7 THRU AD0 = 39, READ)

This register is used to read the configuration jumpers on buffer address pins BA7 through BA0. When in read configuration mode, the buffer address lines have 300 µA current source pulldowns enabled. If there is no external pullup resistor on the buffer address line, then the state of the line is read as a '0'. If a 13K external pullup resistor is connected to a buffer address line, then the state of the line is read as a '1'. The configuration registers should not be read until 100 µsec after enabling read configuration mode, to allow the buffer address line voltages to reach their proper value. Register contents are undefined if not in read configuration mode.

Configuration status low

Bit							
7	6	5	4	3	2	1	0
BA7 THRU BA0							

Configuration status high

Bit							
7	6	5	4	3	2	1	0
0	BA14 THRU BA8						

3.7.14 DRIVE INTERFACE STATUS (AD7 THRU AD0 = 3B, READ)

This register gives status information for the drive controller. It is coded as follows:

Bit							
7	6	5	4	3	2	1	0
RDC	DRDY	WF	HDS	MAC	DRO	IPOL	DSN

3.7.14.1 BIT 7 RESET DRIVE CONTROLLER

This bit reflects the state of the reset drive controller control bit defined in the drive interface control register.

3.7.14.2 BIT 6 DRIVE READY

This bit is set if the $\overline{\text{DRDY}}$ input is asserted by the drive. It can always be read by the local microcontroller regardless of the state of disk controller busy.

3.7.14.3 BIT 5 WRITE FAULT

This bit is set if the $\overline{\text{WF}}$ input is asserted by the drive. It is always valid.

3.7.14.4 BIT 4 HOST DRIVE SELECT

This bit reflects the state of bit 4 of register 46 (hex), the host copy of the SDH register. It is used by the host in AT mode as a drive select. If HDS = 0, then drive 1 is selected. If HDS = 1, then drive 2 is selected. This bit is always accessable to the microcontroller regardless of the state of ABSY.

3.7.14.5 BIT 3 MICROCONTROLLER ACCESS CONTROL

This bit reflects the state of the microcontroller access control bit defined in the drive interface control register.

3.7.14.6 BIT 2 DISABLE RESET OUTPUT

This bit reflects the state of the disable reset output control bit defined in the drive interface control register.

3.7.14.7 BIT 1 INPUT POLARITY

This bit reflects the state of the input polarity control bit defined in the drive interface control register.

3.7.14.8 BIT 0 DISABLE SECTOR NUMBER

This bit reflects the state of the disable sector number control bit defined in the drive interface control register.

3.7.15 DRIVE INTERFACE CONTROL (AD7 THRU AD0 = 3B, WRITE)

This register is used to control the drive controller. It is coded as follows:

Bit							
7	6	5	4	3	2	1	0
RDC	X	X	X	MAC	DRQ	IPOL	DSN

3.7.15.1 BIT 7 RESET DRIVE CONTROLLER

When this bit is asserted, then the drive controller subsection of the WD42C22A resets. It is held reset as long as the bit is asserted. This bit is reset when $\overline{\text{RESET}}$ is asserted.

- 1. Set DRWB=1 (bit 2) in the buffer control register (37_{16}).
- 2. Set ADBP=1 (bit 0) in the buffer control register.
- 3. Set RDQI (bit 1) in the interface control register (38_{16})

3.7.15.2 BIT 3 MICROCONTROLLER ACCESS CONTROL

When this bit is set, the microcontroller is tied to the buffer RAM through the disk controller's port. The microcontroller can then read or write the buffer by reading or writing to the RAM access port (36 hex). The DRWB bit in the buffer manager control port should be set to the proper state before this bit is set. When MAC = 1, then the disk controller task file (registers 21 through

27 hex) cannot be accessed by the microcontroller. If the microcontroller writes to these registers, when MAC = 1 then the disk controller may not act properly. This bit resets when RESET is asserted. The proper sequence for the microcontroller to read/write the RAM is defined under the buffer manager description.

3.7.15.3 BIT 2 DISABLE RESET OUTPUT

When this bit is set, all host initiated soft resets are disabled. Instead of the RESET line being asserted on soft reset only the MCINT line is asserted. It is the responsibility of the local microcontroller to properly reset the board hardware when this bit is set. This bit resets only during power-up.

3.7.15.4 BIT 1 INPUT POLARITY

This bit is used to control the polarity of the INDEX, SCT, WF, and DRDY inputs. If IPOL= 0, the default, then the inputs are active low. If IPOL = 1 then the inputs are active high. In soft sector MFM and RLL modes, DRUN is always active high regardless of the state of IPOL.

3.7.15.5 BIT 0 DISABLE SECTOR NUMBER

When this bit is set then the drive controller does not compare the sector number coming from the drive with the desired sector number when reads or writes are performed. The drive controller will instead write the sector number coming from the drive into the sector number register in the drive controller task file. At the end of each sector, just prior to issuing DRQI or DCI, the drive controller always writes the sector number to the alternate sector number register. This bit resets when RESET is asserted.

3.7.16 ALTERNATE SECTOR NUMBER (AD7 THRU AD0 = 3C, READ)

When the disk controller interrupts the microcontroller, this register holds the sector number of the sector just read or written. It is always updated just prior to the disk BDRQ interrupt (DRQI) or the disk controller interrupt (DCI). It is initialized to FF hex at the start of every command. It is written regardless of the state of the DSN bit described above.

Bit							
7	6	5	4	3	2	1	0
NUMBER OF LAST SECTOR READ OR WRITTEN							

3.8 AT INTERFACE PORTS

3.8.1 DRIVE ZERO STATUS (AD7 THRU AD0 = 3D, READ/WRITE)

In PC/AT mode, bit 6, bit 5, bit 4, bit 2, and bit 0 of the host status register are controlled by the local microcontroller. Bits 6, 5, 4, 2, and 0 of the host status register are set to the values of bits 6, 5, 4, 2, and 0, respectively, of this register if bit 4 of the AT task file copy SDH register (port 46 for microcontroller, port 6 for host) is 0. The other bits of the host status are not affected by this register.

3.8.2 DRIVE ONE STATUS (AD7 THRU AD0 = 3E, READ/WRITE)

In AT mode, bit 6, bit 5, bit 4, bit 2, and and bit 0 of the host status register are controlled by the local microcontroller. Bits 6, 5, 4, 2, and 0 of the host status register is set to the values of bits 6, 5, 4, 2, and 0, respectively, of this register if bit 4 of the AT task file copy SDH register (port 46 for microcontroller, port 6 for host) is 1. The other bits of the host status are not affected by this register.

3.8.3 FIXED DISK REGISTER (AD7 THRU AD0 = 3F, READ)

This register contains the fixed disk register data written by the host.

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	HS3EN	RST	$\overline{IEN}$	0

3.8.4 DIGITAL INPUT REGISTER (AD7 THRU AD0 = 3F, WRITE)

Bit 5 of this register is written by the local microcontroller and read by the host if the fixed disk register bit 3 is zero. This bit is inverted when this register is read by the host. If HS3EN is one, then bit 5 of this register comes from SDH register bit 3.

Bit							
7	6	5	4	3	2	1	0
ECCM	ECC7/ DDRQ	RWC	X	X	X	DS1	DS0

3.8.4.1 BIT 7 ECC MODE

In PC/AT mode, ECCMOD = 1 indicates that the data transferred to the host includes ECC. The ECC is transferred in bytes rather than in words. This bit is reset when $\overline{\text{RESET}}$ is asserted. This bit should not be set in XT or slave host modes.

3.8.4.2 BIT 6 ECC 7 BYTES/ DISABLE BDRQ

When ECCM = 1, then this bit determines the number of ECC bytes transferred to the host. If ECC7 = 1, then 7 bytes are transferred. Otherwise, 4 bytes are transferred. If ECCM = 0, then this bit controls whether or not the drive controller issues BDRQ interrupts. If DDRQ = 0, then the drive controller issues BDRQ interrupts. If DDRQ = 1, then the drive controller does not issue BDRQ interrupts. It should be noted that when BDRQ occurs, the buffer manager loads the disk pointer from its pipeline register and when no BDRQ occurs then the disk pointer keeps incrementing from one sector to the next. This bit resets when $\overline{\text{RESET}}$ is asserted.

3.8.4.3 BIT 5 REDUCE WRITE CURRENT

This bit is set by the microcontroller and indicates the state of the $\overline{\text{RWC}}$ signal going to the drive.

3.8.4.4 BIT 1 DRIVE SELECT 1

This bit controls the state of the $\overline{\text{DS1}}$ output pin. When DS1 = 0, then the $\overline{\text{DS1}}$ output is tri-stated and when DS1 = 1 the the $\overline{\text{DS1}}$ output is low. This bit is reset when $\overline{\text{RESET}}$ is asserted.

3.8.4.5 BIT 0 DRIVE SELECT 0

This bit controls the state of the $\overline{\text{DS0}}$ output pin. When DS0 = 0, then the $\overline{\text{DS0}}$ output is tri-stated and when DS0 = 1 the the $\overline{\text{DS0}}$ output is low. This bit is reset when $\overline{\text{RESET}}$ is asserted.

3.8.5 AT TASK FILE COPY (AD7 THRU AD0 = 40 THRU 47, READ/WRITE)

These registers are a copy of the disk controller task file. They are loaded by the host prior to the start of a command. The local microcontroller must read the command and interpret it and then copy the appropriate parameters from this task file copy to the actual drive controller task file (20-27 hex). At the end of the command, the local microcontroller must update this task file copy before asserting INTRQ and resetting ABSY. The local microcontroller can only access these registers when ABSY=1.

4.0 BUFFER MANAGER ORGANIZATION

The buffer manager can control multiple sector buffers totalling up to 32 Kbytes. The buffer interface requires static RAMs. The sector buffers can be any size up to 2055 bytes, including ECC, and can be located at any byte boundary. The buffer manager has two address counters, one for the host interface and one for the disk data buffer. Both counters can access the SRAM simultaneously. The buffer manager handles the arbitration between the host interface and the drive controller. There is a FIFO in the host data interface that allows a sustained bandwidth of 4 Mwords/sec (8 Mbytes/sec) for 16-bit wide transfers and 8 Mbytes/sec for 8-bit wide transfers. The buffer manager can sustain a RAM bandwidth of 10 Mbytes/sec.

When the local microcontroller wants to access the buffer RAM, it has to use the disk buffer manager logic. It first loads the desired starting address into the disk buffer pointer. The proper buffer manager control bits are then set to enable the local microcontroller access to the buffer. When the local microcontroller accesses the special RAM access port (register 36), the data is read/written through the disk controller's FIFO port to the buffer. The RAM can only be accessed sequentially from the starting address and only in one direction as set by the DRWB control bit in the buffer control register.

Both address counters are pipelined. There are registers that can be loaded with the starting address of the next sector buffer while the current buffer is transferring. This allows noncontiguous buffers to be chained without any loss of RAM bandwidth between sectors.

4.1 ACCESSING BUFFER RAM FROM THE MICRO-CONTROLLER

The microcontroller can read and write the buffer RAM. To read the buffer RAM the procedure is:

1. Set DRWB=1 (bit 2) in the buffer manager control Register (37 hex).
2. Set MAC=1 (bit 3) in the disk controller control register (3B hex).
3. Load the starting address of the data being accessed into the disk buffer pointer registers (34 & 35 hex).
4. Set ADBP=1 (bit 0) in the buffer manager control register (37 hex).

The buffer manager begins reading data out of the RAM starting at the address specified in the disk pointer register and placing it into the FIFO. As the microcontroller reads from the RAM access port (36 hex), sequential bytes from the buffer are transferred from the FIFO to the microcontroller.

The procedure to write to the buffer RAM is:

1. Set DRWB=0 (bit 2) in the buffer manager control register (37 hex).
2. Set MAC=1 (bit 3) in the disk controller control register (3B hex).
3. Load the starting address of the data being accessed into the disk buffer pointer registers (34 & 35 hex).
4. Set ADBP=1 (bit 0) in the buffer manager control register (37 hex).

As the microcontroller writes data to the RAM access port (36 hex), the buffer manager transfers the bytes to sequential locations in the buffer RAM starting at the address specified in the disk pointer register.

NOTE

DRWB should not be changed while MAC = 1.

32

4.2 STARTING HOST TRANSFERS TO/FROM BUFFER RAM

Host transfers can be performed in several modes. The modes available and the setup required to establish each mode are as follows:

HDMA	BDEN	BCNT	H16/8
1	0	X	0
8-bit wide single byte DMA			
1	0	X	1
16-bit wide single word DMA			
1	1	0	0
8-bit wide, 8-byte burst DMA			
1	1	0	1
16-bit wide, 16-byte burst DMA			
1	1	1	0
8-bit wide, continuous burst DMA			
1	1	1	1
16-bit wide, continuous burst DMA			
0	X	X	0
8-bit wide PIO			
0	X	X	1
16-bit wide PIO			

Bits HDMA (bit 7), BCNT(bit 5), and H16/$\overline{8}$ (bit 1) are in the auxilliary buffer manager control register (2F hex) and bit BDEN (bit 1) is in the buffer manager control register (37 hex). All of these modes are available in both the XT and AT host configurations. All of the DMA modes are available in the slave host configuration.

To perform a Host read data transfer the following sequence should be followed.

1. Set up the appropriate transfer mode as described above.
2. Set HRWB=1 (bit 3) in the buffer control register (37 hex).
3. Load the starting address of the desired sector into the host pointer registers (30 & 31 hex). Load the number of bytes into the host transfer count registers (32 & 33 hex).
4. Set AHBP=1 (bit 4) in the buffer manager control register (37 hex). Hardware automatically sets DRQ (bit 3) and resets ABSY (bit 7) in the host status register if AT mode and sets REQ (bit 0) in the hardware status register if XT mode. If DMA transfers are enabled, then the hardware automatically starts the DMA handshake when AHBP is set by the micro-controller.
5. Wait for HPRI=1 (bit 2) in the interface status register (38 hex). $\overline{\text{MCINT}}$ is asserted.
6. Set RHRI=1 (bit 2) in the interface control register (38 hex) to reset the interrupt. If chaining and still more sectors then go to 3.
7. Wait for HPRI=1 (bit 2) in the interface status register (38 hex). $\overline{\text{MCINT}}$ is be asserted.
8. Set RHRI=1 (bit 2) in the interface control register (38 hex) to reset the interrupt. If still more sectors, then go to 3.
9. Set RBSY=1 (bit 3) in the interface control register when the entire command sequence is complete. This resets the ABSY and XBSY host status bits. They stay reset until the next command is issued by the host.

To perform a host write data transfer, the following sequence should be followed.

1. Set up the appropriate transfer mode as described above.
2. Set HRWB=0 (bit 3) in the buffer control register (37 hex).
3. Load the starting address of the desired sector into the host pointer registers (30 & 31 hex). Load the number of bytes into the host transfer count registers (32 & 33)
4. Set AHBP=1 (bit 4) in the buffer manager control register (37 hex). Hardware automatically sets DRQ (bit 3) and resets ABSY (bit 7) in the host status register if AT mode and set REQ (bit 0) in the hardware status register if XT mode. If DMA transfers are enabled, then the hardware automatically starts the DMA handshake when AHBP is set by the micro-controller.
5. Wait for HPRI=1 (bit 2) in the interface status register (38 hex). $\overline{\text{MCINT}}$ is asserted.

6. Set RHRI=1 (bit 2) in the interface control register (38 hex) to reset the interrupt. If chaining and still more sectors then go to 3.

7. Wait for second HPRI=1 (bit 2) in the interface status register (38 hex). MCINT is asserted.

8. Set RHRI=1 (bit 2) in the interface control register (38 hex) to reset the interrupt. If still more sectors then go to 3.

9. Set RBSY=1 (bit 3) in the interface control register when the entire command sequence is complete. This resets the ABSY and XBSY host status bits. They stay reset until the next command is issued by the host.

4.3 CONTROLLER COMMANDS

The WD42C22A Winchester command set contains twelve commands. Four commands (read sector, write sector, format, and set parameter) are directly executed through the command register. The remaining commands are not directly available to the host. These commands may be executed by the local microcontroller transparently to the host. Table 12 lists the commands and command codes.

COMMAND	7	6	5	4	3	2	1	0
Read Sector	0	0	1	0	0	M	L	T
Read Next Data	0	1	1	0	0	0	L	1
Write Sector	0	0	1	1	X	M	L	T
Write ID	1	0	1	1	F	0	A	T
Scan ID	0	1	0	0	0	0	0	T
Format Track	0	1	0	1	0	0	W	1
Format Single Sector	1	1	0	1	0	0	W	1
Compute Correction	0	0	0	0	1	P	0	0
Set Parameter	Z	0	0	R	0	E	H	S
Load Parameter Block	1	0	0	0	1	D	K	U
Sleep	1	0	0	1	1	0	0	0
Dump	1	0	1	0	I	B	L	1

TABLE 12. COMMAND AND COMMAND CODES

Mnemonic definitions for Table 12:

- M=0 Single sector read or write. Sector count is ignored.

M=1 Multiple sector read or write. Used for 1:1 interleave.

- L=0 Normal mode, selected ECC or CRC functions performed.

L=1 Sector extended by 4 or 7 bytes (depends on set parameter command. No ECC generated or checked.

- T=0 Enable retries.

T=1 Disable retries.

- X=0 Write sector specified in sector number register.

X=1 Write sector specified in first byte of the sector buffer.

- F=0 Write new ID immediately after current ID.

F=1 Write new ID offset from current ID.

- A=0 Do not pulse AME when writing new ID.

A=1 Pulse AME when writing new ID.

- W=0 Write gate stays asserted for entire track or sector.

W=1 Write gate deasserted over all gaps during format.

- P=0 Transfer syndrome bytes to buffer and calculate error pattern bytes and transfer them to the buffer.

P=1 Transfer syndrome bytes to the buffer but do not calculate error pattern bytes.

- Z=0 MFM or RLL mode.

Z=1 NRZ mode. Mode used for ESDI drive interface.

- R=0 Disable relocation ID searches.

R=1 Enable relocation ID searches.

- E=0 Sector extension for read long/write long 4 bytes. ECC generator/checker is 4 bytes.

E=1 Sector extension for read long/write long 7 bytes. ECC generator/checker is 7 bytes.

- H=0 SDH register programmed for 3 head select bits.

H=1 SDH register programmed for 4 head select bits.

- S=0 Error correction span 5 bits with 4 byte ECC or 11 bits with 7 byte ECC.

S=1 Error correction span 11 bits with 4 byte ECC or 22 bits with 7 byte ECC.

MODE	MODE CONTROL	OPTIONS														
	Z D K	M	T	L	X	A	F	R	S	E	H	P	U	W	I	B
RLL soft sector	? 0 0	x	x	x	x	x	x	x	x	*	x	x	x			
RLL hard sector	? 1 0	x	x	x	x	x	x	x	x	*	x	x	x	x	x	x
MFM soft sector	0 0 1	x	x	x	x	x	x	x	x	x	x	x	x			
MFM hard sector	0 1 1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
NRZ soft sector	1 0 1	x	x	x	x	x	x	x	x	x	x	x	x			
NRZ hard sector	1 1 1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

? Don't care, could be 0 or 1.

x These options are supported.

* These options have no effect.

TABLE 13. OPTION SUMMARY TABLE

- D=0 Select soft sector drive interface. Default after master reset.

  D=1 Select hard sector drive interface. In this mode, DRUN becomes a sector pulse input.

- K=0 RLL data interface. Selection of this option disables the NRZ option. Defaults to this setting after master reset.

  K=1 Data interface is either MFM or NRZ.

- U=0 Use the standard sector sizes defined under the SDH register description.

  U=1 Select user defined sector size. The desired sector size is put into the cylinder registers prior to issuing a load parameter block command. The auxilliary set parameter command transfers the desired sector size from the cylinder registers to an internal sector size register.

4.4 COMMAND DESCRIPTIONS

4.4.1 READ SECTOR

If M = 0, then the sector specified in sector number register is read. If M = 1, then multiple records are read. If the sector count register = 0, then 256 sectors are read at the desired track.

If T=0, then ID searches are retried for 10 index pulses. DAM not found errors are not retried. There are no retries for CRC/ECC errors. If T=1, ID searches are retried for two index pulses.

If L=0, then normal CRC or ECC read commands are performed. If L=1, then the CRC or ECC check bytes are not computed but instead the CRC or ECC check bytes are loaded into the buffer immediately after the data field. The external sector buffer must be long enough to hold the additional 4 or 7 bytes. If ECC and retry modes have been selected and a data field error occurs there are no attempts to correct the data.

A bad block mark in the ID field sets the error bit and the data field is not read. If the R option in the set parameter command is set then the controller searches immediately after the normal ID field for a special ID field containing mapping information and a special "Relocation ID" flag bit. The RIDF bit in the error register sets if this special ID field is found. If a bad block mark is found in an ID field then the command terminates immediately even if more sectors remain to be read. The task file contents when a bad block bit is detected and the R option is used is as follows:

REGISTER	MEANING
22	Sector number of sector with bad block bit set
23	Sector umber where sector has been relocated
24	LSB of cylinder number where sector has been relocated
25	MS bits of Cylinder where sector has been relocated
26	Head number of relocated sector

If DSN=1 (bit 0) in the drive interface control register (3B hex) than the sector number is not compared when ID searches are performed. The WD42C22A reads the sector as long as the cylinder and head numbers match the desired values. This allows an interleaved track to be read into the buffer in one revolution.

Command Flow:

- MICRO:
  1. Set DRWB=0 (bit 2) in the buffer manager control register (37 hex).
  2. Load the starting address of the first sector into the disk buffer pointer registers (34 & 35 hex).
  3. Set ECCM=0 (bit 7) and DDRQ=1 (bit 6) in the DIR write register (3F hex) and MAC=1 (bit 3) in the drive interface control register (3B hex) to disable DRQI, if desired.
  4. Set ADBP=1 (bit 0) in the buffer manager control register (37 hex).
  5. Set MAC=0 in the drive interface control register.
  6. Issue read command to WD42C22A.
- WD42C22A:
  7. Write 'FF' to alternate sector number register (3C hex). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.
- MICRO:
  8. Load starting address of next sector buffer into disk buffer pointer register. Set ADBP=1 in buffer manager control register if more sectors remaining. Set RDQI (bit 1) in the interface control register (38 hex).
- WD42C22A:
  9. Search for head, cylinder, sector number and sector size code.
  10. When the proper sector ID is found, read sector data and place in buffer.
  11. Write sector number to alternate sector number register. If M = 0, then go to 10.
  12. Decrement sector count, increment sector number. If M = 1, and sector count = 0 then go to 13 else go to step 8.
  13. Set DCI (bit 3) in the interface status register (38 hex). MCINT asserted.
- MICRO:
  14. Read disk controller status register (27 hex) and error register (21 hex).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- ID not found set if ID field not found or if ID field matches, but CRC check fails, and after retry procedure.
- Bad block set if attempt was made to read a sector with bad block mark.
- Relocation ID found if R option enabled and relocation ID detected.
- Data CRC/ECC set if data field CRC or ECC check fails. No attempt is made to correct ECC errors.
- Data AM not found in set if data address mark not found

32

4.4.2 READ NEXT DATA

The read next data command finds the next data field and places it in a buffer. If the WD42C22A detects that the drive number changed since the last read command, then an auto-scan ID is performed and step pulses are issued to update the present cylinder position.

All searches for a data field are retried for two index pulses, but if a data ECC error is detected there are no retries. If after reading the correct ID field, the data address mark is not found a DAM error is set.

The L flag controls the ECC check bytes. If L=0, then the data field is read and ECC is checked. If L=1, then the ECC check bytes are not computed. Instead, the ECC check bytes are loaded into the buffer immediately after the data field. The external sector buffer must be long enough to hold the additional 7 bytes.

NOTE

This command supports only soft sector MFM and RLL mode and is implemented for backward compatibility with the WD5011 and WD5011A.

Command Flow :

- MICRO:
  1. Set DRWB=0 (bit 2) in the buffer manager control register (37 hex).
  2. Load the starting address of the first sector into the disk buffer pointer registers (34 & 35 hex).
  3. Set ADBP=1 (bit 0) in the buffer manager control register (37 hex).
  4. Set ECCM=0 (bit 7) and DDRQ=1 (bit 6) in the DIR write register (3F hex) and MAC=1 (bit 3) in the drive interface control register (3B hex) to disable DRQI, if desired.
  5. Set MAC=0 in the drive interface control register.
  6. Issue read next data command to WD42C22A.
- WD42C22A:
  7. Write 'FF' to alternate sector number register (3C hex). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Set DRQ status bit, activate BDRQ signal to buffer manager. Wait for BRDY signal indicating transfer of buffer pointer.
- MICRO: Set RDQI (bit 1) in the interface control register (38 hex).
- WD42C22A:
  9. Find next data field, read sector data and place in buffer. If data mark error, try data field search again until 2 index pulses occur.
  10. Copy sector number register to alternate sector number register (3C hex). Set DCI (bit 3) in the interface status register (38 hex). MCINT is asserted.
- MICRO:
  11. Read disk controller status register (27 hex) and error register (21 hex).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- Data CRC/ECC set if data field CRC or ECC check fails. No correction is attempted.
- Data AM not found is set if data address mark not found after 2 index pulses of looking for any data field.

4.4.3 WRITE SECTOR

Write from buffer to disk when BRDY signal is activated by the buffer manager. Write total number of sectors specified by sector count register if M = 1. Sectors are written in numerical order. If M = 0, then sector count is ignored and only one sector is written. The data field PLO sync field is nominally 12 bytes long but is extended by the PLO register.

If T=0, then ID searches are retried for 10 index pulses. If T=1, then ID searches are retried for 2 index pulses only.

If L=0, then normal CRC or ECC write sector commands are performed. If L=1, then the CRC or ECC check bytes are not computed and written

to the disk but instead, 4 or 7 additional bytes are read from the buffer and written to the disk immediately after the data field.

If X=0, then the controller searches for the sector number in the sector number register and increments the sector number register and the end of each sector if M=1. If X=1, then the controller searches for the sector specified in the first byte of the sector buffer. The controller reloads the sector number register from the first byte of each subsequent sector buffer if M=1. This allows a track formatted with interleave to be written in one revolution.

A bad block mark in the ID field sets the error bit and the data field is not be written. If the R option in the set parameter command is set, then the controller searches immediately after the normal ID field for a special ID field containing mapping information and a special "Relocation ID" flag bit. The RIDF bit in the error register sets if this special ID field is found. If a bad block mark is found in an ID field then the command terminates immediately even if more sectors remain to be read. The task file contents when a bad block bit is detected and the R option is used is as follows:

REGISTER	MEANING
22	Sector number of sector with bad block bit set
23	Sector number where sector has been relocated
24	LSB of cylinder number where sector has been relocated
25	MS bits of cylinder where sector has been relocated
26	Head number where sector has been relocated

If DSN=1(bit 0) in the drive interface control register (3B hex) then the sector number is not compared when ID searches are performed. The WD42C22A writes the sector as long as the cylinder and head numbers match the desired values. This allows an interleaved track to be written into the buffer in one revolution. This option is only useful when doing the initial write-after-format to place 00 in the data fields.

Command Flow:

- MICRO:
  1. Set DRWB=1 (bit 2) in the buffer manager control register (37 hex).
  2. Load the starting address of the first sector into the disk buffer pointer registers (34 & 35 hex).
  3. Set ECCM=0 (bit 7) and DDRQ=1 (bit 6) in the DIR write register (3F hex) and MAC=1 (bit 3) in the drive register (3B hex) to disable DRQI, if desired.
  4. Set ADBP=1 (bit 0) in the buffer manager control register (37 hex).
  5. Set MAC=0 in the drive interface control register.
  6. Issue write command to WD42C22A.
- WD42C22A:
  7. Write 'FF' to alternate sector number register (3C hex). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.
- MICRO: Load starting address of next sector buffer into disk buffer pointer register. Set ADBP=1 in buffer manager control register if more sectors remaining. Set RDQI (bit 1) in the interface control register (38 hex).
- WD42C22A:
  9. Search for head, cylinder, sector number and sector size code.
  10. When the proper sector ID is found, write buffer data to sector.
  11. Write sector number to alternate sector number register (3C hex). If M = 0 then go to 13.
  12. Decrement sector count, in-

32

crement sector number. If M = 1 and sector count = 0 then go to 13 else go to step 8.

13. Set DCI (bit 3) in the interface status register (38 hex). MCINT asserted.

• MICRO: 14. Read disk controller status register (27 hex) and error register (21 hex).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- ID not found set if exact ID field not found or if ID field matches but CRC check fails, after retry procedure.
- Bad Block set if write sector attempted on any sector with bad block mark.
- Relocation ID found if R option enabled and relocation ID detected.

4.4.4 WRITE ID

Write from buffer to disk when BRDY signal is activated by the buffer manager. Write 4 bytes to create an ID field. The PLO sync field prior to this new ID field is nominally 12 bytes long but is extended by the PLO register.

If T=0 then ID searches are retried for 10 index pulses. If T=1, then ID searches are retried for 2 index pulses only.

If F=0, then the new ID is written immediately after the ID field of the desired sector. If F=1, then the new ID field is written offset from the desired sector ID with the offset determined by the internal sector size register. The sector number register is ignored if F=1. The sector number of the ID to match is taken from the first byte of the buffer. A load parameter block command will have to be issued to set the offset value and another load parameter Block will be needed to set the sector size back to the correct value if the programmable sector size option is being used. An offset of up to 2048 is allowed. This option can be used to reformat a single sector in soft sector mode.

If A=0 then the AME output is held low during the write ID command. If A=1, then the AME output is pulsed at the start of the PLO field before the new ID being written. This option, together with the F option can be used to reformat a single sector in soft sector NRZ mode.

The four bytes in the buffer (F=0) should be as follows:

BYTE 0: 1 1 1 1 $\overline{\text{cyl 10}}$ 1 $\overline{\text{cyl 9}}$ cyl 8

BYTE 1: Low byte of cylinder number

BYTE 2: BB 0 RF 0 HS3 HS2 HS1 HS0

BYTE 3: Sector Number

BB = bad block flag

RF = Relocation ID flag

$\overline{\text{cyl 10}}$ thru cyl 8 = upper three cylinder number bits

HS3 thru HS0 = head select bits

The five bytes in the buffer (F=1) should be as follows:

BYTE 0: Sector Number

BYTE 1: 1 1 1 1 $\overline{\text{cyl 10}}$ 1 $\overline{\text{cyl 9}}$ cyl 8

BYTE 2: Low byte of cylinder number

BYTE 3: BB 0 RF 0 HS3 HS2 HS1 HS0

BYTE 4: Sector Number

BB = bad block flag

RF = Relocation ID flag

$\overline{\text{cyl 10}}$ thru cyl 8 = upper three cylinder number bits

HS3 thru HS0 = head select bits

RF should be set to 1 if the new ID being written is to be a special relocation ID for mapping a defective sector to a new position.

Command Flow:

• MICRO:

1. Set DRWB=1 (bit 2) in the buffer manager control register (37 hex).
2. Load the starting address of the ID buffer data into the disk buffer pointer registers (34 & 35 hex).

3. Set ECCM=0 (bit 7) and DDRQ=1 (bit 6) in the DIR write register (3F hex) and MAC=1 (bit 3) in the drive interface control register (3B hex) to disable DRQI, if desired.
4. Set ADBP=1 (bit 0) in the buffer manager control register (37 hex).
5. Set MAC=0 in the drive inter-control register.
6. Issue Write ID command to WD42C22A.

• WD42C22A: 7. Write 'FF' to alternate sector number register (3C hex). Abort if drive not ready or write fault.
8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.

• MICRO: Set RDQI (bit 1) in the interface control register (38 hex).

• WD42C22A: 9. Search for head, cylinder, sector number and sector size code.
10. When the proper sector ID is found, write buffer data to sector.

• WD42C22A:11. Write sector number to alternate sector number register. Set DCI (bit 3) in the interface status register (38 hex). MCINT asserted.

• MICRO: 12. Read disk controller status register (27 hex) and error register (21 hex).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write Fault and aborted command set if WF pin activated.
- ID not Found set if exact ID field not found or if ID field matches but CRC check fails, after retry procedure.
- Bad Block set if bad block bit detected in ID of desired sector.

4.4.5 SCAN ID

When the next ID field of the present track is encountered, cylinder number, sector size, head number and sector number are loaded into the respective registers.

Command Flow:

• MICRO: 1. Issue Scan ID command to WD42C22A.
2. Write 'FF' to alternate Sector number register (3C hex). Abort if drive not ready or write fault.
3. Search for next ID field and read 4 ID bytes into respective registers. Search for ID field for up to 10 index pulses if T=0, up to 2 index pulses if T=1.

• WD42C22A: 4. Set DCI (bit 3) in the interface status register (38 hex). MCINT asserted.

• MICRO: 5. Read disk controller status register (27 hex) and error register (21 hex).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin active.
- Bad Block set if bad block mark detected.
- ID not found if no ID fields are found.
- Relocation ID found if R option enabled and relocation ID detected.

4.4.6 FORMAT TRACK

This command formats one track using parameters loaded in the task registers file and in buffer memory.

Cylinder, head, and sector size numbers are taken from the task register file. Good block/bad block marks and sector numbers are taken from buffer memory. The total number of sectors formatted is specified by the sector count register. The lengths of GAP 1 and GAP 3 are loaded into the sector number register. The length of the ID PLO sync field is loaded into the PLO length

register if B = 1. The data PLO field length is 12 bytes during format.

The data placed in the gaps comes from an internal register loaded during the load parameter block command. The data placed into the pads comes from another internal register loaded during the load parameter block command.

After the task register file has been loaded with the desired format parameters and the block marks and sector addresses have been loaded into the buffer then the command register is loaded with the format command . When the BRDY signal is activated by the buffer manager the specified number of sectors are written. The block marks and sector numbers are read from the buffer as needed. The data field is written with FF. CRC is automatically computed and written if in CRC mode. If in ECC mode, ECC check bytes are automatically computed and written after the data field. The number of ECC check bytes is determined by the E bit in the set parameter command.

Write Gate is turned on and off within 4 bit times after index if NRZ or hard sector mode is selected or within 6 bit times otherwise. In RLL mode Gap1/Gap3 data should be programmed to be 33 hex with the load parameter command. The W option controls the state of WRITE GATE over the gaps. If W=1, WRITE GATE turns off over the gaps.

The sum of the number of bytes in both the Gap1/Gap3 and ID PLO field must be greater than or equal to 25 bytes to achieve 1:1 interleave.

The interleave table contains the bad block marks and sector numbers for the track. If there is a bad sector and it is desired for the controller to just skip over it then the bad block mark for that sector position should be set to '80' hex and the sector number for that sector should be set to 'FF' hex. If it is desired to map the bad sector then the bad block mark for that sector should be set to '80' hex and the sector number for that sector should be set to the correct value for that position in the interleave table. The R and U options should be set in the set parameter and load parameter block commands. A write ID command then places the relocation information for that sector onto the drive.

The interleave table format is:

- BYTE 0: 1st sector's block mark (00 or 80 hex)
- BYTE 1: 1st sector's sector number
- BYTE 2: 2nd sector's block mark (00 or 80 hex)
- BYTE 3: 2nd sector's sector number

.
.
.

- BYTE 2n: nth sector's block mark (00 or 80 hex)
- BYTE 2n+1: nth sector's sector number

Command Flow:

- MICRO:
  1. Set DRWB=1 (bit 2) in the buffer manager control register (37 hex)
  2. Load the starting address of the interleave table into the disk buffer pointer registers (34 & 35 hex).
  3. Set ECCM=0 (bit 7) and DDRQ=1 (bit 6) in the DIR write register (3F hex) and MAC=1 (bit 3) in the drive interface control register (3B hex) to disable DRQI, if desired.
  4. Set ADBP=1 (bit 0) in the buffer manager control register (37 hex).
  5. Set MAC=0 in the buffer control register.
  6. Issue format command to WD42C22A.

- WD42C22A:
  7. Write 'FF' to the alternate sector number register (3C hex). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer. Wait for leading edge of index.

- MICRO: Set RDQI (bit 1) in the interface control register (38 hex).
- WD42C22A:
  9. Write gap.
  10. Write sector ID using parameters in task register file and buffer memory. Data bytes are FF.
  11. Decrement sector count register. If sector count = 0, then go to step 12, else go to step 9.
  12. Write Gap until leading edge of index pulse.
  13. De-assert Write Gate.
  14. Set DCI (bit 3) in the interface status register (38 hex). MCINT asserted.
- MICRO:
  15. Read disk controller status register (27 hex) and error register (21 hex).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.

Note

Gap length written on disk is 3 bytes longer than gap value specified in sector number register.

4.4.7 FORMAT SINGLE SECTOR

This command formats one sector using parameters loaded in the task register file and in buffer memory. This command only applicable to hard sector mode.

WRITE GATE is turned on and off within 4 bit times after index or sector if NRZ mode is selected or within 6 bit times otherwise. The W option controls the state of WRITE GATE over the gaps. Setting W to 1 turns off WRITE GATE over the gaps.

Cylinder, head, and sector size numbers are taken from the task register file. Good block/bad block marks and sector number are taken from buffer memory. The physical sector position to be formatted is specified by the sector count register. If sector count = 1, then the first sector after index is formatted. For sector count = 2, the second sector after index is formatted, and so on. The lengths of GAP 1 and GAP 3 are loaded into the sector number register. The length of the ID PLO sync field is loaded into the PLO length register.

The data placed in the gaps comes from an internal register loaded during the load parameter block command. The data placed into the pads comes from another internal register loaded during the load parameter block command.

After the task register file has been loaded with the desired format parameters and the block marks and sector number loaded into the buffer, then the command register is loaded with the format single sector command. When the BRDY pin is activated by the buffer manager the controller then looks for the start of the desired sector. The bad block mark and sector number are read from the buffer. The data field is written with FF. CRC is automatically computed and written if in CRC mode. If in ECC mode, ECC check bytes are automatically computed and written after the data field. The number of ECC check bytes is determined by the E bit in the set parameter command.

The data for the buffer is:

- BYTE 0: bad block mark (00 or 80 hex)
- BYTE 1: sector number of formatted sector.

Command Flow:

- MICRO:
  1. Set DRWB=1 (bit 2) in the buffer manager control Register (37 hex).
  2. Load the starting address of the interleave table into the disk buffer pointer registers (34 & 35 hex).
  3. Set ECCM=0 (bit 7) and DDRQ =1 (bit 6) in the DIR write register (3F hex) and MAC=1 (bit 3) in the drive interface control Register (3B hex) to disable DRQI, if desired.
  4. Set ADBP=1 (bit 0) in the buffer manager control register (37 hex).
  5. Set MAC=0 in the drive interface control register.
  6. Issue format single sector command to WD42C22A.

32

- WD42C22A: 7. Write 'FF' to the alternate sector number register (3C hex). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer. Wait for leading edge of index.
- MICRO: Set RDQI (bit 1) in the interface control register (38 hex).
- WD42C22A: 9. Decrement sector count. If sector count = 0 go to 11, else go to 10.
  10. Wait for SECTOR pulse, then go to 9.
  11. Assert WRITE GATE. Write gap.
- WD42C22A:12. Write sector ID using parameters in task register file and buffer memory. Data bytes are FF.
  13. Write gap until leading edge of SECTOR pulse.
  14. De-assert Write Gate.
  15. Set DCI (bit 3) in the interface status register (38 hex). MCINT asserted.
- MICRO: 16. Read disk controller status register (27 hex) and error register (21 hex).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.

4.4.8 COMPUTE CORRECTION

This command is used to compute the pattern and location of a single burst error. It is used after a read sector command has detected a data field ECC error. The compute correction command first writes the four or seven syndrome bytes into the buffer. It then processes the syndrome bytes to compute the error pattern and error location. The error location and error pattern bytes are written into the buffer. Either four or seven error pattern bytes are written to the buffer depending on the ECC length selected. The error pattern bytes are automatically byte aligned.

The P option is used to control whether or not the error pattern bytes are calculated. If P=0, then the error pattern bytes are calculated and sent to the buffer. If P=1, then the error pattern bytes are not calculated. Only the syndrome byte is transferred to the buffer. This option facilitates firmware algorithms that require a matching syndrome before a correction is made. In this case, the firmware calculates the error pattern, corrects the error, and saves the syndrome after initially detecting the error. Then, the firmware dumps and compares the syndrome on the second read of the same sector. An ECC error can now be corrected in one revolution of the disk compared to three revolutions required by earlier WD1010 and WD2010 based controllers.

The error pattern and error location bytes are not valid if the error is found to be uncorrectable. An uncorrectable error is indicated by the appropriate bits in the status and error register.

The buffer contents contains the following information:

- SYNDROME BYTE (MSB)
- SYNDROME BYTE
- SYNDROME BYTE
- SYNDROME BYTE (LSB if 4 byte ECC)
- SYNDROME BYTE (if 7 byte ECC)
- SYNDROME BYTE (if 7 byte ECC)
- SYNDROME BYTE (LSB if 7 byte ECC)
- BYTE OFFSET (MSB)
- BYTE OFFSET (LSB)
- ERROR PATTERN (MSB)
- ERROR PATTERN
- ERROR PATTERN
- ERROR PATTERN (LSB if 4 byte ECC)
- ERROR PATTERN
- ERROR PATTERN
- ERROR PATTERN (LSB if 7 byte ECC)

If the byte offset is 0 then the first data byte of the sector should be exclusive OR'ed with the first error pattern byte (MSB), the second data byte

exclusive OR'ed with the second error pattern byte, and the third data byte with the last error pattern byte (LSB). Exclusive OR the first three error pattern bytes for 5 and 11 bit spans. Exclusive OR the first four error pattern bytes for the 22 bit span.

Command Flow:

- MICRO:
  1. Set DRWB=0 (bit 2) in the buffer manager control register (37 hex).
  2. Load the starting address of the error correction data buffer into the disk buffer pointer Registers (34 & 35 hex).
  3. Set ECCM=0 (bit 7) and DDRQ =1 (bit 6) in the DIR write register (3F hex) and MAC=1 (bit 3) in the drive interface control register (3B hex) to disable DRQI, if desired.
  4. Set ADBP=1 (bit 0) in the buffer manager control register (37 hex).
  5. Set MAC=0 in the drive interface control register.
  6. Issue compute correction command to WD42C22A.
- WD42C22A:
  7. Write 'FF' to the alternate sector number register (3C hex). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer. Wait for leading edge of INDEX.
- MICRO: Set RDQI (bit 1) in the interface control register (38 hex).
- WD42C22A:
  9. Transfer contents of the four (or seven) byte ECC register to buffer, most significant byte first.
  10. Clock the ECC register. Stop if correctable pattern found or if number of clocks exceeds sector size. If number of clocks exceeds sector size, set error bit of status register and ECC error of error register.
  11. Transfer byte count to buffer (2 bytes). Transfer 3 bytes of error pattern to buffer if C=0 and transfer 4 bytes of error pattern if C=1 or 7 byte ECC.
  12. Set DCI (bit 3) in the interface status register (38 hex). MCINT asserted.
- MICRO:
  13. Read disk controller status register (27 hex) and error register (21 hex).

Error Flags:

- CRC/ECC flag set if data field error length exceeds correction span.

NOTE

Default 11 bit correction span after master reset if 7-byte ECC or 5 bit correction span if 4-byte ECC.

4.4.9 SET PARAMETER

The E bit is used to select either 4 byte or 7 byte sector extension for read long and write long commands. It also selects either a 4 or 7 byte internally generated ECC. A 7 byte sector extension and 7 byte ECC are the default after a master reset (due to RLL default). If E is 0 then a 4 byte sector extension and 4 byte ECC are selected if MFM or NRZ mode; if E is 1 then a 7 byte sector extension and 7 byte ECC are selected.

The H bit selects either 3 or 4 head select bits in the SDH register. If H=0, then 3 head select bits are written or compared in the ID fields on the drive. If H=1, then 4 head select bits are written or compared in the ID fields on the drive. The default after master reset is 3 head select bits.

The S bit is used to select either a 5 bit or 11 bit correction span if 4 byte ECC and an 11 bit or 22 bit correction span if 7 byte ECC. An 11 bit correction span is the default parameter following master reset. If S is 0, then a 5 bit correction span is selected if 4 byte ECC, 11 bit correction span if 7 byte ECC. If S is 1 then an 11 bit correction span is selected if 4 byte ECC , 22 bit correction span if 7 byte ECC.

The Z bit is used to select MFM, RLL, or NRZ mode. If K=0 in the load parameter block command, then RLL coding is selected regardless of

the state of Z. If Z is 0 and K is 1, then MFM coding is selected. If Z is 1 and K = 1, then NRZ coding is selected.

The R option is used to enable relocation ID searches. If R=1 for read and write sector commands and a bad block mark is detected in the desired sector's ID, then the WD42C22A searches for a special ID field containing relocation information immediately after the desired sector's ID. This special ID field is placed using the write ID command. When the R option is used, then the U option must be set to 1 in the load parameter block command.

Command Flow:

- MICRO: 1. Issue set parameter command to WD42C22A.
- WD42C22A: 2. Write 'FF' to the alternate sector number register (3C hex). Abort if drive not ready or write fault.
  3. Set or reset internal parameter flip-flop.
  4. Set DCI (bit 3) in the interface status register (38 hex). MCINT asserted.
- MICRO: 5. Read disk controller status register (27 hex) and error register (21 hex).

Error Flags:

- None.

4.4.10 LOAD PARAMETER BLOCK

The D bit is used to indicate the sectoring mode. If D = 0, the default after a master reset, then soft sector mode is selected. If D = 1, then hard sector mode is selected. In hard sector mode, the PLO length register is transferred to the internal GAP length register during the load parameter block command. This GAP register is used to control the delay from INDEX/SECTOR to READ GATE on.

The K bit selects the data interface mode. If K=0, the default after a reset, then RLL mode is selected. If K=1, then the interface is either MFM or NRZ as selected by the set parameter command.

The U bit selects the sector size options. If U=0, then the sector sizes are 128, 256, 512, and 1024 depending on the contents of the SDH register. If U=1, then the sector size is defined by the user. The cylinder registers are loaded with the desired sector size prior to issuing the load parameter block command.

In addition, the load parameter block command is used to load several internal parameters for format, read, and write commands. The task file is loaded with these parameters prior to the start of the command. The registers loaded and the corresponding parameters are:

REGISTER	PARAMETER
21	Delay from INDEX/SECTOR to RG
22	Data written in GAPS
23	Data written in PADS
24	LS byte of sector size, LS byte of offset for write ID command
25	3 MS bits of sector size, 3 MS bits of offset for write ID command

Command Flow:

- MICRO: 1. Load parameters into task file.
  2. Issue load parameter block command to WD42C22A.
- WD42C22A: 3. Write 'FF' to the alternate sector number register (3C hex). Abort if drive not ready or write fault.
  4. Set or reset internal parameter flip-flop.
  5. Copy cylinder registers to internal sector size register. Copy PLO register to internal GAP register. Copy sector count register to internal GAP data register. Copy sector number register to internal PAD data register.
  6. Set DCI (bit 3) in the interface status register (38 hex). MCINT asserted.
- MICRO: 7. Read disk controller status register (27 hex) and error register (21 hex).

Error Flags:

- None.

4.4.11 SLEEP

The sleep command places the WD42C22A in a low power standby mode. When the sleep command is issued to the disk controller section, clocks are disabled and only the buffer manager and host interface logic is enabled. The disk controller can be brought out of the sleep mode by setting RDC=1 (bit 7) in the disk controller control register (3B hex) or by resetting the entire WD42C22A. The microcontroller should **NEVER** attempt to read or write the drive controller task file (registers 21 hex through 27 hex) while the drive controller is in the sleep mode.

Command Flow:

- MICRO: 1. Issue sleep command to WD42C22A.
- WD42C22A: 2. Write 'FF' to the alternate sector number register (3C hex).
  3. Disable drive controller clocks.
- MICRO: 4. Wake up disk controller by setting RDC=1 or by resetting the WD42C22A.

Error Flags:

- None.

4.4.12 DUMP

The dump command sends data off the media regardless of matching ID fields and regardless of the format. The command can dump an ID field, a data field, or both. Dump retrieves all the ID fields from index to index to determine the interleave. Dump can also read the ESDI standard defect list. The command dumps data starting at the first byte after the A1 sync byte for WD format or the first byte after the FE sync byte for ESDI format. This command can only do multisector dumps in hard sector mode.

The command is assumed to be a multisector command. To read just one sector as in an ESDI defect list read, then the sector count must be set to one. There are three options.

The I option controls the number of fields that are dumped for each sector. If I=0, then two fields (ID and data) are dumped for each sector. If I=1, then only one field is dumped for each sector. The type of field is determined by the read gate delay and the sector size. The sector size should be programmed to 1 less than the number of bytes to be dumped for the sector.

The B option controls the sync byte and CRC preset. If B=0, then the sync byte is assumed to FE and the CRC is preset to all zeroes. If B=1, then the sync byte is assumed to be A1 and the CRC is preset to all ones.

The L option selects either CRC or no CRC checking. If L=0, then CRC is checked. If L=1, then either four or seven check bytes are transferred to the buffer depending on the extension selected by the set parameter command. If L=1, then I should also be set to 1. B does not affect the L option.

The PLO register controls the read gate delay fo r the first sector. READ GATE turns on x + 5 + CL bytes after the index pulse. Read gate for subsequent sectors is controlled as in normal read and write commands.

Use the dump command to read an ESDI defect list as follows:

1. Set PLO register = read gate delay - 5.
2. Set sector size = 255 for 256 byte sector.
3. Issue A1 command.

Use the dump command to dump the track interleave for WD format as follows:

1. Set PLO register = read gate delay - 5.
2. Set sector size = 4.
3. Set sector count = number of sectors per track.
4. Issue AD command.

Use the dump command to dump all the data fields on a track for WD format as follows:

1. Set PLO register = read gate delay to start of data PLO - 5.

2. Set sector size = actual number of bytes per sector.

3. Set sector count = number of sectors per track.

4. Issue AF command or AB command.

In this case, the F8 second data sync byte is transferred to the buffer. The buffer requires one extra byte per sector.

One BRDQ interrupt occurs at the very beginning of the command. Therefore, the buffer must be contiguous and large enough to handle all the dumped sectors.

Command Flow:

- MICRO:
  1. Set DRWB=0 (bit 2) in the buffer manager control register (37 hex.)
  2. Load the starting address of the buffer into the disk buffer pointer register (34 & 35 hex).
  3. Set ECCM=0 (bit 7) and DDRQ=1 (bit 6) in the DIR write register (3F hex) and MAC=1 (bit 3) in the drive interface control register (3B hex) to disable DRQI, if desired.
  4. Set ADBP=1 (bit 0) in the buffer manager control register (37 hex).
  5. Set MAC=0 in the drive interface control register.
  6. Issue dump command to WD42C22A.
- WD42C22A
  7. Write FF to alternate sector number register (3C hex). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY indicating transfer of buffer pointer.
- MICRO: Set RDQI (bit 1) in the interface control register (38 hex).
- WD42C22A:
  9. Wait for index.
  10. If I=1, then go to 12 else go to 11.
  11. Search for sync byte. When found, dump 5 data bytes into buffer.
  12. Search for sync byte. When found, dump programmed number of bytes into the buffer.
  13. Decrement sector count. If sector count = 0, then go to 14 else go to step 10.
  14. Set DCI (bit 3) in the interface status register (38 hex). MCINT asserted.
- MICRO:
  15. Read disk controller status register (27 hex) and errror register (21 hex).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- ID not found set if I=0 and index detected while searching for an ID field or if CRC of ID field doesn't zero.
- Data AM not found is set and index is detected while searching for a data field. If I=0 or when searching for either an ID or data field when I=1.
- Data CRC if the data field CRC doesn't zero when I=0 or if either an ID or data field CRC doesn't zero when I=1.

ERRATA

There is a current problem with the dump command. When the dump commamd is executed, there is sometimes an extra byte transferred after either the ID or the data field. When the I=1 option is used, then there is sometimes an extra byte after the expected bytes in the buffer. When the I=0 option is used, then there can be an extra byte between the ID and data fields and it is therefore impossible to determine where the data field starts in the buffer.

The fix for this problem has been identified and will be implemented on any new versions of the WD42C22A. Currently, there is a firmware workaroun to read an ESDI defect list. If the I=1 option is used, then the buffer contains the correct expected data. The firmware ensures that the buffer has one more byte than the number of bytes ex-

pected to be transferred from the WD42C22A.
To read the ID:

1. Set PLO register = **A** - 5. Refer to the following illustration.
2. Set sector size = 4 (for 5 byte ID). Use load parameter command to set sector size.
3. Issure A9 command.

To read the data:

1. Set PLO register = **B** - 5. Refer to the illustration above.
2. Set sector size = 255 (for 256 byte data). Use load parameter command to set sector size.
3. Issue A9 command.

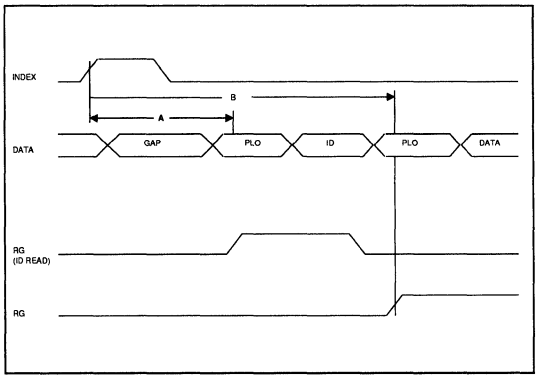


Figure 6. DUMP COMMAND

32

5.0 ELECTRICAL AND TIMING SPECIFICATIONS

5.1 MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (ground) ..... +5 V ± 5%

Max voltage on any pin with respect to V_{SS} ..... -0.5V to 5.5

Operating temperature (T_A) ..... 0°C (32°F) to 70°C (158°F)

Storage temperature ..... 55°C (-67°F) to 125°C (257°F)

NOTE

Maximum limits where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

5.2 DC OPERATING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		±10	µA	V_{IN} = 0.4 to V_{CC}
I_{OZ}	Tri-state and open drain output leakage		±10	µA	V_{OUT} = 0.4 TO V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_{OUT}=-800µA
V_{OL}	Output Low Voltage		0.4	V	I_{OUT}=2.0mA
I_{CC}	Supply Current		100	mA	All outputs open.
I_{CCS}	Supply Current (Standby Mode)		25	mA	All inputs at V_{DD} or V_{SS}, disk controller sleep mode, 15 MHz crystal.

TABLE 14. DC OPERATING CHARACTERISTICS

For pins 75 thru 82, 40 thru 42, 44 thru 48, 74, 8 (HD0 thru HD15, INTRQ, DREQ):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		V	I_{OUT}=-5mA
V_{OL}	Output Low Voltage		0.4	V	I_{OUT}=12mA

For pin 8 ($\overline{IOCS16}$, AT PIO mode only):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.4	V	I_O=20.0mA

For pins 10, 11, and 12 (WD, EARLY, LATE):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4			I_O=-800µA
V_{OL}	Output Low Voltage		0.4	V	I_O=6.0mA

For pin 22 ($\overline{\text{RESET}}$)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.4	V	I_O=6.0 mA

For pins 36, 37 ($\overline{\text{DS0}}$, $\overline{\text{DS1}}$):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.4	V	I_O=48.0 mA

For pins 59-73 (BA0-B14)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{PD}	Pulldown Current in read config. mode	40	160	µA	V_{OUT}=2.4V

For pins 5, 6, 9 ($\overline{\text{HRE}}$, $\overline{\text{HWE}}$, and $\overline{\text{DACK}}$ in slave host mode) and pins 40-42, 44-48 (HD8 through HD15 in 8-bit host mode):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{PU}	Pullup Current	100	2000	µA	V_{OUT}=0.4 V, V_{DD}=5.25 V

For pin 38 (XTALIN when driven by external osc.):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{IH}	Input High Voltage	3.5		V	
VIL	Input Low Voltage		1.0	V	

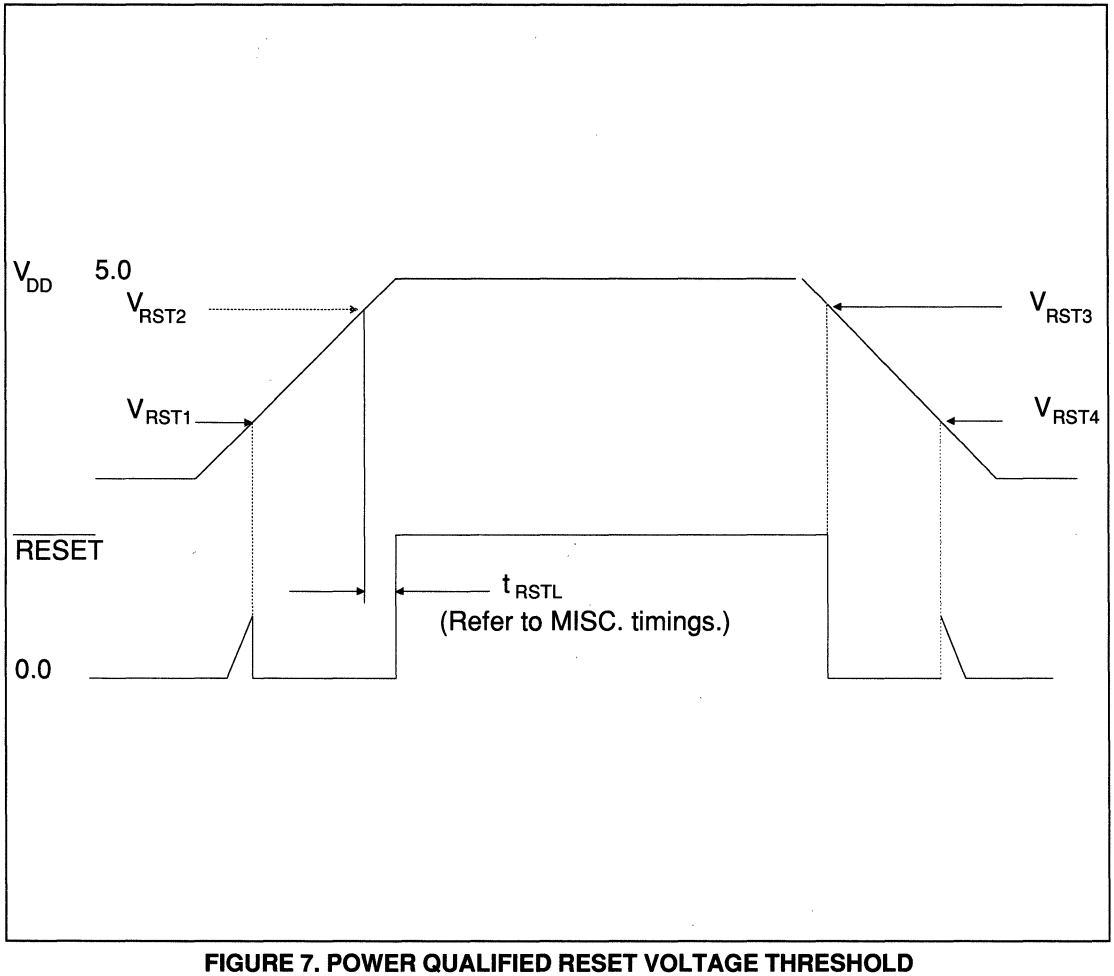


FIGURE 7. POWER QUALIFIED RESET VOLTAGE THRESHOLD

For pin 84 (V_{DD})

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{RST1}	Power Qualified Reset	0.0	2.0	V	See Figure 7.
V_{RST2}	Voltage Threshold	2.5	4.6	V	
V_{RST3}		2.5	4.6	V	
V_{RST4}		0.0	2.0	V	

5.3 AC TIMING CHARACTERISTICS

NOTE

Load capacitance=50 pF each for all other outputs. Timings must be derated for larger load capacitances.

For pins 14, 16, 17, 19 (WC, DRUN, RD, RC):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{RS}	Rise Time		10	nsec	10% to 90%

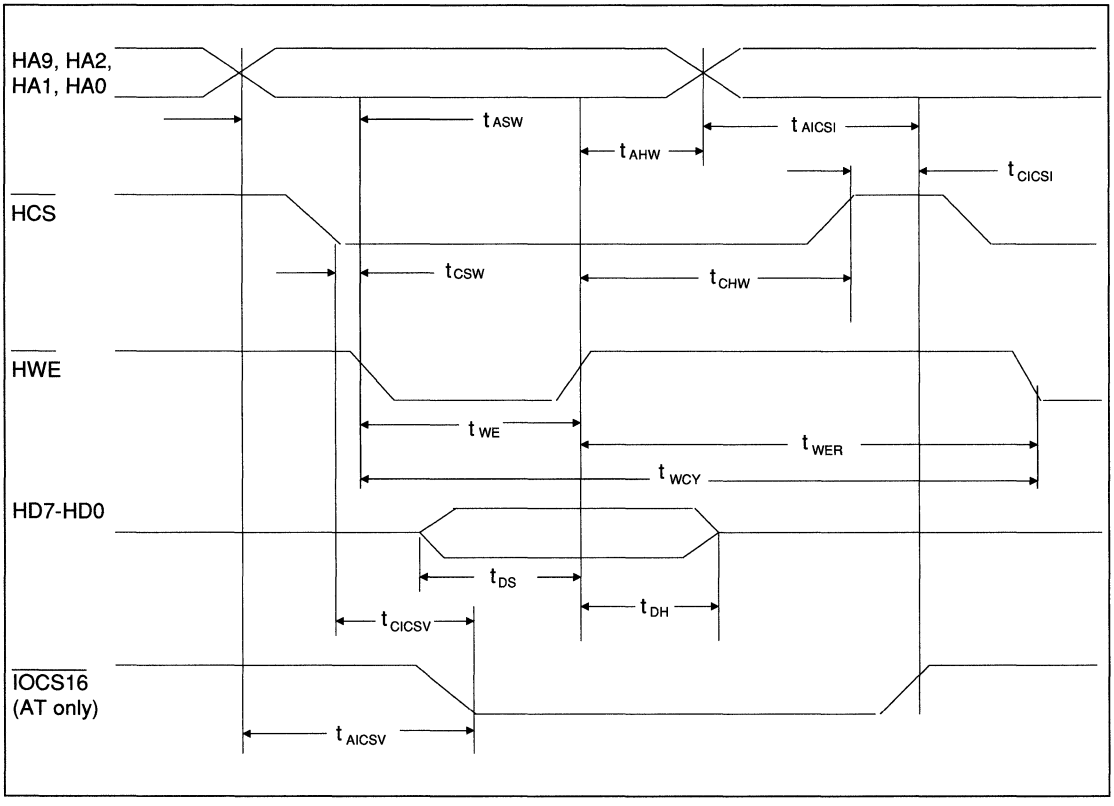


FIGURE 8. AT/XT HOST PROGRAMMED I/O WRITE TIMING

NOTE

A write occurs during the overlap of $\overline{HCS}$ and $\overline{HWE}$.

5.3.1 AT/XT HOST PROGRAMMED I/O WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{ASW}	Address Setup to $\overline{HWE}$ Low	30		ns	
t_{CSW}	$\overline{HCS}$ Setup to $\overline{HWE}$ Low	10		ns	
t_{DS}	Data Setup to $\overline{HWE}$ High	50		ns	Port 0 only.
t_{WE}	$\overline{HWE}$ Pulse Width	75		ns	Port 0 only.
t_{DS}	Data Setup to $\overline{HWE}$ High	50		ns	All other ports.
t_{WE}	$\overline{HWE}$ Pulse Width	100		ns	All other ports
t_{DH}	Data Hold from $\overline{HWE}$ High	15		ns	
t_{AHW}	ADDR Hold from $\overline{HWE}$ High	20		ns	
t_{CHW}	$\overline{HCS}$ Hold from $\overline{HWE}$ High	10		ns	
t_{WER}	$\overline{HCS}$ and $\overline{HWE}$ Inactive	20		ns	
t_{WCY}	Write Cycle Time	100 2*X		ns	Port 0, XTAL=20 MHz Port 0, Any XTAL (X=tXTAL)
t_{WCY}	Write Cycle Time	150		ns	All other ports
t_{CICSV}	$\overline{IOCS16}$ valid from $\overline{HCS}$		30	ns	
t_{AICSV}	$\overline{IOCS16}$ valid from address		40	ns	
t_{CICSI}	$\overline{IOCS16}$ inactive from $\overline{HCS}$		35	ns	Test circuit 1.
t_{AICSI}	$\overline{IOCS16}$ inactive from address		45	ns	Test circuit 1.

TABLE 15. AT/XT HOST PROGRAMMED I/O WRITE TIMING

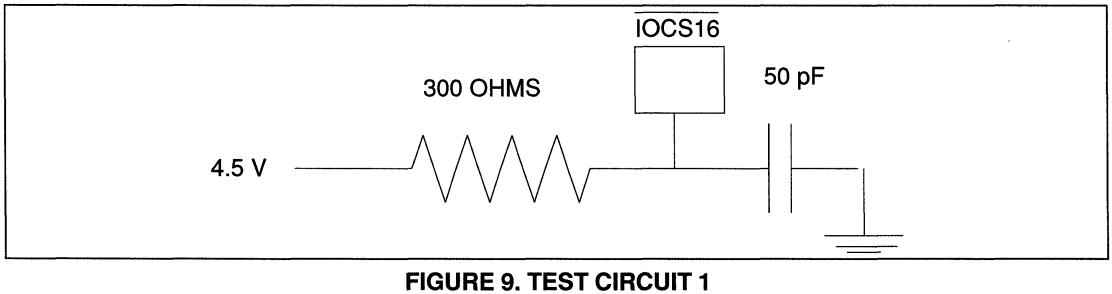


FIGURE 9. TEST CIRCUIT 1

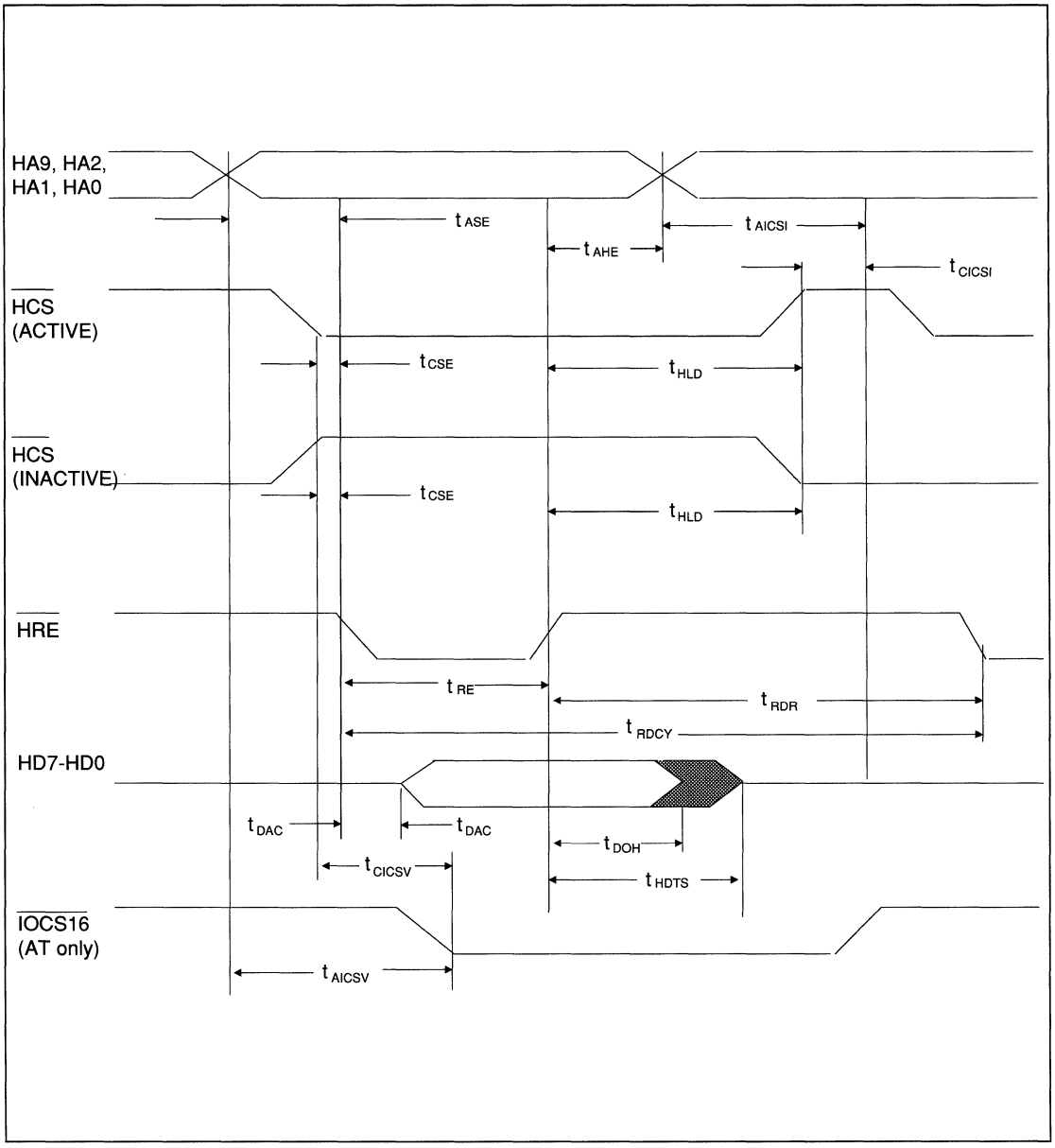


FIGURE 10. AT/XT HOST PROGRAMMED I/O READ TIMING

5.3.2 AT/XT HOST PROGRAMMED I/O READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{ASE}	Address Setup to $\overline{HRE}$ Low	30		ns	
t_{CSE}	$\overline{HCS}$ Setup to $\overline{HRE}$ Low	10		ns	
t_{DAC}	Data Valid from $\overline{HRE}$ Low		60 70 100	ns	Port 0, 8-bit. Port 0, 16-bit. All other ports.
t_{RE}	$\overline{HRE}$ Pulse Width	75 100		ns	Port 0 All other ports
t_{DOH}	Data Hold from $\overline{HRE}$ High	5		ns	
t_{HDTS}	Data Tri-state from $\overline{HRE}$		50	ns	
t_{HLD}	Address, $\overline{HCS}$ Hold from $\overline{HRE}$ High	10		ns	
t_{RDR}	$\overline{HCS}$ and $\overline{HRE}$ Inactive	20		ns	
t_{RDCY}	Read Cycle Time	100 2*X		ns	Port 0, XTAL=20 MHz Port 0, Any XTAL (X=t_{XTAL})
t_{RDCY}	Read Cycle Time	150		ns	All other ports. XTAL=20 MHz
t_{CICSV}	$\overline{IOCS16}$ Valid from $\overline{HCS}$		30	ns	
t_{AICSV}	$\overline{IOCS16}$ Valid from Address		40	ns	
t_{CICSI}	$\overline{IOCS16}$ Inactive from $\overline{HCS}$		35	ns	Test circuit 1
t_{AICSI}	$\overline{IOCS16}$ Inactive from Address		45	ns	Test circuit 1

TABLE 16. AT/XT HOST PROGRAMMED I/O READ TIMING

5.3.3 AT/XT HOST DMA WRITE TIMING

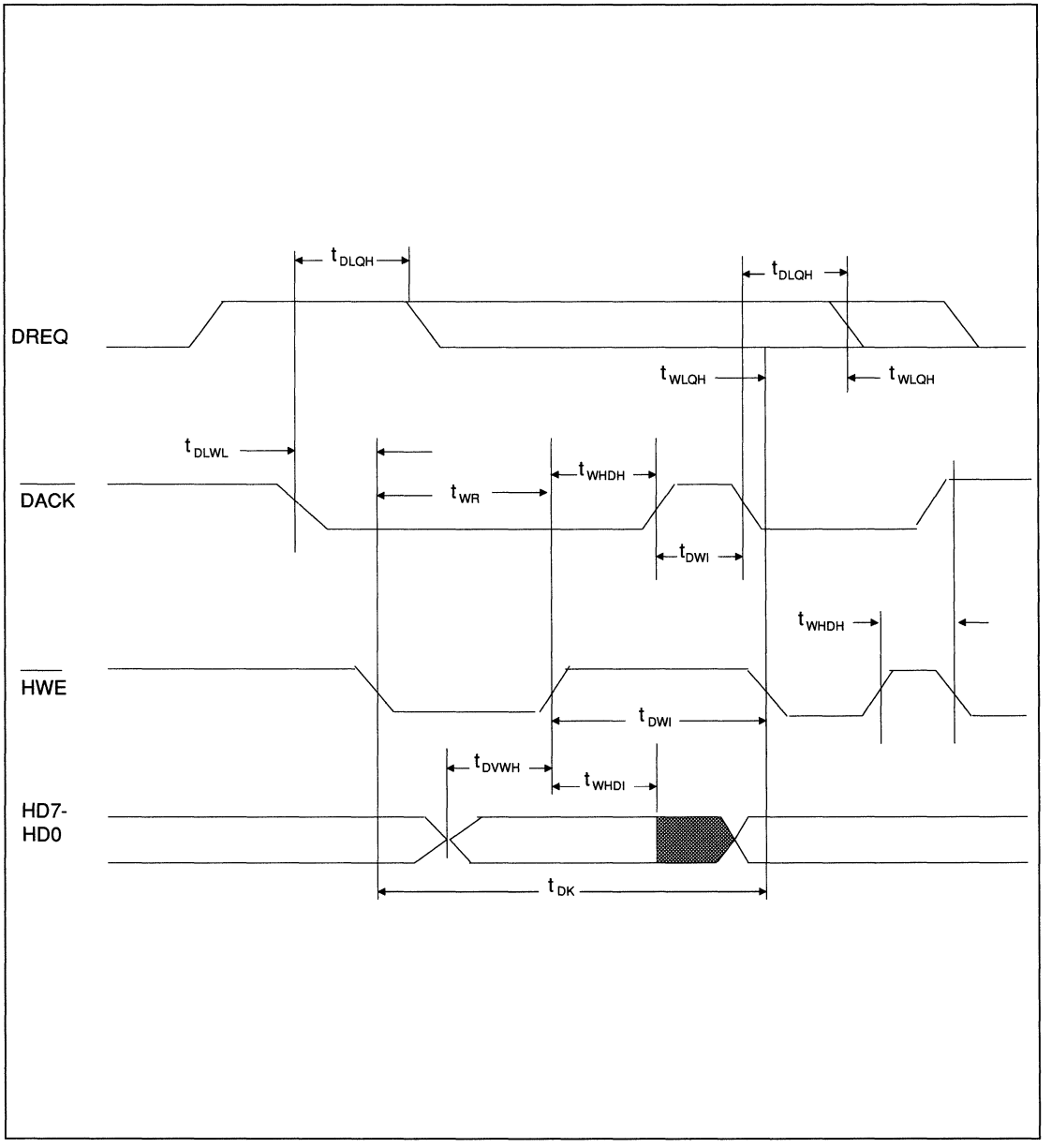


FIGURE 11. AT/XT HOST DMA WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{DLQH}	$\overline{DACK}$ Low to DRQ Low		100	ns	BDEN=0
t_{WLQH}	$\overline{HWE}$ Low to DRQ Low		100	ns	BDEN=1 (Transfer count throttle)
t_{WHQH}	$\overline{HWE}$ High to DRQ Low		100	ns	BDEN =1 (First transfer count throttle)
t_{DK}	DMA Cycle	100 2*X		ns	XTAL=20MHz Any XTAL (X=t_{XTAL})
t_{DLWL}	$\overline{DACK}$ Low to $\overline{HWE}$ Low	0		ns	
t_{WR}	$\overline{HWE}$ Pulse Width	80 100 - t_{DLWL}		ns	$t_{DLWL} \geq 20$ $t_{DLWL} < 20$
t_{DVWH}	Data Valid to $\overline{HWE}$ High	50		ns	
t_{WHDH}	$\overline{HWE}$ High to $\overline{DACK}$ High	0		ns	
t_{WHDI}	$\overline{HWE}$ High to Data Invalid	15		ns	
t_{DWI}	$\overline{DACK}$ and $\overline{HWE}$ Inactive	20		ns	

TABLE 17. AT/XT HOST DMA WRITE TIMING

5.3.4 AT/XT HOST DMA READ TIMING

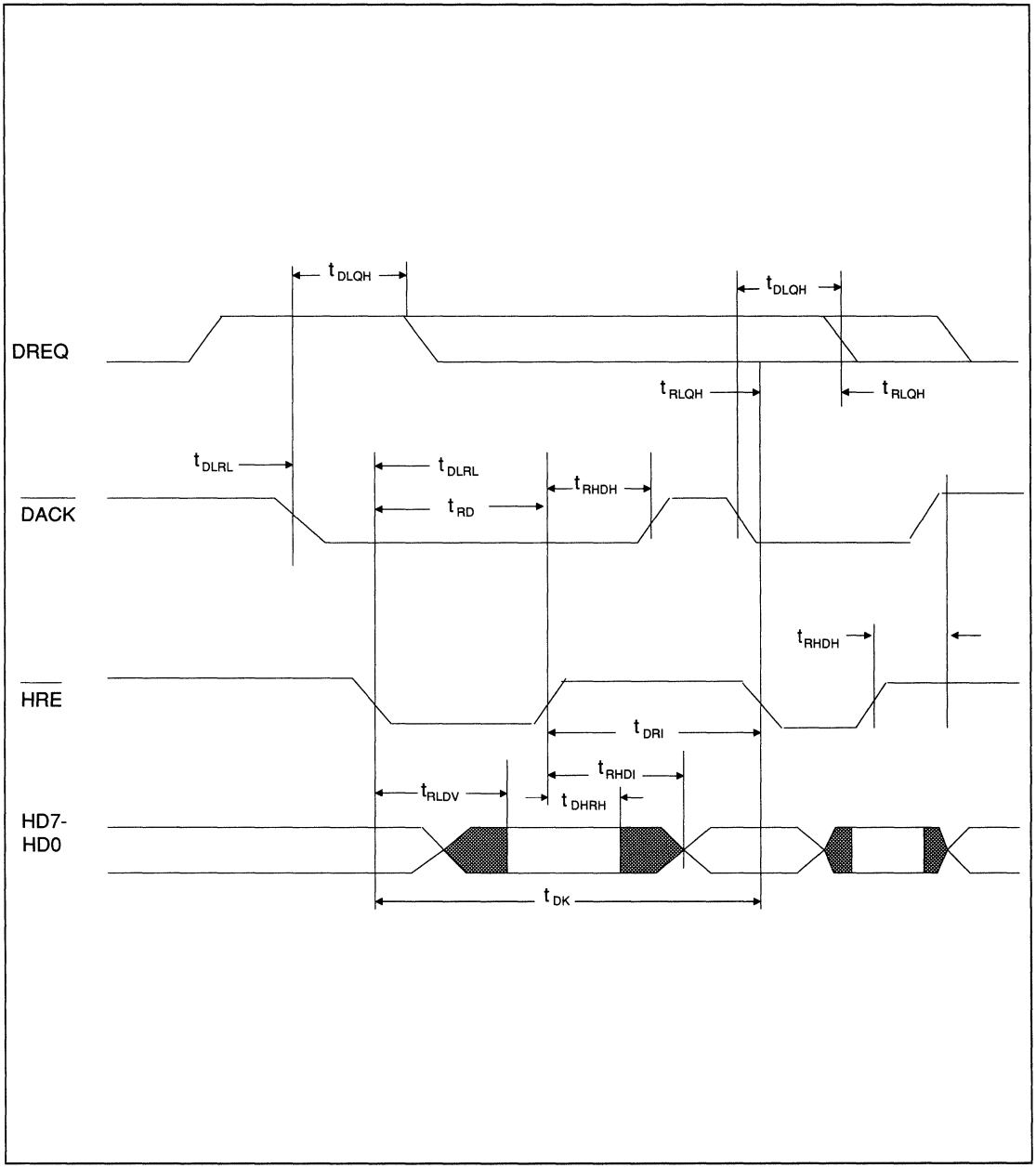


FIGURE 12. AT/XT HOST DMA READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{DLQH}	$\overline{DACK}$ Low to DRQ Low		100	ns	BDEN=0
t_{RLQH}	$\overline{HRE}$ Low to DRQ Low		100	ns	BDEN=1 (Transfer count throttle)
t_{RHQH}	$\overline{HRE}$ High to DRQ Low		100	ns	BDEN=1 (First TC throttle)
t_{DK}	DMA Cycle	100 2*X		ns	XTAL=20MHz Any XTAL (X=t_{XTAL})
t_{DLRL}	$\overline{DACK}$ Low to $\overline{HRE}$ Low	20		ns	
t_{RD}	$\overline{HRE}$ Pulse Width	80 100 - t_{DLRL}		ns	$t_{DLWL} \geq 20$ ns $t_{DLRL} < 20$ ns
t_{RLDV}	$\overline{HRE}$ Low to Data Valid		60 80 - t_{DLRL}	ns	8-bit mode. $t_{DLRL} \geq 20$ ns 8-bit mode. $t_{DLRL} < 20$ ns
t_{RLDV}	$\overline{HRE}$ Low to Data Valid		70 90 - t_{DLRL}	ns	16-bit mode. $t_{DLRL} \geq 20$ ns 16-bit mode. $t_{DLRL} < 20$ ns
t_{RHDH}	$\overline{HRE}$ High to $\overline{DACK}$ High	0		ns	
t_{DHRH}	Data Hold from $\overline{HRE}$ High	5		ns	
t_{RHDI}	$\overline{HRE}$ High to Data tri-state		50	ns	
t_{DRI}	$\overline{DACK}$ and $\overline{HRE}$ Inactive	20		ns	

TABLE 18. AT/XT HOST DMA READ TIMING

5.3.5 SLAVE HOST WRITE TIMINGS

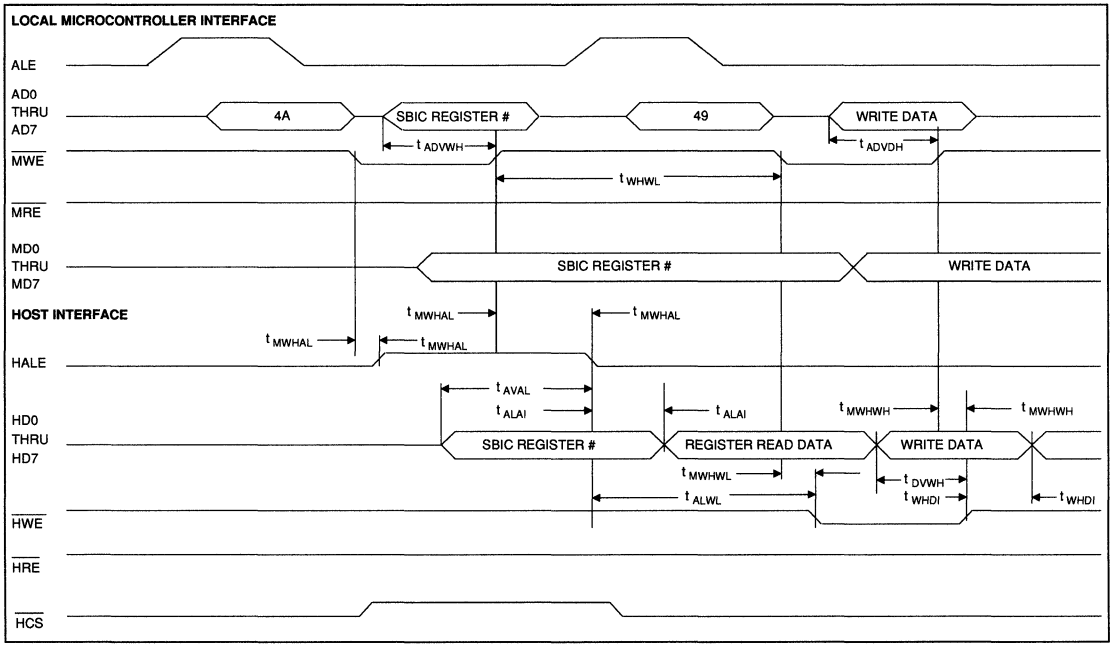


FIGURE 13. SLAVE HOST WRITE TIMING

32

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{WHWL}	Address Port Write to Data Write Recovery Time	120	10000	ns	
t_{MWHAL}	$\overline{MWE}$ to HALE Delay		150	ns	
t_{AVAL}	HD Address Setup to HALE Low	40		ns	AD setup to $\overline{MWE}$ (t_{ADVWH})=130 ns
t_{ALAI}	HD Address Hold From HALE low	0		ns	
t_{ALWL}	HALE Low To $\overline{HWE}$ Low	90		ns	
t_{DVWH}	HD Valid to $\overline{HWE}$ High	70		ns	AD setup to $\overline{MWE}$ (t_{ADVWH})=130 ns
t_{WHDI}	HD Inactive from $\overline{HWE}$	0		ns	
t_{MWHWL}	$\overline{MWE}$ Low to HWE Low		150	ns	
t_{MHWH}	MWE High to HWE High		150	ns	

TABLE 19. SLAVE HOST WRITE TIMING

5.3.6 SLAVE HOST READ TIMINGS

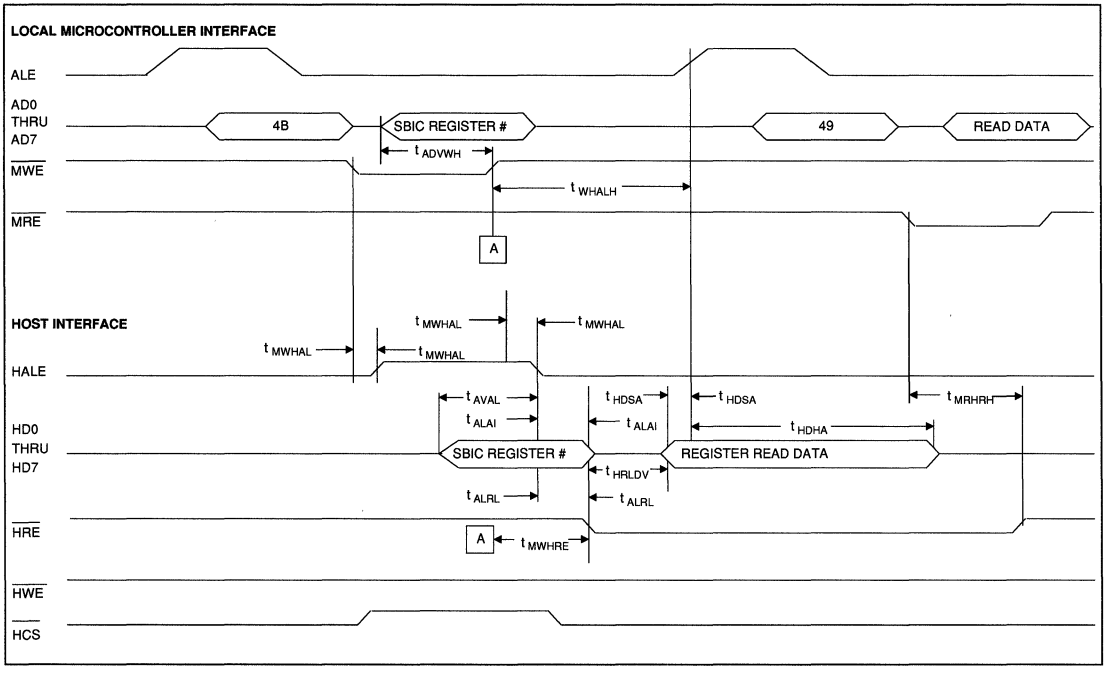


FIGURE 14. SLAVE HOST READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{WHALH}	Address Port Write to ALE High Read Recovery Time	400	10000	ns	t_{HRLDV}=210 ns
t_{MWHAL}	$\overline{MWE}$ to HALE Delay		150	ns	
t_{MHRE}	$\overline{MWE}$ to $\overline{HRE}$ Delay		150	ns	
t_{AVAL}	HD Address Setup to HALE Low	40		ns	AD setup to $\overline{MWE}$ (t_{ADVWH})=130 ns.
t_{ALAI}	HD Address Hold from HALE Low	0		ns	
t_{ALRL}	HALE Low to $\overline{HRE}$ Low	0	50	ns	
t_{HDSA}	HD Data **Setup to** ALE High	40		ns	
t_{HDSA}	HD Data **Hold from** ALE High	40		ns	
t_{MRHRH}	$\overline{MRE}$ Low to $\overline{HRE}$ High Delay	0		ns	
t_{HRLDV}	HRE Low to HD Data Valid Delay				t_{HRLDV} is a function of the slave peripheral device and only affects t_{WHALH}. t_{WALH} = t_{MHRE} + t_{HRLVDV} + t_{HDSA}

TABLE 20. SLAVE HOST READ TIMING

5.3.7 BUFFER RAM WRITE TIMING (INTERNAL OSCILLATOR; XTAL = 8 to 20 MHz))

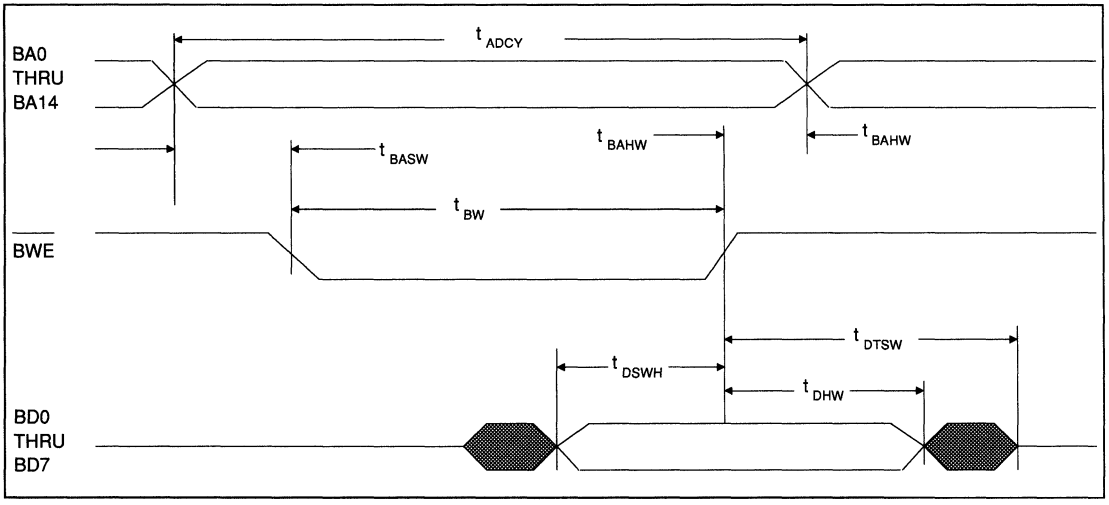


FIGURE 15. BUFFER RAM WRITE TIMING (INTERNAL OSCILLATOR)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	72 125		ns	Max XTAL
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35		ns	Any XTAL
t_{BASW}	Addres Setup to BWE Low	5 5		ns	Max XTAL
t_{BASW}	Addres Setup to BWE Low	$0.5*t_{XTAL}$-20 $0.5*t_{XTAL}$-35		ns	Any XTAL
t_{BW}	BWE Pulse Width	55 85		ns	Max XTAL
t_{BW}	BWE Pulse Width	$1.5*t_{XTAL}$-20 $1.5*t_{XTAL}$-35		ns	Any XTAL
t_{BAHW}	Address Hold From BWE High	5 5		ns	Any XTAL
t_{DSWH}	Data Valid to BWE High	35 60		ns	Max XTAL
t_{DSWH}	Data Valid to BWE High	$1.5*t_{XTAL}$-40 $1.5*t_{XTAL}$-60		ns	Any XTAL
t_{DHW}	Data Hold from BWE High	10 10		ns	Any XTAL
t_{DTSW}	Data Tri-state from BWE High		50	ns	Any XTAL

TABLE 21. BUFFER RAM WRITE TIMING (INTERNAL OSCILLATOR)

5.3.8 BUFFER RAM READ TIMING (INTERNAL OSCILLATOR; XTAL = 8 to 20 MHz)

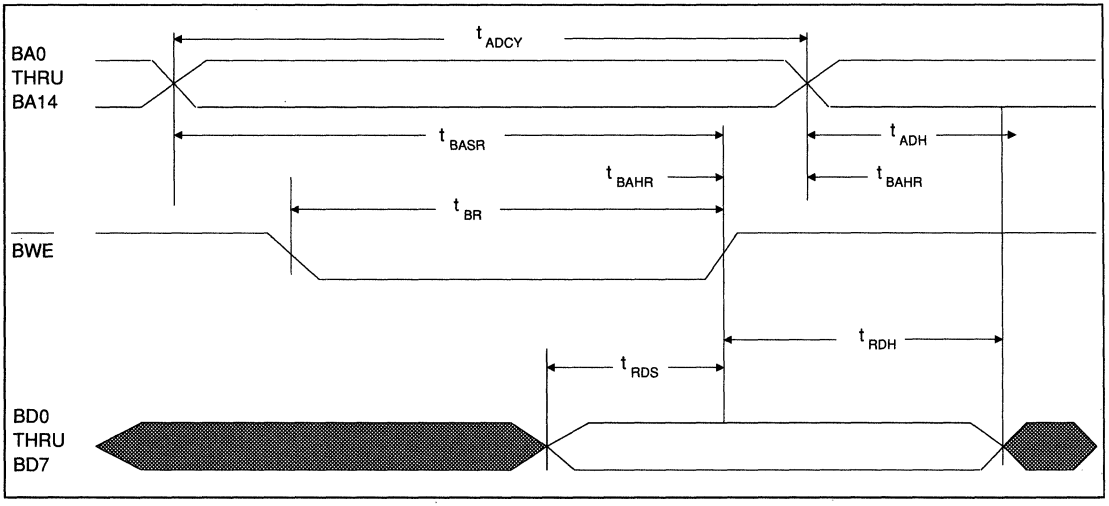


FIGURE 16. BUFFER RAM READ TIMING (INTERNAL OSCILLATOR)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	72 125	ns	Max XTAL
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	Any XTAL
t_{BASR}	Address Setup to $\overline{BOE}$ High	72 125	ns	Max XTAL
t_{BASR}	Address Setup to $\overline{BOE}$ High	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	Any XTAL
t_{BR}	$\overline{BOE}$ Pulse Width	45 75	ns	Max XTAL
t_{BR}	$\overline{BOE}$ Pulse Width	$1.5*t_{XTAL}$-30 $1.5*t_{XTAL}$-45	ns	Any XTAL
t_{BAHR}	Address Hold from $\overline{BOE}$ High	0 0	ns	Any XTAL
t_{RDS}	Data Setup to $\overline{BOE}$ High	5 5	ns	Any XTAL
t_{RDH}	Data Hold from $\overline{BOE}$ High	10 10	ns	Any XTAL
t_{DHW}	Data Hold from Address	10 10	ns	

- All timings in this table **only** are referenced to 1.5V levels.

TABLE 22. BUFFER RAM READ TIMING (INTERNAL OSCILLATOR)

5.3.9 BUFFER RAM WRITE TIMING (EXTERNAL OSCILLATOR; XTAL = 8 to 20 MHz)

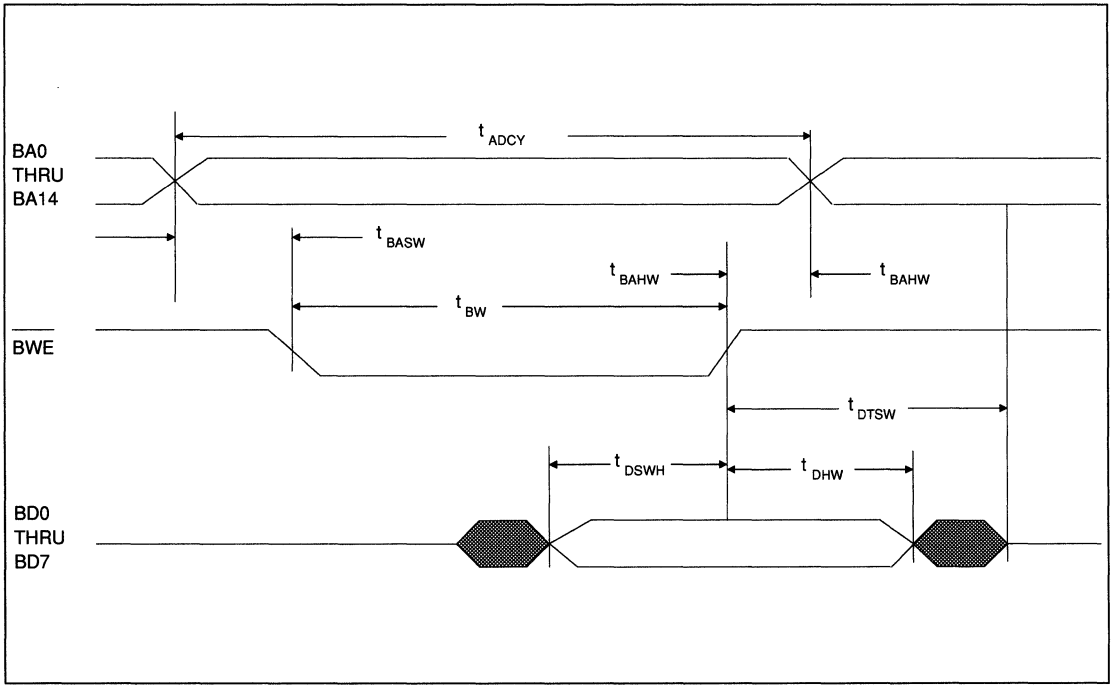


FIGURE 17. BUFFER RAM WRITE TIMING (EXTERNAL OSCILLATOR)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	72 125		ns	Max XTAL
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35		ns	Any XTAL
t_{BASWL}	Address Setup to $\overline{BWE}$ Low	5 5		ns	Max XTAL/ 50% XTAL
t_{BASWL}	Address Setup to $\overline{BWE}$ Low	t_{XCH}-20 t_{XCH}-35		ns	Any XTAL
t_{BASWH}	Address Setup to $\overline{BWE}$ High	60 105		ns	Max XTAL
t_{BASWH}	Address Setup to $\overline{BWE}$ High	$2*t_{XTAL}$-40 $2*t_{XTAL}$-55		ns	Any XTAL
t_{BW}	$\overline{BWE}$ Pulse Width	55 85		ns	Max XTAL/ 50% XTAL
t_{BW}	$\overline{BWE}$ Pulse Width	$t_{XTAL}+t_{XCL}$-30 $t_{XTAL}+t_{XCL}$-35		ns	Any XTAL
t_{BAHW}	Address Hold from $\overline{BWE}$ High	5 5		ns	Any XTAL
t_{DSWH}	Data Valid to $\overline{BWE}$ High	35 60		ns	Max XTAL
t_{DSWH}	Data Valid to $\overline{BWE}$ High	$t_{XTAL}+t_{XCH}$-40 $t_{XTAL}+t_{XCH}$-60		ns	Any XTAL/ %50 XTAL
t_{DHW}	Data Hold from $\overline{BWE}$ High	10 10		ns	Any XTAL
t_{DTSW}	Data tri-state from $\overline{BWE}$ High		50	ns	Any XTAL

• All timings in this table only are referenced to 1.5 V levels except t_{DHW}.

TABLE 23. BUFFER RAM WRITE TIMING (XTAL = 8 TO 20 MHZ)

5.3.10 BUFFER RAM READ TIMING (EXTERNAL OSCILLATOR; XTAL=8 to 20 MHz)

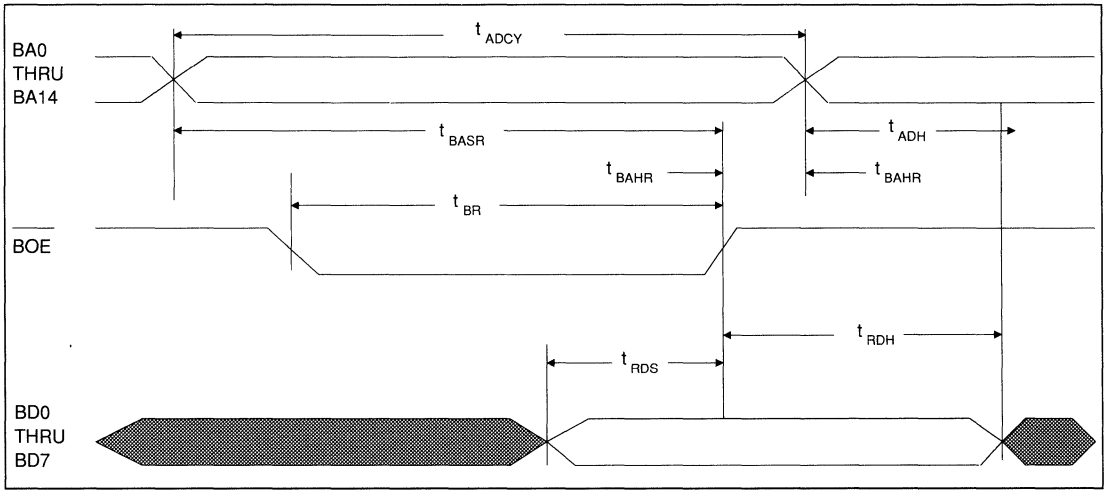


FIGURE 18. BUFFER RAM READ TIMING (EXTERNAL OSCILLATOR)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	72 125	ns	Max XTAL/50% XTAL
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	Any XTAL
t_{BASR}	Address Setup to $\overline{BOE}$ High	72 125	ns	Max XTAL/50% XTAL
t_{BASR}	Address Setup to $\overline{BOE}$ High	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	
t_{BR}	$\overline{BOE}$ Pulse Width	45 75	ns	Max XTAL/50% XTAL
t_{BR}	$\overline{BOE}$ Pulse Width	$t_{XTAL}+t_{XCH}$-30 $t_{XTAL}+t_{XCH}$-45	ns	Any XTAL
t_{BAHR}	Address Hold from $\overline{BOE}$ High	0 0	ns	Any XTAL
t_{RDS}	Data Setup to $\overline{BOE}$ High	5 5	ns	Any XTAL
t_{RDH}	Data Hold from $\overline{BOE}$ High	10 10	ns	Any XTAL
t_{DHW}	Data Hold from Address	10 10	ns	

• All timings in this table referenced to 1.5 V levels.

TABLE 24. BUFFER RAM READ TIMING (EXTERNAL OSCILLATOR)

5.3.11 MICROPROCESSOR WRITE TIMING (INTEL BUS)

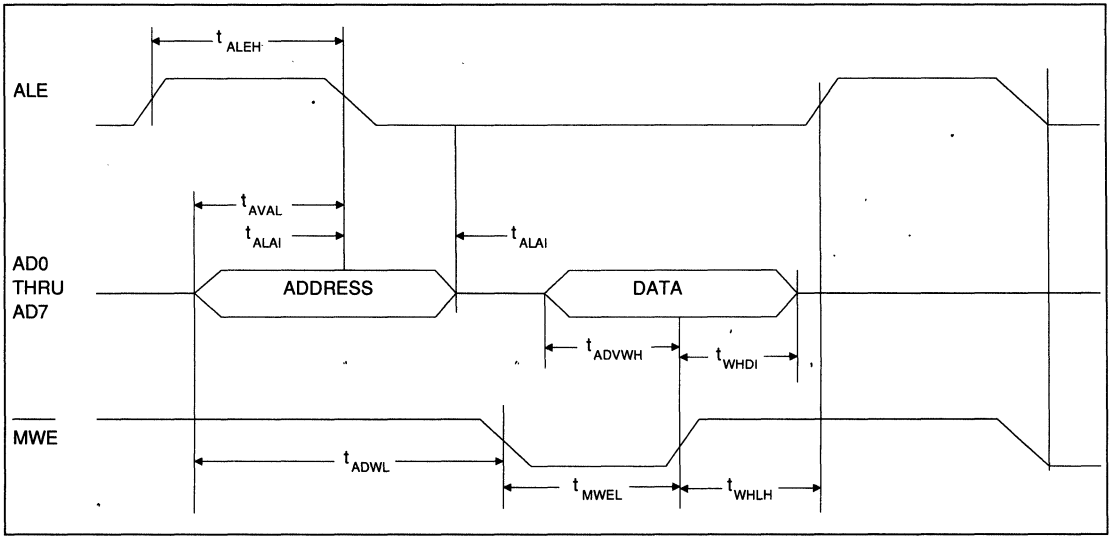


FIGURE 19. MICROPROCESSOR WRITE TIMING (INTEL BUS)

SYMBOL	CHARACTERISTIC	MIN	UNITS	CONDITIONS
t_{AVAL}	Address Setup to ALE Low	15	ns	
t_{ALAI}	Address Hold from ALE Low	5	ns	
t_{ALEH}	ALE High Pulse Width	30	ns	
t_{ADVWH}	Data Setup to $\overline{MWE}$ High	50 130	ns	HSMB=0 HSMB=1
t_{WHDI}	Data Hold from $\overline{MWE}$ High	5	ns	
t_{MWEL}	$\overline{MWE}$ Low Pulse Width	75	ns	
t_{ADWL}	Address Valid to $\overline{MWE}$ Low	55	ns	
t_{WHLH}	$\overline{MWE}$ High to ALE High	10	ns	

TABLE 25. MICROPROCESSOR WRITE TIMING (INTEL BUS)

5.3.12 MICROPROCESSOR WRITE TIMING (MOTOROLA BUS)

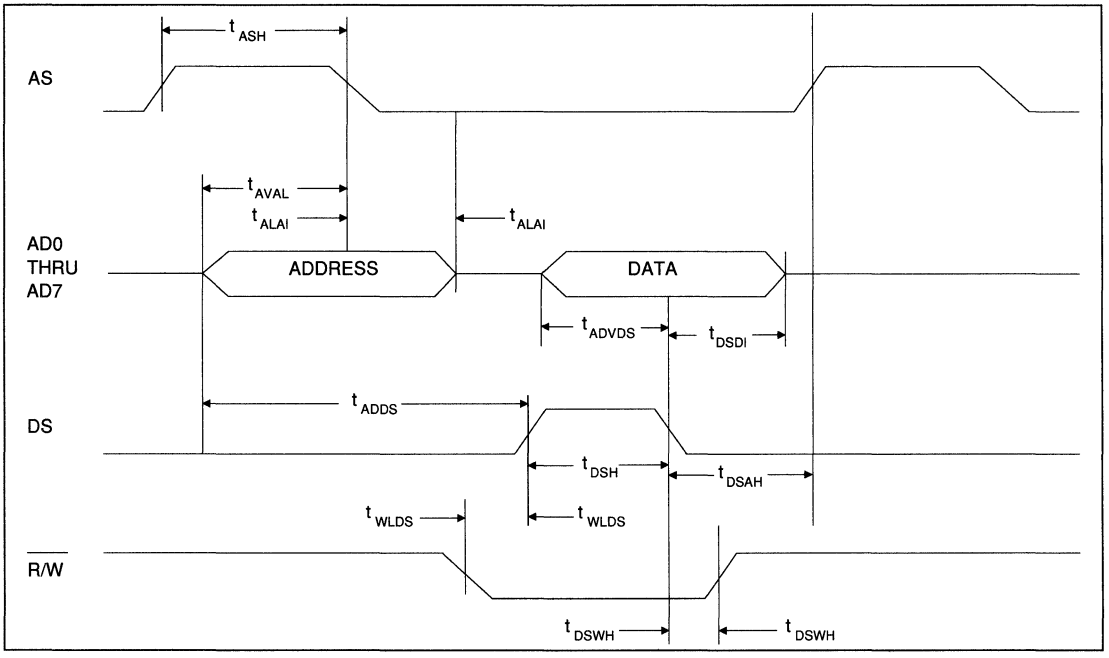


FIGURE 20. MICROPROCESSOR WRITE TIMING (MOTOROLA BUS)

32

SYMBOL	CHARACTERISTIC	MIN	UNITS	CONDITIONS
t_{AVAL}	Address Setup to AS Low	15	ns	
t_{ALAI}	Address Hold from AS	5	ns	
t_{ASH}	AS High Pulse Width	30	ns	
t_{ADVDS}	Data Setup to DS Low	50 130	ns	HSMB=0 HSMB=1
t_{DSDI}	Data Hold from DS Low	5	ns	
t_{DSH}	DS High Pulse Width during Write	75	ns	
t_{WLDS}	R/$\overline{W}$ Low to DS High	5	ns	
t_{DSWH}	DS Low to R/$\overline{W}$ High	20	ns	
t_{ADDS}	Address High to DS High	55	ns	
t_{DSAH}	DS Low to AS High	10	ns	

TABLE 26. MICROPROCESSOR WRITE TIMING (MOTOROLA BUS)

5.3.15 MICROPROCESSOR READ TIMING (INTEL BUS)

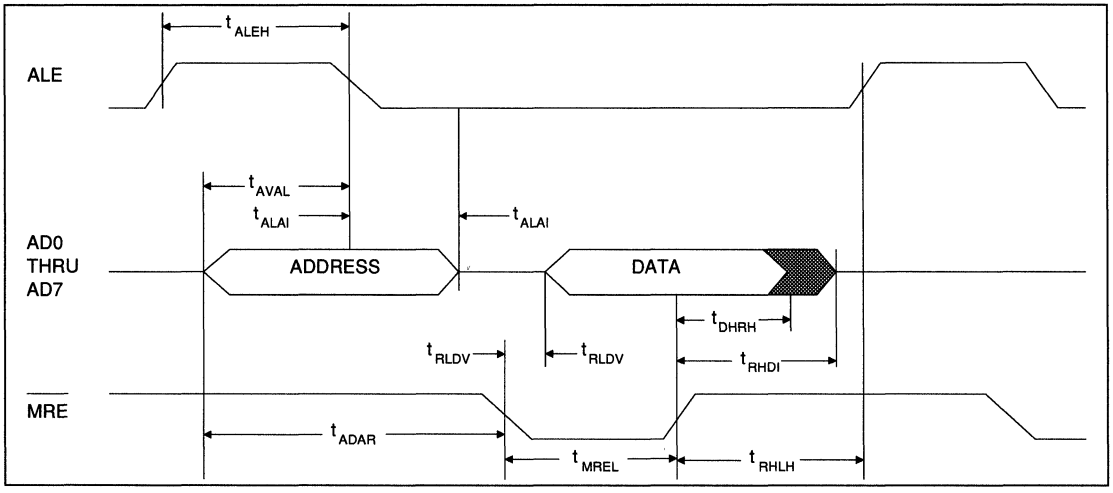


FIGURE 21. MICROPROCESSOR READ TIMING (INTEL BUS)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{AVAL}	Address Setup to ALE Low	15		ns
t_{ALAI}	Address Hold from ALE Low	5		ns
t_{ALEH}	ALE High Pulse Width	30		ns
t_{RLDV}	Data Valid from $\overline{MRE}$ Low		100	ns
t_{DHRH}	Data Hold from $\overline{MRE}$ High	10		ns
t_{RHDI}	Data Tri-state from $\overline{MRE}$ High		50	ns
t_{MREL}	$\overline{MRE}$ Low Pulse Width	100		ns
t_{ADAR}	Address Valid to $\overline{MRE}$ Low	55		ns
t_{RHLH}	$\overline{MRE}$ High to ALE High	10		ns

TABLE 27. MICROPROCESSOR READ TIMING (INTEL BUS)

5.3.16 MICROPROCESSOR READ TIMING (MOTOROLA BUS)

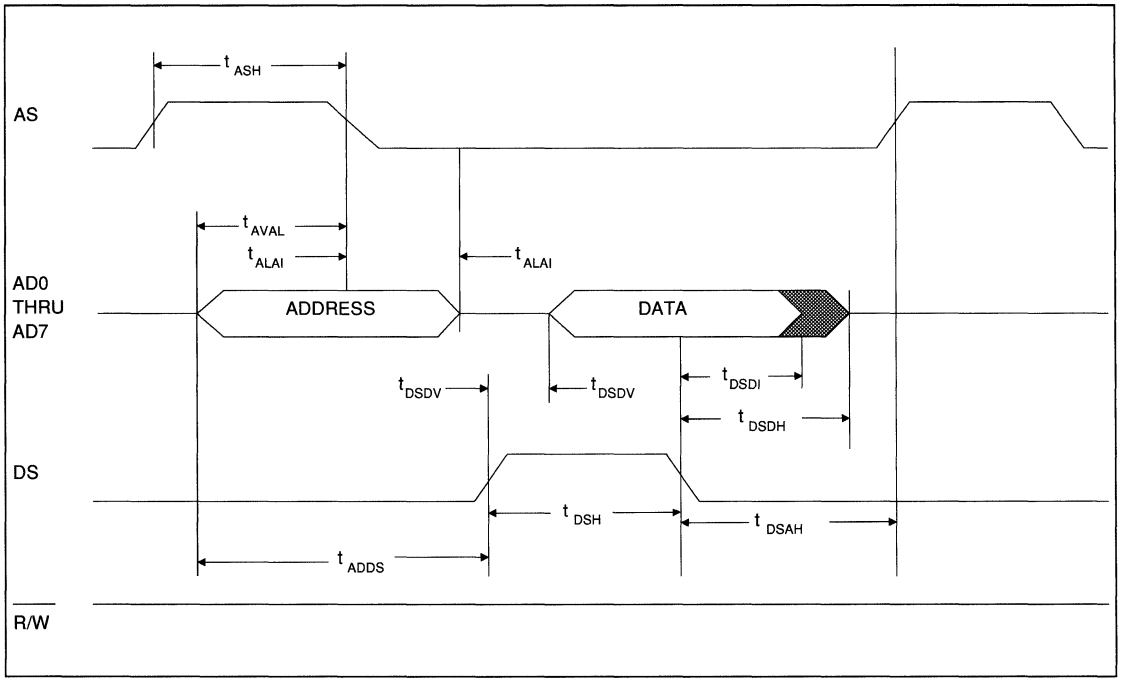


FIGURE 22. MICROPROCESSOR READ TIMING (MOTOROLA BUS)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{AVAL}	Address Setup to AS Low	15		ns
t_{ALAI}	Address Hold from AS Low	5		ns
t_{ASH}	AS High Pulse Width	30		ns
t_{DSDV}	Data Valid from DS High		100	ns
t_{DSDI}	Data Tri-state from DS Low		50	ns
t_{DSH}	DS High pulse Width during Read	100		ns
t_{ADDS}	Address Valid to DS High	55		ns
t_{DSAH}	DS Low to AS High	10		ns

TABLE 28. MICROPROCESSOR READ TIMING (MOTOROLA BUS)

5.3.17 WRITE DATA TIMING (MFM/RLL MODE; WC 5 to 15 MHz)

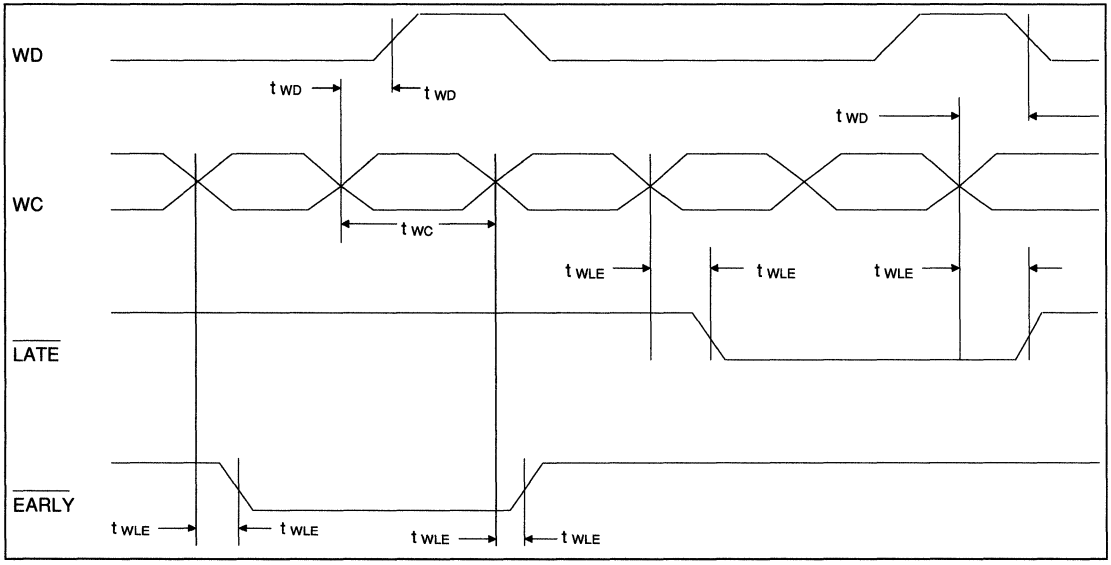


FIGURE 23. WRITE DATA TIMING (MFM/RLL MODE)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS
t_{WC}	WC Pulse Width	28 45	500 500	ns
t_{WLE}	Early/Late Propagation	3 3	15 25	ns
t_{WD}	WD Propagation Delay	3 3	15 25	ns
t_{WCF}	WC Frequency	1 1	15 10	MHz

TABLE 29. WRITE DATA TIMING (MFM/RLL MODE; WC 5 TO 15 MHZ)

5.3.18 WRITE DATA TIMING (NRZ MODE; WC 5 to 15 MHz)

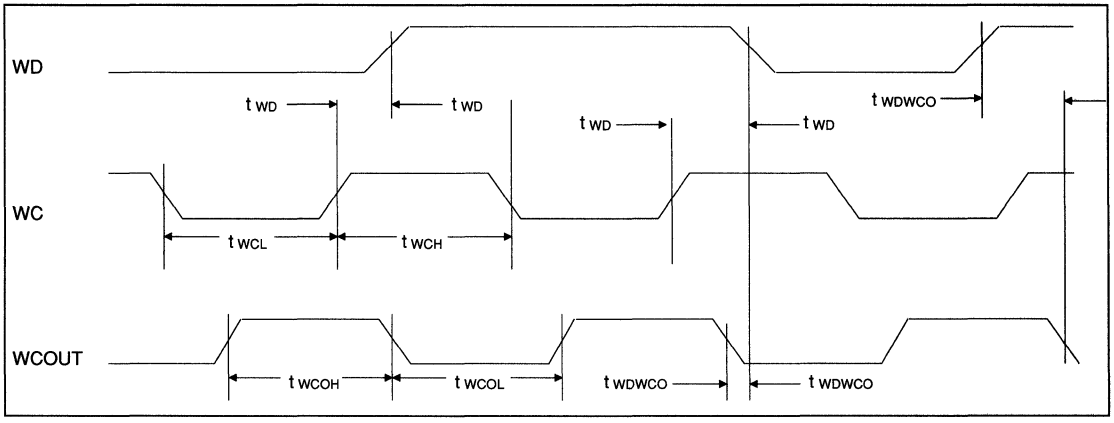


FIGURE 24. WRITE DATA TIMING (NRZ MODE)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS
t_{WCL}	WC Pulse Width Low	20 27	500 500	ns
t_{WCH}	WC Pulse Width High	20 27	500 500	ns
t_{WLE}	Early/Late Propagation	3 3	15 25	ns
t_{WD}	WD Propagation Delay	3 3	15 25	ns
t_{WCF}	WC Frequency	1 1	22 16.5	MHz
t_{WCOL}	WCOUT Pulse Width Low	t_{WCH} - 5 t_{WCH} - 9		ns
t_{WCOL}	WCOUT Pulse Width Low		t_{WCH} + 5 t_{WCH} + 9	ns
t_{WCOH}	WCOUT Pulse Width High	t_{WCH} - 5 t_{WCH} - 9		ns
t_{WCOH}	WCOUT Pulse Width High		t_{WCH} + 5 t_{WCH} + 9	ns
t_{WDWCO}	WD Prop Delay from WCOUT	-5 -8	+5 +8	ns

TABLE 30. WRITE DATA TIMING (NRZ MODE; WC 5 TO 15 MHZ)

5.3.19 READ DATA TIMING (MFM/RLL MODE; RC/WC 5 to 15 MHz)

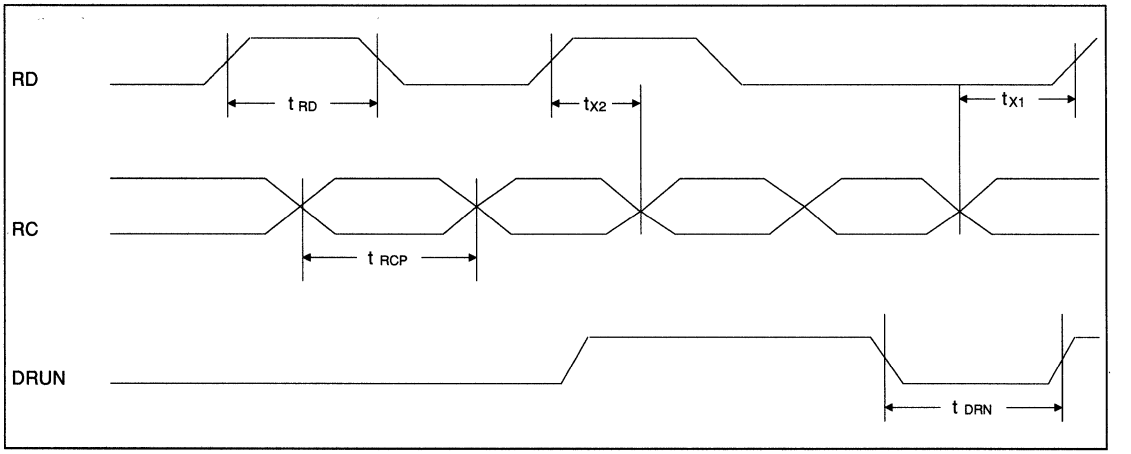


FIGURE 25. READ DATA TIMING (MFM/RLL)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS
t_{RCP}	RC Pulse Width	27 45	500 500	ns
t_{X1}	RC Transition to Next Leading RD	5 10		ns
t_{X2}	Leading RD to Next RC Transition	10 20		ns
t_{RD}	Read Data Pulse Width	20 30	t_{RCP} t_{RCP}	ns
t_{DRN}	DRUN Low Pulse Width	25 25		ns
t_{RCF}	RC Frequency	1 1	15 10	MHz

TABLE 31. READ DATA TIMING (MFM/RLL; RW/WC 5 TO 15 MHZ)

5.3.20 READ DATA TIMING (NRZ MODE; WC 5 to 20 MHz)

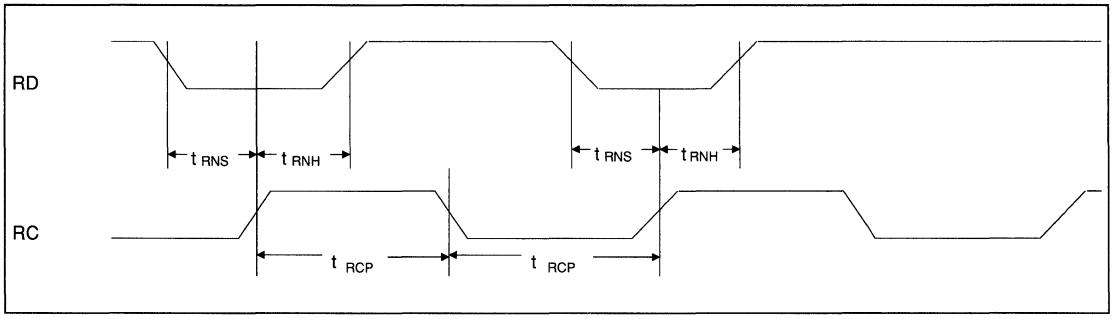


FIGURE 26. READ DATA TIMING (NRZ MODE)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS
t_{RCP}	RC Pulse Width	20 27	500 500	ns
t_{RNS}	RD Setup to RC High	7 10		ns
t_{RNH}	RD Hold from RC High	7 10		ns
t_{RCF}	RC Frequency	1 1	22 16.5	MHz

TABLE 32. READ DATA TIMING (NRZ MODE; WC 5 TO 20 MHZ)

5.3.21 MISCELLANEOUS TIMING

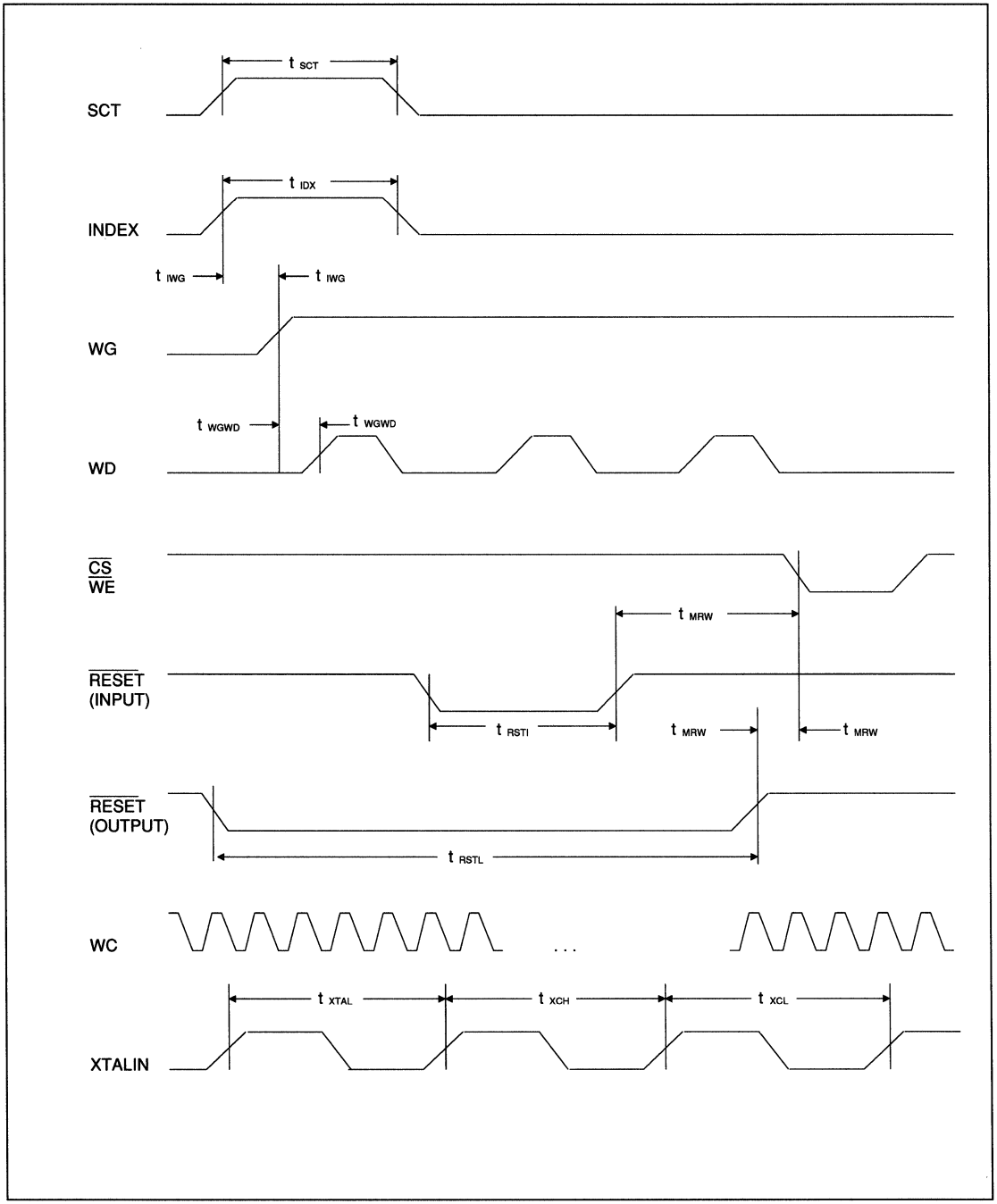


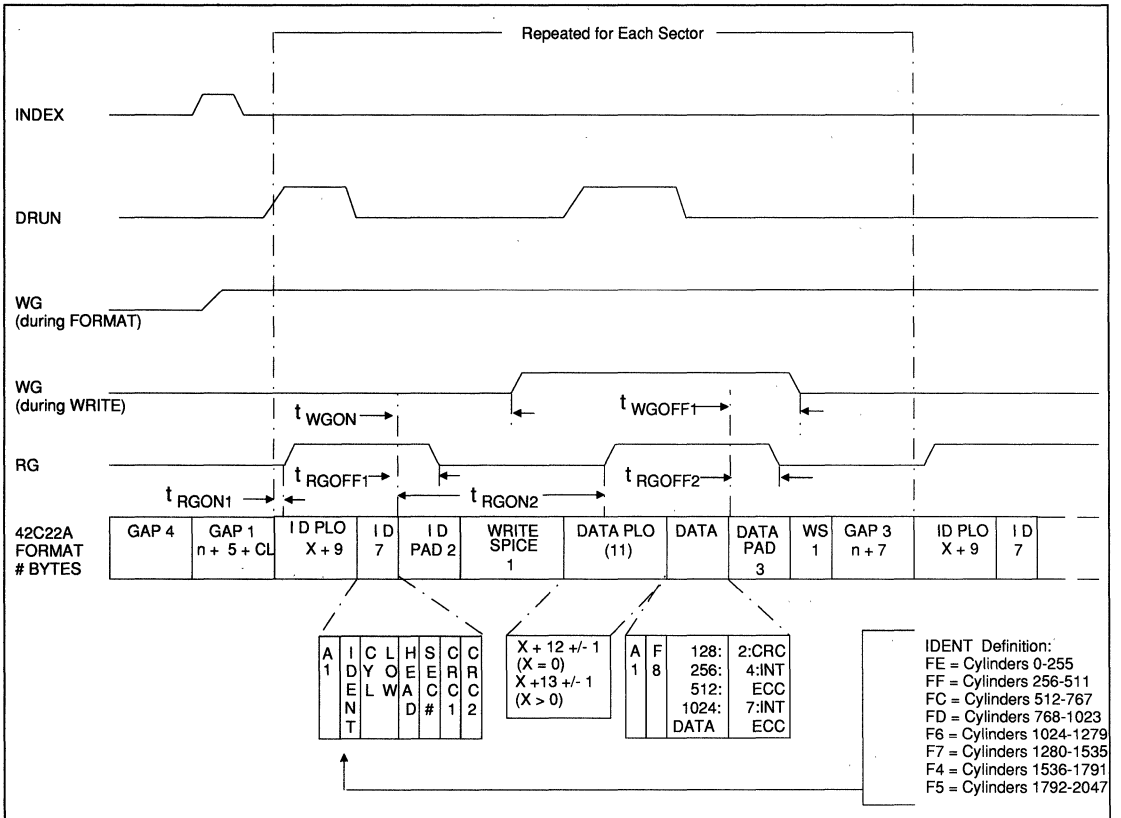
FIGURE 27. MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{IDX}	Index Pulse Width	100		ns	
t_{SCT}	SCT Pulse Width	100		ns	
t_{IWG}	Index to write gate	0	4	WC periods	Gap data=33 in RLL mode. Any gap data in MFM and NRZ.
t_{WGWD}	Write gate to write data	0	4	WC periods	
t_{RSTI}	$\overline{\text{RESET}}$ in pulse width low	24		WC periods	
t_{MRW}	$\overline{\text{MR}}$ Trailing to Host Register Write	2.4		µs	
F_{RCWC}	Difference of RC Frequency from WC Frequency	-15%	+15%		
t_{RSTL}	$\overline{\text{RESET}}$ Out Low Pulse Width during Power-up	51.2		ms	XTAL=10 MHz
t_{RSTL}	$\overline{\text{RESET}}$ Out Low Pulse Width during Power-up	41.3		ms	XTAL=12.5 MHz
t_{RSTL}	$\overline{\text{RESET}}$ Out Low Pulse Width during Power-up	25.6		ms	XTAL=20 MHz
t_{XTAL}	Clock Period	50 70	125	ns	
t_{XCH}	Clock High Time	25 30		ns	
t_{XCL}	Clock Low Time	25 30		ns	

TABLE 33. MISCELLANEOUS TIMING

NOTE

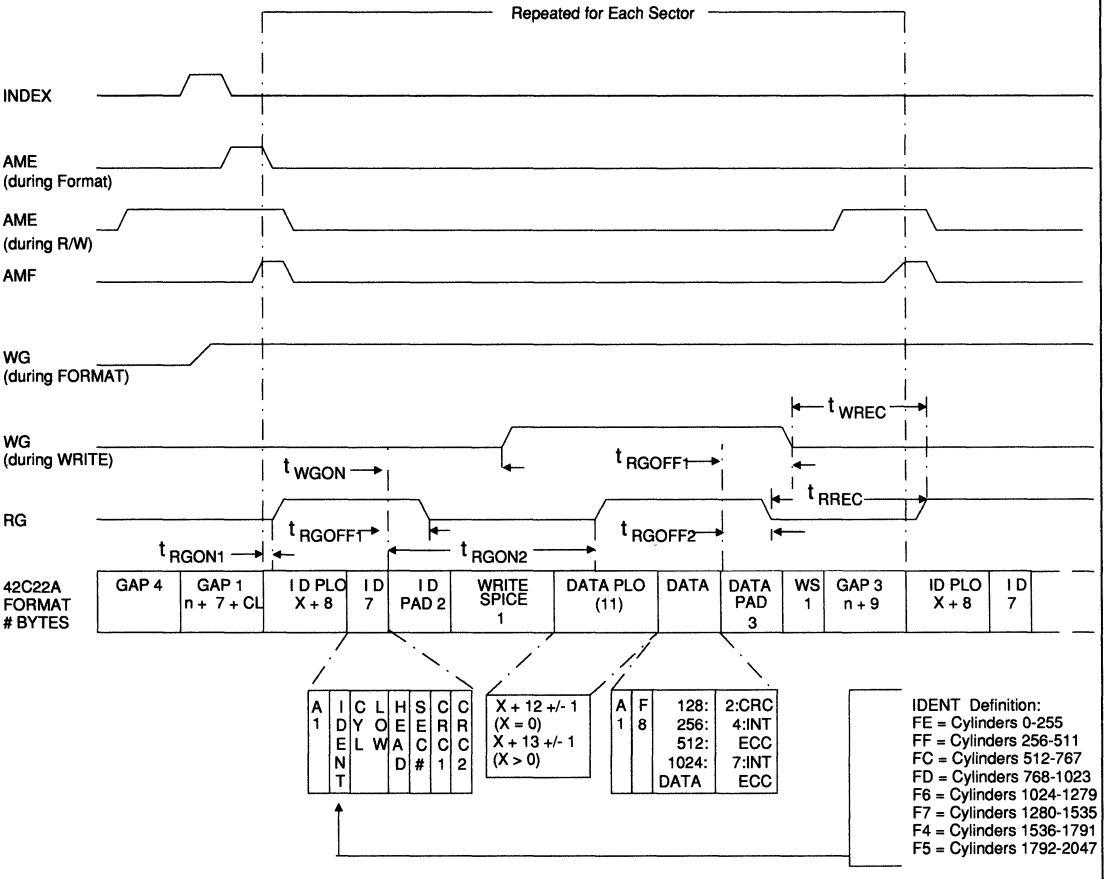
t_{XTAL}, t_{XCH}, and t_{XCL} timings at 2.5 V levels.



NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = 19 ± 1 bit times with respect to DRUN.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.

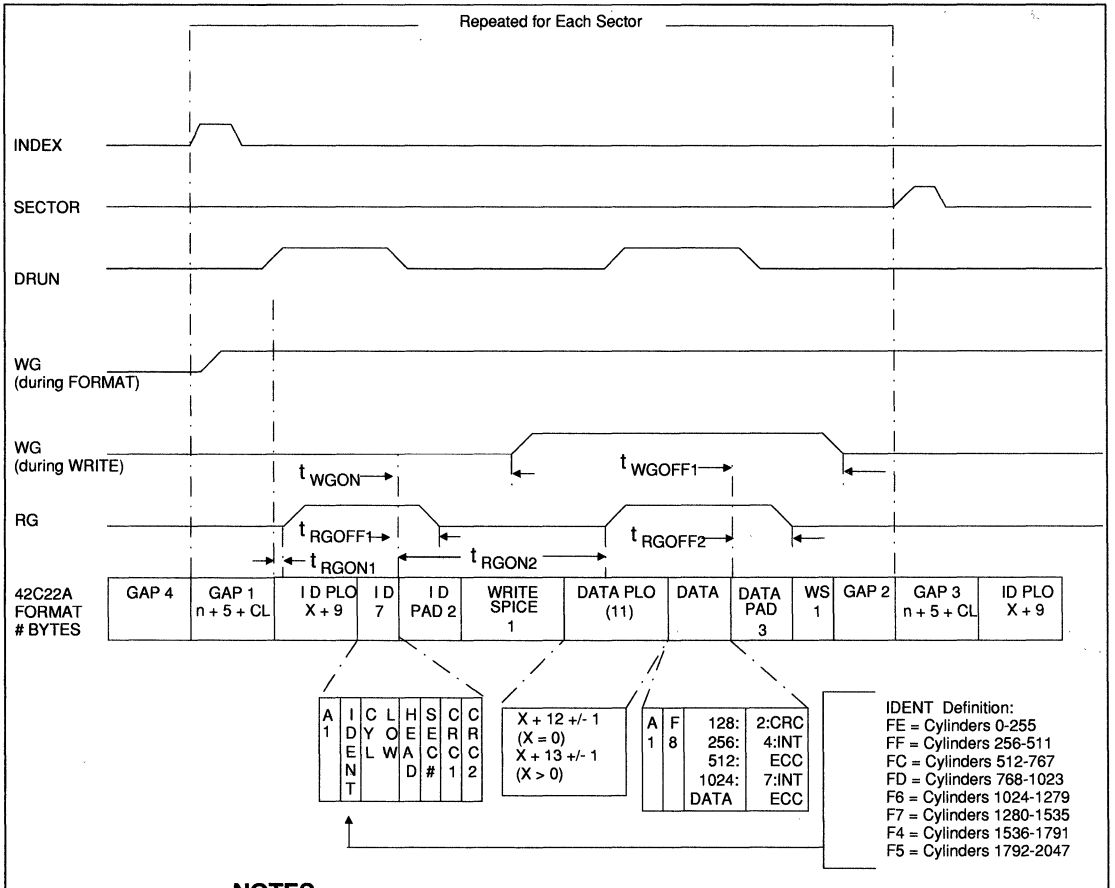
FIGURE 28. SOFT SECTOR MFM/RLL TRACK FORMAT



NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to NRZRD in.
5. t_{WGOFF1} = 28 bit times with respect to NRZWD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to NRZRD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to NRZRD in.
8. t_{RGON1} = 3 ± 1 bit times with respect to AMF.
9. t_{RGON2} = 35 + 1 bit times with respect to NRZRD in.
10. t_{WREC} = 21 to 35 bytes minimum. t_{RREC} = 23 bytes minimum.

FIGURE 29. SOFT SECTOR NRZ TRACK FORMAT

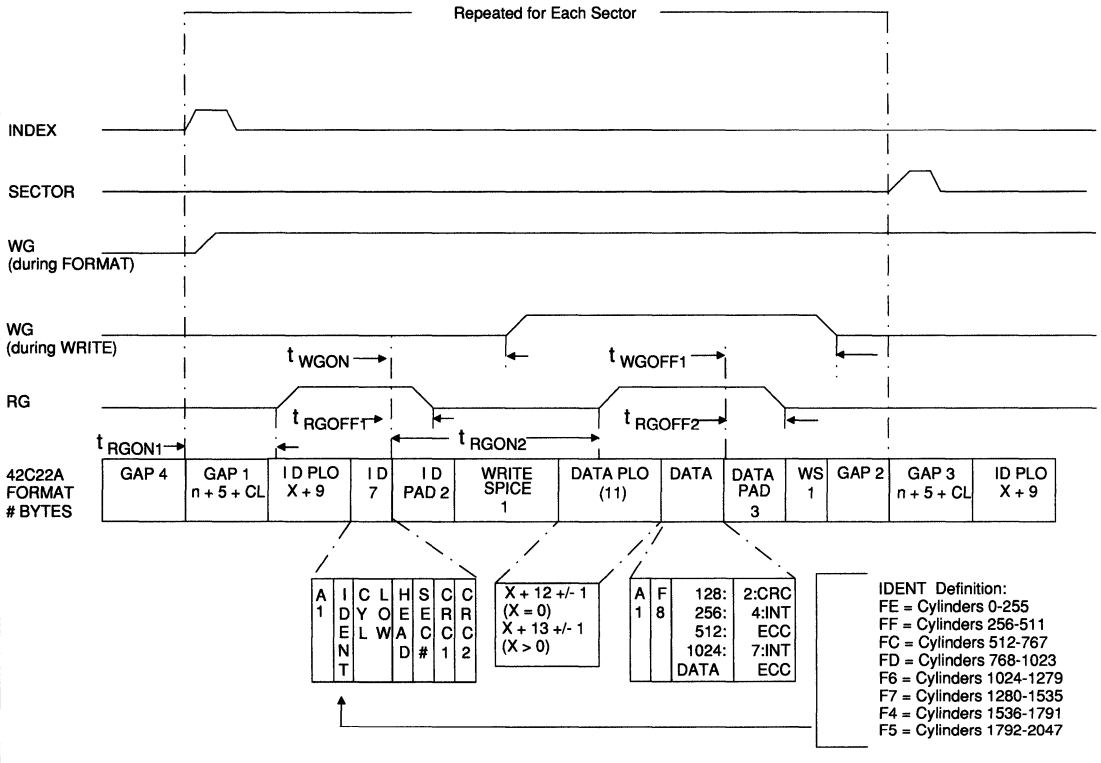


NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = 19 ± 1 bit times with respect to DRUN. SECTOR is tied to DRUNSCT during format. DRUN is tied to DRUNSCT during read and write.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.
10. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.

GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)

FIGURE 30. HARD SECTOR RLL/MFM TRACK FORMAT (WITH SOFT SECTOR READ/WRITE)



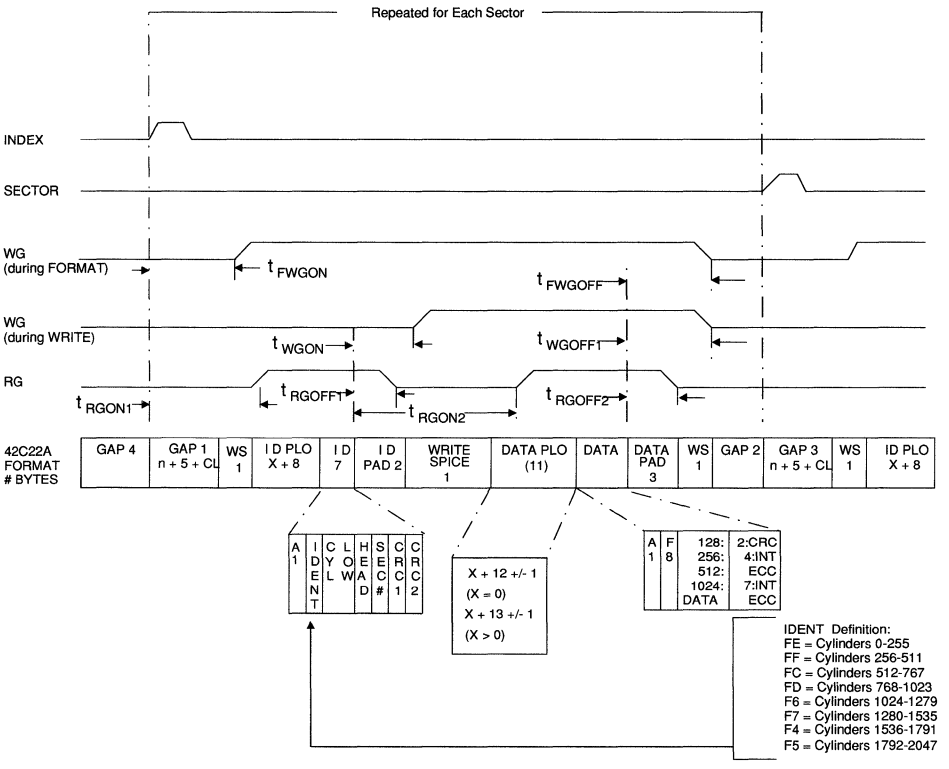
32

NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = z + CL byte times with respect to INDEX/SECTOR (SCT). SECTOR is tied to DRUNSCT always. z = contents of internal GAP register.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.
10. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.

GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)

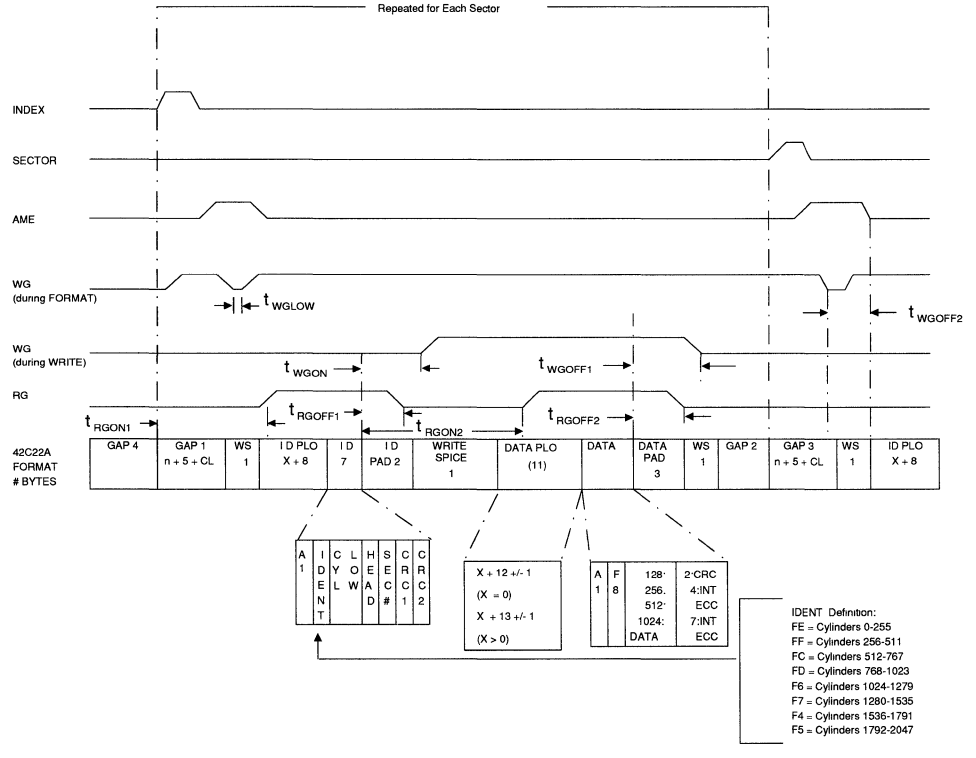
FIGURE 31. HARD SECTOR RLL/MFM TRACK FORMAT (WITH HARD SECTOR READ/WRITE AND CONTINUOUS WG OPTION)



NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = z + CL byte times with respect to INDEX/SECTOR (SCT). SECTOR is tied to DRUNSCT always. z = contents of internal GAP register.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.
10. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.
GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)
11. t_{FWGON} = n + 5 + CL byte times with respect to INDEX/SECTOR. t_{WGOFF} = 20 bit times with respect to WD out.

FIGURE 32. HARD SECTOR RLL/MFM TRACK FORMAT (WITH HARD SECTOR READ/WRITE AND WG PULSE OPTION)



NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0.
4. t_{WGON} = 17 ± 1 bit times with respect to NRZRD in.
5. t_{WGOFF1} = 28 bit times with respect to NRZWD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to NRZRD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to NRZRD in.
8. t_{RGON1} = z + CL byte times with respect to INDEX/SECTOR (SCT). z = contents of internal GAP register.
9. t_{RGON2} = 35 + 1 bit times with respect to NRZRD in.
10. t_{WGLOW} = 2 bit times. t_{WGOFF2} = 8 bit times. Both timings with respect to NRZWD out.
11. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.
GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)

FIGURE 33. HARD SECTOR NRZ TRACK FORMAT

5.4 PIN DIAGRAMS / SPECIFICATIONS

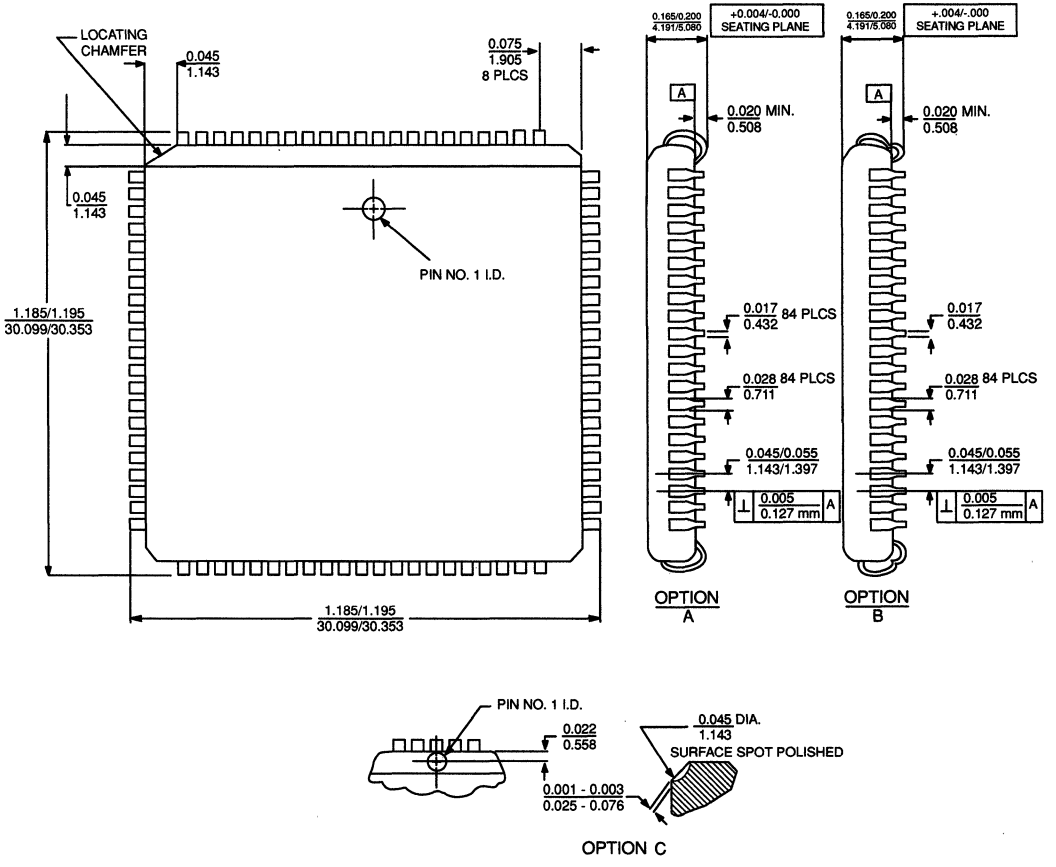


FIGURE 34. 84-LEAD PLCC

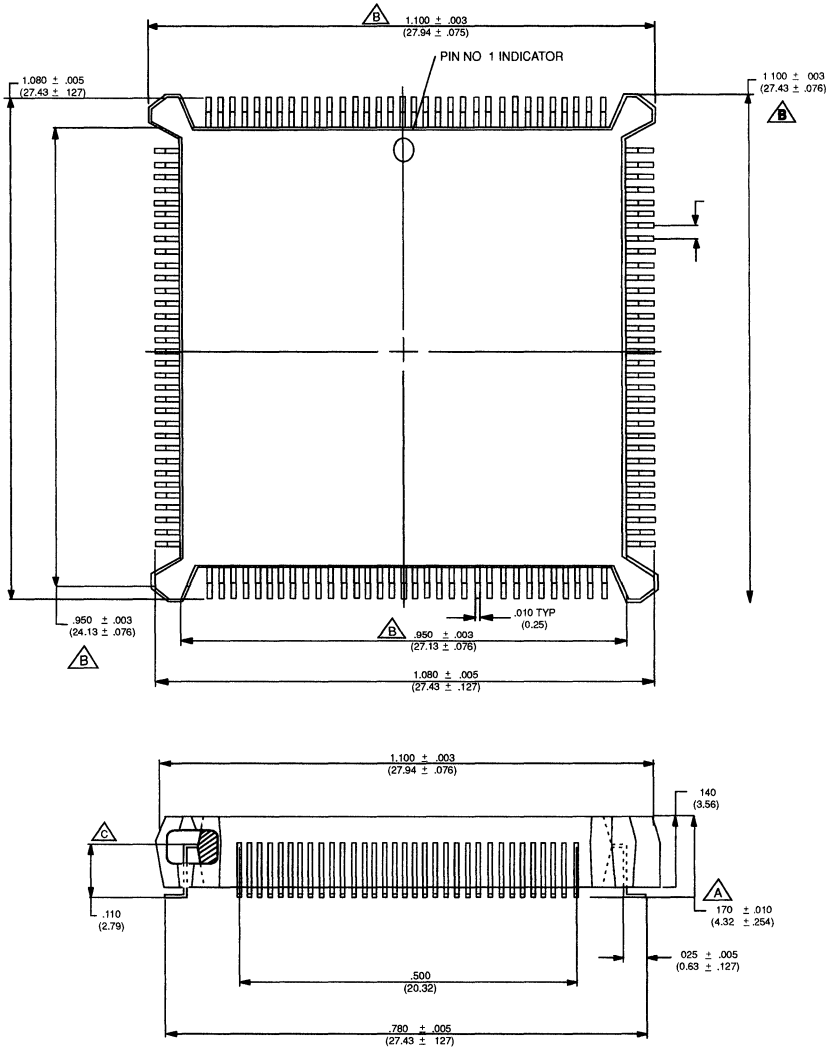
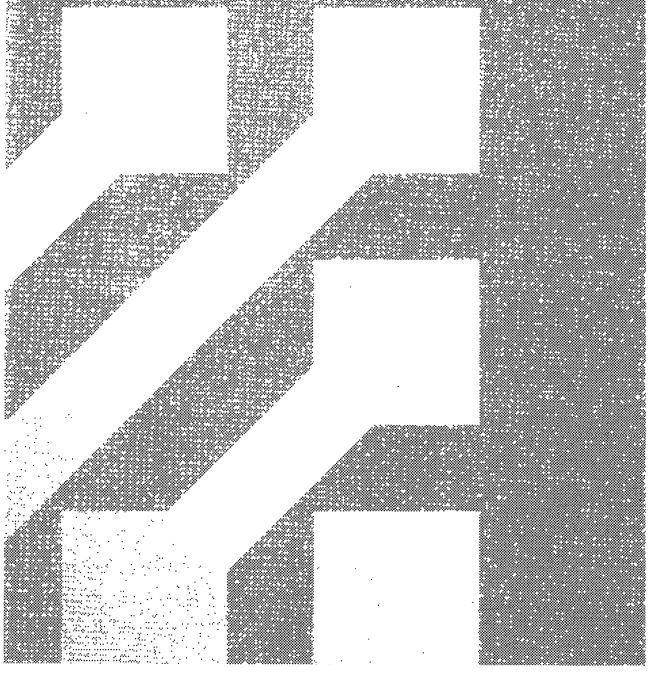


FIGURE 35. 84-LEAD PQFP

WD42C22C

Winchester Disk Subsystem

Controller Device



WESTERN DIGITAL

TABLE OF CONTENTS

Section Title **Page**

Section **Title** **Page**

33

Section Title **Page**

Section Title **Page**

Section Title **Page**

Section **Title** **Page**

33

Section **Title** **Page**

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

Western Digital's WD42C22C integrates a high performance, low cost Winchester formatter/controller, host interface, a buffer manager, and CRC/ECC generator/checker in a single 84-pin LSI device. Operating from a single +5V power supply, the WD42C22C is implemented in a low power CMOS design and is available in an 84-pin PLCC or PQFP (Figure 1). Figure 2 is a block diagram of the WD42C22C.

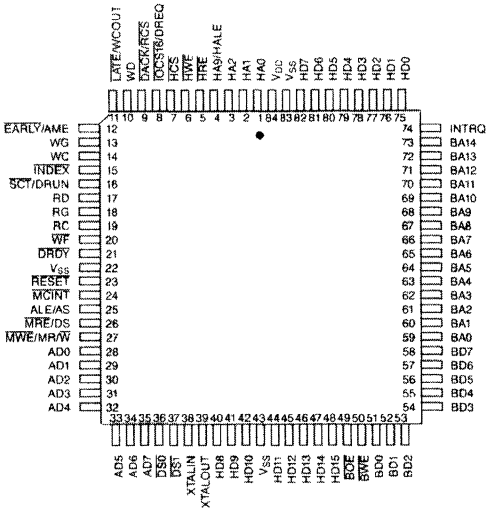


FIGURE 1. PIN DESIGNATION

1.1 FEATURES

- Enhanced host interface
  - IBM Personal Computer AT and XT port compatible
  - Supports AT speeds up to 16 MHz, 1 wait state I/O and 0 wait state memory using 120 ns static RAM (SRAM)
  - Supports AT speeds up to 16 MHz, 1 wait state I/O and 0 wait state memory using 100 ns SRAM
  - Selectable DMA or programmed I/O data transfers in all host interface modes
  - Host port slave mode compatible with ALE based peripherals such as the WD33C93 SBIC
  - Host transfer rates up to 4 Mwords/sec for AT, 4 MB/sec for XT, 10 MB/sec for SCSI
  - Internal 12 mA high current drivers for direct connection to the XT or AT system bus
- Advanced buffer manager
  - Supports 1:1 interleave **without** resorting to wait states
  - Direct interface for up to 32 KB of static RAM
  - Sustained RAM bandwidth up to 10 MB/sec
  - Pipelined host and disk address counters
  - Operates as either ring or scatter-gather buffer
  - Allows full track buffering and facilitates look ahead cacheing algorithms
  - Adaptable disk controller
  - Software selectable MFM, RLL 2,7, or NRZ disk interface
  - Software selectable 56 bit ECC, 32 bit ECC, or 16 bit CRC
  - Software selectable 5, 11, or 22 bit error correction span
  - Software selectable default sector lengths of 128, 256, 512, and 1024 bytes
  - User programmable sector size up to 2048 bytes
  - Software selectable 3 bit or 4 bit head number field
  - Reads and writes at 1:1 Interleave regardless of the formatted interleave
  - 15 Mbs data transfer rate for MFM and RLL
  - 24 Mbs data transfer rate for NRZ
  - Supports hard or soft sectored formats
  - Supports "zero latency" read operations
  - Internal defect management of sector and track level alternates
  - Able to read ESDI defect list format
  - Supports sector servo schemes by disabling WRITE GATE over servo when formatting
  - Internal 48 mA drivers and Schmitt trigger input receivers for direct connection to the drive control cable
- Integrated support features
  - Programmable master/slave mode allows two Integrated Drive Electronics (IDE) disks on one connector
  - Supports both Intel-type(80xx) and Motorola-type(68xx) microcontrollers

33

Internal power-qualified reset to detect low V_{DD}

- Low power sleep mode
- Available in 84-pin PLCC or 84-pin PQFP

1.2 DESCRIPTION

1.2.1 ENHANCED HOST INTERFACE

The WD42C22C host interface port directly connects to the host system bus via internal 12 mA drivers. When operating in either AT or XT mode, all host control, data, and task file address lines directly connect to the WD42C22C. Mapping the device to the desired host system I/O addresses requires external address decode logic. Integrated I/O port compatible AT and XT task file registers assure system compatibility.

To satisfy requirements for faster system bus rates and data transfers, the WD42C22C can operate in 12 MHz or 16 MHz, 1 wait state I/O channels (0 wait state memory) of 286 or 386 microprocessors. DMA or PIO data operations transfer at a rate of 4 Mwords/sec (AT mode) or 4 MB/sec (XT mode). In addition to traditional single mode DMA, burst mode DMA transfers are also available.

An alternative host mode, slave mode, allows communication between the microcontroller and a peripheral device through the host interface. The slave device transfers data to the buffer RAM by using a slave DMA scheme such as the WD-BUS mode in the WD33C93 SCSI bus interface controller (SBIC).

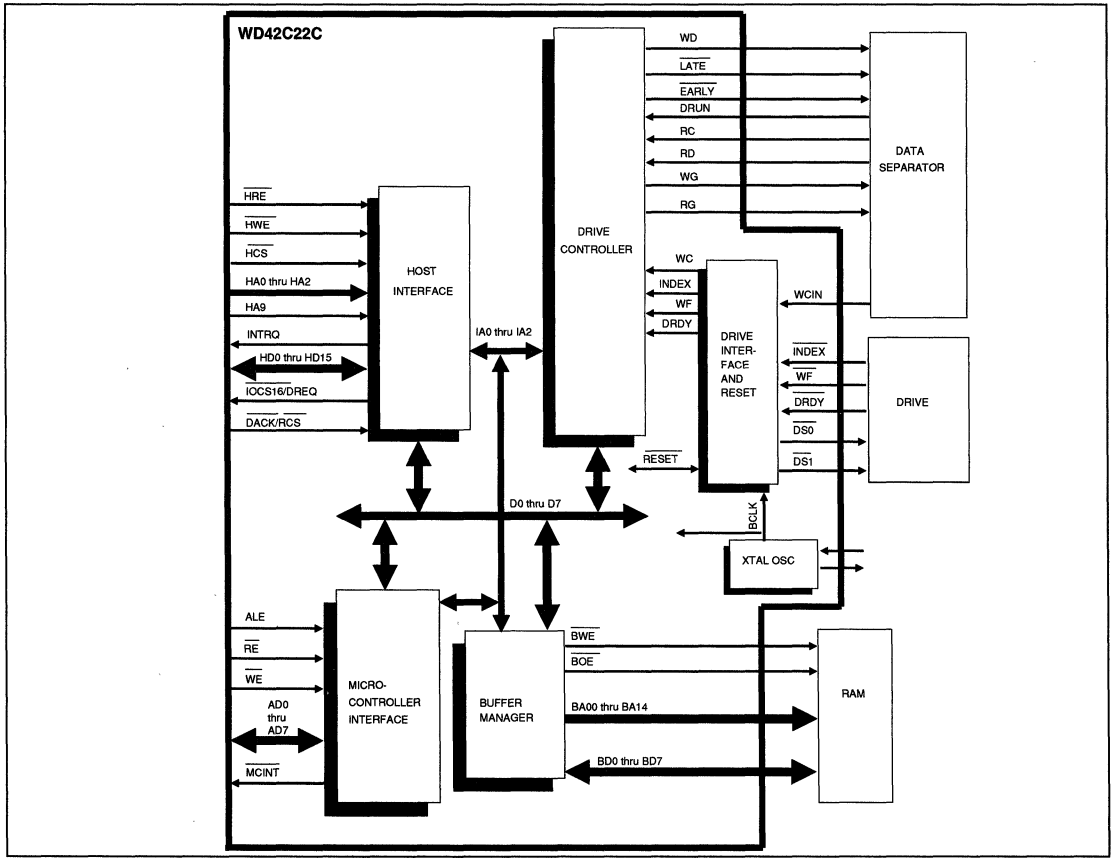


FIGURE 2. WD42C22C BLOCK DIAGRAM

1.2.2 ADVANCED BUFFER MANAGEMENT

The WD42C22C contains an advanced buffer manager satisfying the interface requirements between a byte or word wide host interface bus and a high speed serial disk interface. Optimized for the block oriented data structures of a disk controller, the WD42C22C can manage multiple sector buffers up to 32 KB. Each sector buffer can be any size to 2055 bytes. Pipelined host and disk address counters enable sustained, simultaneous transfers on each port. Sufficient RAM buffer bandwidth is available to support 1:1 interleaved 20 Mb/sec disk transfers while simultaneously performing 16-bit host transfers at a rate in excess of 3 Mwords/sec. Achieving maximum RAM bandwidth requires using 70 nsec static RAM.

The pipelined structure of the buffer manager controls the buffer RAM in either a simple ring structure or a more advanced scatter-gather structure.

1.2.3 ADAPTABLE DISK CONTROLLER

The WD42C22C's versatile design makes the device adaptable for a wide variety of disk interface operations. A designer can select from three data formats, MFM, RLL 2,7, or NRZ. Disk data rates range up to 15 Mbits/sec with MFM and RLL 2,7 encoding, while NRZ data rates range up to 24 Mbits/sec. To support varied data format requirements, the WD42C22C operates in hard or soft sectored mode with programmable sector sizes to 2048 bytes and programmable ID PLO, data PLO, and GAP lengths.

Software selectable retry algorithms and 32 or 56-bit ECC polynomials enhance data integrity. Data integrity can further be ensured through the use of the device's built-in advanced defect management. The WD42C22C can be programmed to automatically detect the presence of a previously assigned defective sector and identify the location of the alternate sector. This allows access to alternate sectors without the typical additional rotational latency associated with defect handling.

With the pipelined architecture of the buffer manager, the designer can program the disk controller to execute "zero-latency" multiple sector read operations. In this mode of operation, the WD42C22C immediately commences data transfer to the RAM buffer upon encountering the first sector on the desired track. All subsequent sectors transfer to the buffer within a single rotational period. Host transfers begin upon location of the first requested sector within the buffer. Simultaneous host and disk transfers continue until all sectors are read from the drive. Zero-latency operation makes available an entire track of data to the host within one rotational period from the time the host requested the data. This differs from traditional implementations which read the entire track within one rotational period **AFTER** the first requested sector has been located. Zero latency read operations eliminate the typical one-half rotational period average latency required to locate the first sector in full track data transfers

The WD42C22C includes an internal power qualified reset circuit for power up and power down conditions. This circuit eliminates the need for costly external circuitry that traditionally performed this function.

The WD42C22C features a multiplexed address/data bus on the microcontroller interface port and supports both Intel (80XX) and Motorola (68XX) type microcontrollers. An internal circuit automatically determines the connected microcontroller and configures the ports for direct interfacing.

33

Internal 48 mA drivers and Schmitt triggers input receivers provide direct connection to the drive control cable. Programmable input polarities assist in integrated drive electronics (IDE) designs.

1.2.4 FLEXIBILITY OF APPLICATION

As a result of its level of integration, a designer can create a wide variety of products. In addition to traditional stand alone Winchester controller boards, the WD42C22C is ideal for multi-function boards, direct system motherboards, and IDE applications. Special design considerations within the WD42C22C facilitate these applications.

1.2.5 TYPICAL APPLICATION

With an external microcontroller, buffer RAM, and a data separator such as the WD10C22B, the WD42C22C forms the basis of a Winchester disk controller product. For AT and XT applications, direct interfacing is available to the system bus. In

these applications, the WD42C22C requires external address decoding to select the primary and secondary I/O address range of the WD42C22C. Other bus interfaces are supported via auxiliary bus controllers such as the WD33C93A SCSI Bus Interface Controller.

For ST506 (MFM) and ST412HP (RLL) applications, the WD42C22C directly connects to the WD10C22 data separator. (Like the WD42C22C, the WD10C22B supports both MFM and RLL encoding methods.) An external microcontroller implements interface specific control lines, e.g. the ST506's $\overline{\text{STEP}}$ and $\overline{\text{DIRECTION}}$ signals. For ESDI applications, the WD42C22C operates in NRZ mode.

1.2.6 PIN DESCRIPTIONS

This section lists the pin number, signal name, and function for all the WD42C22C's pins. The pin descriptions are arranged by functions. Table 1 describes the pin designations for the host interface. Table 2 describes the pin designations for the local microcontroller interface. Table 3 describes the pin designations for the buffer interface. Table 4 describes the pin designations for the drive interface.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	HA0	HOST ADDRESS 0	I	Schmitt-triggered input. These four inputs are used to address the internal registers. Internal decoding of these address signals is a function of the AT/XT and HSMB mode bits. Port compatibility is maintained for both the AT and XT. In slave host mode HALE is used by the peripheral device to latch the address from HD0 through HD7.
2	HA1	HOST ADDRESS 1	I	
3	HA2	HOST ADDRESS 2	I	
4	HA9/ HALE	HOST ADDRESS 9/ HOST ALE	I/O	
5	$\overline{\text{HRE}}$	HOST READ ENABLE	I/O	Schmitt-triggered input. $\overline{\text{HRE}}$ is asserted by the AT or XT with HCS to read an internal register or the FIFO. In slave mode, $\overline{\text{HRE}}$ is asserted when $\overline{\text{MRE}}$ is asserted. It can also be asserted by the slave peripheral in DMA mode.
6	$\overline{\text{HWE}}$	HOST WRITE ENABLE	I/O	Schmitt-triggered input. $\overline{\text{HWE}}$ is asserted by the AT or XT with HCS to write an internal register or the FIFO. In slave mode, $\overline{\text{HRE}}$ is asserted when $\overline{\text{MRE}}$ is asserted. It is also asserted by the slave peripheral in DMA mode.
7	$\overline{\text{HCS}}$	HOST CHIP SELECT	I/O	Schmitt-triggered input. $\overline{\text{HCS}}$ should be decoded from the AT or XT address bus and is used to qualify $\overline{\text{HRE}}$ and $\overline{\text{HWE}}$ for host accesses. In slave mode, $\overline{\text{HCS}}$ is asserted when the local microcontroller is accessing the slave device address space.
8	$\overline{\text{IOCS16}}$/ DREQ	I/O CHIP SELECT 16/ DMA REQUEST	O	This output is programmable to function as the AT bus signal $\overline{\text{IOCS16}}$ when the PIO mode is selected or as a DMA Request signal (DREQ) in the DMA mode. This output is tri-stated at power-up and remains tri-stated until the interface mode is set by the local microcontroller. $\overline{\text{IOCS16}}$ is an open-drain ouput. DREQ is a tri-state output.
9	$\overline{\text{DACK}}$/ RCS	DMA ACKNOWLEDGE/ RAM CHIP SELECT	I	Schmitt-triggered input. $\overline{\text{DACK}}$ is asserted by the host in response to the DREQ signal assertion in order to complete the DMA handshake. $\overline{\text{RCS}}$ is used in slave mode to qualify host data transfers to/from the FIFO.

TABLE 1. HOST INTERFACE PIN DESCRIPTION

33

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
23	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	I/O	Open-drain output and Schmitt input, can be wire-ORed with an external reset. The WD42C22C resets all logic except the Task File when this input is asserted. On power-up, or when requested by the host, this output is asserted.
75 thru 82, 40, 41, 42, 44 thru 48	HD0 thru HD15	HOST DATA 0 thru HOST DATA 15	I/O	Schmitt-triggered inputs. These 16 pins are used during host 16-bit data transfers, and the lower eight bits (HD0-HD7) are used for byte-wide host data transfers as well as all command and status information transfers.
74	INTRQ	INTERRUPT REQUEST	I/O	INTRQ indicates to the AT or XT that a data blocktransfer is requested or a command has been completed. In slave host mode INTRQ is asserted by the slave peripheral device.
83	V_{SS}	GROUND		Ground.
84	V_{DD}	+5V		+5V

TABLE 1. HOST INTERFACE PIN DESCRIPTION (CONT'D)

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
22	V_{SS}	GROUND		Ground.
24	$\overline{MCINT}$	$\overline{\mu CONTROLER\ INTERRUPT}$	O	This output is used as an interrupt signal in order to alert the local microcontroller it is necessary to check command parameters or status. For the XT mode, $\overline{MCINT}$ is asserted when the controller is selected.
25	ALE/AS	ADDRESS LATCH ENABLE/ ADDRESS STROBE	I	Schmitt-triggered input. ALE is used to latch the lower eight address bits from the multiplexed address/data lines (AD7-AD0). AS is used for this function when tied to a Motorola type microcontroller.
26	$\overline{MRE}$/DS	$\overline{\mu CONTROLLER\ READ\ ENABLE}$ /DATA STROBE	I	Schmitt-triggered input. $\overline{MRE}$ is asserted by the local microcontroller to read an internal register or the buffer. DS is used in Motorola type microcontrollers to enable the data transfer.
27	$\overline{MWE}$/ MR/$\overline{W}$	$\overline{\mu CONTROLLER\ WRITE\ ENABLE}$/ uC READ/$\overline{WRITE}$	I	Schmitt-triggered input. $\overline{MWE}$ is asserted by the local microcontroller to write an internal register or the buffer. MR/$\overline{W}$ is used by Motorola type microcontrollers to set the direction of data transfers.
28 thru 35	AD0 thru AD7	ADDRESS/DATA 0 thru ADDRESS/DATA 7	I/O	Schmitt-triggered inputs. These multiplexed address/data lines are used to load the register/buffer address on the falling edge of ALE, and are used for data transfers to/from the local microcontroller.
43	V_{SS}	GROUND		Ground.

TABLE 2. LOCAL MICROCONTROLLER INTERFACE PIN DESCRIPTION

33

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
38	XTALIN	CRYSTAL INPUT	I	Crystal oscillator input. The crystal frequency is twice the buffer data rate.
39	XTALOUT	CRYSTAL OUTPUT	O	Crystal oscillator output.
49	$\overline{\text{BOE}}$	$\overline{\text{BUFFER}}$ OUTPUT ENABLE	O	$\overline{\text{BOE}}$ is asserted by the chip to read data from the external SRAM buffer.
50	$\overline{\text{BWE}}$	$\overline{\text{BUFFER}}$ WRITE ENABLE	O	$\overline{\text{BWE}}$ is asserted by the chip to write data into the external SRAM buffer.
51 thru 58	BD0 thru BD7	BUFFER DATA 0 thru BUFFER DATA 7	I/O	Schmitt-triggered. Buffer data bus, which connects directly to a static RAM.
59 thru 73	BA0 thru BA14	BUFFER ADDR 0 thru BUFFER ADDR 14	I/O	Buffer address bus, for direct connection to 32 KB of SRAM. In XT mode, also used to read jumper configuration data in Read Configuration Mode. In input mode, there is a low current internal pulldown.

TABLE 3. BUFFER INTERFACE PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
10	WD	WRITE DATA	O	WD is the MFM/NRZ write data written to the disk. It is shifted out at a rate determined by write clock. MFM write data should be synchronized by a D flip flop clocked at 10 MHz (for 5 Mbs operation).
11	LATE/ WCOUT	LATE/ WCOUT	O O	LATE is used along with EARLY in the Write Precompensation circuitry to control the delay of WD. In NRZ mode WCOUT is write clock out which can be used to qualify WD in an ESDI application.
12	AME/ EARLY	ADDRESS MARK ENABLE/EARLY	O	In NRZ mode, this output is the Address Mark Enable signal for an ESDI drive. In MFM or RLL mode, this output is EARLY. EARLY and LATE are used in the Write Precompensation circuitry to control the delay of WD.
13	WG	WRITE GATE	O	WG is asserted when valid data is to be written to the disk. It enables write current to the head and is immediately de-asserted if a WRITE FAULT (WF) is detected.
14	WC	WRITE CLOCK	I	A clock used internally to control WD. (Up to 10 MHz for ST412, up to 15 MHz for ESDI).
15	INDEX	INDEX	I	Schmitt-triggered INDEX input for direct connection to the drive control cable.
16	SCT/ DRUN	SECTOR/ DATA RUN	I	Schmitt-triggered input. In hard sector mode, SCT is used to indicate the start of a sector. In soft sector NRZ mode, SCT indicates Address Mark Found. In soft sector MFM or RLL mode, DRUN indicates a sequence of MFM or RLL '0's or a sequence of MFM '1's has been detected.
17	RD	READ DATA	I	RD is MFM or NRZ read data from the drive. Data and clocks are separated internally for MFM data.
18	RG	READ GATE	O	RG is asserted to initiate a search for an address mark. It remains asserted until the end of the ID or data field.

TABLE 4. DRIVE INTERFACE PIN DESCRIPTION

33

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
19	RC	READ CLOCK	I	RC is typically generated from an oscillator phase-locked to the read data.
20	$\overline{WF}$	$\overline{WRITE\ FAULT}$	I	Schmitt-triggered. $\overline{WRITE\ FAULT}$ input for direct connection to the drive control cable.
21	$\overline{DRDY}$	$\overline{DRIVE\ READY}$	I	Schmitt-triggered. $\overline{DRIVE\ READY}$ input for direct connection to the drive control cable.
36	$\overline{DS0}$	$\overline{DRIVE\ SELECT\ 0}$	O	High-current open-drain $\overline{DRIVE\ SELECT}$ outputs for direct connection to the drive control cable.
37	$\overline{DS1}$	$\overline{DRIVE\ SELECT\ 1}$	O	

TABLE 4. DRIVE INTERFACE PIN DESCRIPTION (CONT'D)

2.0 ARCHITECTURE

2.1 POWER-QUALIFIED RESET

This integrated function is used to reliably initialize flip-flops to a predictable state during the application of V_{DD}. It causes the $\overline{RESET}$ output signal to be asserted until VDD reaches a given threshold. It also forces a reset if the V_{DD} falls below a specified threshold.

2.2 DRIVE INTERFACE LOGIC

The drive interface contains high-current 48 mA drivers for direct connection of the drive select outputs to the drive control cable. Schmitt trigger input receivers connect the drive interface logic directly to the control cable inputs.

2.3 DRIVE CONTROLLER ORGANIZATION

The controller is composed of the following major sections:

- PLA Control
- CRC/ECC Logic
- MFM/RLL Decoding
- Address Mark Detector
- Buffer and DMA Control
- Task Register File

The controller is designed to operate with 2 clock inputs, READ CLOCK (RC) and WRITE CLOCK (WC). The PLA controller, processor interface, and buffer control sections use the write clock input. The clock inputs are used for MFM, RLL, or NRZ decoding. The clock frequency is 10 MHz for a 10 Mbs data rate.

The controller reads or writes disk data to a 15 Mbs rate for MFM and RLL and 24 Mbs for NRZ. The RLL implementation is a (2,7,2,4,3) code based on the IBM 3370 code. The only difference lies in the assignments of the code words to the 7 different data streams possible. Error propagation for a single bit error is limited to 4 bits.

When programmed in the NRZ mode, the WD42C22C qualifies NRZ disk data using the Sector / Address Mark Detect signal, and also modifies the RG and WG signals to meet ESDI specifications.

In all modes, the length of the PLO sync and gap fields are software programmable. The ID PLO sync field length, the Gap1/Gap3 length, the Gap1/Gap3 data bytes and the ID CRC pad bytes are programmable during the format command. The data PLO sync field length and the data CRC/ECC pad bytes are programmable during the Write command.

Figure 3 is a block diagram of the drive controller section of the WD42C22C.

2.4 PROGRAMMABLE LOGIC ARRAY (PLA) CONTROLLER

The Programmabla Logic Array (PLA) controller interprets commands, e.g. write, read format, etc. This circuitry's operation is synchronized with the WC input. The PLA controller is started when a command is written into the command register. It generates control signals and operates in a hand-

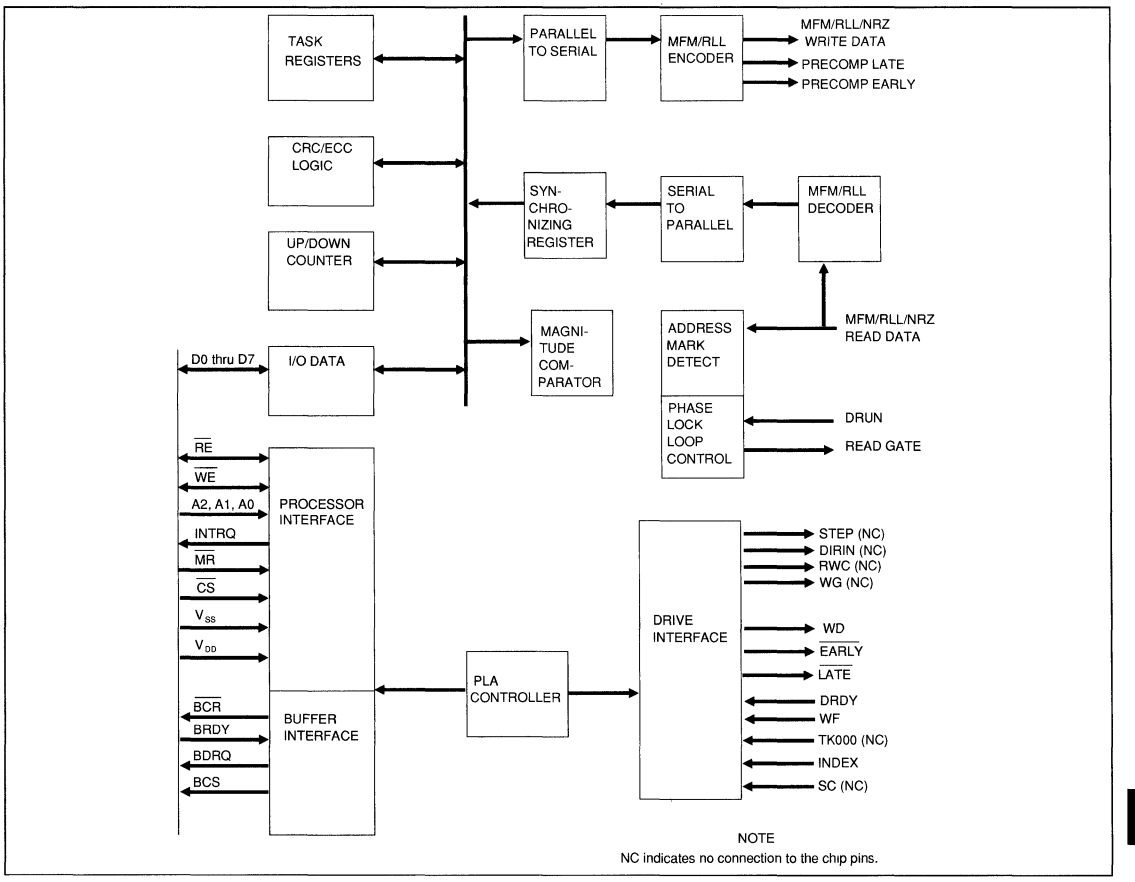


FIGURE 3. DRIVE CONTROLLER BLOCK DIAGRAM

shake mode when communicating with the MFM/RLL decoding block. The MFM/RLL decoding block uses the RC input which may be asynchronous to WC.

2.5 MAGNITUDE COMPARATOR

An 11-bit magnitude comparator calculated drive step direction and number of step pulses between present cylinder position and desired position in earlier Winchester controller versions. This comparator is **not** used in the WD42C22C. A separate high speed equivalence comparator is used to compare ID field bytes when searching for a sector ID field.

2.6 CRC/ECC GENERATOR AND CHECKER

The CRC/ECC generator computes and checks the cyclic redundancy check characters appended to the ID and data fields written on the disk. The CRC mode of operation, defined by the SDH register (bit 7 set to 0) provides a means of verifying the accuracy of the data read from the disk but does not attempt to correct it. (Bit 7 of the SDH register will not implement CRC mode for data fields when RLL mode is selected.) The CRC polynomial used is:

$$X^{16} + X^{12} + X^5 + 1$$

The CRC register is preset to all ones before computation starts.

If the CRC character being generated while reading the data does not equal the one previously written, an error exists. If there is a CRC failure in the ID field, an ID not found is indicated by setting bit 4 of the error register. If the failure is in the data field, bit 6 of the error register is set.

A 32 bit or 56 bit ECC polynomial may be selected instead of the CRC polynomial for the data field. The CRC/ECC selection is controller by bit 7 of the SDH register when the controller is in MFM or NRZ modes. CRC is selected when bit 7 of the SDH register is 0 in MFM or NRZ modes. ECC is selected when bit 7 of the SDH register is 1 in MFM or NRZ modes. Bit 2 in the set parameter command selects either the 32 bit or 56 bit polynomial. RLL mode defaults to the 56 bit polynomial. The CRC or 32 bit ECC options are **not** usable in RLL mode.

The ECC mode of operation (SDH bit 7 = 1) is only applicable to the data field. This feature built into the WD42C22C provides the user with the ability to detect and correct errors in the data field automatically.

The following is a summary of the parameters considered when ECC is used:

- 1. SDH register bit 7.
- 2. Read and write command bit 1 (L).
- 3. Compute correction command.
- 4. Set parameter command.
- 5. Error occurred, bit 0 of the status register.
- 6. On any ECC error the controller stops regardless of the T bit. (Refer to the read command description.)

The SDH register bit 7 must be equal to one to change from the CRC mode to the ECC mode, for MFM and NRZ only.

When an ECC error is detected, no attempt is made to correct it and bit 0 of the status register and bit 6 of the error register are set. The user now has two choices:

- 1. Ignore the error and make no attempt to correct it.
- 2. Use the compute correction command to determine the pattern and location of the error, and correct it within the user's program.

When implementing the compute correction command, use it before executing commands that alter the content of the ECC register. The read, write, scan, and format commands can alter the syndrome and make correction impossible. If the compution correction command determines that the error is uncorrectable, then the error bits in the status register and error register are set.

Although ECC generation starts with the first bit of the F8 byte in the data ID field, the actual ECC bytes produced for the sector are the same as if the A1 byte was included.

The 32-bit ECC polynomial is:

$$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^{6} + X^{2} + 1$$

and is the same one used in the WD1002, WD1003, and WD1006 controller boards. The 32-bit ECC polynomial has an 11 bit maximum single burst correction span. The reverse 32-bit ECC polynomial is:

$$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^{6} + X^{4} + 1$$

The non-detection probability for the 32-bit ECC polynomial is:

$$2.3\ (E\text{-}10),\ r^{\dagger} = 516 \times 8,\ b^{\dagger} = 5$$

and the miscorrection probability is:

$$1.57\ (E\text{-}5),\ r^{\dagger} = 516 \times 8,\ b^{\dagger} = 5$$

The 56-bit ECC polynomial is:

$$X^{56} + X^{52} + X^{50} + X^{43} + X^{41} + X^{34} + X^{30} + X^{26} + X^{24} + X^{8} + 1$$

The 56-bit ECC polynomial has a 22 bit maximum single burst correction span.

The reverse 56-bit ECC polynomial is:

$$X^{56} + X^{48} + X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^{6} + X^{4} + 1$$

The non-detection probability for the 56-bit ECC polynomial is:

$$1.39\ (E\text{-}17),\ r^{\dagger} = 519 \times 8,\ b^{\dagger} = 11$$

and the miscorrection probability is:

$$5.84\ (E\text{-}11),\ r^{\dagger} = 519 \times 8,\ b^{\dagger} = 11$$

The set parameter command selects the number of bits in the correction span, through the use of bit 0.

Read and write commands, with the L bit (bit 1) set to one, are referred to as read long and write long commands. With these commands, no ECC or CRC characters are generated or checked by the WD42C22C. In effect, the four or seven bytes are handled as an additional four or seven bytes of data which pass through the data buffer. With proper use of the write, read long, write long, and read commands, a diagnostic routine may be developed to test the accuracy of the error correction process.

For CRC/ECC calculations, the CRC/ECC register is initialized to all 1's. For CRC/ECC purposes only, the address mark byte has a value of "A1" and is included in the CRC/ECC calculations.

2.7 MFM/RLL ENCODING AND MFM/RLL DECODING

The MFM/RLL encoding section receives 8-bit parallel data and generates either MFM or RLL write data depending on the K option in the load parameter block command. This section operates with a write clock having a frequency of the desired bit rate. The write clock need not be synchronized to read clock (RC).

Data bytes are written to the drive most significant bit first. The MFM/RLL decoding section generates 8 bit binary data from MFM or RLL read data once an address mark has been detected. Table 5 lists the RLL coding rules followed by the controller.

NRZ Data				RLL Code Word Output	
First Bit		Last Bit		First Bit	Last Bit
1	1	X	X	1 0 0 0	X X X X
1	0	X	X	0 1 0 0	X X X X
0	1	1	X	0 0 1 0	0 0 X X
0	1	0	X	0 0 0 1	0 0 X X
0	0	0	X	1 0 0 1	0 0 X X
0	0	1	1	0 0 0 0	1 0 0 0
0	0	1	0	0 0 1 0	0 1 0 0

TABLE 5. RLL CODING RULES

When NRZ mode is selected, the MFM/RLL encode and decode logic is bypassed. NRZ read data is clocked in on the rising edge of Read Clock and NRZ write data is clocked out on the rising edge of WC.

2.8 ADDRESS MARK DETECTOR

An address mark is a unique 2 byte code placed at the beginning of each ID field or data field. A series of zero bytes always precedes each address mark. The address mark detector section begins searching for an address mark when synchronization has been lost after a series of zero bytes is detected. The detection of an address mark establishes resynchronization.

The address mark is composed of a 2 byte sequence. The first byte is used for resynchronization and the second byte specifies ID or data field. For the MFM mode, the first byte is an $A1_{16}$ byte with missing clock (data = A1, clock = 0A). The second byte is encoded with normal MFM rules. FF through FC and F7 through F4 specify the beginning of an ID field and F8 specifies the beginning of a data field.

In RLL mode, the first byte is a unique code which violates normal RLL coding rules but does not violate the 2,7 timing rule. The RLL address mark pattern is 1000 0000 1001 0000 (8090_{16}). The second byte is encoded with normal RLL rules. FF through FC and F7 through F4 specify the beginning of an ID field and F8 specifies the beginning of a data field.

In NRZ mode, an NRZ A1 byte establishes byte synchronization. When the WD42C22C is used to control an ESDI (NRZ) drive, the Sector Pulse (Address Mark Found) signal will qualify read data to prevent false address mark detection.

2.9 CONTROLLER TO DATA SEPARATOR INTERFACE

The read interface section generates READ GATE (RG) from signals sent by the PLA controller and by the DRUN input. In this system, raw read data from the drive is presented to the RD in put. RG is low when the controller is not inspecting read data. When a read command is started and a search begins for an address mark, DRUN from the data separator is examined. Since each

33

address mark should be preceded by approximately 12 bytes of zeroes, RG is activated when a sequence of zeroes is detected by DRUN and read data is examined until either an address mark is detected or a non-zero byte which is not an address mark is detected. If an address mark was detected, and it was preceded by at least 8 bytes of zeroes, read gate is held high and the ID or data field can be read.

If a non-zero non-address mark byte was detected, then RG is dropped for at least 2 byte times, allowing the phase lock loop to resynchronize with WC, before inspecting DRUN input again. If the desired ID field was read, then the sector transfer can be made. If a data field was detected or if the ID bytes did not match, or if an address mark was not preceded by eight bytes of zeroes with six coming after RG on, then RG is lowered and DRUN is inspected again for a sequence of zeroes.

Figures 4 illustrates the PLL control sequence for the ID field. Figure 5 illustrates the PLL control sequence for the data field.

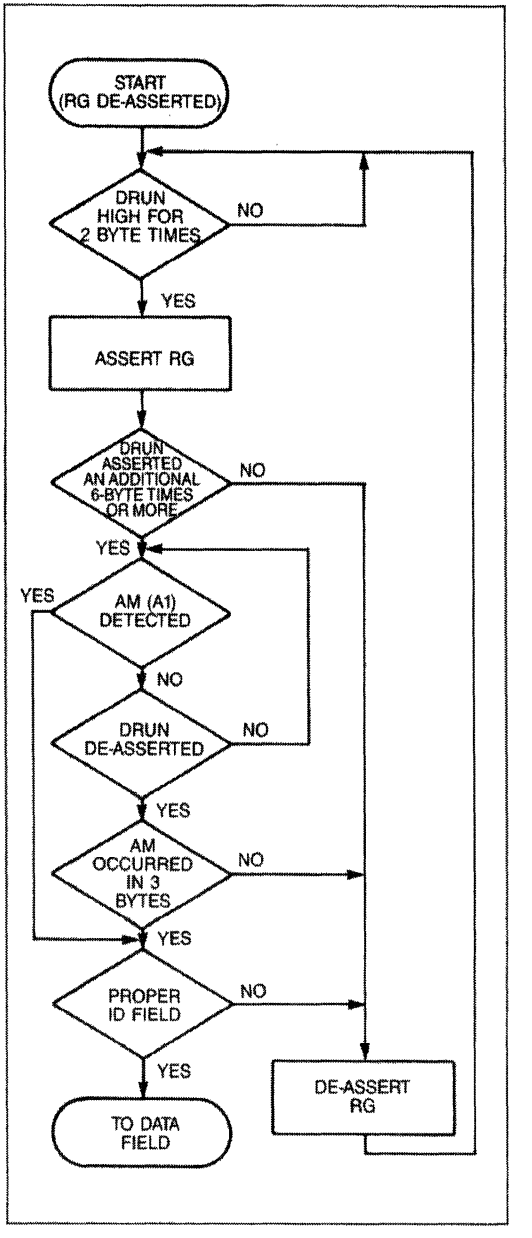


FIGURE 4. PLL CONTROL (ID FIELD)

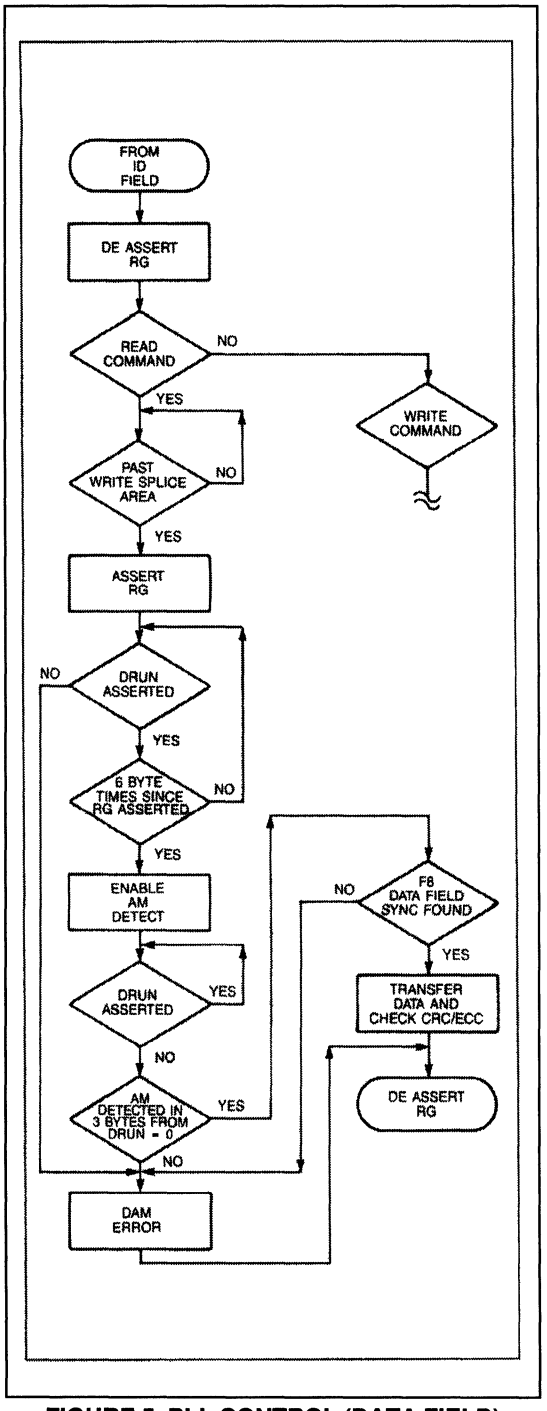


FIGURE 5. PLL CONTROL (DATA FIELD)

The write precompensation circuitry, in the controller to the drive interface, reduces the effects one bit has on another. There are two parts to write precompensation logic, reduced write current (RWC) and shifting of the bits as they are written. The RWC is **NOT** controlled by the drive controller. The local microcontroller should specify when the write current is reduced by asserting its own RWC output.

The shifting of the data bits is controlled by the $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ outputs. These two outputs should be used to delay the output as follows in Table 6:

$\overline{\text{EARLY}}$	$\overline{\text{LATE}}$	DELAY
0	1	no delay
1	1	one unit delay
1	0	two units delay

TABLE 6. EARLY AND LATE DELAYS

The $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ outputs are generated according to the rules in Tables 7 (RLL) and 8 (MFM or NRZ).

RLL Coded Data Pattern			
Preceding Bits	Comp. Bit	Following Bits	Precomp
X 1 0 0	1	0 0 0 X	EARLY
X 0 0 0	1	0 0 0 X	None
X 0 0 0	1	0 0 1 X	LATE
0 1 0 0	1	0 0 1 0	None

TABLE 7. EARLY AND LATE GENERATION (RLL MODE)

MFM Coding - NRZ Data Pattern																
Preceding Bits				Comp. Bit	Following Bits				Precomp
X	X	X	1	1	0	X	X	X	EARLY
X	X	X	0	1	1	X	X	X	LATE
X	X	0	0	0	1	X	X	X	EARLY
X	X	1	0	0	0	X	X	X	LATE

TABLE 8. EARLY AND LATE GENERATION (MFM - NRZ)

3.0 INTERFACE PORTS AND TASK FILES

3.1 HOST INTERFACE ORGANIZATION

The WD42C22C's host interface directly connects to the IBM XT or IBM AT system bus as well as the system bus of any XT or AT compatible. The WD42C22C has high current drivers which allow it to be directly connected to the system bus.

The register configuration for the host interface is dependent on the state of the AT/$\overline{XT}$ control bit in the interface control register which is written by the local microcontroller.

There is an additional slave host mode. In this mode, the microcontroller communicates to a peripheral device with up to 32 registers through the host interface. The slave device can transfer data to/from the buffer RAM by using a slave DMA scheme such as the WD-BUS mode in the SBIC.

The sequence that the microcontroller follows to transfer data between the buffer RAM and the host is defined under the buffer manager description.

3.2 XT HOST INTERFACE

To put the WD42C22C in the XT compatible interface mode the local microcontroller resets the AT/$\overline{XT}$ control bit. In this mode, $\overline{HCS}$ should be active when I/O ports 320 (hex) through 323 (hex) are addressed. (XT I/O ports 320 through 323 are primary ports. XT I/O ports 324 through 327 are secondary ports. Unless otherwise noted, information regarding the primary ports is identical to information on secondary ports.) Table 9 lists the port descriptions for this mode.

HA9	HA2	HA1	HA0	READ PORT	WRITE PORT
X	X	0	0	Read data	Write data
X	X	0	1	Hardware status	Hardware reset
X	X	1	0	Drive configuration	Drive select
X	X	1	1	NOT USED	DMA and interrupt control

TABLE 9. XT PORT DESCRIPTIONS

3.2.1 READ DATA PORT (HA1 THRU HA0 = 0, READ)

The read data port is used to send data and status to the host processor. The data read from this port comes from the buffer RAM under the control of the buffer manager.

3.2.2 WRITE DATA PORT (HA1 THRU HA0 = 0, WRITE)

The write data port is used to send commands and data from the host to the drive controller. The data is written to the buffer RAM under the control of the buffer manager.

3.2.3 HARDWARE STATUS (HA1 THRU HA0 = 1, READ)

This port contains the controller hardware status. It can be read by the host at any time. Bit 7, bit 6, bit 2, and bit 1 are written by the local microcontroller. Bit 5, bit 4, bit 3, and bit 0 are controlled by internal logic. The bits are defined as follows:

Bit							
7	6	5	4	3	2	1	0
X	X	IRQ	DRQ	XBSY	C/D	I/O	REQ

3.2.3.1 BIT 5 INTERRUPT REQUEST

This bit signifies that an interrupt is pending. IRQ reflects the state of the INTRQ output. The INTRQ pin is tri-stated and the IRQ status bit

and internal interrupt flip-flop are reset when the host disables the interrupt or when the WD42C22C is reset, either by the host or by asserting master reset.

3.2.3.2 BIT 4 DMA REQUEST

This bit signals that the WD42C22C is ready for a DMA transfer to take place. The direction of the transfer is determined by the I/O bit. This bit reflects the state of the DREQ output.

3.2.3.3 BIT 3 XT BUSY

This bit indicates that the WD42C22C is busy executing a command and is unable to accept another command. This bit is set by during a reset.

3.2.3.4 BIT 2 COMMAND / $\overline{\text{DATA}}$

This bit tells the host which type of transfer is expected at the read and write data ports. C/$\overline{\text{D}}$ set to 1 indicates that a command or status transfer is expected. C/$\overline{\text{D}}$ set to 0 indicates that a data transfer is expected.

3.2.3.5 BIT 1 INPUT / $\overline{\text{OUTPUT}}$

This bit tells the host the direction of transfer for the two data ports. I/$\overline{\text{O}}$ set to 1 indicates an input (read) by the host and I/$\overline{\text{O}}$ set to 0 indicates an output (write) by the host.

3.2.3.6 BIT 0 REQUEST

This bit is one of the handshaking signals between the host and WD42C22C. When transferring data to/from, the WD42C22C's read data and write data ports by the host, assertion of this bit informs the host that the WD42C22C is ready for the transfer.

3.2.4 CONTROLLER RESET (HA1 THRU HA0 = 1, WRITE)

When this port is written, regardless of the data written, the RESET output is asserted if enabled. If the reset has been disabled by the local microcontroller, then writing to this port asserts $\overline{\text{MCINT}}$ and the local microcontroller is responsible for resetting the logic on the drive controller board.

3.2.5 DRIVE CONFIGURATION INFORMATION (HA1 THRU HA0 = 2, READ)

This register, when read, informs the host about the configuration of the drive(s) attached. This configuration information is written by the local microcontroller.

3.2.6 CONTROLLER SELECT (HA1 THRU HA0 = 2, WRITE)

When this port is written, regardless of the data written, the $\overline{\text{MCINT}}$ output is asserted to inform the local microcontroller that the controller board has been selected.

3.2.7 DMA AND INTERRUPT MASK (HA1 THRU HA0 = 3, WRITE)

This port enables or disables the DMA and interrupt to the host. When IRQEN is set to 1, then interrupts to the host are enabled. This bit is cleared when the WD42C22C is reset. The INTRQ line is tri-stated and the host interrupt is cleared when the interrupts are disabled. When DRQEN is set to 1, then DMA requests to the host are enabled. This bit is cleared when the WD42C22C is reset.

Bit							
7	6	5	4	3	2	1	0
X	X	X	X	X	X	IRQ EN	DRQ EN

33

3.3 AT HOST INTERFACE

To put the WD42C22C in the AT compatible interface mode, the AT/$\overline{\text{XT}}$ control bit is set by the local microcontroller. The $\overline{\text{HCS}}$ chip select should be active when I/O ports $1F0_{16}$ through $1F7_{16}$ and $3F6_{16}$ and $3F7_{16}$ are addressed for primary addressing and for I/O ports 170_{16} through 177_{16} and 376_{16} and 377_{16} for secondary addressing. Only address signals HA8 through $\overline{\text{HA3}}$ and AEN need to be decoded to generate $\overline{\text{HCS}}$. Table 10 describes the ports for AT mode as follows:

ABSY	HA9	HA2	HA1	HA0	READ PORT	WRITE PORT
					AT TASK FILE COPY	
0	0	0	0	0	Read Data (16 bits)	Write Data (16 bits)
0	0	0	0	1	Host Error Register	Write Precomp Cylinder
0	0	0	1	0	Sector Count	Sector Count
0	0	0	1	1	Sector Number	Sector Number
0	0	1	0	0	Cylinder Number Low	Cylinder Number Low
0	0	1	0	1	Cylinder Number High	Cylinder Number High
0	0	1	1	0	SDH	SDH
0	0	1	1	1	Host Status Register	Host Command Register
1	0	X	X	X	Host Status Register	INVALID
					CONTROL PORTS	
X	1	1	1	0	Alternate Status Register	Fixed Disk Register
X	1	1	1	1	Digital Input Register*	NOT USED

*Bit 7 is tri-stated when the digital input register is read to accomodate the floppy disk change status.

TABLE 10. AT MODE PORT DESCRIPTIONS

When port 0 is accessed the $\overline{\text{IOCS16}}$ output is asserted when in AT programmed I/O mode. All buffer data transfers are 16 bits. The ECC byte transfers in a long mode (read or write) are 8 bit transfers. All other register transfers are 8 bits.

Registers 1 through 7 are an identical copy of the drive controller task registers 1 through 7. These registers can be read or written by the host only when the ABSY status bit is not active. Any attempt by the host to read the AT task file copy while ABSY is active results in the host status register being read. The AT task file copy registers cannot be written by the host while ABSY is active.

3.3.1 ERROR REGISTER (HA9, HA2 THRU HA0 = 01, READ)

The error register is read only and contains the specific error status pertaining to a command. The meaning of the status register bits are as follows:

Bit							
7	6	5	4	3	2	1	0
BB	CRC/ ECC	0	IDNF	0	AC	TK0	DMNF

3.3.1.1 BIT 7 BAD BLOCK

A bad block address mark has been detected when trying to read or write that sector. The data field will not be read or written.

3.3.1.2 BIT 6 CRC/ECC DATA FIELD ERROR

An uncorrectable ECC error or a CRC error was detected in the data field.

3.3.1.3 BIT 5 RESERVED

Not used, forced to zero.

3.3.1.4 BIT 4 ID NOT FOUND

Occurs when cylinder, head, sector, size parameters with a correct ID field CRC cannot be

found. For read and write sector commands, with the retry disable bit reset, this bit indicates that after 10 index pulses, an auto-scan ID and auto-seek, and 10 more index pulses, no matching ID field was found. If the retry disable bit is set, then no matching ID field was found after 2 index pulses; no auto-scan or auto-seek is performed.

3.3.1.5 BIT 3 RESERVED

Not used, forced to zero.

3.3.1.6 BIT 2 ABORTED COMMAND

Set if command was started and one of the following conditions occurred:

- 1. Drive not ready
- 2. Write fault
- 3. Illegal command code.

3.3.1.7 BIT 1 TRACK 0 ERROR

This bit, when set, indicates an error detecting Track 0 during a restore.

3.3.1.8 BIT 0 DATA ADDRESS MARK NOT FOUND

Set if the first two bytes of the data field following an ID match are not A1 F8. This condition is checked for read sector commands only.

3.3.2 WRITE PRECOMP CYLINDER REGISTER (HA9, HA2 THRU HA0 = 01, WRITE)

This register is used to control the Reduce Write Current (RWC) signal going to the drive. RWC is turned on if the present position cylinder number is greater than or equal to the 4 times the write precomp cylinder number. If the write precomp cylinder number is FF_{16}, then the RWC is never asserted.

3.3.3 SECTOR COUNT (HA9, HA2 THRU HA0 = 02, READ/WRITE)

This register is used in read sector, write sector, and format commands to implement multiple sector handling with one command. A value of 1 indicates a single sector transfer, a value of 2 indicates a 2 sector transfer, and so forth. A value of 0 indicates a 256 sector transfer. Sector count is decremented and the sector number is incremented after each sector transfer between the buffer and host or drive.

3.3.4 SECTOR NUMBER (HA9, HA2 THRU HA0 = 03, READ/WRITE)

The sector number register is used to hold the number of the desired sector for read and write commands. The sector number can range from 0 to 255.

3.3.5 CYLINDER NUMBER LOW AND HIGH REGISTERS (CYLINDER NUMBER LOW: HA9, HA2 THRU HA0 = 04, READ/WRITE. CYLINDER NUMBER HIGH: HA9, HA2 THRU HA0 = 05, READ/WRITE)

These registers specify the cylinder number for read, write, and format commands. The cylinder number may range in value from 0 to 2047. Cylinder number low register holds the 8 least significant bits of the desired cylinder number. Cylinder number high register holds the three most significant bits of the desired cylinder number in bits 0 through 2. Bits 3 through 7 are not normally used in disk controller boards. These bits are latched when writing to this register. This means that all 8 bits can be used to transfer information between the host and the local microcontroller.

33

3.3.6 SDH REGISTER (HA9, HA2 THRU HA0 = 06, READ/WRITE)

This register is used to specify the desired drive and head numbers and to specify CRC or ECC mode.

Bit							
7	6	5	4	3	2	1	0
CRC/ ECC	0	SS	Drive Number	Head Number			

3.3.6.1 BIT 7 ECC/CRC SELECT

This bit is set for data field ECC mode. It is reset for data field CRC mode.

3.3.6.2 BIT 5 SECTOR SIZE

Bit 5 (SS0) is used to select sector size. If SS0 = 0, then the sector size is 256 bytes and if SS0 = 1, then the sector size is 512 bytes.

3.3.6.3 BIT 4 DRIVE SELECT

Bit 4 specifies the desired drive number. This bit also determines which of the two internal drive status registers are read when the host accesses the host status register or alternate status register. If DS = 0, the host receives drive zero status. If DS = 1, then the host receives drive one status.

3.3.6.4 BITS 3 THROUGH 0 HEAD NUMBER

Bits 3, 2, 1 and 0 specify the desired head number.

3.3.7 HOST STATUS REGISTER (HA9, HA2 THRU HA0 = 7, READ)

The status register reads only and reflects the status of the controller as well as the status of certain drive control lines. Some of the status bits are controlled by the local microcontroller. Drive status comes from two registers in the WD42C22C, one for each drive. Bit 4 of the SDH register in the AT task file copy controls which of the two registers is read when the host reads this port. Reading of the status register by the host resets INTRQ. The description of the status register bits follows:

Bit							
7	6	5	4	3	2	1	0
ABSY	RDY	WF	SC	DRQ	DWC	IDX	ERR

3.3.7.1 BIT 7 AT BUSY

This bit is set to 1 when the controller is accessing the disk. ABSY is activated by the start of a command (writing into the host command register). It is deactivated at end of all commands by the local microcontroller. This bit is also set during a reset.

3.3.7.2 BIT 6 DRIVE READY

This bit reflects the state of the DRDY drive status pin. Any command aborts if DRDY is low. This bit is written by the local microcontroller.

3.3.7.3 BIT 5 WRITE FAULT

This bit reflects the state of the WF drive status pin. Any command aborts if WF is high. This bit is written by the local microcontroller.

3.3.7.4 BIT 4 SEEK COMPLETE

This bit reflects the state of the SC signal coming from the drive. This bit is written by the local microcontroller.

3.3.7.5 BIT 3 DATA REQUEST

This bit is asserted when the host should be transferring data between the RAM buffer and host. This bit is controlled by the buffer manager.

3.3.7.6 BIT 2 DATA WAS CORRECTED

This bit indicates that an error in the data field was detected and corrected. The buffer contains corrected data. This bit is written by the local microcontroller.

3.3.7.7 BIT 1 INDEX

This bit reflects the state of the INDEX pin.

3.3.7.8 BIT 0 ERROR

This bit indicates that a non-recoverable error has occurred. The error register describes the error condition when this bit is active. This bit is written by the local microcontroller.

3.3.8 HOST COMMAND REGISTER (HA9, HA2 THRU HA0 = 7, WRITE)

The command to be executed is written into this register. Writing this register sets ABSY in the status register and asserts the $\overline{\text{MCINT}}$ pin going to the local microcontroller. The command latches in a register which the local microcontroller reads. Writing this register resets INTRQ.

3.3.9 ALTERNATE STATUS REGISTER (HA9, HA2 THRU HA0 = E, READ)

This register is the same as the host status register (7) but mapped at a different address. Refer to page 23 for the bit description.

3.3.10 FIXED DISK REGISTER (HA9, HA2 THRU HA0 = E, WRITE)

The fixed disk register is used by the host to control some of the internal functions of the WD42C22C. Bit 0 and bits 4 through bit 7 are reserved for future definition. These bits are currently not used in the AT protocol but they are implemented in the WD42C22C, i.e. the fixed disk register passes 8 bits between the host and the

local microcontroller. The host should write zeroes to these bits in AT mode. The fixed disk register is coded as follows:

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	HS3EN	RST	$\overline{IEN}$	0

3.3.10.1 BIT 3 HEAD SELECT 3 ENABLE

When HS3EN = 1, then HEAD SELECT 3 is asserted by the local microcontroller. When HS3EN = 0, then RWC is asserted by the local microcontroller.

3.3.10.2 BIT 2 RESET

Writing a 1 to this bit resets the WD42C22C. The RESET output is asserted and remains asserted until this bit is written back to 0. This bit must be on for a minimum of 5.0 µsec. If reset has been disabled by the local microcontroller then writing a '1' to this bit only resets the WD42C22C. $\overline{RESET}$ is not asserted in this case. The WD42C22C asserts $\overline{MCINT}$ and the local microcontroller is responsible for resetting the drive controller board logic.

3.3.10.3 BIT 1 $\overline{INTERRUPT\ ENABLE}$

When $\overline{IEN}$ = 0, then the $\overline{INTRQ}$ output to the host is enabled. When $\overline{IEN}$ = 1, then the INTRQ output to the host is disabled. Disabling interrupts does NOT reset an existing interrupt but inhibits all further interrupts. Any interrupts pending when this bit is set causes the INTRQ output to be asserted. A system master reset does NOT affect the $\overline{IEN}$ bit but resets any existing interrupt. The internal power qualified reset sets $\overline{IEN}$ to 0. When interrupts are disabled, then the INTRQ pin is tri-stated.

3.3.11 DIGITAL INPUT REGISTER (HA9, HA2 THRU HA0 = F, READ)

The digital input register is used by the host to determine the state of WRITE GATE and the drive selects and head selects. Bit 5 is written by the local microcontroller when HS3EN (bit 3 of the fixed disk register) is set to zero. Bit 5 comes from bit 3 of the host SDH register with HS3EN set to one. Bits 0 through bit 4 also come from the host SDH register. When this register is read by the host, then HD7 (pin 82) is tri-stated. It is coded as follows:

Bit							
7	6	5	4	3	2	1	0
X	$\overline{WG}$	$\overline{HS3}$/ RWC	$\overline{HS2}$	$\overline{HS1}$	$\overline{HS0}$	$\overline{DS2}$	$\overline{DS1}$

3.3.11.1 BIT 6 WRITE GATE ON

This bit reflects the state of the $\overline{WG}$ output pin.

3.3.11.2 BIT 5 HEAD SELECT 3/ REDUCE WRITE CURRENT

This bit reflects the state of the $\overline{HS3}$/$\overline{RWC}$ drive control output. The $\overline{RWC}$ bit is written by the local microcontroller. $\overline{HS3}$ comes from the SDH register bit 3.

3.3.11.3 BIT 4, BIT 3, AND BIT 2 HEAD SELECTS

These bits reflect the states of the $\overline{HS2}$, $\overline{HS1}$, $\overline{HS0}$, and drive control outputs respectively. These bits are controlled by SDH register bits 2 through 0 respectively.

3.3.11.4 BIT 1 AND BIT 0 DRIVE SELECTS

These bits indicate which drive is currently being selected by the host. They are controlled by the SDH register bit 4.

33

A D 7	A D 6	A D 5	A D 4	A D 3	A D 2	A D 1	A D 0	READ PORT	WRITE PORT
DISK CONTROLLER TASK FILE									
0	0	0	X	X	X	X	X	BUS TRISTATE	NOT USED
0	0	1	0	0	0	0	0	INVALID	INVALID
0	0	1	0	0	0	0	1	Error Register	PLO Length
0	0	1	0	0	0	1	0	Sector Count	Sector Count
0	0	1	0	0	0	1	1	Sector Number	Sector Number
0	0	1	0	0	1	0	0	Cylinder Number Low	Cylinder Number Low
0	0	1	0	0	1	0	1	Cylinder Number High	Cylinder Number High
0	0	1	0	0	1	1	0	SDH	SDH
0	0	1	0	0	1	1	1	Status Register	Command Register
XT									
0	0	1	0	1	1	0	1	Hardware Status	Hardware Status
0	0	1	0	1	1	1	0	NOT USED	Drive Configuration
BUFFER MANAGER									
0	0	1	1	0	0	0	0	Host Buffer Pointer Low	Host Buffer Pointer Low
0	0	1	1	0	0	0	1	Host Buffer Pointer High	Host Buffer Pointer High
0	0	1	1	0	0	1	0	Host Transfer Count Low	Host Transfer Count Low
0	0	1	1	0	0	1	1	Host Transfer Count High	Host Transfer Count High
0	0	1	1	0	1	0	0	Disk Buffer Pointer Low	Disk Buffer Pointer Low
0	0	1	1	0	1	0	1	Disk Buffer Pointer High	Disk Buffer Pointer High
0	0	1	1	0	1	1	0	Microcontroller RAM Access	Microcontroller RAM Access
0	0	1	1	0	1	1	1	Buffer Status	Buffer Control

TABLE 11. LOCAL MICROCONTROLLER REGISTER MAP

3.4 SLAVE HOST INTERFACE

In slave mode, the WD42C22C host interface can be hooked up to a peripheral device such as the WD33C93 (SBIC). The microcontroller reads and writes the peripheral device through the WD42C22C using the ports as follows:

A BSY	A D 7	A D 6	A D 5	A D 4	A D 3	A D 2	A D 1	A D 0	READ PORT	WRITE PORT
X	0	1	0	0	1	0	0	0	Bus tri-state	Slave address port for reads
X	0	1	0	0	1	0	1	0	Bus tri-state	Slave address port for writes
X	0	1	0	0	1	0	0	1	Slave read data	Slave write data

ABSY	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	READ PORT	WRITE PORT
MISC.										
X	0	0	1	1	1	0	0	0	Interface Status	Interface Control
X	0	0	1	1	1	0	0	1	Configuration Status Low	NOT USED
X	0	0	1	1	1	0	1	0	Configuration Status High	NOT USED
X	0	0	1	1	1	0	1	1	Drive Interface Status	Drive Interface Control
X	0	0	1	1	1	1	0	0	Alternate Sector Number	NOT USED
AT INTERFACE										
X	0	0	1	0	1	0	1	0	AT Control Register	AT Control Register
X	0	0	1	1	1	1	0	1	Drive 0 Status	Drive 0 Status
X	0	0	1	1	1	1	1	0	Drive 1 Status	Drive 1 Status
X	0	0	1	1	1	1	1	1	Fixed Disk Register	Digital Input Register
AT INTERFACE (TASK FILE COPY)										
1	0	1	0	0	0	0	0	1	Write Precomp Cylinder	Error Register
1	0	1	0	0	0	0	1	0	Sector Count	Sector Count
1	0	1	0	0	0	0	1	1	Sector Number	Sector Number
1	0	1	0	0	0	1	0	0	Cylinder Number Low	Cylinder Number Low
1	0	1	0	0	0	1	0	1	Cylinder Number High	Cylinder Number High
1	0	1	0	0	0	1	1	0	SDH	SDH
1	0	1	0	0	0	1	1	1	Command Register (from Host)	NOT USED
SLAVE HOST										
0	0	1	0	0	0	X	X	X	INVALID	INVALID
X	0	1	0	0	1	0	0	0	INVALID	Slave Address Port for reads
X	0	1	0	0	1	0	0	1	Slave Read Data	Slave Write Data
X	0	1	0	0	1	0	1	0	INVALID	Slave Address Port for writes
X	0	1	0	0	1	X	X	X	INVALID	NOT USED
X	0	1	0	1	X	X	X	X	INVALID	NOT USED
X	0	1	1	X	X	X	X	X	BUS TRISTATE	NOT USED
X	1	X	X	X	X	X	X	X	BUS TRISTATE	NOT USED

TABLE 11. LOCAL MICROCONTROLLER REGISTER MAP (CONT'D)

The slave peripheral connects to the WD42C22C using an ALE type interface. Register reads and writes are always 8-bit. The procedure to read or write a slave peripheral register is to first write the register number to the slave address port before the register contents are read or written. This address must always be written before each register access even when consecutively accessing the same register two or more times.

Data transfers between the peripheral device and the WD42C22C are WD-bus mode and can be either 8-bit or 16-bit and is controlled by the H16/8 bit (bit 1 of the auxilliary buffer control register). The slave mode is enabled by the HSMB bit (bit 6 of the auxilliary buffer control register).

3.5 LOCAL MICROCONTROLLER INTERFACE ORGANIZATION

The local microcontroller controls the host interface mode (AT or XT) and controls the buffer manager and the drive controller. The local microcontroller is usually in a sleep state until it is told to do something by the assertion of the MCINT output. In the XT mode, MCINT is asserted when the controller is selected. In the AT mode, MCINT is asserted when the host writes to the command register. In slave host mode, MCINT is asserted when the slave peripheral device asserts its INTRQ signal. MCINT is also asserted at the end of each host or disk transfer regardless of the interface mode.

The local microcontroller can have either the Intel-type (8051) or the Motorola-type (68HC11) interface. The WD42C22C has a built-in MOtorola-inTEL (MOTEL) circuit which can sense the processor interface type and can therefore be directly interfaced to either type processor.

Table 11 lists the register map for the local microcontroller.

3.6 DISK CONTROLLER TASK FILE (AD7 THRU AD0 = 20 THRU 27)

3.6.1 ERROR REGiSTER (AD7 THRU AD0 = 21, READ)

The error register reads only and contains the specific error status pertaining to a command. The meaning of the status register bits are as follows:

Bit							
7	6	5	4	3	2	1	0
BB	CRC/ ECC	RIDF	IDNF	0	AC	0	DMNF

3.6.1.1 BIT 7 BAD BLOCK

A bad block address mark has been detected when trying to read or write that sector. The data field is not be read or written.

3.6.1.2 BIT 6 CRC/ECC DATA FIELD ERROR

A CRC error in the data field has been detected when in CRC mode. In ECC mode, data errors were detected in the data.

3.6.1.3 BIT 5 RELOCATION ID FOUND

This bit is set if a relocation ID is found after detecting the bad block mark in the desired sector's ID field. This bit is only valid if the R option is used in the set parameter command.

3.6.1.4 BIT 4 ID NOT FOUND

Occurs when cylinder, head, sector, size parameters with a correct ID field CRC cannot be found. For a scan ID command, this bit is set after 10 index pulses if the retry disable bit is not set. Otherwise, IDNF is set after 2 index pulse if no ID was found. For read and write sector commands with the retry disable bit set, this bit indicates that after 10 index pulses, auto-scan ID and auto-seek, and 10 more index pulses, no matching ID field was found. If the retry disable bit is set and no matching ID field was found after 2 index pulses, then no auto-scan or auto-seek is performed.

3.6.1.5 BIT 3 RESERVED

Not used, forced to zero.

3.6.1.6 BIT 2 ABORTED COMMAND

Set if command was started and one of the following conditions occurred:

- 1. Drive not ready
- 2. Write fault
- 3. Illegal command code.

3.6.1.7 BIT 1 RESERVED

Not used in WD42C22C, forced to zero.

3.6.1.8 BIT 0 DATA ADDRESS MARK NOT FOUND

Set if the first two bytes of the data field following an ID match are not A1 F8. This condition is checked for read sector commands only.

3.6.2 PLO LENGTH REGISTER (AD7 THRU AD0 = 21, WRITE)

This register is used for two purposes:

- 1. To determine the length of the Data PLO sync field during write commands and to determine the length of the ID PLO sync field during format commands. The contents of this register regulates the PLO field size in all data coding modes.
- 2. To load a value in the internal GAP register. During the load parameter block command, the contents of the lower six bits of the PLO length register are transferred to the internal GAP register. In hard sector NRZ (ESDI) mode, this internal GAP register is used to control the delay between the INDEX or SECTOR pulse and the leading edge of READ GATE. In hard sector MFM or RLL mode, this internal GAP register is used to control the delay between the INDEX or SECTOR pulse and the falling edge of the internally generated DRUN signal. In hard sector MFM or RLL mode, RG is asserted 2 byte times after INDEX or SECTOR. This GAP register is altered by loading the desired GAP register value into the PLO length register and then issuing a load parameter block command.

3.6.3 SECTOR COUNT (AD7 THRU AD0 = 22, READ/WRITE)

Bit							
7	6	5	4	3	2	1	0
NUMBER OF SECTORS/GAP VALUE SECTOR WITH BAD BLOCK							

This register is used for three purposes:

- 1. The sector count register is used in read sector, write sector, and format commands to implement multiple sector handling with one command. A value of 1 indicates a single sector transfer, a value of 2 indicates a 2 sector transfer, and so forth. A value of 0 indicates a 256 sector transfer. Sector count decrements and sector number increments after each sector transfer to or from the buffer.
- 2. To load a value into the internal gap value register. During the load parameter block command the contents of this register are transferred into an internal gap value register. This gap value register specifies the data byte written into the gaps during format commands.
- 3. To specify to the microcontroller the sector number where a bad block bit was detected if relocation ID searches are enabled. If the R option is set in a set parameter command, then during read and write commands if a bad block is detected, the WD42C22C searches for a special ID field containing relocation information. When the command terminates due to a bad block, then the sector number of the sector with the bad block is returned to the microcontroller in this register. This is true whether or not the relocation information is detected.

3.6.4 SECTOR NUMBER (AD7 THRU AD0 = 23, READ/WRITE)

Bit							
7	6	5	4	3	2	1	0
SECTOR NUMBER / GAP SIZE							

The sector number register has three uses:

- 1. To hold the number of the desired sector for read and write commands. The sector number can range from 0 to 255.
- 2. To control the Gap 1 and Gap 3 sizes during format commands. The sector number holds the number of gap bytes minus three for format (number of gap bytes minus six for NRZ mode).
- 3. To load a value into the internal pad value register. During the load parameter block command, the contents of this register are transferred into an internal pad value register. This pad value register specifies the data byte written into the ID and DATA pads during format and write commands.

3.6.5 CYLINDER NUMBER REGISTERS (CYLINDER NUMBER LOW: AD7 THRU AD0 = 24, READ WRITE CYLINDER NUMBER HIGH: AD7 THRU AD0 = 25, READ/WRITE)

This register has two functions:

- 1. To specify the cylinder number for read, write, and format commands. The cylinder number may range in value from 0 to 2047.
- 2. The cylinder number register is used during a load parameter block command to specify the desired sector size if a non-standard sec-

tor size is desired and to specify the offset for a write ID command. To load the internal sector size register, write in the desired sector size into the cylinder registers. Next, issue a load parameter block command. Set U=1 to enable the programmable sector size or programmable write ID offset.

3.6.6 CYLINDER NUMBER REGISTERS (CYLINDER NUMBER LOW: AD7 THRU AD0 = 24, READ/WRITE CYLINDER NUMBER HIGH: AD7 THRU AD0 = 25, READ/WRITE)

Cylinder number low register holds the 8 least significant bits of the desired cylinder number or the 8 least significant bits of the desired sector size.

Cylinder number high register holds the three most significant bits (bits 0 through 2) of the desired cylinder number or the three most significant bits of the desired sector size. Bits three through seven of the cylinder number high register are not used and must be set to zero.

3.6.7 SDH REGISTER (AD7 THRU AD0 = 26, READ/WRITE)

This register is used to specify the desired drive and head numbers and to specify CRC or ECC mode. There are two SDH modes available, three or four bit head number. Three bit head mode is the default after a master reset. Setting the H bit in the set parameter command engages the four bit head mode.

3.6.7.1 SDH REGISTER, THREE-BIT HEAD NUMBER

Bit							
7	6	5	4	3	2	1	0
CRC/ ECC	SS1	SS0	0	0	Head #		

3.6.7.2 SDH REGISTER, FOUR-BIT HEAD NUMBER

Bit							
7	6	5	4	3	2	1	0
CRC/ ECC	SS1	SS0	0	Head #			

3.6.7.3 BIT 7 ECC/CRC SELECT

This bit is set for data field ECC mode. It is reset for data field CRC mode. In RLL mode, this bit is ignored. RLL mode always uses 7-byte ECC. The CRC/ECC flag bit is not written on the disk at format time. The bad block flag is written on the disk in its place.

3.6.7.4 BIT 6 AND BIT 5 SECTOR SIZE

Bits 6 and 5 contain sector size bits. These bits are written on the disk at format time. These bits should be 0 if programmable sector size is used. These bits are reserved for special flags in programmable sector size mode. The possible sector sizes and their selection codes are as follows:

SS1	SS0	Sector Size
0	0	256 byte data field
0	1	512 byte data field
1	0	1024 byte data field
1	1	128 byte data field

The sector sizes can be optionally specified to be any value between 100 and 2048 bytes by using the load parameter block command. The user is responsible for validating the effectiveness of the ECC for sector sizes over 1056 bytes.

3.6.7.5 BIT 4 AND BIT 3 RESERVED BIT 4 DRIVE NUMBER RESERVED

Reserved. Set to 0.

3.6.7.6 BIT 2, BIT 1, AND BIT 0 THREE BIT HEAD NUMBER BIT 3, BIT 2, BIT 1, AND BIT 0 FOUR BIT HEAD NUMBER

Bits 2, 1, and 0 specify the desired head number in the three bit mode. Bits 3, 2, 1, and 0 specify the desired head number in four bit mode. The local microcontroller is responsible for outputting these bits to the drive.

NOTE

These bits are written on the disk at format time. The SDH byte written in the ID field during a format command is NOT the same as the SDH register. The SDH format byte is shown below:

3.6.7.7 SDH ID FIELD FORMAT BYTE (THREE BIT HEAD MODE)

Bit							
7	6	5	4	3	2	1	0
Bad Block	SS1	SS0	0	0	Head #		

3.6.7.8 SDH ID FIELD FORMAT BYTE (FOUR BIT HEAD MODE)

Bit							
7	6	5	4	3	2	1	0
Bad Block	SS1	SS0	0	Head #			

3.6.8 STATUS REGISTER (AD7 THRU AD0 = 27, READ)

The status register is read only and reflects the status of the controller as well as the status of certain drive control lines. If command in progress (bit 1) is set then no other register reads are valid and none of the other register bits are valid. The status register contents are returned for any read and all writes are disabled. The description of the status register bits follows:

Bit							
7	6	5	4	3	2	1	0
0	RDY	WF	1	0	0	0	ERR

3.6.8.1 BIT 7 ALWAYS 0

This bit is always zero when the microcontroller has access to this status register.

3.6.8.2 BIT 6 DRIVE READY

This bit reflects the status of the DRDY. Any command aborts if DRDY is low.

3.6.8.3 BIT 5 WRITE FAULT

This bit reflects the state of the WF pin. Any command aborts if WF is high.

3.6.8.4 BIT 4 ALWAYS 1

This bit reflects the state of the SC input to the drive controller. This signal is internally tied to V_{DD}.

3.6.8.5 BIT 3 ALWAYS 0

This bit reflects the state of the BDRQ signal that goes between the drive controller and the buffer manager. It is always zero when the microcontroller has access to this status register.

3.6.8.6 BIT 2 NOT USED

Forced to 0

3.6.8.7 BIT 1 ALWAYS 0

This bit reflects the state of the command in progress signal in the drive controller. It is always zero when the microcontroller has access to this status register.

3.6.8.8 BIT 0 ERROR

This bit indicates that a non-recoverable error has occurred. The error register describes the error condition when this bit is asserted.

Drive ready and write fault bits reflect the state of their associated input pins. The states of these status register bits are latched at the end of the command and are unlatched after the first status register read. Reading the status register results in the disk controller interrupt being reset.

3.6.9 COMMAND REGISTER (AD7 THRU AD0 = 27, WRITE)

The command to be executed is written into this register. Writing this register sets the internal BUSY and CIP signals and causes the controller to start executing the desired command. Writing this register resets the disk controller interrupt (DCI bit in the interface status register).

3.7 XT INTERFACE PORTS

3.7.1 XT HOST HARDWARE STATUS (AD7 THRU AD0 = 2D, READ/WRITE)

Bits 7, 6, 2, and 1 of this register are written by the local microcontroller and read by the host. The other bits reflect the state of certain hardware signals. This register is readable and valid in all host modes.

Bit							
7	6	5	4	3	2	1	0
1	1	IRQ	DRQ	XBSY	C/$\overline{D}$	I/$\overline{O}$	REQ

3.7.1.1 BITS 6 AND 7 UNDEFINED

These bits are currently undefined in the XT protocol and read as 1.

3.7.1.2 BIT 5 INTERRUPT REQUEST

This bit reflects the state of the INTRQ output. This bit can NOT be written by the microcontroller.

3.7.1.3 BIT 4 DMA REQUEST

This bit reflects the state of the DREQ output. This bit can NOT be written by the microcontroller.

3.7.1.4 BIT 3 XT BUSY

This bit reflects the state of the internal XT BUSY flipflop. This bit is set by during a reset and is set when the WD42C22C is selected in XT mode. This bit can NOT be written by the microcontroller.

3.7.1.5 BIT 2 COMMAND / $\overline{\text{DATA}}$

This bit tells the host which type of transfer is expected at the read data and write data ports. C/$\overline{D}$ = 1 indicates that a command or status transfer is expected and C/$\overline{D}$ = 0 indicates that a data transfer is expected. This bit is written by the microcontroller.

3.7.1.6 BIT 1 INPUT / $\overline{\text{OUTPUT}}$

This bit tells the host the direction of transfer for the two data ports. I/$\overline{O}$ = 1 indicates an input (read) by the host and I/$\overline{O}$ = 0 indicates an output (write) by the host. This bit is written by the microcontroller.

3.7.1.7 BIT 0 REQUEST

This bit indicates the state of the internal host transfer enable. This bit is active when the buffer manager is transferring data between the RAM and the host. This bit can NOT be written by the microcontroller. This bit is identical to the DRQ in the drive zero status and drive one status registers used in AT mode.

3.7.2 HOST DRIVE CONFIGURATION (AD7 THRU AD0 = 2E, WRITE)

This register is used to write the drive configuration information that is read by the host.

3.7.3 BUFFER MANAGER REGISTERS (AD7 THRU AD0 = 30 THRU 37) HOST BUFFER POINTER LOW (AD7 THRU AD0 = 30, READ/WRITE) HOST BUFFER POINTER HIGH (AD7 THRU AD0 = 31, READ/WRITE)

Bit							
7	6	5	4	3	2	1	0
LEAST SIGNIFICANT BYTE OF HOST BUFFER POINTER							

Bit							
7	6	5	4	3	2	1	0
0	MOST SIGNIFICANT BITS OF HOST BUFFER POINTER						

The host buffer pointer low register contains the least significant byte of the host buffer pointer. The host buffer pointer high register contains the seven most significant bits of the host buffer pointer. The host buffer pointer is used as the base address for the internal host buffer counter. The contents of the host buffer pointer registers are transferred to the host buffer pointer counter under the control of the buffer control register.

When the AHBP bit is set in the control register, then the pointer register is transferred to the pointer counter when the transfer counter reaches zero. If the transfer count is already zero, then the transfer occurs immediately. This allows a pending transfer to be queued behind the current transfer. When the pointer is transferred to the counter, the AHBP buffer status bit resets.

3.7.4 HOST TRANSFER COUNT LOW (AD7 THRU AD0 = 32, READ/WRITE HOST TRANSFER COUNT HIGH (AD7 THRU AD0 = 33, READ/WRITE)

The host transfer count low register contains the least significant byte of the host transfer count. The host transfer count high register contains the most significant bits of the host transfer count. The transfer count controls the number of bytes that are to be transferred on the host interface. The transfer count register is transferred to the internal transfer counter at the same time that the host buffer pointer register is transferred to the

host buffer pointer counter. The transfer counter is 12 bits long which gives a maximum transfer count of 4095 bytes.

Bit							
7	6	5	4	3	2	1	0
LEAST SIGNIFICANT BYTE OF HOST TRANSFER COUNT							

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	MS BITS OF HOST TRANSFER COUNT			

3.7.5 DISK BUFFER POINTER LOW (AD7 THRU AD0 = 34, READ/WRITE) DISK BUFFER POINTER HIGH (AD7 THRU AD0 = 35, READ/WRITE)

The disk pointer low register contains the least significant byte of the disk buffer pointer. The disk pointer high register contains the seven most significant bits of the disk buffer pointer. The disk buffer pointer is used as the base address for the internal disk buffer counter. The contents of the disk buffer pointer registers are transferred to the disk buffer pointer counter under the control of the buffer control register. When the ADBP bit is set in the control register, then the pointer is transferred to the counter when the drive controller sets DRQI to 1 (bit 1) in the interface status register (38_{16}). This allows a pending transfer to be queued behind the current transfer. When the pointer register is transferred to the counter, the ADBP bit in the buffer status resets. If ADBP=0 when the drive controller sets DRQI to 1, then the drive controller stops transferring data to the buffer and discontinues the command until ADBP sets.

Bit							
7	6	5	4	3	2	1	0
LEAST SIGNIFICANT BYTE OF DISK BUFFER POINTER							

Bit							
7	6	5	4	3	2	1	0
0	MOST SIGNIFICANT BYTE OF DISK BUFFER POINTER						

3.7.6 MICROCONTROLLER RAM ACCESS PORT (AD7 THRU AD0 = 36, READ/WRITE)

This port is used by the local microcontroller to access the buffer RAM. Accesses to this port go through the drive controller's FIFO. These accesses are enabled by the MAC bit in the drive interface control register. The DRWB bit in the buffer manager control register controls the direction of the accesses.

3.7.7 BUFFER CONTROL REGISTER (AD7 THRU AD0 = 37, WRITE)

This register is used to control the buffer manager.

Bit			
7	6	5	4
AT/$\overline{XT}$	RDCFG	RXC	AHBP
3	2	1	0
HRWB	DRWB	BDEN	ADBP

3.7.7.1 BIT 7 AT / $\overline{XT}$ INTERFACE CONTROL

This bit, along with HSMB, in the auxilliary buffer control register, controls the host interface type. If AT/$\overline{XT}$ = 0, then the interface is XT type if HSMB = 0. If AT/$\overline{XT}$ = 1, then the interface is AT type if HSMB = 0. This bit has no meaning if HSMB = 1. The RESET input and the host soft reset does not affect this bit.

3.7.7.2 BIT 6 READ CONFIGURATION

When this bit is set, all buffer address outputs are placed in a medium impedence state with each buffer address pin having a 180 µA current source pulldown. The buffer manager should be idle when this mode is enabled. This mode is used to read configuration switch information. The microcontroller should wait 100 µsec after setting this bit before reading the configuration registers. This bit resets when $\overline{RESET}$ is asserted.

3.7.7.3 BIT 5 RESET TRANSFER COUNTER

When this bit is set, the internal transfer counter and the host FIFO pointers reset. This bit resets after the transfer counter and FIFO reset.

3.7.7.4 BIT 4 ARM HOST BUFFER POINTER

Writing a 1 to this bit, sets an internal latch. Writing a 0 to this bit has no effect. When this bit is set, then when the internal transfer counter reaches zero the host buffer pointer is transferred to the internal host buffer counter and the host transfer count is transferred to the internal transfer counter. This bit is reset by the WD42C22C after the host pointer and count registers are transferred. This bit resets when $\overline{\text{RESET}}$ is asserted.

3.7.7.5 BIT 3 HOST READ / $\overline{\text{WRITE}}$

This bit controls the direction of the host data transfers. It is used internally to control the direction of the FIFO. When HRWB = 0, then the host writes to the WD42C22C. When HRWB = 1, then the host reads from the WD42C22C.

3.7.7.6 BIT 2 DISK READ / $\overline{\text{WRITE}}$

This bit controls the direction of the disk or local microcontroller data transfers. It is used internally to control the direction of the disk FIFO. When DRWB = 0, then the disk controller or local microcontroller writes to the buffer RAM. When DRWB = 1, then the disk controller or local microcontroller reads from the buffer RAM. When the microcontroller accesses the buffer RAM, then this bit should be written before the ADBP bit is set.

3.7.7.7 BIT 1 BURST DMA ENABLE

When BDEN = 1 and HDMA = 1 in the auxilliary buffer control register, then burst DMA transfers are enabled on the host interface.

3.7.7.8 BIT 0 ARM DISK BUFFER POINTER

Writing a 1 to this bit, sets an internal latch. Writing a 0 to this bit has no effect. When this bit is set, then the disk buffer pointer is transferred to the internal disk buffer counter when the drive controller sets the BDRQ interrupt. This bit also enables the disk controller to continue to the next sector. This bit is reset by the WD42C22C after the pointer registers have been transferred. When the disk controller port is used by the local microcontroller to access the buffer RAM, then setting this bit resets the disk FIFO pointers and the next byte read or written by the microcontroller will be at the new address loaded into the disk buffer pointer.

3.7.8 BUFFER STATUS REGISTER (AD7 THRU AD0 = 37, READ)

This register reflects the status of the buffer manager logic.

Bit			
7	**6**	**5**	**4**
AT/$\overline{\text{XT}}$	RDCFG	RXC	AHBP
3	**2**	**1**	**0**
HRWB	DRWB	BDEN	ADBP

3.7.8.1 BIT 7 AT / $\overline{\text{XT}}$ INTERFACE MODE

This status bit reflects the state of the AT/$\overline{\text{XT}}$ control bit defined above.

3.7.8.2 BIT 6 READ CONFIGURATION

This bit reflects the state of the read configuration control bit defined in the buffer manager control register.

3.7.8.3 BIT 5 RESET TRANSFER COUNTER

This bit reflects the state of the RXC control bit defined in the buffer control register.

3.7.8.4 BIT 4 HOST BUFFER POINTER ARMED

This bit reflects the state of the AHBP control bit defined in the buffer control register.

3.7.8.5 BIT 3 HOST READ / $\overline{\text{WRITE}}$

This bit reflects the state of the HRWB control bit defined in the buffer control register.

3.7.8.6 BIT 2 DISK READ / $\overline{\text{WRITE}}$

This bit reflects the state of the DRWB control bit defined in the buffer control register.

3.7.8.7 BIT 1 BURST DMA ENABLE

This bit reflects the state of the BDEN control bit defined in the buffer control register.

3.7.8.8 BIT 0 DISK BUFFER POINTER ARMED

This bit reflects the state of the ADBP control bit defined in the buffer control register.

3.7.9 AUXILLIARY BUFFER CONTROL REGISTER (AD7 THRU AD0 = 2F, WRITE)

This register is used for additional control of the buffer manager and host interface.

Bit			
7	6	5	4
HDMA	HSMB	BCNT	IDD
3	2	1	0
DSEL	X	H16/$\overline{8}$	SCKS

3.7.9.1 BIT 7 HOST DMA

This bit controls the host data transfers to/from the buffer RAM. If HDMA = 1, then the data is transferred to the host via DMA regardless of the host interface selected. If HDMA = 0, the default, then data is transferred via programmed I/O.

3.7.9.2 BIT 6 HOST SLAVE / $\overline{\text{MASTER}}$

When HSMB = 0, the default, then the host is a master which drives the WD42C22C in either XT or AT type interface. When HSMB = 1, then the host is a slave device which is controlled by the local microcontroller. The slave device can be addressed in either ALE or indirect mode. The SBIC is an example of a device which can be connected to the WD42C22C. The ALE mode supports up to 32 registers in the slave device. Data transfers occur via WD-BUS mode if HDMA = 1 and is an 8-bit transfer if H16/$\overline{8}$ = 0 and a 16-bit transfer if H16/$\overline{8}$ = 1. This bit resets upon power-up but not affected by $\overline{\text{RESET}}$.

3.7.9.3 BIT 5 BURST CONTINUOUS

This bit, along with the HDMA bit, and the BDEN bit in the buffer control register control the bursting of data during DMA transfers. If BCNT = 1, HDMA = 1, and BDEN = 1, then the WD42C22C DMAs data continuously as long as the FIFOs can keep up. If BCNT = 0, HDMA = 1, and BDEN = 1, then the WD42C22C DMAs data in 8-byte or 16-byte maximum length bursts, for 8 and 16 bit host data bus width, respectively.

3.7.9.4 BIT 4 INTELLIGENT DRIVE DECODE

When IDD = 1, then the controller is assumed to be on an intelligent drive. The HD0-15, INTRQ, and DREQ/IOCS16 outputs are always tri-stated if the drive is not selected. If IDD = 0, the default, then the outputs are controlled normally. This bit resets upon power up but not affected by $\overline{\text{RESET}}$.

3.7.9.5 BIT 3 DRIVE SELECT

This bit is used when IDD = 1 to control drive selection. If AT/$\overline{\text{XT}}$ =1, then the drive is considered selected when SDH register bit 4 equals DSEL. If AT/$\overline{\text{XT}}$ = 0, then the drive is considered selected if DSEL = 1 and not selected if DSEL = 0. This bit resets upon power-up but not affected by $\overline{\text{RESET}}$.

3.7.9.6 BIT 1 HOST 16 / $\overline{8}$ BIT

This bit controls the width of the data transfers on the host side. If H16/$\overline{8}$ = 0, then the host data transfers are 8-bit. If H16/$\overline{8}$ = 1, the host data transfers are 16-bit. This bit resets upon power up but not affected by $\overline{\text{RESET}}$.

3.7.9.7 BIT 0 SYNCHRONOUS CLOCK SWITCH

This bit is used to control the clocking of the drive controller so that ESDI drives can be changed or data rates can be changed without the need for external clock deglitching. When SCKS =1, the default, then the WD42C22C synchronously switches the drive controller to the internal buffer clock (BCLK). When SCKS = 0, the WD42C22C switches the drive controller back to WCLK. The switch occurs only if both clocks are present. The CKSRC status bit defined below indicates whether or not the switch occured. When $\overline{\text{RESET}}$ is asserted, the buffer clock clocks the drive controller during the reset and SCKS is set. The microcontroller must switch the clock source to the WCLK input prior to issuing any commands to the drive controller.

3.7.10 AUXILLIARY BUFFER STATUS REGISTER (AD7 THRU AD0 = 2F, READ)

This register gives additional status of the buffer manager and host interface.

Bit			
7	6	5	4
HDMA	HSMB	BCNT	IDD
3	2	1	0
DSEL	CKSC	H16/$\overline{8}$	SCKS

3.7.10.1 BIT 7 HOST DMA

This bit reflects the state of the HDMA control bit defined in the auxilliary buffer control register.

3.7.10.2 BIT 6 HOST SLAVE / $\overline{\text{MASTER}}$

This bit reflects the state of the HSMB control bit defined in the auxilliary buffer control register.

3.7.10.3 BIT 5 BURST CONTINUOUS

This bit reflects the state of the BCNT control bit defined in the auxilliary buffer control register.

3.7.10.4 BIT 4 INTELLIGENT DRIVE DECODE

This bit reflects the state of the IDD control bit defined in the auxilliary buffer control register.

3.7.10.5 BIT 3 DRIVE SELECT

This bit reflects the state of the DSEL control bit defined in the auxilliary buffer control register.

3.7.10.6 BIT 2 CLOCK SOURCE

This bit indicates the source of the drive controller clock. If CKSRC = 1 and SCKS = 1, then the drive controller is being clocked by the buffer clock (BCLK). If CKSRC = 0 and SCKS = 0, then the drive controller is clocked by WCLK. If CKSRC = 1 and SCKS = 0 or CKSRC = 0 and SCKS = 1, then the clock source is undefined. CKSRC should not be checked until at least 10 clock periods after the SCKS has been written. The slower of BCLK and WCLK should be used in determining this delay.

3.7.10.7 BIT 1 HOST 16 / $\overline{8}$

This bit reflects the state of the H16/$\overline{8}$ control bit defined in the auxilliary buffer control register.

3.7.10.8 BIT 0 SYNCHRONOUS CLOCK SWITCH

This bit reflects the state of the SCKS control bit defined in the auxilliary buffer control register.

3.7.11 INTERFACE STATUS REGISTER (AD7 THRU AD0 = 38, READ)

This register is used to indicate the status of the WD42C22C. The bits are defined as follows:

Bit			
7	**6**	**5**	**4**
MINT	DCGI	RSTI	FEI
3	**2**	**1**	**0**
DCI	HPRI	DRQI	CWSI

3.7.11.1 BIT 7 MICROCONTROLLER INTERRUPT

This bit is high if the $\overline{\text{MCINT}}$ output pin is asserted. $\overline{\text{MCINT}}$ is the logical OR of seven sources:

- 1. A host SDH register write
- 2. A host soft reset
- 3. A FIFO error
- 4. The disk controller interrupt signal
- 5. The host transfer count interrupt flip-flop
- 6. The disk controller BDRQ signal
- 7. The command write/select interrupt flip-flop.

If any of the bits 6 through 0 are set, then the MCINT bit is high.

3.7.11.2 BIT 6 DRIVE CHANGE INTERRUPT

This bit sets when the host writes a new value to the SDH register bit 4 when AT mode is selected.

3.7.11.3 BIT 5 SOFT RESET INTERRUPT

This bit sets if the host initiates a soft reset. This bit resets by writing the proper bit in the interface control register.

3.7.11.4 BIT 4 FIFO ERROR INTERRUPT

This bit sets if a FIFO overrun or underrun condition occurs during host or disk transfers. It resets by writing the proper bit in the interface control register.

3.7.11.5 BIT 3 DISK CONTROLLER INTERRUPT

This bit reflects the state of the disk controller interrupt signal. This interrupt occurs at the end of a command. This bit resets either when the disk controller status (port 27_{16}) is read or when the disk controller command (port 27_{16}) register is written.

3.7.11.6 BIT 2 HOST POINTER READY INTERRUPT

This bit reflects the state of the host transfer count interrupt flip-flop. This interrupt sets when the host

transfer counter reaches zero and the FIFO is empty if the host pointer is not armed. It is also set when the host pointer pipeline register is loaded into the host pointer counter. It resets by writing the proper bit in the interface control register.

3.7.11.7 BIT 1 DISK BDRQ INTERRUPT

This bit reflects the state of the disk controller BDRQ signal. It sets when the disk controller starts a transfer between the disk controller and the sector buffer. It resets by writing the proper bit in the interface control register. If ADBP = 0 (bit 0 in the buffer control register, 37_{16}) when this bit first goes from 0 to 1, then DRQI and MCINT is not reset until after the microcontroller writes ADBP = 1.

3.7.11.8 BIT 0 COMMAND WRITE / SELECT / SLAVE INTERRUPT

This bit informs the local microcontroller that a command has been written if the WD42C22C is in AT mode, that the WD42C22C has been

selected if it is in XT mode, or that the slave host device has issued an interrupt if in slave host mode. (Asserts INTRQ. A slave interrupt only triggers on rising edge of INTRQ.) This bit resets by writing the proper bit in the interface control register.

3.7.12 INTERFACE CONTROL REGISTER (AD7 THRU AD0 = 38, WRITE)

This register is used to control various parts of the WD42C22C. The bits are defined as follows:

Bit			
7	**6**	**5**	**4**
SIRQ	RDCI	RSRI	RFEI
3	**2**	**1**	**0**
RBSY	RHRI	RDQI	RCWS

3.7.12.1 BIT 7 SET INTERRUPT

Writing a 1 to this bit generates a host interrupt if interrupts are enabled.

3.7.12.2 BIT 6 RESET DRIVE CHANGE INTERRUPT

Writing a 1 to this bit resets the host SDH write interrupt flip-flop.

3.7.12.3 BIT 5 RESET SOFT RESET INTERRUPT

Writing a 1 to this bit resets the soft reset interrupt flip-flop. In AT mode, the microcontroller must wait for the RST bit (2) in the FDR register ($3F_{16}$) to be reset by the host before this interrupt can be reset.

3.7.12.4 BIT 4 RESET FIFO ERROR INTERRUPT

Writing a 1 to this bit resets the FIFO error interrupt flip-flop.

3.7.12.5 BIT 3 RESET BUSY

Writing a 1 to this bit resets the BSY status bit in the hardware status register if XT mode is selected or it resets the ABSY status bit in the host status register if AT mode is selected. In AT mode, this bit should only be set at the very end of a command after the last DRQ is asserted to the host. Internal logic handles ABSY during buffer transfers to the host.

3.7.12.6 BIT 2 RESET HOST POINTER READY INTERRUPT

Writing a 1 to this bit resets the host pointer ready interrupt flip-flop.

3.7.12.7 BIT 1 RESET DISK BDRQ INTERRUPT

Writing a 1 to this bit resets the disk BDRQ interrupt flip-flop.

3.7.12.8 BIT 0 RESET COMMAND WRITE / SELECT / SLAVE INTERRUPT

Writing a 1 to this bit resets the command write/select/slave interrupt flip-flop.

3.7.13 CONFIGURATION STATUS REGISTERS (LOW: AD7 THRU AD0 = 39, READ HIGH: AD7 THRU AD0 = 3A, READ)

The configuration status registers are used to read the configuration jumpers on buffer address pins. When in read configuration mode, the buffer address lines have 300 µA current source pulldowns enabled. If there is no external pullup

resistor on the buffer address line, then the state of the line is read as a 0. If a 13K external pullup resistor is connected to a buffer address line, then the state of the line is read as a 1. The configuration registers should not be read until 100 µsec after enabling read configuration mode, to allow the buffer address line voltages to reach their proper value. Register contents are undefined if not in read configuration mode.

Configuration status low							
Bit							
7	6	5	4	3	2	1	0
BA7 THRU BA0							
Configuration status high							
Bit							
7	6	5	4	3	2	1	0
0	BA14 THRU BA8						

3.7.14 DRIVE INTERFACE STATUS (AD7 THRU AD0 = 3B, READ)

This register gives status information for the drive controller. It is coded as follows:

Bit							
7	6	5	4	3	2	1	0
RDC	DRDY	WF	HDS	MAC	DRO	IPOL	DSN

3.7.14.1 BIT 7 RESET DRIVE CONTROLLER

This bit reflects the state of the reset drive controller control bit defined in the drive interface control register.

3.7.14.2 BIT 6 DRIVE READY

This bit is set if the $\overline{\text{DRDY}}$ input is asserted by the drive. It can always be read by the local microcontroller regardless of the state of disk controller busy.

3.7.14.3 BIT 5 WRITE FAULT

This bit is set if the $\overline{\text{WF}}$ input is asserted by the drive. It is always valid.

3.7.14.4 BIT 4 HOST DRIVE SELECT

This bit reflects the state of bit 4 of register 46_{16}, the host copy of the SDH register. It is used by the host in AT mode as a drive select. If HDS = 0, then drive 1 is selected. If HDS = 1, then drive 2 is selected. This bit is always accessable to the microcontroller regardless of the state of ABSY.

3.7.14.5 BIT 3 MICROCONTROLLER ACCESS CONTROL

This bit reflects the state of the microcontroller access control bit defined in the drive interface control register.

3.7.14.6 BIT 2 DISABLE RESET OUTPUT

This bit reflects the state of the disable reset output control bit defined in the drive interface control register.

3.7.14.7 BIT 1 INPUT POLARITY

This bit reflects the state of the input polarity control bit defined in the drive interface control register.

3.7.14.8 BIT 0 DISABLE SECTOR NUMBER

This bit reflects the state of the disable sector number control bit defined in the drive interface control register.

3.7.15 DRIVE INTERFACE CONTROL (AD7 THRU AD0 = 3B, WRITE)

This register is used to control the drive controller. It is coded as follows:

Bit							
7	6	5	4	3	2	1	0
RDC	X	X	X	MAC	DRQ	IPOL	DSN

3.7.15.1 BIT 7 RESET DRIVE CONTROLLER

When this bit is asserted, then the drive controller subsection of the WD42C22C resets. It is held reset as long as the bit is asserted. This bit is reset when $\overline{\text{RESET}}$ is asserted.

3.7.15.2 BIT 3 MICROCONTROLLER ACCESS CONTROL

When this bit is set, the microcontroller is tied to the buffer RAM through the disk controller's port. The microcontroller can then read or write the buffer by reading from or writing to the RAM access port (36_{16}). The DRWB bit in the buffer manager control port should be set to the proper

state before this bit is set. When MAC = 1, then the disk controller task file (registers 21_{16} through 27_{16}) cannot be accessed by the microcontroller. If the microcontroller writes to these registers when MAC = 1, then the disk controller may not act properly. This bit resets when RESET is asserted. The proper sequence for the microcontroller to read/write the RAM is defined under the buffer manager description.

3.7.15.3 BIT 2 DISABLE RESET OUTPUT

When this bit is set, all host initiated soft resets are disabled. Instead of the RESET line being asserted on soft reset, only the MCINT line is asserted. It is the responsibility of the local microcontroller to properly reset the board hardware when this bit is set. This bit resets only during power-up.

3.7.15.4 BIT 1 INPUT POLARITY

This bit is used to control the polarity of the INDEX, SCT, WF, and DRDY inputs. If IPOL= 0, the default, then the inputs are active low. If IPOL = 1, then the inputs are active high. In soft sector MFM and RLL modes, DRUN is always active high regardless of the state of IPOL.

3.7.15.5 BIT 0 DISABLE SECTOR NUMBER

When this bit is set, then the drive controller does not compare the sector number coming from the drive with the desired sector number when reads or writes are performed. The drive controller instead writes the sector number coming from the drive into the sector number register in the drive controller task file. At the end of each sector, just prior to issuing DRQI or DCI, the drive controller always writes the sector number to the alternate sector number register. This bit resets when RESET is asserted.

3.7.16 ALTERNATE SECTOR NUMBER (AD7 THRU AD0 = 3C, READ)

When the disk controller interrupts the microcontroller, this register holds the sector number of the sector just read or written. It is always updated just prior to the disk BDRQ interrupt (DRQI) or the disk controller interrupt (DCI). It is initialized to FF_{16} at the start of every command. It is written regardless of the state of the DSN bit described above.

Bit							
7	6	5	4	3	2	1	0
NUMBER OF LAST SECTOR READ OR WRITTEN							

3.8 AT INTERFACE PORTS

3.8.1 AT CONTROL REGISTER (AD7 THRU AD0 = 2A, READ/WRITE)

This register controls the new auto-DRQ option for write, write long, and format commands.

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	ADQ7	ADRQ

3.8.1.1 BITS 7 THROUGH 2 RESERVED

Set to 0.

3.8.1.2 BIT 1 AUTO-DRQ 7 BYTE ECC

When ADRQ = 1 and ADQ = 1, then 7 ECC bytes are transferred to/from the host on a read long or write long command. When ADRQ = 1 and ADQ7 = 0, then 4 ECC bytes are transferred to/from the host on a read long or write long command. When ADRQ = 0, then the ECC7 bit in the fixed disk register ($3F_{16}$) controls the number of ECC bytes transferred on read long and write long commands.

3.8.1.3 BIT 0 AUTO-DRQ ENABLE

When ADRQ = 1 in AT mode, then the WD42C22C automatically sets up the first data transfer from the host for write, write long, and format commands. When ADRQ = 0, the local microcontroller must set up all data transfers to/from the host for all commands.

3.8.2 DRIVE ZERO STATUS (AD7 THRU AD0 = 3D, READ/WRITE)

In PC/AT mode, bits 6, 5, 4, 2, and 0 of the host status register are controlled by the local microcontroller. Bits 6, 5, 4, 2, and 0 of the host status register are set to the values of bits 6, 5, 4, 2, and 0, respectively, of this register if bit 4 of the AT task file copy SDH register (port 46 for microcontroller, port 6 for host) is 0. The other bits of the host status are not affected by this register.

33

3.8.3 DRIVE ONE STATUS (AD7 THRU AD0 = 3E, READ/WRITE)

In AT mode, bits 6, 5, 4, 2, and bit 0 of the host status register are controlled by the local microcontroller. Bits 6, 5, 4, 2, and 0 of the host status register is set to the values of bits 6, 5, 4, 2, and 0, respectively, of this register if bit 4 of the AT task file copy SDH register (port 46 for microcontroller, port 6 for host) is 1. The other bits of the host status are not affected by this register.

3.8.4 FIXED DISK REGISTER (AD7 THRU AD0 = 3F, READ)

This register contains the fixed disk register data written by the host.

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	HS3EN	RST	$\overline{IEN}$	0

3.8.5 DIGITAL INPUT REGISTER (AD7 THRU AD0 = 3F, WRITE)

Bit 5 of this register is written by the local microcontroller and read by the host if the fixed disk register bit 3 is zero. This bit is inverted when this register is read by the host. If HS3EN is one, then bit 5 of this register comes from SDH register bit 3.

Bit							
7	6	5	4	3	2	1	0
ECCM	ECC7/ DDRQ	RWC	X	X	X	DS1	DS0

3.8.5.1 BIT 7 ECC MODE

In PC/AT mode, ECCMOD = 1 indicates that the data transferred to the host includes ECC. The ECC is transferred in bytes rather than in words. This bit is reset when $\overline{RESET}$ is asserted. This bit should not be set in XT or slave host modes.

3.8.5.2 BIT 6 ECC 7 BYTES/ DISABLE BDRQ

When ECCM = 1, then this bit determines the number of ECC bytes transferred to the host. If ECC7 = 1, then 7 bytes are transferred. Otherwise, 4 bytes are transferred. If ECCM = 0, then this bit controls whether or not the drive controller issues BDRQ interrupts. If DDRQ = 0, then the drive controller issues BDRQ interrupts. If DDRQ = 1, then the drive controller does not issue BDRQ interrupts. It should be noted that when BDRQ occurs, the buffer manager loads the disk pointer from its pipeline register and when no BDRQ occurs then the disk pointer keeps incrementing from one sector to the next. This bit resets when $\overline{RESET}$ is asserted.

3.8.5.3 BIT 5 REDUCE WRITE CURRENT

This bit is set by the microcontroller and indicates the state of the $\overline{RWC}$ signal going to the drive.

3.8.5.4 BIT 1 DRIVE SELECT 1

This bit controls the state of the $\overline{DS1}$ output pin. When DS1 = 0, then the $\overline{DS1}$ output is tri-stated and when DS1 = 1 the $\overline{DS1}$ output is low. This bit is reset when $\overline{RESET}$ is asserted.

3.8.5.5 BIT 0 DRIVE SELECT 0

This bit controls the state of the $\overline{DS0}$ output pin. When DS0 = 0, then the $\overline{DS0}$ output is tri-stated and when DS0 = 1 the the $\overline{DS0}$ output is low. This bit is reset when $\overline{RESET}$ is asserted.

3.8.6 AT TASK FILE COPY (AD7 THRU AD0 = 40 THRU 47, READ/WRITE)

These registers are a copy of the disk controller task file. They are loaded by the host prior to the start of a command. The local microcontroller must read the command and interpret it and then copy the appropriate parameters from this task file copy to the actual drive controller task file (20_{16}-27_{16}). At the end of the command, the local microcontroller must update this task file copy before asserting INTRQ and resetting ABSY. The local microcontroller can only access these registers when ABSY=1.

4.0 BUFFER MANAGER ORGANIZATION

The buffer manager can control multiple sector buffers totalling up to 32 Kbytes. The buffer interface requires static RAMs. The sector buffers can be any size up to 2055 bytes, including ECC, and can be located at any byte boundary. The buffer manager has two address counters, one for the host interface and one for the disk data buffer. Both counters can access the SRAM simultaneously. The buffer manager handles the arbitration between the host interface and the drive controller. There is a FIFO in the host data interface that allows a sustained bandwidth of 4 Mwords/sec (8 Mbytes/sec) for 16-bit wide transfers and 8 Mbytes/sec for 8-bit wide transfers. The buffer manager can sustain a RAM bandwidth of 10 Mbytes/sec.

When the local microcontroller wants to access the buffer RAM, it has to use the disk buffer manager logic. It first loads the desired starting address into the disk buffer pointer. The proper buffer manager control bits are then set to enable the local microcontroller access to the buffer. When the local microcontroller accesses the special RAM access port (register 36_{16}), the data is read/written through the disk controller's FIFO port to the buffer. The RAM can only be accessed sequentially from the starting address and only in one direction as set by the DRWB control bit in the buffer control register.

Both address counters are pipelined. There are registers that can be loaded with the starting address of the next sector buffer while the current buffer is transferring. This allows noncontiguous buffers to be chained without any loss of RAM bandwidth between sectors.

4.1 ACCESSING BUFFER RAM FROM THE MICRO-CONTROLLER

The microcontroller can read and write the buffer RAM. To read the buffer RAM the procedure is:

1. Set DRWB = 1 (bit 2) in the buffer manager control Register (37_{16}).
2. Set MAC = 1 (bit 3) in the disk controller control register ($3B_{16}$).
3. Load the starting address of the data being accessed into the disk buffer pointer registers (34 & 35_{16}).
4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).

The buffer manager begins reading data out of the RAM starting at the address specified in the disk pointer register and placing it into the FIFO. As the microcontroller reads from the RAM access port (36_{16}), sequential bytes from the buffer are transferred from the FIFO to the microcontroller.

The procedure to write to the buffer RAM is:

1. Set DRWB = 0 (bit 2) in the buffer manager control register (37_{16}).
2. Set MAC = 1 (bit 3) in the disk controller control register ($3B_{16}$).
3. Load the starting address of the data being accessed into the disk buffer pointer registers (34 & 35_{16}).
4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).

As the microcontroller writes data to the RAM access port (36_{16}), the buffer manager transfers the bytes to sequential locations in the buffer RAM starting at the address specified in the disk pointer register.

NOTE

DRWB should not be changed while MAC = 1.

33

4.2 STARTING HOST TRANSFERS TO/FROM BUFFER RAM

Host transfers can be performed in several modes. The modes available and the setup required to establish each mode are as follows:

HDMA	BDEN	BCNT	H16/8-
1	0	X	0
8-bit wide single byte DMA			
1	0	X	1
16-bit wide single word DMA			
1	1	0	0
8-bit wide, 8-byte burst DMA			
1	1	0	1
16-bit wide, 16-byte burst DMA			
1	1	1	0
8-bit wide, continuous burst DMA			
1	1	1	1
16-bit wide, continuous burst DMA			
0	X	X	0
8-bit wide PIO			
0	X	X	1
16-bit wide PIO			

Bits HDMA (bit 7), BCNT(bit 5), and H16/$\overline{8}$ (bit 1) are in the auxilliary buffer manager control register ($2F_{16}$) and bit BDEN (bit 1) is in the buffer manager control register (37_{16}). All of these modes are available in both the XT and AT host configurations. All of the DMA modes are available in the slave host configuration.

To perform a Host read data transfer the following sequence should be followed.

1. Set up the appropriate transfer mode as described above.
2. Set HRWB = 1 (bit 3) in the buffer control register (37_{16}).
3. Load the starting address of the desired sector into the host pointer registers (30_{16} & 31_{16}). Load the number of bytes into the host transfer count registers (32_{16} & 33_{16}).
4. Set AHBP = 1 (bit 4) in the buffer manager control register (37_{16}). Hardware automatically sets DRQ (bit 3) and resets ABSY (bit 7) in the host status register if AT mode and sets REQ (bit 0) in the hardware status register if XT mode. If DMA transfers are enabled, then the hardware automatically starts the DMA handshake when AHBP is set by the micro-controller.
5. Wait for HPRI = 1 (bit 2) in the interface status register (38_{16}). $\overline{\text{MCINT}}$ is asserted.
6. Set RHRI = 1 (bit 2) in the interface control register (38_{16}) to reset the interrupt. If chaining and still more sectors then go to 3.
7. Wait for HPRI = 1 (bit 2) in the interface status register (38_{16}). $\overline{\text{MCINT}}$ is be asserted.
8. Set RHRI = 1 (bit 2) in the interface control register (38_{16}) to reset the interrupt. If still more sectors, then go to 3.
9. Set RBSY = 1 (bit 3) in the interface control register when the entire command sequence is complete. This resets the ABSY and XBSY host status bits. They stay reset until the next command is issued by the host.

To perform a host write data transfer, the following sequence should be followed.

1. Set up the appropriate transfer mode as described above.
2. Set HRWB = 0 (bit 3) in the buffer control register (37_{16}).
3. Load the starting address of the desired sector into the host pointer registers (30_{16} & 31_{16}). Load the number of bytes into the host transfer count registers (32_{16} & 33_{16})
4. Set AHBP = 1 (bit 4) in the buffer manager control register (37_{16}). Hardware automatically sets DRQ (bit 3) and resets ABSY (bit 7) in the host status register if AT mode and set REQ (bit 0) in the hardware status register if XT mode. If DMA transfers are enabled, then the hardware automatically starts the DMA handshake when AHBP is set by the micro-controller.
5. Wait for HPRI = 1 (bit 2) in the interface status register (38_{16}). $\overline{\text{MCINT}}$ is asserted.

6. Set RHRI = 1 (bit 2) in the interface control register (38_{16}) to reset the interrupt. If chaining and still more sectors then go to 3.

7. Wait for second HPRI = 1 (bit 2) in the interface status register (38_{16}). $\overline{\text{MCINT}}$ is asserted.

8. Set RHRI = 1 (bit 2) in the interface control register (38_{16}) to reset the interrupt. If still more sectors then go to 3.

9. Set RBSY = 1 (bit 3) in the interface control register when the entire command sequence is complete. This resets the ABSY and XBSY host status bits. They stay reset until the next command is issued by the host.

4.3 CONTROLLER COMMANDS

The WD42C22C Winchester command set contains twelve commands. Four commands (read sector, write sector, format, and set parameter) are directly executed through the command register. The remaining commands are not directly available to the host. These commands may be executed by the local microcontroller transparently to the host. Table 12 lists the commands and command codes.

COMMAND	7	6	5	4	3	2	1	0
Read Sector	0	0	1	0	0	M	L	T
Read Next Data	0	1	1	0	0	0	L	1
Write Sector	0	0	1	1	X	M	L	T
Write ID	1	0	1	1	F	0	A	T
Scan ID	0	1	0	0	0	0	0	T
Format Track	0	1	0	1	0	0	W	1
Format Single Sector	1	1	0	1	0	0	W	1
Compute Correction	0	0	0	0	1	P	0	0
Set Parameter	Z	0	0	R	0	E	H	S
Load Parameter Block	1	0	0	0	1	D	K	U
Sleep	1	0	0	1	1	0	0	0
Dump	1	0	1	0	I	B	L	1

TABLE 12. COMMAND AND COMMAND CODES

Mnemonic definitions for Table 12:

- M=0 Single sector read or write. Sector count is ignored.
  M=1 Multiple sector read or write. Used for 1:1 interleave.
- L=0 Normal mode, selected ECC or CRC functions performed.
  L=1 Sector extended by 4 or 7 bytes (depends on set parameter command. No ECC generated or checked.
- T=0 Enable retries.
  T=1 Disable retries.
- X=0 Write sector specified in sector number register.
  X=1 Write sector specified in first byte of the sector buffer.
- F=0 Write new ID immediately after current ID.
  F=1 Write new ID offset from current ID.
- A=0 Do not pulse AME when writing new ID.
  A=1 Pulse AME when writing new ID.
- W=0 Write gate stays asserted for entire track or sector.
  W=1 Write gate deasserted over all gaps during format.
- P=0 Transfer syndrome bytes to buffer and calculate error pattern bytes and transfer them to the buffer.
  P=1 Transfer syndrome bytes to the buffer but do not calculate error pattern bytes.
- Z=0 MFM or RLL mode.
  Z=1 NRZ mode. Mode used for ESDI drive interface.
- R=0 Disable relocation ID searches.
  R=1 Enable relocation ID searches.
- E=0 Sector extension for read long/write long 4 bytes. ECC generator/checker is 4 bytes.
  E=1 Sector extension for read long/write long 7 bytes. ECC generator/checker is 7 bytes.
- H=0 SDH register programmed for 3 head select bits.
  H=1 SDH register programmed for 4 head select bits.
- S=0 Error correction span 5 bits with 4 byte ECC or 11 bits with 7 byte ECC.
  S=1 Error correction span 11 bits with 4 byte ECC or 22 bits with 7 byte ECC.
- D=0 Select soft sector drive interface. Default after master reset.
  D=1 Select hard sector drive interface. In

33

MODE	MODE CONTROL			OPTIONS														
	Z	D	K	M	T	L	X	A	F	R	S	E	H	P	U	W	I	B
RLL soft sector	?	0	0	x	x	x	x	x	x	x	x	*	x	x	x			
RLL hard sector	?	1	0	x	x	x	x	x	x	x	x	*	x	x	x	x	x	x
MFM soft sector	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x			
MFM hard sector	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
NRZ soft sector	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x			
NRZ hard sector	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

? Don't care, could be 0 or 1.
x These options are supported.
* These options have no effect.

TABLE 13. OPTION SUMMARY TABLE

this mode, DRUN becomes a sector pulse input.

- K=0 RLL data interface. Selection of this option disables the NRZ option. Defaults to this setting after master reset.

  K=1 Data interface is either MFM or NRZ.

- U=0 Use the standard sector sizes defined under the SDH register description.

  U=1 Select user defined sector size. The desired sector size is put into the cylinder registers prior to issuing a load parameter block command. The auxilliary set parameter command transfers the desired sector size from the cylinder registers to an internal sector size register.

- I=0 Dump two fields per sector. Dump 5 ID bytes and the number of data bytes set by the sector size.

  i=1 Dump only one field per sector. The sizeof the field is set by the sector size and type of field (ID versus data) is controlled by where RG is asserted.

- B=0 FE sync byte and zero preset CRC.

  B=1 A1 sync byte and ones preset CRC.

Table 13 summarizes the data formats and options supported by these formats.

4.4 COMMAND DESCRIPTIONS

4.4.1 READ SECTOR

If M = 0, then the sector specified in sector number register is read. If M = 1, then multiple records are read. If the sector count register = 0, then 256 sectors are read at the desired track.

If T=0, then ID searches are retried for 10 index pulses. DAM not found errors are not retried. There are no retries for CRC/ECC errors. If T=1, ID searches are retried for two index pulses.

If L=0, then normal CRC or ECC read commands are performed. If L=1, then the CRC or ECC check bytes are not computed but instead the CRC or ECC check bytes are loaded into the buffer immediately after the data field. The external sector buffer must be long enough to hold the additional 4 or 7 bytes. If ECC and retry modes have been selected and a data field error occurs there are no attempts to correct the data.

A bad block mark in the ID field sets the error bit and the data field is not read. If the R option in the set parameter command is set then the controller searches immediately after the normal ID field for a special ID field containing mapping information and a special "Relocation ID" flag bit. The RIDF bit in the error register sets if this special ID field is found. If a bad block mark is found in an ID field then the command terminates immediately

even if more sectors remain to be read. The task file contents when a bad block bit is detected and the R option is used is as follows:

REGISTER	MEANING
22	Sector number of sector with bad block bit set
23	Sector umber where sector has been relocated
24	LSB of cylinder number where sector has been relocated
25	MS bits of Cylinder where sector has been relocated
26	Head number of relocated sector

If DSN = 1 (bit 0) in the drive interface control register ($3B_{16}$) than the sector number is not compared when ID searches are performed. The WD42C22A reads the sector as long as the cylinder and head numbers match the desired values. This allows an interleaved track to be read into the buffer in one revolution.

Command Flow:

- MICRO:
  1. Set DRWB = 0 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the first sector into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC=1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC = 0 in the drive interface control register.
  6. Issue read command to WD42C22C.
- WD42C22C:
  7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.
- MICRO: Load starting address of next sector buffer into disk buffer pointer register. Set ADBP=1 in buffer manager control register if more sectors remaining. Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Search for head, cylinder, sector number, and sector size code.
  10. When the proper sector ID is found, read sector data and place in buffer.
  11. Write sector number to alternate sector number register. If M = 0, then go to 10.
  12. Decrement sector count, increment sector number. If M = 1, and sector count = 0 then go to 13 else go to step 8.
  13. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO:
  14. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- ID not found set if ID field not found or if ID field matches, but CRC check fails, and after retry procedure.
- Bad block set if attempt was made to read a sector with bad block mark.
- Relocation ID found if R option enabled and relocation ID detected.
- Data CRC/ECC set if data field CRC or ECC check fails. No attempt is made to correct ECC errors.
- Data AM not found in set if data address mark not found.

33

4.4.2 READ NEXT DATA

The read next data command finds the next data field and places it in a buffer. If the WD42C22C detects that the drive number changed since the last read command, then an auto-scan ID is performed and step pulses are issued to update the present cylinder position.

All searches for a data field are retried for two index pulses, but if a data ECC error is detected there are no retries. If after reading the correct ID field, the data address mark is not found a DAM error is set.

The L flag controls the ECC check bytes. If L=0, then the data field is read and ECC is checked. If L=1, then the ECC check bytes are not computed. Instead, the ECC check bytes are loaded into the buffer immediately after the data field. The external sector buffer must be long enough to hold the additional 7 bytes.

NOTE

This command supports only soft sector MFM and RLL mode and is implemented for backward compatibility with the WD5011 and WD5011A.

Command Flow :

- MICRO:
  1. Set DRWB = 0 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the first sector into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
  4. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC=1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  5. Set MAC=0 in the drive interface control register.
  6. Issue read next data command to WD42C22C.
- WD42C22C:
  7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Set DRQ status bit, activate BDRQ signal to buffer manager. Wait for BRDY signal indicating transfer of buffer pointer.
- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Find next data field, read sector data and place in buffer. If data mark error, try data field search again until 2 index pulses occur.
  10. Copy sector number register to alternate sector number register ($3C_{16}$). Set DCI (bit 3) in the interface status register (38_{16}). MCINT is asserted.
- MICRO:
  11. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- Data CRC/ECC set if data field CRC or ECC check fails. No correction is attempted.
- Data AM not found is set if data address mark not found after 2 index pulses of looking for any data field.

4.4.3 WRITE SECTOR

Write from buffer to disk when BRDY signal is activated by the buffer manager. Write total number of sectors specified by sector count register if M = 1. Sectors are written in numerical order. If M = 0, then sector count is ignored and only one sector is written. The data field PLO sync field is nominally 12 bytes long but is extended by the PLO register.

If T = 0, then ID searches are retried for 10 index pulses. If T = 1, then ID searches are retried for 2 index pulses only.

If L = 0, then normal CRC or ECC write sector commands are performed. If L = 1, then the CRC or ECC check bytes are not computed and written

to the disk but instead, 4 or 7 additional bytes are read from the buffer and written to the disk immediately after the data field.

If X = 0, then the controller searches for the sector number in the sector number register and increments the sector number register and the end of each sector if M = 1. If X = 1, then the controller searches for the sector specified in the first byte of the sector buffer. The controller reloads the sector number register from the first byte of each subsequent sector buffer if M = 1. This allows a track formatted with interleave to be written in one revolution.

A bad block mark in the ID field sets the error bit and the data field is not be written. If the R option in the set parameter command is set, then the controller searches immediately after the normal ID field for a special ID field containing mapping information and a special "Relocation ID" flag bit. The RIDF bit in the error register sets if this special ID field is found. If a bad block mark is found in an ID field then the command terminates immediately even if more sectors remain to be read. The task file contents when a bad block bit is detected and the R option is used is as follows:

REGISTER	MEANING
22	Sector number of sector with bad block bit set
23	Sector number where sector has been relocated
24	LSB of cylinder number where sector has been relocated
25	MS bits of cylinder where sector has been relocated
26	Head number where sector has been relocated

If DSN = 1(bit 0) in the drive interface control register ($3B_{16}$) then the sector number is not compared when ID searches are performed. The WD42C22C writes the sector as long as the cylinder and head numbers match the desired values. This allows an interleaved track to be written into the buffer in one revolution. This option is only useful when doing the initial write-after-format to place 00 in the data fields.

Command Flow:

- MICRO:
  1. Set DRWB = 1 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the first sector into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC = 1 (bit 3) in the drive register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP=1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC = 0 in the drive interface control register.
  6. Issue write command to WD42C22C.
- WD42C22C:
  7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQ is enabled.) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.
- MICRO: Load starting address of next sector buffer into disk buffer pointer register. Set ADBP=1 in buffer manager control register if more sectors remaining. Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Search for head, cylinder, sector number and sector size code.
  10. When the proper sector ID is found, write buffer data to sector.
  11. Write sector number to alternate sector number register ($3C_{16}$). If M = 0 then go to 13.
  12. Decrement sector count, increment sector number. If M = 1 and sector count = 0

33

then go to 13 else go to step 8.

13. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.

• MICRO:

14. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- ID not found set if exact ID field not found or if ID field matches but CRC check fails, after retry procedure.
- Bad Block set if write sector attempted on any sector with bad block mark.
- Relocation ID found if R option enabled and relocation ID detected.

4.4.4 WRITE ID

Write from buffer to disk when BRDY signal is activated by the buffer manager. Write 4 bytes to create an ID field. The PLO sync field prior to this new ID field is nominally 12 bytes long but is extended by the PLO register. A value of 0 results in a 2048 byte PLO field and should not be used.

If T = 0 then ID searches are retried for 10 index pulses. If T = 1, then ID searches are retried for 2 index pulses only.

If F = 0, then the new ID is written immediately after the ID field of the desired sector. If F = 1, then the new ID field is written offset from the desired sector ID with the offset determined by the internal sector size register. A load parameter block command will have to be issued to set the offset value and another load parameter block will be needed to set the sector size back to the correct value if the programmable sector size option is being used. An offset of up to 2048 is allowed. This option can be used to reformat a single sector in soft sector mode.

If A = 0, then the AME output is held low during the write ID command. If A = 1, then the AME output is pulsed at the start of the PLO field before the new ID being written. This option, together with the F option, can be used to reformat a single sector in soft sector NRZ mode.

The four bytes in the buffer (F = 0) should be as follows:

BYTE 0: 1 1 1 1 $\overline{\text{cyl 10}}$ 1 $\overline{\text{cyl 9}}$ cyl 8

BYTE 1: Low byte of cylinder number

BYTE 2: BB 0 RF 0 HS3 HS2 HS1 HS0

BYTE 3: Sector Number

BB = bad block flag

RF = Relocation ID flag

$\overline{\text{cyl 10}}$ thru cyl 8 = upper three cylinder number bits

HS3 thru HS0 = head select bits

The five bytes in the buffer (F = 1) should be as follows:

BYTE 0: Sector Number

BYTE 1: 1 1 1 1 $\overline{\text{cyl 10}}$ 1 $\overline{\text{cyl 9}}$ cyl 8

BYTE 2: Low byte of cylinder number

BYTE 3: BB 0 RF 0 HS3 HS2 HS1 HS0

BYTE 4: Sector Number

BB = bad block flag

RF = Relocation ID flag

$\overline{\text{cyl 10}}$ thru cyl 8 = upper three cylinder number bits

HS3 thru HS0 = head select bits

RF should be set to 1 if the new ID being written is to be a special relocation ID for mapping a defective sector to a new position.

Command Flow:

• MICRO:

1. Set DRWB = 1 (bit 2) in the buffer manager control register (37_{16}).
2. Load the starting address of the ID buffer data into the disk buffer pointer registers (34_{16} & 35_{16}).
3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC = 1 (bit 3) in the drive

interface control register ($3B_{16}$) to disable DRQI, if desired.

4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
5. Set MAC = 0 in the drive interface control register.
6. Issue Write ID command to WD42C22C.

• WD42C22C:
7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.

• MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).

• WD42C22C:
9. Search for head, cylinder, sector number and sector size code.
10. When the proper sector ID is found, write buffer data to sector.

• WD42C22C:
11. Write sector number to alternate sector number register. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.

• MICRO:
12. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write Fault and aborted command set if WF pin activated.
- ID not Found set if exact ID field not found or if ID field matches but CRC check fails, after retry procedure.
- Bad Block set if bad block bit detected in ID of desired sector.

4.4.5 SCAN ID

When the next ID field of the present track is encountered, cylinder number, sector size, head number and sector number are loaded into the respective registers.

Command Flow:

• MICRO:
1. Issue Scan ID command to WD42C22C.

• WD42C22C
2. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
3. Search for next ID field and read 4 ID bytes into respective registers. Search for ID field for up to 10 index pulses if T=0, up to 2 index pulses if T=1.
4. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.

• MICRO:
5. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin active.
- Bad Block set if bad block mark detected.
- ID not found if no ID fields are found.
- Relocation ID found if R option enabled and relocation ID detected.

33

4.4.6 FORMAT TRACK

This command formats one track using parameters loaded in the task registers file and in buffer memory.

Cylinder, head, and sector size numbers are taken from the task register file. Good block/bad block marks and sector numbers are taken from buffer memory. The total number of sectors formatted is specified by the sector count register. The lengths of GAP 1 and GAP 3 are loaded into the sector number register. The length of the ID PLO sync field is loaded into the PLO length register if B = 1. The data PLO field length is 12 bytes during format.

The data placed in the gaps comes from an internal register loaded during the load parameter

block command. The data placed into the pads comes from another internal register loaded during the load parameter block command.

After the task register file has been loaded with the desired format parameters and the block marks and sector addresses have been loaded into the buffer then the command register is loaded with the format command. When the BRDY signal is activated by the buffer manager, the specified number of sectors are written. The block marks and sector numbers are read from the buffer as needed. The data field is written with FF. CRC is automatically computed and written if in CRC mode. If in ECC mode, ECC check bytes are automatically computed and written after the data field. The number of ECC check bytes is determined by the E bit in the set parameter command.

Write Gate is turned on and off within 4 bit times after index if NRZ or hard sector mode is selected or within 6 bit times otherwise. In RLL mode, Gap1/Gap3 data should be programmed to be 33_{16} with the load parameter command. The W option controls the state of WRITE GATE over the gaps. If W=1, WRITE GATE turns off over the gaps.

The sum of the number of bytes in both the Gap1/Gap3 and ID PLO field must be greater than or equal to 25 bytes to achieve 1:1 interleave.

The interleave table contains the bad block marks and sector numbers for the track. If there is a bad sector and it is desired for the controller to just skip over it, then the bad block mark for that sector position should be set to 80_{16} and the sector number for that sector should be set to FF_{16}. If it is desired to map the bad sector then the bad block mark for that sector should be set to 80_{16} and the sector number for that sector should be set to the correct value for that position in the interleave table. The R and U options should be set in the set parameter and load parameter block commands. A write ID command then places the relocation information for that sector onto the drive.

The interleave table format is:

- BYTE 0: 1st sector's block mark (00_{16} or 80_{16})
- BYTE 1: 1st sector's sector number
- BYTE 2: 2nd sector's block mark (00_{16} or 80_{16})
- BYTE 3: 2nd sector's sector number

.
.
.

- BYTE 2n: nth sector's block mark (00_{16} or 80_{16})
- BYTE 2n+1: nth sector's sector number

Command Flow:

- MICRO:
  1. Set DRWB = 1 (bit 2) in the buffer manager control register (37_{16})
  2. Load the starting address of the interleave table into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC = 1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC = 0 in the buffer control register.
  6. Issue format command to WD42C22C.
- WD42C22C:
  7. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer. Wait for leading edge of index.
- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Write gap.
  10. Write sector ID using parameters in task register file

and buffer memory. Data bytes are FF.

11. Decrement sector count register. If sector count = 0, then go to step 12, else go to step 9.
12. Write Gap until leading edge of index pulse.
13. De-assert Write Gate.
14. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.

- MICRO: 15. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.

Note

Gap length written on disk is 3 bytes longer than gap value specified in sector number register.

4.4.7 FORMAT SINGLE SECTOR

This command formats one sector using parameters loaded in the task register file and in buffer memory. This command only applicable to hard sector mode.

WRITE GATE is turned on and off within 4 bit times after index or sector if NRZ mode is selected or within 6 bit times otherwise. The W option controls the state of WRITE GATE over the gaps. Setting W to 1 turns off WRITE GATE over the gaps.

Cylinder, head, and sector size numbers are taken from the task register file. Good block/bad block marks and sector number are taken from buffer memory. The physical sector position to be formatted is specified by the sector count register. If sector count = 1, then the first sector after index is formatted. For sector count = 2, the second sector after index is formatted, and so on. The lengths of GAP 1 and GAP 3 are loaded into the sector number register. The length of the ID PLO sync field is loaded into the PLO length register.

The data placed in the gaps comes from an internal register loaded during the load parameter block command. The data placed into the pads comes from another internal register loaded during the load parameter block command.

After the task register file has been loaded with the desired format parameters and the block marks and sector number loaded into the buffer, then the command register is loaded with the format single sector command. When the BRDY pin is activated by the buffer manager, the controller then looks for the start of the desired sector. The bad block mark and sector number are read from the buffer. The data field is written with FF. CRC is automatically computed and written if in CRC mode. If in ECC mode, ECC check bytes are automatically computed and written after the data field. The number of ECC check bytes is determined by the E bit in the set parameter command.

The data for the buffer is:

- BYTE 0: bad block mark (00_{16} or 80_{16})
- BYTE 1: sector number of formatted sector.

Command Flow:

- MICRO:
  1. Set DRWB = 1 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the interleave table into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ECCM=0 (bit 7) and DDRQ =1 (bit 6) in the DIR write register ($3F_{16}$) and MAC=1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC=0 in the drive interface control register.
  6. Issue format single sector command to WD42C22C.
- WD42C22C:
  7. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buff-

33

er manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer. Wait for leading edge of index.

- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C: 9. Decrement sector count. If sector count = 0 go to 11, else go to 10.
  10. Wait for SECTOR pulse, then go to 9.
  11. Assert WRITE GATE. Write gap.
- WD42C22C:12. Write sector ID using parameters in task register file and buffer memory. Data bytes are FF.
  13. Write gap until leading edge of SECTOR pulse.
  14. De-assert Write Gate.
  15. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO: 16. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.

4.4.8 COMPUTE CORRECTION

This command is used to compute the pattern and location of a single burst error. It is used after a read sector command has detected a data field ECC error. The compute correction command first writes the four or seven syndrome bytes into the buffer. It then processes the syndrome bytes to compute the error pattern and error location. The error location and error pattern bytes are written into the buffer. Either four or seven error pattern bytes are written to the buffer depending on the ECC length selected. The error pattern bytes are automatically byte aligned.

The P option is used to control whether or not the error pattern bytes are calculated. If P = 0, then the error pattern bytes are calculated and sent to the buffer. If P = 1, then the error pattern bytes are not calculated. Only the syndrome byte is transferred to the buffer. This option facilitates firmware algorithms that require a matching syndrome before a correction is made. In this case, the firmware calculates the error pattern, corrects the error, and saves the syndrome after initially detecting the error. Then, the firmware dumps and compares the syndrome on the second read of the same sector. An ECC error can now be corrected in one revolution of the disk compared to three revolutions required by earlier WD1010 and WD2010 based controllers.

The error pattern and error location bytes are not valid if the error is found to be uncorrectable. An uncorrectable error is indicated by the appropriate bits in the status and error register.

The buffer contents contains the following information:

- SYNDROME BYTE (MSB)
- SYNDROME BYTE
- SYNDROME BYTE
- SYNDROME BYTE (LSB if 4 byte ECC)
- SYNDROME BYTE (if 7 byte ECC)
- SYNDROME BYTE (if 7 byte ECC)
- SYNDROME BYTE (LSB if 7 byte ECC)
- BYTE OFFSET (MSB)
- BYTE OFFSET (LSB)
- ERROR PATTERN (MSB)
- ERROR PATTERN
- ERROR PATTERN
- ERROR PATTERN (LSB if 4 byte ECC)
- ERROR PATTERN
- ERROR PATTERN
- ERROR PATTERN (LSB if 7 byte ECC)

If the byte offset is 0, then the first data byte of the sector should be exclusive OR'ed with the first error pattern byte (MSB). Each succeeding data byte exclusive OR'ed with the succeeding error pattern byte until the fourth data byte is exclusive OR'ed with the fourth error pattern byte (LSB). Exclusive OR the first two error pattern bytes for 5 bit spans. Exclusive OR the first three error pat-

tern bytes for 11 bit spans. Exclusive OR the first four error pattern bytes for the 22 bit span.

Command Flow:

- MICRO:
  1. Set DRWB=0 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the error correction data buffer into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ECCM=0 (bit 7) and DDRQ =1 (bit 6) in the DIR write register ($3F_{16}$) and MAC=1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP=1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC=0 in the drive interface control register.
  6. Issue compute correction command to WD42C22C.
- WD42C22C:
  7. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.
- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Transfer contents of the four (or seven) byte ECC register to buffer, most significant byte first.
  10. Clock the ECC register. Stop if correctable pattern found or if number of clocks exceeds sector size. If number of clocks exceeds sector size, set error bit of status register and ECC error of error register.
  11. Transfer byte count to buffer (2 bytes). Transfer 4 bytes of error pattern to buffer if 4 byte ECC. Transfer 7 bytes of error pattern 7 byte ECC.
  12. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO:
  13. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- CRC/ECC flag set if data field error length exceeds correction span.

NOTE

Default 11 bit correction span after master reset if 7-byte ECC or 5 bit correction span if 4-byte ECC.

4.4.9 SET PARAMETER

The E bit is used to select either 4 byte or 7 byte sector extension for read long and write long commands. It also selects either a 4 or 7 byte internally generated ECC. A 7 byte sector extension and 7 byte ECC are the default after a master reset (due to RLL default). If E is 0, then a 4 byte sector extension and 4 byte ECC are selected if MFM or NRZ mode. If E is 1, then a 7 byte sector extension and 7 byte ECC are selected.

The H bit selects either 3 or 4 head select bits in the SDH register. If H=0, then 3 head select bits are written or compared in the ID fields on the drive. If H=1, then 4 head select bits are written or compared in the ID fields on the drive. The default after master reset is 3 head select bits.

The S bit is used to select either a 5 bit or 11 bit correction span if 4 byte ECC and an 11 bit or 22 bit correction span if 7 byte ECC. An 11 bit correction span for 7 byte ECC is the default parameter following master reset. If S is 0, then a 5 bit correction span is selected if 4 byte ECC, 11 bit correction span if 7 byte ECC. If S is 1, then an 11 bit correction span is selected if 4 byte ECC, 22 bit correction span if 7 byte ECC.

The Z bit is used to select MFM, RLL, or NRZ mode. If K=0 in the load parameter block command, then RLL coding is selected regardless of the state of Z. If Z is 0 and K is 1, then MFM coding is selected. If Z is 1 and K = 1, then NRZ coding is selected.

The R option is used to enable relocation ID searches. If R=1 for read and write sector com-

mands and a bad block mark is detected in the desired sector's ID, then the WD42C22C searches for a special ID field containing relocation information immediately after the desired sector's ID. This special ID field is placed using the write ID command. When the R option is used, then the U option must be set to 1 in the load parameter block command.

Command Flow:

- MICRO: 1. Issue set parameter command to WD42C22C.
- WD42C22A: 2. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
3. Set or reset internal parameter flip-flop.
4. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO: 5. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- None.

4.4.10 LOAD PARAMETER BLOCK

The D bit is used to indicate the sectoring mode. If D = 0, the default after a master reset, then soft sector mode is selected. If D = 1, then hard sector mode is selected. In hard sector mode, the PLO length register is transferred to the internal GAP length register during the load parameter block command. This GAP register is used to control the delay from INDEX/SECTOR to READ GATE on.

The K bit selects the data interface mode. If K=0, the default after a reset, then RLL mode is selected. If K=1, then the interface is either MFM or NRZ as selected by the set parameter command.

The U bit selects the sector size options. If U=0, then the sector sizes are 128, 256, 512, and 1024 depending on the contents of the SDH register. If U=1, then the sector size is defined by the user. The cylinder registers are loaded with the desired sector size prior to issuing the load parameter block command.

In addition, the load parameter block command is used to load several internal parameters for format, read, and write commands. The task file is loaded with these parameters prior to the start of the command. The registers loaded and the corresponding parameters are:

REGISTER	PARAMETER
21	Delay from INDEX/SECTOR to RG
22	Data written in GAPS
23	Data written in PADS
24	LS byte of sector size, LS byte of offset for write ID command
25	3 MS bits of sector size, 3 MS bits of offset for write ID command

Command Flow:

- MICRO: 1. Load parameters into task file.
2. Issue load parameter block command to WD42C22C.
- WD42C22C: 3. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
4. Set or reset internal parameter flip-flop.
5. Copy cylinder registers to internal sector size register. Copy PLO register to internal GAP register. Copy sector count register to internal GAP data register. Copy sector number register to internal PAD data register.
6. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO: 7. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- None.

4.4.11 SLEEP

The sleep command places the WD42C22C in a low power standby mode. When the sleep command is issued, the disk controller section clocks are disabled and only the buffer manager and host interface logic is enabled. The disk controller can be brought out of the sleep mode by setting RDC = 1 (bit 7) in the disk controller control register ($3B_{16}$) or by resetting the entire WD42C22C. The microcontroller should **NEVER** attempt to read or write the drive controller task file (registers 21_{16} through 27_{16}) while the drive controller is in the sleep mode.

Command Flow:

- MICRO: 1. Issue sleep command to WD42C22C.
- WD42C22C: 2. Write FF to the alternate sector number register ($3C_{16}$).
  3. Disable drive controller clocks.
- MICRO: 4. Wake up disk controller by setting RDC=1 or by resetting the WD42C22C.

Error Flags:

- None.

4.4.12 DUMP

The dump command sends data off the media regardless of matching ID fields and regardless of the format. The command can dump an ID field, a data field, or both. Dump retrieves all the ID fields from index to index to determine the interleave. Dump can also read the ESDI standard defect list. The command dumps data starting at the first byte after the A1 sync byte for WD format or the first byte after the FE sync byte for ESDI format. This command can only do multisector dumps in hard sector mode.

The command is assumed to be a multisector command. To read just one sector as in an ESDI defect list read, then the sector count must be set to one. There are three options.

The I option controls the number of fields that are dumped for each sector. If I = 0, then two fields (ID and data) are dumped for each sector. If I = 1, then only one field is dumped for each sector. The type of field is determined by the read gate delay and the sector size. The sector size should be programmed to 1 less than the number of bytes to be dumped for the sector.

The B option controls the sync byte and CRC preset. If B = 0, then the sync byte is assumed to FE and the CRC is preset to all zeroes. If B = 1, then the sync byte is assumed to be A1 and the CRC is preset to all ones.

The L option selects either CRC or no CRC checking. If L = 0, then CRC is checked. If L = 1, then either four or seven check bytes are transferred to the buffer depending on the extension selected by the set parameter command. If L = 1, then I should also be set to 1. B does not affect the L option.

The PLO register controls the read gate delay for the first sector. READ GATE turns on x + 5 + CL bytes after the index pulse. Read gate for subsequent sectors is controlled as in normal read and write commands.

Use the dump command to read an ESDI defect list as follows:

1. Set PLO register = read gate delay - 5.
2. Set sector size = 255 for 256 byte sector.
3. Issue A1 command.

Use the dump command to dump the track interleave for WD format as follows:

1. Set PLO register = read gate delay - 5.
2. Set sector size = 4.
3. Set sector count = number of sectors per track.
4. Issue AD command.

Use the dump command to dump all the data fields on a track for WD format as follows:

1. Set PLO register = read gate delay to start of data PLO - 5.
2. Set sector size = actual number of bytes per sector.

33

3. Set sector count = number of sectors per track.

4. Issue AF command or AB command.

In this case, the F8 second data sync byte is transferred to the buffer. The buffer requires one extra byte per sector.

One BRDQ interrupt occurs at the very beginning of the command. Therefore, the buffer must be contiguous and large enough to handle all the dumped sectors.

Command Flow:

- MICRO:
  1. Set DRWB = 0 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the buffer into the disk buffer pointer register (34_{16} & 35_{16}).
  3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC = 1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC = 0 in the drive interface control register.
  6. Issue dump command to WD42C22C.
- WD42C22C
  7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY indicating transfer of buffer pointer.
- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Wait for index.
  10. If I=1, then go to 12 else go to 11.
  11. Search for sync byte. When found, dump 5 data bytes into buffer.
  12. Search for sync byte. When found, dump programmed number of bytes into the buffer.
  13. Decrement sector count. If sector count = 0, then go to 14 else go to step 10.
  14. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO:
  15. Read disk controller status register (27_{16}) and errror register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- ID not found set if I = 0 and index detected while searching for an ID field or if CRC of ID field doesn't zero.
- Data AM not found is set and index is detected while searching for a data field. If I=0 or when searching for either an ID or data field when I = 1.
- Data CRC if the data field CRC doesn't zero when I = 0 or if either an ID or data field CRC doesn't zero when I = 1.

5.0 ELECTRICAL AND TIMING SPECIFICATIONS

5.1 MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (ground) ..... +5 V ± 5%

Max voltage on any pin with respect to V_{SS} ..... -0.5V to 5.5

Operating temperature (T_A) ..... 0°C (32°F) to 70°C (158°F)

Storage temperature ..... -55°C (-67°F) to 125°C (257°F)

NOTE

Maximum limits where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

5.2 DC OPERATING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		±10	µA	V_{IN} = 0.4 to V_{CC}
I_{OZ}	Tri-state and open drain output leakage		±10	µA	V_{OUT} = 0.4 TO V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_{OUT}=-800µA
V_{OL}	Output Low Voltage		0.4	V	I_{OUT}=2.0mA
I_{CC}	Supply Current		100	mA	All outputs open.
I_{CCS}	Supply Current (Standby Mode)		25	mA	All inputs at V_{DD} or V_{SS}, disk controller sleep mode, 15 MHz crystal.

TABLE 14. DC OPERATING CHARACTERISTICS

For pins 75 thru 82, 40 thru 42, 44 thru 48, 74, 8 (HD0 thru HD15, INTRQ, DREQ):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		V	I_{OUT}=-5mA
V_{OL}	Output Low Voltage		0.4	V	I_{OUT}=12mA

For pin 8 ($\overline{IOCS16}$, AT PIO mode only):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.4	V	I_O=20.0mA

For pins 10, 11, and 12 (WD, EARLY, LATE):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4			I_O=-800µA
V_{OL}	Output Low Voltage		0.4	V	I_O=6.0mA

33

For pin 22 ($\overline{RESET}$)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.4	V	I_O=6.0 mA and VDD at spec. IO=2.0 mA and VDD at VRST2 max VRST3 max.

For pins 36, 37 ($\overline{DS0}$, $\overline{DS1}$):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.4	V	I_O=48.0 mA

For pins 59-73 (BA0-B14)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{PD}	Pulldown Current in read config. mode	40	160	µA	V_{OUT}=2.4V

For pins 5, 6, 9 ($\overline{HRE}$, $\overline{HWE}$, and $\overline{DACK}$ in slave host mode) and pins 40-42, 44-48 (HD8 through HD15 in 8-bit host mode):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{PU}	Pullup Current	100	2000	µA	V_{OUT}=0.4 V, V_{DD}=5.25 V

For pin 38 (XTALIN when driven by external osc.):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{IH}	Input High Voltage	3.5		V	
VIL	Input Low Voltage		1.0	V	

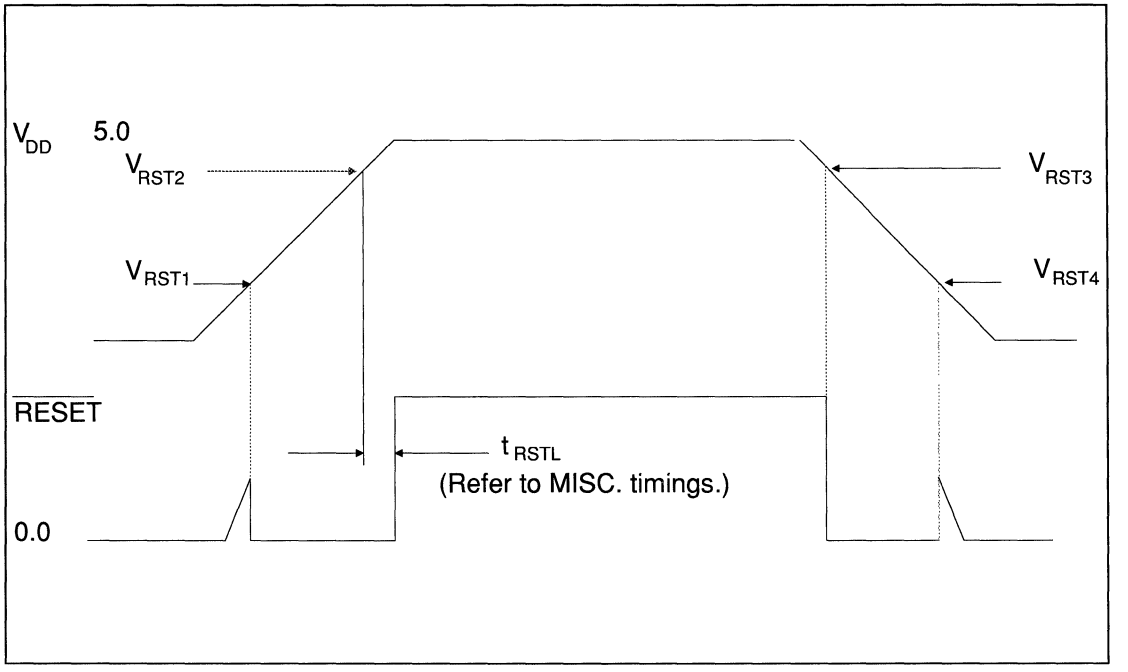


FIGURE 6. POWER QUALIFIED RESET VOLTAGE THRESHOLD

For pins 1-7, 9, 15, 16, 20, 21, 23, 25-35, 40-42, 44-48, 51-58, 59-73, 74, 75-82 (HA0-HA2, HA9, $\overline{HRE}$, HWE, HCS, DACK, INDEX, SCT, WF, DRDY, RESET, ALE, MRE, MWE, AD0-AD7, HD8-HD15, BD0-BD7, BA0-BA15, INTRQ, HD0-HD7)

33

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VIH / VIL	Input Voltage Hysteresis	400		mV	

For pin 84 (V_{DD})

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{RST1}	Power Qualified Reset Voltage Threshold	0.0	2.0	V	See Figure 7.
V_{RST2}		2.5	4.6	V	
V_{RST3}		2.5	4.6	V	
V_{RST4}		0.0	2.0	V	

5.3 AC TIMING CHARACTERISTICS

NOTE

Load capacitance=50 pF each for all other outputs. Timings must be derated for larger load capacitances.

For pins 14, 16, 17, 19 (WC, DRUN, RD, RC):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{RS}	Rise Time		10	nsec	10% to 90%

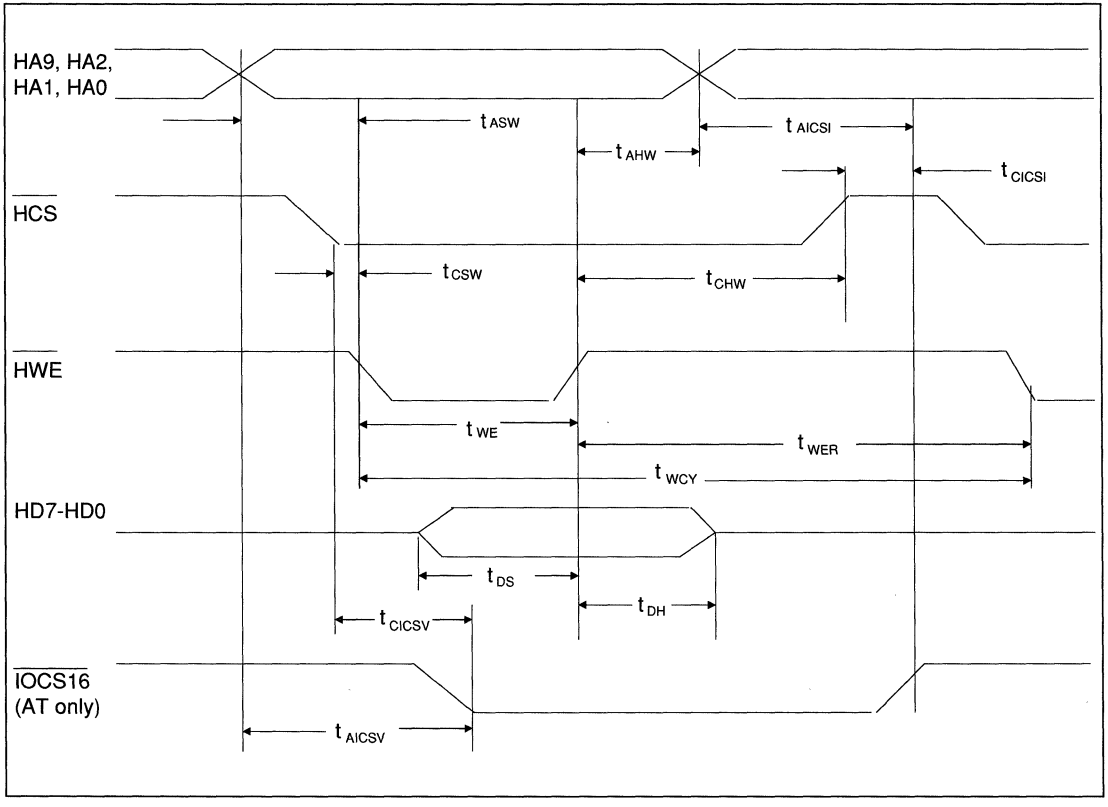


FIGURE 7. AT/XT HOST PROGRAMMED I/O WRITE TIMING

NOTE

A write occurs during the overlap of $\overline{HCS}$ and $\overline{HWE}$.

5.3.1 AT/XT HOST PROGRAMMED I/O WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{ASW}	Address Setup to $\overline{HWE}$ Low	30		ns	
t_{CSW}	$\overline{HCS}$ Setup to $\overline{HWE}$ Low	10		ns	
t_{DS}	Data Setup to $\overline{HWE}$ High	30		ns	Port 0 only.
t_{WE}	$\overline{HWE}$ Pulse Width	75		ns	Port 0 only.
t_{DS}	Data Setup to $\overline{HWE}$ High	50		ns	All other ports.
t_{WE}	$\overline{HWE}$ Pulse Width	100		ns	All other ports
t_{DH}	Data Hold from $\overline{HWE}$ High	15		ns	
t_{AHW}	ADDR Hold from $\overline{HWE}$ High	20		ns	
t_{CHW}	$\overline{HCS}$ Hold from $\overline{HWE}$ High	10		ns	
t_{WER}	$\overline{HCS}$ and $\overline{HWE}$ Inactive	20		ns	
t_{WCY}	Write Cycle Time	125 2*X		ns	Port 0, XTAL>16 MHz Port 0, XTAL<16MHz (X=t_{XTAL})
t_{WCY}	Write Cycle Time	150		ns	All other ports
t_{CICSV}	$\overline{IOCS16}$ valid from $\overline{HCS}$		30	ns	
t_{AICSV}	$\overline{IOCS16}$ valid from address		40	ns	
t_{CICSI}	$\overline{IOCS16}$ inactive from $\overline{HCS}$		35	ns	Test circuit 1.
t_{AICSI}	$\overline{IOCS16}$ inactive from address		45	ns	Test circuit 1.

TABLE 15. AT/XT HOST PROGRAMMED I/O WRITE TIMING

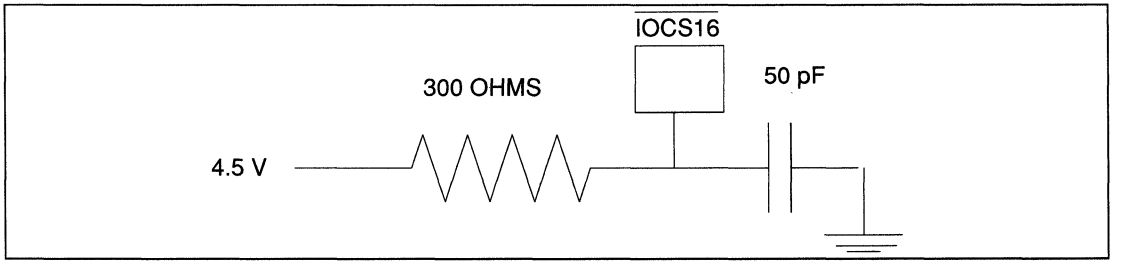


FIGURE 8. TEST CIRCUIT 1

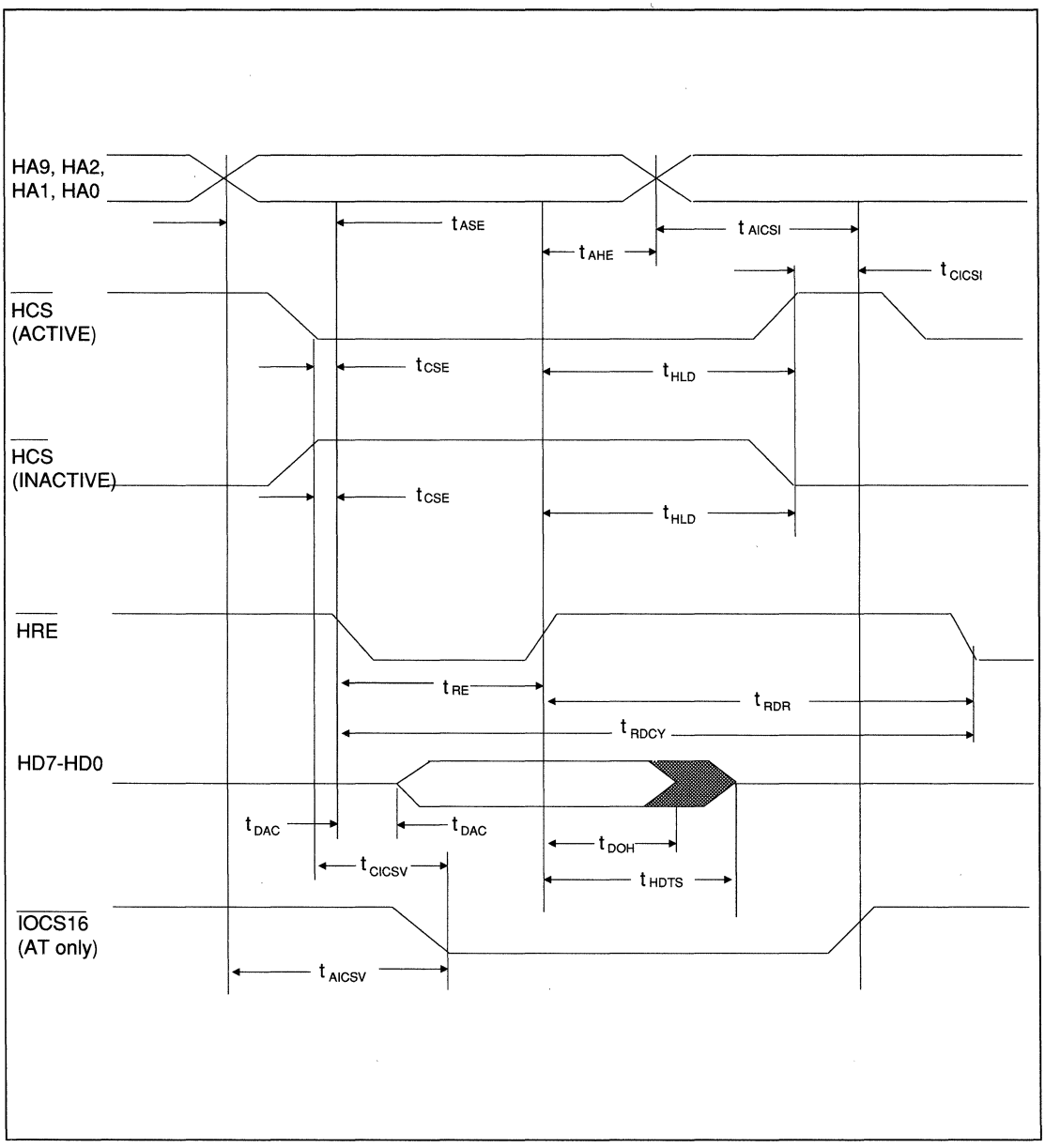


FIGURE 9. AT/XT HOST PROGRAMMED I/O READ TIMING

5.3.2 AT/XT HOST PROGRAMMED I/O READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{ASE}	Address Setup to $\overline{HRE}$ Low	30		ns	
t_{CSE}	$\overline{HCS}$ Setup to $\overline{HRE}$ Low	10		ns	
t_{DAC}	Data Valid from $\overline{HRE}$ Low		60 70 100	ns	Port 0, 8-bit. Port 0, 16-bit. All other ports.
t_{RE}	$\overline{HRE}$ Pulse Width	75 100		ns	Port 0 All other ports
t_{DOH}	Data Hold from $\overline{HRE}$ High	5		ns	
t_{HDTS}	Data Tri-state from $\overline{HRE}$		50	ns	
t_{HLD}	Address, $\overline{HCS}$ Hold from $\overline{HRE}$ High	10		ns	
t_{RDR}	$\overline{HCS}$ and $\overline{HRE}$ Inactive	20		ns	
t_{RDCY}	Read Cycle Time	125 2*X		ns	Port 0, XTAL>16 MHz Port 0, XTAL<16 MHz (X=t_{XTAL})
t_{RDCY}	Read Cycle Time	150		ns	All other ports.
t_{CICSV}	$\overline{IOCS16}$ Valid from $\overline{HCS}$		30	ns	
t_{AICSV}	$\overline{IOCS16}$ Valid from Address		40	ns	
t_{CICSI}	$\overline{IOCS16}$ Inactive from $\overline{HCS}$		35	ns	Test circuit 1
t_{AICSI}	$\overline{IOCS16}$ Inactive from Address		45	ns	Test circuit 1

TABLE 16. AT/XT HOST PROGRAMMED I/O READ TIMING

33

5.3.3 AT/XT HOST DMA WRITE TIMING

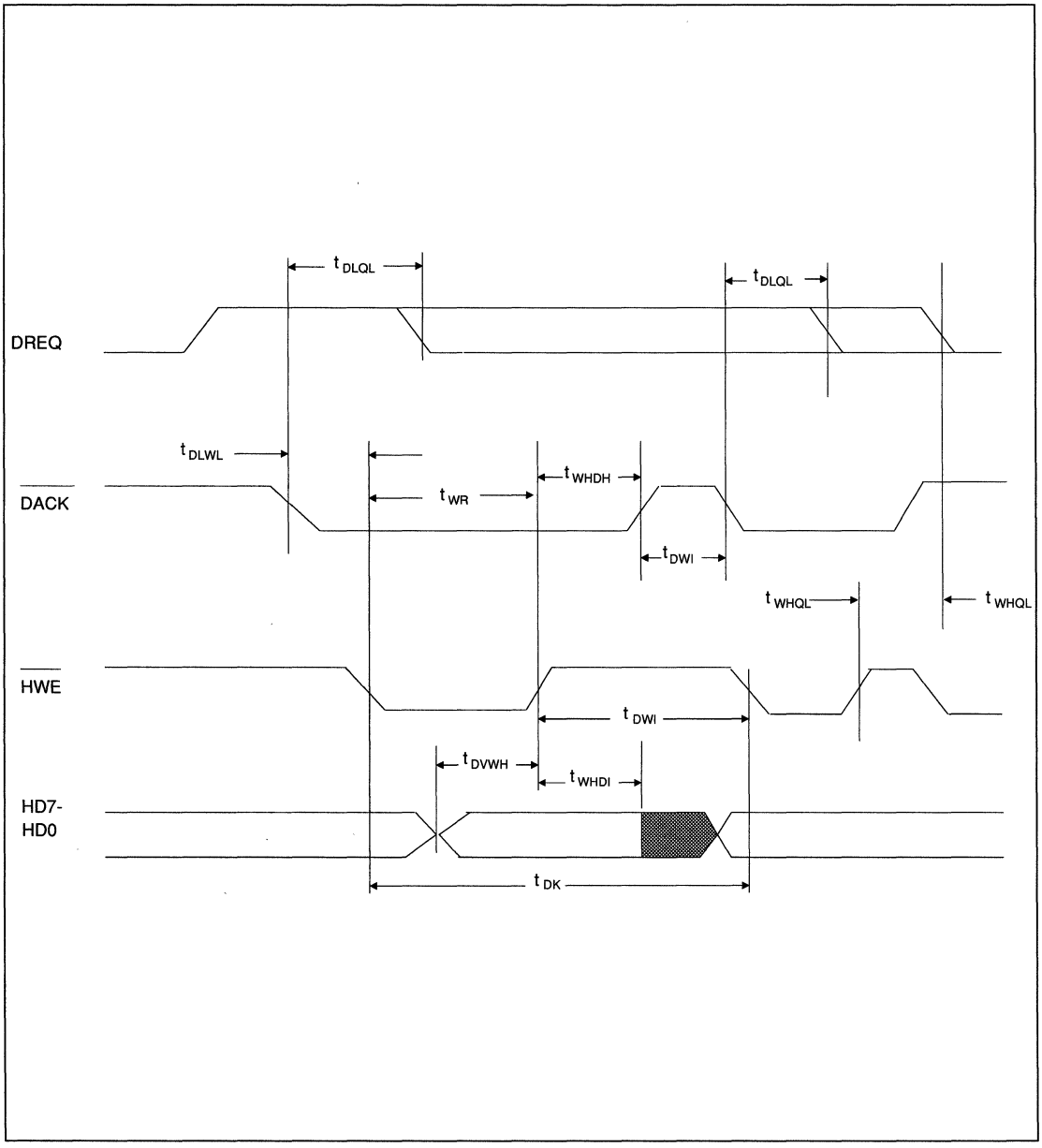


FIGURE 10. AT/XT HOST DMA WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{DLQL}	$\overline{DACK}$ Low to DRQ Low		100	ns	BDEN=0
t_{WHQL}	$\overline{HWE}$ High to DRQ Low		4*X +100	ns	BDEN=1. First transfer count throttle. (X=t_{XTAL})
t_{DK}	DMA Cycle	100 2*X		ns	XTAL=20MHz Any XTAL (X=t_{XTAL})
t_{DLWL}	$\overline{DACK}$ Low to $\overline{HWE}$ Low	0		ns	
t_{WR}	$\overline{HWE}$ Pulse Width	80		ns	
t_{DVWH}	Data Valid to $\overline{HWE}$ High	30		ns	
t_{WHDH}	$\overline{HWE}$ High to $\overline{DACK}$ High	0		ns	
t_{WHDI}	$\overline{HWE}$ High to Data Invalid	15		ns	
t_{DWI}	$\overline{DACK}$ and $\overline{HWE}$ Inactive	20		ns	

TABLE 17. AT/XT DMA WRITE TIMING

33

5.3.4 AT/XT HOST DMA READ TIMING

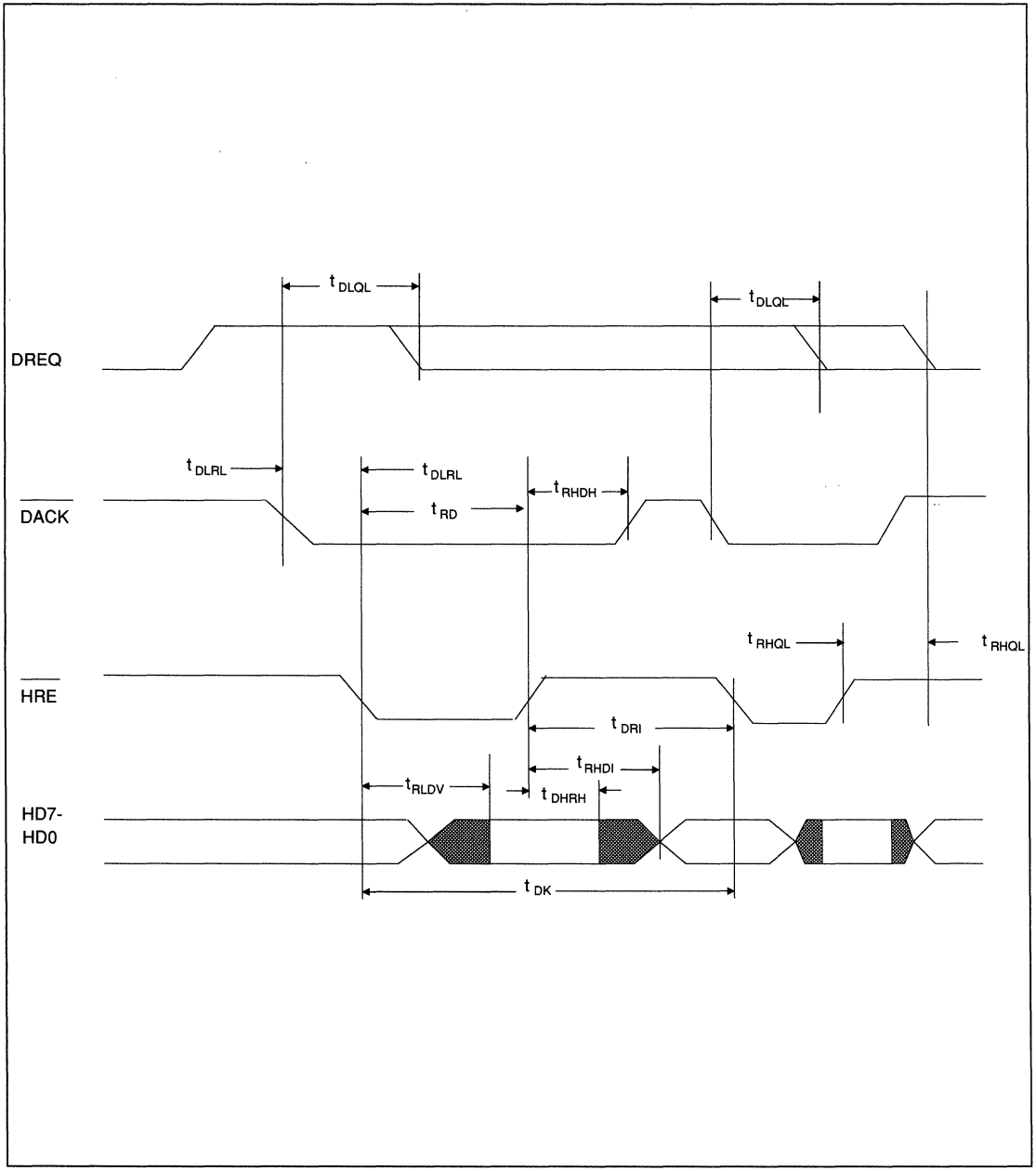


FIGURE 11. AT/XT HOST DMA READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{DLQL}	$\overline{DACK}$ Low to DRQ Low		100	ns	BDEN=0
t_{RHQL}	$\overline{HRE}$ High to DRQ Low		4*X +100	ns	BDEN=1. First TC throttle. (X=t_{XTAL})
t_{DK}	DMA Cycle	100 2*X		ns	XTAL=20MHz Any XTAL (X=t_{XTAL})
t_{DLRL}	$\overline{DACK}$ Low to $\overline{HRE}$ Low	0		ns	
t_{RD}	$\overline{HRE}$ Pulse Width	80		ns	
t_{RLDV}	$\overline{HRE}$ Low to Data Valid		60 70	ns	8-bit mode 16-bit mode
t_{RHDH}	$\overline{HRE}$ High to $\overline{DACK}$ High	0		ns	
t_{DHRH}	Data Hold from $\overline{HRE}$ High	5		ns	
t_{RHDI}	$\overline{HRE}$ High to Data tri-state		50	ns	
t_{DRI}	$\overline{DACK}$ and $\overline{HRE}$ Inactive.	20		ns	

TABLE 18. AT/XT DMA READ TIMING

33

5.3.5 SLAVE HOST WRITE TIMINGS

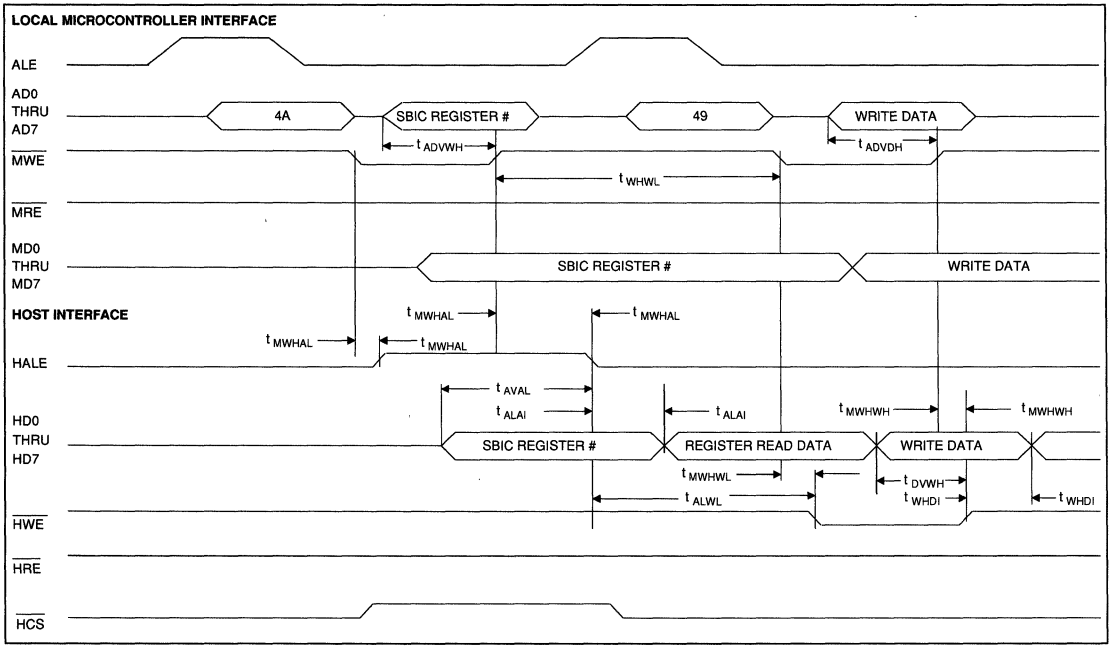


FIGURE 12. SLAVE HOST WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{WHWL}	Address Port Write to Data Write Recovery Time	120	10000	ns	
t_{MWHAL}	$\overline{MWE}$ to HALE Delay		150	ns	
t_{AVAL}	HD Address Setup to HALE Low	40		ns	AD setup to $\overline{MWE}$ (t_{ADVWH})=130 ns
t_{ALAI}	HD Address Hold From HALE low	0		ns	
t_{ALWL}	HALE Low To $\overline{HWE}$ Low	90		ns	
t_{DVWH}	HD Valid to $\overline{HWE}$ High	70		ns	AD setup to $\overline{MWE}$ (t_{ADVWH})=130 ns
t_{WHDI}	HD Inactive from $\overline{HWE}$	0		ns	
t_{MWHWL}	$\overline{MWE}$ Low to HWE Low		150	ns	
t_{MHWH}	MWE High to HWE High		150	ns	

TABLE 19. SLAVE HOST WRITE TIMING

5.3.6 SLAVE HOST READ TIMINGS

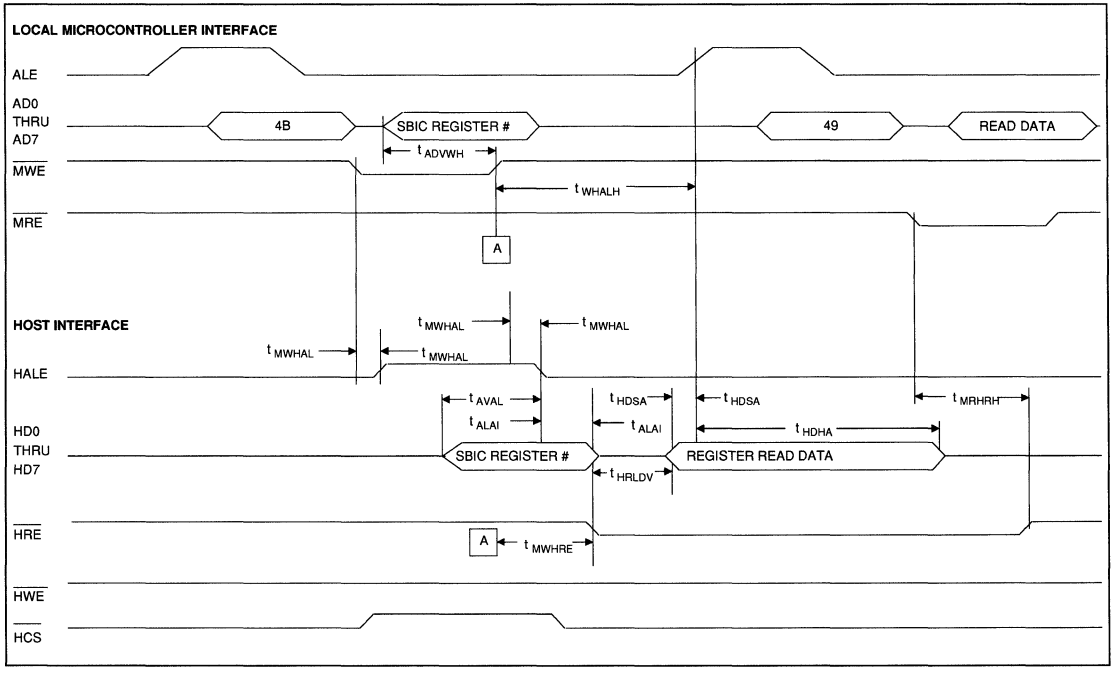


FIGURE 13. SLAVE HOST READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{WHALH}	Address Port Write to ALE High Read Recovery Time	400	10000	ns	t_{HRLDV}=210 ns
t_{MWHAL}	$\overline{MWE}$ to HALE Delay		150	ns	
t_{MWHRE}	$\overline{MWE}$ to $\overline{HRE}$ Delay		150	ns	
t_{AVAL}	HD Address Setup to HALE Low	40		ns	AD setup to $\overline{MWE}$ (t_{ADVWH})=130 ns.
t_{ALAI}	HD Address Hold from HALE Low	0		ns	
t_{HDSA}	HD Data **Setup to** ALE High	40		ns	
t_{HDHA}	HD Data **Hold from** ALE High	40		ns	
t_{MRHRH}	$\overline{MRE}$ Low to $\overline{HRE}$ High Delay	0		ns	
t_{HRLDV}	HRE Low to HD Data Valid Delay				t_{HRLDV} is a function of the slave peripheral device and only affects t_{WHALH}. t_{WALH} = t_{MWHRE} + t_{HRLDV} + t_{HDSA}

TABLE 20. SLAVE HOST READ TIMING

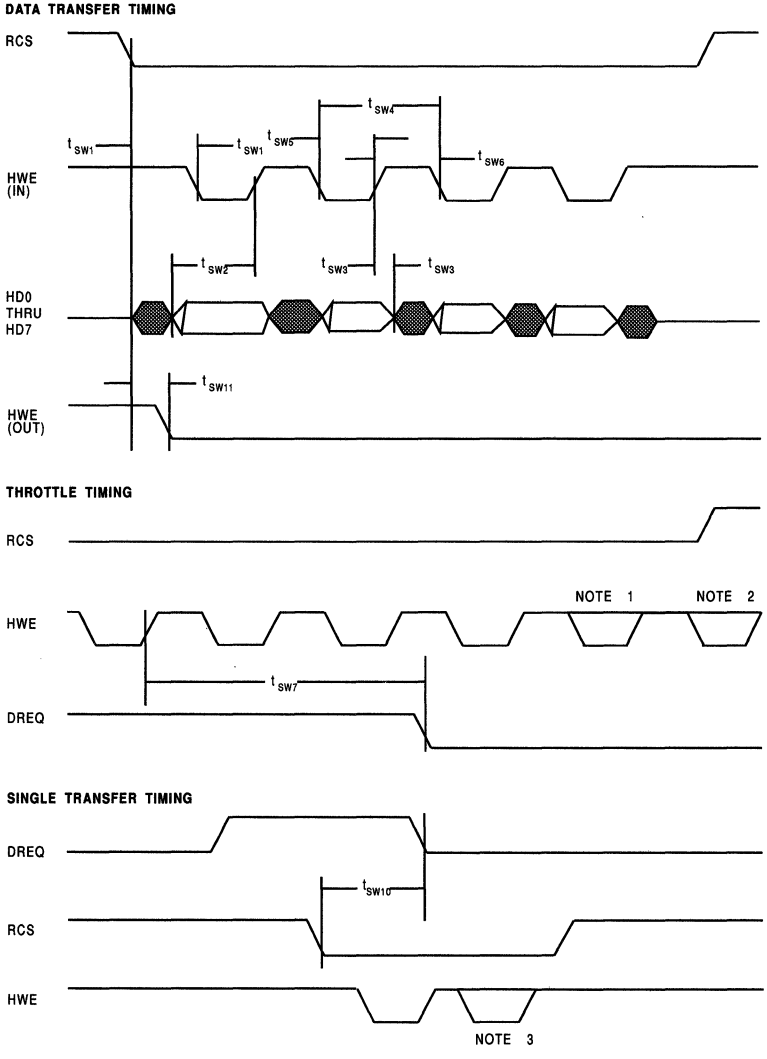


FIGURE 14. SLAVE HOST DMA WRITE TIMING

5.3.7 SLAVE HOST DMA WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN BIN 02 BIN 03 BIN 05	MAX BIN 02 BIN 03 BIN 05	UNITS	CONDITIONS
t_{SW1}	$\overline{RCS}$ Low to $\overline{HWE}$ First Transfer of Burst	0 0 0		ns	
t_{SW2}	HD Valid to $\overline{HWE}$ Rising	30 30 30		ns	
t_{SW3}	$\overline{HWE}$ Rising to HD Invalid	15 15 15		ns	
t_{SW4}	$\overline{HWE}$ Cycle Time	200 200 100		ns	$t_{XTAL} < t_{SW4} / 2$
t_{SW5}	$\overline{HWE}$ Low Pulse Width	80 80 30		ns	
t_{SW6}	$\overline{HWE}$ High Pulse	30 30 30		ns	
t_{SW7}	$\overline{HWE}$ Rising to DRQ Low		4*X + 100 4*X + 100 4*X + 50	ns	Intermediate throttle. X = t_{XTAL}
t_{SW10}	$\overline{RCS}$ Low to DREQ Low		100 100 50		Throttle when transfer count < 16 or single transfer mode
t_{SW11}	$\overline{DACK}$ Low to $\overline{HWE}$ Out Tri-state		60 60 60	ns	HSMB = 1

TABLE 21. SLAVE HOST DMA WRITE TIMING

The following notes apply to Figure 15.

NOTE 1

SBIC guarantees no transfer here at 5 MB/s transfer rate.

NOTE 2

SBIC guarantees no transfer here at 10 MB/s transfer rate.

NOTE 3

SBIC guarantees no transfer here.

Although 4 transfers may occur after the FIFO goes almost full at 10 MB/s and only 3 bytes remain at that time, the buffer manage guarantees that at least 1 additional transfer occurs out of the FIFO prior to the fourth host transfer after the almost full condition. This guarantees that no overrun condition occurs.

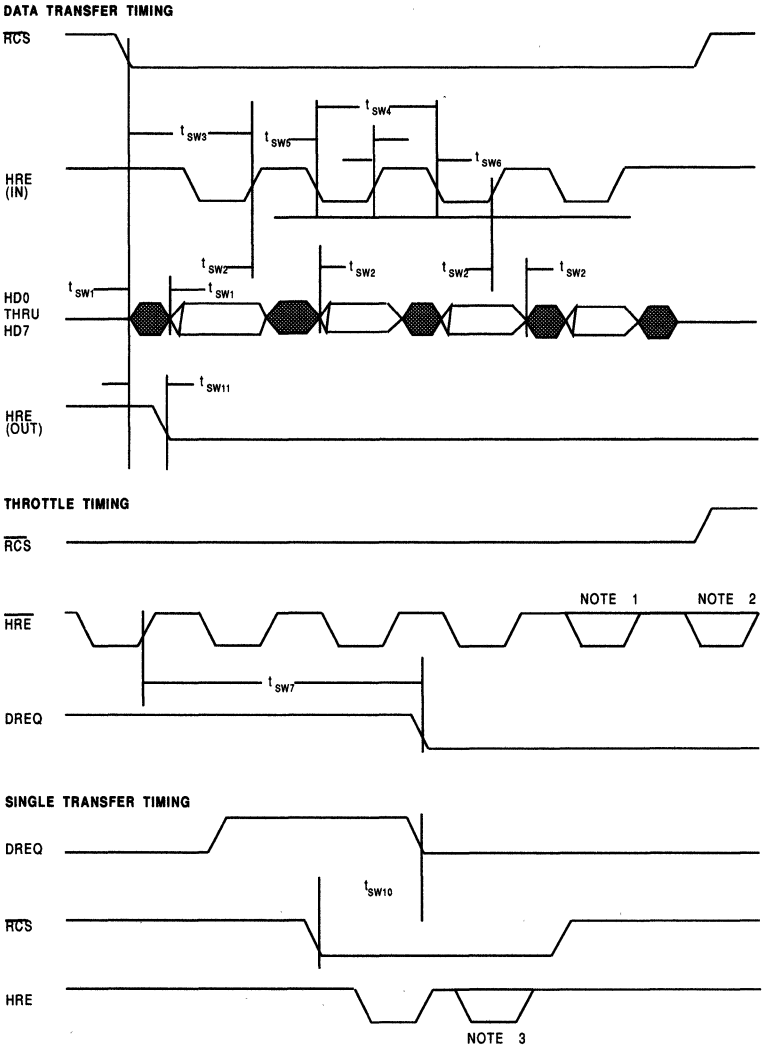


FIGURE 15. SLAVE HOST DMA READ TIMING

5.3.8 SLAVE HOST DMA READ TIMING

SYMBOL	CHARACTERISTIC	MIN BIN 02 BIN 03 BIN 05	MAX BIN 02 BIN 03 BIN 05	UNITS	CONDITIONS
t_{SW1}	$\overline{RCS}$ Low to HD Valid First Transfer of Burst	0 0 0		ns	
t_{SW2}	$\overline{HRE}$ Rising to HD Valid	5 5 5	180 180 180	ns	
t_{SW3}	$\overline{RCS}$ Low to First $\overline{HRE}$ Rising Edge	140 140 100		ns	
t_{SW4}	$\overline{HRE}$ Cycle Time	200 200 100		ns	$t_{XTAL} < t_{SW4} / 2$
t_{SW5}	$\overline{HRE}$ Low Pulse Width	80 80 30		ns	
t_{SW6}	$\overline{HRE}$ High Pulse	30 30 30		ns	
t_{SW7}	$\overline{HRE}$ Rising to DRQ Low		4*X + 100 4*X + 100 4*X + 50	ns	Intermediate throttle. X = t_{XTAL}
t_{SW10}	$\overline{RCS}$ Low to DREQ Low		100 100 50		Throttle when transfer count < 16 or single transfer mode
t_{SW11}	$\overline{DACK}$ Low to $\overline{HRE}$ Out Tri-state		60 60 60	ns	HSMB = 1

TABLE 22. SLAVE HOST DMA READ TIMING

The following notes apply to Figure 16.

NOTE 1

SBIC guarantees no transfer here at 5 MB/s transfer rate.

NOTE 2

SBIC guarantees no transfer here at 10 MB/s transfer rate.

NOTE 3

SBIC guarantees no transfer here.

Although 4 transfers may occur after the FIFO goes almost full at 10 MB/s and only 3 bytes remain at that time, the buffer manage guarantees that at least 1 additional transfer occurs out of the FIFO prior to the fourth host transfer after the almost full condition. This guarantees that no overrun condition occurs.

5.3.9 BUFFER RAM WRITE TIMING (INTERNAL OSCILLATOR; XTAL = 8 - 25 MHZ)

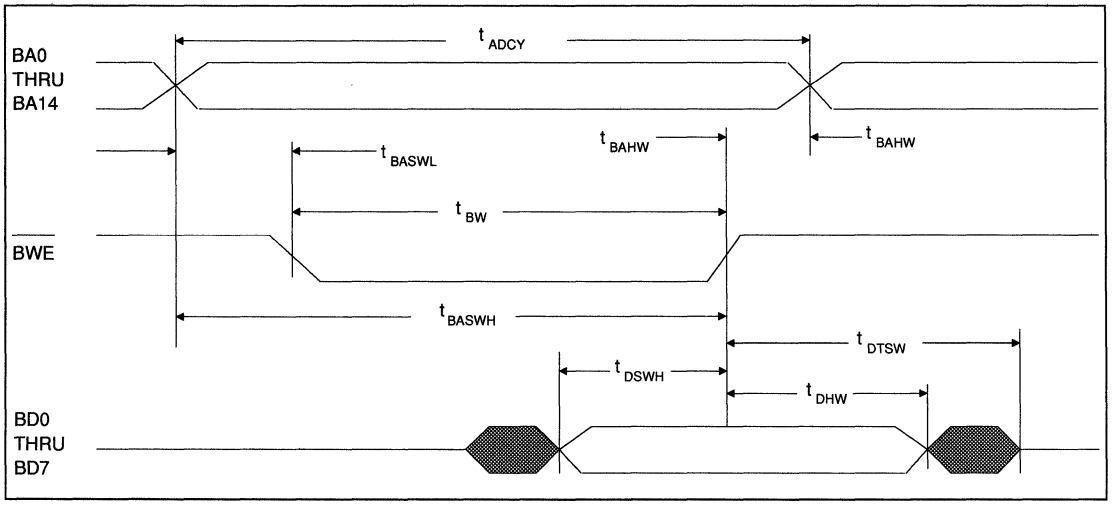


FIGURE 16. BUFFER RAM WRITE TIMING (INTERNAL OSCILLATOR)

SYMBOL	CHARACTERISTIC	MIN Bin 02 Bin 03 Bin 05	MAX	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35 $2*t_{XTAL}$-25		ns	Any XTAL
t_{BASWH}	Addres Setup to $\overline{BWE}$ High	$2*t_{XTAL}$-40 $2*t_{XTAL}$-55 $2*t_{XTAL}$-35		ns	Any XTAL
t_{BASWL}	Addres Setup to $\overline{BWE}$ Low	$0.5*t_{XTAL}$-20 $0.5*t_{XTAL}$-35 $0.5*t_{XTAL}$-20		ns	Any XTAL
t_{BW}	$\overline{BWE}$ Pulse Width	$1.5*t_{XTAL}$-30 $1.5*t_{XTAL}$-35 $1.5*t_{XTAL}$-25		ns	Any XTAL
t_{BAHW}	Address Hold From $\overline{BWE}$ High	5 5 5		ns	Any XTAL
t_{DSWH}	Data Valid to $\overline{BWE}$ High	$1.5*t_{XTAL}$-40 $1.5*t_{XTAL}$-60 $1.5*t_{XTAL}$-35		ns	Any XTAL
t_{DHW}	Data Hold from $\overline{BWE}$ High	10 10 10		ns	Any XTAL
t_{DTSW}	Data Tri-state from $\overline{BWE}$ High		50	ns	Any XTAL

TABLE 23. BUFFER RAM WRITE TIMING (INTERNAL OSCILLATOR)

5.3.10 BUFFER RAM READ TIMING (INTERNAL OSCILLATOR; XTAL = 8 - 20 MHZ)

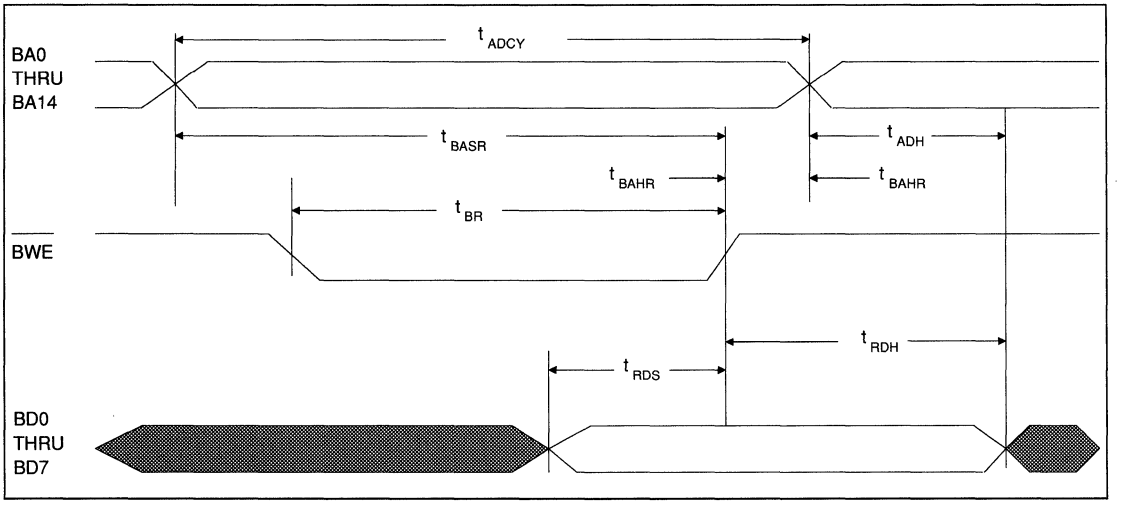


FIGURE 17. BUFFER READ TIMING (INTERNAL OSCILLATOR)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	72 125	ns	Max XTAL
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	Any XTAL
t_{BASR}	Address Setup to $\overline{BOE}$ High	72 125	ns	Max XTAL
t_{BASR}	Address Setup to $\overline{BOE}$ High	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	Any XTAL
t_{BR}	$\overline{BOE}$ Pulse Width	45 75	ns	Max XTAL
t_{BR}	$\overline{BOE}$ Pulse Width	$1.5*t_{XTAL}$-30 $1.5*t_{XTAL}$-45	ns	Any XTAL
t_{BAHR}	Address Hold from $\overline{BOE}$ High	0 0	ns	Any XTAL
t_{RDS}	Data Setup to $\overline{BOE}$ High	5 5	ns	Any XTAL
t_{RDH}	Data Hold from $\overline{BOE}$ High	10 10	ns	Any XTAL
t_{DHW}	Data Hold from Address	10 10	ns	

• All timings in this table **only** are referenced to 1.5V levels.

TABLE 24. BUFFER READ TIMING (INTERNAL OSCILLATOR)

33

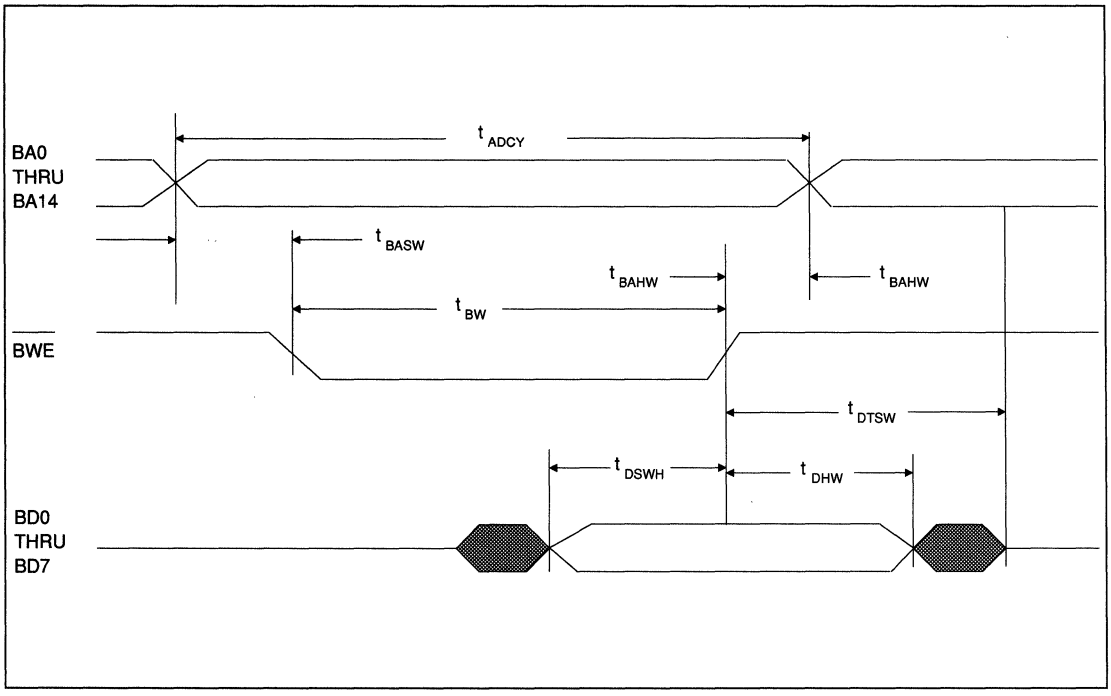


FIGURE 18. BUFFER RAM WRITE TIMING (EXTERNAL OSCILLATOR)

5.3.11 BUFFER RAM WRITE TIMING (EXTERNAL OSCILLATOR; XTAL = 8 to 20 MHz)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	72 125		ns	Max XTAL
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35		ns	Any XTAL
t_{BASWL}	Address Setup to $\overline{BWE}$ Low	5 5		ns	Max XTAL/ 50% XTAL
t_{BASWL}	Address Setup to $\overline{BWE}$ Low	t_{XCH}-20 t_{XCH}-35		ns	Any XTAL
t_{BASWH}	Address Setup to $\overline{BWE}$ High	60 105		ns	Max XTAL
t_{BASWH}	Address Setup to $\overline{BWE}$ High	$2*t_{XTAL}$-40 $2*t_{XTAL}$-55		ns	Any XTAL
t_{BW}	$\overline{BWE}$ Pulse Width	55 85		ns	Max XTAL/ 50% XTAL
t_{BW}	$\overline{BWE}$ Pulse Width	$t_{XTAL}+t_{XCL}$-30 $t_{XTAL}+t_{XCL}$-35		ns	Any XTAL
t_{BAHW}	Address Hold from $\overline{BWE}$ High	5 5		ns	Any XTAL
t_{DSWH}	Data Valid to $\overline{BWE}$ High	35 60		ns	Max XTAL
t_{DSWH}	Data Valid to $\overline{BWE}$ High	$t_{XTAL}+t_{XCH}$-40 $t_{XTAL}+t_{XCH}$-60		ns	Any XTAL/ %50 XTAL
t_{DHW}	Data Hold from $\overline{BWE}$ High	10 10		ns	Any XTAL
t_{DTSW}	Data tri-state from $\overline{BWE}$ High		50	ns	Any XTAL

• All timings in this table only are referenced to 1.5 V levels except t_{DHW}.

TABLE 25. BUFFER RAM WRITE TIMING (EXTERNAL OSCILLATOR)

5.3.12 BUFFER RAM READ TIMING (EXTERNAL OSCILLATOR; XTAL=8 to 20 MHz)

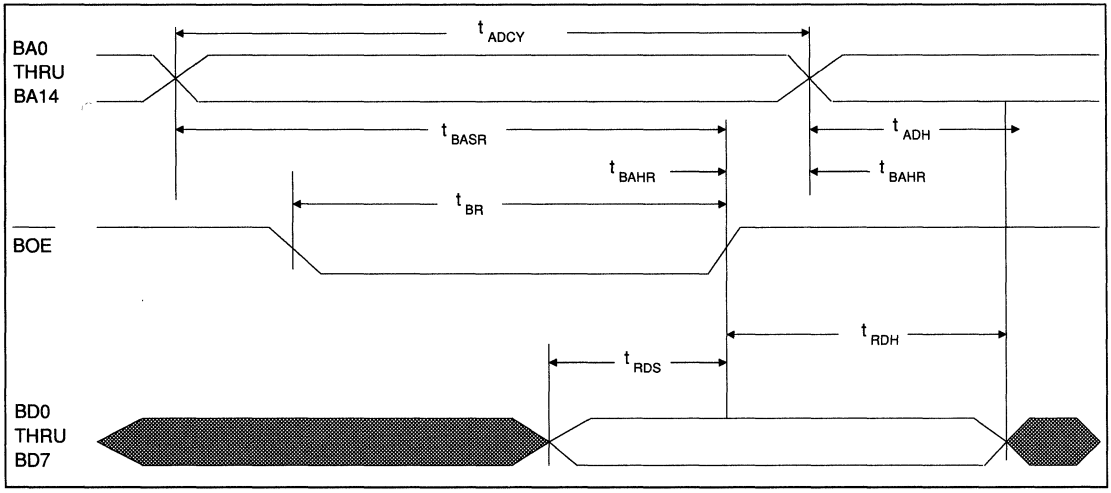


FIGURE 19. BUFFER RAM READ TIMING (EXTERNAL OSCILLATOR)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	72 125	ns	Max XTAL/50% XTAL
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	Any XTAL
t_{BASR}	Address Setup to $\overline{BOE}$ High	72 125	ns	Max XTAL/50% XTAL
t_{BASR}	Address Setup to $\overline{BOE}$ High	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	
t_{BR}	$\overline{BOE}$ Pulse Width	45 75	ns	Max XTAL/50% XTAL
t_{BR}	$\overline{BOE}$ Pulse Width	$t_{XTAL}+t_{XCH}$-30 $t_{XTAL}+t_{XCH}$-45	ns	Any XTAL
t_{BAHR}	Address Hold from $\overline{BOE}$ High	0 0	ns	Any XTAL
t_{RDS}	Data Setup to $\overline{BOE}$ High	5 5	ns	Any XTAL
t_{RDH}	Data Hold from $\overline{BOE}$ High	10 10	ns	Any XTAL
t_{DHW}	Data Hold from Address	10 10	ns	

• All timings in this table referenced to 1.5 V levels.

TABLE 26. BUFFER RAM READ TIMING (EXTERNAL OSCILLATOR)

5.3.13 MICROPROCESSOR WRITE TIMING (INTEL BUS)

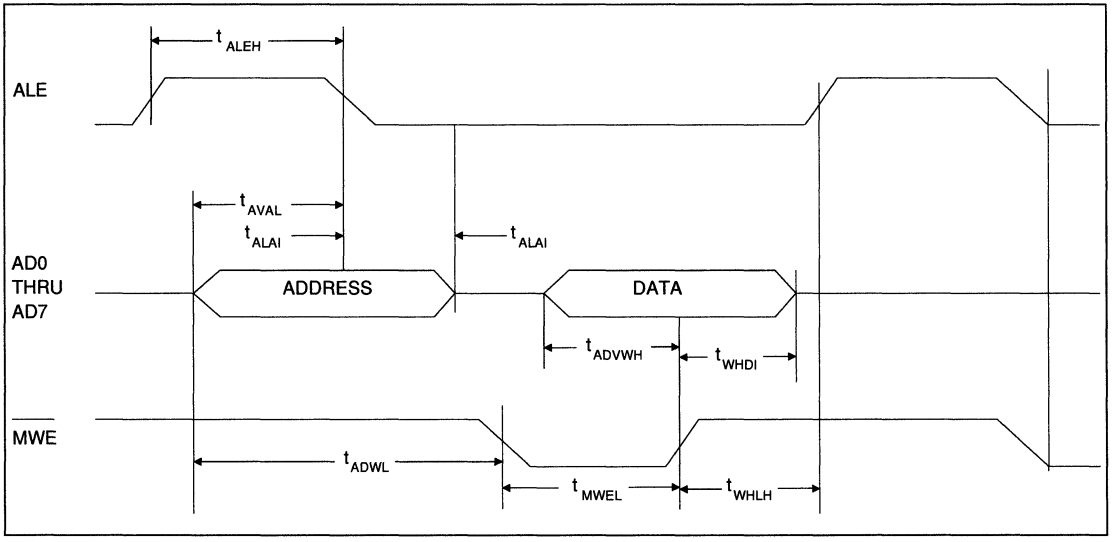


FIGURE 20. MICROPROCESSOR WRITE TIMING (INTEL BUS)

SYMBOL	CHARACTERISTIC	MIN	UNITS	CONDITIONS
t_{AVAL}	Address Setup to ALE Low	15	ns	
t_{ALAI}	Address Hold from ALE Low	5	ns	
t_{ALEH}	ALE High Pulse Width	30	ns	
t_{ADVWH}	Data Setup to $\overline{MWE}$ High	50 130	ns	HSMB=0 HSMB=1
t_{WHDI}	Data Hold from $\overline{MWE}$ High	5	ns	
t_{MWEL}	$\overline{MWE}$ Low Pulse Width	75	ns	
t_{ADWL}	Address Valid to $\overline{MWE}$ Low	55	ns	
t_{WHLH}	$\overline{MWE}$ High to ALE High	10	ns	

TABLE 27. MICROPROCESSOR WRITE TIMING (INTEL BUS)

33

5.3.14 MICROPROCESSOR WRITE TIMING (MOTOROLA BUS)

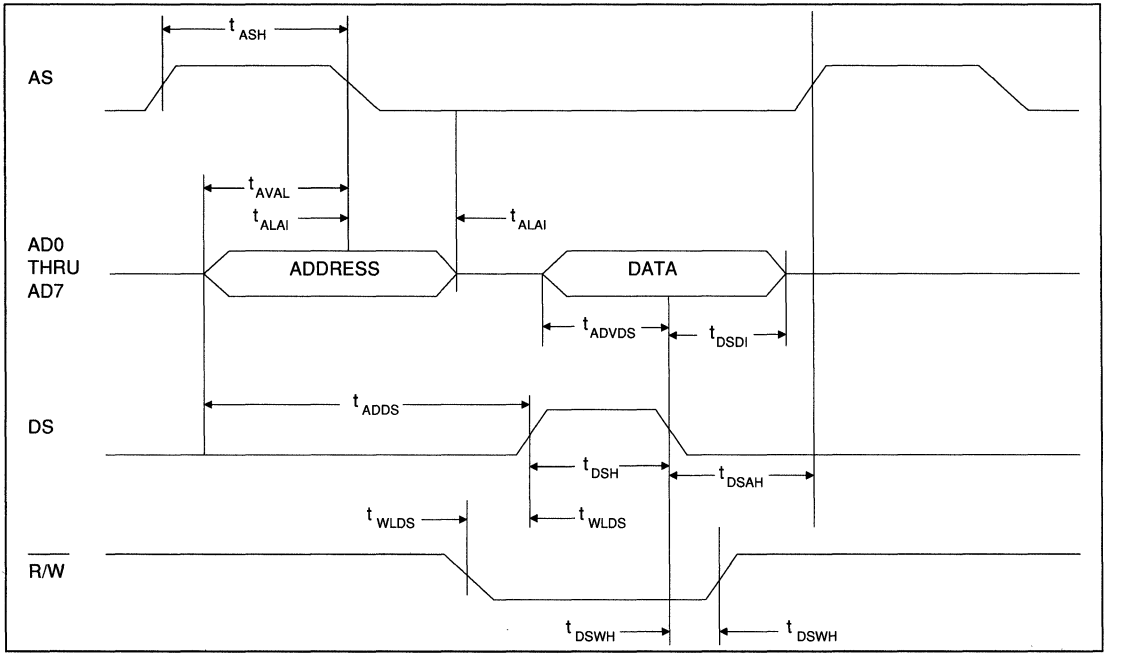


FIGURE 21. MICROPROCESSOR WRITE TIMING (MOTOROLA BUS)

SYMBOL	CHARACTERISTIC	MIN	UNITS	CONDITIONS
t_{AVAL}	Address Setup to AS Low	15	ns	
t_{ALAI}	Address Hold from AS	5	ns	
t_{ASH}	AS High Pulse Width	30	ns	
t_{ADVDS}	Data Setup to DS Low	50 130	ns	HSMB=0 HSMB=1
t_{DSDI}	Data Hold from DS Low	5	ns	
t_{DSH}	DS High Pulse Width during Write	75	ns	
t_{WLDS}	R/$\overline{W}$ Low to DS High	5	ns	
t_{DSWH}	DS Low to R/$\overline{W}$ High	20	ns	
t_{ADDS}	Address High to DS High	55	ns	
t_{DSAH}	DS Low to AS High	10	ns	

TABLE 28. MICROPROCESSOR WRITE TIMING (MOTOROLA BUS)

5.3.15 MICROPROCESSOR READ TIMING (INTEL BUS)

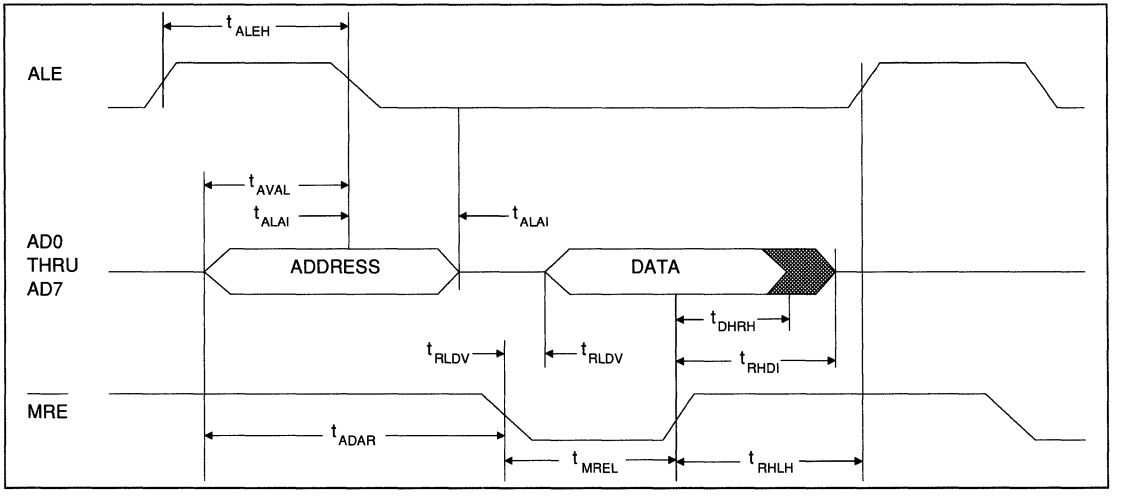


FIGURE 22. MICROPROCESSOR READ TIMING (INTEL BUS)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{AVAL}	Address Setup to ALE Low	15		ns
t_{ALAI}	Address Hold from ALE Low	5		ns
t_{ALEH}	ALE High Pulse Width	30		ns
t_{RLDV}	Data Valid from $\overline{MRE}$ Low		100	ns
t_{DHRH}	Data Hold from $\overline{MRE}$ High	10		ns
t_{RHDI}	Data Tri-state from $\overline{MRE}$ High		50	ns
t_{MREL}	$\overline{MRE}$ Low Pulse Width	100		ns
t_{ADAR}	Address Valid to $\overline{MRE}$ Low	55		ns
t_{RHLH}	$\overline{MRE}$ High to ALE High	10		ns

TABLE 29. MICROPROCESSOR READ TIMING (INTEL BUS)

33

5.3.16 MICROPROCESSOR READ TIMING (MOTOROLA BUS)

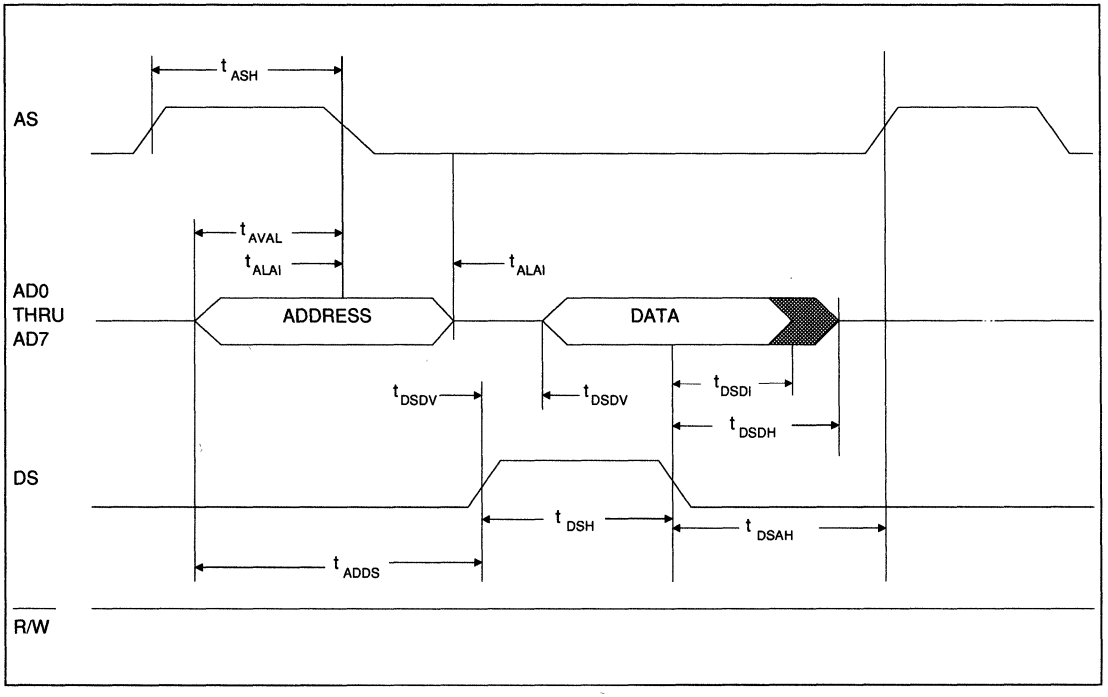


FIGURE 23. MICROPROCESSOR READ TIMING (MOTOROLA BUS)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{AVAL}	Address Setup to AS Low	15		ns
t_{ALAI}	Address Hold from AS Low	5		ns
t_{ASH}	AS High Pulse Width	30		ns
t_{DSDV}	Data Valid from DS High		100	ns
t_{DSDI}	Data Tri-state from DS Low		50	ns
t_{DSH}	DS High pulse Width during Read	100		ns
t_{ADDS}	Address Valid to DS High	55		ns
t_{DSAH}	DS Low to AS High	10		ns

TABLE 30. MICROPROCESSOR READ TIMING (MOTOROLA BUS)

5.3.17 WRITE DATA TIMING (MFM/RLL MODE; WC 5 to 15 MHz)

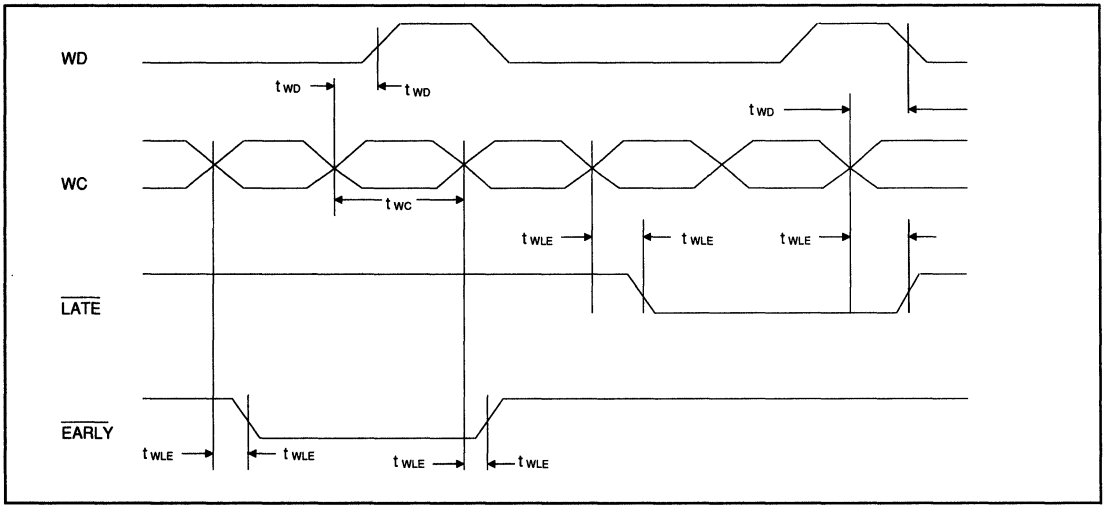


FIGURE 24. WRITE DATA TIMING (MFM/RLL MODE)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
		20 MHz		
		12 MHz		
t_{WC}	WC Pulse Width	28	500	ns
		45	500	
t_{WLE}	Early/Late Propagation	3	15	ns
		3	25	
t_{WD}	WD Propagation Delay	3	15	ns
		3	25	
t_{WCF}	WC Frequency	1	15	MHz
		1	10	

TABLE 31. WRITE DATA TIMING (MFM/RLL MODE)

33

5.3.18 WRITE DATA TIMING (NRZ MODE; WC 5 to 15 MHz)

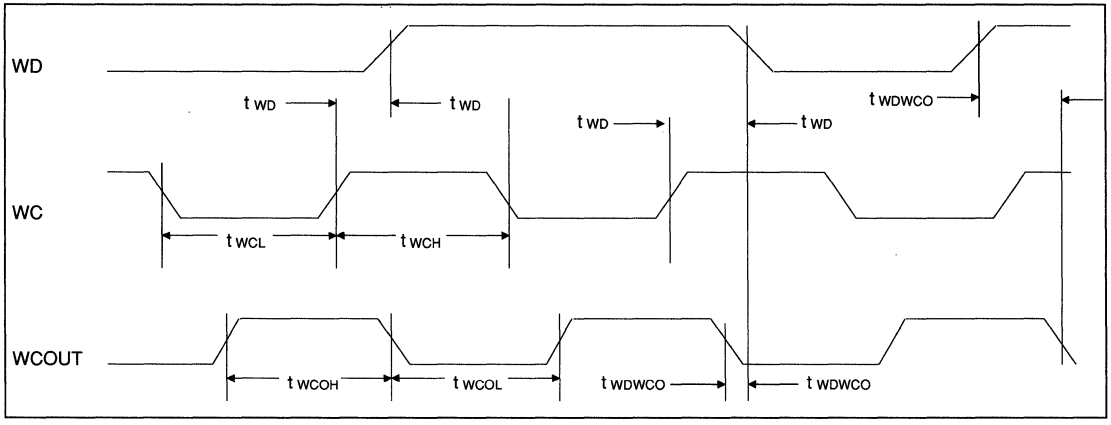


FIGURE 25. WRITE DATA TIMING (NRZ MODE)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS
t_{WCL}	WC Pulse Width Low	20 27	500 500	ns
t_{WCH}	WC Pulse Width High	20 27	500 500	ns
t_{WLE}	Early/Late Propagation	3 3	15 25	ns
t_{WD}	WD Propagation Delay	3 3	15 25	ns
t_{WCF}	WC Frequency	1 1	22 16.5	MHz
t_{WCOL}	WCOUT Pulse Width Low	t_{WCH} - 5 t_{WCH} - 9		ns
t_{WCOL}	WCOUT Pulse Width Low		t_{WCH} + 5 t_{WCH} + 9	ns
t_{WCOH}	WCOUT Pulse Width High	t_{WCH} - 5 t_{WCH} - 9		ns
t_{WCOH}	WCOUT Pulse Width High		t_{WCH} + 5 t_{WCH} + 9	ns
t_{WDWCO}	WD Prop Delay from WCOUT	-5 -8	+5 +8	ns

TABLE 32. WRITE DATA TIMING (MFM/RLL MODE)

5.3.19 READ DATA TIMING (MFM/RLL MODE; RC/WC 5 to 15 MHz)

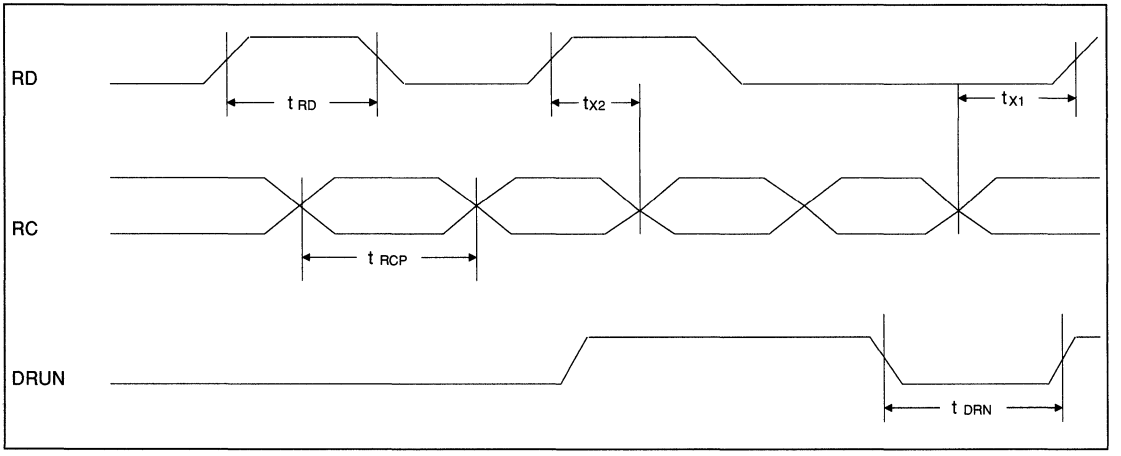


FIGURE 26. READ DATA TIMING (MFM/RLL)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS
t_{RCP}	RC Pulse Width	27 45	500 500	ns
t_{X1}	RC Transition to Next Leading RD	5 10		ns
t_{X2}	Leading RD to Next RC Transition	10 20		ns
t_{RD}	Read Data Pulse Width	20 30	t_{RCP} t_{RCP}	ns
t_{DRN}	DRUN Low Pulse Width	25 25		ns
t_{RCF}	RC Frequency	1 1	15 10	MHz

TABLE 33. READ DATA TIMING (MFM/RLL)

33

5.3.20 READ DATA TIMING (NRZ MODE; WC 5 to 20 MHz)

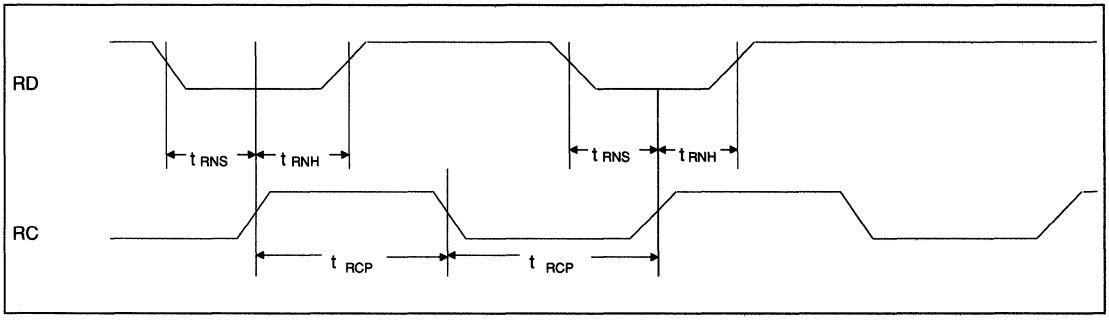


FIGURE 27. READ DATA TIMING (NRZ MODE)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS
t_{RCP}	RC Pulse Width	20 27	500 500	ns
t_{RNS}	RD Setup to RC High	7 10		ns
t_{RNH}	RD Hold from RC High	7 10		ns
t_{RCF}	RC Frequency	1 1	22 16.5	MHz

TABLE 34. READ DATA TIMING (NRZ MODE)

5.3.21 MISCELLANEOUS TIMING

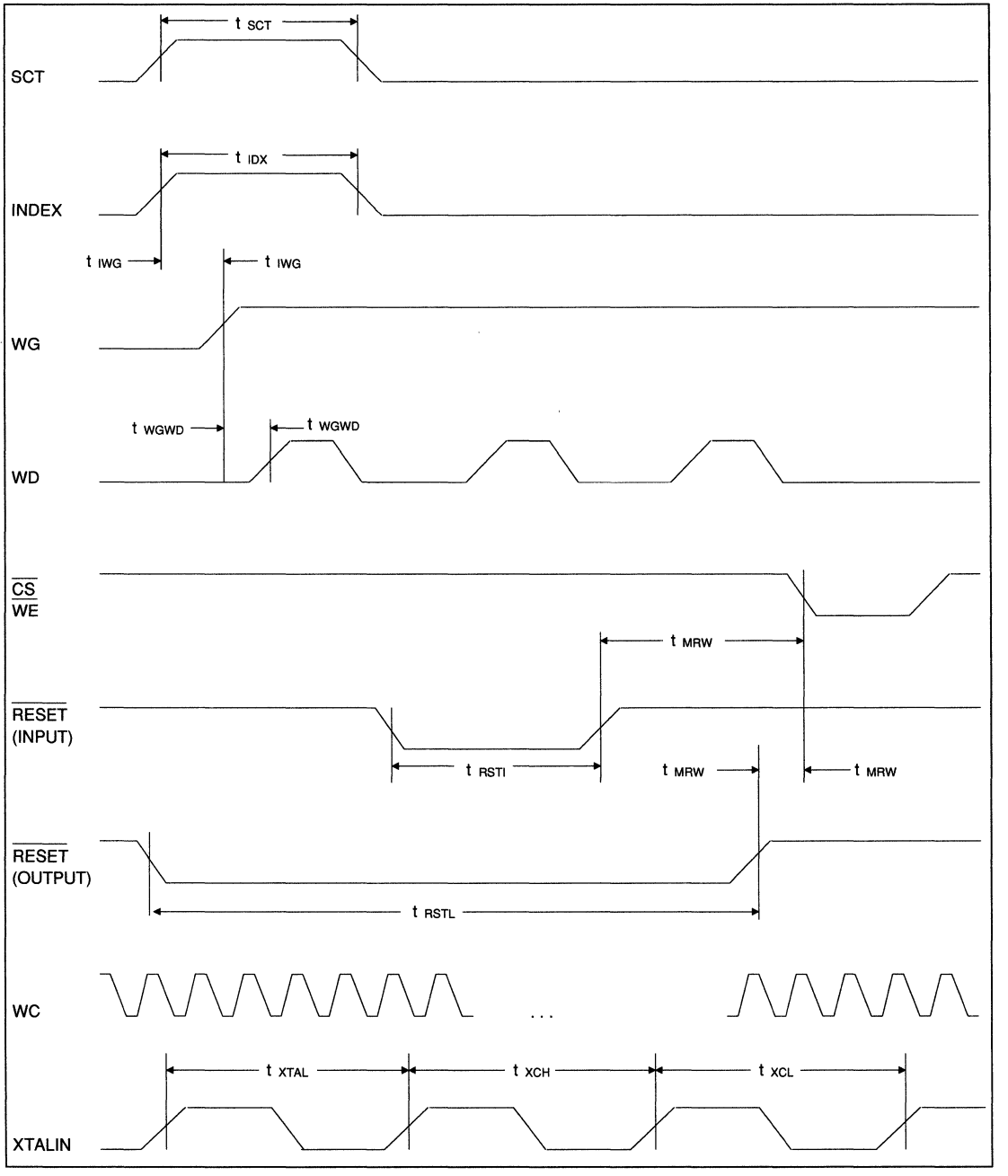


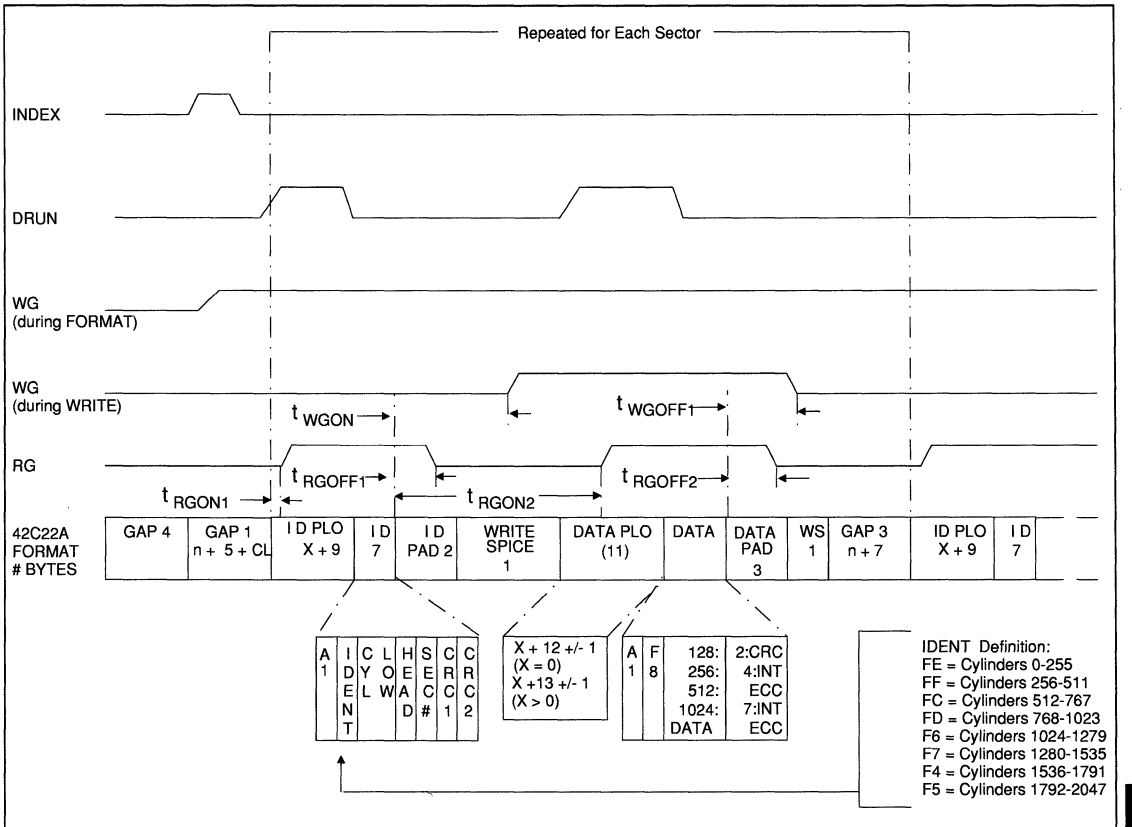
FIGURE 28. MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{IDX}	Index Pulse Width	100		ns	
t_{SCT}	SCT Pulse Width	100		ns	
t_{IWG}	Index to write gate	0	4	WC periods	Gap data=33 in RLL mode. Any gap data in MFM and NRZ.
t_{WGWD}	Write gate to write data	0	4	WC periods	
t_{RSTI}	$\overline{\text{RESET}}$ in pulse width low	24		WC periods	
t_{MRW}	$\overline{\text{MR}}$ Trailing to Host Register Write	2.4		µs	
F_{RCWC}	Difference of RC Frequency from WC Frequency	-15%	+15%		
t_{RSTL}	$\overline{\text{RESET}}$ Out Low Pulse Width during Power-up	51.2		ms	XTAL=10 MHz
t_{RSTL}	$\overline{\text{RESET}}$ Out Low Pulse Width during Power-up	41.3		ms	XTAL=12.5 MHz
t_{RSTL}	$\overline{\text{RESET}}$ Out Low Pulse Width during Power-up	25.6		ms	XTAL=20 MHz
t_{XTAL}	Clock Period	50 70	125	ns	
t_{XCH}	Clock High Time	25 30		ns	
t_{XCL}	Clock Low Time	25 30		ns	

NOTE

t_{XTAL}, t_{XCH}, and t_{XCL} timings at 2.5 V levels.

TABLE 35. MISCELLANEOUS TIMING

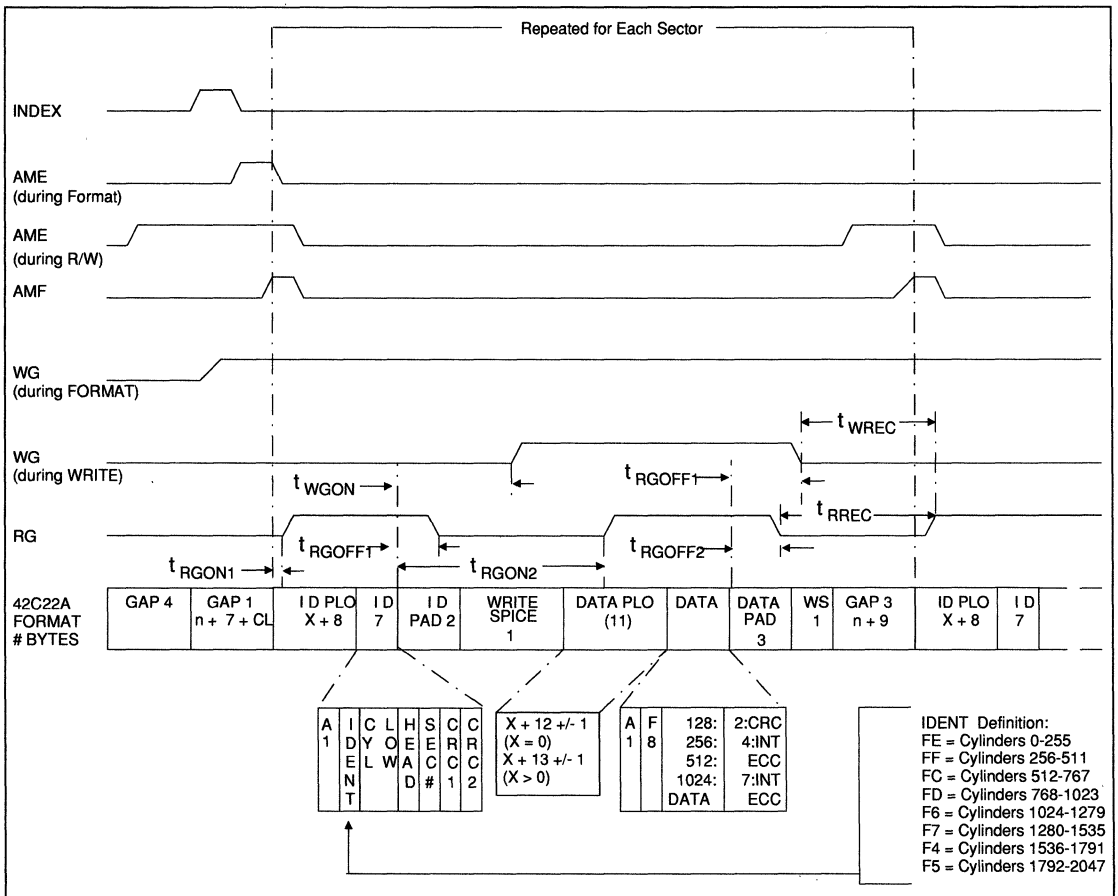


33

NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = 19 ± 1 bit times with respect to DRUN.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.

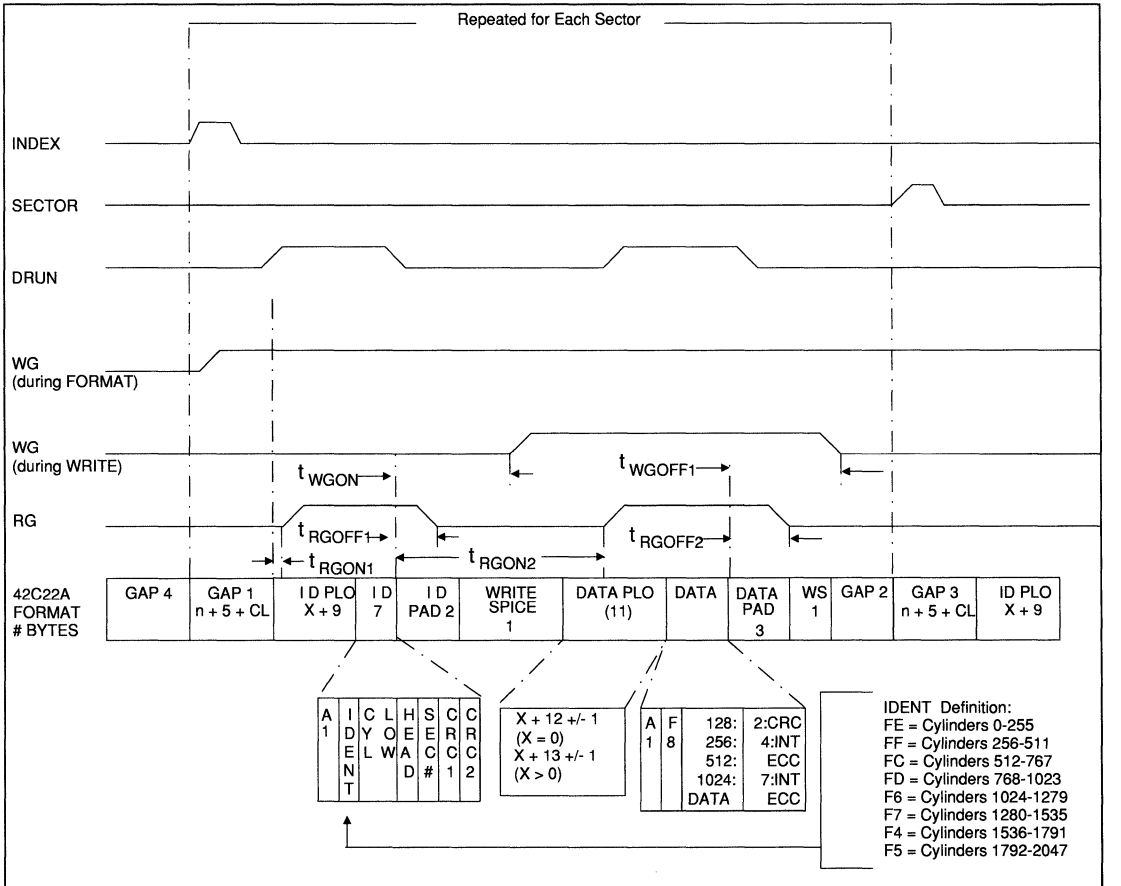
FIGURE 29. SOFT SECTOR MFM/RLL TRACK FORMAT



NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to NRZRD in.
5. t_{WGOFF1} = 28 bit times with respect to NRZWD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to NRZRD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to NRZRD in.
8. t_{RGON1} = 3 ± 1 bit times with respect to AMF.
9. t_{RGON2} = 35 + 1 bit times with respect to NRZRD in.
10. t_{WREC} = 21 to 35 bytes minimum. t_{RREC} = 23 bytes minimum.

FIGURE 30. SOFT SECTOR NRZ TRACK FORMAT

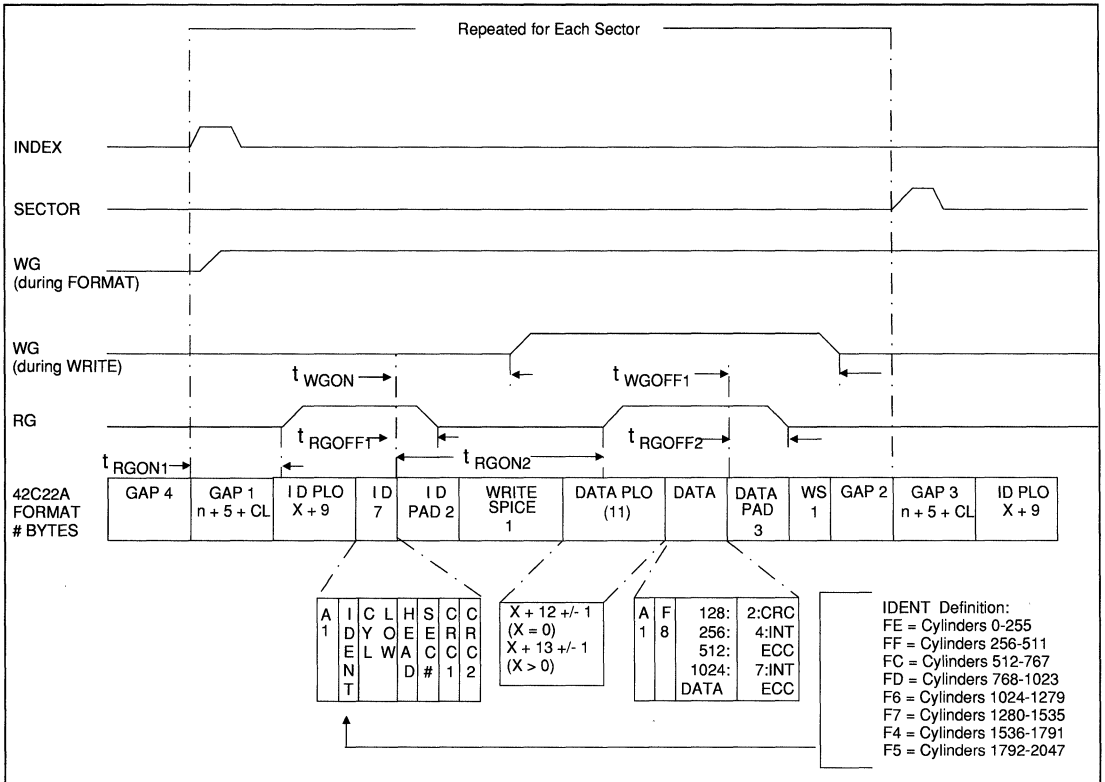


NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = 19 ± 1 bit times with respect to DRUN. SECTOR is tied to DRUNSCT during format. DRUN is tied to DRUNSCT during read and write.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.
10. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.

GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)

FIGURE 31. HARD SECTOR RLL/MFM TRACK FORMAT (WITH SOFT SECTOR READ/WRITE)

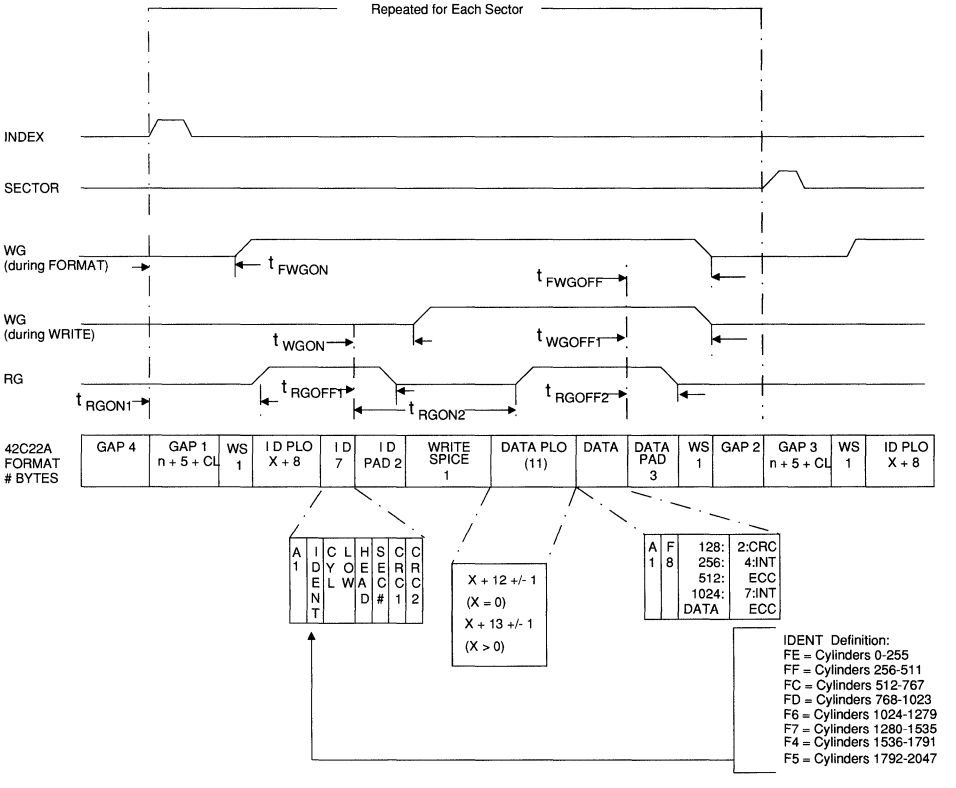


NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = z + CL byte times with respect to INDEX/SECTOR (SCT). SECTOR is tied to DRUNSCT always. z = contents of internal GAP register.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.
10. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.

GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)

FIGURE 32. HARD SECTOR RLL/MFM TRACK FORMAT (WITH HARD SECTOR READ/WRITE AND CONTINUOUS WG OPTION)

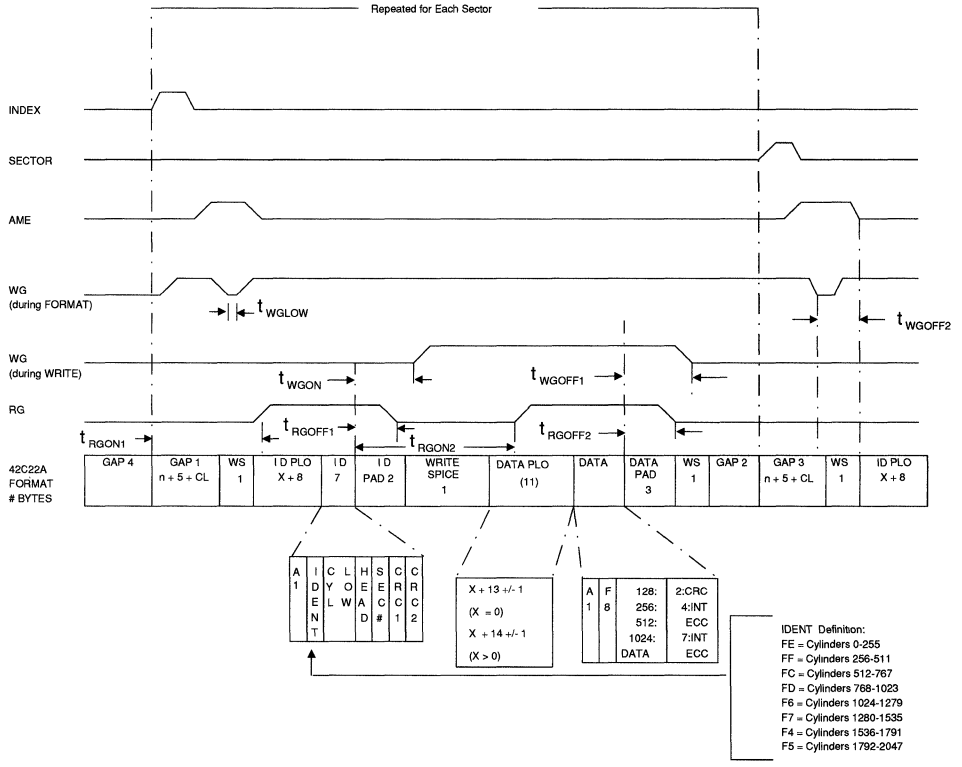


33

NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = z + CL byte times with respect to INDEX/SECTOR (SCT). SECTOR is tied to DRUNSCT always. z = contents of internal GAP register.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.
10. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.
GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)
11. t_{FWGON} = n + 5 + CL byte times with respect to INDEX/SECTOR. t_{WGOFF} = 20 bit times with respect to WD out.

FIGURE 33. HARD SECTOR RLL/MFM TRACK FORMAT (WITH HARD SECTOR READ/WRITE AND WG PULSE)



NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0.
4. t_{WGON} = 17 ± 1 bit times with respect to NRZRD in.
5. t_{WGOFF1} = 28 bit times with respect to NRZWD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to NRZRD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to NRZRD in.
8. t_{RGON1} = z + CL byte times with respect to INDEX/SECTOR (SCT). z = contents of internal GAP register.
9. t_{RGON2} = 35 + 1 bit times with respect to NRZRD in.
10. t_{WGLOW} = 2 bit times. t_{WGOFF2} = 8 bit times. Both timings with respect to NRZWD out.
11. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.
GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)

FIGURE 34. HARD SECTOR NRZ TRACK FORMAT

5.4 PACKAGE DIAGRAMS

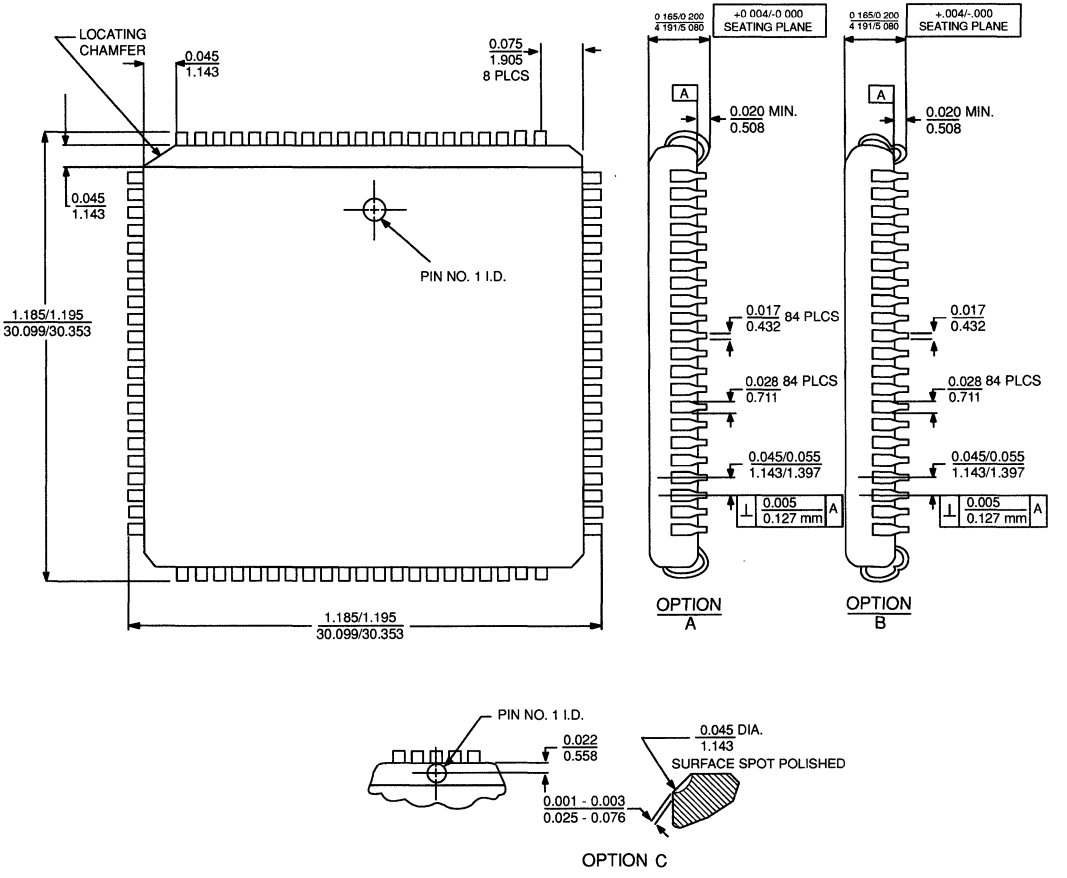


FIGURE 35. 84-LEAD PLCC

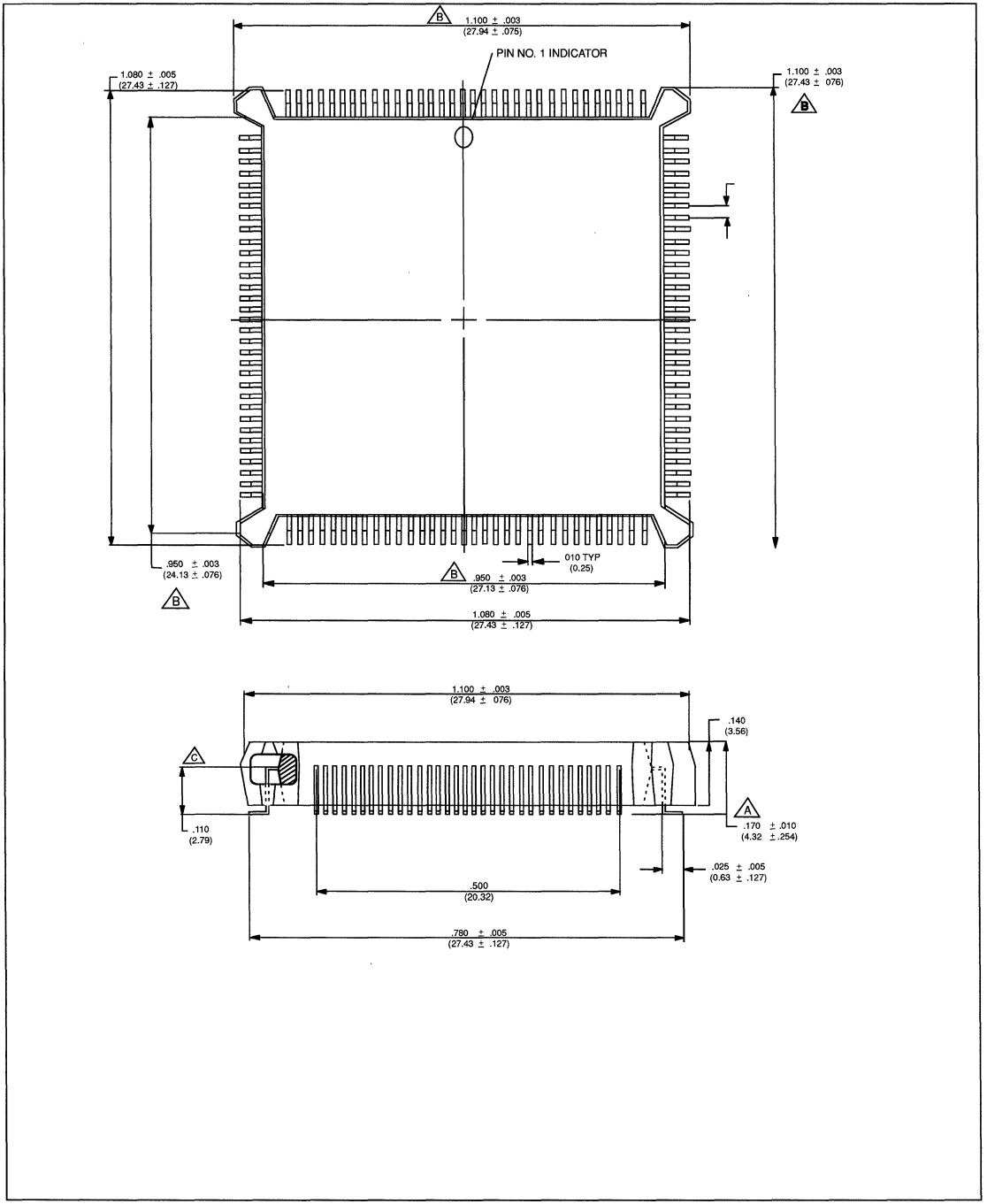


FIGURE 36. 84-LEAD PQFP

WD57C65

Floppy Disk Subsystem

Controller Device

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

1.1 FEATURES

- IBM PS/2 and IBM PC XT Compatible
- 100% Software Compatible with WD37C65B
- Integrated High Performance DPLL Data Separator
  - —<10E-9 industry standard error rates
  - —Data rates of 125, 250, 300, 500 Kbits/second
- Automatic Write Precompensation
  - —Defeat option
  - —Programmable values of 62,125,187, and 250 nanoseconds for standard data rates.
- On Chip Clock Generation
  - —Two TTL clock inputs (44 pin PLCC)
  - —One XTAL oscillator circuit for standard data rates.
- Enhanced Host Interface
  - —Read/write accesses compatible with an 8 or 12 MHz 286 microprocessor with 0 wait states
  - —Twenty LSTTL output drive capability
  - —TTL Schmitt trigger inputs (except Data Bus)
- Direct Floppy Disk Drive Interface - No Buffers Needed
  - —48mA sink output drivers
  - —Schmitt trigger input line receivers
  - —Supports three drives
- Complete Application Support for Systems Compatible with the IBM PS/2 and IBM PC XT.
  - —Register file on chip.
  - —PC XT mode provides required signal qualification to DMA channel
  - —BIOS compatible

1.2 DESCRIPTION

The WD57C65 Floppy Disk Subsystem Controller is an LSI device which incorporates all the functional blocks that typically make up a floppy disk subsystem controller, such as the formatter/controller, data separation, write precompensation, data rate selection, clock generation, and floppy drive interface drivers and receivers. Traditionally, data rate selection, drive selection, and motor control have been output ports of the host processor's architecture. The WD57C65 provides all the necessary status and control registers necessary to integrate all the functions of the floppy disk subsystem on a single chip.

The WD57C65 is designed for systems compatible with the IBM PS/2 and IBM PC XT and interfaces with three 5.25 or 3.5-inch floppy disk drives. It is available in a 40-pin, totally encapsulated plastic DIP or a 44-pin PLCC package.

The WD57C65 retains the core of the WD37C65B floppy disk controller so that the Micro-Sequencer is functionally equivalent and all commands will execute identically to ensure software compatibility. The Control State Machine is also functionally equivalent. The Micro-Sequencer and the Control State Machine operate at eight times the selected bit data rate in MFM and sixteen times the bit data rate in FM.

2.0 ARCHITECTURE

Figure 1 shows a block diagram of the WD57C65 "superchip".

2.1 HOST INTERFACE

The host interface provides the standard host access signals (eight control signals and eight data signals), but with enhanced timing. A detailed interface description appears in the Interface section of this document.

2.2 FLOPPY DRIVE INTERFACE

The floppy drive interface provides data separation that has been designed to address high-performance error rates on floppy disk drives. It contains all the necessary logic to achieve 2nd order, type 2, phase-locked loop performance. Write precompensation is included along with the usual formatting, encoding/decoding, stepper motor control, and status sensing functions. A detailed interface description appears in the Interface section of this document.

2.3 CLOCK AND TIMING GENERATOR

This logical block provides all the clocks needed by the WD57C65: Master Clock, Write Clock and Sampling Clock. Sampling Clock (SCLK) is the clock which drives the digital phase lock loop data separator that is used during data recovery. This clock frequency is always 32 times the selected data rate. The encoder logic uses the Write Clock (WCLK) to place MFM or FM on the serial Write Data stream to the disk. WCLK always has a frequency two times the selected data rate. Master clock (MCLK) is used by the microsequencer. MCLK and MCLK/ clock all latches in a two-phase scheme. One microinstruction cycle is four MCLK cycles. MCLK has a frequency equal to eight times the selected MFM data rate or 16 times the FM data rate. Table 1 presents the Clock Data Rates. Figure 2 illustrates the XTAL oscillator circuits for the 44-pin PLCC configuration.

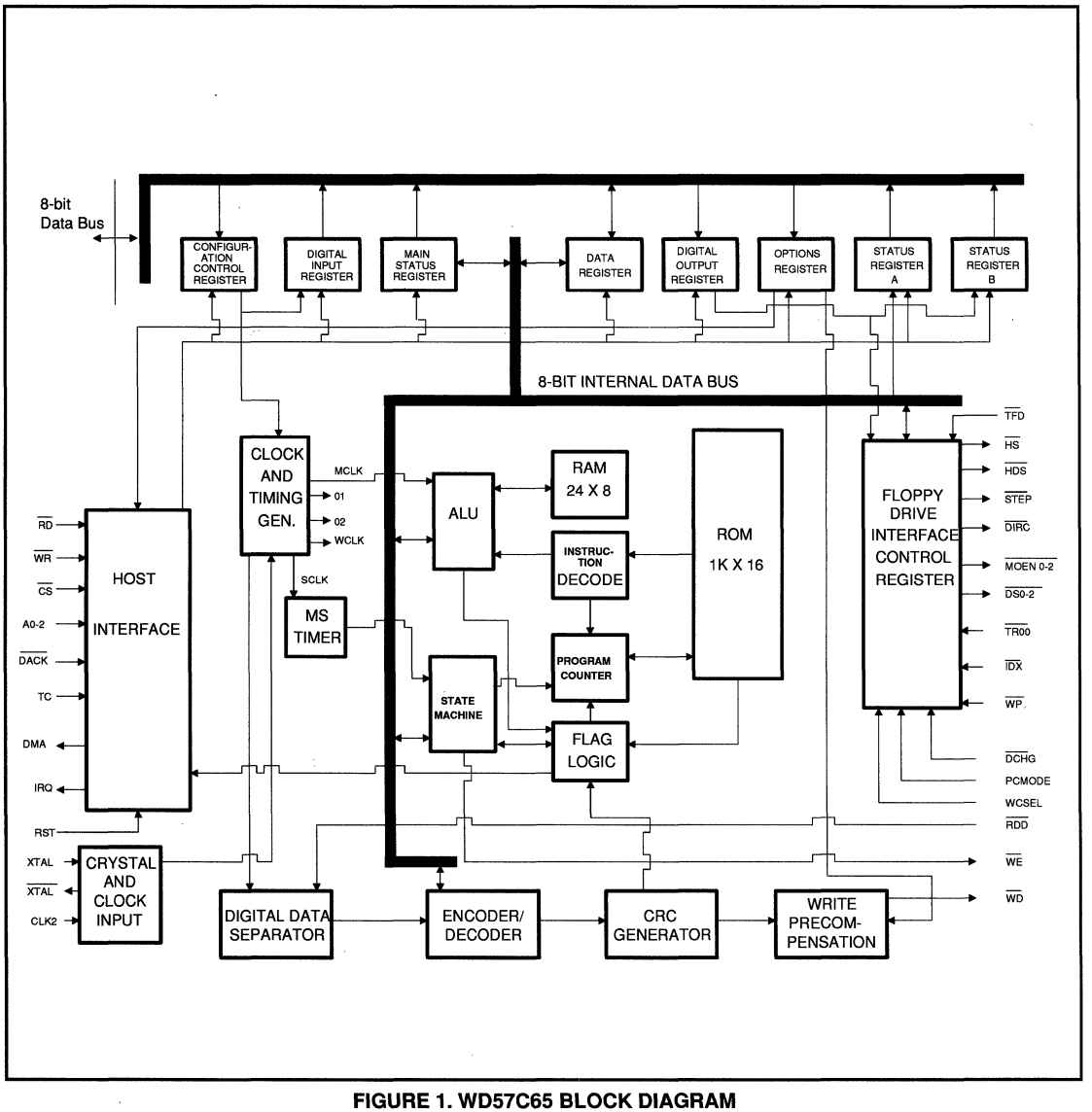


FIGURE 1. WD57C65 BLOCK DIAGRAM

2.4 CRYSTAL AND CLOCK INPUT

An XTAL oscillator circuit (Figure 2) provides the necessary signal for internal timing when using the 44-pin PLCC package. There is one 16 Mhz oscillator on the WD57C65 which handles all standard data rates (500, 250, 125 Kbits/sec) and one TTL level clock input used for non-standard data rates; e.g. 300 Kbits/second used in PC AT designs. **Note, however, that the WD57C65 does not support the IBM PC AT due to register address mapping conflicts.**

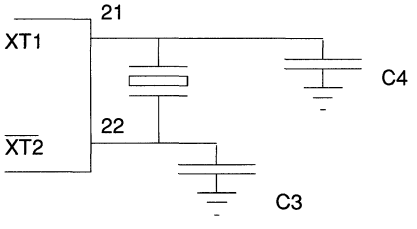
When using the 40-pin DIP, one TTL level clock input handles the standard data rates. The 40-pin DIP does not support non-standard rates.

2.5 WRITE PRECOMPENSATION

The WD57C65 maintains the standard first level algorithm to determine when write precompensa-

TABLE 1. CLOCK DATA RATE

DATA RATE	CODE	SCLK	MCLK	WCLK
500 kb/s	MFM	16.0 MHz	4.0 MHz	1.0 MHz
250 kb/s	FM	8.0 MHz	4.0 MHz	500 KHz
250 kb/s	MFM	8.0 MHz	2.0 MHz	500 KHz
125 kb/s	FM	4.0 MHz	2.0 MHz	250 KHz
300 kb/s	MFM	9.6 MHz	2.4 MHz	600 KHz



16.0 MHz +/- 100 ppm
R series = 30 Ohms maximum
C shunt = 10 pf maximum
C3 = 47 pf 5% mica
C4 = 15 pf 5% mica

FIGURE 2. XTAL OSCILLATOR CIRCUITS FOR THE 44-PIN PLCC

tion should be applied. These EARLY and LATE signals are used internally to select the appropriate delay in the Write Data pulse stream. The encoded write data signal is synchronized to the 16 MHz clock, if this is the frequency on pin XTAL, and clocked through a shift register. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexer gates the chosen bit to the output. The output data pulse width has 25% duty cycle, i.e. one-fourth of the bit cell period, also equal to half of the WCLK period.

The Write Precompensation value is micro programmable. The precompensation values are defined by two bits in the Options Register (bit 2 and 3). After reset the default value for Precompensation is +/- two clocks and is valid for all tracks. There is no write precompensation value for FM. Precompensation can be disabled by the use of bit 2 in the Configuration Control Register for models compatible with the IBM PS/2 Model 30. For models compatible with the IBM PS/2 Models 50,60 and 80, bit 4 in the Options Register disables Write precompensation. The precompensation value is independent of track.

2.6 DATA SEPARATOR

The Data Separator is a WD92C32 Digital Phase Lock Loop Floppy Disk Data Separator (DPLL). It was designed to address high performance error rates on floppy disk drives, and to provide superior performance in terms of available bit jitter tolerance. It contains the necessary logic to achieve classical 2nd order, type 2, phase-locked loop performance. Figure 3 is a simplified block diagaram of the WD92C32. The bit jitter tolerance for the data separator is 60%, which guarantees an error rate of <10E-9.

2.7 WD57C65 REGISTERS

The WD57C65 provides nine registers for status, control, option selection and buffering functions. These registers are described in detail in the Interface Description.

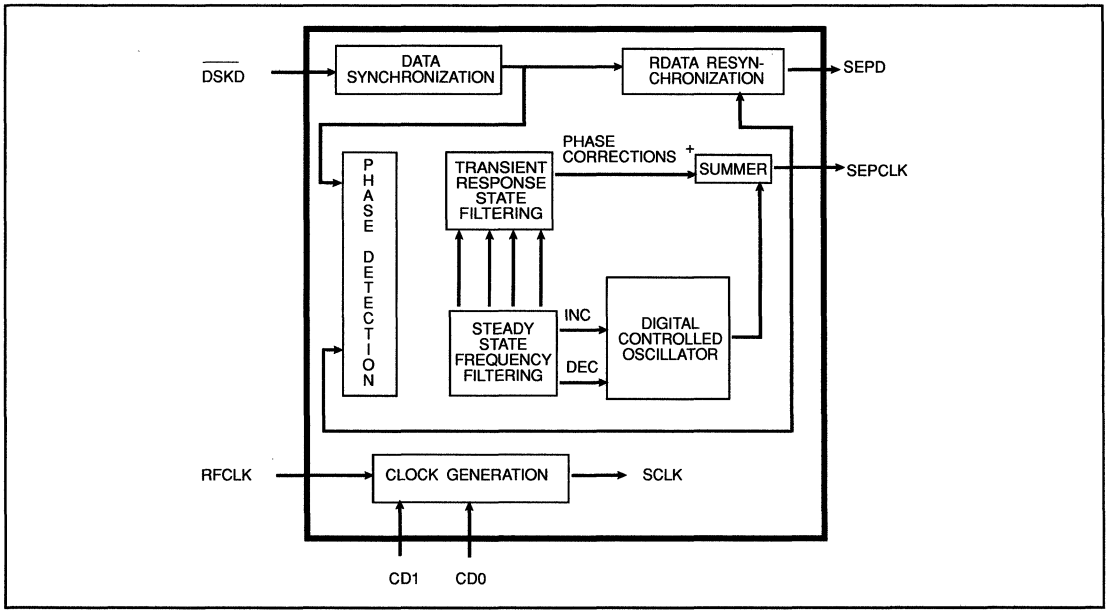


FIGURE 3. WD92C32 SIMPLIFIED BLOCK DIAGRAM

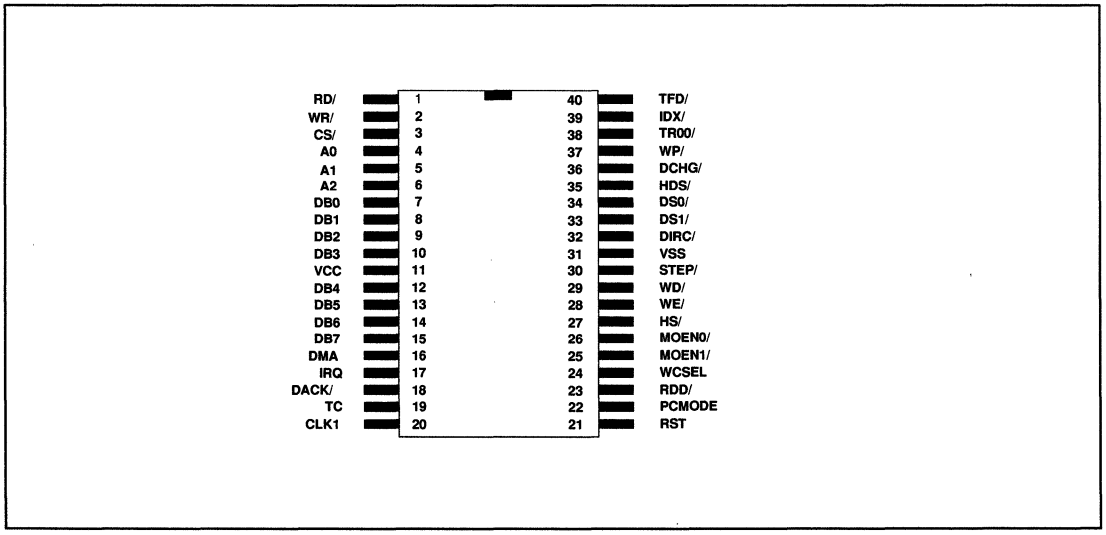


FIGURE 4. WD57C65 40-PIN DIP

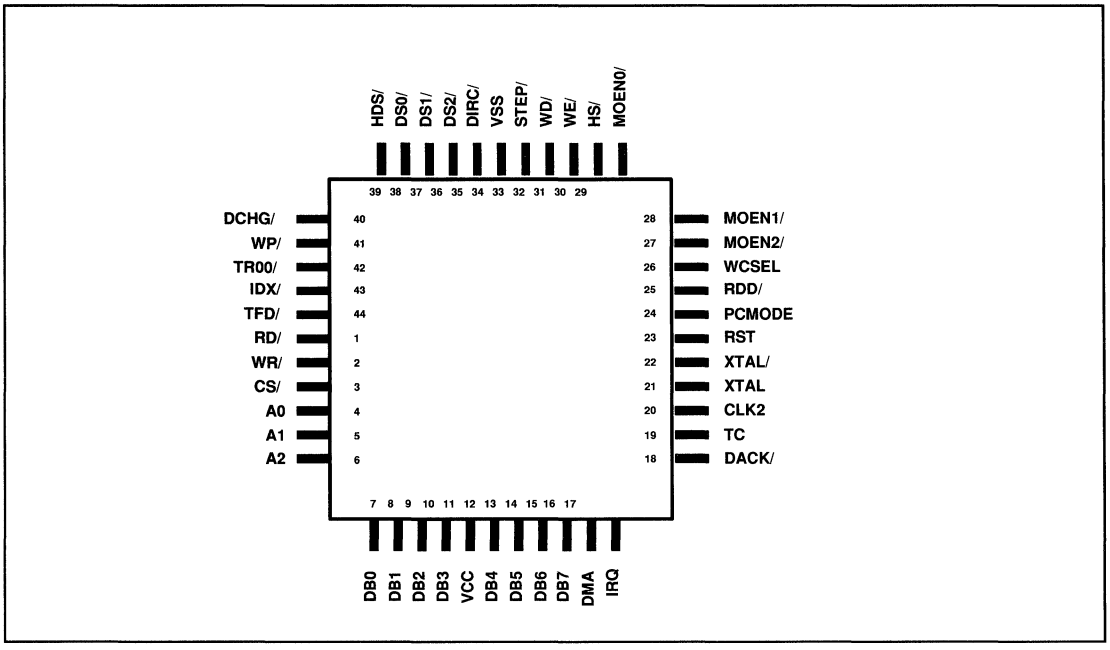


FIGURE 5. WD57C65 44-PIN PLCC

3.0 INTERFACE DESCRIPTION

Figures 4 and 5 show the pinouts of the floppy subsystem controllers for systems compatible with the IBM PS/2. Table 2 provides a pinout signal description of the WD57C65.

Table 2 below lists the DIP/PLCC pin numbers and the corresponding signal and signal function description. Note: For pin numbers separated by a "/", the first number is a DIP pin number. The number following the slash is the PLCC pin number.

D/P PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
1	RD/	Read	I	Control signal for transfer of data or status onto the data bus by WD57C65.
2	WR/	Write	I	Control signal for latching data from the bus into WD57C65 buffer register. Also other registers of Write - only type.
3	CS/	Chip Select	I	Enables RD/ or WR/ operation from the host.
4-6	A0-2	Address	I	Address lines selecting data.
7-10,12-15	DB0-7	Data Bus	I/O	8 bit bi-directional tri-state data bus.
11	VCC			+5V Supply
16	DMA	Direct Memory-Access	O	DMA request for byte transfers of data. In a mode compatible with the IBM PC XT and IBM PS/2 Model 30, this pin is tri-stated, enabled by DMAEN signal from the Digital Output register. In modes compatible with the IBM PS/2 Models 50, 60 and 80, this internal signal, DMAEN, is always forced valid.
17	IRQ	Interrupt Request	O	Interrupt request indicating completion IRQ/ of command execution or data transfer requests (in non-DMA mode). In modes compatible with the IBM PC XT and PS/2 model 30, this pin is tri-stated, enabled by DMAEN signal from the Digital Output register and is active high. It is open drain for modes compatible with the IBM PS/2 Models 50, 60 and 80, requires external pull-up, and is active low.
18	DACK/	DMA Acknowledge	I	Used by DMA controller to transfer data from WD57C65 onto the bus. Logical equivalent to CS/ and Addr=101 . In a mode compatible with the IBM PC XT and IBM PS/2 Model 30, this signal is qualified by DMAEN from the Digital Output register. In modes compatible with the IBM PS/2 Model 50, 60 and 80, this signal is not qualified.
19	TC	Terminal Count	I	This signal indicates to WD57C65 that TC/ data transfer is complete. TC is always qualified by DACK/. In the IBM PC XT and IBM PS/2 Model 30, qualification by DACK/ requires Digital Output Register signal DMAEN to be logically true. In the IBM PS/2 models 50, 60 and 80, TC is active low, and the internal signal DMAEN is always forced valid.
20/NA	CLK1	Clock 1	I	16 MHz TTL level clock input used to generate all internal timings for standard data rates. Non-standard data rates (300 Kbits/second) are not supported by the 40-pin DIP package.

TABLE 2. PINOUT DESCRIPTION

D/P PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
NA/20	CLK2	Clock 2	I	TTL level clock input used for non-standard data rates, such as 300 Kbits/second in an IBM PC AT application. Must be 32 times MFM data rate; i.e. 9.6 MHz for 300 Kbits/second, and can only be selected from the Control Register. It has an internal pull-up.
NA/21	XTAL	XTAL	I	Oscillator input requiring 16MHz crystal. This oscillator is used for all standard data rates. It may be driven with a TTL level signal.
NA/22	XTAL/	XTAL	O	XTAL oscillator drive output fro 44-pin PLCC.
21/23	RST	Reset	I	Resets controller, placing micro-sequencer in idle. Resets device outputs.
22/24	PCMODE	PC MODE	I	PC application mode select. Selects a mode compatible with the IBM's PC XT and IBM PS/2 Model 30, or a mode compatible with the IBM PS/2 Models 50, 60 and 80.
23/25	RDD/	Read Disk Data	I	This Schmitt Trigger (ST) input senses the serial bit stream from the disk drive. The falling edge of each pulse represents a flux transition of the encoded data.
24/26	WCSEL	Write Control Select	I	Allows direct interface to both 5.25 and 3.5-inch floppy disk drives. For logical function see Table 3.
NA/27	MOEN2/	Floppy Drive Motor Enable	O	This high current driver (HCD) output, when active low, enables disk drive #2. This signal comes from Digital Output Register.
25/28	MOEN1/	Floppy Drive Motor Enable	O	This HCD output, when active low, enables disk drive #1. This signal comes from Digital Output Register.
26/29	MOEN0/	Floppy Drive Motor Enable	O	This HCD output, when active low, enables disk drive #0. This signal comes from Digital Output Register
27/30	HS/	Head Select	O	This HCD output selects the head, or side of the floppy disk that is being read or written. Logic 1 = side 0, logic 0 = side 1.
28/31	WE/	Write Enable	O	This HCD output goes active low just prior to writing on the diskette. This allows current to flow through the write head.
29/32	WD/	Write Data	O	This HCD output is write data. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
30/33	STEP/	Step	O	This HCD output issues an active low pulse for each track-to-track movement of the head. The state of the Direction signal at the trailing edge of the STEP pulse determines the direction of the head motion.

TABLE 2. PINOUT DESCRIPTION (CONT'D)

D/P PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
31/34	VSS			Ground
32/35	DIRC/	Direction Control	O	This HCD output determines the direction of the head stepper motor. Logic 1 = outward motion, logic 0 = inward motion.
35/39	HDS/	High Density Select	O	This HCD output indicates to the drive the appropriate write current level to use for the data rate and media density currently being used. The active logic level used to select between High Density vs Double Density is determined by the WCSEL input pin.
34/38	DS0/	Drive Select 0	O	This HCD output, when active low, enables Drive O's interface. This signal comes from the Digital Output register. This signal is qualified by MOEN0/ active low.
33/37	DS1/	Drive Select 1	O	This HCD output, when active low, enables Drive 1's interface. This signal comes from the Digital Input register. This signal is qualified by MOEN1/ active low.
NA/36	DS2/	Drive Select 2	O	This HCD output, when active low, enables Drive 2's interface. This signal comes from the Digital input Digital Input register. This signal is qualified by MOEN2/ active low.
36/40	DCHG/	Diskette Change	I	This is a Schmitt Trigger input which is an active low signal when the disk drive door is open or if the diskette has possibly changed since last drive selection. This status is reflected in the Digital Input Register.
37/41	WP/	Write Protected	I	This Schmitt Trigger input indicates status from the disk drive, going active low when a diskette is Write Protected.
38/42	TR00/	Track 00	I	This Schmitt Trigger input indicates status from the drive, going active low when the head is positioned over the outermost track, track 00.
39/43	IDX/	Index	I	This Schmitt Trigger input indicates status from the drive, going active low when the head is positioned over the beginning of a track marked by an index hole.
40/44	TFD/	Twp Floppy Drive	I	This Schmitt Trigger input indicates status from the drive, going active low when a second drive is installed.

TABLE 2. PINOUT DESCRIPTION (CONT'D)

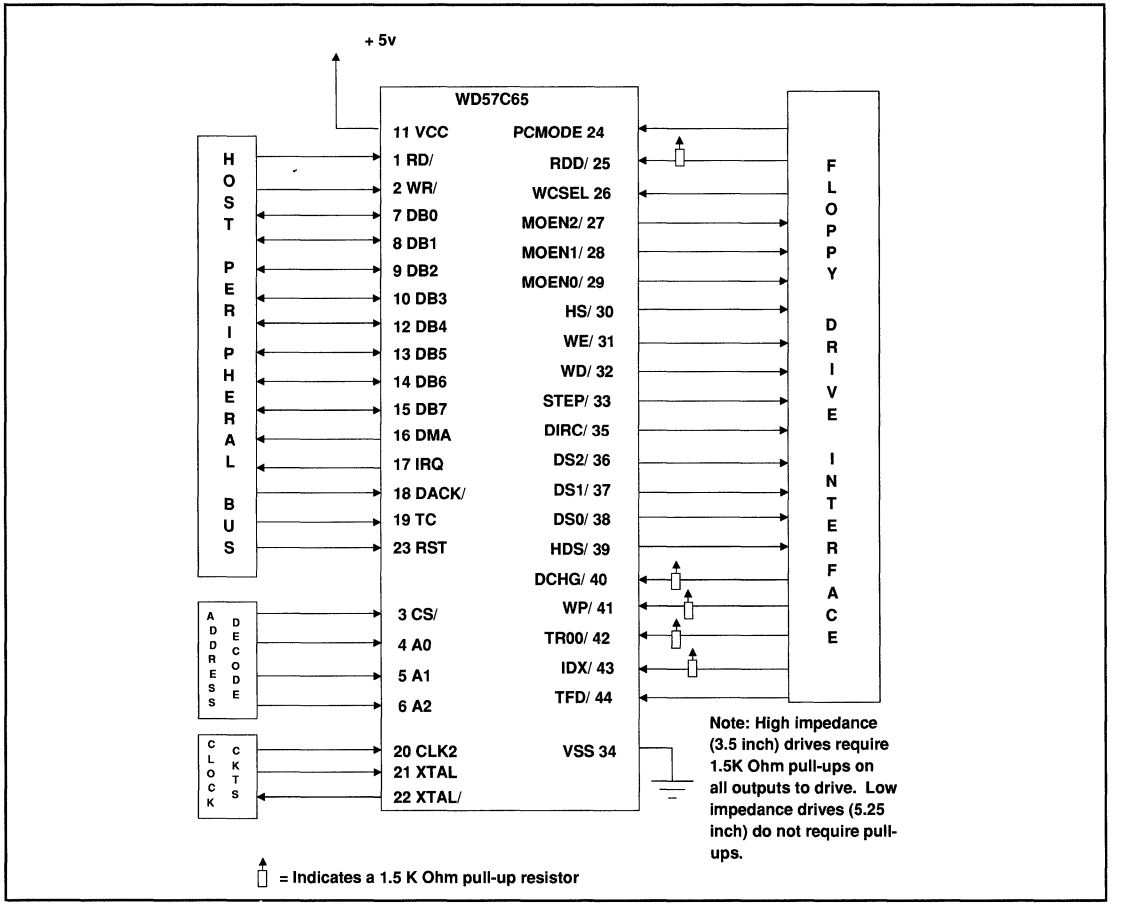


FIGURE 6. TYPICAL WD57C65 SYSTEM

Figure 6 illustrates a typical interface system for the WD57C65.

3.1 FLOPPY DRIVE INTERFACE

The WD57C65 Floppy Drive Interface provides different options than its predecessor, the WD37C65B. Most notably, it supports three drives rather than just two. A new input signal, Write Control Select (WCSEL) allows interfacing with 5.25 and 3.5 inch floppy drives. WCSEL and the selected data rate determine the correct logical level on the High Density Select (HDS/) output pin. If WCSEL = 0, HDS/ = CR0/. If WCSEL =1, HDS/ = CR1. Refer to Table 3, HDS Truth Table.

PCMODE input signal selects either IBM PC XT-PS/2 30 mode or the PS/2 50, 60, and 80 mode. WD57C65 does not support IBM AT systems.

Since PS/2 compatible systems require a Two Floppy Drive (TFD/) pin, the WD57C65 provides TFD/ and has dropped the PCVAL pin used for precompensation in the WD37C65B predecessor. Write precompensation values are determined by bits 2 and 3 in the Options Register. The reset default value for write precompensation is +/- 2 clocks.

3.2 HOST INTERFACE

Host Microprocessor Peripheral Bus provides eight control signals and eight data signals. In the XT and PS2 30 mode, IRQ and DMA Request are tri-stated and enabled by DMAEN, which is internally provided by the Digital Output Register. In PS/2 50, 60 and 80 mode, IRQ is open drain, active low, requires external pull-up, and DMAEN is always forced valid. The data bus, DMA, and IRQ outputs are designed to handle 20 LSTTL loading. Inputs, except the data bus, are Schmitt trigger receivers and can be hooked up to a bus or backplane without any additional buffering.

DATA RATE AND CODE	WCSEL	HDS	DESCRIPTION
500 K MFM or 250 K FM	0 1	1 0	5.25" High Density / 1.2 MByte FDD 3.5" High Density / 1.44 MByte FDD
300 K MFM	0 1	0 0	5.25" Double Density / 1.2 MByte FDD Not Defined
250 K MFM or 125 K FM	0 1	1 1	5.25" Double Density / 360 KByte FDD 3.5" Double Density / 720 KByte FDD or 1.44 MByte FDD
125 K FM	0 1	0 1	5.25" Single Density / 360 KByte FDD 3.5" Single Density / 720 KByte FDD

TABLE 3. HDS TRUTH TABLE

During the command or result phases, the Main Status Register must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data is read from or written into the Data Register, the CPU should wait for 12 microseconds before reading the Main Status Register. Bits D6 and D7 in the Main Status Register must be in a "0" and "1" state, respectively, before each byte of the command word may be written into the WD57C65. Many of the commands require multiple bytes. As a result, the Main Status Register must be read prior to each byte transfer to the WD57C65. During the result phase, Bits D6 and D7 in the Main Status Register must both be "1's" before reading each byte from the Data Register. Note that this reading of the Main Status Register before each byte transfer to the WD57C65 is required only in the command and result phases, and not during the execution phase. Note also that DB6 and DB7 in the MSR can be polled instead of waiting 12 microseconds.

During the execution phase, the Main Status Register need not be read. If the WD57C65 is in the non-DMA mode, then receipt of each data byte (WD57C65 is reading data from the FDD) is indicated by an interrupt signal on pin 17 (IRQ=1). The generation of a Read signal (RD=0) will clear the interrupt as well as output the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13 microseconds for the MFM mode and 27 microseconds for the FM mode), then it may poll the Main Status Register and bit D7 (RQM) functions as the interrupt signal. If a Write command is in process, then the WR signal performs the reset to the Interrupt signal.

All timing mentioned above is double for mini-floppy (5.25-inch) data rates.

Note that in the non-DMA mode it is necessary to examine the Main Status Register to determine the cause of the interrupt since it could be a data interrupt or a command termination interrupt, either normal or abnormal. If the WD57C65 is in the DMA mode, no interrupt signals are generated during the execution phase. The WD57C65 generates DMA requests when each byte of data is available. The DMA controller responds to this request with both DACK/ = 0 (DMA Acknowledge) and a RD/ =0 (Read signal). When the DMA Acknowledge signal goes low (DACK/ = 0), then the DMA Request is cleared (DMA = 0). If a Write Command has been issued, then a WR signal will appear instead of RD. After the execution phase has been completed (Terminal Count has occurred or the EOT sector is read or written), then an interrupt occurs (IRQ = 1). This signifies the beginning of the Result phase. When the first byte of data is read during the result phase, the Interrupt automatically clears (IRQ = 0).

The RD/ or WR/ signals should be asserted while DACK/ is true. The CS/ signal is used in conjunction with RD/ and WR/ as a gating function during programmed I/O operations. CS has no effect during DMA operations. If the non-DMA mode is chosen, the DACK/ signal should be pulled up to VCC. During the result phase all bytes shown in the Command Table must be read. The Read Data Command, for example, has several bytes of data in the result phase. All seven bytes must be read in order to successfully complete the Read Data command. The WD57C65 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes

ADDRESS MAP	CS/	A2	A1	A0	R/W/RW
Status Register A	0	0	0	0	Read only
Status Register B	0	0	0	1	Read only
Digital Output Register	0	0	1	0	Write only
Not Defined	0	0	1	1	Not defined
Main Status Register	0	1	0	0	Read only
Main Data Register	0	1	0	1	Read/Write
Options Register	0	1	1	0	Write only
Digital Input Register	0	1	1	1	Read only
Configuration Control Register	0	1	1	1	Write only

TABLE 4. ADDRESS REGISTER MAP

to be read during the result phase. The WD57C65 contains an address decoder for the register file on the host interface side. The address mapping is shown in Table 4. The Main Status Register mentioned may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are available only during the result phase and may be read only after completing a command. The particular command that has been executed determines how many of the status registers will be read.

The bytes of data which are sent to the WD57C65 during the command phase, and are read out of the WD57C65 in the result phase, must occur in the order shown in the Command Table. The command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the command or result phases is allowed. After the last byte of data in the command phase is sent to the WD57C65, the execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the result phase, the command is automatically ended and the WD57C65 is ready for a new command.

4.0 WD57C65 REGISTERS

4.1 CONFIGURATION CONTROL REGISTER

The Configuration Control Register provides support logic that latches the three least significant bits of the data bus upon receiving CS/ Address = 111 and WR/. These bits select the desired data rate, which in turn controls the internal clock generation. Clock switchover is internally "deglitched," allowing continuous operation after changing data rates. If the Configuration Control Register is not used, the data rate is governed by the supplied clock or crystal. The frequency must be 32 times the desired MFM data rate up to a maximum frequency of 16 MHz. This implies a maximum data rate of 500 kbits/second, unless the Configuration Control Register is used.

34

Switching this clock must be "glitchless" or the device will need to be reset. Tables 5 and 6 show the Configuration Control Register.

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	Data Rate	F/F	0	None (1)
1	Data Rate	F/F	0	None (1)
2	Reserved	None	N/A	None
3	Reserved	None	N/A	None
4	Reserved	None	N/A	None
5	Reserved	None	N/A	None
6	Reserved	None	N/A	None
7	Reserved	None	N/A	None

Note 1: 250K data rate is selected if bits 0 and 1 are anything but "0,0" in models compatible with the IBM PS/2 50, 60 and 80.

TABLE 5. CONFIGURATION CONTROL REGISTER FOR SYSTEMS COMPATIBLE WITH IBM PS/2 50, 60 AND 80

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	Data Rate	F/F	0	None (3)
1	Data Rate	F/F	0	None
2	No Write Precompensation	F/F	0	None
3	Reserved	None	N/A	None
4	Reserved	None	N/A	None
5	Reserved	None	N/A	None
6	Reserved	None	N/A	None
7	Reserved	None	N/A	None

Note 3: Undefined in applications compatible with IBM PS/2 30, but supported by the 57C65.

TABLE 6. CONFIGURATION CONTROL REGISTER FOR IBM PC XT AND IBM PS/2 30

CR1	CR0	DATA RATE	COMMENTS
0	0	500 K	MFM, RST default (Defined in both modes)
0	0	250 K	FM (Undefined in PC applications)
0	1	300 K	MFM (Defined in applications compatible with IBM PC/AT)
1	0	250 K	MFM (Defined in modes compatible with PC XT and PS/2)
1	0	125 K	FM (Undefined in PC applications)
1	1	125 K	FM (Undefined in PC applications)

Bit 2 (CR2) is undefined in the IBM PS/2 50, 60 and 80 modes, and is set to a "1".

Bit 4 (CR4) enables (0) or disables (1) write precompensation in the IBM PS/2 50, 60 and 80 mode.

In the IBM PC XT and PS/2 30 mode, CR2 enables (0) or disables (1) write precompensation

TABLE 7. DATA RATE SELECTION

4.2 MAIN STATUS REGISTER AND STATUS REGISTERS 0-3

The Main Status Register is an eight-bit register that contains the status information of the FDC, and may be accessed at any time. Only the Main Status Register may be read and used to facilitate the transfer of data between the processor and WD57C65. The DIO and RQM bits in the Main Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last RD or WR during a command or result phase and DIO and RQM getting set is 12 microseconds if 500 kbits/second MFM data rate is selected. (If 250 kbits/second MFM is selected the delay is 24 microseconds.) For this reason, every time the Main Status Register is read, the CPU should wait 12 microseconds. The maximum time from the trailing edge of the last RD/ in the result phase to when DB4 (FDC busy) goes low is 12 microseconds. Tables 8 through 12 show the bits in the Master Status Register and Status Registers 0 through 3.

BIT NUMBER	BIT NAME	SYMBOL	DESCRIPTION
DB0	FDD 0 BUSY	D0B	FDD number is 0 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB1	FDD 1 BUSY	D1B	FDD number 1 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB2	FDD 2 BUSY	D2B	FDD number 2 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB3	FDD 3 BUSY	D3B	FDD number 3 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB4	FDC BUSY	CB	A READ or WRITE command is in progress. FDC will not accept any other command.
DB5	EXECUTION MODE	EXM	This bit is set only during Execution phase in non-DMA mode. When DB5 goes low, Execution phase has ended and Results sPhase has started. It operates only during non-DMA mode of operation.
DB6	DATA INPUT	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = 1, then transfer is from Data Register to the processor. If DIO = 0, then transfer is from the processor to Data Register.
DB7	REQUEST FOR MASTER	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

TABLE 8. MAIN STATUS REGISTER BITS

BIT NUMBER	BIT NAME	SYMBOL	DESCRIPTION
D7	INTERRUPT CODE	IC	D7 = 0 AND D6 = 0. Normal termination of command was completed and properly executed.
D6			Execution of command was started but was not successfully completed.
D5	SEEK END	SE	When the FDC completes the SEEK command, this flag is set to 1 (high).
D4	EQUIPMENT CHECK	EC	If the Track 0 signal fails to occur afater 255 step poulses (Recalibrate Command), then this flag is set.
D3	NOT READY	NR	Since drive Ready is always presumed true, this will always be a logic 0.
D2	HEAD SELECT	HS	This flag is used to indicatae the state of the head at interrupt.
D1	UNIT SELECT 1	US1	This flag is used to indicate a Drive Unit Number at interrupt.
D0	UNIT SELECT 0	US0	This flag is used to indicate a Drive Unit Number at interrupt.

TABLE 9. STATUS REGISTER 0 BITS

BIT NUMBER	BIT NAME	SYMBOL	DESCRIPTION
D7	END OF CYLINDER	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D6			Not used. This bit is always 0 (low).
D5	DATA ERROR	DE	When the FDC detects a *CRC error in either the ID field of the data field, this flag is set.
D4	OVERRUN	OR	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D3			Not used. This bit is always 0 (low).
D2	NO DATA	ND	During execution of READ DATA, WRITE DELETED DATA, or SCAN command, if the FDC cannot find the sector specified in the **IDR Register, this flag is set. During execution of the READ ID command, if the FDC cannot read the ID field without an error, then this flag is set. During execution of the READ A TRACK command, if the starting sector connot be found, then this flag is set.
D1	NOT WRITEABLE	NW	During execution of WRITE DATA, WRITE DELETED DATA or FORMAT A TRACK commands, if the FDC detects a WP signal from the FDD, then this flag is set.
D0	MISSING ADDRESS MARK	MA	If the FDC cannot detect the ID Address Maark after encountering the index hole twice, then this flag is set. At the same time the MD (Missing Address Mark in data field) of Status Register 2 is set.

TABLE 10. STATUS REGISTER 1 BITS

BIT NUMBER	BIT NAME	SYMBOL	DESCRIPTION
D7			Not Used. This bit is always 0 (low).
D6	CONTROL MARK	CM	During execution of the jREAD DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D5	DATA ERROR	DD	If the FDC detects a CRC error in the data field, then this flag is set.
D4	WRONG CYLINDER	WC	This bit is related to the ND bit, and when the contents of ***C on the medium is different from that sored in the IDR, this flag is set.
D3	SCAN EQUAL	SH	During execution of the SCAN command, if the condition of "equal" is satisfied, this flag is set.
D2	SCAN NOT	SN	During execution of the SCAN command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D1	BAD CYLINDER	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF, then this flag is set.
D0	MISSING ADDRESS MARK IN DATA FIELD	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or then this flag is set.

TABLE 11. STATUS REGISTER 2 BITS

BIT NUMBER	BIT NAME	SYMBOL	DESCRIPTION
D7			Not used. This bit is always 0 (low).
D6	$\overline{\text{WRITE PROTECTED}}$	$\overline{\text{WP}}$	This bit is used to indicate the status of the WRITE PROTECTED signal from the FDD.
D5	READY	RY	This bit is always a logic 1. Drive is presumed to be ready.
D4	TRACK 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D3	$\overline{\text{WRITE PROTECTED}}$	$\overline{\text{WP}}$	This bit is used to indicate the status of the WRITE PROTECTED signal from the FDD.
D2	HEAD SELECT	HS	This bit is used to indicate the status of the Side Select signal to the FDD.
D1	UNIT SELECT 1	US1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D0	UNIT SELECT 2	US0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

TABLE 12. STATUS REGISTER 3 BITS

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	+ Direction	TSB	N/A	None
1	- Write Protection	TSB	N/A	None
2	- Index	TSB	N/A	None
3	+ Head 1 Select	TSB	N/A	None
4	- Track 0	TSB	N/A	None
5	+ Step	TSB	N/A	None
6	- 2nd Drive Installed	TSB	N/A	None
7	Interrupt	TSB	N/A	None

TABLE 13. STATUS REGISTER A FOR IBM PS/2 50, 60 AND 80

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	- Direction	TSB	N/A	None
1	+ Write Protect	TSB	N/A	None
2	+ Index	TSB	N/A	None
3	- Head 1 Select	TSB	N/A	None
4	+Track 0	TSB	N/A	None
5	+ Step	SR F/F	0	STEP (1)
6	+ DRQ	TSB	N/A	None
7	Interrupt	TSB	N/A	None

TABLE 14. STATUS REGISTER A FOR IBM PC XT AND IBM PS/2 30

4.3 STATUS REGISTER A (CS/ = 0 AND ADDRESS = 000 - READ ONLY)

Note 1: Not synchronized to unknown PAL clocks in systems compatible with the IBM PS2. Reset is forced to logic "0" for test purposes. Also resets to logic "0" when address 3F7 is read and STEP causes a set condition.

TSB = Tri-state buffer

SR F/F = Set Reset Flip Flop

If Storage Element is "none", Reset Condition reflects fixed logic state.

4.4 STATUS REGISTER B (CS/ = 0 AND ADDRESS = 001 - READ ONLY)

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	Motor Enable 0	TSB	N/A	None
1	Motor Enable 1	TSB	N/A	None
2	Write Enable	TSB	N/A	None
3	Read Data	Toggle F/F	0	RDD/ (1)
4	Write Data	Toggle F/F	0	WD/ (2)
5	Drive Select	TSB	N/A	None (3)
6	Reserved	Unused TSB	1	None
7	Reserved	Unused TSB	1	None

Note 1: Not synchronized to unknown PAL clocks in systems compatible with the IBM PS/2 50, 60 and 80. Reset is forced to logic "0" for test purposes.

Note 2: Not synchronized to unknown PAL clocks in systems compatible with the IBM PS/2 50, 60 and 80. Reset is forced to logic "0" for test purposes. This "WD" clock is an internal signal not qualified by WE/ signal.

Note 3: This status reflects Digital Output Register bit 0 only.

TABLE 15. STATUS REGISTER B FOR IBM PS/2 50, 60 AND 80

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	- Drive Select 2	TSB	N/A	None (5)
1	- Drive Select 3	TSB	N/A	None (5)
2	Write Enable	SR F/F	0	WE/ (4)
3	Read Data	SR F/F	0	RDD/ (4)
4	Write Data	SR F/F	0	WD/ (4)
5	- Drive Select 0	TSB	N/A	None (5)
6	- Drive Select 1	TSB	N/A	None (5)
7	Reserved	Unused TSB	0	None

Note 4: Not synchronized to unknown PAL clocks in systems compatible with IBM PS/2 30. Reset is forced to logic "0" for test purposes and when reading address 357. WE/, RDD/ and WD/ are internal signals and cause a set condition.

Note 5: Drive select signals (0-3) are qualified by Motor Enable signals (0-3)

TSB = Tri-state Buffer

SR F/F = Set Reset Flip Flop.

If Storage Element is none, Reset Condition reflects fixed logic state.

TABLE 16. STATUS REGISTER B FOR IBM PC XT AND IBM PS/2 30

A0	A1	A2	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	FUNCTION
1	0	0	0	0	1	Read Main Status Register
1	0	1	0	0	1	Read from Data Register
1	0	1	0	1	0	Write into Data Register

TABLE 17. MASTER STATUS AND DATA REGISTERS RELATIONSHIP

4.5 DATA REGISTER

The eight-bit Data Register stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The relationship between the Master Status Register and the Data Register and the signals RD/, WR/, CS/ and A0-A2 are shown in Table 17.

4.6 DIGITAL OUTPUT REGISTER (CS/=0 AND ADDRESS = 010 - WRITE ONLY)

The Digital Output Register (DOR) provides support logic that latches the data bus upon receiving CS/, Address = 010 and WR/. This register replaces the typical latched port seen in floppy subsystems used to control disk drive spindle motors and select drives. Table 18 illustrates the bit decode (bits 0 and 1 of the DOR) used to select drives 0 through 2. Table 19 provides a bit descsription of the contents of the DOR.

DSEL1	DSEL0	DRIVE
0	0	Drive 0
0	1	Drive 1
1	0	Drive 2
1	1	Not Supported

TABLE 18. BIT DECODE FOR DRIVE SELECT

34

BIT	SIGNAL	FUNCTION
DOR0	DSEL0	Drive Select. If decode select is "0" and MOEN0/ is active low, then DS0/ is selected. If decode select is "1" and MOEN1/ is active low, then DS1/ is selected. If decode select is "2" and MOEN2/ is active low, then DS2/ is selected if in a mode compatible with the IBM PC XT and IBM PS/2 Model 30. Although DS2/ is undefined in applications compatible with the IBM PS/2 50, 60 and 80, the WD57C65 supports DS2/ in both modes.
DOR1	DSEL1	Drive Select
DOR2	SRST/	Soft Reset, active low
DOR3	DMAEN	DMA Enable. Active in a mode compatible with the IBM PC XT and IBM PS/2 Model 30, qualifies DMA and IRQ outputs and also DACK/input. In modes compatible with the IBM PS/2 models 50, 60 and 80 this internal signal is always valid.
DOR 4	MOEN0	Motor enable (Inverted output is MOEN0/)
DOR 5	MOEN1	Motor enable (Inverted output is MOEN1/)
DOR6	MOEN2	Motor enable (Inverted output is MOEN2/) Undefined in applications compatible with the IBM PS/2 50, 60 and 80, but supported by the WD57C65 in both modes.)
DOR7		Reserved

TABLE 19. DIGITAL OUTPUT REGISTER

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	Drive Select	F/F	0	None (1)
1	Drive Select	F/F	0	None (1)
2	- Reset	F/F	0	None
3	Reserved	Unused F/F	N/A	None
4	Motor 0	F/F	0	None
5	Motor 1	F/F	0	None
6	Motor 2	F/F	0	None (1)
7	Reserved	Unused F/F	N/A	None

Note 1: Although undefined in applications compatible with the IBM PS/2 50, 60 and 80, this signal is supported by the WD57C65.

TABLE 20. DIGITAL OUTPUT REGISTER FOR IBM PS/2 50, 60 AND 80

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	Drive Select	F/F	0	None
1	Drive Select	F/F	0	None
2	- Reset	F/F	0	None
3	DMA and Interrupt Enable	F/F	0	None
4	Motor 0	F/F	0	None
5	Motor 1	F/F	0	None
6	Motor 2	F/F	0	None
7	Reserved	Unused F/F	N/A	None (2)

Note 2: This bit is defined as Motor Enable 3 in models compatible with the IBM PS/2 30, but WD57C65 does not support it.

TSB = Tri-state Buffer F/F = Flip Flop

If Storage Element is "none", Reset condition reflects fixed logic state.

TABLE 21. DIGITAL OUTPUT REGISTER FOR IBM PC XT AND PS/2 30

4.7 DIGITAL INPUT REGISTER (CS/=0 AND ADDRESS = 111 - READ ONLY)

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	- High Density Select	TSB	N/A	None
1	Reserved	Unused TSB	1	None
2	Reserved	Unused TSB	1	None
3	Reserved	Unused TSB	1	None
4	Reserved	Unused TSB	1	None
5	Reserved	Unused TSB	1	None
6	Reserved	Unused TSB	1	None
7	Disk Change	TSB	N/A	None

TABLE 22. DIGITAL INPUT REGISTER FOR IBM PS/2 50, 60 & 80

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	Reserved	Unused TSB	0	None
1	250K Rate Select	TSB	N/A	None
2	No Write Precompensation	TSB	N/A	None
3	DMA, Interrupt Enable	TSB	N/A	None
4	Reserved	Unused TSB	0	None
5	Reserved	Unused TSB	0	None
6	Reserved	Unused TSB	0	None
7	- Disk Change	TSB	N/A	None

TSB = Tri-state Buffer
F/F = Flip Flop
If Storage Element is "none" or "unused", Reset Condition reflects fixed logic state.

TABLE 23. DIGITAL INPUT REGISTER FOR IBM PC XT AND PS/2 30

4.8 OPTIONS REGISTER

BIT	SIGNAL	FUNCTION
0	Boot Disk Select	If "0", causes DS1/ and MOEN/1 to be swapped in H/W with DS0/ and MOEN0/. Therefore, if DOR selects Drive 0, then actually Drive #1 will be selected and enabled, allowing a S/W operating system to be booted from the disk drive.
1	SWTC	Software Terminal Count allows a TC to be issued to the core controller under BIOS driver control.
2-3	PCV	These two bits define the precompensation values, as shown in the truth table below.
4	NWP	This bit disables write precompensation in modes compatible with IBM PS/2 50, 60 and 80 only.

TABLE 24. OPTIONS REGISTER

BIT 3	BIT 2	PRECOMP VALUE
0	0	±1 Clock
0	1	±2 Clocks
1	0	±3 Clocks
1	1	±4 Clocks
* RST Default		

TABLE 25. TRUTH TABLE

Note: Clk = Clk 1 for all data rates, except when 300 Kb/s is selected which requires Clk 2. In PS/2 model 30 precompensation can be disabled by using bit 2 in the Configuration Control Register. In PS/2 50, 60 and 80, bit 4 of the Options Register disables precompensation.

BIT	SIGNAL NAME / FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	Boot Disk Select	F/F	0	None
1	SWTC	F/F	0	None
2	PCV	F/F	0	None
3	PCV	SR F/F	1	None
4	No Write Precompensation	F/F	0	None
5	Reserved	Unused F/F	0	None
6	Reserved	Unused F/F	0	None
7	Reserved	Unused F/F	0	None

F/F = Flip Flop SR F/F = Set Reset Flip Flop

TABLE 26. OPTIONS REGISTER

5.0 SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Voltages referenced to VSS	
VCC	7.0 Volts
Voltage at any pin	-0.3 to VCC +0.3 Volts
Storage Temperature	-55^{o} to $+150^{o}$ C
Operating Temperature	0^{o} to $+70^{o}$ C

5.2 DC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
+5V Supply	VCC	4.5	5.5	V
Input Low Voltage - Data Bus & XTOSC	VIL		0.8	V
Input High Volt - Data Bus & XTOSC	VIH	2.0		V
Input Low Threshold-Schmitt Trigger	VILT	0.8		V
Input High Threshold-Schmitt Trigger	VIHT		2.0	V
Schmitt Trigger Input Hysteresis	VIHYS	0.45		V
Output Low - DBx,IRQ,DMA ; Io=12.0mA	VOL		0.4	V
Output High - DBx,IRQ,DMA; Io=-5.0mA	VOH	2.8		V
Output Low - High Current; Io=48mA	VOLHC		0.4	V
PQR trip threshold	VPQR	2.75	4.35	V
Latch Up Current Low	ILUL	40		mA
Latch Up Current High	ILUH	-40		mA
Leakage Current Low	ILL		10	µA
Leakage Current High	ILH		-10	µA
Supply Current - 100µA source loads	ICC		40	mA
Supply Current - 5mA source loads	ICCHL		90	mA
Power Dissipation - ICC max *	PD		400	mW
Power Dissipation - ICCHL max *	PDHL		550	mW

* Includes open drain high current drivers at Vol = 0.4V

5.3 TIMING CHARACTERISTICS (CL=100pf):

PARAMETER	SYMBOL	MIN	MAX	UNIT
Clock Period	tCY	60		nS
Clock Active (High or Low)	tPH	25		nS
Clock Rise Time (Vin 0.8 to 2.0)	tR		5	nS
Clock Fall Time (Vin 2.0 to 0.8)	tF		5	nS
A0-2 Set Up Time to RD- low	tAR	10		nS
A0-2, Hold Time to RD- high	tRA	0		nS
CS-, DACK Set Up Time to RD- low	tCDR	0		nS
CS-, DACK Hold Time to RD- high	tRCD	0		nS
RD- Width	tRR	80		nS
Data Access Time from RD- low	tRD		70	nS

PARAMETER	SYMBOL	MIN	MAX	UNIT
DB to Float Delay from RD- high	tDF	10	40	nS
A0-2 Set Up Time to WR- low	tAW	10		nS
A0-2, Hold Time to WR- high	tWA	0		nS
CS-, DACK Set Up Time to WR- low	tCDR	0		nS
CS-, DACK Hold Time to WD- high	tRCD	0		nS
WR- Width	tWW	60		nS
Data Set Up Time to WR- high	tDW	60		nS
Data Hold Time from WR- high	tWD	0		nS
IRQ Reset Delay Time from RD- high	tRI		1MCY+100nS	
IRQ Reset Delay Time from WR- high	tWI		1MCY+100nS	
DMA Cycle Time	tMCY	52		MCY
DMA Reset Delay Time from DACK- low	tAM		80	nS
DACK- Delay Time from DMA high	tMA	0		nS
DACK- Width	tAA	80		MCY
TC Width	tTC	60		nS
Reset Width - TTL driven CLK1	tRST	60		nS
Reset Width - Software Reset	tSRST	5		MCY
RDD- Active Time Low	tRDD	40		nS
WD- Write Data Width Low	tWDD	1/2 (typ)		WCY
DIRC- Hold & Set Up to STEP- low	tDST	4		MCY
DSx- Hold time from STEP- low	tSTU	20		MCY
STEP- Active Time Low	tSTP	24		MCY
STEP- Cycle Time	tSC	132		MCY
DIRC- Hold Time after STEP-	tSTD	96		MCY
IDX- Index Pulse Width	tIDX	2		MCY
RD- Delay from DMA	tMR	0		nS
WR- Delay from DMA	tMW	0		nS
RD- or WR- Response from DMA high	tMRW		48	MCY
Chip Access Delay from RST low - TTL	tCA	32		MCY
Chip Access Delay from SRST- low	tCAS	40		MCY
Chip Access Delay - osc XT1 at 16 MHz	tXCA	500		µS
TC Delay from last DMA or IRQ, RD-	tTCR	0	192	MCY
TC Delay from last DMA or IRQ, WR-	tTCW	0	384	MCY

Note:

1) CY = CLK1 or XT1 period

2) MCY = MCLK period, dependent on selected data rate

3) WCY = WCLK period, dependent on selected data rate

4) Timing based on 3.5-inch floppy data rates.

- **MCY:**
  - 500 KByte MFM = 250 nsec.
  - 250 KByte MFM = 500 nsec.
- **MCLK:**
  - 8.0 MHz = 125 nsec.
  - 4.0 MHz = 250 nsec.
  - 2.0 MHz = 500 nsec.

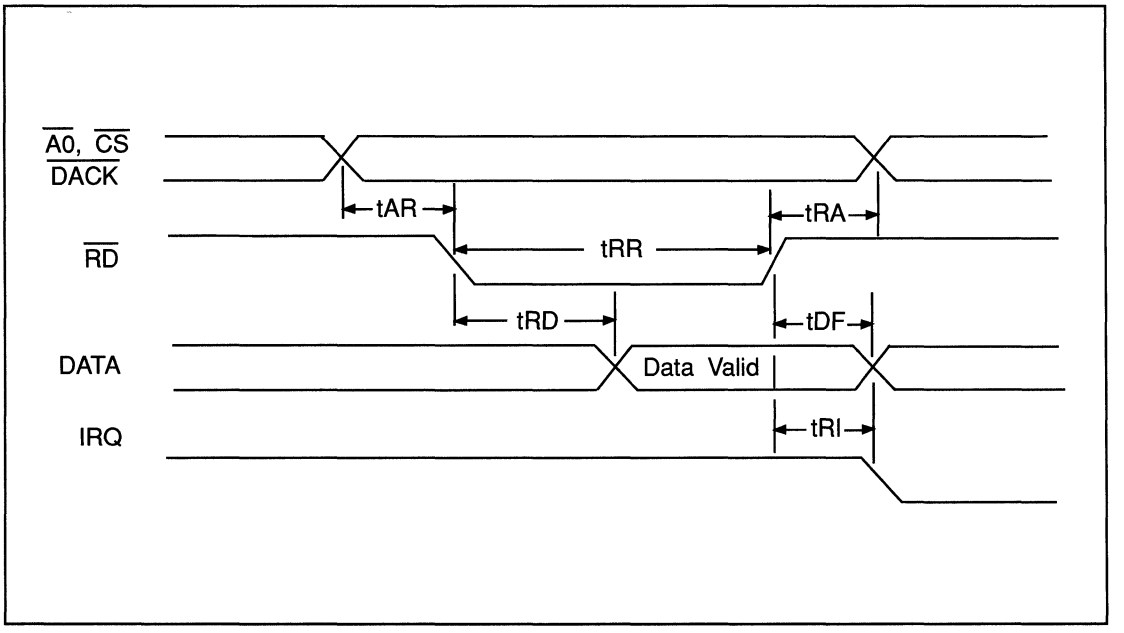


FIGURE 7. READ TIMING

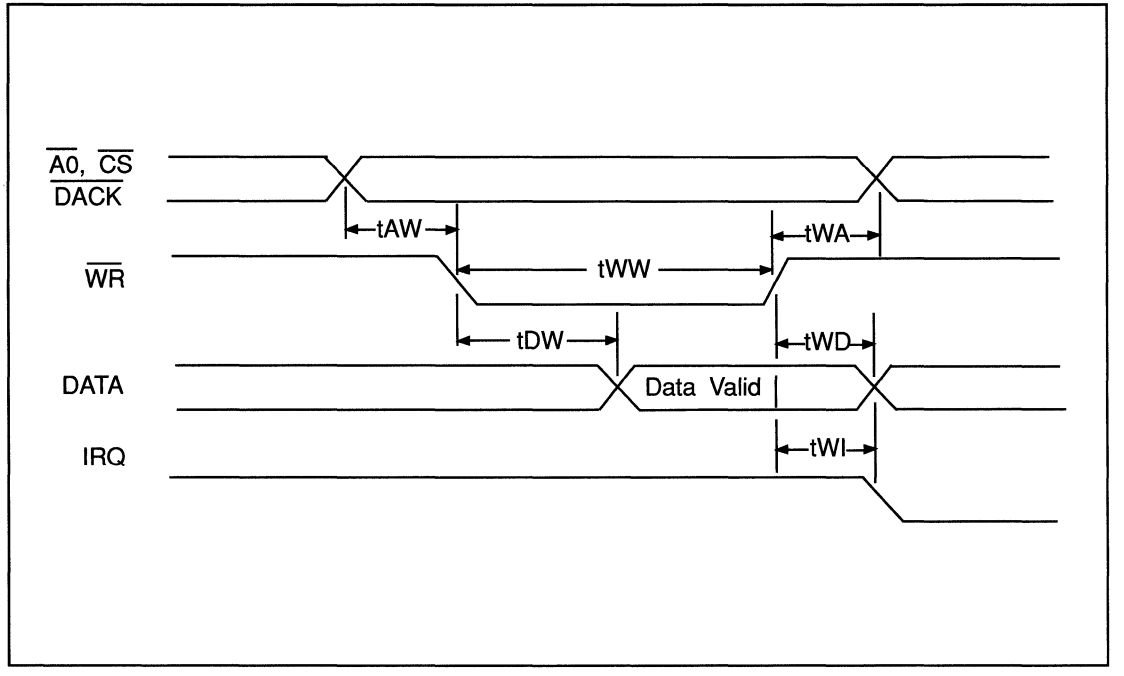


FIGURE 8. WRITE TIMING

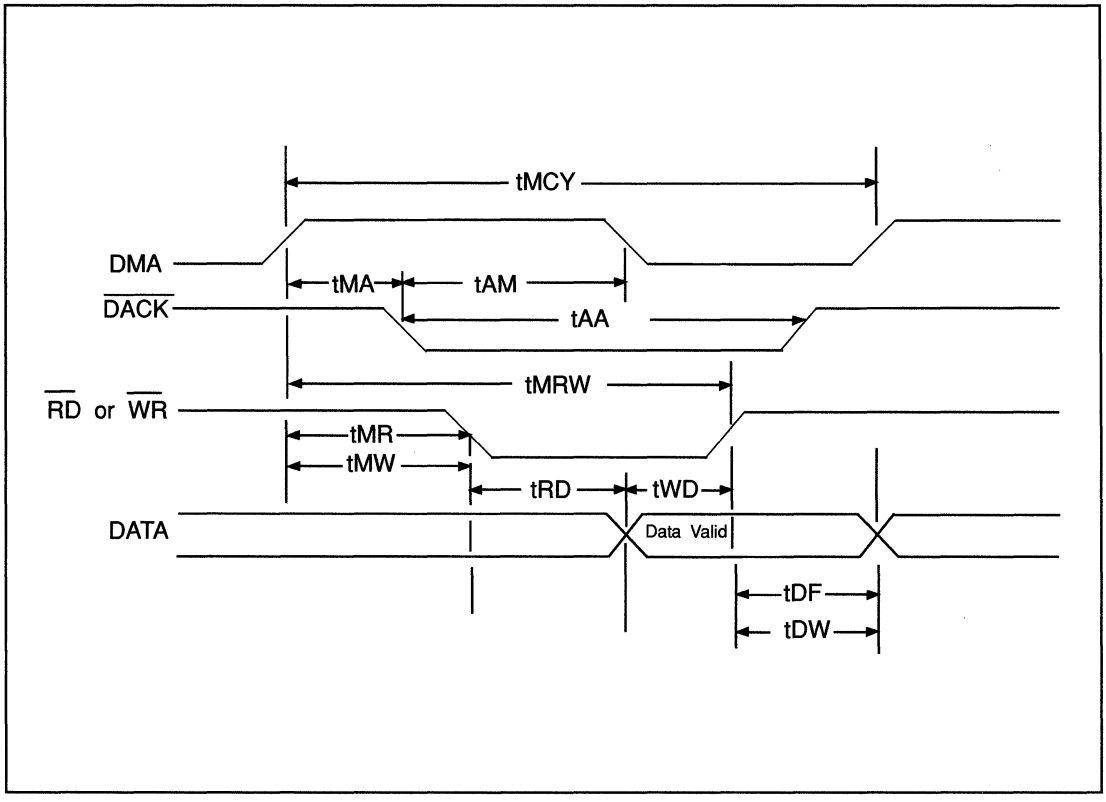


FIGURE 9. DMA TIMING

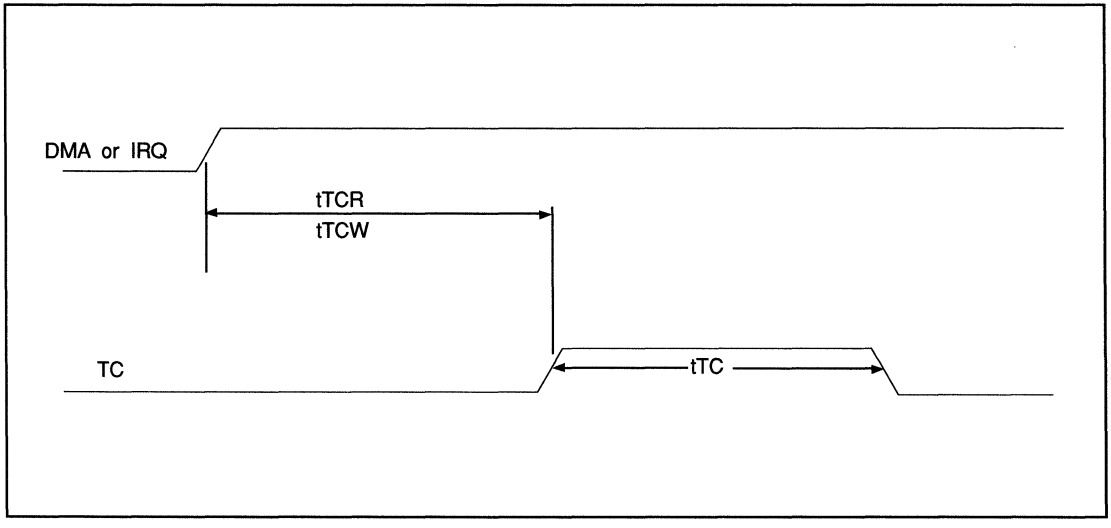


FIGURE 10. TERMINAL COUNT TIMING

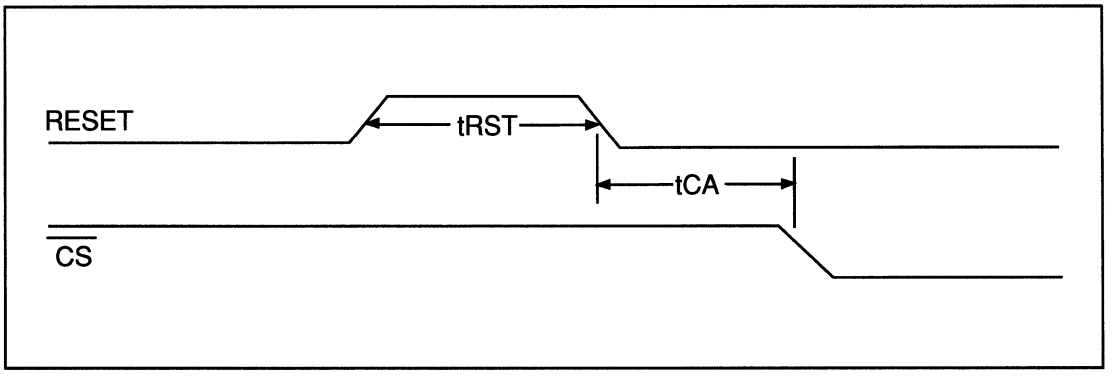


FIGURE 11. RESET TIMING

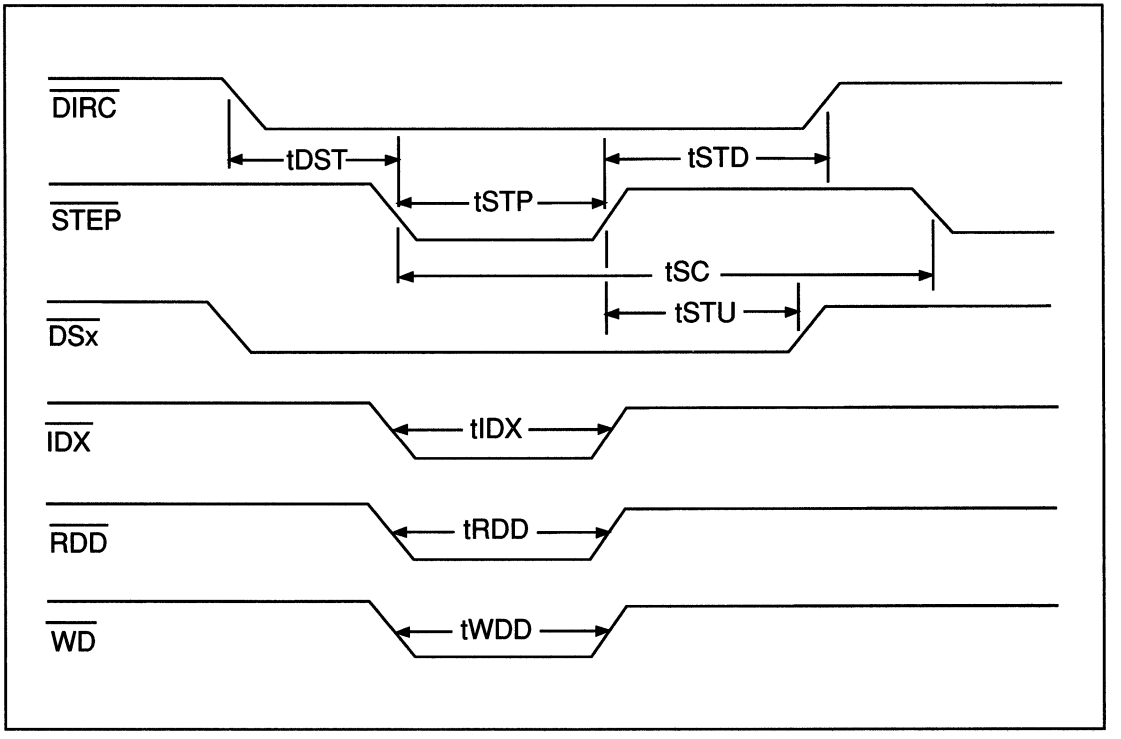


FIGURE 12. DISK DRIVE TIMING

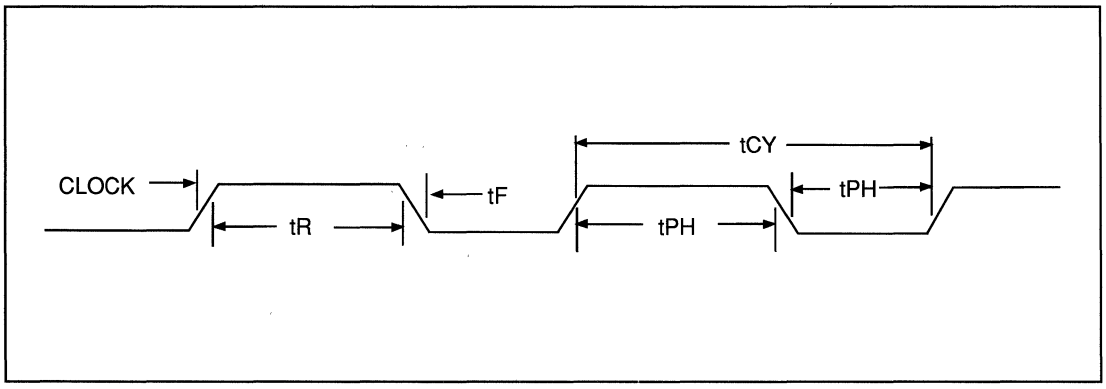


FIGURE 13. CLOCK TIMING

6.0 COMMAND SUMMARY

6.1 COMMAND PARAMETERS

The WD57C65 performs 15 different host supplied commands:

READ DATA
READ DELETED DATA
WRITE DATA
WRITE DELETED DATA
READ A TRACK
READ ID
FORMAT A TRACK
SCAN EQUAL
SCAN LOW OR EQUAL
SCAN HIGH OR EQUAL
RECALIBRATE
SENSE INTERRUPT STATUS
SPECIFY
SENSE DRIVE STATUS
SEEK

A multibyte transfer from the processor initiates each command. The results after execution of the command may also be a multibyte transfer back to the processor. The commands consist of three phases: the command phase, the execution phase, and the result phase.

Command phase - The Floppy Disk Controller (FDC) receives all information required to perform a particular operation from the processor.

Execution phase - The FDC performs the operation it was instructed to do.

Result phase - After completion of the operation, status and other housekeeping information are available to the processor.

Tables 27 through 41 show the required parameters and results for each command. Most commands require nine command bytes and return seven bytes during the result phase. The "W" to the left of each bytes indicates a command phase byte to be written. An "R" indicates a result byte. Table 42, page 35, lists and defines all of the symbols used in tables 27 through 41.

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution.
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 27. READ DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution.
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 28.READ DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution.
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 29. WRITE DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution.
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 30. WRITE DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US1	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system. FDD reads all data fields from index hole to EOT.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 31. READ A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
EXECUTION										The first correct ID information on the cylinder is stored in Data Register.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information read during Execution Phase from floppy disk.
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 32. READ ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	N	N	N	N	N	N	N	N	Bytes/Sector
	W	SC	SC	SC	SC	SC	SC	SC	SC	Sectors/Track
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	Gap 3
	W	D	D	D	D	D	D	D	D	Filler Byte
EXECUTION										Floppy Disk Controller (FDC) formats an entire track.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	In this case, the ID information
	R	R	R	R	R	R	R	R	R	has no meaning.
	R	N	N	N	N	N	N	N	N	

TABLE 33. FORMAT A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to
	W	H	H	H	H	H	H	H	H	command execution.
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	STP	STP	STP	STP	STP	STP	STP	STP	
EXECUTION										Data compared between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after com-
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	mand execution.
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after com-
	R	R	R	R	R	R	R	R	R	mand execution.
	R	N	N	N	N	N	N	N	N	

TABLE 34. SCAN EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	STP	STP	STP	STP	STP	STP	STP	STP	
EXECUTION										Data compared between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 35. SCAN LOW OR EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	STP	STP	STP	STP	STP	STP	STP	STP	
EXECUTION										Data compared between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution.
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 36. SCAN HIGH OR EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W W	0 X	0 X	0 X	0 X	0 X	1 0	1 US1	1 US0	Command Codes
EXECUTION										Head retracted to Track zero.

TABLE 37. RECALIBRATE

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	0	0	0	Command Codes
RESULTS	R R	ST0 PCN	ST0 PCN	ST0 PCN	ST0 PCN	ST0 PCN	ST0 PCN	ST0 PCN	ST0 PCN	Status information about the FDC at the end of seek operation

TABLE 38. SENSE INTERRUPT STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W W W	0 SRT HLT	0 SRT HLT	0 SRT HLT	0 SRT HLT	0 HUT HLT	0 HUT HLT	1 HUT HLT	1 HUT ND	Command Codes

TABLE 39. SPECIFY

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W W	0 X	0 X	0 X	0 X	0 X	0 HS	0 US1	0 US0	Command Codes
RESULTS	R	ST3	ST3	ST3	ST3	ST3	ST3	ST3	ST3	Status information about the FDC.

TABLE 40.SENSE DRIVE STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W W W	0 X NCN	0 X NCN	0 X NCN	0 X NCN	1 X NCN	1 HS NCN	1 US1 NCN	1 US0 NCN	Command Codes
EXECUTION										Head is positioned over proper cylinder on the diskette.

TABLE 41. SEEK

SYMBOL	NAME	DESCRIPTION
A0	ADDRESS LINE 0	A0 controls selection of Main Status Register (A0=0) or Data Register (A0=1).
C	CYLINDER NUMBER	C stands for the current/selected cylinder (track) numbers 0 through 255 of the medium.
D	DATA	D stands for the data pattern which is going to be written into a sector.
D7 - D0	DATA BUS	8-bit DATA BUS, where D7 stands for a most significant bit, and D0 stands for a least significant bit.
DTL	DATA LENGTH	When N is defined as 00, DTL stands for the DATA LENGTH which users are going to read out or write into the sector.
EOT	END OF TRACK	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL	GAP LENGTH	GPL stands for the length of Gap 3. During the FORMAT Command, it determines the size of Gap 3.
H	HEAD ADDRESS	H stands for head number 0 or 1 as specified in the ID field.
HLT	HEAD LOAD TIME	HLT stands for the HEAD LOAD TIME in FDD (2 to 254ms in 2ms increments).
HS	HEAD SELECT	HS stands for a selected head number 0 or 1 and controls the polarity of pin 25 (in 40 pin DIP) or pin 28 (in 44 pin PLCC).
HUT	HEAD UNLOAD TIME	HUT stands for the HEAD UNLOAD TIME after a Read or Write operation has occurred (16 to 240ms in 16ms increments).
MF	FM or MFM	If MF is low, FM mode is selected. If it is high, MFM mode is selected.
MT	MULTITRACK	If MT is high, a MULITRACK operation is performed. If MT=1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N	NUMBER	N stands for the NUMBER of data bytes written in a sector.
NCN	NEW CYLINDER NUMBER	NCN stands for a NEW CYLINDER NUMBER which is going to be reached as a result of the Seek operation. Desired position of head.
ND	NON-DMA MODE	ND stands for operation in the NON-DMA MODE.
PCN	PRESENT CYLINDER	PCN stands for the cylinder number at the completion of the SENSE INTERRUPT STATUS Command. Position of head at present time.
R	RECORD	R stands for the sector number which will be read or written.
R/W	READ/WRITE	R/W stands for either READ or WRITE signal.
SC	SECTOR	SC indicates the number of sectors per cylinder.

TABLE 42. COMMAND SYMBOL DESCRIPTIONS

SYMBOL	NAME	DESCRIPTION
SK	SKIP	SK stands for SKIP Deleted Data Address mark.
SRT	STEP RATE TIME	SRT stands for the Stepping Rate for the FDD (1 to 16ms in 1ms increments). Stepping Rate applies to all drives. In 2's complement format, F(Hex)=1ms, E(Hex)=2ms, etc.
ST0 ST1 ST2 ST3	STATUS 0 STATUS 1 STATUS 2 STATUS 3	ST0-3 stands for one of four registers which store the STATUS information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0=0). ST0-3 may be read only after a command has been executed and contains information relevant to that particular command.
STP	---	During a SCAN operation, if STP=1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP=2, then alternate sectors are read and compared.
US0,US1	UNIT SELECT	US stands for a selected drive; binary encoded, 1 of 4.

TABLE 42. COMMAND SYMBOL DESCRIPTIONS (CONTINUED)

6.2 COMMAND DESCRIPTIONS

6.2.1 READ DATA

A set of nine byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits for the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number (R) stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and placed on the data bus. This continuous read function is called a "Multi-sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time as the DACK/ for the last byte of data. Upon receipt of this signal, the FDC stops outputting data to the processor, but continues to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and terminate the Read Data command at the end of the sector. The amount of data handled by a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (number of bytes/sector). Table 43 lists the Transfer Capacity.

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note: this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length as a sector. If DTL is smaller than the actual data length of a sector, the data beyond DTL in the sector is not sent to the Data Bus. The FDC reads (internally) the complete sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read operation. When N is non-zero, then DTL has no meaning and sets to FF (hexadecimal.)

Upon completion of the Read Data command, and after Head Unload Time Interval (specified in the Specify command) has elapsed, the head unloads. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a "1" (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to "0" and "1", respectively.)

Multi-Track MT	MFM/FM MF	Bytes /Sect or N	Maximum Transfer Capacity (Bytes/Sector) Number of Sectors	Final Sector Read From Diskettes
0 0	0 1	00 01	(128)(26)=3,328 (256)(26)=6,656	26 at Side 0 or 26 at Side 1
1 1	0 1	00 01	(128)(52)=6,656 (256)(52)=13,312	26 at Side 1
0 0	0 1	01 02	(256)(15)=3,840 (512)(15)=7,680	15 at Side 0
1 1	0 1	01 02	(256)(30)=7,680 (512)(15)=15,360	15 at Side 1
0 0	0 1	02 03	(512)(8)=4,096 (1024)(8)=8,192	8 at Side 1 or 8 at Side 1
1 1	0 1	02 03	(512)(16)=8,192 (1024)(16)=16,384	8 at Side 1

TABLE 43. TRANSFER CAPACITY

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
0	0	Equal to EOT	C+1	NC	R=0	NC
0	1	Less than EOT	NC	NC	R+1	NC
0	1	Equal to EOT	C+1	NC	R=0	NC
1	0	Less than EOT	NC	NC	R+1	NC
1	0	Equal to EOT	NC	LSB	R=0	NC
1	1	Less than EOT	NC	NC	R+1	NC
1	1	Equal to EOT	C+1	LSB	R=0	NC

Notes: NC (No Change): The same value as the one at the beginning of command execution. LSB (Least Significant Bit): The least significant bit of H is complemented.

TABLE 44. C, H, R, AND N VALUES

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If it detects a read error (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to "1" (high). If a CRC error occurs in the Data Field, the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a "1" (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to "0" and "1", respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in status Register 2 to a "1" (high), and terminates the Read Data command, after reading all the data in the sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the processor must service the FDC every 27 microseconds in the FM mode, and every 13 microseconds in the MFM mode. If not, the FDC sets the OR (Overrun) flag in Status Register 1 to a "1" (high), and terminates the Read Data command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result phase is dependent upon the state of the MT bit and EOT byte. Table 44 shows the values for C, H, R, and N, when the processor terminates the command.

6.2.2 WRITE DATA

The FDC requires nine bytes of command for the Write Data mode. After the Write Data command issues, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C,H,R,N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the sector number stored in "R" is incremented by one, and the next data field is written. The FDC continues this Multi-Sector Write Operation until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC, the FDC continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detect a read error (CRC error) in one of the ID fields, it sets the DE (Data Error) flag of Status Register 1 to a "1" (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to "0" and "1", respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data command for details:

- Transfer Capacity
- EN (End of Cylinder) flag
- ND (No Data) flag
- Head Unload Time interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N≠0

In the Write Data mode, data transfers between the processor and FDC via the data bus, must occur every 27 microseconds in the FM mode and every 13 microseconds in the MFM mode. If the

time interval between data transfers is longer than this, then the FDC sets the OR (Overrun) flag in Status Register 1 to a "1" (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to "0" and "1", respectively.)

6.2.3 WRITE DELETED DATA

This command is the same as the Write Data command except a Deleted Data Address mark is written at the beginning of the data field instead of the normal Data Address mark.

6.2.4 READ DELETED DATA

This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field (and SK = 0 [low]), it will read all the data in the sector and set the CM flag in Status Register 2 to a "1" (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address mark and reads the next sector.

6.2.5 READ A TRACK

This command is similar to the Read Data command, except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hold, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR. It sets the ND flag of the Status REgister 1 to a "1" (high) if there is no comparison. Multi-Track or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID Address mark on the diskette after it senses the index hold for the second time, it sets the MA (missing Address mark) flag in Status Register 1 to a "1" (high) and terminates the command. (Status Register 0 has bits 7 and 6 set to "0" and "1", respectively.)

6.2.6 READ ID

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, then the MA (Missing Address mark) flag in Status Register 1 is set to a "1" (high). If no data is found, then the ND (No Data) flag is also set in Status Register 1 to a "1" (high). The command is then terminated with bits 7 and 6 in Status Register 0 set to "0" and "1", respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

6.2.7 FORMAT A TRACK

The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette: Gaps, Address marks, ID fields and data fields, all per the IBM System 34 (double density) or System 3740 (single density) format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (gap length), and D (data pattern) which the processor supplies during the command phase. The data field is filled with the byte of data stored in D. The processor supplies the ID field for each sector; that is, the processor makes four data requests per sector for C (cylinder number), H (head number), R (sector number) and N (number of bytes/sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the WD57C65 for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the Interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by "1" after each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

Table 45 shows the relationship between N, SC, and GPL for various sector sizes.

6.2.8 SCAN COMMANDS

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexadecimal byte of FF either from memory or from FDD, can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). If, after a whole sector of data is compared, and the conditions are not met, the sector number increments (R + STP $\xrightarrow{}_8$ R), and the scan operation continues. The scan operation

Format	Sector Size Bytes/sector	N	SC	GPL 1	GPL 2,3
8" Standard Floppy					
FM Mode	128	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5 1/4" Minifloppy					
FM Mode	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3 1/2" Sony Microfloppy					
FM Mode	128	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

Notes:
1. Suggested values of GPL in Read 0, Write commands to avoid splice point between data field and ID field of contiguous sections.
2. Suggested values of GPL in format command.
3. All values except sector size are hexadecimal.
4. In MFM mode FDC cannot perform a Read/Write/format operation with 126 bytes/sector. (N=00)

TABLE 45. N, SC, AND GPL RELATIONSHIP

continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a "1" (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a "1" (high) and terminates the Scan command. The receipt of a Terminal Count signal from the processor or DMA controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and then to terminate the command. Table 46 shows the status of bits SH and SN under various conditions of Scan.

Command	Status Register 2 Bit 2=SN	Bit 3=SH	Comments
Scan Equal	0	1	$D_{FFD}=D_{Processor}$
Scan Equal	1	0	$D_{FFD}\neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FFD}=D_{Processor}$
Scan Low or Equal	0	0	$D_{FFD}<D_{Processor}$
Scan Low or Equal	1	0	$D_{FFD}>D_{Processor}$
Scan Low or Equal	0	1	$D_{FFD}=D_{Processor}$
Scan High or Equal	0	0	$D_{FFD}>D_{Processor}$
Scan High or Equal	1	0	$D_{FFD}<D_{Processor}$

TABLE 46. STATUS OF BITS SH AND SN

If the FDC encounters a Deleted Data Address mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (Control Mark) flag of Status Register 2 to a "1" (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address mark and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control mark) flag of Status Register 2 to a "1" (high) in order to show that a deleted sector had been encountered.

During the Scan command, the processor or DMA controller supplies the data for comparison against the data read from the diskette. In order to avoid having the OR (Overrun) flag set in Status Register 1, it is necessary to have the data available in less than 27 microseconds (FM mode) or

34

13 microseconds (MFM mode). If an Overrun occurs, the FDC ends the command with bits 7 and 6 of Status Register 0 set to "0" and "1", respectively.

6.2.9 SEEK

The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent Present Cylinder Registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to a "1" (high), and step pulses are issued. (Step In)

PCN > NCN: Direction signal to FDD set to a "0" (low), and step pulses are issued. (Step Out)

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse issues, NCN is compared against PCN, and when NCN = PCN, the SE (Seek End) flag sets in Status Register 0 to a "1" (high), and the command terminates. At this point FDC interrupt goes high. Bits D0B-D3B in the Main Status Register set during the Seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the FDC is in the FDC Busy state; but during the Execution phase, it is in the non-busy state. While the FDC is in the non-busy state, another Seek command may be issued, and in this manner parallel Seek operations may be done on up to four drives at once. No other command can be issued for as long as the FDC is in the process of sending step pulses to any drive.

If the time to write three bytes of Seek command exceeds 150 microseconds, the timing between the first two step pulses may be shorter than set in the Specify command by as much as 1 millisecond.

6.2.10 RECALIBRATE

The function of this command is to retract the Read/Write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and step pulses are issued. When the Track 0 signal goes high, the SE (Seek End) flag in Status Register 0 is set to a "1" (high) and the command terminates. If the Track 0 signal is still low after 77 step pulses have issued, the FDC sets the SE (Seek End) and EC (Equipment Check) flags of Status Register 0 to both "1s" (highs), and terminates the command after bits 7 and 6 of Status Register 0 are set to "0" and "1", respectively.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also applies to the Recalibrate command.

6.2.11 SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following conditions:

1. Upon entering the Result phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Cylinder command
   g. Write Deleted Data command
   h. Scan commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate command
4. During Execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an Execution phase in non-DMA mode, DB5 in the Main Status Register is high. Upon entering the Result phase, this bit clears. Conditions 1 and 4 do not require Sense Interrupt Status commands. The interrupt clears by Reading/Writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command, when issued, resets the Interrupt signal and via bits 5,6, and 7 of Status Register 0, identifies the cause of the interrupt.

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no Result phase. When the disk drive has reached the desired head position, the WD57C65 will set the interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual

Seek End Bit 5	Interrupt Code Bit 6	Bit 7	Cause
0	1	1	Ready Line changed state, either polaritv
1	0	0	Normal Termination of Seek or Recalibrate command

TABLE 47. INTERRUPT CAUSE

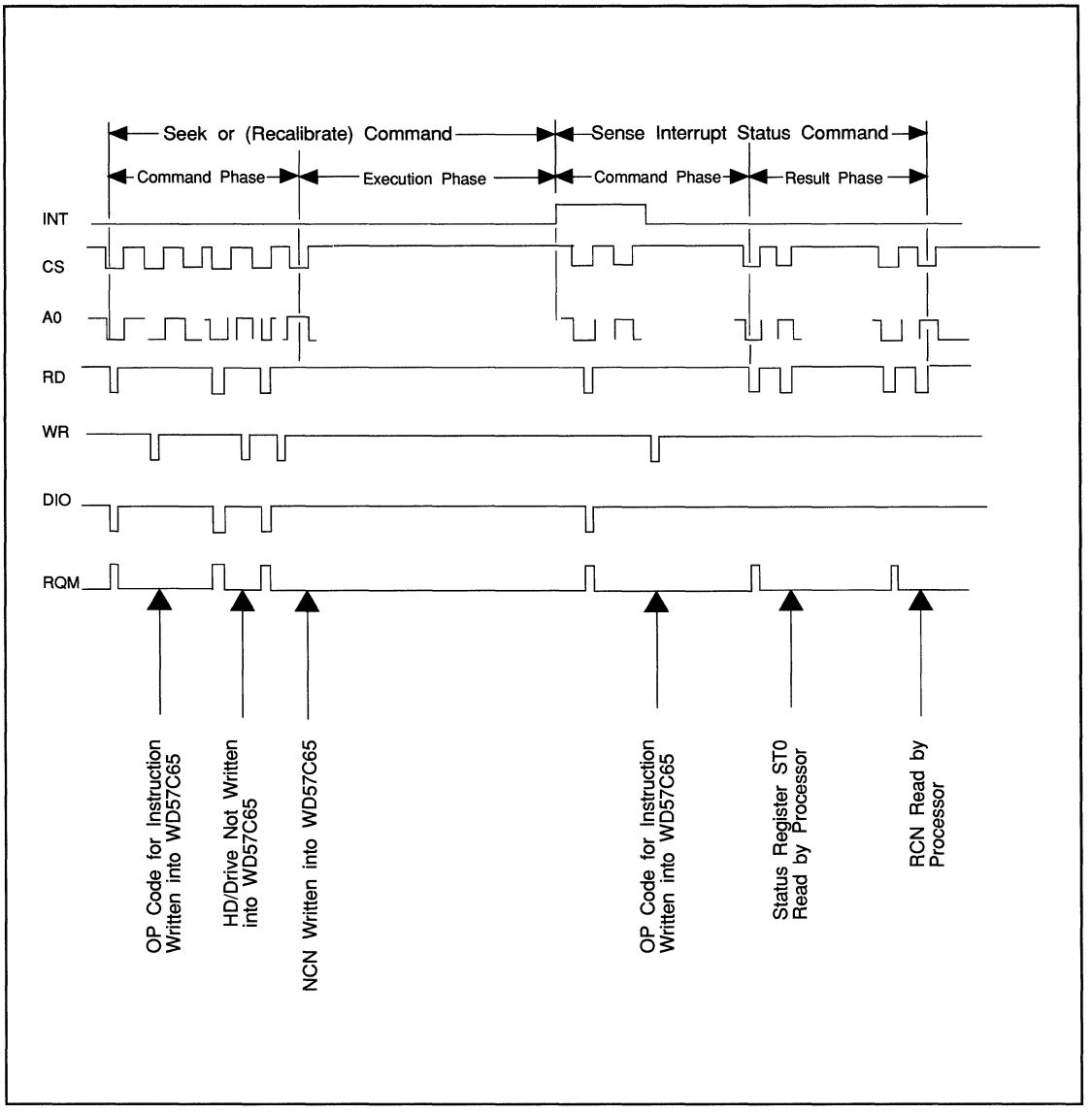


FIGURE 14. SEEK, RECALIBRATE, AND SENSE INTERRUPT

cause of the interrupt, which could be Seek End or a change in ready status from one of the drives. See Figure 14.

The Specify command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240 milliseconds in increments of 16 milliseconds (01 = 16 milliseconds, 02 = 32 milliseconds . . . OF_{16} = 240 milliseconds). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 milliseconds in increments of 1 millisecond (F = 1 millisecond, E = 2 milliseconds, D = 3 milliseconds, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the Read/Write operation

starts. This timer is programmable from 2 to 254 milliseconds in increments of 2 milliseconds (011 = 2 milliseconds, 02 = 4 milliseconds, 03 = 6milliseconds ...7F = 254 milliseconds).

The time intervals mentioned above are a direct function of the clock (CLK on pin 20). Times indicated above are for a 16 MHz clock; if the clock was reduced to 8 MHz, then all time intervals are increased by a factor of 2.

The choice of DMA or non-DMA operation is made by the ND (Non-DMA) bit. When this bit is high (ND = 1), the Non-DMA mode is selected; and when ND = 0, the DMA mode is selected.

6.2.12 SENSE DRIVE STATUS

The processor uses this command whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

6.2.13 INVALID

If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to "1" and "0", respectively. No interrupt is generated during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status Register are both high (1), indicating to the processor that the WD57C65 is in the result phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0, it will find 80 hex, indicating an Invalid command was received.

A Sense Interrupt Status command must follow after a Seek or Recalibrate interrupt; otherwise the FDC will not consider the next command.

In some applications, the user may wish to use this command as a No-Op command to place the FDC in a standby or No Operation state.

STORAGE

WD60C40

Peripheral Cache

Manager Device

35

WESTERN DIGITAL

TABLE OF CONTENTS

TABLE OF CONTENTS, Continued

TABLE OF CONTENTS, Continued

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

1.1 ARCHITECTURAL DESCRIPTION

The WD60C40 peripheral cache manager (PCM) controls a large amount (up to 1 megabyte) of dynamic RAM, and the buffering required to allow the seemingly simultaneous access of this buffer by up to 3 requestors. The three requestors are assumed to be two block oriented devices, and a microprocessor.

The two devices interface to the dynamic RAM, are designed to support block oriented peripheral formatter chips, such as the ADS10C00 Hard Disk Formatter, or block oriented bus interface chips, such as the WD33C93A SCSI Bus Interface Chip. The implication of block oriented devices, is that the devices will not have the capability of randomly accessing data within the memory array. This restriction allows for the removal of the addressing pins that are normally associated with an interface. The 20 bit address counters that are required to select a byte within the array, are now incorporated into the WD60C40.

The buffer control logic interfaces with an external dynamic RAM array and arbitrates the access into this array from the three external sources. The internal arbitrator in the PCM also includes the refresh logic that is internal to the PCM into its arbitration. Each device port has built into it a byte-wide FIFO that will act as a buffer while the port is waiting for its time slot in the arbitration mechanism.

The dynamic RAM memories do not have the random access bandwidth to sustain multiple high speed devices. The dynamic RAM memories do incorporate a feature known as "page mode or static column" that increases their bandwidth to the point that they will sustain multiple high speed devices. The dynamic RAMs have a multiplexed address bus with the address into the array being divided into two parts, a row address and a column address.

The dynamic RAMs allow a feature that if the next access into the array is in the same row (same page) then only the column address must be up dated from the addressing logic. This scheme carries the penalty that a FIFO must be available to hold the data to/from the port to ensure that when a port gains access to the RAM, it can transfer data in a continuous block. The PCM incorporates 15 bytes of FIFO into each of the peripheral ports to support the page mode memory and CAS control static column architecture. This scheme has the advantage that the memory bandwidth is increased by a factor of about 75% over the random access bandwidth, allowing a large buffer memory to be mechanized by inexpensive dynamic RAMs, but having the performance characteristics of a static RAM buffer.

The external dynamic RAM buffer may be 8 bits or 9 bits wide. The depth of the array and the organization of the devices that make up the array are as follows:

SIZE	ORGANIZATION		
16 KB	2	216Kb x 4	(+ 64Kb x 1 parity)
64 KB	2	64Kb x 4	(+ 64Kb x 1 parity)
64 KB	8	64Kb x 1	(+ 64Kb x 1 parity)
256 KB	2	256Kb x 4	(+ 256Kb x 1 parity)
256 KB	8	256Kb x 1	(+ 256Kb x 1 parity)
1 MB	2	1Mb x 4	(+ 1Mb x 1 parity)
1 MB	8	1Mb x 1	(+ 1Mb x 1 parity)

In the following description, refer to Figure 1, the block diagram of the WD60C40, and to the example board environment in Figure 2. A typical situation to use as an example of the actions within the part is that of a disk controller. In this example, port 'B' of the device is connected to a bus interface controller (ex. WD33C93A), and port 'A' of the device is connected to a disk interface controller (ex. ADS10C00).

The example begins with the assumption that all devices are currently active, and the refresh time has arrived, and the microprocessor is requesting a data item. The PCM is currently servicing the FIFO that is attached to the device port 'A'. The microprocessor is currently at a wait bus cycle because of the RDY signal from the PCM being inactive. The PCM will move data to/from the memory and the port 'A' FIFO until the FIFO is full/empty, or the transfer counter of port 'A' exhausts. If during this sequence, the PCM detects that a dynamic RAM page boundary is being crossed, the PCM will update the row address, and continue the page mode transfer. While this action is occuring, any byte transfers to/from the other device port are stored in that device port's FIFO. When port 'A' has finished its data transfers, the PCM will first service the host data re-

quest, then the refresh request(s), both of which have priority over block transfers. The PCM will then initiate transfer between the port 'B' FIFO, and the dynamic RAMs.

The PCMs priority system when arbitrating is:

- microprocessor requests
- refresh requests
- the higher priority peripheral channel
- the lower priority peripheral channel

The control of the peripheral channel priority is under firmware control if the channels are peers in their capability of sustaining a pause in their transfers. If a channel is programmed as 'non-pausible', and the other channel is 'pausible' then this channel is given priority in the arbitration mechanism regardless of the other firmware priority controls. If the channels are peers, such as both being 'pausible' or both being 'non-pausible', then the priority of the channels is controlled by firmware selecting one of the channels as higher priority through option register 2. See also the descriptions of the AHI bit in option register 2, and PAUS bits in the channel control register.

Note that arbitration does not occur until the requestor currently being serviced has completed its entire burst. This means that page mode bursts between the channels and memory are not interrupted by requests from higher priority requestors. There are two exceptions to this general rule. The first exception is a non-pausible device that is selected by firmware as having higher arbiter priority. This channel is then allowed an "urgent request", when its FIFO is almost exhausted. This "urgent request" will send a false end of transfer signal through the other port and cause arbitration to occur, and this channel will then win arbitration if the single cycle devices are not requesting. This is done to minimize the occurence of over/under-run errors in high priority non-pausible devices. The second exception that causes a burst to be halted is for a refresh burst. The refresh request occurs at regular intervals (see option register section for specific details), but if it is not serviced because of a channel burst, then the request is queued into a counter. When 4 refresh cycles have been queued (about 60 µsec.), then the "urgent request" mechanism will force arbitration, and a burst of 4 refresh cycles will be performed. This is done to maintain memory data integrity.

To finish the architectural description of the device, the last items are the programmable features of the internal logic that allow the controller firmware to control and "tune" the actions of the PCM. The first item the PCM needs to be aware of is if the devices are capable of being throttled. Most devices that attach to peripherals have minimum data buffering, so the port logic must be programmed to look for overrun/underrun situations when the FIFO is full/empty. Some devices that attach to busses or other peripherals that have variable data rates, are capable of being 'stalled' when the FIFO is full/empty, and the port logic is capable of holding the port until the FIFO is ready.

The PCM also implements a "pipelined" pointer mechanism that allows the programmer to set the pointer (buffer address) of the current device transfer, and if required, set the pointer of the next transfer, while the current transfer is taking place. This address is held in the address pointer holding register to be automatically transferred to the address pointer at the end of the current transfer. If the next transfer's buffer is contiguous with the current transfer's buffer, then the address pointer "pipeline" need not be loaded, and when the next transfer begins the address pointer will continue from its current position. This address is therefore only necessary if the next transfer is at a memory address that is not contiguous with the end of the current transfer. The transfer counter is always loaded from the transfer counter holding register at the start of a new block transfer, but the transfer counter holding register need only be reloaded if the block size of a transfer needs to be changed. When the current transfer finishes, the firmware can be interrupted, while the hardware continues directly into the next transfer. With this mechanism, the firmware now has a block time to determine what is to be done when this transfer finishes, rather than doing this during the inter-block gap times. If pipelined (ie. continuous) transfers are required then microprocessor action is required whenever the pipeline becomes empty. If the next transfer is the same size as the current, and contiguous in address, then the firmware need only issue a new channel start command. Alternatively the firmware can load new values into the "pipeline" registers before issuing the start, and dynamically control the transfer size and buffer location. The firmware can poll the status or wait for an interrupt (if enabled) to indicate that the holding registers are available.

The device channels are mechanized with 8 or 9 data lines, and 5 control/handshake lines. Four control signals are programmable to allow interfaceing to multiple types of device controller chips. Features such as the master/slave relationships between the PCM and the external peripheral controller, the polarity and timing of the signals that do the handshake, input/output control direction, and the mode that the control lines emulate are all programmable.

1.2 FEATURES

- 5 Volt Only Operational Power.
- 1.25 micron CMOS for low power consumption.
- 84 pin JEDEC PLCC or 84 pin JEDEC PQFP packages.
- Supports dynamic memory configurations from 16 KB to 1 MB.
- Supports static memory configurations.
- Supports parity on the memory array.
- Supports parity on peripheral ports.
- Aggregate memory bandwidth of greater than 9.0 Mbytes/sec, using industry standard 100 ns. dynamic RAMs.
- Aggregate memory bandwidth of greater than 12 Mbytes/sec, using 80 ns. dynamic RAMs
- Supports 2 peripheral channels.
- High Speed Channels support peripheral data rates of:
  - 6.25 Mbytes/sec as bus master with 25 MHz input clock, the maximum data rate is input clock divided by 4.
  - 10.0 Mbytes/sec as bus slave, with 25 MHZ input clock, the maximum data rate is input clock divided by 2.5.
- Programmable configuration of device channel interface.
- Internal FIFOs on peripheral channels.
- Supports independant transfers on both peripheral ports and microprocessor simultaneously.
- Large memory allows peripheral controllers to be implemented that "decouple" the host and disk transfer rates, maintaining 1:1 disk interleave regardless of host transfer rate.
- Provides "minimum chip count" solution for mechanizing a peripheral cache controller.
- Supports high speed microprocessor bus cycles, such as Intel* 80186 or 80188 type processors running at 12.5 MHz with no wait states required when accessing the PCM task file registers.

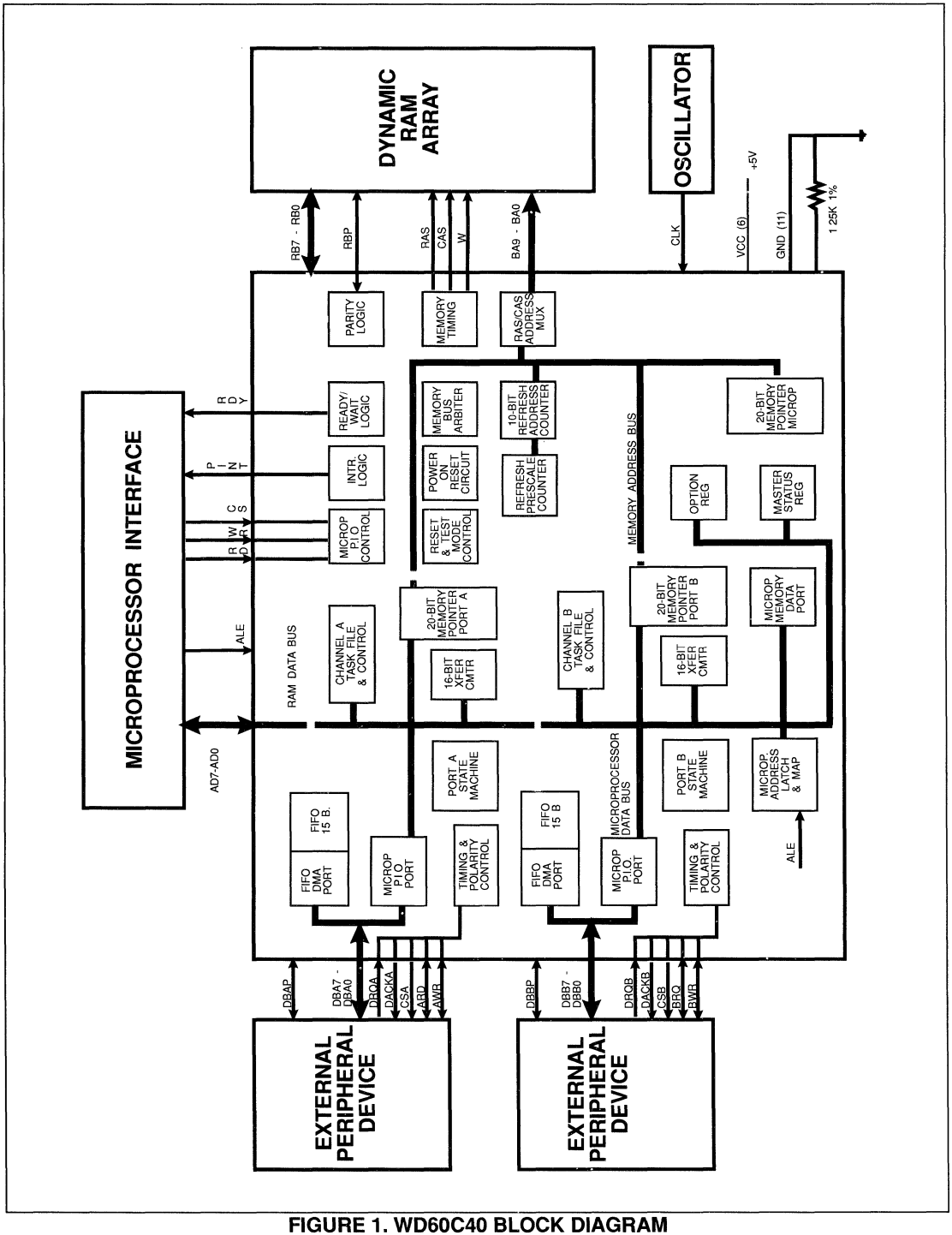


FIGURE 1. WD60C40 BLOCK DIAGRAM

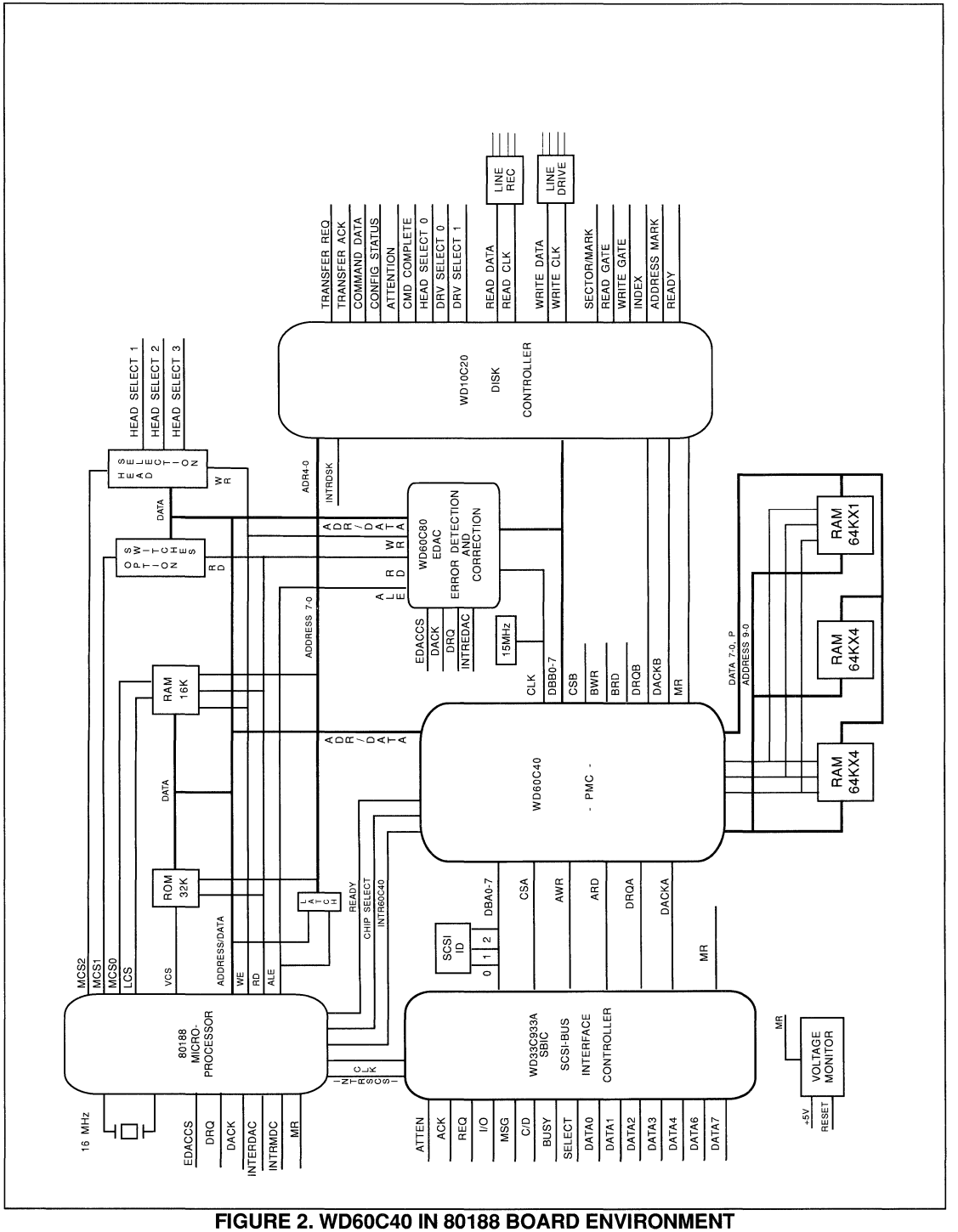


FIGURE 2. WD60C40 IN 80188 BOARD ENVIRONMENT

2.0 PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O
1,22,30,43, 56,64	V_{CC}	+5 Volt power supply connection	I
2,11,21,23, 29,42,44,57, 63,65,75	GND	Ground power supply connection	I
3 thru 10	AD0 thru AD7	µP ADDRESS/DATA BUS	I/O
12 thru 19	DBB0 thru DBB7	DEVICE BUS B DATA	I/O
20	DBBP	DEVICE BUS B PARITY BIT	I/O
24	$\overline{CSB}$	CHANNEL SELECT B	O
25	DRQB	DEVICE PORT B CYCLE REQUEST	I/O[1]
26	DACKB	DEVICE PORT B CYCLE ACKNOWLEDGE	I/O[2]
27	$\overline{BRD}$	DEVICE PORT B READ STROBE	I/O
28	$\overline{BWR}$	DEVICE PORT B WRITE STROBE	I/O
31 thru 38	RB7 thru RB0	DYNAMIC RAM DATA BUS	I/O
39	RBP	DYNAMIC RAM PARITY BIT	I/O
40	W/$\overline{WE}$	DYNAMIC RAM WRITE/STATIC RAM $\overline{WE}$	O
41	$\overline{CAS}$/$\overline{OE}$	DYNAMIC RAM $\overline{CAS}$/STATUS RAM $\overline{OE}$	O
45	$\overline{RAS}$	RAM ROW ADDRESS STROBE	O
46 thru 55	BA0[3] thru BA9	RAM ADDRESS BUS[3]	O
58	$\overline{AWR}$	$\overline{DEVICE\ PORT\ A\ WRITE\ STROBE}$	I/O
59	$\overline{ARD}$	$\overline{DEVICE\ PORT\ A\ READ\ STROBE}$	I/O
60	DACKA	DEVICE PORT A CYCLE ACKNOWLEGE	I/O[2]
61	DRQA	$\overline{DEVICE\ PORT\ A\ CYCLE\ REQUEST}$	I/O[1]
62	$\overline{CSA}$	$\overline{CHANNEL\ SELECT\ A}$	O
66	DBAP	DEVICE BUS A PARITY BIT	I/O
67 thru 74	DBA7 thru DBA0	DEVICE BUS A DATA BUS	I/O
76	CLK	CLOCK	I
77	$\overline{RST}$	$\overline{RESET}$	I
78	$\overline{CS}$	$\overline{\mu P\ BUS\ CHIP\ SELECT}$	I
79	$\overline{WR}$	$\overline{\mu P\ BUS\ WRITE\ CYCLE\ STROBE}$	I
80	$\overline{RD}$	$\overline{\mu P\ BUS\ READ\ CYCLE\ STROBE}$	I
81	ALE	µP ADDRESS STROBE	I
82	$\overline{PINT}$	$\overline{\mu P\ INTERRUPT\ REQUEST}$	O[4]
83	RDY	µP WAIT CONTROL	O[4]
84	RBIAS[5]	RESISTOR BIAS[5]	I

NOTES:

1 I = WD60C40 bus master mode. O = WD60C40 bus slave mode

2 I = WD60C40 bus slave mode. O = WD60C40 bus master mode.

3 BA0 is the LSB.

4 Open drain output

5 Resistor bias for output drive circuitry 1.24KΩ ± 1% connected from this pin to ground.

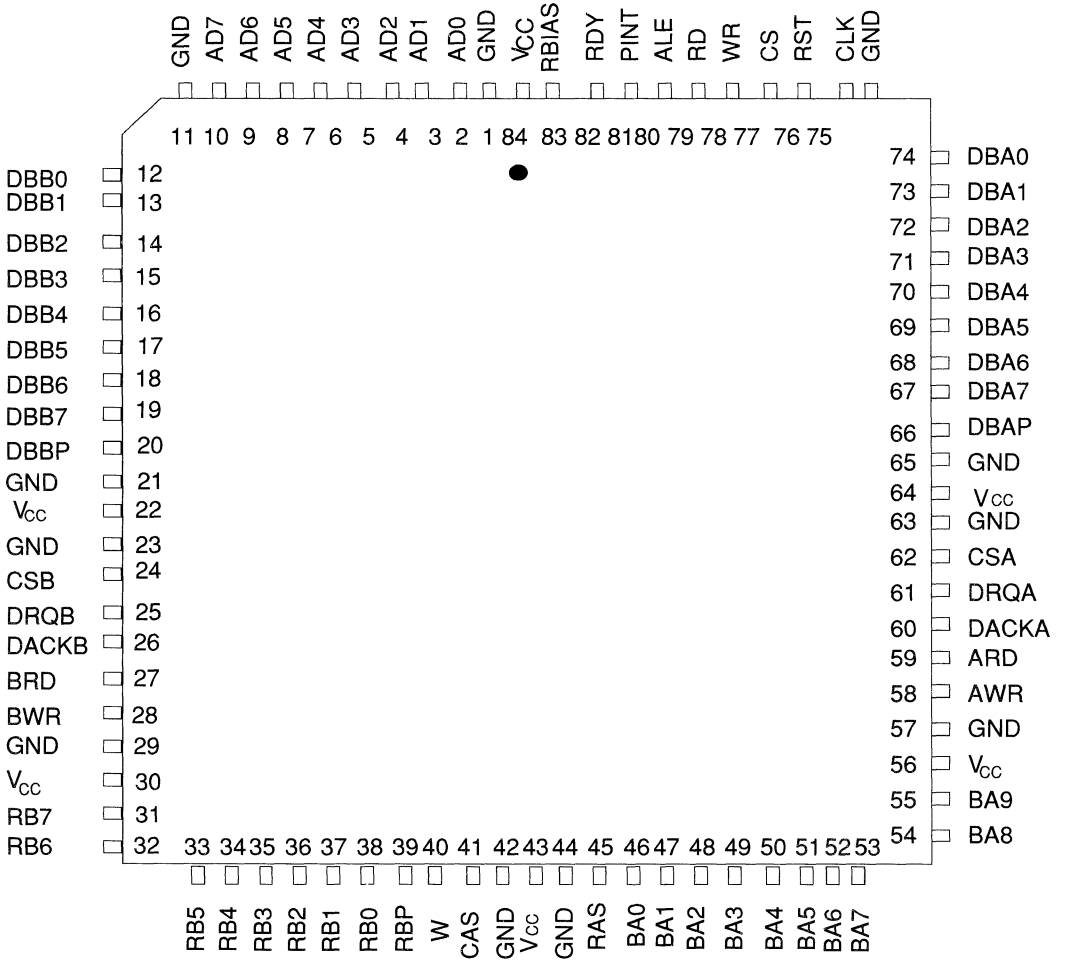


FIGURE 3. PIN DESIGNATION

35

3.0 NON-CHANNEL REGISTERS

The PCM was intended for use with the Intel 80186 processor and as such has been designed to interface easily with the 16 bit data bus of that processor. This is not to say that it cannot easily attach to other 8 or 16 bit microprocessors like Intel 8085, 8051, or 8096. The main requirement is that it be supplied with a multiplexed address/data bus with A7 to A0 multiplexed with D7 to D0 in that order.

As the PCM has only an eight bit data bus and it was decided not to handle the BHE signal, there are certain characteristics of the PCM that need explaining. First, all internal registers appear on even and the following odd byte address. This is because address signal A0 is not used inside of the PCM. The order of the registers was also arranged so that they appear in the order that they would normally be programmed. This allows the PCM to be attached to the 80186 and string move operations used to allow the fastest possible handling of loading the PCM.

Finally, the registers associated with the operation of the PCM itself do not decode the signal A7 so that they appear in both halves of the register map, facilitating an easier modulization of the driving firmware. Only the even addresses of the registers will be shown. Refer to page 10-35 for a summary of all the non-channel registers.

3.1 OPTION REGISTER

Address = 60H or E0H
Read/write register

7	6	5	4	3	2	1	0
MPAR	CAW1	CAW0	SRAM	RRC3	RRC2	RRC1	RRC0

The option register is a read/write only register to the firmware. The bits represent settings of options that must be selected to match the board design. There is the facility to read option switches and allow the firmware to assertain the hardware configuration in user 'adjustable' implementations. This register should be the first written after a reset sequence, and should not be written to thereafter unless another reset sequence has occurred.

3.1.1 RRC3 Thru RRC0 Refresh Rate Count Field

The refresh rate count field indicates to the PCM the prescale count to use for determing the refresh rate of the dynamic RAMs. The value of the refresh rate count field is effectively multiplied by 32, then subtracted from 512 to determine the number of clocks that will occur between refresh cycles. The value of this field is dependent upon the frequency of the PCMs clock. The following table shows the relationship of clock frequency, and refresh rate count field values, to produce 15.6 microsecond refresh cycles (for standard 128 cycle 2 ms. dynamic RAMs).

Field Value	Cycle Count	Freq. Range[1] Low	Freq. Range[1] High	Refresh Intrvl[2] Low	Refresh Intrvl[2] High
12	128	8.2	10.2	15.6	12.5
11	160	10.4	12.2	15.4	13.1
10	192	12.4	14.2	15.5	13.5
9	224	14.4	16.4	15.6	13.7
8	256	16.6	18.4	15.4	13.9
7	288	18.6	20.4	15.5	14.1
6	320	20.6	22.4	15.5	14.3
5	352	22.6	24.4	15.6	14.4

[1] Frequency ranges are in MHz.
[2] Refresh intervals are in µs.
NOTE:
The other field values are valid but are unlikely to be useful to the customer.

3.1.2 SRAM Static Ram Mode (bit 4)

The Static Ram Mode bit informs the PCM that the memory array is composed of static RAMs. When the bit is set, the PCM is in static RAM mode. This changes the signals that the PCM uses to access the memory array. Because of the multiplexed address bus of dynamic RAMs, it will be necessary for an external latch to be added to demultiplex the address lines. In addition, external address decoding will be necessary to expand the RAM to the full addressable capability. To assist in this, two of the RAM control signals change when the static RAM bit is set. First, the RAS signal is

used to control the external latch that is to demultiplex the address, when a valid row address is available on BA8 to BA0. RAS is intended to drive the clock input of a 74F373 type octal D-type latch, there is a direct analogy to the operation of dynamic RAMs at this point, with the exception that the row address latch is external to the memory devices. Secondly, static RAMs also have different read and write characteristics to dynamic RAMs. In dynamic mode, the W signal, signals the RAMs that a write cycle is about to occur, with the actual write action being generated by the falling edge of the CAS signal. This is known as early write mode. A read would occur if the CAS signal went active (low) with the W signal inactive (high). In static mode, the W and CAS signals change to support the separate WE and OE signals of static RAMs. In static mode, the CAS becomes the OE signal, still being active low but it will only occur on RAM read cycles, having the same shape and timing as for dynamic RAM cycles. The W signal becomes the WE signal, still being active low and only occuring in write cycles, but of a shape and timing similar to the CAS/OE signal. Finally, the arbitration logic no longer receives refresh requests as the static RAMs require no refresh, of course. At this stage it should be noted that the static RAM configuration is still liable to the row change overhead, when a row boundary is crossed during a burst of data cycles between the peripheral port FIFO and the memory.

The PCM is initialized to a special state at power up to ensure that there is no activity on the RAM control pins. This feature is used in the "power start" of the dynamic RAMs, which need to be left for a minimum time after power up. Please refer to the "Reset Sequences" section of this document for a description.

3.1.3 CAW1, CAW0 Column Address Width Field (bits 6,5)

The column address width field informs the PCM the type of RAM array that it is dealing with. The PCM uses the field to control the address multiplexer to the RAMs, and to determine the page mode boundaries of the RAMs. When a new page is detected, then the PCM executes a new RAS cycle, RAS goes inactive to precharge the RAS signal and then RAS goes active to latch the new row address and establish access in the new RAM page.

This field has no affect if the SRAM bit (bit 4) is set. When the SRAM mode is in effect, the PCM is forced to the ten bit column address mode.

00 = Ten bit column address (1meg DRAM). Bits 19 - 10 will be output on BA9 - BA0 during RAS time. Bits 9 - 0 will be output on BA9 - BA0 during CAS time.

01 = Nine bit column address (256K DRAM). Bits 18 - 9 will be output on BA9 - BA0 during RAS time. Bits 8 - 0 will be output on BA8 - BA0 during CAS time.

10 = Eight bit column address (64K DRAM). Bits 17 - 8 will be output on BA9 - BA0 during RAS time. Bits 7 - 0 will be output on BA7 - BA0 during CAS time.

11 = Six bit column address (16K DRAM). Bits 15 - 6 will be output on BA9 - BA0 during RAS time. Bits 5 - 0 will be output on BA5 - BA0 during CAS time.

3.1.4 MPAR = Memory Parity Enable (bit 7)

The parity enable bit informs the PCM that the memory array has a parity bit attached. When the bit is set, the PCM will generate odd parity (the sum of all one bits including the parity bit will be an odd number) on memory writes, and check parity on memory reads. If there is even parity on a memory read, the PCM will cause a parity error interrupt in the appropriate status register. When the bit is reset, the PCM will not generate parity on a write, or check parity on a read. The microprocessor firmware can use this bit to test the parity logic of the PCM, when there is parity memory. When the parity enable bit is reset, the RBP pin of the PCM will be at a logic one level during a write cycle.

3.2 OPTION REGISTER 2

Address = 62H or E2H
Read/write register
The option register 2 is initialized to zero by the PCM reset sequence

7	6	5	4	3	2	1	0
0	0	NOWAIT	WAITE	AHI	INTE	BINTE	AINTE

3.2.1 AINTE A Channel Interrupt Enable

The A channel interrupt enable bit allows interrupts from the "A" peripheral channel to exit the PCM by way of the PINT pin. This allows the programmer the capability to selectively disable interrupts from this channel while still allowing PCM interrupts from the other PCM resources. This bit only affects the transmission of the channels interrupt to the PINT pin, and does not affect the operation of any of the channels interrupt enables, or interrupt status flags.

3.2.2 BINTE B Channel Interrupt Enable

This bit performs the same function as AINTE, but for the "B" channel.

'A' CHANNEL	'B' CHANNEL	AHI	PRIORITY
Non-pausible	Pausible	X	A Channel
Pausible	Non-pausible	X	B Channel
Non-pausible	Non-pausible	1	A Channel
Non-pausible	Non-pausible	0	B Channel
Pausible	Pausible	1	A Channel
Pausible	Pausible	0	B Channel

3.2.3 WAITE Wait Enable

This bit is the master enable for any PCM wait condition to exit the PCM by the RDY pin. This allows the programmer the capability to selectively disable the RDY pin from the PCM. This bit only affects the transmission of the wait to the RDY pin, and does not affect the operation of any of the PCM wait sequences, or status.

3.2.4 NOWAT Non-waitable Microprocessor Interface (bit 5)

The "non-waitable" bit is used to distinguish to the PCM that the microprocessor or board design does not support the RDY function to extend bus cycles. This bit controls how the PCM will perform accesses to the data buffer and programmed I/O to the peripheral ports. This bit is reset by the PCM reset sequence.

When this bit is a zero, the PCM is to be used in a board with multiple devices sharing the microprocessor ready signal. The internal "ready" status of the PCM is gated with the CS signal, so only when the PCM is selected does it drive RDY. When the microprocessor accesses the data buffer or the peripherals for programmed I/O, then the PCM will assert RDY low to halt the bus cycle until it can perform the access. The PCM uses the leading edge of the data strobe to trigger the access, and if the firmware is writing data, then there is a specified time from the leading edge of the strobe that write data must become available within. When the access is complete, the PCM will deassert the RDY signal and allow the bus cycle to finish.

When this bit is a one, the PCM is used in a configuration with a microprocessor that does not support wait states, and the RDY signal is normally used as a status signal to a microprocessor's PIO input pin and polled by the firmware, or the internal status of the RDY pin is polled through the PCM task file register. In this configuration, the PCM will not gate the CS signal with the internal RDY status, so the RDY status will be available continuously. The PCM uses the trailing edge of the strobe to trigger the access, and as such there is no timing requirement on the write data from leading edge of strobe.

3.3 MASTER STATUS REGISTER

Address = 64H or E4H
Read/write register

7	6	5	4	3	2	1	0
DNR	0	0	PRNR	BANR	PPE	BINTR	AINTR

3.3.1 AINTR Channel A Interrupt Request Read only bit

3.3.2 BINTR Channel B Interrupt Request Read only bit

Setting AINTR (BINTR) indicates that the channel detected a situation requiring microprocessor action. The normal use of the interrupt is that the channel has completed an operation. The interrupt bit does not indicate if the operation was completed successfully, or if it terminated because of an error. The channel interrupt bit for each channel resets when the microprocessor clears all the interrupting states in the particular channel status register. This bit represents the 'or' function of all the interrupt conditions in the channel.

3.3.3 PPE Processor Parity Error

The processor parity error bit is set when a buffer read operation from the microprocessor interface resulted in a parity error. The bit is reset by the writing a one to the PPE bit. Writing a zero to PPE does not affect this bit.

3.3.4 BANR Buffer Access Not Ready Read only bit

The PCM "buffer access not ready" status bit is used to signal the microprocessor that the PCM is currently performing an access of the buffer and the registers that are associated with the buffer are not available. When the access is complete, this bit will be reset. See also the "DNR" bit in the master status register.

3.3.5 PRNR Power Reset Not Ready (bit 4) Read only bit

The PCM "power reset not ready" status bit is used to signal the microprocessor that the PCM is currently performing a power on reset sequence, or a programmed reset sequence, and all registers in the PCM except this register are not available. When the reset sequence is complete, this bit will be reset. See also the "DNR" bit in the master status register.

3.3.6 DNR Device Not Ready (bit 7) Read only bit

- The PCM "device not ready" status bit is used to signal the microprocessor that the PCM is currently performing a task that does not allow access to some resource in the PCM. The bit is essentially a logical 'or' of four conditions in the device that require multiple clock times to resolve themselves. The conditions are:

- the buffer manager reset sequence
- the microprocessor access of the buffer memory
- the microprocessor access of either of the peripheral ports for programmed I/O.

When the power is applied to the PCM, or firmware issues a soft reset, the bit will set indicating that all internal registers except this register are inaccessable. This bit will then reset when the PCM has completed its reset sequence. The "PRNR" bit in the master status register will also reflect this condition.

When the microprocessor accesses either of the peripheral ports for programmed I/O, or the microprocessor accesses the data buffer, the "device not ready" will reflect the status of the RDY pin of the PCM. This feature allows the firmware to 'poll' the PCM during these accesses when the board design or the microprocessor does not support the RDY function in hardware. The three accesses that cause this bit go to true are all independent, and can be occuring simultaneously. Because of the 'or' mechanism the bit will be false only when all accesses have completed.

When the microprocessor interface does support the RDY function, then there is no need to check this bit after the PCM has completed its reset sequence. When this bit is set because of RDY, the microprocessor is still in a wait state while the specific access is performed, and when the microprocessor is released from the wait state, then this bit is known to be reset.

3.4 BUFFER DATA LATCH

Address = 68H or E8H
Read/write register

7	6	5	4	3	2	1	0
BDL7	BDL6	BDL5	BDL4	BDL3	BDL2	BDL1	BDL0

The buffer data latch register holds the data last transferred between the microprocessor and buffer. The register is in the task file address space, so access of the register does not cause RDY to go false (no wait states). Access of the buffer data latch not cause the triggering of a buffer access.

The register is used when the board or microprocessor does not support the RDY function in hardware. Refer to the buffer access register description for specific details of the interaction of this register and the Buffer Access Register. The register is also useful for diagnostic purposes to test the PCM internal data path between the microprocessor and the internal task file.

3.5 MICROPROCESSOR ADDRESS POINTER

Address = 6EH or EEH (MP19 - MP16)
6CH or ECH (MP15 - MP08)
6AH or EAH 9MP07 - MP00)
Read/write register

7	6	5	4	3	2	1	0
0	0	0	0	MP19	MP18	MP17	MP16
MP15	MP14	MP13	MPM12	MP11	MP10	MP09	MP08
MP07	MP06	MP05	MP04	MP03	MP02	MP01	MP00

3.5.1 MP19 thru MP00 Microprocessor Address Pointer

The Microprocessor Address Pointer is a 20 bit register/counter that supplies the address lines to the buffer memory when the microprocessor is requesting a buffer data access. These registers may be read or written when the "BANR" bit in the master status register is reset, to show or set the current RAM window. If the microprocessor accesses the buffer through the Autoincrement Access Register, then this pointer will increment after the access has been performed.

3.6 TEST ADDRESS AND STATUS REGISTER

Address = 78H or F8H
Read/write register

7	6	5	4	3	2	1	0
TAS7	TAS6	TAS5	TAS4	TAS3	TAS2	TAS1	TAS0

The Test Address and Status register is a window into the internal logic of the PCM to allow greater visibility of the internal functioning of the device, and therefor greater test comprehensiveness.

The mechanization is that there is an address register in the PCM that can be loaded when a microprocessor write to this register occurs. This allows the selection of several internal registers and counters, and state machine registers, and the subsequent display of their content by reading this location.

This location also interacts with the Reset and Test register to invoke the test functions. Specifically there is an interlock so that test mode is more difficult to invoke, and less prone to be enabled accidently. The sequence to enable test mode is to write 80H to this register when all the test bits in the Reset and Test register are zero. This must be followed with a write to the Reset and Test register with the selected test mode (the soft reset bit must be zero). Then write F0H to this register. Once this procedure has been executed, then write the test address to this location, and read this location to view the desired internal status. When test mode is invoked, the only way to restore normal operation is to issue a soft reset, or assert the $\overline{RST}$ pin.

3.7 RESET AND TEST REGISTER

Address = 7AH or FAH
Write only register

7	6	5	4	3	2	1	0
SWRST	0	BRST	ARST	TSMEM	CNTRT	MTPBF	MTPAF

The Reset and test register allows a software reset of the PCM device. It is important that, during the normal operation, the value written to this register is 80H. This register is also used for setting test modes and a value in this register other than 80H causes the PCM to behave unpredictably to the user. The actions that occur when the register is written with 80H are identical to those that occur during power up, and the reset sequences that are described in the reset sequences section. This register is register is initialized to 00H when either the reset input pin (RST) is asserted, or the software reset function is invoked.

3.7.1 MTPAF Microprocessor to Port A FIFO Test (bit 0)

The microprocessor to port A FIFO test is used to verify the integrity of the internal data paths from/to the port FIFO, and to allow testing of the FIFO data cells. When this bit is set, the memory controller sets the data path from the memory side of the port FIFO to the buffer access register in the microprocessor section. The port should be in loopback mode, and when the microprocessor writes or reads the buffer access register the data will be transferred from/to the port FIFO instead of the external memory. Specifically, if the port has the DIR bit set so that data is to go from memory to the peripheral, then the microprocessor would write to the buffer access register, and the data would be read back from the FIFO through the channel data latch in loop back mode. The reverse direction has the microprocessor writing to the channel data latch, and reading the resultant data in the buffer access register.

3.7.2 MTPBF Microprocessor to Port B FIFO Test (bit 1)

This is identical to bit 0 but uses the B channel.

3.7.3 CNTRT Counter Test Mode (bit 2)

When this bit is set, the 16 and 20 bit counters will be divided along 4 bit boundaries, and the carry input to these boundaries will be forced true. The example is of the Buffer Address Pointer, if it is initially set to 12345H, when an access through the autoincrement access register is made, the counter will contain as its next value 23456H. The counters affected by this bit are:

- port A address pointer
- port A transfer counter
- port A EDAC idle counter
- port B address pointer
- port B transfer counter
- port B EDAC idle counter
- buffer address pointer
- refresh address counter.

3.7.4 TSMEM Tri-state Memory Interface (bit 3)

When this bit is set the control signals to the memory interface are forced to a tri-state mode, to allow testing of the memory devices by an external test machine.

3.7.5 ARST A Channel Reset (bit 4)

When written with a one causes the 'A' Channel to receive a reset. This reset does not affect the memory controller, or the other peripheral channel. The reset is removed when a zero is written into the bit, or a PCM reset sequence is initiated. When a channel is receiving a reset it will have its PNRA bit in its Channel Status Register set.

3.7.6 BRST B Channel Reset (bit 5)

This is identical to bit 4 but resets the 'B' Channel.

3.7.7 SWRST Software Reset (bit 7)

When written with a one causes initiation of the PCM reset sequence. This bit is self resetting when the PCM completes the reset sequence (denoted by the PRNR bit in the master status register being cleared), and initiates the PCM reset sequence on the trailing edge of the write strobe of this register.

3.8 BUFFER ACCESS REGISTER

Address = 7CH or FCH
Read/write register

7	6	5	4	3	2	1	0
BAR7	BAR6	BAR5	BAR4	BAR3	BAR2	BAR1	BAR0

The Buffer Access Register is the window that the microprocessor uses to load/store data to/from the buffer memory. The microprocessor address pointer supplies the address to/from which the RAM transfer will be made.

When the microprocessor and board design support the RDY function in hardware, (the NOWAT bit is zero), then this register passes the data through to/from the microprocessor and buffer. The leading edge of the microprocessors read or write strobe causes a "not ready" signal to the microprocessor, holding this state until memory arbitration and the actual data transfer has been accomplished. When the transfer is complete by RDY going true, then the cycle will end and the task is complete. There is no need of the buffer data latch when using the PCM in this mode.

In the case where the RDY function is not supported in the hardware, (the NOWAT bit is one), then the firmware must perform a program sequence to complete a transfer. If the microprocessor is writing data to the buffer, then it will write to this register and data will be latched along with the fact it is a write. The trailing edge of the strobe will cause the PCM to request arbitration for the buffer. The firmware is free at this time to perform other tasks, or poll the "DNR" status bit or the "BANR" in the Master Status Register, or poll the PCM RDY pin. When the access is complete then "not ready" will go false, and the firmware is again allowed to access the buffer.

If the microprocessor desires to read the buffer, then it must first read this register and discard the data. This action is only used to initiate the arbiter request, and latch the fact it is a read access. The trailing edge of the strobe will cause the buffer access to initiate. When the "not ready" condition goes false, then the data that was fetched is available in this register, and also in the Buffer Data Latch. Note that reading the Buffer Data Latch does not cause a "not ready" condition, or perform another access of the buffer, where if data is read from this register then another access will be initiated.

3.9 AUTOINCREMENT ACCESS REGISTER

Address = 7E or FE
Read/write register

7	6	5	4	3	2	1	0
BAR7	BAR6	BAR5	BAR4	BAR3	BAR2	BAR1	BAR0

The autoincrement data register performs the identical function of the buffer access register with the added feature that at the end of the data transaction, the microprocessor address pointer increments to the next address.

If the firmware desires to read or write a small block of data in the buffer, then access through this register will simplify the programming sequence. When the PCM is in the "waitable" microprocessor mode, then firmware need only continuously read or write data through this register. The transfer of data to/from the buffer occurs while the microprocessor is in a wait state, and the incrementing of the Microprocessor Address Pointer occurs in the intervening time between consecutive microprocessor bus cycles. If the PCM is in the "non-waitable" microprocessor mode, then firmware must poll the "not ready" status between accesses of this register. In this mode when reading a string of bytes from the buffer, if the last byte is accessed from this register, then another buffer access will occur, and the address pointer will be incremented. If this is not desired, then the last byte read from the buffer should be read from the buffer data latch instead of from this register.

The autoincrement access register is intended for use when small blocks of data are to be moved to/from the buffer while both ports are transferring data. If a large amount of data is to be moved to/from the microprocessor it is suggested that one of the ports be used in loopback mode, to achieve the maximum data transfer rate.

4.0 DEVICE CHANNELS

There are two device channels that the PCM controls. The channel registers are independent and identical across the two channels. Within the PCM the channels appear as 64 byte memory spaces in the chips total address space of 256 bytes. The channels are referred to as A, and B, with channel A being the 64 bytes of address space from 00H to 3FH, channel B being the 64 bytes of address space from 80H to BFH. Because the devices attached to the channels get their address lines (if necessary) directly from the microprocessor bus the even only address characteristic of the internal registers does not apply.

The registers that control the channels, are in the 32 bytes of address space that immediately follow the respective channels address space. The registers for channel A are in the address space of 40H to 5FH. The registers for channel B are in the address space of C0H to DFH. As these registers are internal, the odd addresses in the channel's respective address blocks are just a ghost image of the registers at the even addresses.

When the controller firmware accesses a register that controls a channel, the microprocessor will not have to wait for access, because these registers are all within the PCM chip, and are always available for immediate access. When the controller firmware accesses a register in a device on a channel, the PCM must evaluate the state and mode of the channel to determine if access of the register is possible. If the PCM is the bus master, then it will arbitrate the access of the channel, and will insert wait states for the microprocessor. The number of wait states for this access is dependant upon both the strobe timing of the channel, and the arbitration time of the channel. If the PCM is in slave mode it will not attempt the access but cause an I/O error interrupt and status to occur.

The channels function is to allow access between a peripheral device and the data buffer. The characteristics of any transfer have both fixed and

variable components. The fixed components are associated with the peripheral device and the hardware that will perform the transfer. These components are set at the beginning of the total transfer, and do not vary for the duration of the transfer. The variable components of the transfer are associated with the data buffer itself, and the arrangement of data, and the firmware control of the data. The fixed components are not 'pipelined', and are set by firmware at the start of a (group of) transfer(s).

The channel 'pipeline' mechanism allows firmware to control the data buffer on the fly. In applications where the firmware is attempting to either control a ring buffer or a cache, the mechanism allows the firmware to 'look ahead' to its next operation.

The registers have been organized in the order in which they would normally be programmed. It is especially important to ensure that the timing register is set up before the control register.

4.1 CHANNEL TIMING REGISTER

The channel timing register is used to control hardware actions that occur during a transfer to the external device. The action the register performs is that of controlling the pulse timing on the channel when the PCM is the bus master. This allows peripheral devices of various timing characteristics to be interfaced to the PCM. The register also defines to the channel logic specific characteristics of the external peripheral device, such as its handshake signal polarities, and parity capability.

The firmware is only allowed to write to the channel timing register when the channel is idle. The channel state machine will set the I/O error bit in the channel interrupt status register if the channel timing register is written while the channel is busy.

All bits in the register are cleared by the reset sequence.

Channel A Address = 40H
Channel B Address = C0H
Read/write register - not pipelined

7	6	5	4	3	2	1	0
LPBM	PPE	DKPL	RQPL	SDTC	DLY	SC1	SC0

NOTE
There is an A or B appended to each bit name corresponding to the appropriate channel.

4.1.1 SC0(1)A (SC0(1)B) Channel Strobe Control Field

The channel strobe control field is a two bit field that is used to control the width of the read and write strobes to the peripheral devices when the channel is in modes where the PCM is the bus master (DMA), or when doing PIO operations. The width of the strobes is programmable by setting the field. When the PCM is doing DMA cycles, for values of 0,1,2,3 the strobes will be 2,4,6,8 clocks wide respectively. When the PCM is doing PIO cycles, for values of 0,1,2,3 the strobes will be 4,6,8,10 clocks wide respectively.

4.1.2 DLYA (DLYB) Delay Strobe Bit

Normally, the $\overline{CS}$ and DACK signals go active two PCM clock before the $\overline{RD}$ or $\overline{WR}$ signals. When this bit is set, this period is extended by 2 PCM clocks. The primary use of this feature is for external decoding logic if multiple peripheral devices exist on the channel.

4.1.3 SDTCA (SDTCB) Strobe Deasserted Time Control Bit

This bit is relevant when the PCM is the bus master and in burst data transfer mode, then this bit is used to control the time that the RD and WR signals are deasserted. When this bit is zero, the RD and WR strobes will be deasserted for two PCM clocks during a data burst. When this bit is one, the RD and WR signals will be deasserted for 4 PCM clocks during a data burst.

4.1.4 RQPLA (RQPLB) DMA Request Polarity Bit

This bit controls the polarity of the PCM port DRQ pin. When this bit is set the PCM will consider the DRQ pin as active high. This is true whether this pin is receiving the request when the PCM is bus master or transmitting the request when the PCM is bus slave.

4.1.5 DKPLA (DKPLB) DMA Acknowledge Polarity Bit

This bit controls the polarity of the PCM port DACK pin. When this bit is set, the PCM will consider the DACK pin as active high. This is true whether this pin is transmitting the acknowledge when the PCM is bus master or receiving the acknowledge when the PCM is bus slave. Note that both the above situations occur when EDAC redundancy byte counting is enabled.

4.1.6 PPEA (PPEB) Port Parity Enable Bit

The device port can be optionally set to check the parity on transfers to the PCM from the peripheral device. Odd parity is supported and is generated when this bit is set. When this bit is set, all reads (data going into PCM) of the device channel by the PCM (either as master or slave) will result in parity checking being done, and interrupts being generated if even parity is detected. It should be noted that **ALL** transfers, including programmed I/O, are checked if this bit is set. When the PPE bit is reset, the port parity bit will be at a logic one level when data is transferring from the PCM to the peripheral device.

4.1.7 LPBMA (LPBMB) Loop Back Mode Enable

The purpose of this bit is to enable the microprocessor to use the FIFO to speed block transfers between the microprocessor and the buffer RAM. When set, this bit paths the channel data latch to the FIFO. It inactivates the outputs of the channel (CS, DACK, DRQ, WR, RD, and data bus). The microprocessor will appear to the channel as an external device and the channel will appear as if in slave mode. More explicitly the loopback mode sets the channel to a state of a non-pausible slave mode. In this state the microprocessor can transfer data to/from the FIFO at its maximum speed with the channel monitoring the FIFO for overrun/underrun conditions. The channel mode bits in the Channel Control Register need not be changed, but the Direction, and Interrupt Enable bits need to be programmed as if programming for an external transfer. In all other channel registers programming is as if for a normal external transfer, with the normal pipeline mechanisms in operation. Note the Direction bit in the Channel Control Register still needs to reflect the direction of transfer to/from an external device. As such the direction bit is SET for a transfer from the buffer to microprocessor (similar to a peripheral write command), though the microprocessor issues READ cycles to access the FIFO data.

4.2 CHANNEL CONTROL REGISTER

Channel A Address = 42H
Channel B Address = C2H
Read/write register - not pipelined

7	6	5	4	3	2	1	0
SLAV	BRST	DISK	EDAC	PAUS	DIR	IVE	IBE

NOTE: There is an A or B appended to to each bit name corresponding to the appropriate channel.

Where the Timing Control Register sets the physical environment of the interface with the external device, the Channel Control Register sets the logical environment of the interface. The register contains two types of parameters about the transfer being programmed. The high order 5 bits are used to identify the logical protocol that the PCM is going to use to interface to the external device. The low 3 bits are used to set a firmware environment to control the manbagement of the transfer direction and interrupts desired.

The firmware is only allowed to write to the chanbnel control register when the channel is idle. The channel state machine will set the I/O error bit in the channel interrupt status register if the channel c ontrol register is written while the channel is busy.

Whenever the firmware writes to the channel control register, the PCM will take 10 PCM clocks to synchronize the action to the PCM clock, and advance the channels status. During this time the firmware can only access non-channel registers.

The register is initalized to A8H by the rest sequence.

4.2.1 IBEA (IBEB) Interrupt on Busy Bit

The busy interrupt bit indicates to the channel that the microprocessor desires an interrupt when the channel very busy status bit transitions from a one to a zero.

4.2.2 DIRA (DIRB) Channel Transfer Direction Bit

The channel transfer direction bit is used to inform the PCM the direction of the transfer of this channel. The PCM uses this information to determine the read/write control of the buffer. When the transfer direction bit is a zero, the device is transferring data to the buffer (device read mode, buffer write mode). When the transfer direction bit is a one, the device is transferring data from the buffer (device write mode, buffer read mode).

The transfer direction bit is used by the channel logic to position the transfer counter, and the input of the FIFO to the source of the data. When the direction bit is a zero, (data transfer from the peripheral to the buffer), the transfer counter is monitoring the device handshake signals, and the count reflects the number of bytes that remain to be transferred from the peripheral device, to the input of the FIFO. When the transfer count exhausts and the FIFO goes empty, the logic will signal the end of this transfer if EDAC mode is not in effect. If EDAC mode is in effect, the channel will monitor the DACK pin to count EDAC trans fers, and when the EDAC idle counter exhausts and the FIFO is empty, it will signal the end of this transfer.

When the direction bit is a one, (data transfer from the buffer to the peripheral), the transfer counter is monitoring the buffer signals, and the count reflects the number of bytes that remain to be transferred from the buffer to the input of the

FIFO. When the transfer count exhausts and the FIFO goes empty, the logic will signal the end of this transfer if EDAC mode is not in effect. If EDAC mode is in effect when the FIFO goes empty, the channel will monitor the DACK pin to count EDAC transfers, and when the EDAC idle counter exhausts it will signal the end of this transfer.

4.2.3 PAUSA (PAUSB) Channel Pause Control Bit (bit 3)

The bit is used by the memory arbiter. When this port is pausible (this bit set), and the other port is non-pausible (this bit reset), then the other port

will have higher priority in the memory arbiter. If this bit is set the same in both channel control registers, then priority is determined by the "AHI" bit in the option 2 register.

This bit enables the "urgent request" logic. Because it controls priority, if the highest priority port's FIFO is near to overrun/underrun condition, then an "urgent request" is sent to the arbiter to stop the other port's burst and force arbitration.

4.2.4 EDACA (EDACB) EDAC Idle Enable (bit 4)

The EDAC Idle Enable bit is used to allow the port interface to share control of the peripheral bus with the WD60C80 EDAC device. The EDAC (Error Detection And Correction) is used in disk applications to append redundancy information to data blocks to allow error correction. The bit when set will allow the PCM to strip this information and not transfer it to the buffer on reads, and to allow the EDAC to append the information to the device data on writes. The EDAC bit is only relevant when the channel is programmed to be a bus master. The Channel EDAC Idle Counter contains a count of the number of redundancy bytes to ignore between data transfers. When this bit is set the transfer counter must be programmed for a single block size. When the transfer count exhausts the channel will tri-state the DACK pin and begin to count DACK pulses until the EDAC idle counter exhausts. While the EDAC idle counter is enabled, no transfers are allowed between the port and the FIFO (the redundancy bytes transfer between peripheral and the EDAC device). When the EDAC idle count exhausts the channel will then continue normal pipeline operations if the firmware has programmed them.

4.2.5 DISKA (DISKB) Disk Type Device (bit 5)

BRSTA (BRSTB) Burst Transfer Device (bit 6)

SLAVA (SLAVB) Slave Mode Interface (bit 7)

These three bits are used collectively to define to the port logic the type of peripheral device it will interface with, and the protocol to use with the interface signals. The signals will be described as per their individual significance, and then their collective significance. The names are derived from relationships they assume when the bit is set.

The SLAVE bit is used to instruct the channel that the external device is the bus master, and as such will control the $\overline{WR}$ and $\overline{RD}$ interface signals. When the bit is zero, the PCM is the bus master and controls the $\overline{WR}$ and $\overline{RD}$ signals. The master/slave relationship controls whether the PCM has the capability of performing programmed I/O on the external bus. When the microprocessor attempts to do programmed I/O and the channel is in a master and non-disk mode, the channel will arbitrate the external bus and interleave the programmed I/O with the DMA transfers the external device is requesting. When the channel is in slave mode, programmed I/O is rejected. If the microprocessor attempts programmed I/O an I/O error interrupt and status are asserted.

The BURST bit defines to the channel that the multiple bytes may be transferred between the external device and the FIFO with a single iteration of the protocol pins (DRQ and DACK). When the bit is a zero then SINGLE cycle mode, where an iteration of the protocol pins result in a single byte being transferred.

The DISK bit defines to the channel that the external device is a disk formatter device, and causes the protocol pins to maintain a different protocol than the normal REQUEST and ACKNOWLEDGE. When the bit is a zero then the normal DRQ and DACK protocol is enforced. Programmed I/O is inhibited when in a disk mode.

In the following text the three bits are grouped with the ordering of SLAVA (SLAVB), BRSTA (BRSTB), and DISKA (DISKB).

4.2.6 000 DMA Single Cycle Master

In this mode, the DRQ pin is the data request and is an input, the DACK pin is the data acknowledge and an output. In this mode, the PCM is con sidered to be the bus master, and the peripheral chip is the bus slave. The peripheral device uses the DACK signal to qualify the data strobes from the PCM. The WR pin is a low true output pin from the PCM, and is active when the PCM is programmed with a channel transfer direction bit set, and the peripheral device has requested service. The WR signal is used to clock data from the PCM to the peripheral device. The RD pin is a low true output pin from the PCM, and is active when the PCM is programmed with a channel transfer direction bit cleared, and the peripheral device has requested service. The RD signal is used to

clock data from the peripheral device to the PCM. The PCM will also use the WR and RD signals when the microprocessor requests programmed input/output of the peripheral device. At this time, the PCM will output the chip select signal to the peripheral device. The timing of the WR and RD signals is programmed in the timing control register of the channel.

In the Single Cycle DMA mode, the PCM will cycle the DACK signal for each byte transferred. The peripheral device can use the DACK signal to deassert its DRQ. This mode is designed to interface with older DMA style peripherals that interfaced with the Intel 8237 DMA chip. This mode will only transfer a byte when the channel FIFO is capable, therefore it is implied that overrun/underrun detection is the responsibility of the peripheral device. The channel will continue to transfer data if a parity error is detected, with the channel counters being captured at the time the error is detected. This mode is compatible with the EDAC device, and supports interleave of programmed I/O through the port and the DMA transfers.

4.2.7 001 DMA Single Cycle Disk

This mode is specifically for the ADS10C00 Disk Formatter Chip. The interface is the same as the DMA Single Cycle Master mode, in that the peripheral device requests service with the DRQ signal, and the PCM which is the bus master acknowledges the request with the DACK signal. The timing of the DACK signal is modified for the ADS10C00 requirements, with the leading edge of the DACK being returned asynchronously in response to the DRQ, and the data and trailing edge occuring synchronous to the PCM clock. In the DMA single cycle disk mode the WR and RD signals are not used. Instead the direction of data transfer is known to both the external device, and the PCM device, so the direction strobes are not required. In this mode the DACK signal is all that is required, as it acts both as an acknowledgement of data transfer, but also as the timing strobe. In this mode the PCM will attempt to transfer a byte on demand from the external device. If the channel FIFO becomes empty or full when another byte transfer is to take place, the channel will latch the data late occurance, and capture the channel counters for the firmware. The transfer will continue until the current transfer count is exhausted. If a parity error is detected during the transfer, the parity error status is latched along with the channel counters, and the transfer continues until the transfer counter exhausts. Since the ADS10C00 device supplies a seperate port for programmed I/O, then programmed I/O through the PCM port is not allowed in this mode. This mode is compatible with the EDAC device.

4.2.8 010 DMA Burst Cycle Master

This mode, tuned for the WD33C93 device, is the same as the DMA Single Cycle Master with the exception that at the end of the data strobe (either WR or RD) the DRQ signal is sampled, and if it is still active and the channel FIFO is capable of transferring another byte, the channel logic will keep the DACK signal asserted, and proceed to transfer another byte of data. This burst sequence will continue until either the external device deasserts DRQ, or the channel FIFO becomes unable to transfer another byte, or the microprocessor has requested a programmed I/O cycle on the external bus. The channel will continue to transfer data if a parity error is detected. This mode allows the highest data rate of the PCM bus master modes, but also requires the bus slave to deassert the DRQ in the shortest amount of time. When the PCM is programmed for strobe timing of 2 PCM clocks (SC1A(B), SC0A(B) = 00), and strobe deassert time of 2 PCM clocks (SDTCA(B) = 0) then the PCM is capable of transferring data at 1/4 the PCM clock rate. This yields a transfer rate of 6.25 Mbytes per second with a 25 MHz clock to the PCM. **(DRQ deassertion time needs to be strictly followed to guarantee reliable operation.)** Since the DACK signal does not change for multiple byte bursts, this mode is incompatible with the EDAC device.

4.2.9 011 Programmed I/O Mode

This mode is used to allow programmed I/O to occur to slave devices. Since it is a master mode then programmed I/O is enabled, but since it does not specify one of the specified interface protocols of bus masters, then it will not perform any peripheral transfers, and the DACK output will remain inactive at all times. When programmed I/O is to occur in a slave such as the WD50C1X configuration, then the firmware will set this mode while programmed I/O is to occur, and set the slave mode again after the programmed I/O is complete. Note that for DMA Single Cycle Master mode, and DMA Burst Cycle Master mode, that programmed I/O requests are interleaved with the data transfers, and there is no need to set Programmed I/O mode to do programmed I/O.

4.2.10 100 Single Cycle Slave Mode

The Single Cycle Slave Mode is similar to the DMA Single Cycle Master Mode, with the sense of the master/slave relationship reversed. In this mode the PCM is assumed to be attached to a host system bus as a DMA slave device. In this mode the sense of the DRQ and the DACK pins are reversed, in that the PCM makes the DRQ pin an output, and requests data from the bus master, and the DACK pin is used by the bus master to signal the PCM that the data transaction is to take place. In this mode it is the responsibility of the bus master to drive the data strobe lines during a data transaction. This configuration is targeted for the XT* environment, and the interface is consistent with the protocol of the Intel 8237 DMA chip, when programmed as it is in that environment.

4.2.11 101 Unused and Reserved Mode

4.2.12 110 Burst Cycle Slave Mode

This mode is similar to the Single Cycle Slave Mode, with the exception that the PCM will not deassert the DRQ output signal unless the FIFO does not have the capability of accepting another byte of data.

4.2.13 111 Slave Burst Mode Disk

In this mode, the connotation of the DRQ pin and the DACK pin change. The PCM is considered to be the bus slave, and the peripheral device is considered to be the bus master. The DRQ pin in this mode becomes an input, and monitors the BDRQ of the peripheral device. The DACK pin in this mode becomes an output, and signals the peripheral device when the peripheral device can continue with its next burst of data. For this discussion, the DACK pin will be referred to as BRDY. The WR pin and the RD pin in this mode are driven by the external bus master, the disk formatter. The protocol of the DRQ and BRDY signals is meant to accomodate the WD50C1X series of disk formatter devices. If the disk formatter is reading the disk then it will transfer a sectors worth data to the FIFO and set DRQ active. It will then wait for the PCM to assert BRDY to indicate that it can proceed with the next sector transfer. If the PCM exhausts its transfer count, and the pipeline register is empty, the PCM will not assert BRDY until the channel pointers have been set for the next transfer. If the PCM has not exhausted its transfer count, or continues in a pipeline operation, then it will send BRDY to the disk formatter to let it proceed with its transfer. If the disk formatter is writing to the disk, it will assert DRQ at the start of the transfer, and wait for BRDY. The PCM will assert BRDY when the channel is started and data is available in the FIFO. At the end of the sector transfer the disk formatter will again signal with DRQ if it desires to continue. If the PCM has the proper conditions to allow the next transfer it will again send BRDY. When programmed I/O is to occur to the WD50C1X device, the firmware must first set the channels mode to master for programmed I/O, then perform the programmed I/O, then return to this mode before starting the channel. If an error occurs (either parity error or data late error) during the transfer of data, the PCM will latch the errorstatus, and the channel counters. When the disk formatter again sends BDRQ the PCM will not send the BRDY signal, effectively halting the disk formatter from proceeding. The user can handle the error condition in one of two ways. The user can issue a stop to the channel, and clear the error, then restart the channel which will then allow the disk formatter to proceed when it sees BRDY. The user can supply external hardware to allow the firmware to reset the disk formatter, as the formatter chip is known to be in a state where write gate is not being asserted.

4.3 CHANNEL STATUS REGISTER

Channel A Address = 44H
Channel B Address = C4H
Read only register

7	6	5	4	3	2	1	0
0	0	DKST	RQST	PNR	FMT	VBSY	BSY

NOTE:There is an A or B appended to each bit name corresponding to the appropriate channel.

4.3.1 BSYA (BSYB) Channel Busy Status

The channel is currently engaged in a transfer.

4.3.2 VBSYA (VBSYB) Channel Very Busy Status

Specifically, this status bit indicates that the pipeline registers cannot be written into. One reason these registers are not available is because the channel is currently engaged in a transfer, and the pipeline registers of the transfer counter and the buffer pointers are currently loaded with the values of the next transfer.. The two status bits inform the firmware the state of the channel. When the two bits are both false, then the channel is currently idle, and the firmware can load the buffer pointer and transfer counter, and initiate an operation on the device. When the busy status is set, but the very busy status is false, the channel is in the busy state. In this state the pipeline registers are available for the firmware to load the values of the next transfer. When the firmware loads the pipeline registers and issues the start channel pulse, the channel will show very busy status. This statis is the very busy state and indicates to the firmware that the channel is not available for any new pointers.

4.3.3 FMTA (FMTB) Channel FIFO Empty Status (Bit 2)

Indicates the current status of the channel FIFO.

4.3.4 PNRA (PNRB) Port Not Ready Status (Bit 3)

The PCM "port not ready" status bit is used to signal the microprocessor that the PCM is currently performing a programmed I/O access of the peripheral, and the registers that are associated with the channels programmed I/O are not available. When the access is complete, this bit will be reset. See also the "DNR" bit in the master status register. This bit is also set if the channel is currently receiving a reset.

4.3.5 RQSTA (RQSTB) Channel DRQ Pin Status (Bit 4)

In order to allow the firmware to poll the state of devices while the channel is in slave mode, the state of the channel's DRQ pin is available on this bit. The DRQ is an input which has programmable polarity. This bit DOES NOT show the actual level of the DRQ pin but rather the logical state; set if DRQ is active, and reset if DRQ is inactive.

4.3.6 DKSTA (DKSTB) Channel DACK Pin Status (bit 5)

Indicates the logical state of the channel DACK pin.

4.4 CHANNEL INTERRUPT STATUS REGISTER

Channel A Address = 46H
Channel B Address = C6H
Read and write/clear bits

7	6	5	4	3	2	1	0
AERR	IOPE	IOE	REJ	LATE	PERR	VBI	BSYI

4.4.1 BSYIA (BSYIB) Interrupt From Busy

This status bit will be set when the busy interrupt bit in the channels control register (bit 0) is set, and the channel busy status bit transi tions from a one to a zero (the channel state transitions from busy to idle). This bit is cleared when a one is written to it.

4.4.2 VBIA (VBIB) Interrupt From Very Busy

This status bit will be set when the very busy interrupt bit in the channels control register (bit 1) is set, and the channel very busy status bit transitions from a one to a zero (the channel state transitions from very busy to busy). This bit is cleared when a one is written to it.

4.4.3 PERRA (PERRB) Channel Parity Error Bit

The channel parity error bit indicates to the firmware that the channel detected a parity error during a read of data either from the dynamic RAMs, or from the peripheral device. When the channel detects a parity error, it will interrupt the microprocessor, set the channel parity error flag. The transfer will continue until the end of the current block, at which time the PCM will wait for the firmware to clear the error and restart transfers.

When the transfer direction is from the buffer to the peripheral then the error occurred in the memory, and the firmware can determine the location of the parity error by reading the current value of the channel pointer, which was captured at the time of the error. When the transfer direction is from the peripheral device to the buffer, then the error occurred on the channel external interface, and the transfer counter will determine the exact byte in error. This bit is cleared when a one is written to it.

4.4.4 LATEA (LATEB) Channel Data Late Error Bit (bit 3)

The channel data late error bit indicates to the firmware that the channel detected a data overrun/underrun error during a transfer of data to/from the channel FIFO. When the channel detects a data late error, it will interrupt the microprocessor, set the channel data late error status. The detection of the overrun/underrun condition is disabled by the channels pause bit being set. This bit is cleared when a one is written to it.

4.4.5 REJA (REJB) Channel Command Reject Error Bit (bit 4)

The channel command reject error bit indicates to the firmware that there was an attempt to start a transfer when the channel had very busy status bit set, or without clearing the channel after an error. When the channel detects this condition it will interrupt the microprocessor, and set the command reject status. The transfer will not be affected. When the current transfer finishes the channel will not perform the next transfer in the pipeline because it is assumed that the pipeline register was corrupted previous to the erroneous start. No transfer will be initiated by the erroneous start command. This bit is cleared when a one is written to it.

4.4.6 IOEA (IOEB) I/O Error Bit (bit 5)

The channel I/O error bit indicates to the firmware that there was an attempt to do a programmed I/O cycle to a channel that was in slave mode, or the channel control register was written while the channel was busy. The I/O error does not halt a transfer in progress, or corrupt an external transfer. The status indicates to the microprocessor that the previous programmed I/O transaction did not transfer valid data, or the load of the channel control register did not take place. This bit is cleared when a one is written to it.

4.4.7 IOPEA (IOPEB) Programmed I/O Parity Error (bit 6)

The channel programmed I/O parity error bit indicates to the firmware that a parity error occurred during a programmed I/O read of the peripheral device. The detection of a programmed I/O parity error does not affect a transfer in progress if the programmed I/O cycle was interleaved with device data transfers in either the DMA Single Cycle Master mode, or the DMA Burst Cycle Master mode. This bit is cleared when a one is written to it.

4.4.8 AERRA (AERRB) Any Error Bit (bit 7)

The Any Error status bit is a read only bit, and is the logical 'or' of the five error status bits. It is provided for convenience to the firmware to easily determine if the previous operation was successful.

sistor through an option jumper to either V_{CC} or GND will passively pull the data line to the desired signal level. The PCM will latch the state of the data bus lines at the end of its reset sequence, so there is a minimum of 5 µs. plus 16 PCM clocks for the resistor to pull the signal to an acceptable level. The value of the resistor is derived from the reset sequence time, and the capacitance of the data lines. The maximum resistor value should be used to reduce the DC and AC loading of the data lines. Since the channel data latch is used for other functions, it is a requirement of the firmware that if the reset status is to be saved, that the firmware must read the channel data latch and save it in its local memory before attempting either programmed I/O to/from the external device, or to put the channel in loopback mode.

4.5 CHANNEL DATA LATCH

Channel A Address = 48H
Channel B Address = C8H
Read / write register

7	6	5	4	3	2	1	0
CDL7	CDL6	CDL5	CDL4	CDL3	CDL2	CDL1	CDL0

NOTE: There is an A or B appended to each bit name corresponding to the appropriate channel.

The Channel Data Latch holds the data associated with 3 different functions performed on the channel. The access of the register does not cause a wait condition.

The first function is that of the "Reset Status Latch." When the PCM is reset either by power being applied, or by writing into the PCM reset register, the PCM samples the channel bus and saves the data in the channel data latch for the firmware. The intent is that the board designer will install passive resistor networks that allow option jumper status to be reflected on the channel bus at reset time. There is an assumption here that the external device will tri-state the channel data bus bits during the power reset condition. With the PCM and the external device both tri-state, a resistor through an option jumper to either V_{CC} or GND will passively pull the data line to the desired signal level. The PCM will latch the state of the data bus lines at the end of its reset sequence, so there is a minimum of 5 µs plus 16 PCM clocks for the resistor to pull the signal to an acceptable level. The value of the resistor is dereived from the reset sequence time, and the capacitance of the data lines. The maximum resistor value should be used to reduce the DC and AC loading of the data lines. Since the channel data latch is used for other functions, it is a requirement of the firmware that if the reset status is to be savbed, that the firmware must read the channel data latch and save it in its local memory before attempting either programmed I/O to/from the external device, or to put the channel in loopback mode.

The second function of the channel data latch is for the loopback mode of the channel. In the loopback mode the microprocessor will read data from this latch, and write data to the latch without wait states. The channel logic will transfer the data between the latch and the FIFO, and check for overrun conditions. See also the "LPBMA" ("LPBMB") bit in the Channel Timing Register.

The third function is that of the port programmed I/O data latch. When the "RDY" function is supported in hardware, then programmed I/O proceeds through the normal address space reserved for external peripheral I/O. The leading edge of the microprocessors read or write strobe causes a "not ready" signal to the microprocessor, holding this state until arbitration for the peripheral port and the actual data transfer has been accomplished. When the transfer is complete by RDY going true, then the cycle will end and the task is complete. In this case this register is not used, though it still performs its intended function of capturing the programmed I/O data to/from the peripheral.

In the case where the RDY function is not supported in the hardware, then the firmware must perform a program sequence to complete a transfer. If the microprocessor is writing data to the port, then it will write to the programmed I/O data space, and data will be latched along with the fact it is a write. The trailing edge of the strobe will cause the PCM to request arbitration for the channel. The firmware is free at this time to perform other tasks, or poll the "DNR" status bit or the "PNRA" ("PNRB") in the Channel Status Register, or poll the PCM RDY pin. When the access is complete then "not ready" will go false, and the firmware is again allowed to access the channel for programmed I/O.

If the microprocessor desires to read the channel, then it must first read from the programmed I/O data space, and discard the data. This action is only used to initiate the arbiter request, and latch the fact it is a read access. The trailing edge of the strobe will cause the buffer access to initiate. When the "not ready" condition goes false, then the data that was fetched is available in this

register, and also in the programmed I/O data space. If the data is then read from the programmed I/O data space, then another programmed I/O cycle will be initiated, while if the data is read from this register, another programmed I/O access will not take place.

4.6 CHANNEL BUFFER POINTER

Channel A Address = 4EH (BP19 - BP16)
Channel A Address = 4CH (BP15 - BP08)
Channel A Address = 4AH (BP07 - BP00)
Channel B Address = CEH (BP19 - BP16)
Channel B Address = CCH (BP15 - BP08)
Channel B Address = CAH (BP07 - BP00)
Pseudo-read/write registers

7	6	5	4	3	2	1	0
0	0	0	0	BP19	BP18	BP17	BP16
BP15	BP14	BP13	BP12	BP11	BP10	BP09	BP08
BP07	BP06	BP05	BP04	BP03	BP02	BP01	BP00

NOTE: There is an A or B appended to each bit name corresponding to the appropriate channel.

4.6.1 BP19A (BP19B) through BP00A (BP00B) Buffer Pointer Address Bits

The channel buffer pointer is composed of three registers that contain the 20 bit memory address of the data. The actual hardware that mechanizes the buffer pointer is a presettable 20 bit counter, which is the actual pointer, a 20 bit holding register connected to the preset inputs of the counter (the pipeline register), and a 20 bit latch connected to the outputs of the counter for reading the counter. The microprocessor can actually only load the pipeline register from its data bus. When the firmware writes to any of the bytes in the buffer address pointer, a flag in the PCM is set to remember that the pipeline register was written. The channel state machine will use this flag to indicate that the buffer address pointer is to be loaded with a new value. When the channel state machine enters the "busy" state it will test and clear the flag, and load the counter from the holding register if the flag was set. See also the description of channel "states" in the Channel Start Register.

If the channel enters the "busy" state and the flag is cleared, indicating that firmware did not load the pipeline register, then the counter continues from its current position. The firmware then can mechanize a ring buffer system with only the firmware overhead of writing the starting address at the initial transfer, and then only issuing start commands for succeeding transfers. The data will then appear as a single large contiguous block. If data is to be transferred from discontiguous areas of the data buffer as in a cache buffer system, then the firmware has the added overhead of writing the next address to the pipeline register for each transfer segment that is not contiguous.

If the microprocessor desires to read the counter while it is active, the firmware must first write to the capture pointer register, which will make a copy of the counter at the time, and the microprocessor can then read the 3 bytes of address without any sampling errors. When the channel detects an error during a transfer it will copy the counter to the capture latch register for reading. When the channel transitions to the idle state, and the previous operation had no error, the address pointer is automatically copied to the capture latch register for reading.

4.7 CHANNEL TRANSFER COUNTER

Channel A Address = 52H (TC15 - TC08)
Channel A Address = 50H (TC07 - TC00)
Channel B Address = D2H (TC15 - TC08)
Channel B Address = D0H (TC07 - TC00)
Pseudo-read/write registers

7	6	5	4	3	2	1	0
TC15	TC14	TC13	TC12	TC11	TC10	TC09	TC08
TC07	TC06	TC05	TC04	TC03	TC02	TC01	TC00

4.7.1 TC15 through TC00 Transfer Counter Bits

The channel transfer counter appears as a read/write register, but in fact it is a write only register, and a read only counter. When the firmware writes to the transfer counter it is writing to a pipeline register. When the transfer counter is read, it is reading a capture latch that is loaded from the actual counter. The reason for this mechanization is that the pipeline register needs to hold the byte count of the transfer, and to load this value into the counter each time the channel begins an operation. This value only need change when the firmware requires a different granularity of data. When the channel detects an error, both the address pointer and the transfer counter are captured. The data that the firmware requires is how far into the transfer the operation proceeded before the error was detected. When the firmware reads the actual counter, the value is the residual count of the number of bytes that are left in the transfer, and from this information the firmware can deduce the number of bytes that transferred sucessfully. The firmware can also sample the current transfer counter by writing to the Channel Pointer Capture Register.

The channel transfer counter is composed of two registers that contain the 16 bit value that is the number of data bytes of the current transfer. The actual hardware that mechanizes the transfer counter is a presettable 16 bit down counter, which is the actual counter, and a 16 bit holding register which is the pipeline. The counter is unidirectional going from number of bytes that is desired to be transferred, to zero. The microprocessor can actually only load the pipeline register from its data bus.

When the Channel Start Register is set, and the channel is currently idle, then the channel state machine will load the transfer counter from the pipeline register, and start the operation. At this time the pipeline register is now free, and the firmware can load the transfer count of the next transfer into the pipeline register.

It should be noted here that for most devices that are envisioned, the block size that will be entered into the transfer counter, will be the sector (frame, etc.) size of the attached block oriented device and from that time the firmware will probably not load the transfer counter pipeline register. Hence if the firmware starts the channel again, the transfer counter will continually be updated with the block size of the device, without the firmware repeatedly loading the value on each transfer. The transfer count can be multiples of the device block size, if the firmware desires to cluster blocks together and view them as larger data items. A special case exists when EDAC Idle Enable control bit is set in the Channel Control register, in that the transfer counter is used to count the number of bytes between redundancy fields, and therefore can not be multiples of the block size.

4.8 CHANNEL START REGISTER

Channel A Address = 54H
Channel B Address = D4H
Write onlyregister

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Whenever the firmware writes to the channel start register, the PCM will take 10 PCM clocks to synchronize the action to the PCM clock, and advance the channels status. During this time the firmware can only access non-channel registers.

Under normal conditions the PCM will have the channel enabled before the device is armed for a transfer. The exception to this is likely to be a programmable device that requires the PCM to be the bus slave (eg. WD501X type devices). In that case the mode will have to be changed to slave after the firmware has set up the device, as there is no programmed I/O facility in slave mode. It should be noted that once the operation of the peripheral device has been started, it may assume master status at any time, and as such, can fight the PCM if the firmware does not enter slave mode before this happens. Also, delay in starting the transfer by writing to this register, may result in over/underrun errors in the peripheral device. Writing into the channel start register will produce varied responses from the channel, depending upon the current mode and state of the channel.

When the channel is in the idle state (busy and very busy status are both cleared), and the firmware writes into the channel start register, this indicates to the channel that the firmware desires the channel to begin operations. The channel state machine will load the transfer counter from the transfer counter pipeline register, and if the channel buffer address pointer pipeline has been written into, it will load the buffer pointer from the pipeline register, the flag for the address pointer will be reset, and channel busy status will set. When the busy status is set the pipeline registers are now available for the firmware to write the parameters of the next transfer.

When the channel is in the busy state (busy status set, and very busy status cleared), and the firmware writes into the channel start register, this indicates to the channel that the firmware desires the channel to continue operations when the current operation finishes. The channel very busy status will set. When the very busy status is set the pipeline registers are not available for the firmware to write. The channel is now considered to be in the very busy state. The channel will clear the very busy status and exit the very busy state when the current transfer completes. When the transfer completes the channel state machine will advance to the busy state and perform the same sequences that are described going from idle to busy. The channel counters are now set with values for the new transfer and the pipeline registers are again available for the firmware to queue the parameters of another transfer and issue another start.

When the channel is in the very busy state (busy and very busy status are both set), and the firmware writes into the channel start register, this will cause the channel to set the command rejected status and terminate operations on the channel when the current transfer completes. The channel state machine assumes that the firmware has corrupted the values in the pipeline when it issued the last start command. When the current operation completes the channel state machine will stay in the command reject error state until a channel stop is issued, which will then bring the state machine back to idle.

Finally, any attempt to start a channel with an uncleared error will result in a command reject error.

4.9 CHANNEL STOP REGISTER

Channel A Address = 56H
Channel B Address = D6H
Writeonly register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Whenever the firmware writes to the channel stop register, the PCM will take 10 PCM clocks to synchronize the action to the PCM clock, and advance the channels status. During this time the firmware can only access non-channel registers.

4.10 CHANNEL POINTER CAPTURE REGISTER

Channel A Address = 58H
Channel B Address = D8H
Write only register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Whenever the firmware writes to the channel pointer capture register, the PCM will take 10 PCM clocks to synchronize the action to the PCM clock, and advance the channels status. During this time the firmware can only access non-channel registers.

When channel pointer capture register is written into, the capture latches for the channel pointer and channel transfer counter will sample the current state of the counters. This allows the microprocessor to detect the current position of the pointer and counter while they are active.

4.11 EDAC IDLE COUNTER

Channel A Address = 5AH
Channel B Address = DAH
Pseudo-read/write register

7	6	5	4	3	2	1	0
EC07	EC06	EC05	EC04	EC03	EC02	EC01	EC00

In order for the PCM to function with an external Error Detection and Correction device (EDAC), it is necessary for the PCM to be able to ignore (or "idle") while data transfers intended for or generated by the EDAC device transpire. To this end, each channel has an 8 bit down counter called the EDAC idle counter. It is mechanized by an 8 bit holding register that is loaded by the microprocessor with the number of bytes that should be ignored at the end of each block transferred, and an 8 bit down counter, decremented on the trailing edge of DACK once the PCM has finished its transfer. This counter is not latched like the address pointers and transfer counters, so any attempt to read this counter while it is running may result in synchronization errors. This value need only be set, to suit the EDAC device being used, after a reset condition. Thereafter the EDAC mode can be enabled and disabled using the EDAC Idle Enable Bit in the Channel Control Register.

5.0 MICROPROCESSOR INTERFACE

The PCM interface to the controller microprocessor is designed to be compatible with microprocessors of the multiplexed address/data bus design. It is specifically targeted to interface to Intel 80186 microprocessor with no external logic, but with some external logic the PCM can interface to other microprocessors that have multiplexed buses, or to non-multiplexed bus microprocessors. Speed penalties will exist for these implementations.

The PCM appears to the microprocessor as a contiguous address space of 256 bytes. The 8 bit address that decodes the unique location within the PCM is supplied by 8 multiplexed address/data pins. The address bit 0 is however ignored as all internal registers are mechanised to appear on even byte boundaries to suit the 80186. The PCM latches the address during the ADDRESS LATCH ENABLE signal. The 8 bits are used as both address information at ALE time, and data information at all other times. The PCM latches the bus address on all microprocessor cycles, but only responds to those cycles that are accompanied by the chip select signal. This signal is derived by the controller designer by doing a decode of the address information above bit A07, or using the already decoded outputs of the 80186. The controller designer has the flexibility to map the PCM's address space into the microprocessors memory space, or the I/O space, or a combination of both.

The PCM's interface includes a general interrupt signal to inform the microprocessor of changes of states of status within the PCM, and two signals to control the direction and timing of microprocessor bus cycles that involve the PCM. There are also two signals that allow the PCM to synchronize resource sharing for the microprocessor. When the PCM detects a bus cycle within its address range (chip select asserted), it decodes the address that it has latched, and determines

the resource that is to be accessed. The PCM has control of 4 general resources (internal registers, buffer memory, channel A, and channel B), and maps these resources into the address space.

The microprocessor interface deviates at this point depending upon the microprocessor that is interfaced, and the microprocessor and board design to support the READY/WAIT signal. In the case where the microprocessor and board design support the RDY function, the PCM uses the microprocessor RDY line to hold the microprocessor in a wait condition if the resource is not ready for immediate access. The internal register set of the PCM does not insert any wait states. The access of the other resources may or may not insert wait states.

If the microprocessor is accessing a device on one of the peripheral device channels, the local bus arbitrator for that channel will deassert RDY to the microprocessor until the channel is free for the microprocessor access to proceed. When the channel has been acquired the PCM will assert CSA or CSB (peripheral chip select) to select the peripheral device. When the access of the peripheral device is finished, the PCM will assert RDY, which will allow the microprocessor to proceed. If the access of the peripheral channel results in an I/O error, there will be no wait states inserted. If the microprocessor is accessing the buffer RAM, the memory arbiter will deassert RDY to the microprocessor until the buffer access has been done.

In the case where the microprocessor or the board design does not support the RDY function, the previously described actions to initiate the PCM function are identical. The difference is when the PCM deasserts the RDY function. In this case the microprocessor will not go into a wait condition, and is free to continue executing code. Internally, the PCM latches the access initiated, and the direction of the access, and proceeds to complete the access without holding the microprocessor. Data latches in each port and the buffer area will hold the data for the microprocessor while the access is in the arbitration queue. The microprocessor now has the responsibility of testing status (either in a PCM internal register, or the RDY signal), and when the access is complete, and to fetch the accessed data if the access was a read.

6.0 I/O MEMORY MAP

The PCM has within it four resources that the controller's firmware can access. The first resource is the PCM's register file. This consists of various registers that the firmware can read and write to both control the operation of the PCM, and sense the status of operations. The registers that are associated with a particular channel, are in an address space that is adjacent to the channel, and registers that are not associated with a particular channel use a partial decode of addressing so they are made to appear in both channels address space. Since these registers are dedicated to the microprocessor, there is no arbitration required to access these registers, and bus cycles to these registers involve no wait states.

The second resource that the PCM controls is the memory array. The memory array is made to appear to the firmware as a single memory location. The access to the actual memory location must be arbitrated along with accesses from the two peripheral channels, so access to the buffer memory may encounter some significant delays when there is heavy buffer traffic. The addressing of the memory array can either be static by loading the microprocessor page register, or can be made to autoincrement when searching through the data buffer.

The other two resources that the PCM controls are the device buses. The 2 device buses are made to appear as 64 byte spaces. Channel A devices appear in the offset range of 00H to 3FH. Channel B devices appear in the offset range of 80H to BFH. The actual registers that can be accessed through the channel, and the locations that they are made to appear at are under control of the board designer.

FCH	DATA BUFFER
E0H	BUFFER MGR. REGISTERS
C0H	CHANNEL B REGISTERS
80H	CHANNEL B
7CH	DATA BUFFER
60H	BUFFER MGR. REGISTERS
40H	CHANNEL A REGISTERS
00H	CHANNEL A

7.0 INTERRUPTS

All interrupt conditions within the PCM are grouped into a single interrupt line going out of the WD60C40. Individual interrupt conditions can be enabled/disabled within the PCM, but there is no prioritization of interrupts within the device. Interrupt conditions are reset when the firmware writes a one to the bit to clear the particular interrupt con dition.

8.0 RESET SEQUENCES

The PCM chip will be initialized when the $\overline{RST}$ pin is asserted, or the firmware writes a one into the soft reset bit of the PCM reset register. When the PCM is reset, it aborts all transfers, sets channel control registers to 00 and tri-states the port's control lines ($\overline{RD}$, $\overline{WR}$, DRQ, DACK), disables refresh by resetting the RAM control logic to a special state, and clears all interrupts. The firmware is responsible for setting up refresh and initializing the RAM to suit the dynamic RAM requirements. Resetting the PCM terminates access of the dynamic RAM array, allowing the idle time requirement of dynamic RAMs at power on. When the PCM option register is written to, this signals the PCM that the idle time requirement of the dynamic RAM array has passed, and the PCM will begin refresh cycles if refresh is enabled, it is the requirement of the controller firmware to delay the required idle time interval from power on condition before writing into the PCM's option register, to delay the required time interval from enabling refresh until the dynamic RAMs are ready for operation, and to initialize the memory array to proper parity. The PCM is initialized to static RAM mode by master reset. When the PCM is reset, the memory signals will be deasserted, and the channel control signals will all be tri-state. The memory signals will return to normal operation when the firmware writes into the option register. The channel signals will return to normal operation when the firmware writes into the channel control register. It should be noted that programmed I/O to the peripheral port can not be performed until the channel control register is written as master mode after a reset.

9.0 READY SEQUENCES AND LATENCIES

The RDY (ready) signal will be asserted low when the PCM has an internal resource that is unavailable to the firmware. Then time that the signal will be asserted depends upon the mode that the microprocessor interface is in, and the resource that is being accessed. When the PCM is in the 'waitable' microprocessor mode, the RDY signal will assert low when the internal address decode with CS selects a resource. The resource will start its access 3 PCM clocks after the microprocessor's data strobe asserts. When the PCM is in the 'non-waitable' mode, the RDY signal will assert low 30 ns. after the microprocessor's data strobe ends. The resource will start its access after the 3 PCM clocks for synchronization. These times are in addition to the following discussion which describes the components that determine the time of the particular access.

When the firmware accesses the buffer, the time the access takes is dependant upon the microprocessor's placement in the memory arbitration scheme, and any latency associated with its request occuring while a port data burst is in progress. The microprocessor is the highest priority device in the memory arbitration scheme, since it is a single cycle device, and its request period can be controlled by the firmware. The latency associated with a port data burst is found from the equation:

TBRST = 2 (N) + 4 (P+1) expressed in PCM clocks

N = number of bytes in the ports burst

P = number of RAS cycles occuring during the burst, or # of page boundaries crossed during burst.

Example

If the port transfers 22 bytes during the burst, and crosses a page boundary, then the total burst will require 52 PCM clocks. For a PCM clock frequency of 16 Mhz. this will be a time of 3.25 microseconds.

The N factor in the above equation depends upon the number of bytes in the FIFO when the burst begins, and the memory transfer rate, and the peripheral transfer rate. The value of N should be

determined by simulation but an estimation can be made from the equation:

N = MTR (IFBC) / (MTR - PTR)

MTR = memory transfer rate, 1/2 PCM clock frequency

PTR = peripheral transfer rate, (in MHz)

IFBC = initial FIFO byte count at start of burst

NOTE:
IFBC is in the range of 0 to 15 for WD60C40

The memory transfer rate when the port is in a burst is 2 PCM clocks per byte. If the PCM is supplied with a 16 MHz clock, then the memory trans fer rate will be 8 MHz (8 Mbytes/second). The peripheral transfer rate is supplied in the same terms as the memory transfer rate. As an example the WD33C93A SCSI interface peripheral is capable of a transfer rate of 4 Mbytes/second, or 4 MHz. The FIFO size in the PCM is 15 bytes. If these values are applied to the equation, and use the value of 14 bytes for the initial FIFO condition, the result is 29 bytes for the expected burst. At the memory transfer rate of 8 Mbytes per second, this would yield a burst time of 3.625 microseconds.

It can be seen that as the peripheral transfer rate approaches the memory transfer rate, the denominator of the equation approaches zero, and the size of the burst increases rapidly. Therefore if the PCM is designed into a system with the peripheral transfer rate very close to the memory transfer rate, large microprocessor buffer access times can be expected. The size of burst is limited by the refresh mechanism of the PCM. The PCM will queue up to 4 refreshes, and then force an ar bitration, which the microprocessor will win because it is highest priority. In a system that has refreshes programmed at the normal rate of 15.6 microseconds, this effectively limits the maximum burst and the maximum latency to about 62 microseconds.

10.0 NON-CHANNEL REGISTERS MAP

7	6	5	4	3	2	1	0	REGISTER/ ADDRESS
MPAR	CAW1	CAW0	SRAM	RRC3	RRC2	RRC	RRC0	OPT 60H or E0H
0	0	NOWAIT	WAITE	AHI	INTE	BINTE	AINTE	OP2 62H or E2H
DNR	0	0	PRNR	BANR	PPE	BINTR	AINTR	MSR 64H or E4H
0	0	0	0	0	0	0	0	66H or E6H
BDL7	BDL6	BDL5	BDL4	BDL3	BDL2	BDL1	BDL0	BDL 68H or E8H
MP07	MP06	MP05	MP04	MP03	MP02	MP01	MP00	MAP 6AH or EAH
MP15	MP14	MP13	MP12	MP11	MP10	MP09	MP08	6CH or ECH
0	0	0	0	MP19	MP18	MP17	MP16	6EH or EEH
TAS7	TAS6	TAS5	TAS4	TAS3	TAS2	TAS1	TAS0	TAS 78H or F8H[1]
SWRST	0	BRST	ARST	TSMEM	CNTRT	MTPBF	MTPAF	RTR 7AH or FAH
BAR7	BAR6	BAR5	BAR4	BAR3	BAR2	BAR1	BAR0	BAR 7CH or FCH
BAR7	BAR6	BAR5	BAR4	BAR3	BAR2	BAR1	BAR0	AAR 7EH or FEH

NOTES
All "odd" addresses willl access the "even" address that is one lower.
[1]Contents of addresses 70H (or F0H) through 76H (or F6H) must be written as 00 and read as 00.

35

11.0 CHANNEL REGISTERS MAP

7	6	5	4	3	2	1	0	REGISTER/ ADDRESS
LPBM	PPE	DKPL	RQPL	SDTC	DLY	SC1	SC0	CTR 40H or C0H
SLAV	BRST	DISK	EDAC	PAUS	DIR	IVE	IBE	CCR 42H or C2H
0	0	DKST	RQST	PNR	FMT	VBSY	BSY	CSR 44H or C4H
AERR	IOPE	IOE	REJ	LATE	PERR	VB1	BSY1	ISR 46H or C6H
CDL7	CDL6	CDL5	CDL4	CDL3	CDL2	CDL1	CDL0	CDL 4BH or C8H
BP07	BP06	BP05	BP04	BP03	BP02	BP01	BP00	CBP 4AH or CAH
BP15	BP14	BP13	BP12	BP11	BP10	BP09	BP08	4CH or CCH
0	0	0	0	BP19	BP18	BP17	BP16	4EH or CEH
TC07 TC15	TC06 TC14	TC05 TC13	TC04 TC12	TC03 TC11	TC02 TC10	TC01 TC09	TC00 TC08	CTC 50H or D0H 52H or D2H
0	0	0	0	0	0	0	0	CST 54H or D4H
0	0	0	0	0	0	0	0	CSP 56H or D6H
0	0	0	0	0	0	0	0	CCP 58H or D8H
EC07	EC06	EC05	EC04	EC03	EC02	EC01	EC00	CEC 5AH or DAH
0	0	0	0	0	0	0	0	Reserved 5CH or DCH
0	0	0	0	0	0	0	0	Reserved 5EH or DEH

NOTE:
There is an A or B appended to each bit name corresponding to the appropriate channel.

12.0 ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power Supply	V_{CC}	4.5	5.5	V
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Ouptut Low Voltage I_{OL} = 2.0 mA	V_{OL}		0.4	V
Output High Voltage, IOH = 400 µA	V_{OH}	2.8		V
Leakage Current Low	I_{LL}		10	µA
Leakage Current High	I_{LH}		-10	µA
Supply Current	I_{CC}		100	mA
Power Dissipation	PD		500	mW

The output loading depends on the pin function and are as follows:

IOL	IOH	SIGNAL NAME
6 mA	-2.5mA	AD7 to AD0
2 mA	-1.0 mA	CSA, CSB DRQA, DRQB DACKA, DACKB ARD, BRD AWR, BWR DBA7 to DBA0, DBAP DBB7 to DBB0, DBBP RB7 to RB0, RBP BA9 to BA0 RAS, CAS, $\overline{W}$
6 mA	O.D.	RDY PINT

35

13.0 MISCELLANEOUS CHARACTERISTICS

Operating Temperature	0^{o} to 70^{o} C
Absolute Maximum Ratings	All voltages referenced to V_{SS}
V_{CC}	7.0 Volts
Voltage to any pin	-0.3 to V_{CC} + 0.3 Volts
Storage Temperature	-40^{o} to $+125^{o}$ C

NOTE:
Maximum limits indicate the point where permanent device damage occurs. Continuous operation at these limits is not intended, and should be limited to those conditions specified in Electrical Characteristics sections.

14.0 TIMING SPECIFICATION

In these timing diagrams the following assumptions have been made:

(1) As port B is identical to port A, only port A timings need be shown.

(2) The DRQA signal has been programmed as active HIGH.

(3) The DACKA signal has been programmed as active LOW.

(4) The timing specifications assume the following loading on each pin.

MAX LOADING	PIN NAMES
120 PF MAX	BA9 to BA0 RB7 to RB0, $\overline{RBP}$ RAS, CAS, W
100 PF MAX.	AD7 to AD0
50 PF MAX.	CSA, CSB DACKA, DACKB ARD, BRD AWR, BWR DBA7 to DBA0, DBAP DBB7 to DBB0, DBBP RDY PINT

14.0 TIMING DIAGRAMS

The timing diagrams use the following nomenclature:

REF

The Reference number on the timing waveform diagram.

NAME

Abbreviated Symbol by which the timing is referred.

DESCRIPTION

Description of the timing referred.

REFERENCE

The reference edge to which the timing is specified.

LE = Leading edge

TE = Trailing edge

RE = Rising edge

FE = Falling edge

IC = Initial Condition

R/S

Classification of requirement/specification.

R = Requirement of the external circuit.

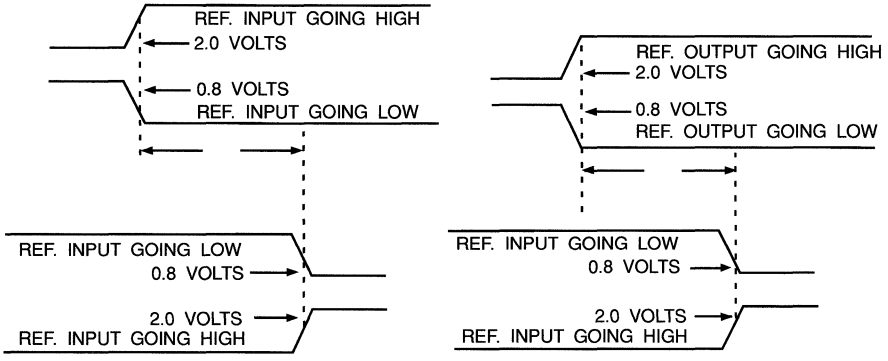
S = WD60C40 output timing specification.

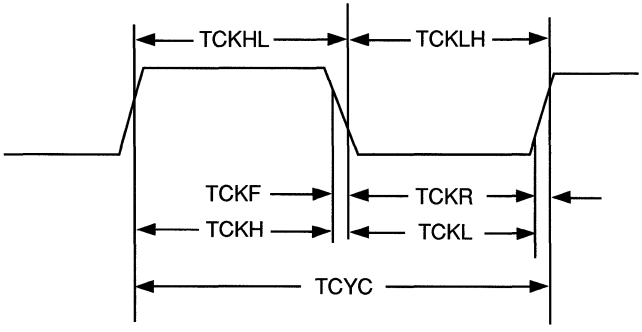
TIMING

Value, unit, and characteristic of timing.

AC TIMINGS

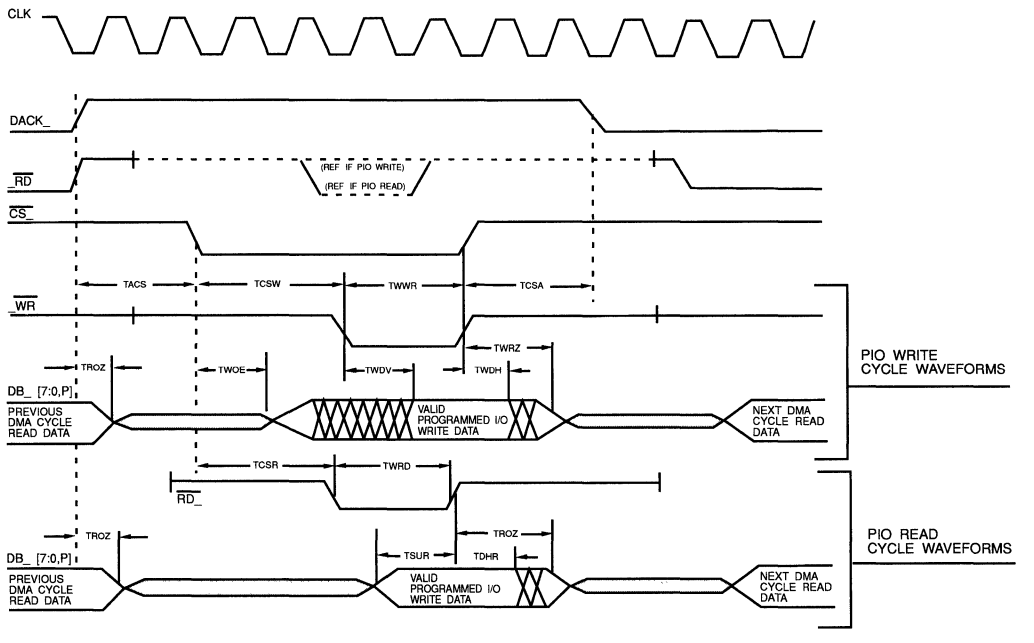
** RAM PORT VIL = 0.8 VOLTS, VIH = 2.4 VOLTS
VOL = 0.8 VOLTS, VOH = 2.4 VOLTS





NAME	REF	R/S	MINIMUM	MAXIMUM
TCYC = Input Clock Period		R	40 NS	
TCKL = Input Clock Low		R	17 NS	
TCKH = Input Clock High		R	17 NS	
TCKR = Input Clock Rise		R		5 NS
TCKF = Input Clock Fall		R		5 NS
TCKHL = Input Clock High to Low		R	20 NS	
TCKLH = Input Clock Low to High		R	20 NS	

FIGURE 4. RISE/FALL AND MISC. TIMING

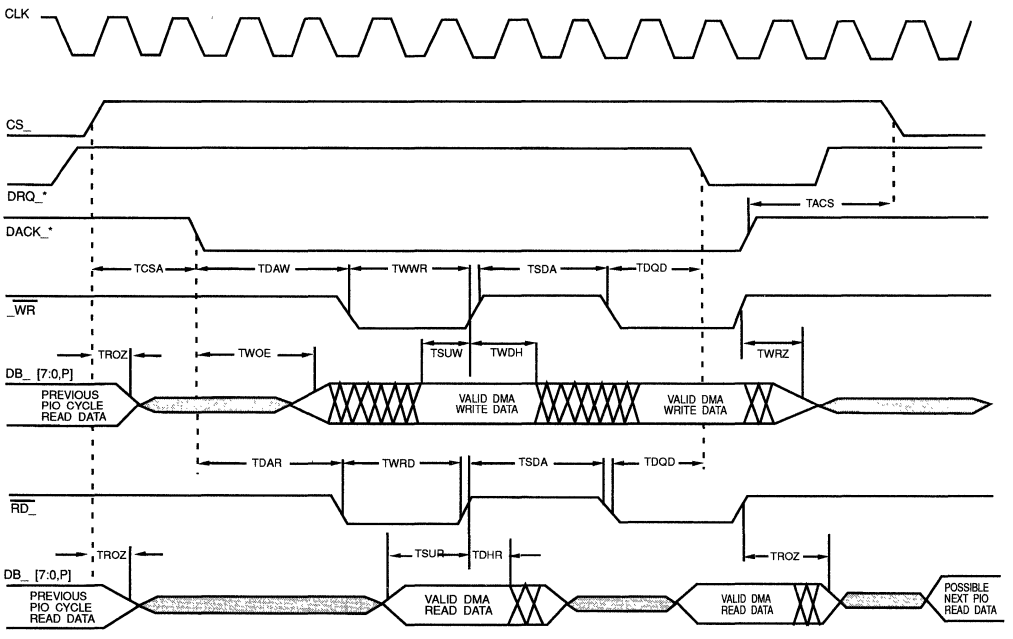


NAME	REF	R/S	MINIMUM	MAXIMUM
TACS = Time of DACK to Chip Select	TE	S	2 TCYC - 15 NS **	
TCSA = Time of Chip Select to DACK	TE	S	2 TCYC - 15 NS **	
TCSW = Chip Select to Write Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWWR = Width of Write Strobe (See SC in Section 4.1)		S	4 TCYC - 15 NS	10 TCYC + 15 NS
TWOE = Time to Output Enable in Write	LE	S	0 NS	
TWDV = Time to Data Valid in Write	LE	S		40 NS
TWDH = Time of Data Hold in Write	TE	S	TCKH - 5 NS	
TWRZ = Time of Write Strobe to High Z	TE	S	TCKH - 5 NS	TCKH + 20 NS
TCSR = Chip Select to Read Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWRD = Width of Read Strobe (See SC in Section 4.1)		S	4 TCYC - 15 NS	10 TCYC + 15 NS
TSUR = Data Setup Time of Read Data	TE	R	30 NS	
TDHR = Data Hold Time of Read Data	TE	R	0 NS	
TROZ = Time of Read Strobe to High Z	TE	R		2 TCYC **

** If SDTC in Section 4.1 is set, then value is 4 TCYC

FIGURE 5. PIO READ/WRITE OF EXTERNAL DEVICES

35



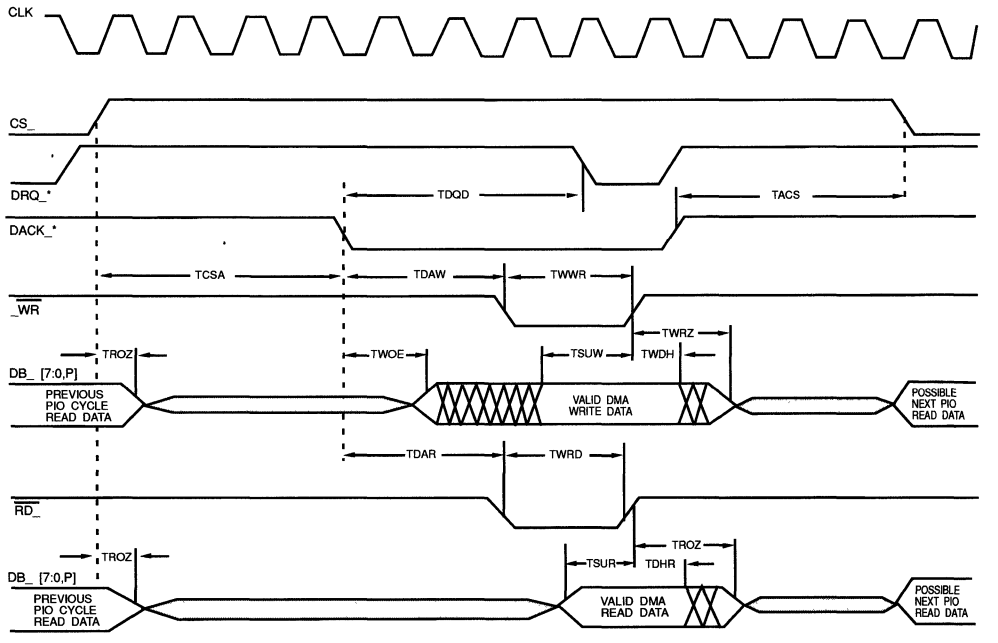
NAME	REF	R/S	MINIMUM	MAXIMUM
TACS = Time of DACK to Chip Select	TE	S	2 TCYC - 15 NS **	
TCSA = Time of Chip Select to DACK	TE	S	2 TCYC - 15 NS **	
TDAW = Time DACK to Write Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWWR = Width of Write Strobe (See SC in Section 4.1)		S	2 TCYC - 15 NS	8 TCYC + 15 NS
TWOE = Time to Output Enable in Write	LE	S	0 NS	
TSUW = Data Setup Time to Write	TE	S	2 TCYC - 40 NS	8 TCYC + 15 NS
TWDH = Time of Data Hold in Write	TE	S	TCKH - 5 NS	
TWRZ = Time of Write Strobe to High Z	TE	S	TCKH - 5 NS	TCKH + 20 NS
TDAR = Time DACK to Read Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWRD = Width of Read Strobe (See SC in Section 4.1)		S	2 TCYC - 15 NS	8 TCYC + 15 NS
TSUR = Data Setup Time of Read Data	TE	R	30 NS	
TDHR = Data Hold Time of Read Data	TE	R	0 NS	
TROZ = Time of Read Strobe to High Z	TE	R		2 TCYC **
TDQD = Time to DRQ Deasserted (to stop Burst)	LE	R		2 TCYC - 20 NS ***
TSDA = Time of Strobe Deactivated (See SDTC in Section 4.1)		S	2 TCYC - 15 NS	4 TCYC + 15 NS

* DRQ Polarity shown high true; DACK polarity shown low true.

** If SDTC in Section 4.1 is set, then value is 4 TCYC.

*** Based on SC and SDTC set to zero. Add 2 TCYC for each programmed state.

FIGURE 6. DMA BURST MODE TRANSFERS



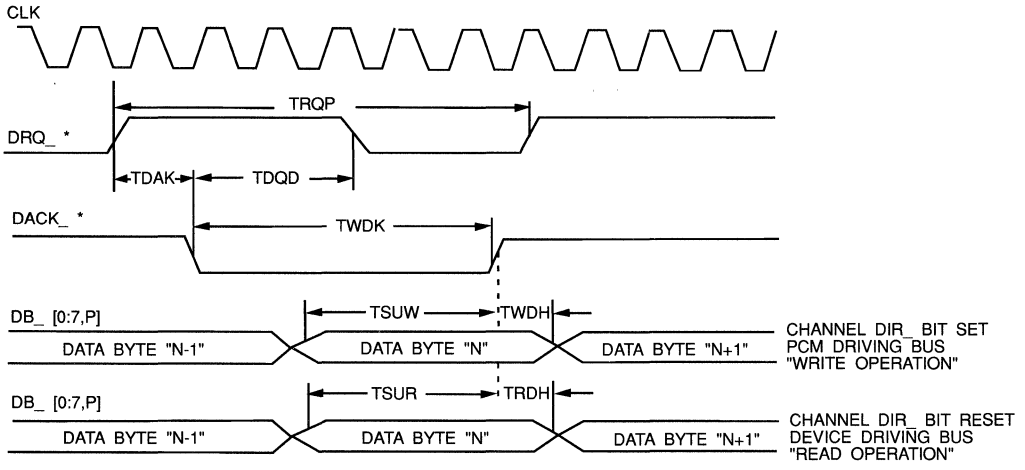
NAME	REF	R/S	MINIMUM	MAXIMUM
TACS = Time of DACK to Chip Select	TE	S	2 TCYC - 15 NS **	
TCSA = Time of Chip Select to DACK	TE	S	2 TCYC - 15 NS **	
TDAW = Time DACK to Write Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWWR = Width of Write Strobe (See SC in Section 4.1)		S	2 TCYC - 15 NS	8 TCYC + 15 NS
TWOE = Time to Output Enable in Write	LE	S	0 NS	
TSUW = Data Setup Time to Write	TE	S	2 TCYC - 40 NS	8 TCYC + 15 NS
TWDH = Time of Data Hold in Write	TE	S	TCKH - 5 NS	
TWRZ = Time of Write Strobe to High Z	TE	S	TCKH - 5 NS	TCKH + 20 NS
TDAR = Time DACK to Read Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWRD = Width of Read Strobe (See SC in Section 4.1)		S	2 TCYC - 15 NS	8 TCYC + 15 NS
TSUR = Data Setup Time of Read Data	TE	R	30 NS	
TDHR = Data Hold Time of Read Data	TE	R	0 NS	
TROZ = Time of Read Strobe to High Z	TE	R		2 TCYC **
TDQD = Time to DRQ Deasserted (to stop Burst)	LE	R		2 TCYC - 20 NS ***
TSDA = Time of Strobe Deactivated (See SDTC in Section 4.1)		S	2 TCYC - 15 NS	4 TCYC + 15 NS

* DRQ Polarity shown high true; DACK polarity shown low true.

** If SDTC in Section 4.1 is set, then value is 4 TCYC.

*** Based on SC and SDTC set to zero. Add 2 TCYC for each programmed state.

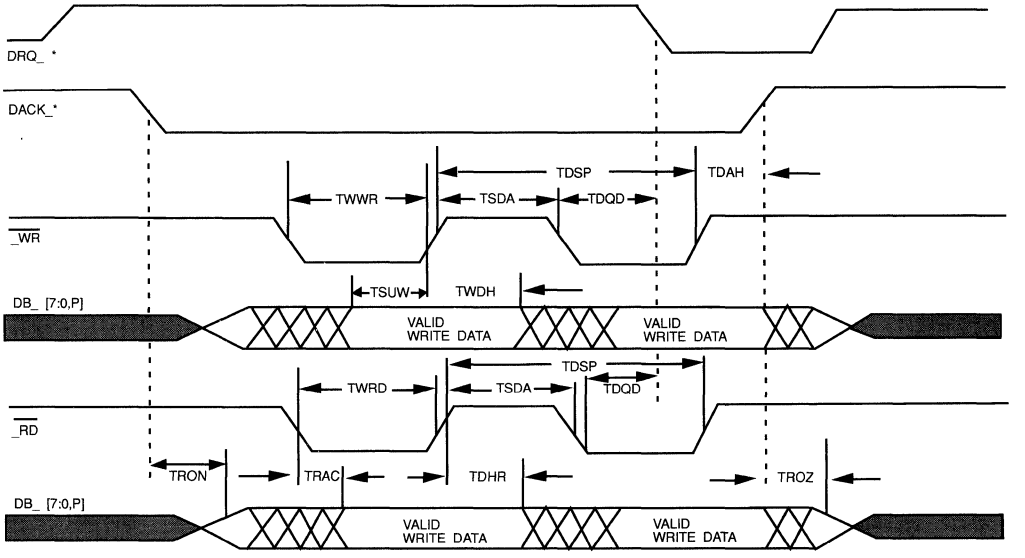
FIGURE 7. DMA SINGLE CYCLE MODE



NAME	REF	R/S	MINIMUM	MAXIMUM
TDAK = Time DRQ to Acknowledge	LE	S		35 NS
TDQD = Time to DRQ Deasserted	LE	R		3 TCYC
TRQP = Time of Request Period		R	6.5 TCYC	
TWDK = Width of DACK Signal		S	3.5 TCYC	5.5 TCYC + 15 NS
TSUW = Data Setup Time of Write Data	TE	S	2 TCYC - 40 NS	
TWDH = Data Hold Time of Write Data	TE	S	TCKH - 5 NS	
TSUR = Data Setup Time of Read Data	TE	R	30 NS	
TDHR = Data Hold Time of Read Data	TE	R	0 NS	

* DRQ polarity shown high true; DACK polarity shown low true
** If SDTC in Section 4.1 is set, then value is 4 TCYC
*** Based on SC and SDTC set to zero. Add 2 TCYC for each programmed state

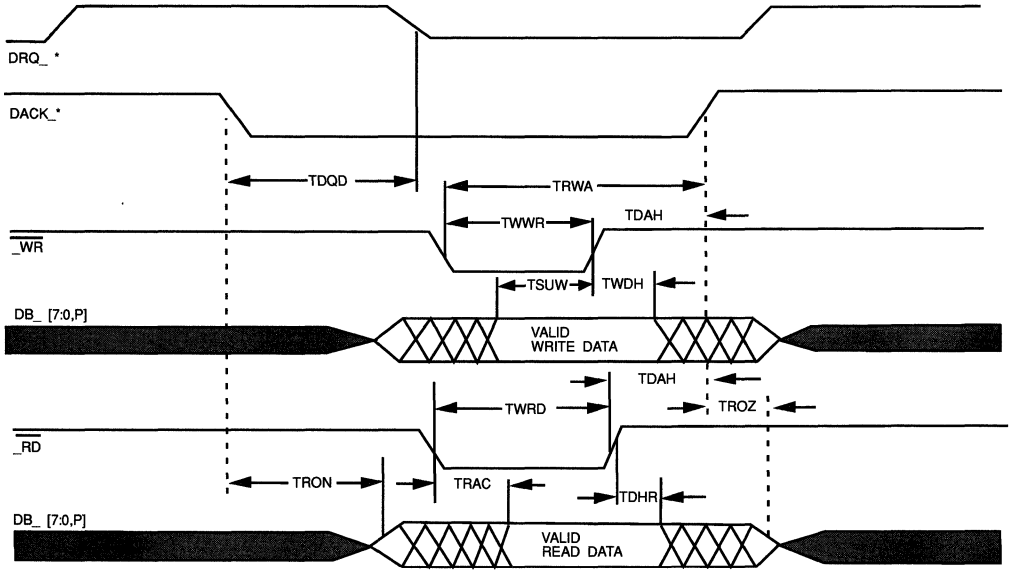
FIGURE 8. BUS MASTER DISK MODE



NAME	REF	R/S	MINIMUM	MAXIMUM
TWWR - Width of Write Strobe		R	50 NS	
TSDA = Time of Strobe Deactivated		R	50 NS	
TDQD = Time to DRQ Deasserted	LE	S		35 NS
TDSP = Time of Data Strobe Period		R	2.5 TCYC	
TDAH = Time of DACK Hold	TE	R	0 NS	
TSUW = Data Setup Time to Write	TE	R	20 NS	
TWDH = Time of Data Hold in Write	TE	R	10 NS	
TRON = Time Read Output Enable from DACK (If DIR bit is set)	LE	S	0 NS	50 NS
TWRD = Width of Read Strobe		R	50 NS	
TRAC = Data Access Time	LE	S		45 NS
TDHR = Data Hold Time of Read Data		S	10 NS	45 NS
TROZ = Time of Read Strobe to High Z		S		50 NS

* DRQ polarity shown high true; DACK polarity shown low true

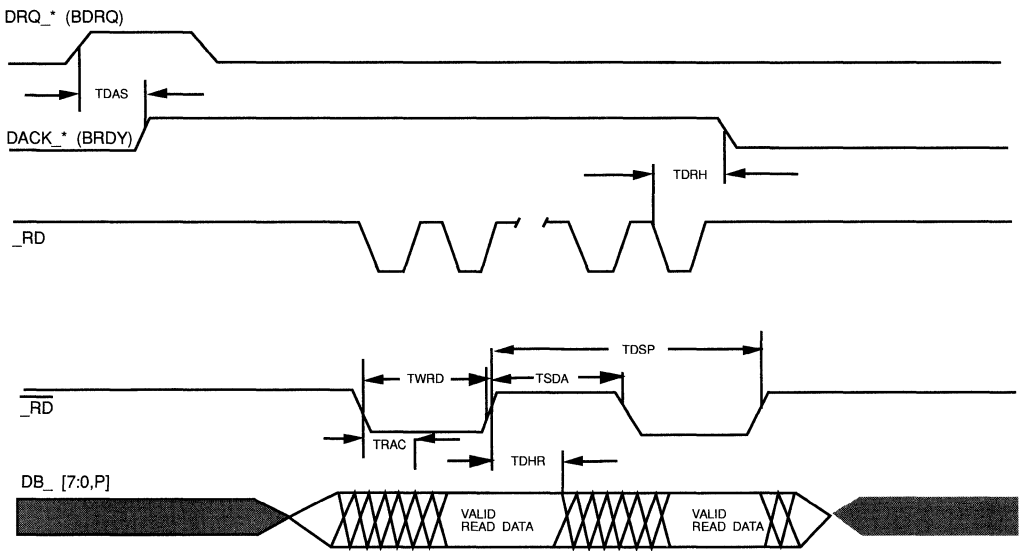
FIGURE 9. SLAVE BURST MODE TRANSFERS



NAME	REF	R/S	MINIMUM	MAXIMUM
TWWR - Width of Write Strobe		R	50 NS	
TDQD = Time to DRQ Deasserted	LE	S	1.5 TCYC	3.5 TCYC + 15 NS
TDAH = Time of DACK Hold	TE	R	0 NS	
TSUW = Data Setup Time to Write	TE	R	20 NS	
TWDH = Time of Data Hold in Write	TE	R	10 NS	
TRON = Time Read Output Enable from DACK (If DIR bit is set)	LE	S	0 NS	50 NS
TWRD = Width of Read Strobe		R	50 NS	
TRAC = Data Access Time	LE	S		45 NS
TDHR = Data Hold Time of Read Data	TE	S	10 NS	45 NS
TROZ = Time of Read Strobe to High Z	TE	S		50 NS
TRWA = Time of R/W to DACK Inactive	LE	S	2 TCYC + 15 NS	

* DRQ polarity shown high true; DACK polarity shown low true

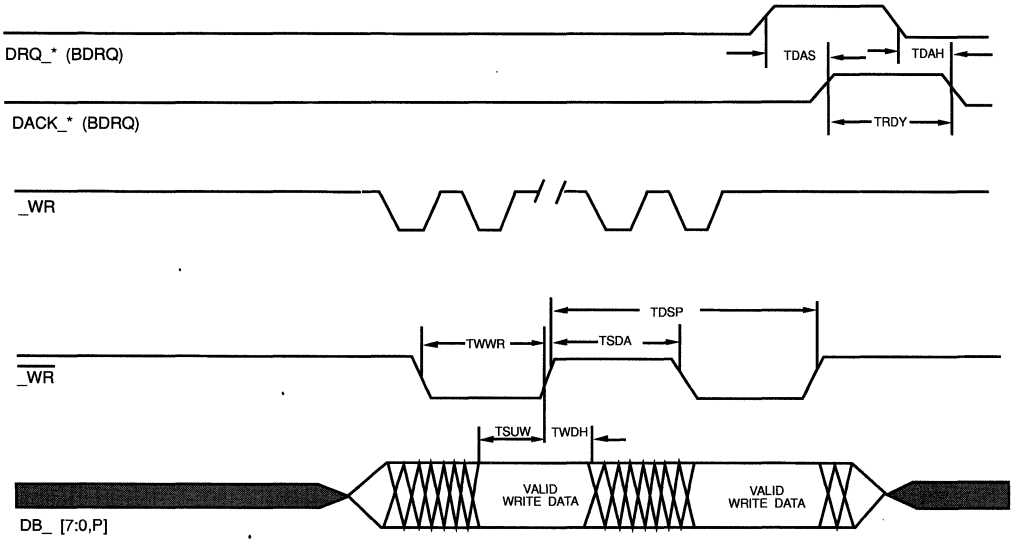
FIGURE 10. SLAVE SINGLE CYCLE TRANSFER



NAME	REF	R/S	MINIMUM	MAXIMUM
TDAS = Time of DACK Setup	LE	S	3.5 TCYC	5.5 TCYC + 15 NS
TSDA = Time of Strobe Deactivated		R	50 NS	
TDSP = Time of Data Strobe Period		R	2.5 TCYC	
TDAH = Time of DACK Hold	LE	S		6 TCYC
TRAC = Data Access Time	LE	S		45 NS
TDHR = Data Hold Time of Read Data	LE	S	10 NS	
TWRD = Width of Read STrobe		R	50 NS	

* DRQ polarity shown high true; DACK polarity shown low true

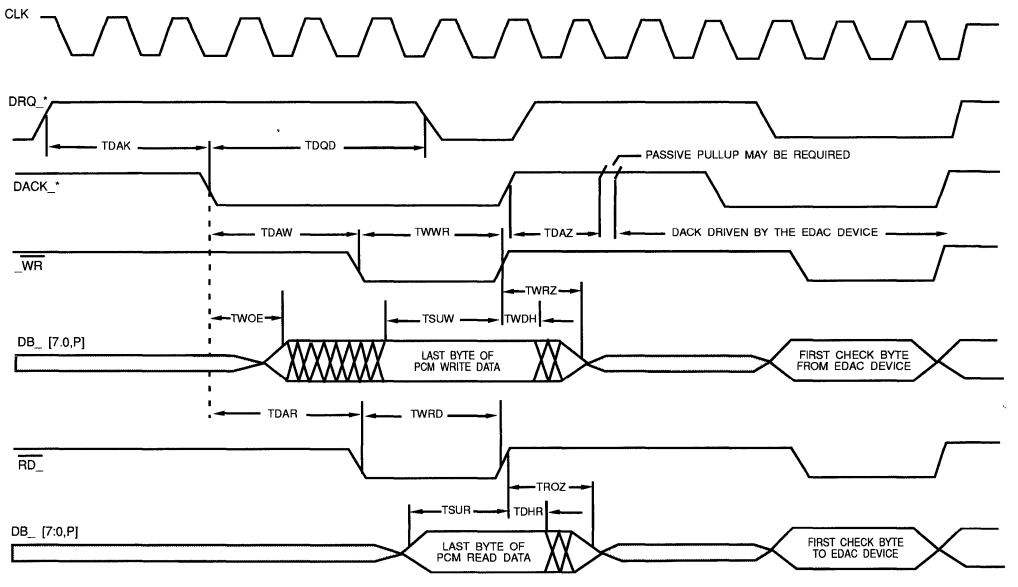
FIGURE 11. SLAVE BURST DISK MODE (READ)



NAME	REF	R/S	MINIMUM	MAXIMUM
TWWR = Width of Write Strobe		R	50 NS	
TSDA = Time of Strobe Deactivated		R	50 NS	
TDSP = Time of Data Strobe Period		R	2.5 TCYC	
TDAH = Time of DACK Hold	TE	R	2 TCYC	
TSUW = Data Setup Time to Write	TE	R	20 NS	
TWDH = Time of Data Hold in Write	TE	R	10 NS	
TRDY = Width of BRDY (DACK)		R	10 TCYC	
TDAS = Time of DACK Setup		S		6 TCYC

* DRQ polarity shown high true; DACK polarity shown low true

FIGURE 12. SLAVE BURST DISK MODE (WRITE)



NAME	REF	R/S	MINIMUM	MAXIMUM
TACS = Time of DACK to Chip Select	TE	S	2 TCYC - 15 NS **	
TCSA = Time of Chip Select to DACK	TE	S	2 TCYC - 15 NS **	
TDAW = Time DACK to Write Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWWR = Width of Write Strobe (See SC in Section 4.1)		S	2 TCYC - 15 NS	8 TCYC + 15 NS
TWOE = Time to Output Enable in Write	LE	S	0 NS	
TSUW = Data Setup Time to Write	TE	S	2 TCYC - 40 NS	8 TCYC + 15 NS
TWDH = Time of Data Hold in Write	TE	S	TCKH - 5 NS	
TWRZ = Time of Write Strobe to High Z	TE	S	TCKH - 5 NS	6.5 TCYC
TDAR = Time DACK to Read Strobe (See DLY in Section 4.1)	LE	S	2 TCYC - 15 NS	4 TCYC + 15 NS
TWRD = Width of Read Strobe (See SC in Section 4.1)		S	2 TCYC - 15 NS	8 TCYC + 15 NS
TSUR = Data Setup Time of Read Data	TE	R	30 NS	
TDHR = Data Hold Time of Read Data	TE	R	0 NS	
TROZ = Time of Read Strobe to High Z	TE	R		2 TCYC **
TDQD = Time to DRQ Deasserted (to stop Burst)	LE	R		2 TCYC - 20 NS ***
TSDA = Time of Strobe Deactivated (See SDTC in Section 4.1)		S	2 TCYC - 15 NS	4 TCYC + 15 NS
TDAZ = Time to Dack High Z	TE	S		6 TCYC

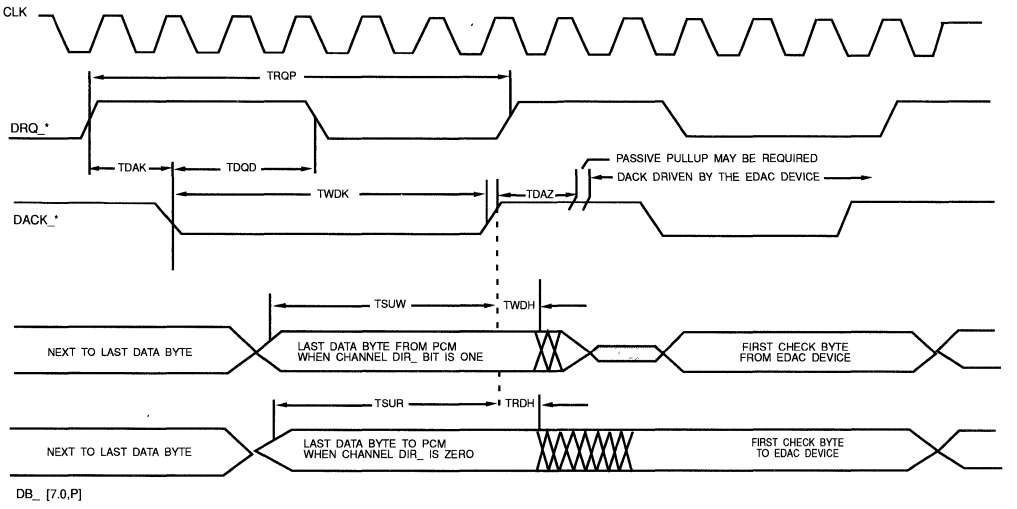
* DRQ Polarity shown high true; DACK polarity shown low true.

** If SDTC in Section 4.1 is set, then value is 4 TCYC.

*** Based on SC and SDTC set to zero. Add 2 TCYC for each programmed state.

FIGURE 13. EDAC MODE (DMA SINGLE CYCLE)

35



NAME	REF	R/S	MINIMUM	MAXIMUM
TDAK = Time DRQ to Acknowledge	LE	S		35 NS
TDQD = Time to DRQ Deasserted	LE	R		3 TCYC
TRQP = Time of Request Period		R	6.5 TCYC	
TWDK = Width of DACK Signal		S	3.5 TCYC	5.5 TCYC + 15 NS
TSUW = Data Setup Time of Write Data	TE	S	2 TCYC - 40 NS	
TWDH = Data Hold Time of Write Data	TE	S	TCKH - 5 NS	
TSUR = Data Setup Time of Read Data	TE	R	30 NS	
TDHR = Data Hold Time of Read Data	TE	R	0 NS	
TDAZ = Time to DACK High Z	TE	S		6 TCYC

* DRQ polarity shown high true; DACK polarity shown low true
** If SDTC in Section 4.1 is set, then value is 4 TCYC
*** Based on SC and SDTC set to zero. Add 2 TCYC for each programmed state

FIGURE 14. EDAC MODE (DMA DISK)

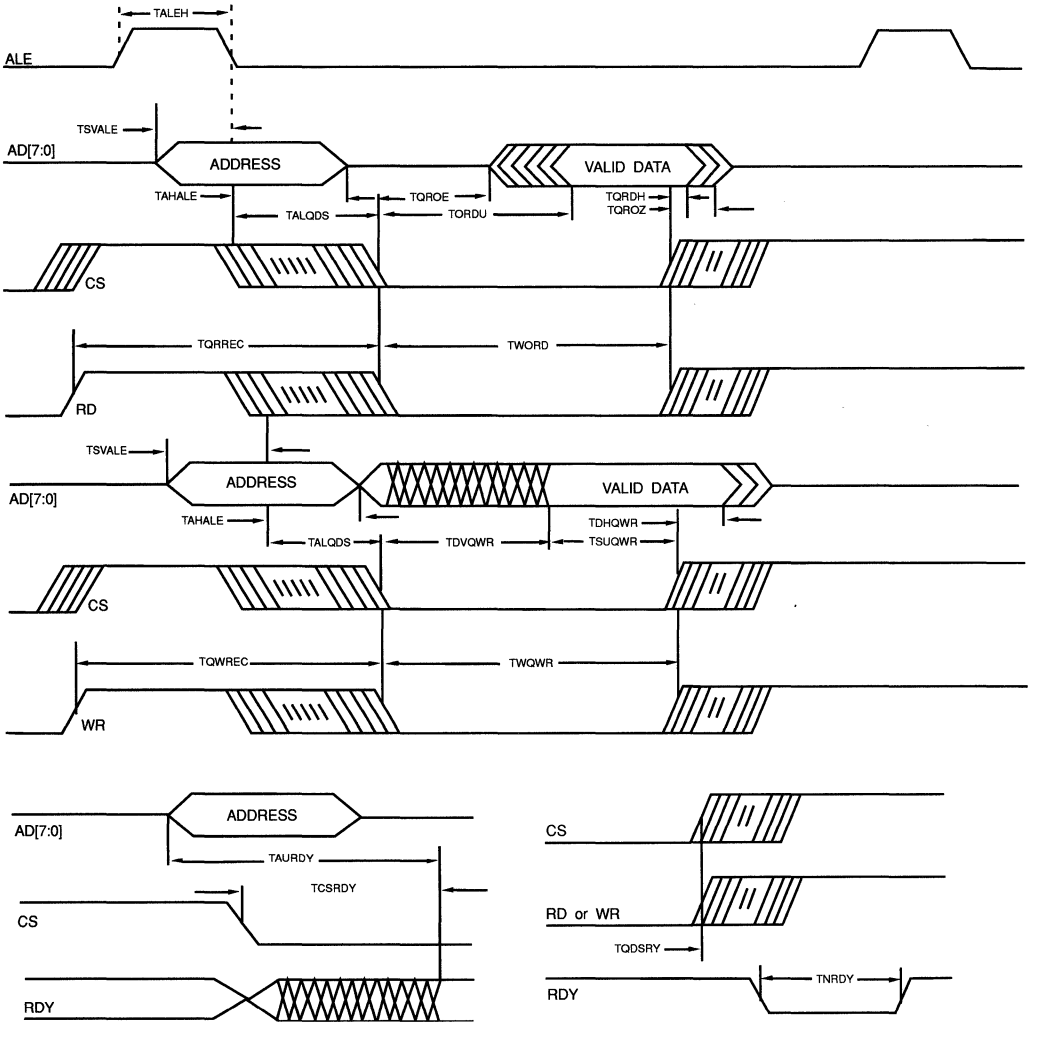


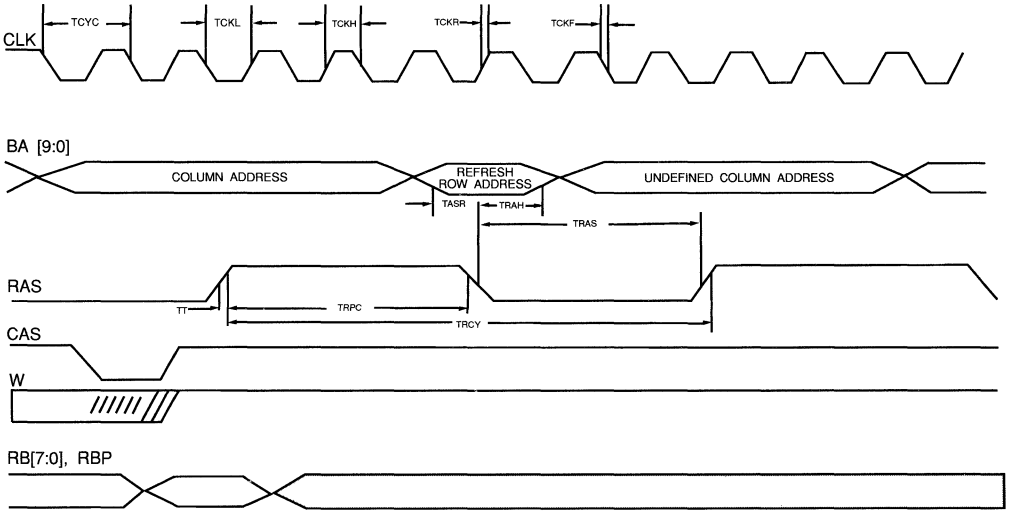
FIGURE 15. MICROPROCESSOR BUS TIMING

35

NAME	REF.	R/S	TIMING
TALEH = ALE High Pulse Width		R	35 NS MIN.
TSVALE = Address Setup Before T.E. ALE	TE	R	15 NS MIN.
TAHALE = Address Hold after T.E. ALE	TE	R	15 NS MIN.
TALQDS = ALE T.E. to Qualified Data Strobe	TE	R	30 NS MIN.
TWORD = Pulse Width Qualified Read Strobe		R	110 NS MIN.
TQROE = Qualified Read Strobe to Output Enabled	LE	S	40 NS MAX.
TQRDV = Qualified Read Strobe to Data Valid	LE	S	95 NS MAX.
TQRDH = Data Hold from Qualified Read Strobe	TE	S	0 NS MIN.
TQROZ = T.E. Qualified Read Strobe to High Impedance	TE	S	60 NS MAX.
TQRREC = Recovery Time after Qualified Read Strobe	TE	R	120 NS MIN.
TWQWR = Pulse Width Qualified Write Strobe		R	110 NS MIN.
TDVQWR = Data Valid from L.E. Qualified Write	*	R	3 CLK MAX.
TSUQWR = Data Setup to T.E. Qualified Write	TE	R	30 NS MIN.
TDHQWR = Data Hold from T.E. Qualified Write	TE	R	10 NS MIN.
TQWREC = Recovery Time after Qualified Write Strobe	TE	R	120 NS MIN.
Waitable Microprocessor Interface			
TAURDY = Address Valid to Ready Valid	LE	S	50 NS MAX.
TCSRDY = Chip Select to Readh Valid	LE	S	35 NS MAX.
Non-Waitable Microprocessor Interface			
TQDSRY = T.E. Qualified Data Strobe to Not Ready	TE	S	60 NS MAX.
Either Microprocessor Interface			
TNRDY = Time Not Ready	**	S	6 CLK MIN.

* Required in Waitable Mode Only
** See Section 5.0 for maximum

FIGURE 15. MICROPROCESSOR BUS TIMING, Continued



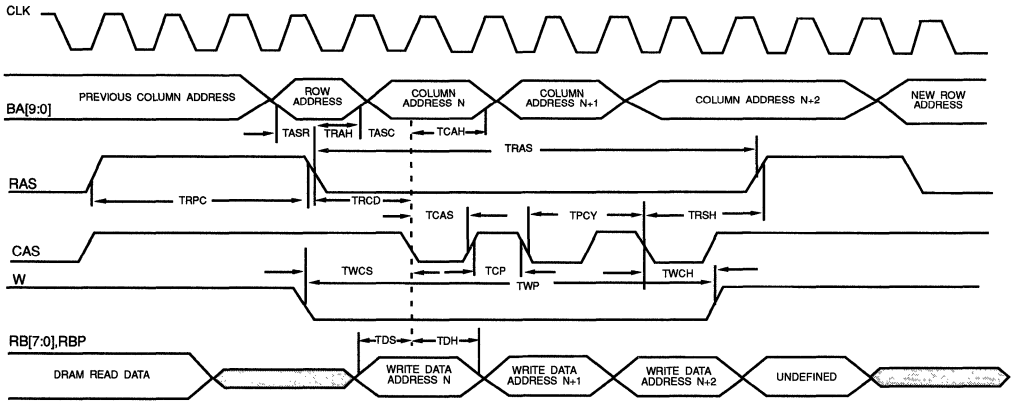
NAME	REF	R/S	MINIMUM	MAXIMUM
TCYC = Input CLock Period		R	40 NS	
TCKL = Input Clock Low		R	17 NS	
TCKH = Input Clock High		R	17 NS	
TCKR = Input Clock Rise		R		5 NS
TCKF = Input Clock Fall		R		5 NS
TRAS = Time of RAS Low		S	3.5 TCYC - 15 NS	
TRPC = Time of RAS Precharge (RAS High)		S	2.5 TCYC - 5 NS	TRFC
TASR = Address Setup to L.E. RAS	FE	S	TCYC - 20 NS	TCYC
TRAH = Address Hold from L.E. RAS	FE	S	TCYC - 15 NS	
TRCY = RAS Cycle Time		S	6 TCYC	TRFC **
TRFC = Refresh Cycle Time (Programmable)		S	32 TCYC	512 TCYC ***
TT = Transition Time All Outputs		S	3 NS	20 NS

** This specification assumes no other memory requests other than Refresh.

*** This is the maximum programmable value. The programmed value is based on DRAM specification.

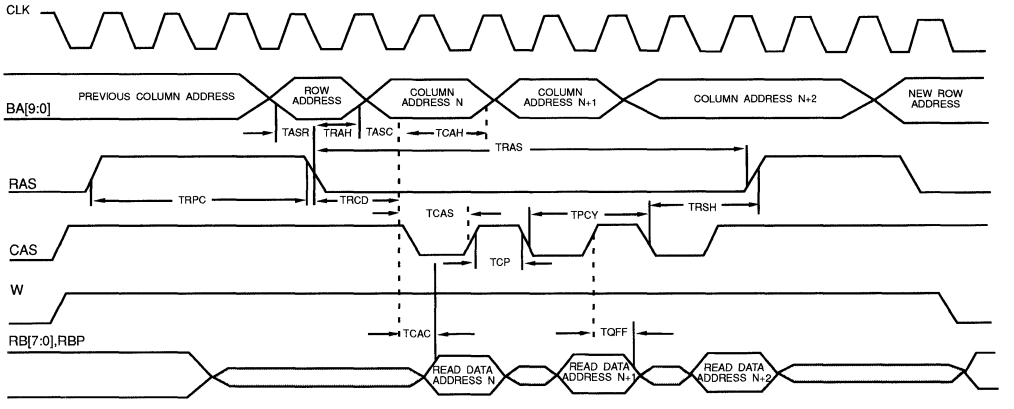
FIGURE 16. RAS ONLY REFRESH TIMING

35



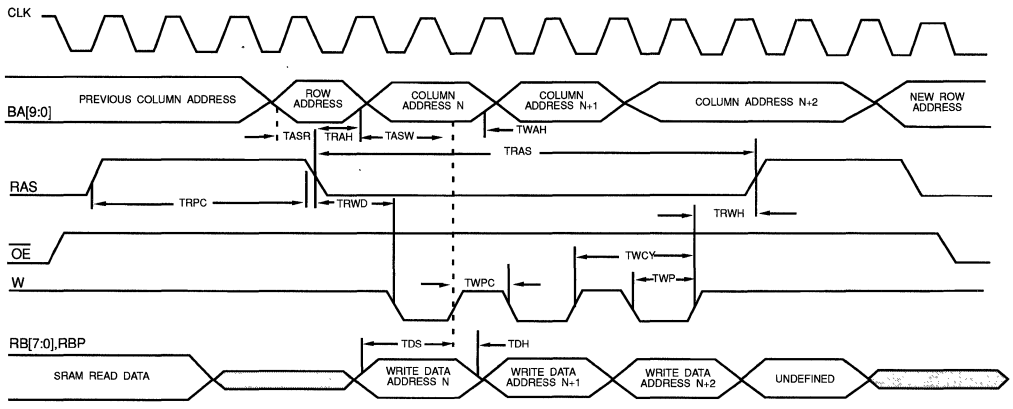
NAME	REF	R/S	MINIMUM	MAXIMUM
TRAS = Time of RAS Asserted		S	3.5 TCYC - 15 NS	
TRPC = Time of RAS Precharge (RAS High)		S	2.5 TCYC - 5 NS	TRFC
TASR = Address Setup to L.E. RAS	FE	S	TCYC - 20 NS	TCYC
TRAH = Address Hold from L.E. RAS	FE	S	TCYC - 15 NS	
TRCY = RAS Cycle Time		S	6 TCYC	
TT = Transition Time All Outputs		S	3 NS	20 NS
TRCD = L.E. RAS to L.E. CAS Delay	LE	S	2 TCYC - 25 NS	
TCAS = Time of CAS Asserted		S	TCYC	
TCP = Time of CAS Precharge (CAS High)		S	TCYC - 20 NS	
TWP = Time of Write Asserted		S	2 TCYC	
TASC = Address Setup to L.E. CAS	LE	S	TCKH - 15 NS	
TCAH = Address Hold from L.E. CAS	LE	S	1.5 TCYC - 15 NS	
TDS = Data Setup to L.E. CAS	LE	S	TCKH - 15 NS	
TDH = Data Hold from L.E. CAS	LE	S	1.5 TCYC - 15 NS	
TRSH = RAS Hold from L.E. CAS	LE	S	TCYC	
TWCS = Write Setup to L.E. CAS	LE	S	TCYC	
TWCH = Write Hold from L.E. CAS	LE	S	TCYC	

FIGURE 17. PAGE MODE WRITE TIMING



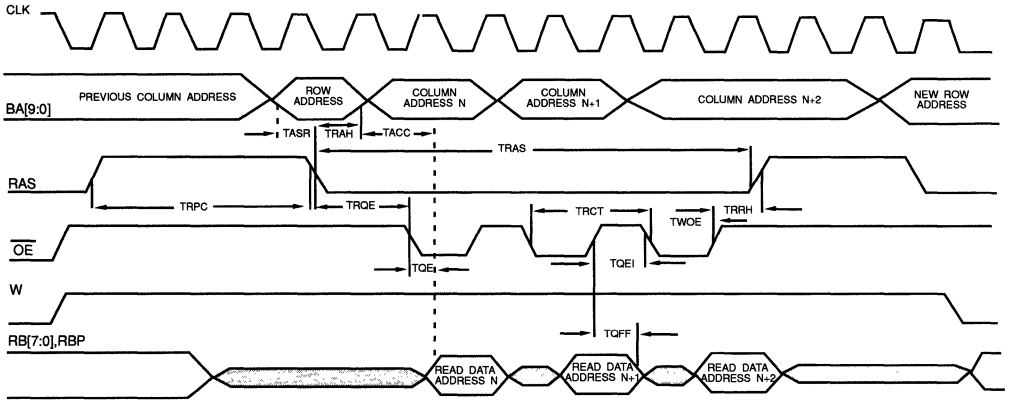
NAME	REF	R/S	MINIMUM	MAXIMUM
TRAS = Time of RAS Asserted		S	3.5 TCYC - 15 NS	
TRPC = Time of RAS Precharge (RAS High)		S	2.5 TCYC - 5 NS	TRFC
TASR = Address Setup to L.E. RAS	FE	S	TCYC - 20 NS	TCYC
TRAH = Address Hold from L.E. RAS	FE	S	TCYC - 15 NS	
TRCY = RAS Cycle Time		S	6 TCYC	
TT = Transition Time All Outputs		S	3 NS	20 NS
TRCD = L.E. RAS to L.E. CAS Delay	LE	S	1.5 TCYC - 5 NS	
TCAS = Time of CAS Asserted		S	TCYC	
TCP = Time of CAS Precharge (CAS High)		S	TCYC - 20 NS	
TASC = Address Setup to L.E. CAS	LE	S	TCKH - 15 NS	
TCAH = Address Hold from L.E. CAS	LE	S	1.5 TCYC - 15 NS	
TRSH = RAS Hold from L.E. CAS	LE	S	TCYC	
TCAC = CAS Access Time	LE	R		TCYC
TOFF = Data High-Z Delay	TE	R	0 NS	30 NS

FIGURE 18. PAGE MODE READ TIMING



NAME	REF	R/S	MINIMUM	MAXIMUM
TRAS = Time of RAS Asserted		S	3.5 TCYC - 15 NS	
TRPC = Time of RAS Precharge (RAS High)		S	2.5 TCYC - 5 NS	TRFC
TASR = Address Setup to L.E. RAS	FE	S	TCYC - 20 NS	TCYC
TRAH = Address Hold from L.E. RAS	FE	S	TCYC - 15 NS	
TRCY = RAS Cycle Time		S	6 TCYC	
TT = Transition Time All Outputs		S	3 NS	20 NS
TRWD = L.E. RAS to L.E. Write Delay	LE	S	2 TCYC - 25 NS	
TWCY = Write Cycle		S	2 TCYC	
TWPC = Time of Write Precharge (Write High)		S	TCYC - 20 NS	
TWP = Time of Write Asserted		S	TCYC	
TASW = Address Setup to T.E. Write	TE	S	1.5 TCYC - 15 NS	
TWAH = Address Hold from T.E. Write	TE	S	5 NS	
TDS = Data Setup to T.E. Write	TE	S	1.5 TCYC - 15 NS	
TDH = Data Hold from T.E. Write	TE	S	5 NS	
TRWH = RAS Hold Time from T.E. Write	TE	S	0 NS	

FIGURE 19. STATIC RAM WRITE TIMING



NAME	REF	R/S	MINIMUM	MAXIMUM
TRAS = Time of RAS Asserted		S	3.5 TCYC - 15 NS	
TRPC = Time of RAS Precharge (RAS High)		S	2.5 TCYC - 5 NS	TRFC
TASR = Address Setup to L.E. RAS	FE	S	TCYC - 20 NS	TCYC
TRAH = Address Hold from L.E. RAS	FE	S	TCYC - 15 NS	
TRCY = RAS Cycle Time		S	6 TCYC - 15 NS	
TT = Transition Time All Outputs		S	3 NS	20 NS
TROE	LE	S	2 TCYC - 25 NS	
TWOE		S	TCYC	
TOEI		S	TCYC - 20 NS	
TACC		R	TCYC	1.5 TCYC - 15 NS
TRRH	TE	S	0 NS	
TOE	LE	R		TCYC
TOFF	TE	R	0 NS	30 NS
TRCT		S	2 TCYC	

FIGURE 20. STATIC RAM READ TIMING

15.0 PACKAGE DIAGRAMS

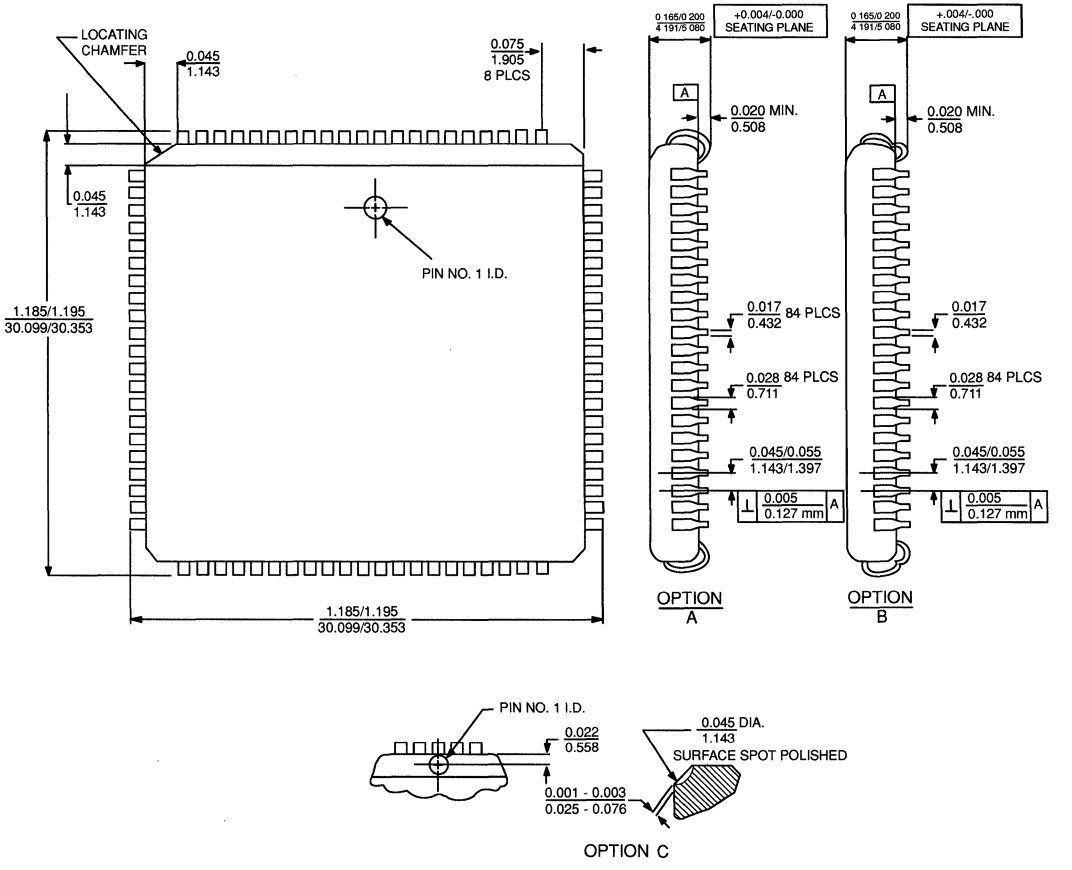


FIGURE 21. 84 LEAD PLCC

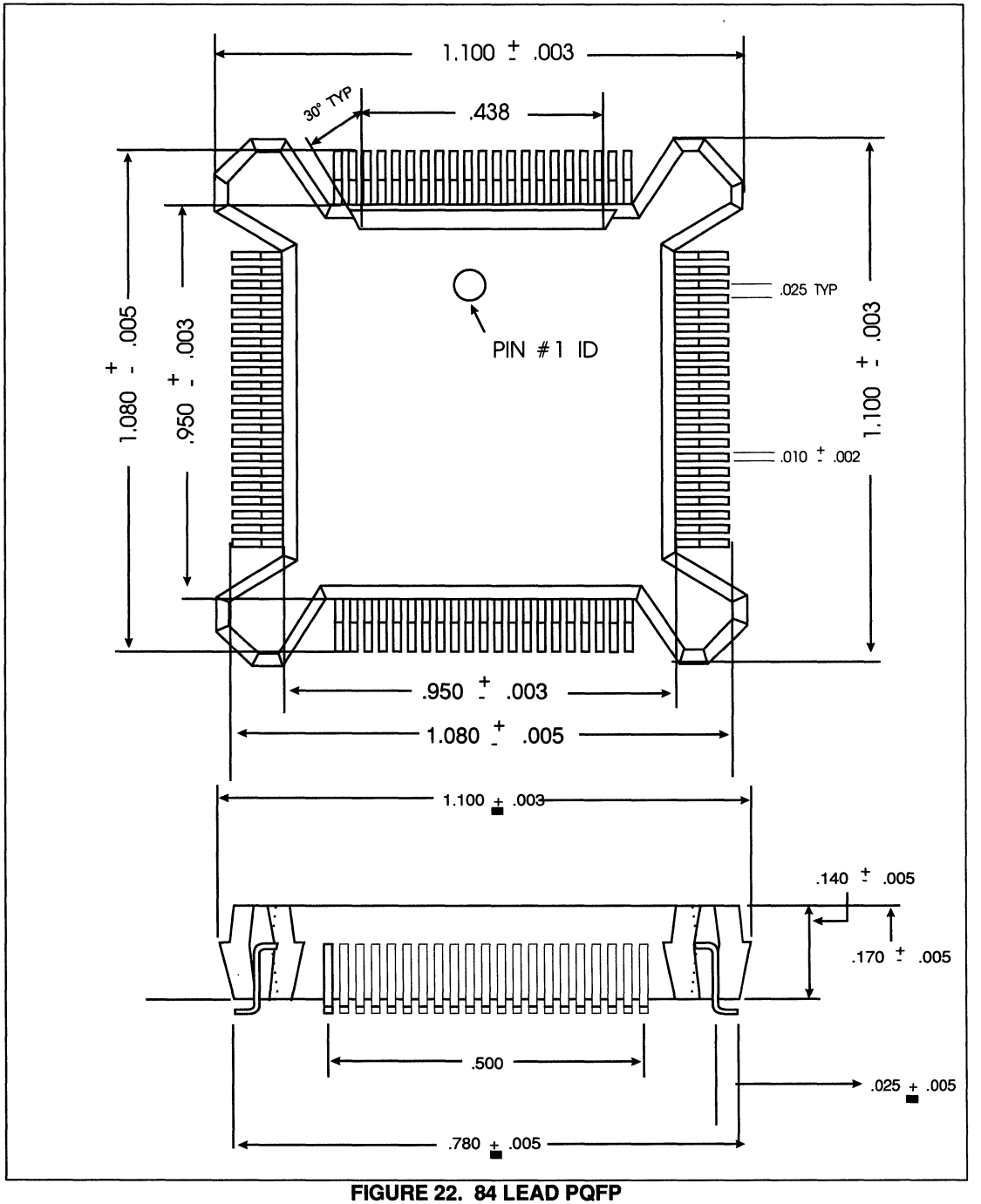


FIGURE 22. 84 LEAD PQFP

35

STORAGE

WD60C80

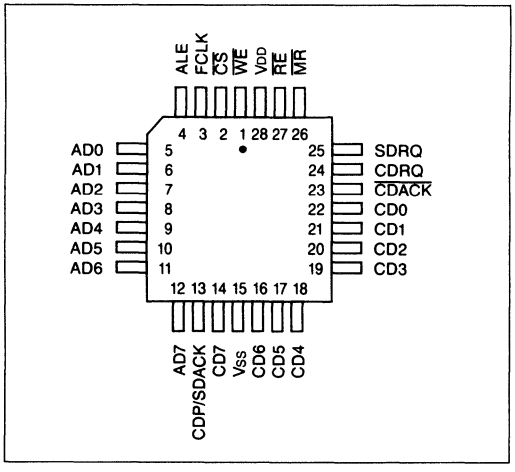
Error Detection and Correction Chip (EDAC)

WESTERN DIGITAL

WD60C80
Error Detection and Correction Chip (EDAC)

FEATURES

- High speed on-the-fly Reed-Solomon encoding and error detection up to 3 Mbyte/sec when clocked at 24 MHz. (Maximum clock frequency = 25.0 MHz)
  - —On-the-fly generation of check bytes and syndrome bytes. No latency associated with the code generation
  - —Programmable polynomial selections (degrees 4, 8, 16)
  - —Programmable interleave selections (1, 2, 3, 4, 5, 8, 10)
  - —Optional 4-byte GF(256) CRC
  - —Corrects up to 8-byte per interleave, or 80 bytes per sector
  - —Low redundancy overhead (7.8% for 1Kbyte sector, degree 16 and 5 interleaves, no CRC)
  - —Degree 16 and CRC polynomials are compatible with ANSI X3B11 standard
  - —Programmable sector size up to 2.5Kbyte (including data, CRC and ECC) in one-byte increments
  - —Write (ECC generation) and read (error detection) mode of operations
- Generates syndrome bytes compatible with the high-speed correction software algorithm licensed by Western Digital Corporation
  - —Zero latency delay for sectors with no error
  - —Supports correction of single byte error in 200 μsec using 8MHz 80188 microprocessor
- Fully independent processor port, allowing taskfile access at any time at all, independent of controller bus activity
  - —Full complement of programmable options and status information
  - —Status bytes with interleave-in-error number
  - —Supports simultaneous redundancy read/syndrome output transfers
- The internal 4-byte data path FIFO to capture data streams up to 1/5 the clock frequency (5.0 Mbyte/sec max.) without handshaking
  - —Optionally supports the parity bit on the controller bus
- The internal 20-byte syndrome FIFO to support continuous back-to-back transfer with minimal gap length
  - —Supports DMA or programmed I/O up to 1/5 the clock frequency (5.0 Mbyte/sec max.)
  - —Syndrome bytes can be directed to the controller bus to support single RAM application
- Low cost single chip Error Detection and Correction
- Protocol compatible with the WD60C40 PCM and WD10C00 Disk SerDes
- Using Hyperbolic Drivers™ to suppress power/ground transient noise
- Single +5V supply
- 28 pin PLCC package
- Implemented in 1¼ μm dual metal CMOS technology



WD60C80
DEVICE PINOUT

36

PIN DESCRIPTIONS

PIN	SYMBOL	PIN NAME	DESCRIPTION
1	$\overline{WE}$	Write Enable	TTL Input, Low Active; ANDed with $\overline{CS}$, it controls the Taskfile write operation by the processor.
2	$\overline{CS}$	Chip Select	TTL Input, Low Active; Controls the Taskfile access by the processor. The pin must be set high during the reset.
3	FCLK	Fast Clock	TTL Input; The primary clock input. f $\leq$25 MHz. The frequency must be greater than or equal to the nominal bit transfer rate for the application.
4	ALE	Address Latch Enable	TTL Input, High Active; The high level latches the multiplexed address vector on AD1-AD3 pins to the internal address register to control the Taskfile access.
5-12	AD0-AD7	Processor Data Bus	TTL Bidirectional, True Level; Multiplexed data/address bus used by the processor to access the internal Taskfile Registers and Syndrome transfer.
13	CDP/SDACK		TTL Bidirectional; Dual-Function Pin.
	CDP	CD bus Parity	TTL Bidirectional, True level; The parity bit input/output for the CD bus.
	SDACK	Syndrome DMA Acknowledge	TTL Input; Active Level Programmable. The external DMA controller indicating that the DMA cycle is granted.
14-22	CD0-CD7	Controller Data Bus	TTL Bidirectional, True Level; (Less Pin 15) Data, CRC, ECC bytes are transferred to/from the target disk controller via this bus. An option exists to use this bus for the Syndrome transfer.
15	VSS	Logic/Power Ground	
23	$\overline{CDACK}$	Controller Bus DMA Acknowledge	TTL Bidirectional, Low Active; During the data read phase, WD60C80 reads the data on CD bus while this signal (input) is active. During the redundancy read/write phases WD60C80 inputs/outputs the CRC/check bytes while this signal (output) is active.
24	CDRQ	Controller Bus DMA Request	TTL Input, High Active; DMA Request from the target disk controller. It is sampled and used for $\overline{REQ}$ ACK protocol between the WD60C80 and the controller/buffer manager during the redundancy read/ write phase of the operation.
25	SDRQ	Syndrome DMA Request	TTL Output, High Active; Indicates to the external DMA controller that syndrome bytes are ready to be transferred.
26	$\overline{MR}$	Master Reset	TTL Input, Low Active; Initializes the chip to the power-on default condition.
27	$\overline{RE}$	Read Enable	TTL Input, Low Active; ANDed with $\overline{CS}$, it controls the Taskfile read operation by the processor.
28	VDD	Power Supply	+5 V $\pm$ 10%

DESCRIPTION

The WD60C80 Error Detection And Correction (EDAC) device is a high-speed, CMOS LSI, designed to provide high power Reed-Solomon error correction code support for the applications where data integrity is critical for optical or magnetic disk drives, tape drives and communication links.

INTRODUCTION

The WD60C80 Error Detection And Correction (EDAC) device is a high-speed CMOS LSI designed to provide high power Reed-Solomon error correction code support for the applications where data integrity is critical.

The WD60C80 generates the Reed-Solomon code with the coefficients from GF(256) with the generator polynomials of degree four, eight or 16. It also generates 4-bytes GF(256) CRC code in order to (a) detect mis-corrections and (b) support extended correction to correct up to 16 bytes of error per interleave (depending on the polynomial degree chosen). The degree 16 polynomial and the CRC are the standard adopted by ANSI X3B11 committee to be used for optical disk storage.

Using degree 16 polynomials and 10 interleaves (interleave factors are programmable between one to 10 in seven steps), the WD60C80 can correct up to 80 bytes per sector of data with only 160 bytes of ECC overhead (164 if CRC is used).

The WD60C80 can be used to (a) generate ECC bytes (hereafter referred to as "check bytes" or "redundancies", interchangeably) by reading in the data field, or (b) generate the syndrome by reading the potentially erred data field and redundancies. The external processor needs to perform the actual data correction using the syndrome bytes. The software support is available from Western Digital Corporation.

The WD60C80 can be clocked as high as 25.0 MHz, and has the maximum byte/sec throughput of 1/8 the clock frequency. If this minimum clock frequency requirement is met, it can synchronize itself to the data flow and performs its function properly. Therefore, if an application calls for multiple data rates, this device can handle it without having its clock switched.

The WD60C80 can support the average data rate of up to three Mbyte/sec when clocked at 24 MHz, with the short burst (four bytes of less) of up to 4.8 Mbyte/sec. The code is generated on-the-fly at the data rate. It supports the sector size (including the check bytes and CRC) up to 2,550 bytes in one byte increment. Syndrome bytes can be transferred at the maximum speed of 4.8 Mbyte/sec when clocked at 24 MHz, and the internal 20-byte syndrome FIFO allows continuous back-to-back transfer of sectors with minimal inter-sector gap lengths.

In order to support the high data rate reliably, it employs the proprietary Hyperbolic Driver to suppress power/ground transient noise. The ground level transient noise is kept to less than 400 mV at all times.

The WD60C80 is applicable to all areas where error correction is important to maintain high data throughput and integrity such as controllers for optical or magnetic disk drives, tape drives and communication links.

The device is implemented using 1¼ μm double metal CMOS process, and packaged in a 28-pin PLCC. It requires a single + 5.0 Volt $\pm$ 10% supply and rated at the full specification in the temperature range of 0°C to 70°C.

ARCHITECTURE

The WD60C80 has two operation modes;
a) Read mode and
b) Write mode.

In read mode, it reads a full block of data and redundancies. The acquired data may contain errors, so it generates the redundancy code internally, and compares them with the acquired redundancies to generate syndrome bytes. These syndrome bytes, equal in number to the redundancy bytes, are transferred to the external processor, who will process the information and actually perform the error correction.

In write mode, the WD60C80 reads just the data bytes, generates redundancies, and appends them to the end of the data byte flow. This formatting function is performed on the bus by arbitrating between the WD60C80 and the external buffer manager.

The WD60C80 relies on an external processor to setup the desired configuration or to recover from operational failure by reading or writing the internal taskfile registers, there is a seperate 8-bit port for that purpose. This port can be accessed at any time regardless of the activity of the data/redundancy generator.

In order to perform the above functions, the WD60C80 has three distinctive interfaces.

a) The processor interface (ALE, $\overline{CS}$, $\overline{WE}$, $\overline{RE}$ pins)
b) The controller interface (CDRQ, $\overline{CDACK}$ pins)
c) The syndrome transfer interface (SDRQ, SDACK pins).

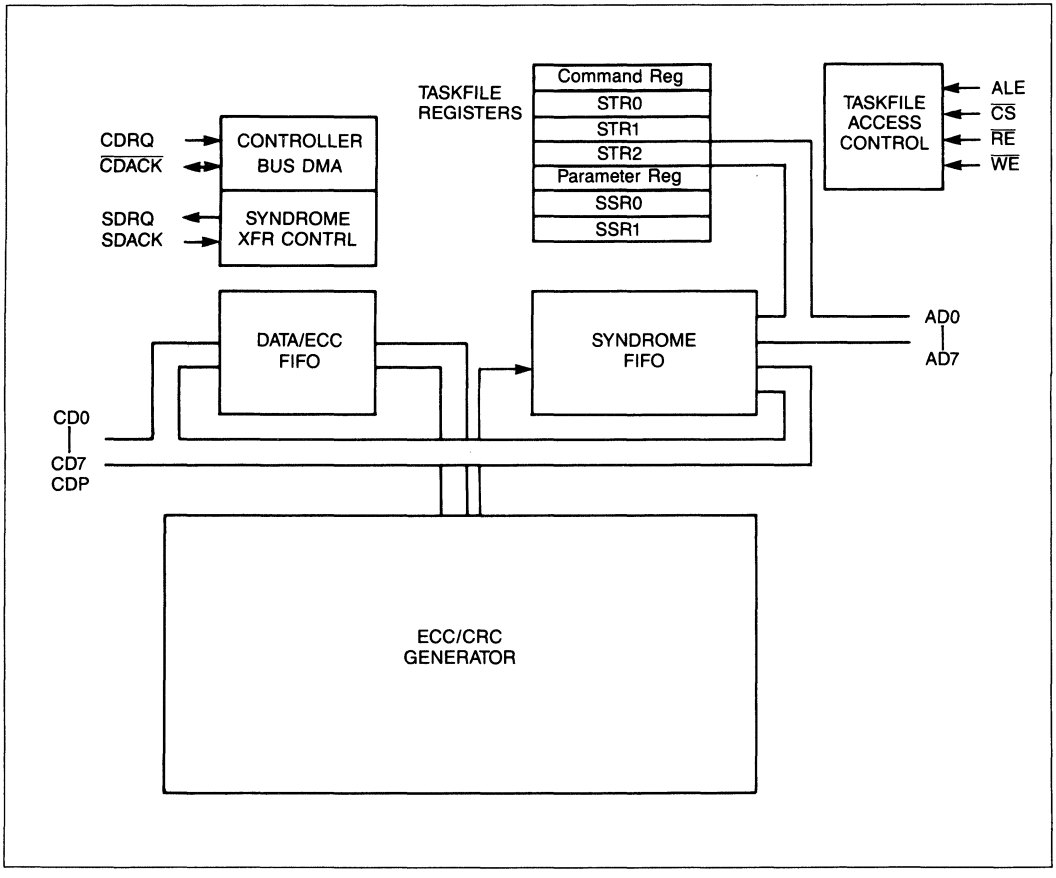
The controller bus and syndrome transfer interfaces are simple REQ-ACK protocol of a regular DMA controller. It has two physical ports or busses, eight bits wide each.

a) The processor bus (designated ADx in the pin description)
b) The controller bus (designated CDx in the pin description).

The controller interface works exclusively on the controller bus, (designated as CDx in the pin-out description) handling the target (e.g., disk controller) data reads and writes, while the processor interface works exclusively for the processor bus, and used to access the internal taskfile registers. The syndrome transfer interface works on either the processor bus or the controller bus, depending on the chosen option, to transfer syndrome/status bytes during the read operation.

The controller bus has an optional ninth bit, which is used as the parity bit for higher data integrity. The WD60C80 can generate and check for odd parity on each byte read/written. It is activated by properly setting the Parameter Register.

Because the device is packaged in a 28-pin PLCC, two pin functions are multiplexed on one physical pin and hence not available at the same time. If the parity generation/checking is to be supported on the controller bus, the DMA mode syndrome transfer must be given up, since SDACK (Syndrome DMA Acknowledge) and CDP (Controller Bus Parity bit) are assigned the same pin. This pin can be only programmed to function as one of the two. Some DMA devices (most ones with memory to memory transfer capability) and integrated processors (such as Intel™ i80188/86) have their DMA function implemented like a programmed I/O (i.e., generates Address and $\overline{RE}$ or $\overline{WE}$, rather than issuing a DMA $\overline{Acknowledge}$), which allows for syndrome DMA transfer and parity checking at the same time.



WD60C80 SIMPLIFIED BLOCK DIAGRAM

Data/ECC FIFO is bidirectional, allowing the data and ECC/CRC bytes to pass through in the appropriate directions. It is four-byte deep, and has special control logic that lets a data byte pass through right into the ECC and CRC generator if the FIFO is empty, in order to improve the overall throughput.

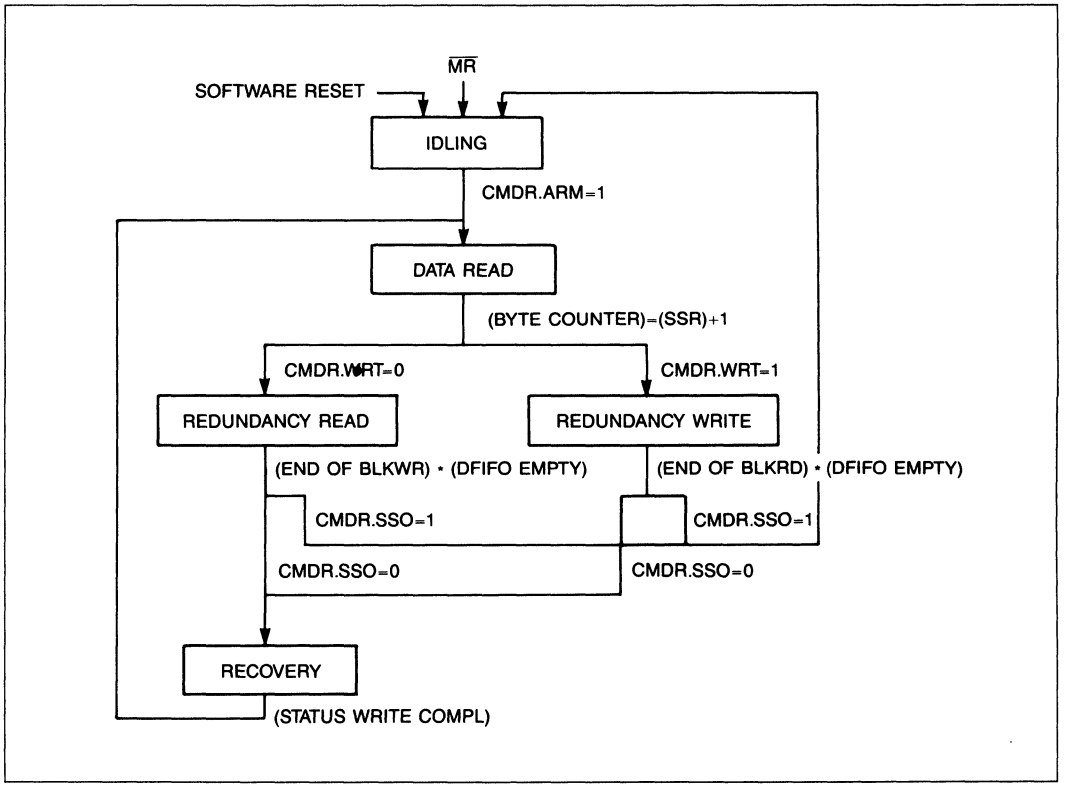
Syndrome FIFO is unidirectional (read-only) FIFO used to smooth the transfer of CRC residue, syndrome and status bytes. Its output can be directed to either the controller bus or the processor bus.

There are seven taskfile registers on the processor bus. They can be read/written at any time, independent of the controller bus activity, allowing the external processor to interact with the device without any special protocol.

Control Sequences

The WD60C80 has five independent states as listed below:

1) Idling	WD60C80 is completely dormant.
2) Data Read	WD60C80 reads data bytes from the CDbus.
3) Redundancy Write	WD60C80 writes ECC/CRC to the CDbus.
4) Redundancy Read	WD60C80 reads ECC/CRC from the CDbus.
5) Recovery	End of a block and reinitialize for the next.



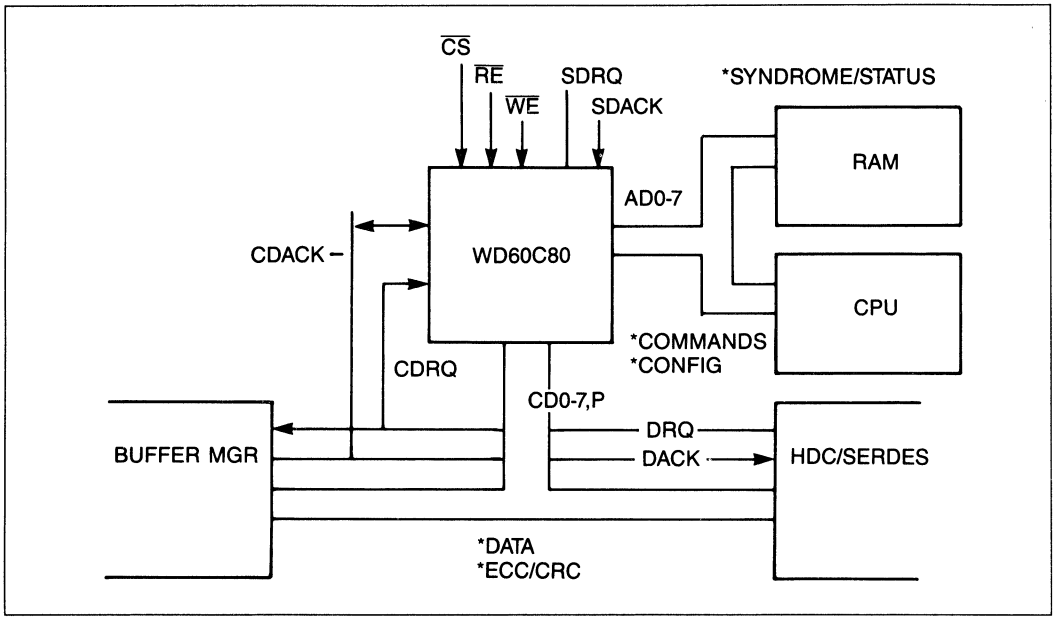
WD60C80 BASIC CONTROL FLOW DIAGRAM

(END OF BLKWR) = All ECC/CRC bytes written out to the data/ECC FIFO.
(END OF BLKRD) = All ECC/CRC bytes processed and the last syndrome byte is output to the syndrome FIFO.
(STATUS WRITE COMPL) = The final status bytes written to the syndrome FIFO.

The operational details and the hardware protocol on the bus transactions on each state are described in the following sections.

Basic Topology

The WD60C80 is designed to be placed between a buffer manager and a target peripheral device (e.g., disk serdes). It is assumed that the buffer manager and the target will transfer the data bytes using REQ-ACK protocol. The buffer manager is normally the DMA master, with the target peripheral being the permanent slave.



WD60C80 BASIC TOPOLOGY

The WD60C80 listens to the CD bus and (when ARMed), picks up a byte every time $\overline{\text{CDACK}}$ pulses, as a valid data byte. When all data bytes are read and processed, the WD60C80 becomes a temporary bus master (i.e., it performs the REQ-ACK protocol with the target peripheral device) and transfers the ECC and CRC bytes. Unless it is used with a buffer manager device such as the WD60C40 that has a special arbitration mode with WD60C80, some external support logic is required between the buffer manager DMA and the WD60C80 to give this device the control of the bus during Redundancy Read/Write phases.

During the Redundancy Read phase, the WD60C80 generates syndrome bytes equal in number with the ECC bytes. They are output through (by default,) the processor bus to the CPU memory. It performs the REQ-ACK protocol with the external DMA controller (in DMA mode) as a slave device. Optionally, the syndrome bytes can be output through the controller bus, though due to the external bus arbitration overhead, the throughput of the transfer will be much lower in this case.

Controller Bus Interface

The "Controller Bus" refers to the CD0 through CD7 pins plus the optional CDP pin which is multiplexed with SDACK function. They are used to connect the WD60C80 to the bus between the buffer manager device and the target peripheral controller device. Depending on the option chosen, it can also be a port to transfer the syndrome/status bytes during the READ operation. This bus behaves in three different manners depending on the state the device is in.

Data Read Phase

The data read phase (state) is entered when the ARM bit of the command register is set high. The WD60C80 CD bus behaves passively in this mode, with all the CDx pins and the $\overline{\text{CDACK}}$ pin being inputs. CDRQ pin is inactive in this phase. When the $\overline{\text{CDACK}}$ signal (issued by the buffer manager) becomes active (low), the WD60C80 grabs the data byte on the CD0 through CD7 pins and stores it into the internal FIFO. Care should be taken that it does not necessarily get the data byte at the trailing edge of the $\overline{\text{CDACK}}$ pulse, but can actually gets it anytime after four clock cycles after the leading edge of the pulse.

This is done to speed up the internal processing of the data, to shrink the blank time between the Data Read Phase and the Redundancy Write Phase. Also it should be noted that the $\overline{CDACK}$ pulse needs to be wider than 2.0 clock cycles to insure a proper read.

The average transfer cycle on the controller bus during this phase should not exceed one eighth of the WD60C80 clock frequency, which is the rate at which the device processes a byte. But in order to be more flexible, the transfer cycles can proceed at the maximum rate of one fifth the clock frequency (e.g., at 25.0 MHz clocking, up to 5 Mbyte/sec) for a short span, up to about 10 bytes in length. A longer burst than that can result in a data FIFO overflow.

If the average data rate is slower than one eighth the clock frequency, then the WD60C80 will slow down automatically and synchronize itself to the bus transaction. Therefore, there is no need to tweak the clock frequency of the device to match any special data rate, as long as the frequency is high enough.

Redundancy Write Phase

The WD60C80 enters the Redundancy Write Phase (State) if the WRITE operation is chosen in the command register, and the prescribed number of bytes (in the sector size register) are read from the controller bus and finished processing inside the ECC generator.

In this phase, the WD60C80 performs REQ-ACK protocol with the target peripheral device, outputting the generated ECC and CRC bytes to the controller bus. The $\overline{CDACK}$ pin as well as all the CDx pins become outputs, and CDRQ input gets activated, the WD60C80 becoming the temporary bus master. Unless it is used with a buffer manager like the WD60C40 which knows when to release the bus, some external support logic is necessary between the buffer manager and the WD60C80, isolating the buffer manager from the DMA protocol to transfer the ECC/CRC bytes. In particular, the DACK output of the buffer DMA device must be tri-stated.

Notice when the WD60C80 shifts from the Data Read Phase to the Redundancy Write Phase, there is more than a "Byte Time (eight clock cycles)" before the first ECC/CRC byte can be output after the last data byte is loaded. The worst case latency of 12 clock cycles if the data FIFO is empty prior to receiving the last data byte; the best case is ten clock cycles.

Some target devices such as a disk serdes cannot tolerate the data transfer latency longer than one byte time, so some extra support logic between the WD60C80 and the target controller device is necessary to support those devices. A few examples for this logic are:

1) Place a data holding register or FIFO in front of the target device so that the controller won't run out of data before the WD60C80 can output the first ECC/CRC bytes. This register should be bidirectional, for dealing with the Read operation.
2) Set the WD60C80's clock frequency high enough so that the worst case switch-over time is narrower than the "one byte time" of the target controller device. This method is applicable if the required data rate is significantly less than the specified maximum clock frequency of the WD60C80.

After the WD60C80 takes over the bus, it transfers the ECC/CRC bytes pretty much at the target data rate (eight clock cycles/byte, if FCLK frequency is matched to the target data rate). If it is requested and there are a few bytes accumulated in the data FIFO, then it can transfer as fast as six clock cycles/byte.

Notice it does not cause a FIFO overflow, if the CDRQ pin is held inactive (low) for an extended period of time. The WD60C80 will stop generating redundancies when the FIFO is full.

When all the ECC bytes are generated and the data FIFO becomes empty (i.e., all of them are transferred to the target device), then the WD60C80 changes its state to the Recovery Phase. The $\overline{CDACK}$ pin becomes an input again, and the final status information is output to the Syndrome FIFO, where the processor can read it.

The WD60C80 changes its state to either the Data Read Phase for the next block if the Multiple Sector Operation is selected, or to the Idling Phase if the Single Sector Operation is selected.

Redundancy Read Phase

The WD60C80 enters Redundancy Read Phase (State) if READ operation is chosen in the command register and the last data byte is input through the controller bus, then processed internally.

Similar to the Redundancy Write Phase, it performs REQ-ACK protocol with the target controller device as a temporary bus master, but to read CRC/ECC the part of the block. Same restrictions and support logic requirements apply as the Redundancy Write case. Notice at the end of the block, it takes longer to get ready for the next block in the READ operation than the WRITE operation, because the data/ECC FIFO may become full when the last ECC byte is read from the controller bus, due to the read-ahead feature on this device. If the transfer is taking place at the WD60C80 data rate or less, and therefore not utilizing the read-ahead feature, then it should take just as long as the WRITE mode operation to get back to the Data Read Phase of the next block (Multiple Sector Operation).

If extra CDRQs are generated by the target controller at the end of the block, the WD60C80 will generate spurious $\overline{CDACK}$ pulse and loads whatever is on

the CD bus at the time. Since the internal state machine knows how many ECC bytes it should process, it will not fetch these spurious bytes from the FIFO. This prevents the FIFO from becoming empty, and consequently, prevents the WD60C80 from going into Recovery Phase. This can cause a system hang-up, so care should be taken.

When the Syndrome-on-the-Controller-Bus option is selected, the syndrome output also takes place on this bus, physically. The transfer is controlled by the SDRQ pin (output) and SDACK pin (input), and the bus arbitration between the two channels of the DMA is expected to be done external to this device. When two transfers collide on the bus, neither transfer takes place and consequently, both transfers are broken. This is an option meant for a low cost application where data buffer and the syndrome information share the same physical RAM, and it is not expected to be used for high throughput applications, where a large overhead associated with the DMA arbitration cannot be tolerated.

Processor Bus Interface

The processor bus refers to the AD0 through AD7 pins controlled by ALE, $\overline{CS}$, $\overline{RE}$ and $\overline{WE}$ pins. Depending on the options, the SDRQ and SDACK pins also control this bus. This bus is used primarily by the external processor to setup the operation modes/configurations of the WD60C80 as well as reading the operational/error status of the device. It is also used as the port to transfer syndrome/status bytes during the READ operation, by default.

Internal Register Interface

The internal taskfile read/write interface is native to the Intel 8085, 80186, 80188 and 8051 series of processors. Other processors with multiplexed address/data bus can be readily supported, but some external logic is needed to support processors with non-multiplexed bus.

In order to ease the interfacing to the 16-bit processors, some of which insist on even or odd boundaries for byte accesses, all internal registers of the WD60C80 are mirrored on even and odd addresses.

The processor can read any register at any time, without disturbing the internal operation. Before writing to any of these registers, however, it is suggested to soft reset the device (set the RST bit on the command register). If any options or configurations are changed while the device is active, it can disrupt the current operation, and in the worst case, it can hang up (The soft reset is effective even in the case of hang up). Consequently, it is suggested that all setups are made before the command register is written with the ARM bit set active.

When the Syndrome FIFO is read by the processor, care should be taken that the $\overline{CS}$ $\overline{RE}$ signal is wider than 2.0 clock cycles of the WD60C80, or it can upset the internal FIFO pointers. This situation is usually detected by the Syndrome/Status stream that is longer than expected. Because the pointer information cannot be accessed from the outside of the device, it is not possible to detect when the error happened, leading to a possible miscorrection.

Syndrome/Status Transfer

When the WD60C80 is operating in the READ mode, it generates syndrome bytes as it reads ECC bytes from the target controller device through the controller bus. They can be read using either PIO (programmed I/O) mode access, where the access is made just like another register read, or DMA mode, where the SDRQ pin and the SDACK pin are used to perform REQ-ACK protocol.

Code Description and Performance

The WD60C80 implements Reed Solomon error correcting code of degree 16, distance 17, long distance code. There are 16 redundancy (ECC) bytes generated per interleave, and it is capable of correcting up to eight symbol (byte) errors per interleave in any combinations of random and burst errors. This polynomial is compatible with the ANSI X3B11 error detection and correction encoding standard for 5¼ inch optical storage devices.

The 32-bit CRC code covered by the same format standard is also supported. The same CRC polynomial is used regardless of the selection of the ECC polynomials.

In addition, to support high density magnetic storage devices which do not require such a wide correction span, degree four and eight polynomials are provided for smaller ECC overhead (four and eight bytes per interleave, respectively), narrower correction span (two and four bytes per interleave, respectively), and shorter correction time (software dependent).

The device supports seven different interleave factors to optimize between the ECC overhead and correctable burst error length, once a proper polynomial is chosen. It supports one (no interleave), two, three, four, five, eight and 10-way interleaving. Because the coefficients of the generator polynomial is chosen from the GF(256), there can be only 255 symbols or bytes, per interleave including the ECC bytes. For that reason, the data field length of a block cannot exceed 255 times the interleave factor, less ECC/CRC overhead.

(The Maximum Data Field Length)
= 255 X (Interleave Factor) –
(ECC Overhead)–(CRC Overhead)

Number of ECC/Syndrome Bytes generated
(ECC Overhead)

Polynomial	Interleave Factors 1	2	3	4	5	8	10
Degree 16	16	32	48	64	80	128	160
Degree 8	8	16	24	32	40	64	80
Degree 4	4	8	12	16	20	32	40 (Bytes)

CRC Overhead = 0 if CRC is disabled.
= 4 if CRC is enabled.

Example:
For Degree 16, 10 interleave, no CRC,
(The Maximum Data Field Length)
= 255 X 10–160–0
= 2,390 Bytes

When used on 512-data-byte physical block, degree 16 polynomial, with five-way interleave with the CRC enabled, there are 103 data bytes in the first two interleaves and 102 bytes in the last three interleaves. The interleaves 0, 2, 3 and 4 include a byte each of CRC, which are also protected by the ECC, then each interleave has 16 bytes of redundancy (ECC).

EXAMPLE BLOCK FORMAT
(Degree 16, five interleaves, with CRC)

		INTERLEAVE			
0	**1**	**2**	**3**	**4**	
D0	D1	D2	D3	D4	→ ROW 0 PARITY
D5	D6	D7	D8	D9	→ ROW 1 PARITY
D10	D11	D12	D13	D14	→ ROW 2 PARITY
D15	D16	D17			→ ROW 3 PARITY
		D507	D508	D509	→ ROW 101 PARITY
D510	D511	CRC0	CRC1	CRC2	→ ROW 102 PARITY (UP TO D511)
CRC3	R0	R1	R2	R3	
R4	R5	R6	R7	R8	USED TO COMPUTE CRC0-CRC3
R9					
					LEGENDS:
		R71	R72	R73	D0-D511: 512 BYTES DATA
					CRC0-CRC3: 4 BYTES CRC
R74	R75	R76	R77	R78	CR0-R79: 80 BYTES ECC
R79					

They are output to the target peripheral controller in the order of D0 through D511, CRC0 through CRC3, R0 through R79.

Supported Polynomials

This section contains the definition of the polynomials supported by the WD60C80. Knowledge of the Reed-Solomon Code is assumed.

Finite Field Definition

This definition is common to all the polynomials including CRC.

Let β^1 represent elements of a finite field generated by the polynomial over GF(2):

$p(x) = X^8 + X^5 + X^3 + X^2 + 1$

The elements of the finite field employed by the code are:

$\alpha^1 = (\beta^1)^{88}$

ECC Generator polynomial for degree 16

Degree 16, distance 17, self-reciprocal, with coefficients from GF(256)

$$g(x) = \prod_{i=120}^{135} (x + \alpha^i)$$

ECC Generator polynomial coefficients in decimal are:
1 92 160 86 11 68 2 1 167 1 2 68 11 86 160 92 1

Code Type: Long distance, interleaved, Reed-Solomon code operating on one byte symbols.

Redundancy: Sixteen bytes per interleave.

Guaranteed Correction Span: Eight random symbol (byte) errors per interleave.

Special Considerations:
1) Redundancy bytes are inverted before writing.
2) The shift register implementing the code is initialized to zero.

ECC Generator polynomial for degree 8

Degree eight, distance nine, self-reciprocal, with coefficients from GF(256)

$$g(x) = \prod_{i=124}^{131} (x + \alpha^i)$$

ECC Generator polynomial coefficients in decimal are:
1 114 71 86 130 86 71 114 1

Code Type: Long distance, interleaved, Reed-Solomon code operating on one byte symbols.

Redundancy: Eight bytes per interleave.

Guaranteed Correction Span: Four random symbol (byte) errors per interleave.

Special Considerations:
1) Redundancy bytes are inverted before writing.
2) The shift register implementing the code is initialized to zero.

ECC Generator polynomial for degree 4

Degree four, distance five, self-reciprocal, with coefficients from GF(256)

$$g(x) = \prod_{i=126}^{129} (x + \alpha^i)$$

ECC Generator polynomial coefficients in decimal are:
1 64 61 64 1

Code Type: Long distance, interleaved, Reed-Solomon code operating on one byte symbols.

Redundancy: Four bytes per interleave.

Guaranteed Correction Span: Two random symbol (byte) errors per interleave.

Special Considerations:
1) Redundancy bytes are inverted before writing.
2) The shift register implementing the code is initialized to zero.

CRC Generator polynomial

The data field CRC code is specially constructed so that its residue can be adjusted as correction occurs. When correction is complete, the residue shall have been adjusted to zero.

Degree four, distance five, coefficients from GF(256)

$$g(x) = \prod_{i=136}^{139} (x + \alpha^i)$$

CRC Generator polynomial coefficients in decimal are:
1 232 194 35 198

Code Type: Reed-Solomon CRC operating on bytes.

Redundancy: Four bytes per sector, regardless of the number of interleave.

Statistical Detection Capability: The data field CRC code fails to detect an uncorrectable sector with probability of 2.3E-10 undetected uncorrectable sectors per uncorrectable sector.

Special Considerations:
1) The CRC code is applied to the XOR sum of data bytes across the interleaves.
2) Redundancy bytes are not inverted before writing.
3) The shift register implementing the code is initialized to zero.

Probability of uncorrectable error

Uncorrectable error rate is defined as the ratio of uncorrectable events to total bits transferred, and expressed in the formula below:

(Uncorrectable Error Rate)

$$= \frac{\text{Block Errors}}{\text{Bit}} = \frac{1}{kn} \sum_{i>e}^{n} \binom{n}{i} p^i (1-p)^{n-i}$$

where $\binom{n}{r} = \frac{n!}{r!\,(n-r)!}$

- n = Interleave length in symbols
- e = Maximum number of symbol errors correctable per interleave
- k = Symbol width in bits (8 bits for WD60C80)
- p = Raw symbol error probability (symbol errors/symbol)

(This formula is quoted from "Product Description for the NG8510", Data Systems Technology.)

It is assumed that error bursts occur at random intervals and each burst is assumed to affect a single symbol (one byte). If error bursts cluster or if error bursts span more than one symbol, the actual uncorrectable error rate will be greater. If each burst

is assumed to affect two symbols, the uncorrectable error rate becomes twice, and so on. A more complex computation is required when each burst is assumed to affect more than the number of interleaves employed.

Miscorrection Probability

Miscorrection probability of the code is 1.6E-6. Only those error events where the number of symbols in error in a single interleave exceeds eight are subject to miscorrection. The probability of transferring undetected erroneous data is the product of the probability of having more than eight errors in an interleave and the miscorrection probability of the code. For the degree 16 code, this probability is 7.7E-23 for a raw burst error rate of 1.0E-4.

Correction Software Support

The WD60C80 requires a companion software algorithm. This algorithm normally resides in the ROM of the external processor. Western Digital licenses the software implementing the required algorithm.

Internal Register Description

The WD60C40 has seven internal taskfile registers to set its operation modes, select programmable options and configurations, and report operational status. They are all accessed through the processor port using standard CPU interface with multiplexed address/data bus.

Register Map

The internal taskfile registers are mapped by the lower 4-bits of multiplexed address lines. For ease of interfacing to 16-bit processors, some of which require byte accesses to be on even or odd address boundaries, all registers are mirrored on even and odd addresses.

The address bits are latched by the internal address register which retains its contents until the next access, upon the ALE pulse input. Hence if a processor does not have a multiplexed bus, it can load the register address first by pulsing the ALE pin, then perform a read or a write in the next instruction.

A3,A2,1,0	HEX	SYMBOL	NAME	R/W,R/O	WIDTH
000X	0,1	CMDR	Command Register	R/W	8 bits
001X	2,3	STR0	Status Register 0	R/O	8 bits
010X	4,5	STR1	Status Register 1		8 bits
011X	6,7	STR2	Status Register 2		8 bits
100X	8,9	PRMR	Parameter Register	R/W	8 bits
101X	A,B	SSR1	Sector Size Register	R/W	4 bits
110X	C,D	SSR0	Sector Size Register		8 bits
111X	E,F		Syndrome FIFO	R/O	8 bits

Command Register

CMDR

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FT	SCB	CRC	SSO	WRT	ARM	RSV	RST

The Command Register is a Read/Write register that is used to set the WD60C80's operating mode. Since this register is used to activate/deactivate the device, writing to this register should be the last in the set up procedure.

Bit 0 RST–Software Reset/Abort Current Operation
Setting this bit high forces the internal reset logic to be activated, and the WD60C80 will halt current operation and clear itself to the default state. The following items are cleared:

- Command Register except RST bit.
- Parameter Register.
- Sector Size Registers.
- Status Registers.
- All internal state machines.
- Both (Data, Syndrome) internal FIFOs.

This bit does not clear by itself, so it needs to be set and then reset later by the external processor. It needs to be left set longer than four cycles of the input clock.

Bit 1 RSV – Reserved
This bit is reserved for a future enhancement.

Bit 2 ARM – Activate WD60C80 Function
This bit, when set high, activates the internal state machine of the WD60C80 to begin its operation by listening to the CD-bus activity. When low, the device is completely dormant. The taskfile should be initialized and set up prior to setting this bit.

Bit 3 WRT – Write Operation
When set high, the WD60C80 performs a write operation i.e., reads a block of data and outputs specified CRC/ECC. If it is low (default after reset), it performs a read operation (i.e., reads a block of data), CRC and ECC and generates a block of syndrome bytes, to be read by the external processor.

Bit 4 SSO – Single Sector Operation
When set high, the WD60C80 will operate on one block of data before clearing the ARM bit and disabling itself. The external processor has to activate the device before it can process another block. All other register content will be preserved.
When low (default after reset), it stays active and processes consecutive blocks of data until the ARM bit is externally cleared to a low.

Bit 5 CRC – CRC Encoding Enable
When set high, the WD60C80 activates its internal 32-bit CRC generator on read and write operations for extended correction and lower miscorrection probability. It adds four extra bytes to each block, between the data field and the redundancy field.

When low (default after reset), it disables the CRC generator.

Bit 6 SCB – Syndrome Transfer on Controller Bus
When set high, the WD60C80 directs the syndrome byte output to the controller bus (CDx pins) during the read operation thus enabling the user to share a single RAM for storing read/write data and syndrome information. Notice the option is valid only if the DMA transfer option is selected on the Parameter Register.

The parity check/generation option therefore is not available. When this mode of operation is chosen, it is the system designer's responsibility to arbitrate the controller bus between the data/ECC transfer and syndrome transfer. Due to this overhead, the actual throughput of the bus tends to be low, and the application should be limited to a low transfer rate environment.

When it is low (default after reset), the device directs the syndrome bytes through the processor bus, and the external processor or DMA device can perform the transfer with either PIO or DMA option

Bit 7 FT – FIFO Threshold ON

When set high, the WD60C80 delays setting the SDRQ pin until at least 10 bytes are accumulated inside the syndrome FIFO. This guarantees the burst DMA transfer of at least 10 bytes, reducing bus arbitration overhead between the processor and the DMA device, when the bus bandwidth requirement is high.

When set low (default after reset), the device sets SDRQ every time there is a byte in the syndrome FIFO. In either case, the SDRQ will clear itself when the last byte in the FIFO is being read.

Parameter Register

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PRMR	PCD	SDH	DMA	PS1	PS0	IS2	IS1	IS0

The Parameter Register is a Read/Write register that is used to set the operating configuration of WD60C80.

Bit 0-2 IS0-2 – Interleave Factor Selection Code
These three bits are used to specify the interleave factor of the ECC. For more details on interleaving.

IS2	IS1	IS0	Interleave Factor
0	0	0	5 (Default after reset)
0	0	1	10
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	8
1	1	X	1 (i.e., no interleaving)
(X = Don't Care)			

Bit 3-4 PS0-1 – Polynomial Selection Code
These two bits are used to specify the ECC polynomials to be used for the WD60C80 operation.

PS1	PS0	Polynomial
0	0	Degree 16 (Default after reset)
0	1	Degree 8
1	X	Degree 4
(X = Don't Care)		

Bit 5 DMA – Syndrome DMA Transfer Option
(Parity Check/Generation Disable) If this bit is set high, it enables the DMA mode operation on the syndrome transfer during the read, and disables the parity checker/generator. The DMA mode and parity checking are mutually exclusive options, because they share the same pin (CDP/SDACK) for their function. For DMA mode operation, this pin functions as SDACK, along with SDRQ, to perform Request-Acknowledge protocol.

The syndrome bytes will be output through the processor or the controller bus depending on the selection made in the Command Register. Notice this is the only way to direct the syndrome to the controller bus.

If this bit is set low (default after reset), then the syndrome transfer is performed in PIO (Programmed I/O) mode, where the external processor/DMA device accesses the syndrome FIFO as an internal register through the processor bus. An ALE pulse must be used to latch the address of the syndrome FIFO (0E Hex), then the device activates $\overline{CS}$ and $\overline{RE}$ to read it. Notice that to properly shift the internal FIFO pointer, $\overline{CS}$ $\overline{RE}$ pulse width must be wider than two FCLK cycles. In this mode, the CDP/SDACK pin becomes

the parity bit for the controller bus (CDx pins). When a byte is output from this bus, an odd parity (the total number of "high" bits in the nine bit field is odd) is output on this pin. If parity check is also enabled (see PCD bit), the WD60C80 will inspect the incoming data for odd parity (odd number of "high" bits at the CD0-CD7 and CDP pins) at the trailing edge of $\overline{\text{CDACK}}$ signal (input).

Using the PIO access method, the external processor can read the syndrome FIFO regardless of DMA bit setting. However, it can upset the byte count of the a DMA device if the processor tries to read the FIFO concurrently.

Bit 6 SDH – SDACK Pin Polarity Option (High Active)

This bit is used to control the polarity of SDACK pin, when DMA option is selected. When set high, the SDACK becomes a high active signal.

If set low, it becomes a low active signal, much like the $\overline{\text{CDACK}}$ pin. It defaults to active low after reset.

Bit 7 PCD – Parity Check Disable Option

This bit disables the parity checker, while leaving the parity generator ON. In order for this bit to be effective, the DMA bit must be set low, or both parity checker and generator is disabled.

After reset, this bit is set low, enabling the parity checker.

Sector Size Register

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SSRO	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0
SSR1					SS11	SS10	SS9	SS8

(INTERLEAVE FACTOR + 1) $\leq$ (SSR) $\leq$ (INTERLEAVE FACTOR X 255) – 1

The Sector Size Register is a Read/Write register that is used to set the length of the data field of a block. The register is 12-bit long, divided into the least significant 8-bit and the most significant 4-bit registers. The external processor is expected to set these registers to (number of data bytes - 1) prior to ARMing the device.

The contents of these registers are not decremented on each byte transferred, but rather, used to compare with the output of the internal data byte counter. Therefore, once they are loaded, the value stays intact until another value is loaded. This makes it convenient for multiple sector operation.

Example:

In order to set for the data field length of 1,024 bytes,
(Sector Size Register) = 1,024 - 1 = 1,023 = 3FF Hex
Store FF Hex to SSR0
Store 03 Hex to SSR1

Although it is a 12-bit register, the maximum data field length is limited to 255 times the specified interleave factor. This limitation is imposed by the finite field theory, which limits the length of any interleave to be less than or equal to 255 bytes due to the usage of coefficients from GF(256). The WD60C80 hardware requires at least one byte of data in each interleave to insure proper operation, therefore the minimum data field length is one plus the interleave factor. Violation of this rule may lead to all-zero CRC and all-FF(Hex) ECC bytes.

Example:

If degree 16, 10 interleave is selected,
11 $\leq$ (SECTOR SIZE REGISTER) $\leq$ 2,389.
The total sector length (less ID field) is:
(SECTOR SIZE REGISTER) + 1 + 4 (CRC BYTES) + 160 (ECC BYTES)

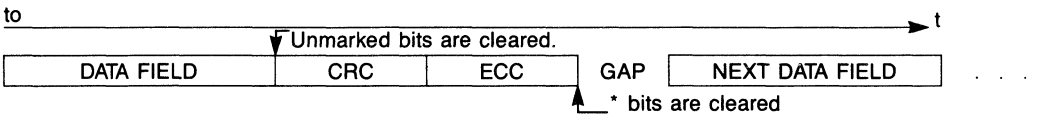
(SECTOR SIZE REG) + 1	4	160 Bytes
DATA FIELD	CRC	ECC

Status Registers

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
STRO	N/U	N/U	PERR*	DFO*	SFO	EERR	SDRQ!	BUSY!
STR1	I7E	I6E	I5E	I4E	I3E	I2E	I1E	I0E
STR2	N/U	CERR	PERR*	DFO*	SFO	EERR	I9E	I8E

N/U = Not Used

All bits are cleared at the end of the data field except:
* marked bits clear at the end of the current block.
! marked bits are real time signals and not latched.



The Status Registers are Read-Only registers that report operational status and error conditions of WD60C80. The values of STR1 and STR2 at the end of each block are also sent to the syndrome FIFO to be read by the host processor during read or write operations to check for any failures. STR0 is intended for general checking of the operational status of the device, so a few bits of information are covered in both STR0 and STR2.

Byte 0 Bit 0 BUSY – Device Busy
This is a real time signal indicating the active status of the WD60C80. When ARM = 1 is written to the command register, this bit is set high, indicating the active status. When a single sector operation is specified, this bit is cleared at the end of each block. Otherwise it stays ON until the ARM bit is externally cleared or reset/abort is activated.

Byte 0 Bit 1 SDRQ – Syndrome Transfer DMA Request

This is a real time signal indicating the syndrome FIFO has syndrome/status bytes inside and ready for transfer. This is similar to the SDRQ pin, except it ignores the FIFO threshold option. It is intended to be used with the PIO mode of syndrome transfer operation.

Byte 0 Bit 2 EERR – ECC Error Found
Byte 2 Bit 2
This is a latched status indicating that during the read operation, the device found a discrepancy(ies) between the internally generated ECC and retrieved ECC.

When this bit is set high, one or more of the "Interleave n in error" bits should also be set high. If there is an error(s), this bit is set during the ECC field of the block in question, and stays valid until the end of the data field of the next block.

Byte 0 Bit 3 SFO – Syndrome FIFO Overflow
Byte 2 Bit 3
This is a latched status indicating that during the read operation, the syndrome FIFO suffered an overflow due to insufficient access by the processor or DMA device. A syndrome byte is generated every time a redundancy byte is received and processed, and the system is expected to read them out at least at the data rate. The syndrome FIFO is 20-byte deep to smooth out the traffic on the bus, but most operations generate more than 20 bytes of syndrome/status. When an overflow occurs, the syndrome transfer logic still delivers the correct number of bytes, but there will be several garbage bytes among those transferred. This bit stays valid until the end of the data field of the next block.

Byte 0 Bit 4 DFO – Data FIFO Overflow
Byte 2 Bit 4
This is a latched status indicating that during the read or write operation, the data FIFO suffered an overflow, due to excessive transfer on the controller bus, or the FCLK frequency is too low. The device is expected to be clocked at least eight times the required data rate in byte/sec, and it is capable of supporting a 10-byte burst of 1/5 the clock frequency. Since the WD60C80 does not have any means of handshaking during the data read phase, any transfer rate adjustment must be made between the buffer manager and the target device, such as a disk controller, on the controller bus. When the overflow occurs, the device typically appears to be operating properly, except it has this error flag set and most likely generates wrong CRC and ECC codes. This bit stays valid till the end of the current block.

Byte 0 Bit 5 PERR – Parity Error Detected on Controller Bus
Byte 2 Bit 5
This is a latched status indicating parity error detection on the controller bus during the read or write operation. During the data read phase (if PIO option is selected and Parity Check is enabled), the WD60C80 checks for odd parity on the controller bus at the trailing edge of the $\overline{\text{CDACK}}$ signal (input). An odd parity is when you an have odd number of "high" bits in the nine-bits field (CD0-CD7, CDP). If any error is detected, this flag is set and stays valid until the end of the current block. This error flag, however, does not disturb other operations of the device, so its operation will complete as normal. It is the responsibility of the system firmware to analyze and recover from the error.

Byte 1 Bit 0 I0E – Interleave 0 in Error
This is a latched status indicating an ECC error(s) is detected in the first interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 1 I1E – Interleave 1 in Error
This is a latched status indicating an ECC error(s) is detected in the second interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 2 I2E – Interleave 2 in Error
This is a latched status indicating an ECC error(s) is detected in the third interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 3 I3E – Interleave 3 in Error
This is a latched status indicating an ECC error(s) is detected in the fourth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 4 I4E – Interleave 4 in Error
This is a latched status indicating an ECC error(s) is detected in the fifth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 5 I5E – Interleave 5 in Error
This is a latched status indicating an ECC error(s) is detected in the sixth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 6 I6E – Interleave 6 in Error
This is a latched status indicating an ECC error(s) is detected in the seventh interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 7 I7E – Interleave 7 in Error
This is a latched status indicating an ECC error(s) is detected in the eighth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 2 Bit 0 I8E – Interleave 8 in Error
This is a latched status indicating an ECC error(s) is detected in the ninth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

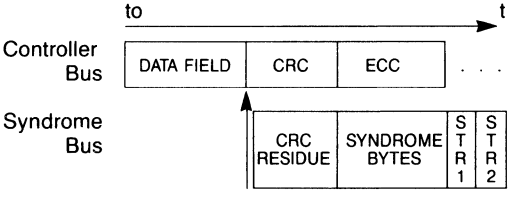
Byte 2 Bit 1 I9E – Interleave 9 in Error
This is a latched status indicating an ECC error(s) is detected in the tenth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 2 Bit 6 CERR – CRC Error Detected
This is a latched status indicating a CRC error is detected during the read operation. The processor should be able to find non-zero CRC residue. This bit is set during the CRC field and stays valid until the end of the data field of the next block.

Syndrome FIFO

Syndrome FIFO is a Read-Only 20-byte deep FIFO register used to transfer syndrome / status bytes during the read operation. It can be accessed either in DMA or in PIO mode, by setting up the Parameter Register properly. Even if it is set up for DMA mode transfer, the processor can still read it through PIO mode access, but the reverse is not true. Its status is indicated by the SDRQ pin and the SDRQ bit in the status register byte 0.

Timing Relationship between the Data flow and Syndrome Transfer



Syndrome FIFO cleared

During the read operation, the host must read through this FIFO, four bytes of CRC residue (if CRC option is set), syndrome bytes (number of bytes varies depending on the ECC polynomial and the interleave factor) and two bytes of final status (copies of status register byte 1 and 2, at the end of the block), in that order. During the CRC and ECC field, one byte is generated every eight FCLK cycles, and accumulated in this FIFO. It is the host's responsibility to read them out before the FIFO overflow occurs, or he can lose several syndrome bytes.

Number of Syndrome Bytes generated

	Interleave Factors							
Polynomial	**1**	**2**	**3**	**4**	**5**	**8**	**10**	
Degree 16	16	32	48	64	80	128	160	
Degree 8	8	16	24	32	40	64	80	
Degree 4	4	8	12	16	20	32	40	(Bytes)

(Total # of bytes to be transferred)
= CRC Residue (4) + Syndrome Bytes + Status Bytes (2)

During the write operation, no syndrome bytes are generated, but two bytes of final status are reported through this FIFO at the end of each block.

Regardless of FIFO threshold option, SDRQ will be set high (true) at the end of the block.

36

The syndrome FIFO is cleared of its contents at the end of the data field of every block. So the external host has until the end of the next data field to finish reading the syndrome bytes, as long as there is no FIFO overflow.

The host can read them out as fast as one fifth of the clock frequency, but care must be taken to insure the $\overline{CS}$ $\overline{RE}$ pulse width (PIO mode) or SDACK width (DMA mode) to be more than 2.0 clock cycles. The supported DMA protocol is the slave side of demand driven burst transfer (i.e., SDRQ stays high (true) as long as there is a byte in the FIFO), and the external master DMA device can read them out in a burst, until SDRQ clears.

If, for any reason, the DMA device tries to read the syndrome FIFO when SDRQ is not set, not only it is likely to get a garbage byte, but that may also also upset the internal FIFO pointer, thereby making the next-to-be-read syndrome byte inaccessible. This situation is not reported in the status register, so one must be careful to insure sufficient setup and hold time for the DMA protocol.

DC ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings indicate where permanent damage to the device may occur if exceeded. Continuous operation at these limits is not intended and should be avoided.

Operating Temperature ..... 0°C (32°F) to 70°F (158°F)
Storage Temperature ..... −55°C (−67°F) to +125°C (257°F)
Minimum Voltage on any pin with respect to V_{SS} ..... −0.3V
Maximum Voltage on any pin with respect to V_{DD} ..... +0.3V
V_{DD} with respect to V_{SS} ..... +7.0V

DC OPERATING CHARACTERISTICS

The following characteristics apply to the WD60C80 device in the given conditions, in the ambient temperature between 0°C and 70°C.

SYMBOL	CHARACTERISTIC	MIN	NOM	MAX	UNIT	COND.
V_{DD}	Power Supply Voltage	4.50	5.00	5.50	V	[1]
I_{DD}	Power Supply Current			25.0	mA	[1]

[1] Ta = 0°C, FCLK frequency = 25.0 MHz, all outputs open.

FOR ALL INPUTS:

SYMBOL	CHARACTERISTIC	MIN	NOM	MAX	UNIT	COND.
I_{IL}	Input Leakage Current			10.0	μA	[2]
V_{IL}	Input Low Level Voltage			0.8	V	
V_{IH}	Input High Level Voltage	2.0			V	

[2] Input Voltage = V_{DD}

FOR ALL OUTPUTS:

SYMBOL	CHARACTERISTIC	MIN	NOM	MAX	UNIT	COND.
I_{OZ}	Output Leakage Current			10.0	μA	[3]
V_{OH}	Output High Level Voltage Voltage	2.8 2.8			V V	[4] [6]
V_{OL}	Output Low Level Voltage Voltage			0.4 0.4	V V	[5] [7]

[3] Output Voltage = V_{DD}
[4] Applies to AD0 through AD7 pins only. Io = −2.5 mA
[5] Applies to AD0 through AD7 pins only. Is = +6.0 mA
[6] Applies to all other output/bidirectional pins. Io = −1.0 mA
[7] Applies to all other output/bidirectional pins. Is = +2.0 mA

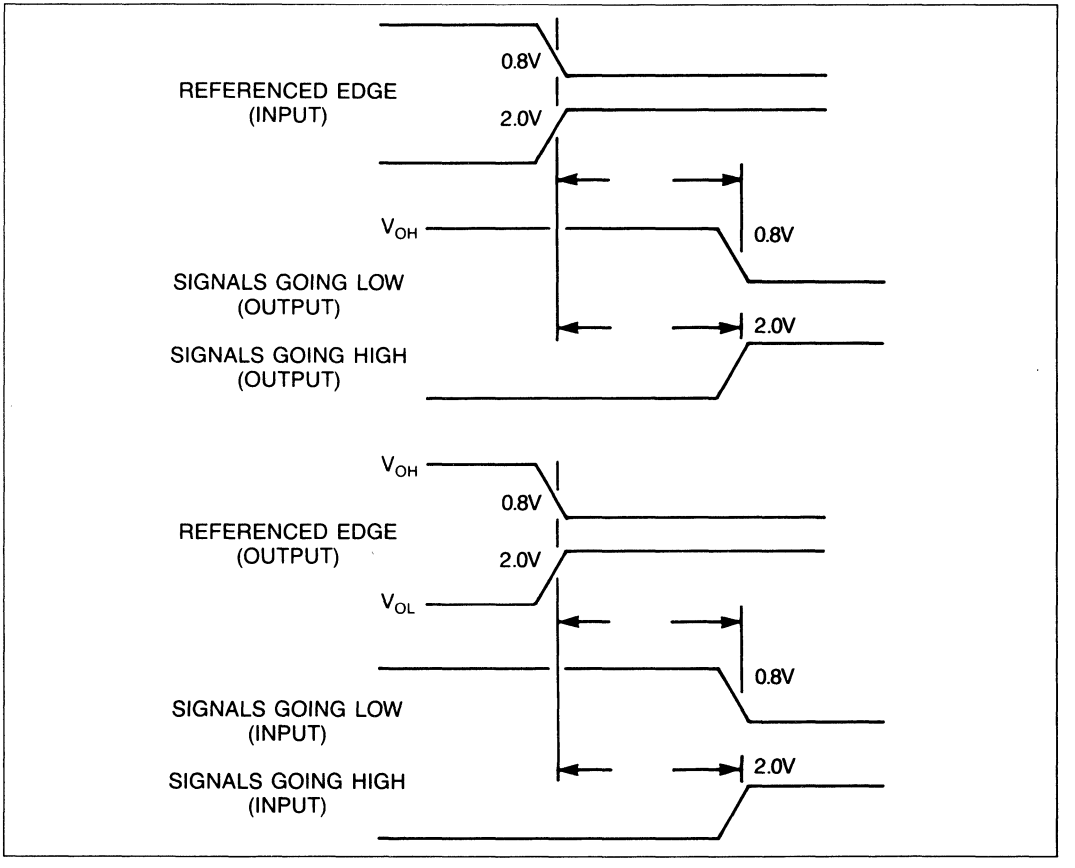
DC OPERATING CHARACTERISTICS (continued)

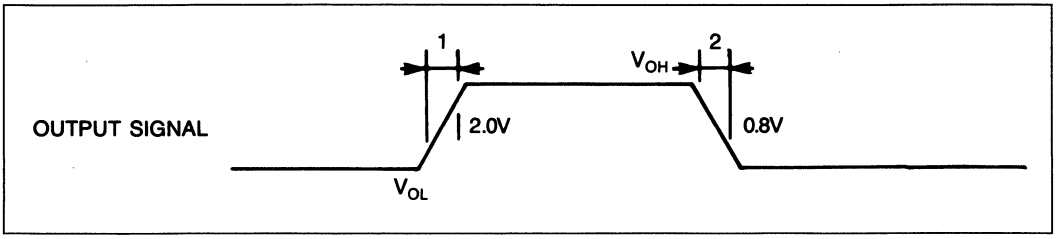
SYMBOL	CHARACTERISTIC	MIN	NOM	MAX	UNIT	COND.
I_{LU}	Latch Up Current	±40			mA	

AC TIMING CHARACTERISTICS

REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING
* Reference Number on the Timing Waveform Diagram.	* Abbreviated Symbol the Timing is Referred.		* The Reference Edge to which the Timing is Specified. L.E. = Leading Edge T.E. = Trailing Edge I.C. = Initial Condition	* Classification of Requirement/Specification R = Requirement on the External Interface S = WD60C80 Output Timing Specification	

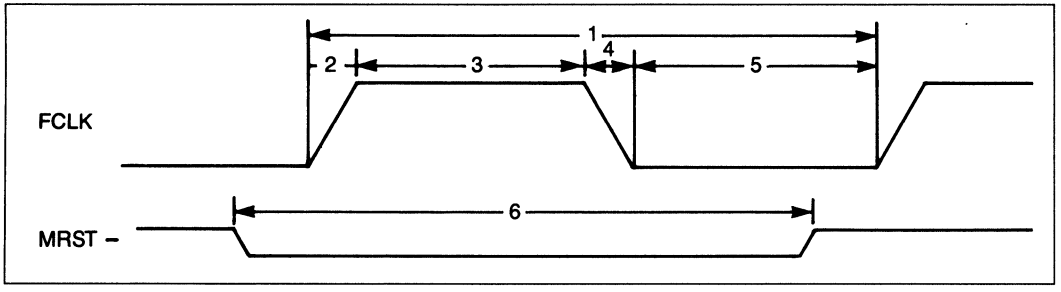
All the timing specifications assume the voltage levels shown below.
Capacitive loading on AD0-AD7 pins are 100 pF, and all other outputs are 50 pF.





REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TR	Output Rise Time	From V_{OL} to 2.0V	S	25 nsec	Max
2	TF	Output Fall Time	From V_{OH} to 0.8V	S	25 nsec	Max

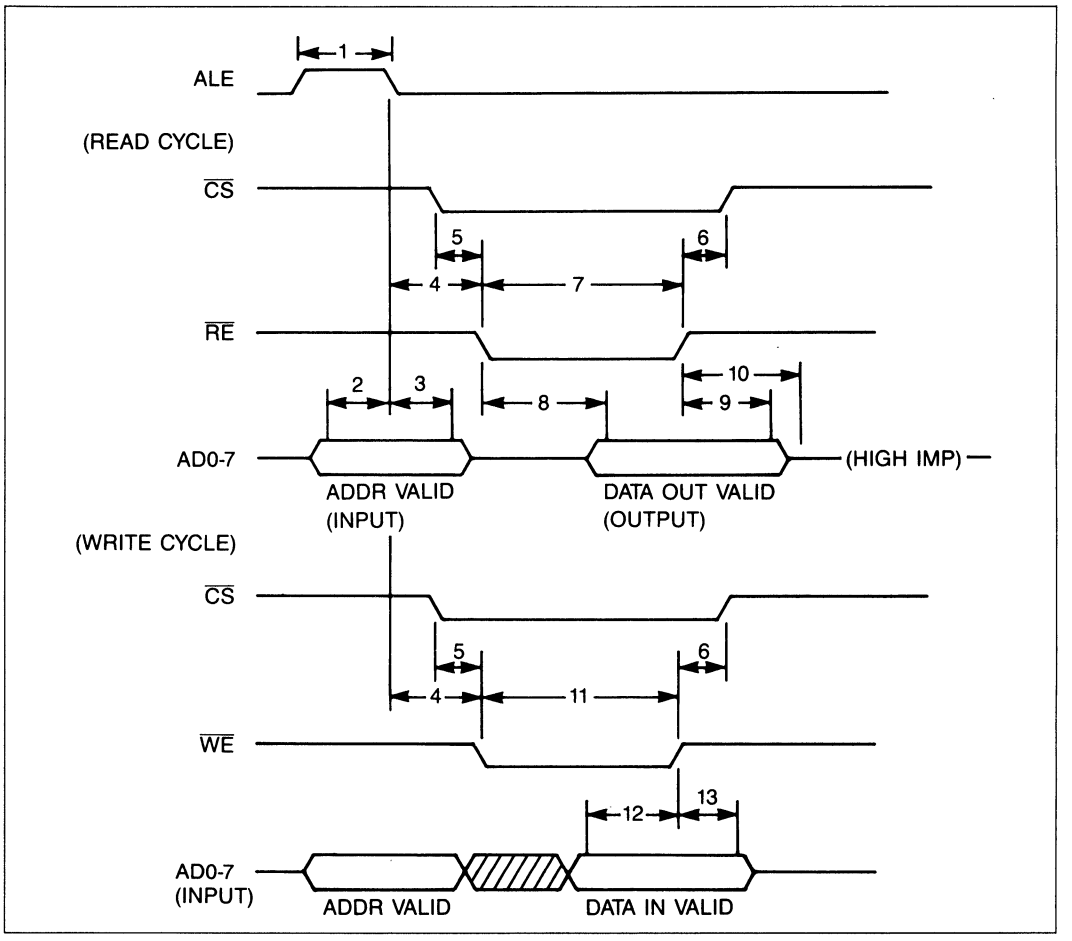
OUTPUT RISE/FALL TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	CLK	FCLK Cycle Time*		R	40 nsec	Min [1]
				R	60 nsec	Min [2]
2	TCR	FCLK Rise Time		R	10 nsec	Max
3	TCH	FCLK High Time		R	.4 CLK	Min
4	TCF	FCLK Fall Time		R	10 nsec	Max
5	TCL	FCLK Low Time		R	.4 CLK	Min
6	TMR	$\overline{MR}$ Pulse Width		R	80 CLK	Min

* This specification is used to define several other timings.
[1] The maximum clock frequency is 25 MHz if Degree 4 or Degree 8 polynomial is selected.
[2] If the Degree 16 polynomial is selected, the maximum clock frequency is 16.7 MHz.

CLOCK/RESET TIMING

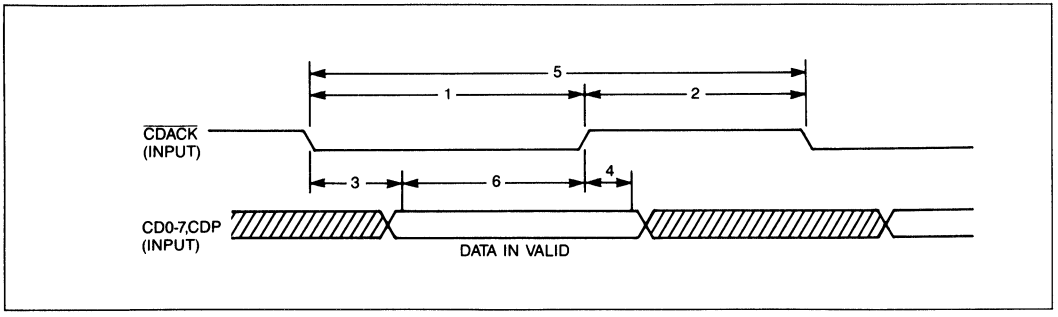


REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TALW	ALE Pulse Width		R	50 nsec	Min
2	TADS	Address Setup Time	Before T.E., ALE	R	15 nsec	Min
3	TADH	Address Hold Time	After T.E., ALE	R	15 nsec	Min
4	TRWD	RE/We Setup Time	After T.E., ALE	R	15 nsec	Min
5	TCSE	$\overline{CS}$ Setup Time	Before L.E., RE/WE	R	0 nsec	Min
6	THLD	$\overline{CS}$ Hold Time	After T.E., RE/WE	R	0 nsec	Min
7	TRE	$\overline{RE}$ Pulse Width		R	120 nsec	Min
					2.0 CLK	Min [1]
8	TDAC	Data Output Delay	After L.E., $\overline{RE}$	S	95 nsec	Max
9	TDOH	Data Hold Time	After T.E., $\overline{RE}$	S	20 nsec	Min
10	TDOT	Data Bus High imp.	After T.E., $\overline{RE}$	S	75 nsec	Max
11	TWE	$\overline{WE}$ Pulse Width		R	130 nsec	Min
12	TDS	Data Setup Time	Before T.E., $\overline{WE}$	R	50 nsec	Min
13	TDH	Data Hold Time	After T.E., $\overline{WE}$	R	10 nsec	Min

[1] This restriction applies only when reading the syndrome FIFO.

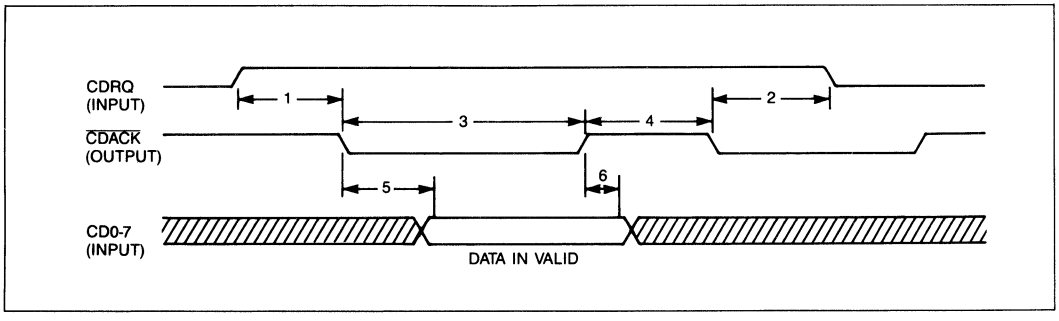
TASKFILE ACCESS TIMING
(Including PIO mode Syndrome Transfer)

CONTROLLER BUS TIMING



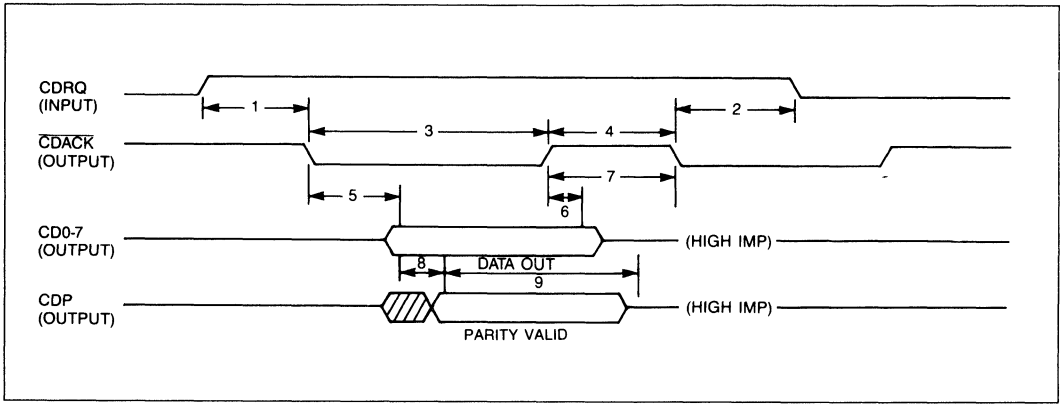
REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TCDK1	CDACK INP Pulse Width		R	2.0 CLK + 10nsec 100 μsec	Min Max
2	TCDC1	Transfer Recovery Time	After T.E. CDACK	R	2.0 CLK + 20 nsec	Min
3	TACC1	Data Access Time	After L.E. CDACK	R	4.0 CLK – 80 nsec	Max
4	TCDH1	Data Hold Time	After T.E. CDACK	R	10 nsec	Min
5	TCCDK	Transfer/Cycle Time	Between L.E. CDACK	R	5.0 CLK	Min
6	TCDS1	Data Setup Time	Before T.E. CDACK	R	40 nsec	Min

REDUNDANCY READ TIMING



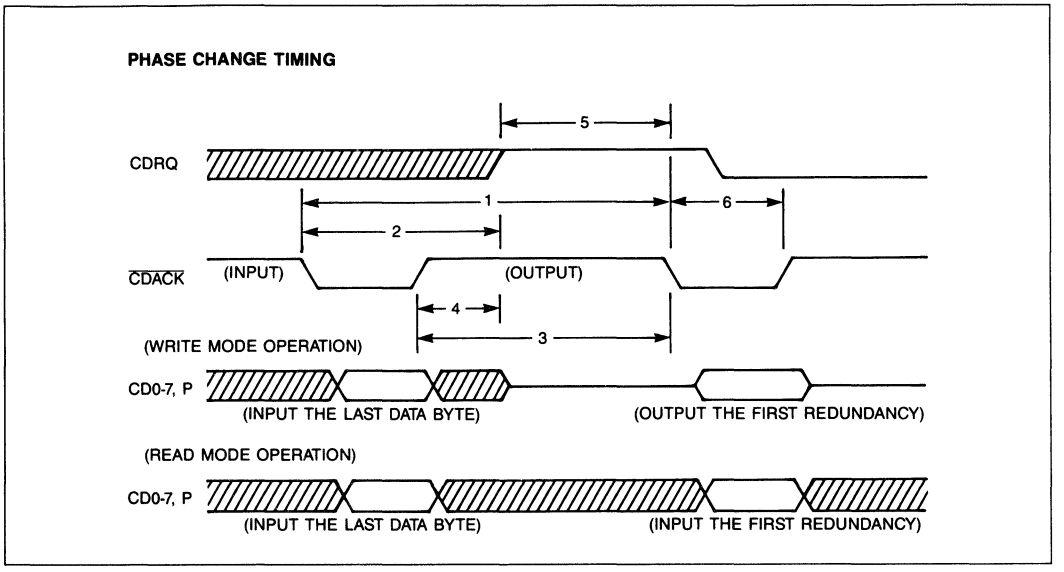
REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TCDD	CDACK Synchro Delay	After L.E., DRQ	S	2.0 CLK 4.0 CLK + 20 nsec	Min Max
2	TDRR	CDRQ Reset Timing	After L.E., CDACK	R	2.0 CLK – 15 nsec	Max
3	TCDK2	CDACK Out Pulse Width		S	4.0 CLK – 40 nsec	Min
4	TDCD2	CDACK Recovery Time	After T.E., CDACK	S	2.0 CLK	Min
5	TACC2	Data Valid Delay Time	After L.E., CDACK	S	4.0 CLK – 80 nsec	Max
6	TCDH2	Data Hold Time	After T.E., CDACK	S	10 nsec	Min

DATA READ TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TCDD	CDACK Synchro Delay	After L.E., CDRQ	S	2.0 CLK	Min
					4.0 CLK + 20 nsec	Max
2	TDRR	CDRQ Reset Timing	After L.E., $\overline{\text{CDACK}}$	R	2.0 CLK – 15 nsec	Max
3	TCDK2	CDACK Out Pulse Width		S	4.0 CLK – 40 nsec	Min
4	TCDC2	CDACK Recovery Time	After T.E., $\overline{\text{CDACK}}$	S	2.0 CLK	Min
5	TCDD	Data Valid Delay Time	After L.E., $\overline{\text{CDACK}}$	S	45 nsec	Max
6	TCDH2	Data Hold Time	After T.E., $\overline{\text{CDACK}}$	S	20 nsec	Min
7	TCDOT	Data Bus High Imp.	After T.E., $\overline{\text{CDACK}}$	S	50 nsec	Max
8	TCDPD	Parity Bit Delay Time	After CD0-7 Valid	S	20 nsec	Max
9	TCDPT	Parity Bit High Imp.	After CD0-7 H.I.	S	10 nsec	Max

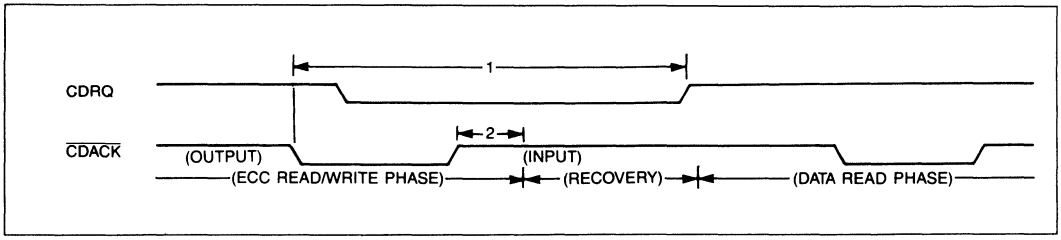
REDUNDANCY OUTPUT TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING
***WRITE Mode Operation (Assumes FIFO empty prior to receiving the last data)**					
1	TSOLW	Switch Over Cycle Time	After L.E., $\overline{CDACK}$	S	10.0 CLK Min [1] 12.0 CLK + 25nsec Max[1]
2	TCDLW	$\overline{CDACK}$ Direc. Reversal	After L.E., $\overline{CDACK}$	S	4.0 CLK Min[2] 6.0 CLK + 25nsec Max[2]
3	TSOTW	Switch Over Delay	After T.E., $\overline{CDACK}$	S	2.0 CLK Min
4	TCDTW	$\overline{CDACK}$ Direc. Reversal	After T.E., $\overline{CDACK}$	S	1.0 CLK Min
***READ Mode Operation (Assumes FIFO not full after receiving the last data)**					
1	TSOLR	Switch Over Cycle Time	After L.E., $\overline{CDACK}$	S	6.0 CLK Min[1] 8.0 CLK +24nsec Max[1]
2	TCDLR	$\overline{CDACK}$ Direc. Reversal	After L.E., $\overline{CDACK}$	S	4.0 CLK Min[2] 6.0 CLK + 25nsec Max[2]
3	TSOTR	Switch over Delay	After T.E., $\overline{CDACK}$	S	2.0 CLK Min
4	TCDTR	$\overline{CDACK}$ Direc. Reversal	After T.E., $\overline{CDACK}$	S	1.0 CLK Min
***WRITE/READ Operations**					
5	TCDD	$\overline{CDACK}$ Synchro Delay	After L.E., CDRQ	S	4.0 CLK + 20nsec Min[3]
6	TCDK2	$\overline{CDACK}$ Out Pulse Width		S	4.0 CLK – 40nsec Min

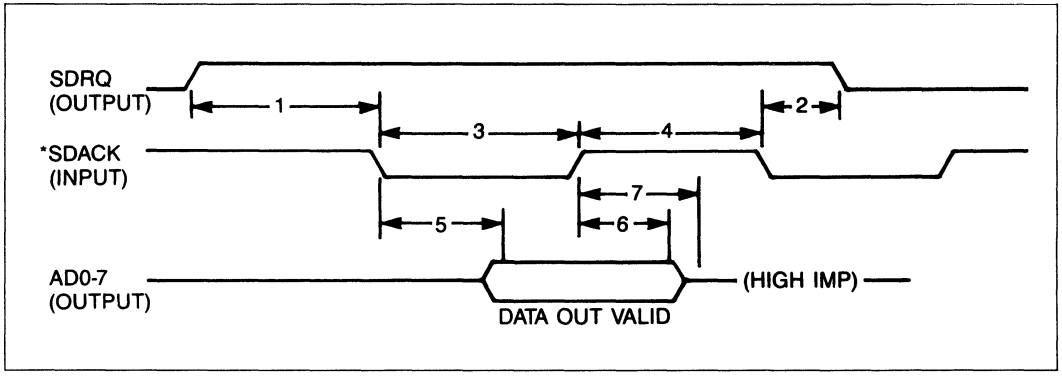
[1] This specification applies if TSOTR/W is met.
[2] This specification applies if TCDTR/W is met.
[3] This specification supercedes TSOLR/W and TCDLR/W.

PHASE CHANGE TIMING



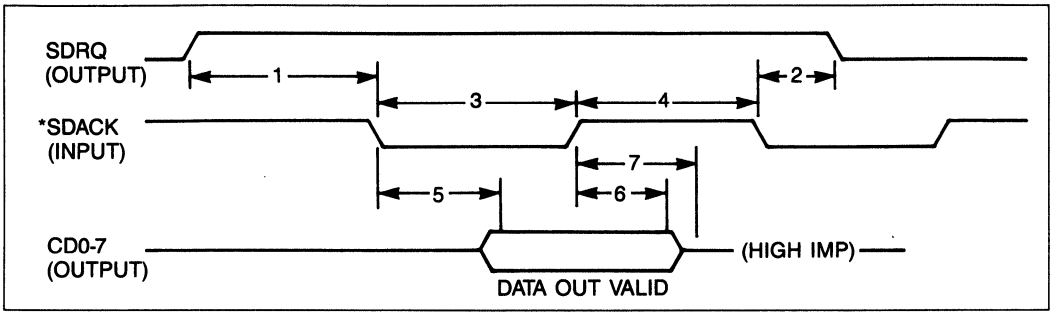
REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING
1	TSWI	Interblock Gap Time	After L.E., CDACK	R	15.0 CLK Min (Write OP) 47.0 CLK Min (Read OP)
2	TCDI	CDACK Direc. Reversal	After L.E., CDACK	S	1.0 CLK Min

INTER-BLOCK GAP TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TSDD1	SDACK Setup Time	After L.E., SDRQ	R	0 nsec	Min
2	TSDR	SDACK Reset Timing	After L.E., SDACK	S	80 nsec	Max
3	TSDK1	SDACK Pulse Width		R	3.0 CLK	Min
4	TSDC1	Transfer Recovery Time	After T.E., SDACK	R	2.0 CLK + 10 nsec	Min
5	TSDA1	Data Output Delay	After L.E., SDACK	S	85 nsec	Max
6	TSDH1	Data Hold time	After T.E., SDACK	S	40 nsec	Min
7	TSDT1	Data Bus High Imp.	After T.E., SDACK	S	85 nsec	Max

DMA TRANSFER TIMING (SYNDROME ON PROCESSOR BUS)

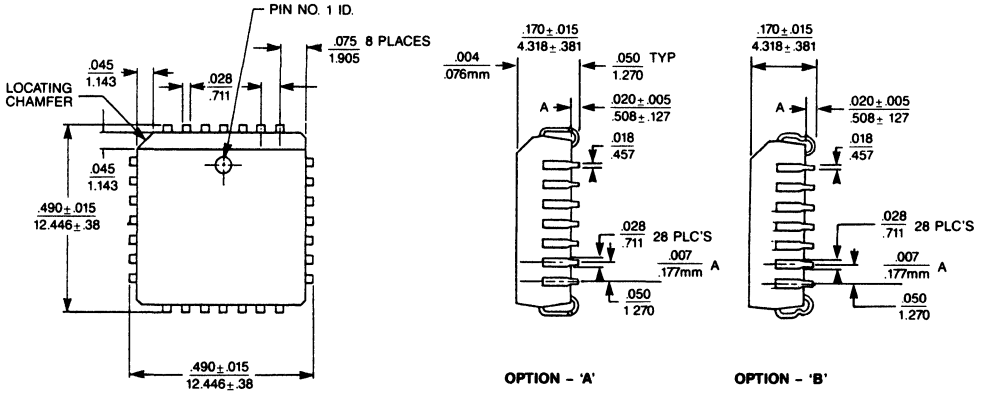


REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TSDD2	SDACK Setup Time	After L.E., SDRQ	R	0 nsec	Min
2	TSDR	SDACK Reset Timing	After L.E., SDACK	S		
3	TSDK2	SDACK Pulse Width		R	4.0 CLK	Min
4	TSDC2	Transfer Recovery Time	After T.E., SDACK	R	2.0 CLK + 10 nsec	Min
5	TSDA2	Data Output Delay	After L.E., SDACK	S	110 nsec	Max
6	TSDH2	Data Hold Time	After T.E., SDACK	S	40 nsec	Max
7	TSDT2	Data Bus High Imp.	After T.E., SDACK	S	120 nsec	Max

* SDACK low active option is shown.

SYNDROME TRANSFER TIMING (SYNDROME ON CONTROLLER BUS)

PACKAGE INFORMATION



28 LEAD PLASTIC "JH"

WD83B692

Ethernet Transceiver

WESTERN DIGITAL

TABLE OF CONTENTS

APPENDICES

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 DESCRIPTION AND APPLICATION

The WD83B692 Ethernet Transceiver is a high-speed, bipolar line transmitter/receiver. The device includes analog transmit and receive buffers, a 10-MHz on-board oscillator, timing logic for jabber and heartbeat functions, output drivers, and a bandgap reference, in addition to a current reference and collision detector. The WD83B692 is pin-for-pin compatible with the National DP8392/NS32492 Coaxial Transceiver Interface (CTI).

The Ethernet Transceiver (ET) is used as a coaxial cable line transmitter/receiver for Ethernet/Cheapernet-type local area networks (LANs). In Ethernet applications, the ET is part of a transceiver media attachment unit (MAU) that connects directly to the coaxial transmission media and communicates with the data terminal equipment (DTE) through a transceiver cable, the attachment unit interface (AUI).

1.1 FEATURES

- Conforms to Ethernet II (10BASE5) and Cheapernet (10BASE2) IEEE 802.3 standards, including IEEE 802.3 reliability specifications and receive mode collision circuitry requirements
- Provides complete integration of transceiver function (except signal and power isolation)
- Requires minimal external components
- Contains on-board jabber function
- Provides combined noise rejection and squelch circuits for transmit and receive inputs
- Provides heartbeat disable to allow use in repeaters
- Incorporates high speed bipolar technology

2.0 THEORY OF OPERATION

This document describes the operation of the WD83B692 Ethernet Transceiver, and provides information on the following:

1. Receiver
2. Transmitter
3. Collision Signaling
4. Collision Detection
5. Jabber Function
6. Heartbeat Function

The WD83B692 is part of a three-device set that implements the complete 802.3 IEEE-compatible Ethernet network node electronics (see Figure 1-1). The WD83C690 Ethernet LAN controller (ELC) and the WD83C691 Ethernet Manchester encoder/decoder (MED) comprise the other two devices in the set. The ELC provides media access protocol functions and performs buffer management tasks, while the MED provides the Manchester encoding and decoding for transmission and data clock separation from received data.

Figure 1-1 shows the connection for Ethernet applications of the WD83B692 ET between the coaxial cable and the DTE.

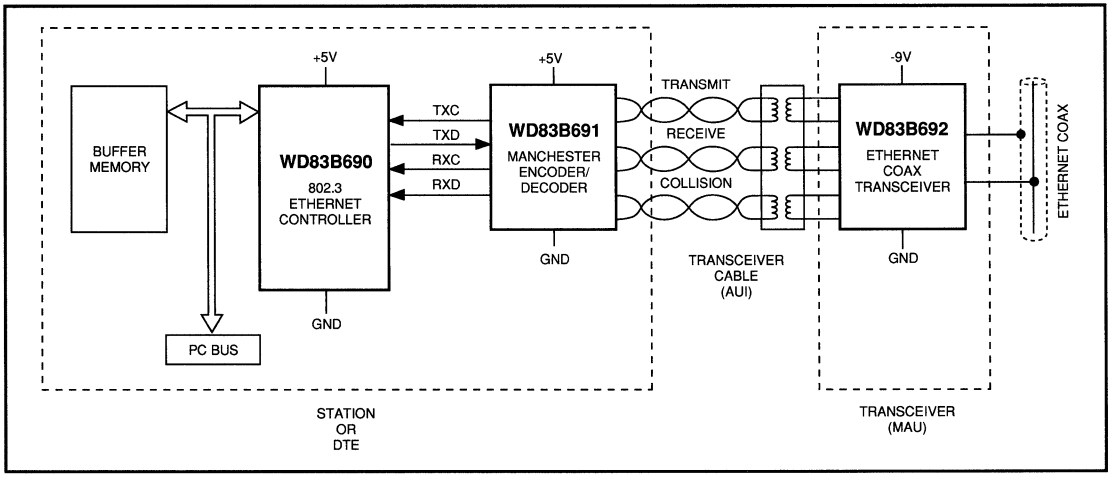


FIGURE 1-1. WD83B692 SYSTEM INTERFACE

37

The coaxial transmitter is a current source driver with a controlled pulse waveform that minimizes jitter and spurious harmonics during transmissions. The receiver senses data on the coaxial transmission media and outputs the data to the Manchester encoder/decoder via the RX+ and RX- AUI pins. These pins drive the AUI cable through a pulse isolation transformer.

3.0 OPERATIONAL DESCRIPTION

This section describes the six basic functions of the Ethernet Transceiver, including receiving, transmitting, collision signaling, collision detection, jabber timing, and the heartbeat function. Refer to Figure 3-1 for a general system block diagram.

3.1 Receiver Functions

The receiver senses signals at pin 14 through the RXI input, which minimizes reflections on the transmission media using a low capacitance, high resistance input buffer amplifier. The CDS ground input at pin 16 attaches directly to the input buffer from the coaxial shield to eliminate ground loop noise.

In addition to the input buffer, the receiver data path consists of an equalizer, data slicer, receiver squelch circuitry, and an output line driver.

The equalizer improves the jitter margin; the data slicer restores equalized received signals to fast transition signals with binary levels to drive the receiver line driver; and the receiver line driver drives the AUI cable through an isolation transformer that connects to the AUI interface. See Figure 3-2.

Noise on the transmission media is rejected by the receiver squelch circuitry, which determines valid data via two criteria: DC level and pulse width. The DC voltage level is detected and compared to a set level in the receiver comparator circuit. The pulse width must be greater than 20 nsec and repeat at valid data rates. It is detected using a pulse detector, operating like a retriggerable one-shot that resets at approximately two signal bit times. The pulse width detector disables the receiver line driver at the end of a transmission (Figure C-1).

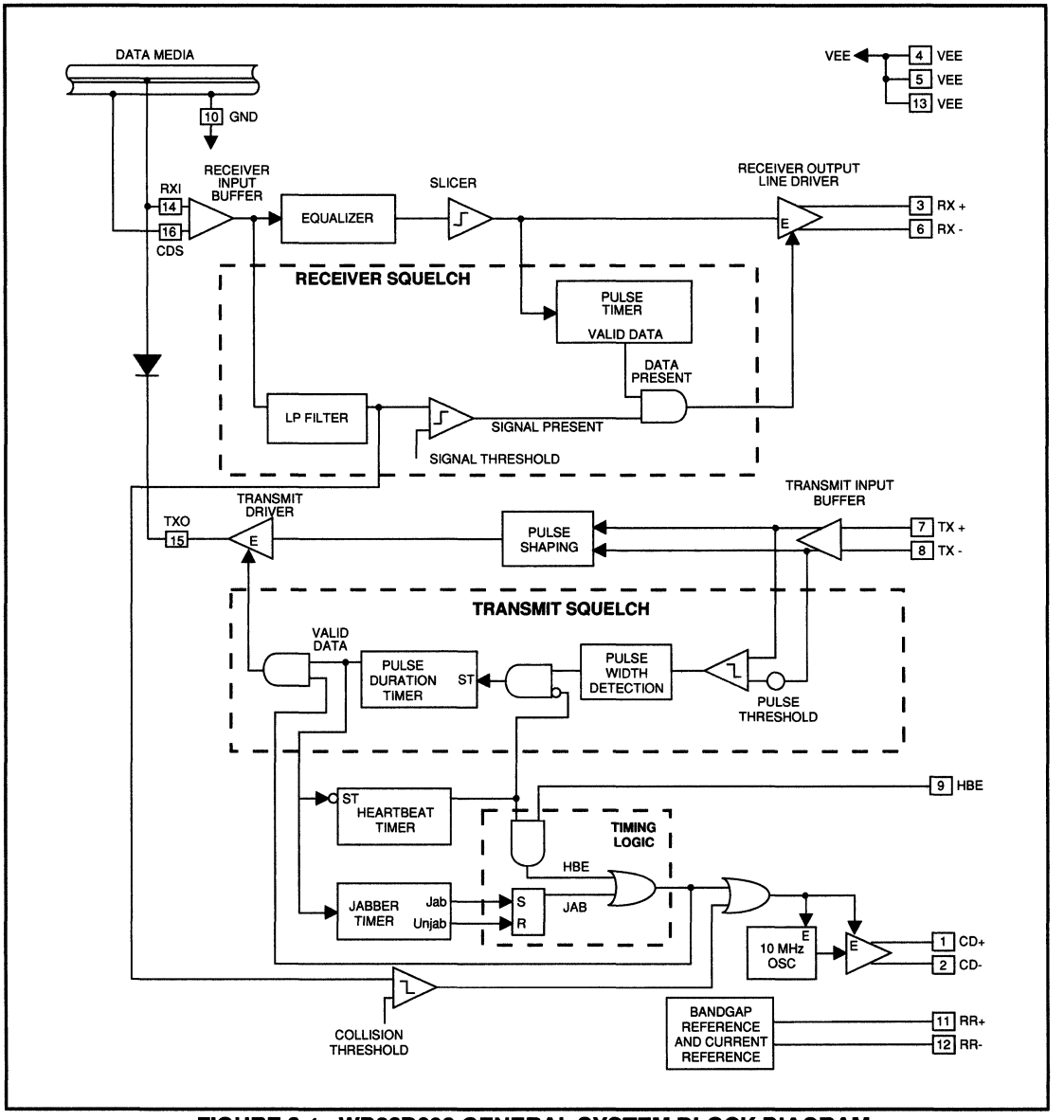


FIGURE 3-1. WD83B692 GENERAL SYSTEM BLOCK DIAGRAM

37

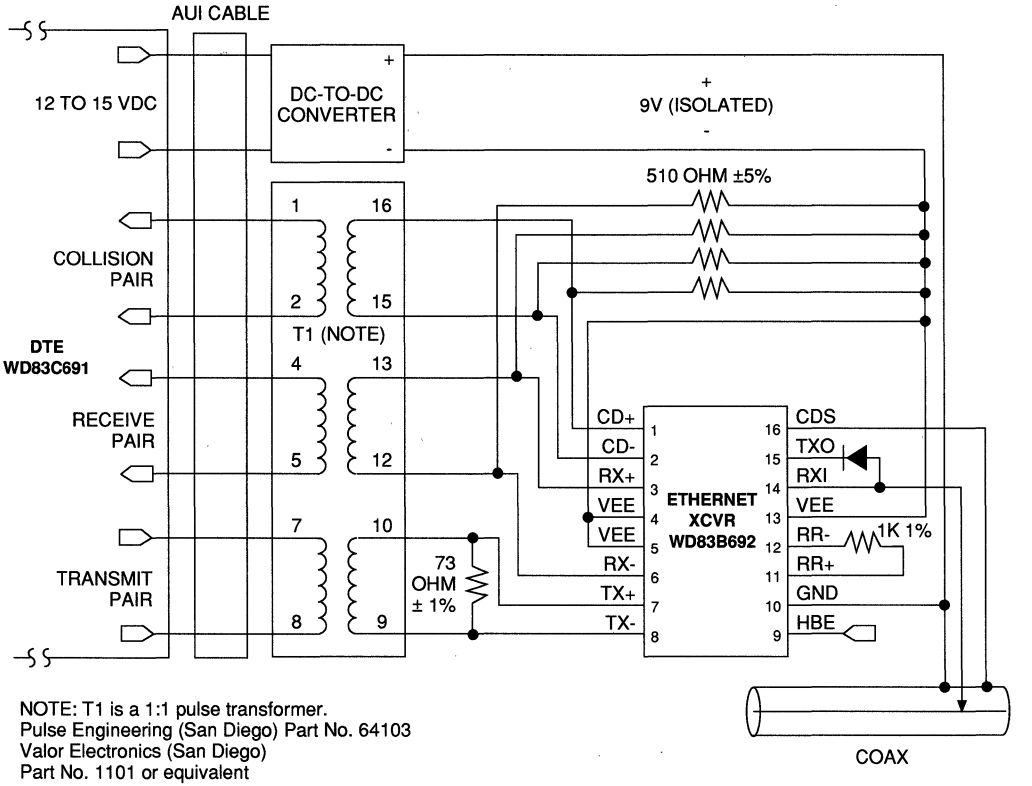


FIGURE 3-2. CONNECTION DIAGRAM

3.2 Transmitter Functions

The transmitter data path consists of a transmit input buffer, a pulse-shaping network (ramp generator), transmit squelch circuitry, a transmit driver, and a transmit output line driver.

The self-biasing, transmit input buffer receives data through an isolation transformer and translates the AUI differential analog signal to digital signals suitable for driving the pulse shaping network. The pulse shaping network gives equal rise and fall times to the transmit driver, which uses a high impedance current source output to drive the transmission media. The capacitance of the transmit driver is isolated from the transmission media by an external diode with a low capacitance anode. The shield of the transmission media serves as the ground return for the transmitter function.

A transmit squelch circuit, which consists of a pulse threshold detector, a pulse width detector, and a pulse duration timer, is used to suppress noise, as well as crosstalk, on the AUI cable. The squelch circuitry disables the transmit driver if the signal at TX+ or TX- is smaller than the pulse threshold. Pulse noise is rejected by a pulse width detector that passes only pulses with durations greater than 20 nsec. The pulse duration timer disables the transmit driver if no pulses are received for two-bit periods following valid pulses. At the end of a transmission, the pulse duration timer disables the transmitter and triggers the blanking timer, used to block "dribble" bits.

3.3 Collision Signaling

When collision signaling is enabled, a 10-MHz signal is sent to the CD% pins (1,2) through an isolation transformer to the Manchester encoder/decoder. When the function is disabled, this output goes to a zero differential state. The 10-MHz output from the CD pins indicates a collision on the transmission media, a heartbeat function, or that the transmitter is in jabber mode.

3.4 Collision Detection

A collision occurs when two or more transmitters simultaneously access the transmission media. A collision is detected by comparing the DC level of the transmission media to a collision threshold. The received signal at RXI (pin 14) is buffered and sent through a low pass filter, then compared in the collision threshold circuit. If the DC level exceeds the collision threshold, the 10-MHz oscillator and CD outputs are enabled.

3.5 Jabber Function

When valid data is transmitted, the jabber timer is started. If there is valid data for more than 20 msec, a latch is set which disables the transmitter and enables the 10-MHz output on the CD pins. The latch is reset within 0.5 seconds after the valid data is removed from the transmitter input (TX%). This action resets the jabber timer and disables the 10-MHz oscillator and CD output. The TX% inputs must remain inactive during the 0.5-second reset period.

3.6 Heartbeat Function

The 10-MHz oscillator and CD outputs are enabled for about 1 µsec at approximately 1.1 µsec after the end of each transmission. The heartbeat signal tells the DTE that the circuit is functioning. This is implemented by starting the heartbeat timer when the valid data signal indicates the end of a transmission.

A.0 APPENDIX A

A.1 PIN DESIGNATIONS

Figure A-1 illustrates the 16-pin DIP device. Table A-1 lists all pin designations.

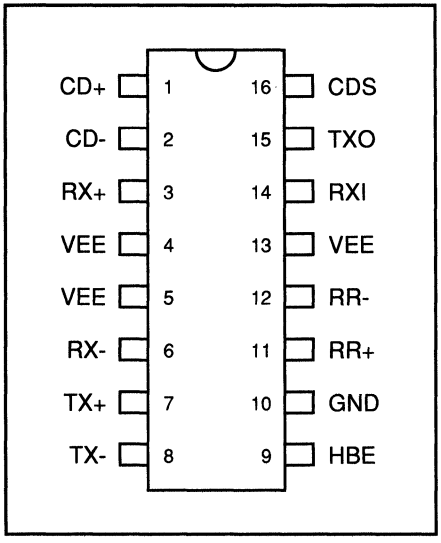


FIGURE A-1. WD83B692 16-PIN DIP ETHERNET TRANSCEIVER

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
1,2	CD+,CD-*	Collision Output	Balanced differential line driver outputs from the collision detect circuitry. The 10-MHz signal from the internal oscillator is transferred to these outputs in the event of collision, jabber, or a heartbeat condition. These outputs are open emitters; pull-down resistors to VEE are required. When operating into a 78-ohm transmission line, these resistors should be 500 ohms. In Cheapernet applications, where the 78-ohm drop cable is not used, higher resistor values (up to 1.5K) may be used to save power.
3,6	RX+,RX-*	Receiver Output	Balanced differential line driver outputs from the receiver. These outputs require 500-ohm pull-down resistors.
7,8	TX+,TX-*	Transmit Input	Balanced differential line receiver inputs to the transmitter. The common mode voltage for these inputs is determined internally. Signals meeting transmitter squelch requirements are wave-shaped and output at TXO (pin 15).
9	HBE	Heartbeat Enable	This input enables CD heartbeat when grounded and disables it when connected to VEE.
10	GND	Ground	Ground positive supply. A 0.1 μ F ceramic decoupling capacitor must be connected across GND and VEE as close to the component as possible.
11,12	RR+, RR-	External Resistor	A fixed, 1.0K, 1.0% resistor connected between these pins establishes internal operating currents.
14	RXI	Receiver Input	Connects directly to the coaxial cable. Signals meeting receiver squelch requirements are equalized for intersymbol distortion, amplified, then output at the RX+ or RX- pin.
15	TXO	Transmitter Output	In both Ethernet and Cheapernet applications, this connects through an isolation diode to the coaxial cable.

TABLE A-1. PIN DESIGNATIONS

PIN NUMBERS	MNEMONIC	SIGNAL NAME	FUNCTION
16	CDS	Collision Detect Sense	This is the ground sense connection for the collision detect circuit. This pin should be connected separately to the shield to avoid ground drops from altering the receive mode collision.
4,5,13	VEE	Negative Supply	These pins should be connected to a large area of the lower metal layer on the PC board to handle heat dissipation.

TABLE A-1. PIN DESIGNATIONS (Continued)

*IEEE names for CD± = CI±; RX± = DI±; TX± = DO±

B.0 APPENDIX B

B.1 DC OPERATING CHARACTERISTICS

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not recommended; operation should be limited to those conditions specified under Recommended Operating Characteristics.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-12V
Input Voltage	0 to -12V
Package Power Rating at 25° C (77° F)	2.5 Watts

(PC Board Mounted)

Derate linearly at the rate of 20 mWatts/°C

Lead Temperature (soldering, 10 seconds)	300°C (572 °F)

Electrostatic Discharge (ESD) 1200V*

* All pins tested per MIL-STD-883 Method 3015, Human Body Model. For the RXI pin only, the specified value is 500V.

Storage Temperature -65°C (-85°F) to 150°C (302°F)

(For actual dissipation of the device refer to Table B-1.)

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (VEE)	-9V ±5%
Ambient Temperature	0°C (32°F) to 70°C (158°F)

37

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	NOTES*
VOC	Common Mode Output Voltage (RX%, CD%)	-2.5	-2.0	-1.5	V	3,7,8
VOB	Differential Output Voltage Imbalance (RX%, CD%)	-	-	%40	mV	3,8,9
IOB	Differential Output Current Imbalance	-	-	%4.0	mA	3,8,9
VOD	Differential Output Voltage	%600	-	%1200	mV	3,8
ZR	Input Impedance Real (TX%)	1.24	-	-	KΩ	-
ZI	Input Capacitance (TX%)	0	-	6.0	pF	-
VTC	Common Mode Input Voltage (TX%)	-1.8	-	-1.2	V	12
VLT	Differential Logic Threshold (TX%)	0	-	338	mV	-
CMR	Common Mode Rejection (TX%)	40	-	-	dB	11
HE	Heartbeat Enable	VEE+1.5	GND	-	V	-
HD	Heartbeat Disable	-	VEE	VEE+.01	V	-
RR	Reference Resistor	0.99	-	1.01	KΩ	-
IEE1	Supply Current - Non-Transmitting	-	85	130	mA	-
IEE2	Supply Current - Transmitting	-	125	180	mA	-
IRX1	Receive Input Bus Current	-2.0	-	+20	µA	3
CX	Input Capacitance (RXI)	-	1.2	-	pF	3
RRXI	Shunt Resistance - Non-Transmitting (RXI)	1.0	-	-	MΩ	3

TABLE B-1. DC OPERATING CHARACTERISTICS

Ta = 0°C (32°F) to 70°(158°), VEE = -9V% 5% (See Note 2 on page 1-11.)

*Refer to Notes on p. 1-11.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	NOTES
VCD	Collision Threshold (Receive Mode)	-1.58	-1.492	-1.404	V	10
VSQ	Input Squelch Threshold	-0.6	-	-0.35	V	-
ITDC	Transmit Output DC Current Level	37	41	45	mA	4
ITAC	Transmit Output AC Current Level	%28	-	ITDC	mA	4,5
RTXON	Shunt Resistance - Transmitting (TXO)	7.5	10	-	KΩ	4,6
RTXOF	Shunt Resistance - Non-Transmitting (TXO)	200	-	-	KΩ	4
ILOF	Leakage Current - Non-Transmitting	-	-	%1.0	µA	3,4
CTXO	Capacitance - Non-Transmitting	-	8	-	pF	3,4

TABLE B-1. DC OPERATING CHARACTERISTICS (continued)

NOTES:

1. Currents into device pins are positive; currents out of device pins are negative. If not specified, voltages are referenced to ground.
2. All typicals are for VEE = -9V, Ta = 25°.
3. 0 > VEE > -9.5V.
4. The voltage on TXO is -4V < V(TXO) < 0.0V.
5. The AC current measurement is referenced to the DC current level.
6. The shunt resistance does not degrade the ITAC current if five transmitters are simultaneously driving a 50Ω-terminated coax cable.
7. Operating or idle state.
8. Test load as shown in Figure B-1.
9. Device measurement taken in idle state.
10. This threshold can be determined by monitoring the CD% output with a DC level into RXI.
11. The TXO does not switch with a 100 mVpp common mode sine wave input for frequencies from 0 to 10 MHz input to TX+, TX- with a common mode DC level from 0 to -3V.
12. This is a self-bias, level-generated on device, and is measured with a DC voltmeter with no external load on the TX+ or TX- pin.

37

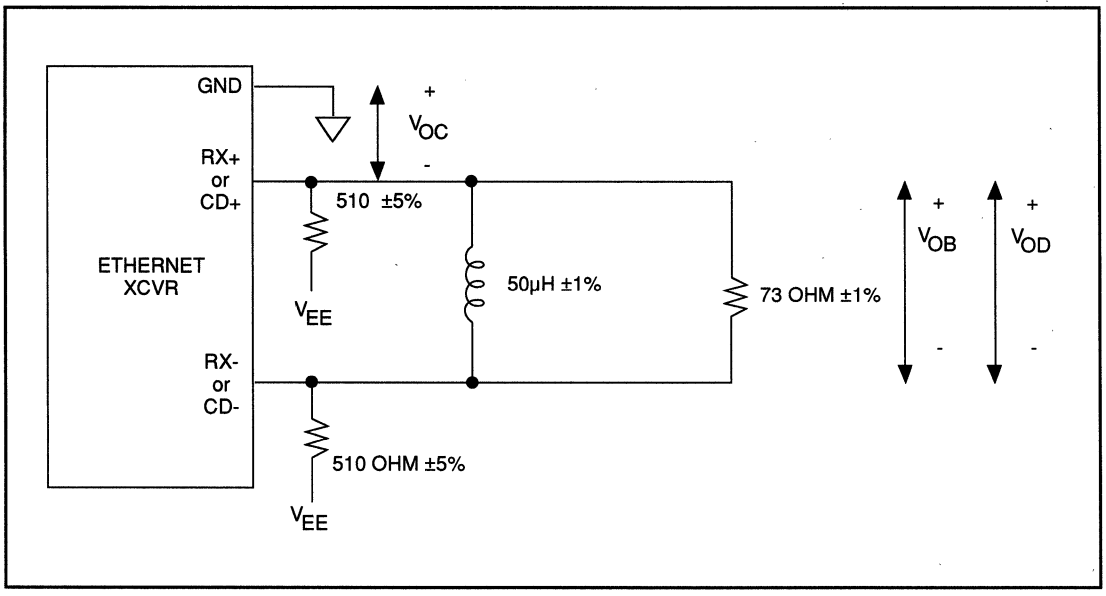


FIGURE B-1. TEST LOAD FOR CD% OR RX%

C.0 APPENDIX C
C.1 AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	NOTES*
	Transmit Specification					
t_{TST}	Transmitter Start-up Delay (See Figure C-2)	-	1	2	bits	8
t_{TD}	Transmitter Propagation Delay (See Figure C-2)	-	25	50	nsec	8
t_{TS}	Transmitter Jitter	-	%0.5	2.0	nsec	7,8
t_{TR}	Transmitter Rise Time; 10 - 90% (See Figure C-2)	20	25	30	nsec	-
t_{TF}	Transmitter Fall Time; 90 - 10% (See Figure C-2)	20	25	30	nsec	-
t_{TM}	t_{TR} and t_{TF} Mismatch (See Figure C-2)	-	1	-	nsec	-
	TX% Transmit Squelch Timing					
t_{TON}	Transmit Turn-on Pulse Width at VTS (See Figure C-2)	8	25	30	nsec	-
t_{TOFF}	Minimum Transmit Turn-off Pulse Width at VTS (See Figure C-2)	-	180	-	nsec	-
	Receive Specification					
t_{RJ}	Receive Jitter (See Figure C-6)	-	2	4	nsec	5
t_{RON}	Receiver Start-up Delay (See Figure C-1)	-	4	5	bits	4
t_{RD}	Propagation Delay (See Figure C-1)	-	15	50	nsec	-

TABLE C-1. AC OPERATING CHARACTERISTICS

Ta = 0°C (32°F) to 70°C (158°F); see note 3 on page 1-16. VEE = -9V%5%, Bit Time = 100 nsec

*Refer to Notes on p. 16.

37

Transmit Specifications

The first bit transmitted from TXO may have data and phase violations. The second through last bit reproduce the TX% signal with less than or equal to specified jitter.

There is no logical signal inversion between TX% and TXO output. A low level from TX+ to TX- results in more current flowing from the coaxial cable into the TXO pin.

At the end of transmission, when the transmitter changes from the enabled state to the idle state, no spurious pulses are generated, i.e., the transition on TXO proceeds monotonically to zero current.

Receive Specifications

The first bit sent from RX% may have data and phase violations. The second through last bit reproduce the received signal with less than or equal to specified jitter.

There is no logical signal inversion between the RXI input and the RX% output. A high level at RXI produces a positive differential voltage from RX+ to RX-.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	NOTES*
	RX%, CD% Specification					
t_{RR}	Differential Outputs Rise Time	-	4	5	nsec	-
t_{RF}	Differential Outputs Fall Time	-	4	5	nsec	-
t_{EV}	Dynamic Pulse Envelope	(See Figure C-9)				6
v_{CM}	AC Common Mode Signal	-	-	50	mV	-

TABLE C-1. AC OPERATING CHARACTERISTICS (continued)

*Refer to Notes on p. 16.

Active to Idle Transition

The output waveform conforms to the limits as specified in Figure C-10.

Short Protection

The electrical and physical characteristics of the RX%, CD% outputs are not altered if the pins are shorted together or to ground.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	NOTES*
	CD% Collision Detection Timing					
t_{CON}	Collision Turn-on Delay (See Figure C-3)	-	7	9	bits	-
t_{COFF}	Collision Turn-off Delay (see Figure C-3)	-	-	20	bits	-
f_{CD}	Collision Frequency (See Figure C-3)	8.5	-	11.5	MHz	-
t_{CP}	Collision Pulse Width (See Figure C-3)	40	-	60	nsec	-
t_{HON}	CD Heartbeat Delay (see Figure C-4)	0.6	-	1.6	µsec	-
t_{HW}	CD Heartbeat Duration (See Figure C-4)	0.6	1.0	1.5	µsec	-

TABLE C-1. AC OPERATING CHARACTERISTICS (continued)

*Refer to Notes on p. 16.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	NOTES
Jabber Timing						
t_{JA}	Jabber Activation Delay (See Figure C-5)	20	50	150	msec	-
t_{JR}	Jabber Reset Unjab Time (See Figure C-5)	250	300	750	msec	-

TABLE C-1. AC OPERATING CHARACTERISTICS (continued)

NOTES

1. Absolute maximum ratings are values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.
2. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.
3. All typicals are given for VEE = -9V and Ta = 25°.
4. RXI low to RX± out of idle state.
5. Using the test configuration load shown in Figure C-6, jitter is measured at RX± in relation to transmitter edges. The waveform is a 10-MB Manchester-coded signal with an amplitude of 0.749 to 2.6 Vpp. The waveform has a rise and fall time of 25 ± 1 nsec and zero jitter. The DC level is from 0 to 2.6V and does not clip input waveform.
6. The dynamic voltage waveform stays within the shaded area of Figure C-9 when loaded as shown in Figure B-1.
7. Transmitter jitter is the difference in propagation delay from TX± to TXO for rising and falling output transition. This is measured using a random Manchester-coded signal.
8. The TX± input operates with signals meeting the RX± timing and amplitude specifications.

TIMING DIAGRAMS

Table C-2 lists all timing diagrams. Figures C-1 through C-12 illustrate all timings.

FIGURE NUMBER	TITLE
C-1	Receiver Timing
C-2	Transmitter Timing
C-3	Collision Timing
C-4	Heartbeat Timing
C-5	Jabber Timing
C-6	Receive Jitter Timing
C-7	Coaxial Transceiver Receive Timing
C-8	Coaxial Transceiver Transmit Timing
C-9	Dynamic Pulse Envelope
C-10	Enable to Idle Transition; CD±,RX±
C-11	Test Loads
C-12	Test Circuit for TX± Input

TABLE C-2. WD83B692 TIMING DIAGRAMS

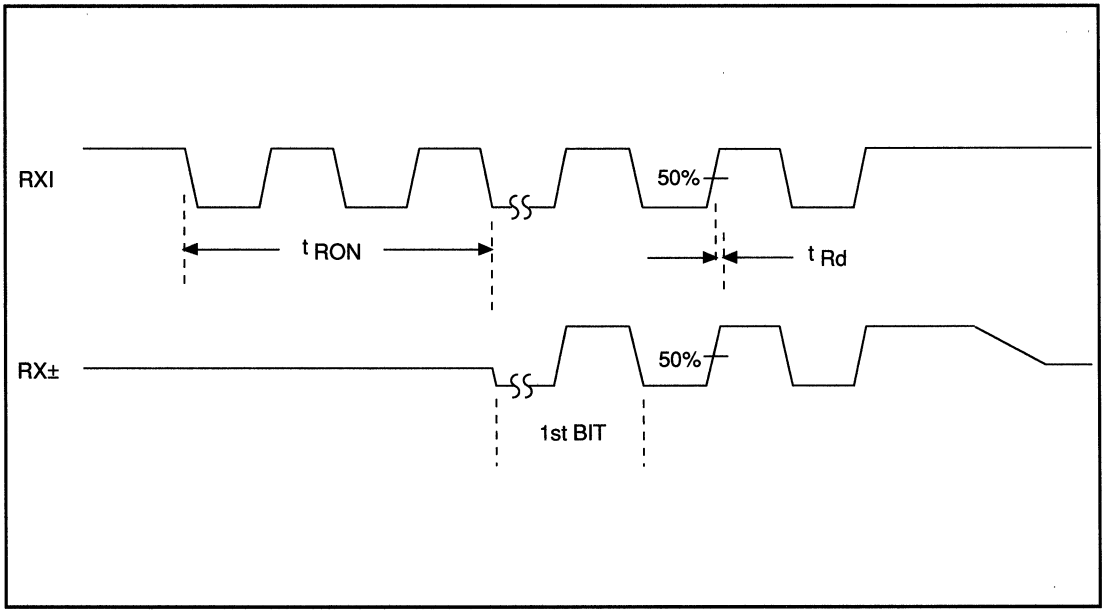


FIGURE C-1. RECEIVER TIMING

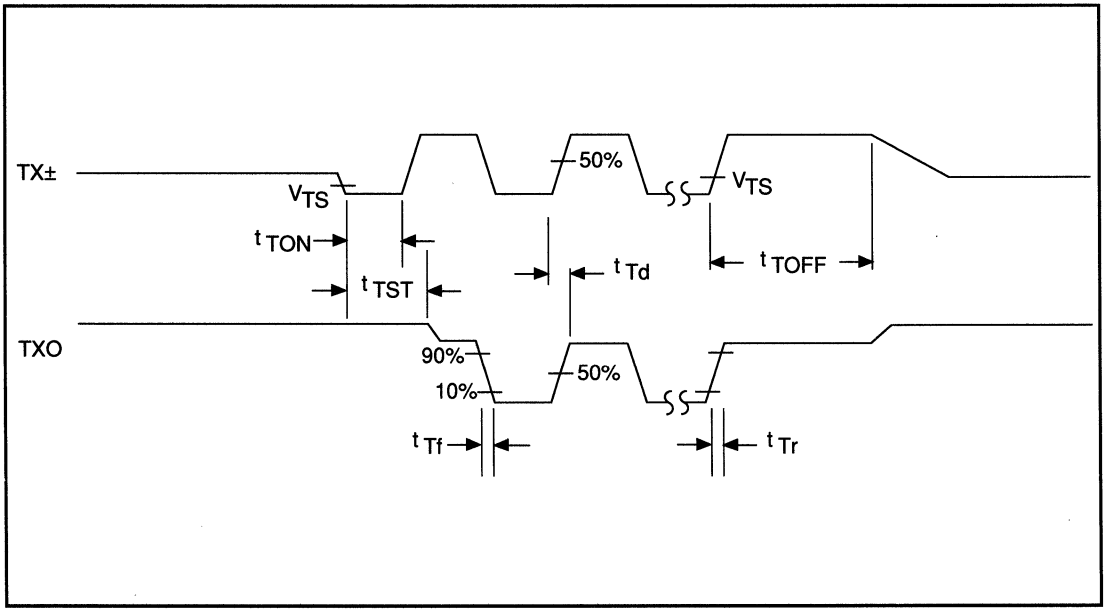


FIGURE C-2. TRANSMITTER TIMING

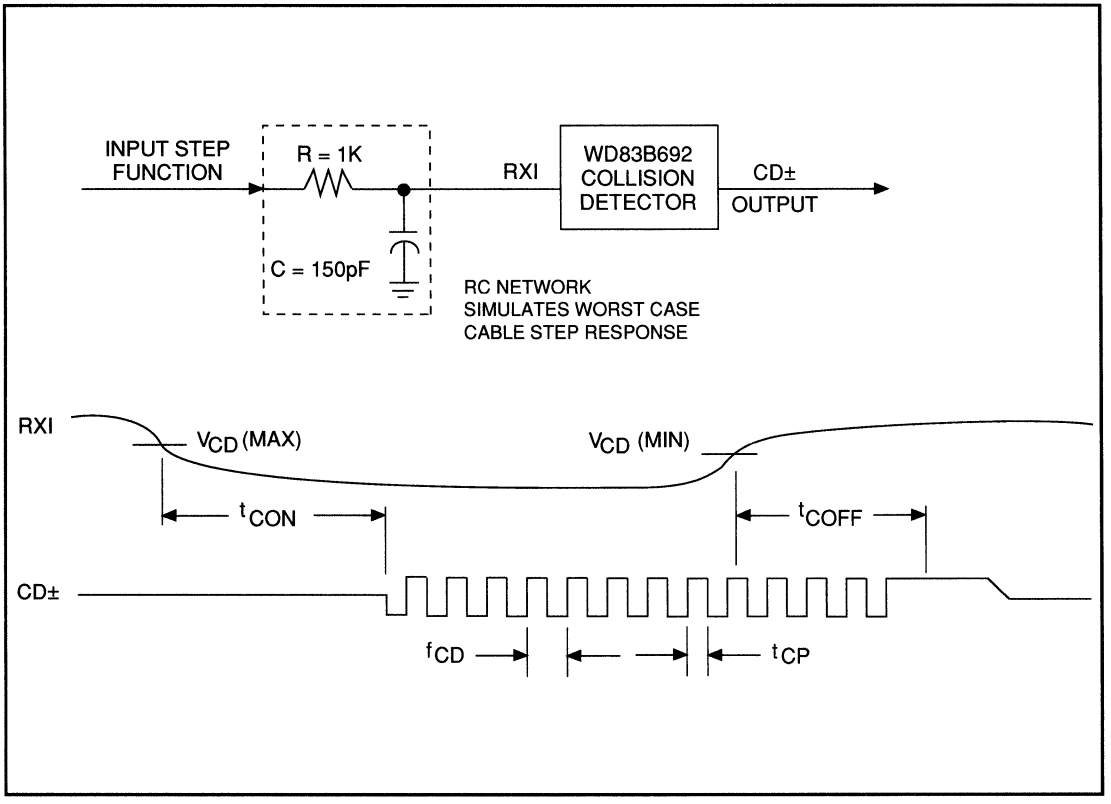


FIGURE C-3. COLLISION TIMING

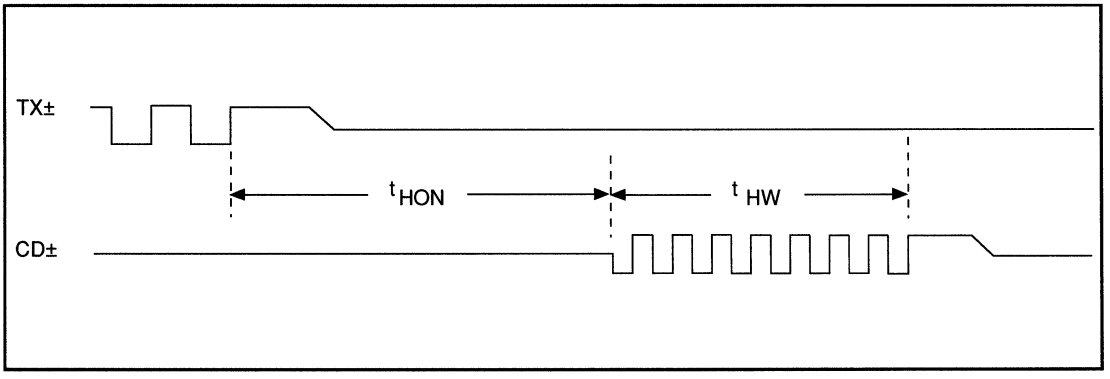


FIGURE C-4. HEARTBEAT TIMING

37

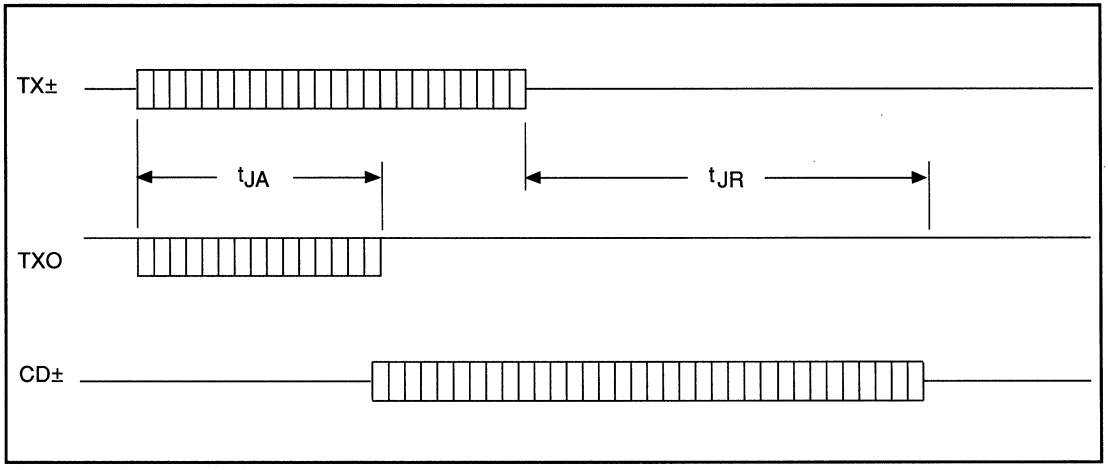


FIGURE C-5. JABBER TIMING

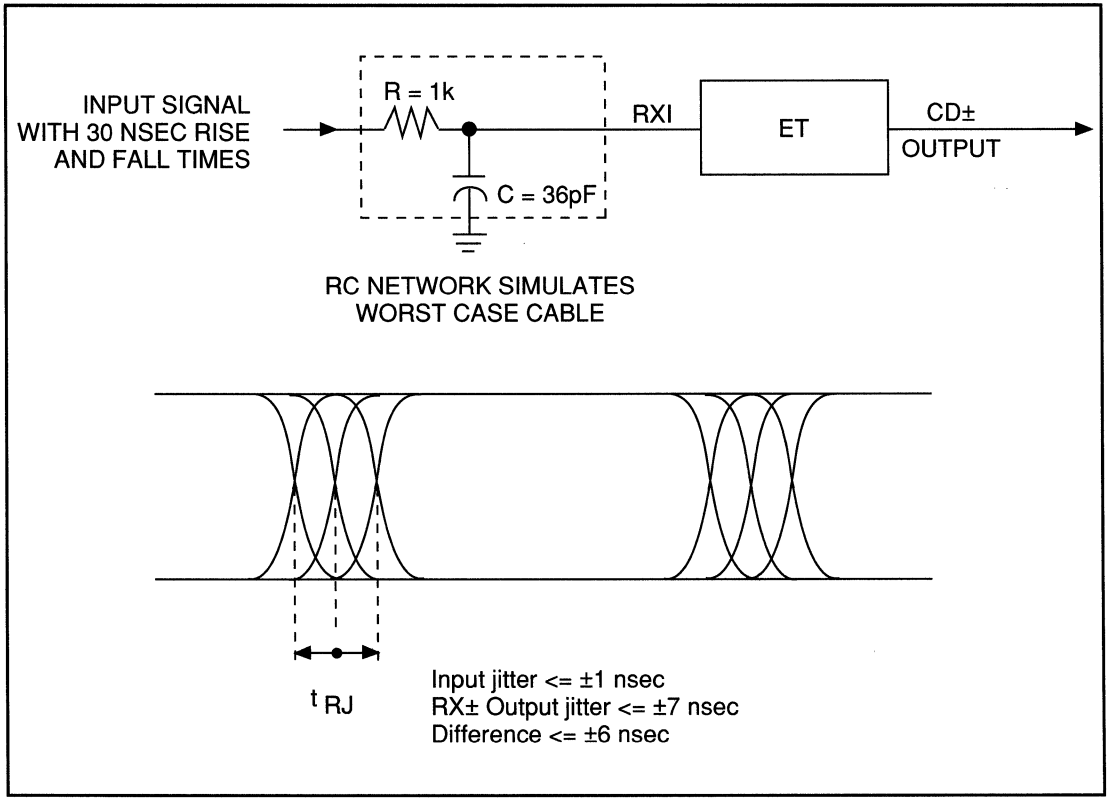


FIGURE C-6. RECEIVE JITTER TIMING

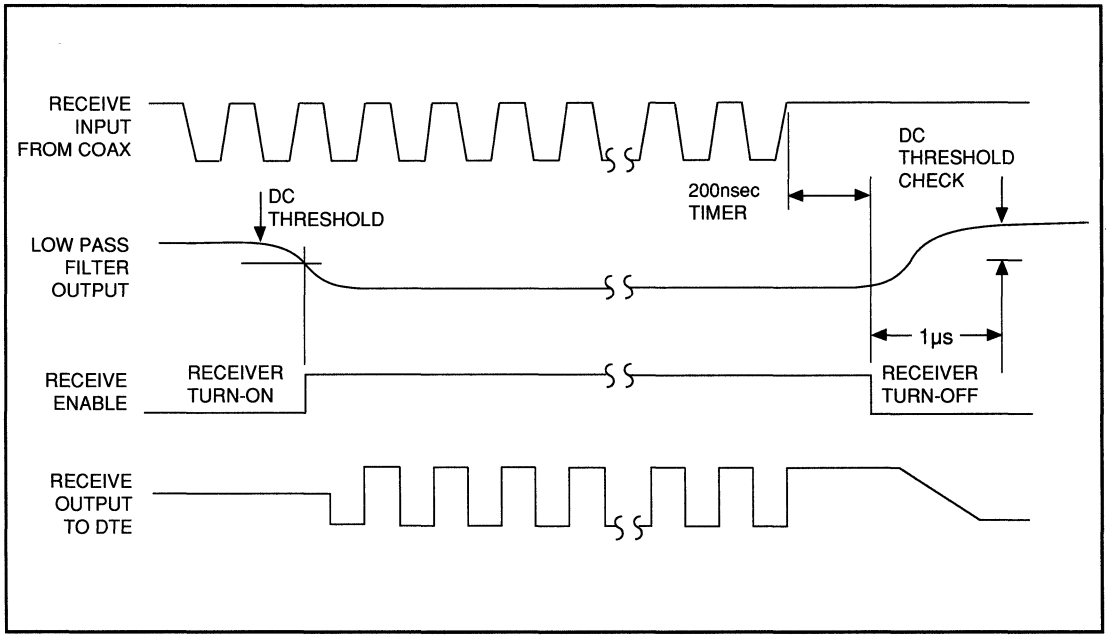


FIGURE C-7. COAXIAL TRANSCEIVER RECEIVE TIMING

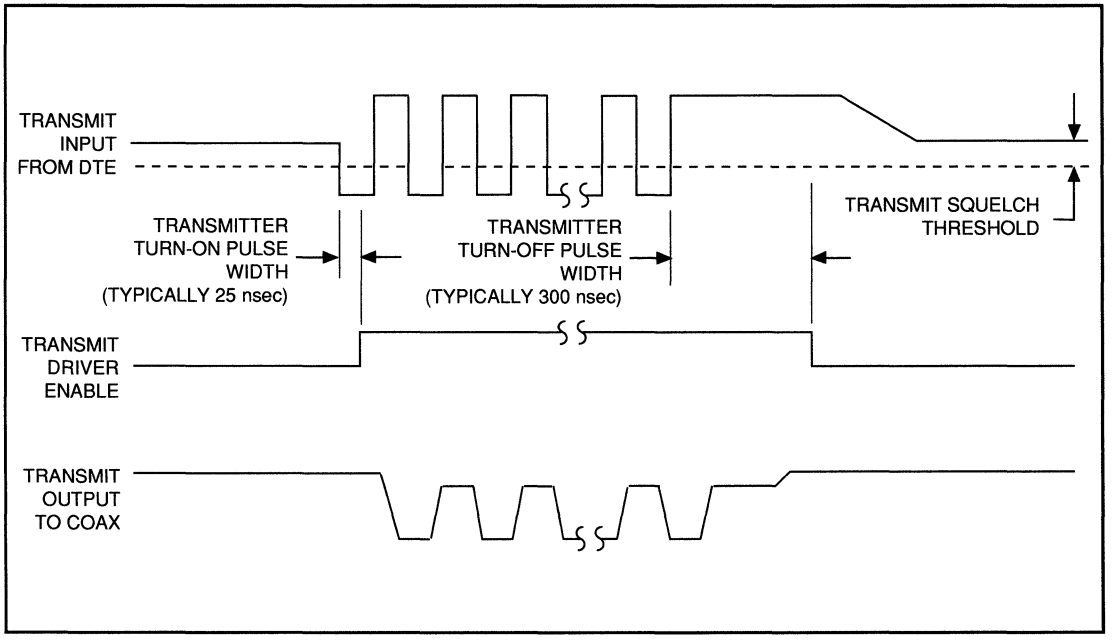


FIGURE C-8. COAXIAL TRANSCEIVER TRANSMIT TIMING

37

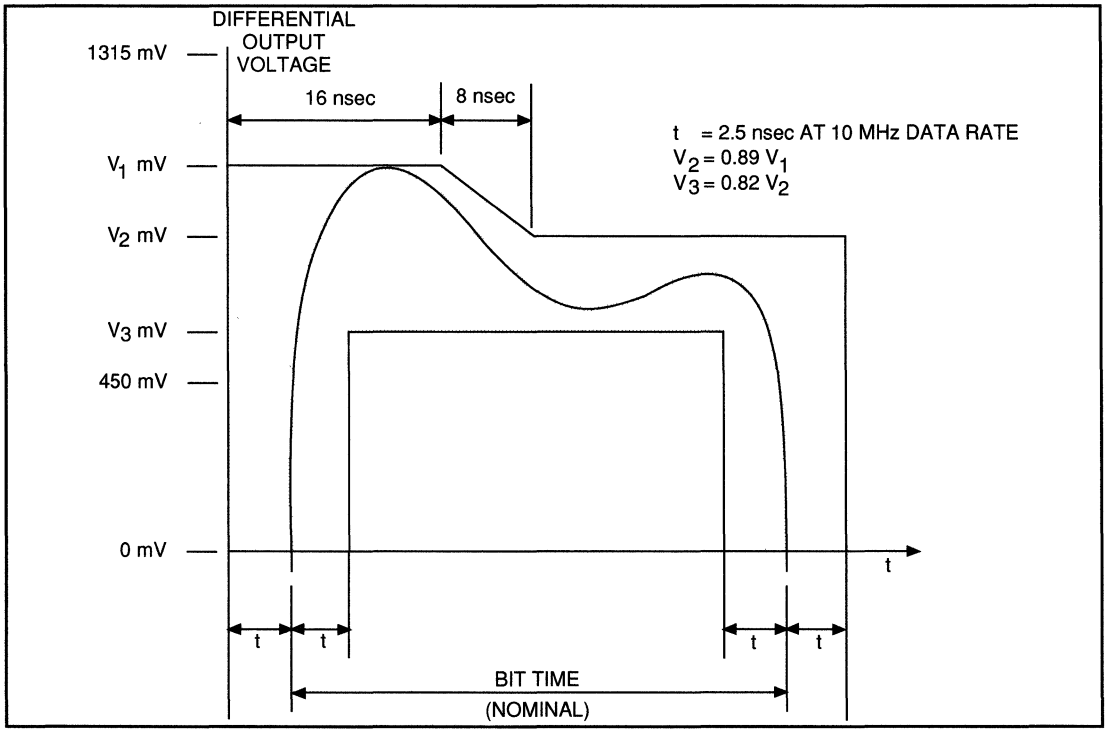


FIGURE C-9. DYNAMIC PULSE ENVELOPE

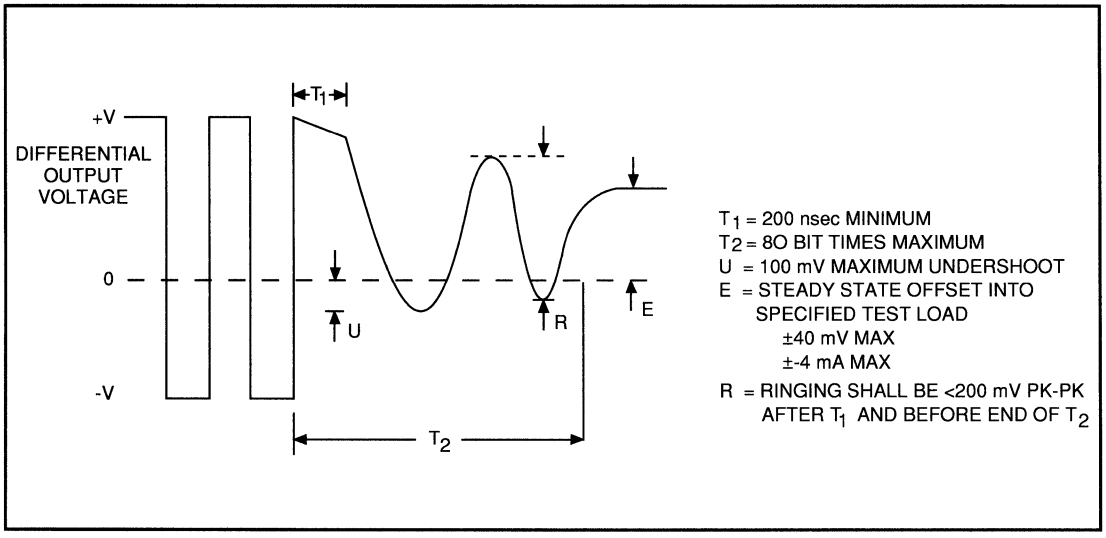


FIGURE C-10. ENABLE TO IDLE TRANSITION CD±,RX±

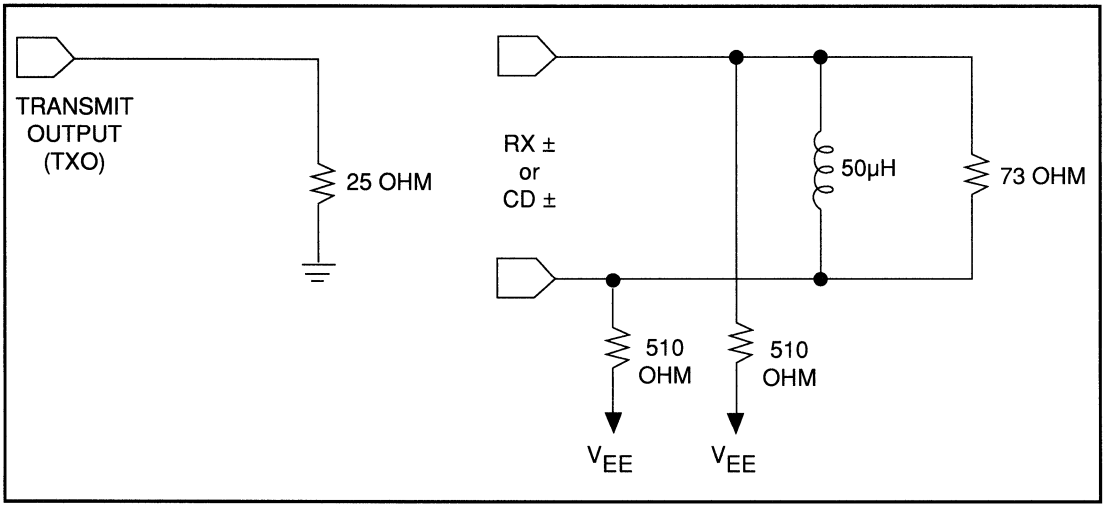


FIGURE C-11. TEST LOADS

37

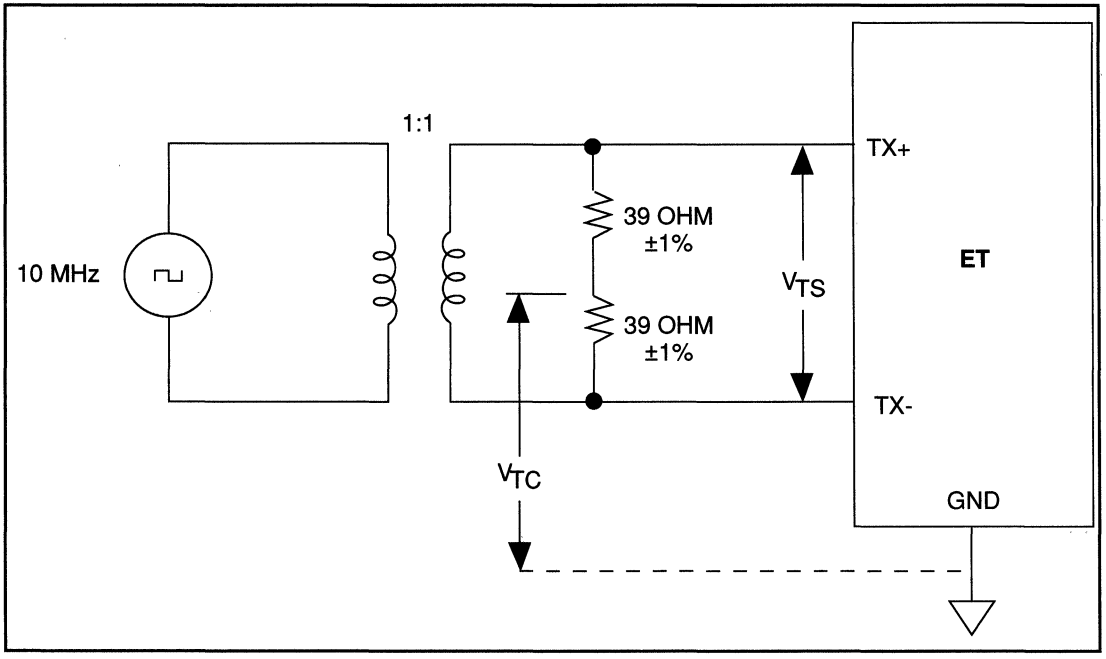


FIGURE C-12. TEST CIRCUIT FOR TX± INPUT

D.0 APPENDIX D

D.1 PACKAGE SPECIFICATIONS

Figure D-1 illustrates the 16-Pin DIP package showing dimensions in inches (and millimeters).

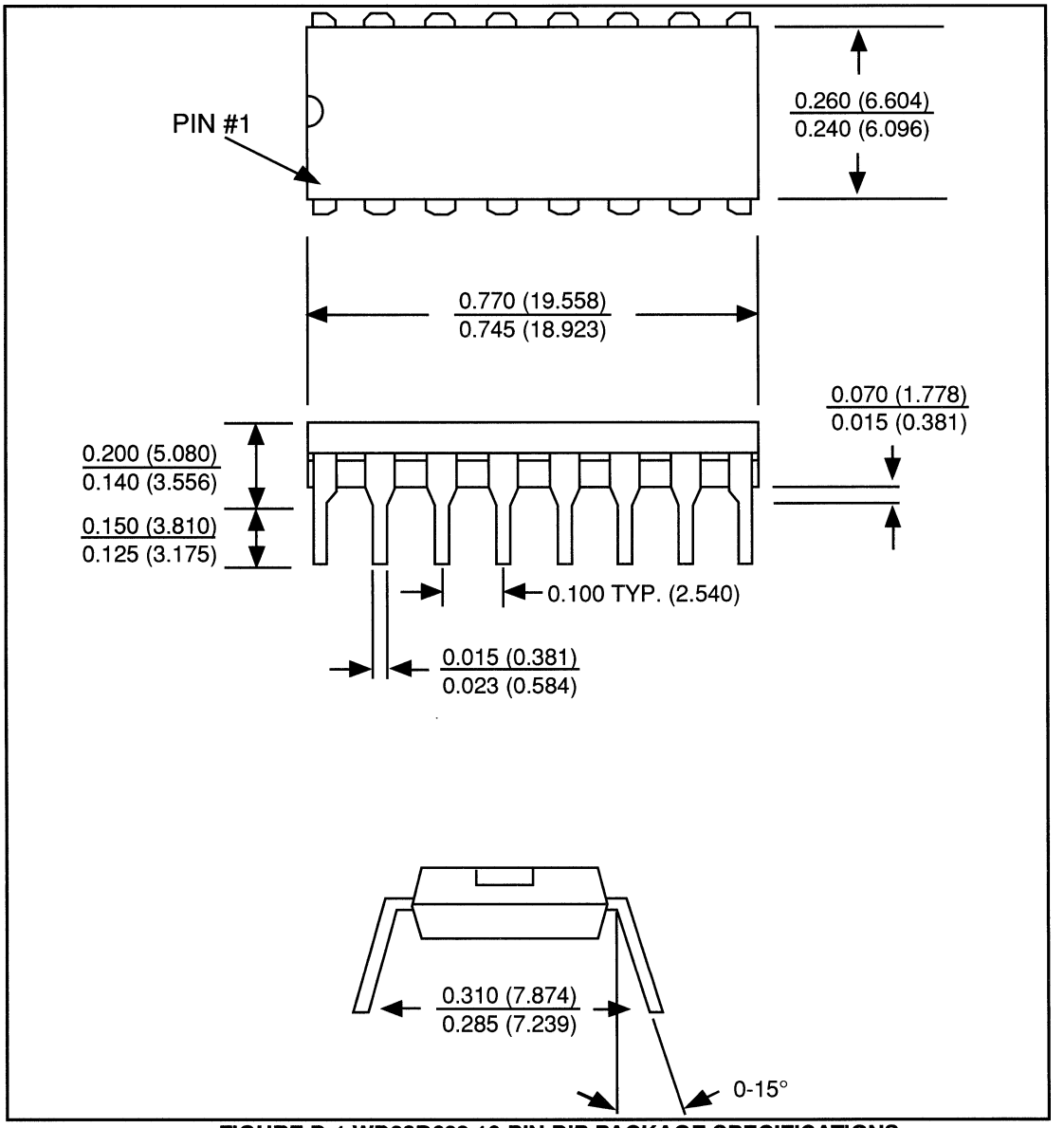


FIGURE D-1 WD83B692 16-PIN DIP PACKAGE SPECIFICATIONS

37

WD83C584

Bus Interface

Controller Device

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

APPENDICES

1.0 INTRODUCTION

1.1 DESCRIPTION

The WD83C584 is a single device bus interface controller that enables a LAN controller device to function with the standard PC XT, AT or compatible bus with minimum external logic. This device interfaces with BIOS ROM, shared memory, external EEPROM and the LAN controller. It's internal registers are automatically loaded with configuration data from the external EEPROM.

1.2 FEATURES

- Host: IBM PC/XT/AT, PS/2s, and compatibles
- Interfaces to:
  - WD83C690, 8390
  - BIOS ROM: 16, 32 or 64 Kbyte windows in memory space
  - Shared Memory
- 16-bit or 8-bit Memory Data
  - 8-bit I/O Data
- Bus Speed: Supports 8.33 MHz EISA
- SRAM Memory:
  - 8-bit: 8 or 32 Kbyte
  - 16-bit: 16 or 64 Kbyte
- Shared Memory Mapped
  - allowing 16-bit 1 wait state or 8-bit 4 wait state transfers
  - Zero Wait State on AT busses allowing 16-bit 0 wait state or 8-bit 2 wait state memory transfers
- Interfaces to external EEROM which stores:
  - I/O Address
  - Memory Address
  - Memory Size
  - BIOS ROM Address
  - Configuration
  - LAN Address
- Controls 128 Byte External EEROM

38

2.0 PIN OUTS

2.1 PIN DESCRIPTIONS

2.2.1 PC Bus Signals

PIN	NAME	DESCRIPTION
97 96 95 94 93 92 91	LA23 (I) LA22 LA21 LA20 LA19 LA18 LA17	PC LA ADDRESS BUS These input signals (unlatched) are used to address memory. They give the system up to 16 Mbyte of addressability. They are valid when BALE is high. Their purpose is to generate memory address decodes during 0 and 1 wait state memory Read/Write cycles.
19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03	SA19 (I) SA18 SA17 SA16 SA15 SA14 SA13 SA9 SA8 SA7 SA6 SA5 SA4 SA3 SA2 SA1 SA0	PC ADDRESS BUS Address lines SA 19-13 & SA 9-0 are used to decode and address memory. SA 15-13 and SA 9-0 are used for I/O addressing.
99	BALE (I)	PC ADDRESS LATCH ENABLE Used to enable address lines LA23-17 from the LA bus.
98	$\overline{\text{SBHE}}$ (I)	PC BUS HIGH ENABLE Indicates a transfer of data on the upper byte of the data bus, SD8 - SD15.
100	$\overline{\text{M16CS}}$ (0)	PC MEMORY 16-BIT CHIP SELECT Signals the system board that the present transfer is a 16-bit memory cycle. It is derived from a decode of LA23 - LA17. It is driven by a tri-state driver.
77	BIT8 (I)	PC 8-BIT BUS / 16-BIT BUS A 0 or low signal on this input indicates that the data bus is an 16-bit bus. A 1 or high signal indicates that the data bus is 8 bits.
47 46 45 44 43 42 41 40	SD7 (I/O) SD6 SD5 SD4 SD3 SD2 SD1 SD0	PC DATA BUS These signals provide the low order data bus bits. They are the PC's access to the internal registers.

TABLE 2-1. PC BUS SIGNALS

PIN	NAME	DESCRIPTION
21	CLK (I)	PC CLOCK PC system clock used to synchronize the zero wait state line when used in the 8-bit interface mode.
33	RSTDRV (I)	PC RESET Used to reset or initialize logic at power up time.
58	$\overline{IOR}$ (I)	PC I/O READ When low, this input transfers the contents of the selected I/O register onto the PC data bus.
59	$\overline{IOW}$ (I)	PC I/O WRITE When low, this input transfers the contents of the PC data bus onto the selected I/O register.
82 22	$\overline{MEMR}$ (I) $\overline{SMEMR}$ (I)	PC MEMORY READ These inputs connect to the memory read signals on the PC bus. When this signal is active, it enables data from the buffer memory onto the PC data bus. $\overline{SMEMW}$ is active only when the memory address is within the first 1 Mbyte of memory space.
81 23	$\overline{MEMW}$ (I) $\overline{SMEMW}$ (I)	PC MEMORY WRITE This input connects to the memory write signal on the PC bus. When this signal is active, it enables data on the PC bus to be stored on the buffer memory. $\overline{SMEMW}$ is active only when the memory address is within the first 1 Mbyte of memory space.
20	AEN (I)	PC ADDRESS ENABLE This input connects to the address enable signal on the PC bus. If Address Enable is active, the WD83C584 will not respond to any command.
24	IORDY (O)	PC READY I/O Channel Ready is pulled low (not ready) by a memory or I/O device to lenthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. This signal is driven by a tri-state buffer capable of sinking 24 mA.
32	$\overline{0WS}$ (O)	PC ZERO WAIT STATE Zero wait state signal tells the host processor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, $\overline{0WS}$ is derived from an address decode gated with a $\overline{MEMR}$ or $\overline{MEMW}$ command. In order to run a memory cycle to an 8-bit device with a minimum of two wait states, $\overline{0WS}$ should be driven active one system clock after the $\overline{SMEMR}$ or $\overline{SMEMW}$ command is gated with the address decode for the device. Memory Read and Write commands to an 8-bit device are active on the falling edge of the system clock. $\overline{0WS}$ is a tri-state output capable of sinking 24 mA.
90 86 87 88 89 85 84 83	IRQ2/9 (O) IRQ3 (O) IRQ4 (O) IRQ5 (O) IRQ7 (O) IRQ10 (O) IRQ11 (O) IRQ15 (O)	PC INTERRUPT REQUESTS An interrupt request is generated when INT is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request. Only one line is active at a time; all others are tri-stated.

TABLE 2-1. PC BUS SIGNALS (Continued)

38

2.2.2 LAN Signals

PIN	NAME	DESCRIPTION
37 38 39	$\overline{B0OE}$ (O) $\overline{B1OE}$ (O) $\overline{SWAP}$ (O)	PC BUFFER OUTPUT ENABLE Controls the least significant, most significant and swap byte buffers respectively.
36	BUFDIR (O)	PC BUFFER DIRECTION Provides direction control for an external data buffer. BUFDIR is "1" for writes and "0" for reads.
78	BSCK (I)	LAN CLOCK 20 MHz clock.
55	BREQ (I)	LAN BUS REQUEST Bus Request is used to request the local bus for DMA transfers. this signal is generated when the LAN controller FIFO needs servicing.
56	BACK (O)	LAN BUS ACKNOWLEDGE Bus Acknowledge indicates that the LAN controller has been granted the bus.
60	$\overline{CS}$ (O)	LAN CHIP SELECT Places the LAN in slave mode for access to LAN internal registers.
57	$\overline{ACK}$ (I)	LAN SLAVE I/O ACKNOWLEDGE Active low when LAN controller grants access to WD83C584. Used to insert wait states to WD83C584 until the LAN controller is synchronized for a register read or write operation.
54	INT (I)	LAN INTERRUPT Indicates that the LAN controller requires CPU attention after reception transmission or completion of DMA transfers.
53	$\overline{RESET}$ (O)	LAN RESET Hardware reset to the LAN controller IC.

TABLE 2-2. LAN SIGNALS

2.2.3 EEROM Signals

PIN	NAME	DESCRIPTION
50 49 48	$\overline{\text{INIT2}}$ (I) $\overline{\text{INIT1}}$ (I) $\overline{\text{INIT0}}$ (I)	EEROM INITIALIZE There are three EEPROM initialization pins. Depending on the state of these pins, the WD83C584 registers will power up from different EEROM bytes. The following table shows the bytes from which it will power up. Refer to each register to determine the value of each byte loaded at power up. One case is special, it causes the WD83C584 to its INITIAL state which overrides EEROM. (Refer to each register for their INITIAL values.) Note that the LAN ADDRESS is read from locations 40-47.

$\overline{\text{INIT2}}$	$\overline{\text{INIT1}}$	$\overline{\text{INIT0}}$	EE ADDRESS
1	1	1	00-07
1	1	0	08-0F
1	0	1	10-17
1	0	0	18-1F
0	1	1	20-27
0	1	0	28-2F
0	0	1	30-37, INITIAL CONDITION
0	0	0	38-3F

35	$\overline{\text{TEST}}$	TEST Used for factory testing. Must be pulled up to +5V with 10 Kohm, 5% resistor.
64	EECS (O)	EEROM CHIP SELECT
63	EESK (O)	EEROM CLOCK
62	EEDI (O)	EEROM DATA INPUT
61	EEDO (I)	EEROM DATA OUTPUT An external 9346 serial EEROM is used to store up to 1024 bits of EEROM data. The above signals interface to this chip. The EEROM is used to initialize registers at power up time. It takes about 2 ms to read all 16 registers after the end of the reset pulse. It takes about 200 ms to store EEROM.

TABLE 2-3. EEROM SIGNALS

38

2.2.4 RAM Signals

PIN	NAME	DESCRIPTION
71	$\overline{\text{RAMOE}}$ (O)	RAM OUTPUT ENABLE This output connects to the output enable pins on the buffer RAM.
70	$\overline{\text{RAMWR}}$ (O)	RAM WRITE ENABLE This output connects to the write enable pins on the buffer RAM.
68 69 67	$\overline{\text{RMCS0}}$ (O) $\overline{\text{RMCS1}}$ (O) RAM12 (O)	RAM0 CHIP SELECT RAM1 CHIP SELECT These outputs provide the chip select signals needed by the buffer RAMs.
66 65	MA13 (I) MA0 (I)	These inputs are connected to memory address bus. They are used for memory address decode.
73	MEM16 (O)	MEMORY 16 ENABLE Indicates the host PC to RAM access will be 16 bits wide. This output will not go active if the WD83C584 is used and programmed for 8-bit applications.
72	LAN16 (O)	LAN 16 ENABLE Indicates the LAN controller to RAM access will be 16 bits wide.

TABLE 2-4. RAM SIGNALS

2.2.5 General I/Os

PIN	NAME	DESCRIPTION
52 26 27	OUT3 (O) OUT2 (O) OUT1(O)	OUTPUTS These three output pins follow bits D1, D2 and D3 in the IRR register.
30 31	INPUT2 (I) INPUT1 (I)	INPUTS These two input pins are readable via software from IRR bits D1 and D2.

TABLE 2-5. GENERAL I/Os

2.2.6 ROM Signals

PIN	NAME	DESCRIPTION
76	$\overline{\text{ROMOE}}$ (O)	BIOS ROM OUTPUT ENABLE Chip Select for BIOS ROM. This signal gates ROM data onto the SD7-0 bus.
75 74	ROM15 (O) ROM14 (O)	ROM ADDRESS LINES These attach to the ROM address bits 15 and 14. Depending on the state of the RAM and FLSH bits, these lines do the proper addressing and write strobes for RAM and FLASH ROM.

TABLE 2-6. ROM SIGNALS

2.2.7 Voltages

PIN	NAME	DESCRIPTION
34	POWER (I)	POWER SENSING INPUT This signal is used to sense that the input power has risen to a useable level. This signal has a Schmidtt trigger input.
02,28, 79	VCC (I)	+5V (3 pins)
01,29 51,80	GND (I)	GROUND (4 pins)

TABLE 2-7. VOLTAGES

38

3.0 THEORY OF OPERATION

3.1 INITIALIZATION

Upon power-up, the WD83C584 accesses an external EEROM to set up its initial configuration. This takes about 2 milliseconds to read the data from the EEPROM into the WD83C584. After this time the BIOS ROM and I/O Ports will be enabled. The Shared Memory is always disabled upon power up, and must be enabled by software.

3.2 ARBITRATION

Arbitration for the bus is mainly between the PC and the LAN controller. The LAN controller asserts BREQ and if the bus is free, a BACK is returned. When the LAN controller has the bus, it is in complete control and must provide all RAM and interface signals. Also, access to the ROM and the internal registers on the WD83C584 must also arbitrate for the bus.

3.3 RAM BUFFER

The RAM buffer uses either 8K or 32K SRAMs. It may be either 8 bits or 16 bits wide (giving 64K maximum).

3.4 EXTERNAL EEROM

The WD83C584 accesses an external EEROM. The contents of the EEROM are loaded into the internal registers of the WD83C584 upon power up.

The use of EEROM has several advantages over a separate PROM for the LAN address. It can also reduce the number of jumpers needed on the board. It allows for reconfiguration without removing the board from the system.

Upon power up, the EEROM data is read into the WD83C584 registers. Of course, the first time the EEROM is powered up, it will have random data. The $\overline{\text{INIT}}$ inputs allow the EEROM to be set to a known initial state.

All 128 bytes of EEROM can be accessed and modified from the WD83C584. They are read into the LAN Address registers 8 bytes at a time. Once there, they can be changed and stored back into the EEPROM.

4.0 INTERNAL REGISTERS

In the following descriptions, several values of each register are given as follows:

RESET	The value during RSTDRV time.
INITIAL	If the $\overline{INIT2}$, 1, 0 pins (50,49,48) are connected such that 001 is present on these inputs, this value is loaded into the register immediately after RSTDRV time.
POWER-UP	If not in the INITIAL setting, this value is loaded into the register immediately after RSTDRV time.
RECALL	This value is loaded each time a recall is performed.
REGISTER VALUES:	? = value unknown EE = value loaded from EEROM 1 = logical 1 0 = logical 0 n/a = not used

4.1 I/O MAP

0x00	MEMORY SELECT REGISTER (MSR)
0x01	INTERFACE CONFIGURATION REGISTER (ICR)
0x02	I/O ADDRESS REGISTER (IA)
0x03	BIOS ROM ADDRESS REGISTER (BIO)
0x04	INTERRUPT REQUEST REGISTER (IRR)
0x05	LA ADDRESS REGISTER (LAAR)
0x06	INITIALIZATION JUMPERS
0x07	GENERAL PURPOSE DATA REGISTER (GP2)
0x08-0x0F	LAN ADDRESS REGISTERS (LAR)
0x10-0x1F	LAN CONTROLLER REGISTERS (LAN)

38

4.2 MEMORY SELECT REGISTER (MSR)

Offset 0x00

Upon power-up, MENB is 0. Thus the memory is disabled at power up, and will not be enabled until the MSR has been programmed with the MENB bit a "1". It is possible to program the memory select bits and the memory enable bit simultaneously.

	D7 RST	D6 MENB	D5 RA18	D4 RA17	D3 RA16	D2 RA15	D1 RA14	D0 RA13
RESET	0	0	0	0	0	0	0	0
INITIAL	0	0	EE	EE	EE	EE	EE	EE
POWER-UP	0	0	EE	EE	EE	EE	EE	EE
RECALL	EE	EE	EE	EE	EE	EE	EE	EE

BIT	NAME	DESCRIPTION
D7	RST	SOFTWARE RESET Set to 1 and then back to 0 to force a hardware reset to the LAN Controller.
D6	MENB	MEMORY ENABLE Set to 1 to enable PC access to shared memory.
D5	RA18	MEMORY ADDRESS BITS
D4	RA17	Must be set to the address at which the shared memory is to be placed. These
D3	RA16	bits correspond to system memory address bits SA18 through SA13.
D2	RA15	SA19 is assumed to be a "1". For example, address C4000 could be selected
D1	RA14	by writing 0x62 to this register. In 16-bit mode, A19 is set by the LAAR register.
D0	RA13	

4.3 INTERFACE CONFIGURATION REGISTER

(ICR) Offset 0x01, (Read/Write)

The ICR determines the configuration of the WD83C584.

	D7 STO	D6 RIO	D5 RX7	D4 RLA	D3 MSZ	D2 IR2	D1 n/a	D0 BT16
RESET	0	0	0	0	0	0	0	0
INITIAL	0	0	0	0	0	0	0	0
POWER-UP	0	0	0	0	EE	EE	EE	NA
RECALL	EE	EE	EE	EE	EE	EE	EE	NA

38

BIT	NAME	DESCRIPTION
D7	STO	NON-VOLATILE EEROM STORE Set to 1 to store registers into EEROM. The bit will be automatically reset. It takes a maximum of 200 ms for a store to take place. It will be reset when the store is complete. This bit may be polled to determine when the store operation is complete. The EEROM has a limited number of stores that can take place. The store operation should only take place at initial board configuration or at initial installation.
D6	RIO	RECALL I/O ADDRESS FROM EEROM Set to 1 to recall the I/O address from EEROM into the I/O Address Register. It will be reset when the recall is complete. This bit may be polled to determine when the recall is complete.
D5	RX7	RECALL ALL BUT I/O and LAN ADDRESS Set to 1 to recall registers with offsets 0x00 and 0x02 through 0x07. It will be reset when the recall is complete. This bit may be polled to determine when the recall is complete.
D4	RLA	RECALL LAN ADDRESS Set to 1 to recall the LAN address only from EEROM (Registers 0x08 through 0x0F). It will be reset when the recall is complete. This bit may be polled to determine when the recall is complete.
D3	MSZ	SRAM SIZE This is the physical size of the SRAM chips on the board. 0 = 8K, 1 = 32K In order to determine the RAM window in host memory, this bit must be combined with LAN16 as follows: **MSZ** **LAN16** **SIZE** 0 0 8 Kbytes 0 1 16 Kbytes 1 0 32 Kbytes 1 1 64 Kbytes
D2	IR2	Used to select the second set of IRQ lines. See IRR register.
D1	OTHER REGISTER ACCESS	This bit idetermines whether the BIOS ROM Address Register (BIO) or the EEROM Address Register (EAR) is enabled. At power up, BIO is enabled. 0 = BIO; 1 = EAR.
D0	BIT16	16-BIT BUS When the WD83C584 is used in an 8-bit interface, this bit is read/writable. When used in a 16-bit interface, it will always read a 1.

4.4 I/O ADDRESS REGISTER (IAR)

Offset 0x02, (Read/Write)

The IAR sets the I/O address of the board. If the INIT2, INIT1, INIT0 pins are "001" at power-up, the I/O address will be hard initialized at 280.

	D7 IA15	D6 IA14	D5 IA13	D4 IA9	D3 IA8	D2 IA7	D1 IA6	D0 IA5
RESET	0	0	0	0	0	0	0	0
INITIAL	0	0	0	1	0	1	0	0
POWER-UP	EE	EE	EE	EE	EE	EE	EE	EE
RECALL	EE	EE	EE	EE	EE	EE	EE	EE

BIT	NAME	DESCRIPTION
D7	IA15	I/O ADDRESS BITS
D6	IA14	Must be set to the I/O address at which you want the board to be placed. These
D5	IA13	bits correspond to system address bits SA15 thru SA13 and SA9 thru SA5.
D4	IA9	For example, address 0x280 could be selected by writing to 0x14 to this register.
D3	IA8	
D2	IA7	
D1	IA6	
D0	IA5	

Note: Address bits SA15 through SA13 can be used to select multiple boards while still taking up what is normally considered only 32 bytes of I/O space.

38

4.5 BIOS ROM ADDRESS REGISTER (BIO)

EEROM Address Register (EAR)
Offset 0x03, (Read/Write)

There are two registers at this offset. Depending on what was **last written** to ICR-D1 (OTHER) one register or the other will be accessed.

ICR-D1 = 0:BIO will be accessed
ICR-D1 = 1:EAR will be accessed.

The BIO sets the memory address of the BIOS ROM.

The ROM socket may be populated with a 64K ROM, a 32K RAM, or a 32K FLASH ROM.

	D7 RS1	D6 RS0	D5 BA18	D4 BA17	D3 BA16	D2 BA15	D1 BA14	D0 INT
RESET	0	0	0	0	0	0	0	0
INITIAL	0	0	0	1	0	1	0	0
POWER-UP	EE	EE	EE	EE	EE	EE	EE	EE
RECALL	EE	EE	EE	EE	EE	EE	EE	EE

BIT	NAME	DESCRIPTION
D7	RS1	BIOS ROM SIZE
D6	RS0	RS1 RS0 0 0 ROM cannot be accessed 0 1 16 Kbyte ROM 1 0 32 Kbyte ROM 1 1 64 Kbyte ROM
D5	BA18	BIOS ROM MEMORY ADDRESS BITS
D4	BA17	Must be set to the memory address at which you want the BIOS ROM is to be
D3	BA16	placed. These bits correspond to system memory address bits SA18 through
D2	BA15	SA13. SA19 is assumed to be a "1". For example, a 16 Kbyte ROM at
D1	BA14	D8000 could be selected by writing 0x6C to this register.
D0	INT	Setting this bit raises one of the IRQ lines to the PC. This may be used as a software interrupt. It must be reset to remove the IRQ.

4.6 EEROM ADDRESS REGISTER (EAR)

The EAR allows additional EEROM to be accessed. In order to access this register a "1" should be written to ICR-D1 (OTHER).

Operation of EEROM is as follows:

During power up or recall, 8 bytes of EEROM are loaded into the WD83C584 first 8 registers. Which 8 bytes are read depends on the position of the INIT input jumper pins. In the case that the INIT pins are all unjumpered (all 1s), bytes from 0X00 to 0X0F will be read. In all cases, these bytes will be from EEROM locations between 0X00 and 0X3F. During a store operation, the first 8 bytes are always written to the first 8 EEROM locations (0X00 through 0X07).

At power up, the EAR was set with EA6, EA5, EA4, EA3 = 1000. The next 8 bytes are read into the LAN address registers using the EAR register addresses. Thus the LAN address should be stored at 0X40.

When the ICR-D1 bit is set. This EAR register may be programmed to point at other EEROM addresses. A STO or RLA would then transfer between the LAN address registers and this other EEROM address.

During a recall, ICR-D1 bit is not changed. Also the BIOS ROM ADDRESS (BIO) is recalled to offset 3 and not this EAR. There is no EEROM backup for the EAR. During a STO, the BIO is stored.

When the ICR-D1 bit is set, the EAR is readable from the host, not the BIO.

	D7 EA6	D6 EA5	D5 EA4	D4 EA3	D3 RAM	D2 RPE	D1 RP1	D0 RP
RESET	1	0	0	0	0	0	0	0
INITIAL	1	0	0	0	0	0	0	0
POWER-UP	1	0	0	0	0	0	0	0
RECALL	EE	EE	EE	EE	EE	EE	EE	EE

BIT	NAME	DESCRIPTION
D7	EA6	EEROM ADDRESS
D6	EA5	This determines which 8 bytes will be accessed with a recall or STO store.
D5	EA4	The default 0x80 says that bytesD4 EA3 0x40-0x47 will be read into the
D4	EA3	LAN registers. A 0x10 would cause bytes 0x08-0x0F to be stored or read to or from the LAN ADDRESS registers. When ICR-D1 = 0, the EEROM Address will be reset to 0x40.
D4	RAM	RAM Indicates that a 32K RAM is installed in the ROM socket.
D2	RPE	ROM PAGE
D1	RP1	RPE enables ROM paging. The RP1 and RP0 bits determine what page of
D0	RP0	ROM will be accessed. A page is equal to 16 Kbytes. Four 16-Kbyte pages are accessible.

38

4.7 INTERRUPT REQUEST REGISTER (IRR)

Offset 0x04, (Read/Write)

The IRR controls which Interrupt Request will be used.

	D7 IEN	D6 IR1	D5 IR0	D4 FLSH	D3 OUT3	D2 OUT2	D1 OUT1	D0 OWS8
RESET	0	0	0	0	0	0	0	0
INITIAL	0	0	0	1	0	1	0	0
POWER-UP	EE	EE	EE	EE	EE	EE	EE	EE
RECALL	EE	EE	EE	EE	EE	EE	EE	EE

BIT	NAME	DESCRIPTION
D7	IEN	INTERRUPT ENABLE Enables the appropriate IRQ line onto the bus. The IRQ lines are tri-stated otherwise.
ICR-D2	IR2	INTERRUPT REQUEST
D6	IR1	These bits determine which Interrupt Request Line will be enabled. IR2
D5	IR0	is found as ICR-D2.

IR2	IR1	IR0
0	0	0 IRQ2/9
0	0	1 IRQ3
0	1	0 IRQ5
0	1	1 IRQ7
1	0	0 IRQ10
1	0	1 IRQ11
1	1	0 IRQ15
1	1	1 IRQ4

D4	FLSH	FLASH MEMORY This says that a 32K flash memory is in the ROM socket. It may be written to.
D3	OUT3	OUTPUT PINS
D2	OUT2	The three output pins follow the data stored on these bits.
D1	OUT1	
D0	0WS8	8-BIT ZERO WAIT STATE ENABLE If set to 0: Zero Wait State disabled . Every memory byte access will include 4 states. If set to 1: Zero Wait State enabled, 2 wait states will be included with every memory byte access.

4.8 LA ADDRESS REGISTER (LAAR)

Offset 0x05 (Read/Write)

The LA address bits are used to decode the high order memory address when operating in 16-bit memory access mode. This register contains the LA bits which the memory will be compared against. This register has LA address bits LA23-19. Bits A18 and A17 are selected in the Memory Address register.

	D7 M16EN	D6 L16EN	D5 OWS16	D4 LA23	D3 LA22	D2 LA21	D1 LA20	D0 LA19
RESET	0	0	0	0	0	0	0	1
INITIAL	0	0	0	0	0	0	0	1
POWER-UP	0	EE	EE	EE	EE	EE	EE	EE
RECALL	0	EE	EE	EE	EE	EE	EE	EE

BIT	NAME	DESCRIPTION
D7	M16EN	ENABLE 16 BIT MEMORY ACCESS Set to 1 to enable 16-bit memory access. This bit should only be set when all other interrupts have been disabled.
D6	L16EN	ENABLE 16 BIT LAN OPERATION Set to 1 to allow 16-bit operation between the LAN controller and the on-board RAM memory. This bit has another function, when operating in 8 bit mode only 8K byte RAM will be used. In 16-bit mode, the entire RAM (either 16K byte or 64K byte) will be available.
D5	0WS16	0WS 16 ENABLE Enable zero wait state operation when running 16 bit memory accesses.
D4-0	LA23-19	LA MEMORY DECODE BITS Must be set to select the address at which the shared memory is to be accessed. These bits correspond to system memory address bits LA23 through LA19. For example, to select and enable base address register D0000, write a 0x01 to this register and 0x68 to the memory address register.

4.9 INITIALIZE JUMPER REGISTER

Offset 0x06 (Read)

PIN	NAME	DESCRIPTION
D7		Undefined, will read a "0".
D6	IN2	INPUT PINS
D5	IN1	These bits read the state of the 2 input pins.
D4,3		Undefined, will read a "0".
D2	INIT2	INITIALIZE PINS
D1	INIT1	These read the contents of the 3 initialize pins. They are active low.
D0	INIT0	

4.10 GENERAL PURPOSE REGISTER 2 (GP2)

Offset 0x07 (Read/Write)

The GP2 is a byte register which is completely undefined and may be used as needed by software.

	D7	D6	D5	D4	D3	D2	D1	D0
RESET	?	?	?	?	?	?	?	?
INITIAL	EE	EE	EE	EE	EE	EE	EE	EE
POWER-UP	EE	EE	EE	EE	EE	EE	EE	EE
RECALL	EE	EE	EE	EE	EE	EE	EE	EE

38

4.11 LAN ADDRESS REGISTERS (LAR)

Offset 0x08-0x0F

The LAN Address Registers contains the unique LAN address that has been assigned to a board. It should be read and written to the LAN controller. Bytes of the LAN address may be read at the offsets given below.

	D7	D6	D5	D4	D3	D2	D1	D0
RESET	?	?	?	?	?	?	?	?
INITIAL	EE	EE	EE	EE	EE	EE	EE	EE
POWER-UP	EE	EE	EE	EE	EE	EE	EE	EE
RECALL	EE	EE	EE	EE	EE	EE	EE	EE

OFFSET	DESCRIPTION
0x08	Globally Assigned Address Block (LSB)
0x09	Globally Assigned Address Block
0x0A	Globally Assigned Address Block (MSB)
0x0B	Unique Board Address (LSB)
0x0C	Unique Board Address
0x0D	Unique Board Address
0x0E	WD Board ID Byte
0x0F	Checksum, causes the twos complement sum of all 8 LAN Address Register bytes to be 0xFF.

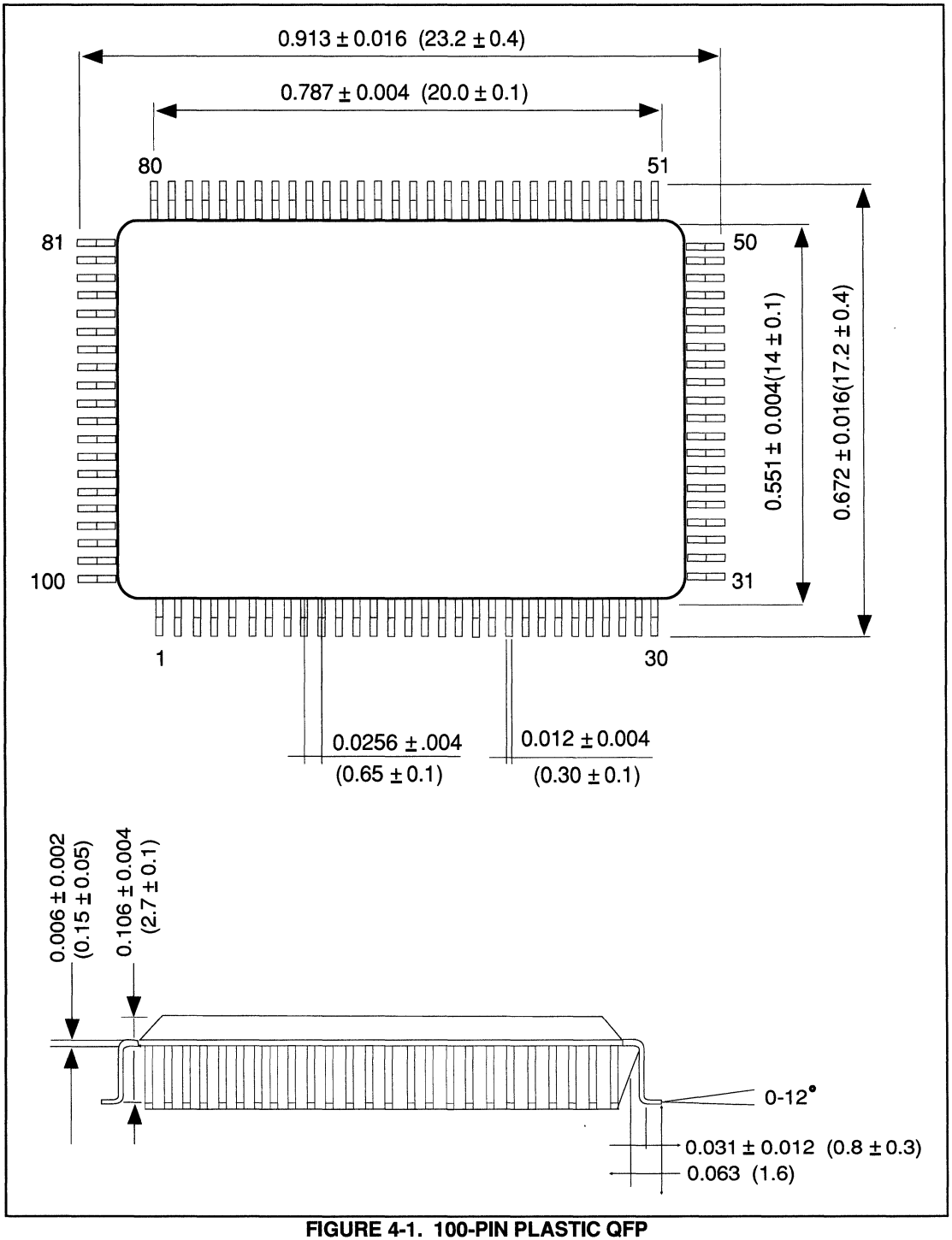


FIGURE 4-1. 100-PIN PLASTIC QFP

38

5.0 TIMING DIAGRAMS

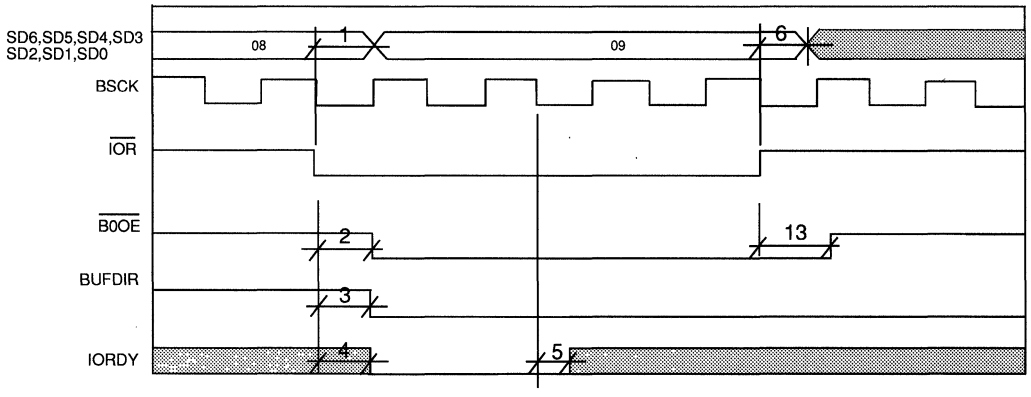


FIGURE 5-1. I/O READ

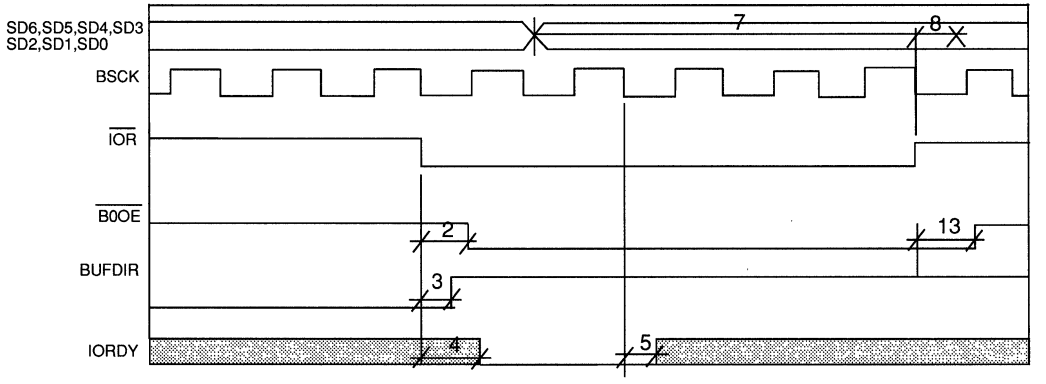


FIGURE 5-2. I/O WRITE

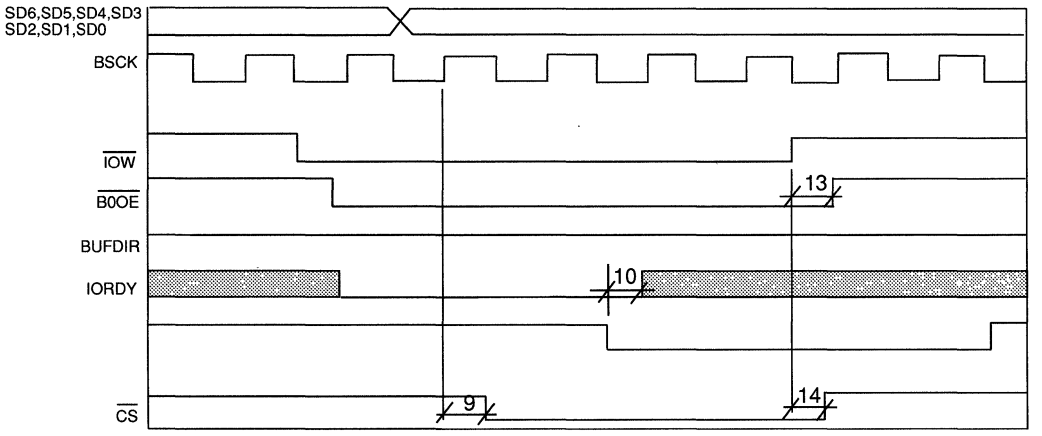


FIGURE 5-3. I/O WRITE TO LAN CONTROLLER

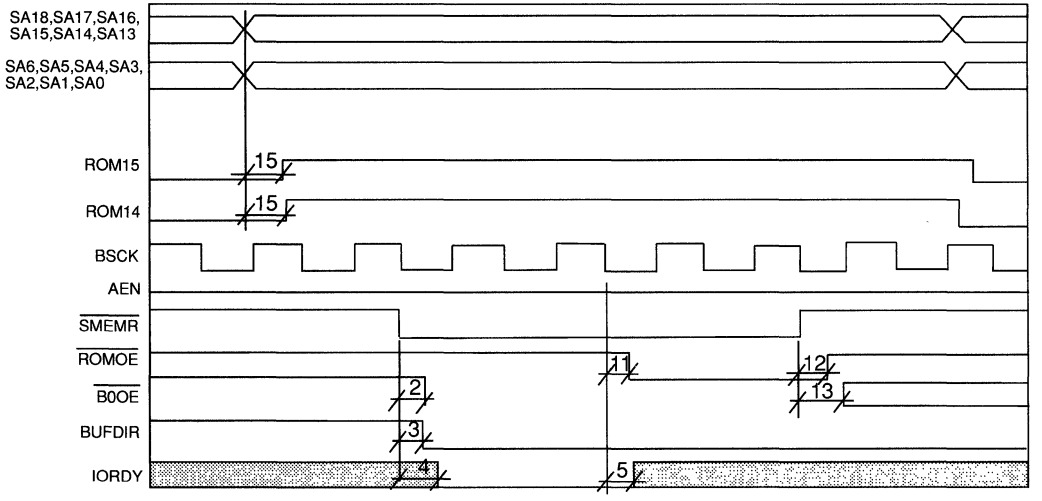


FIGURE 5-4. ROM READ

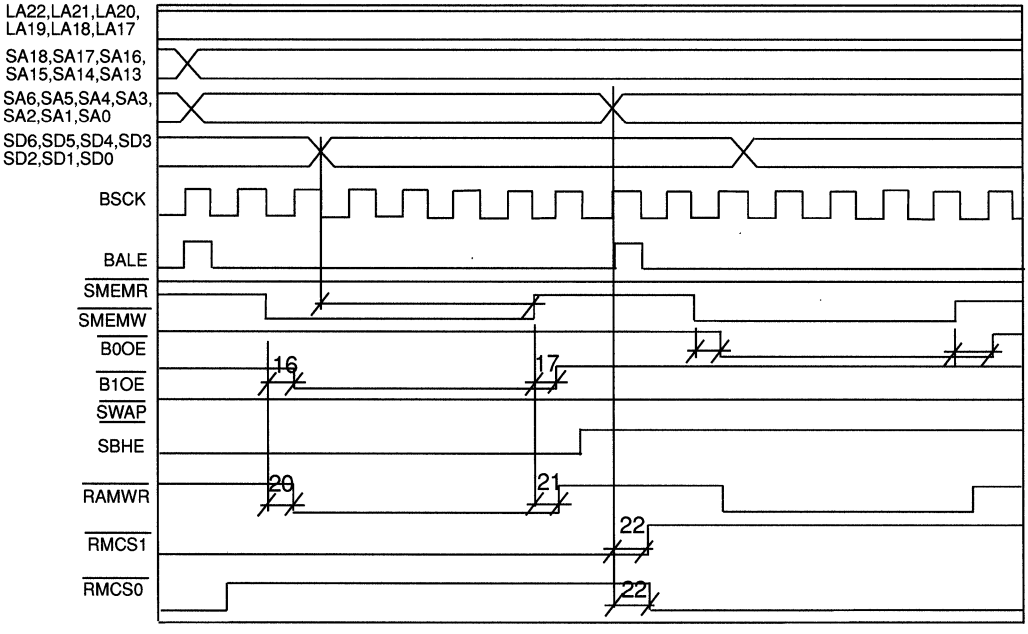


FIGURE 5-5. RAM WRITE, 8 BIT

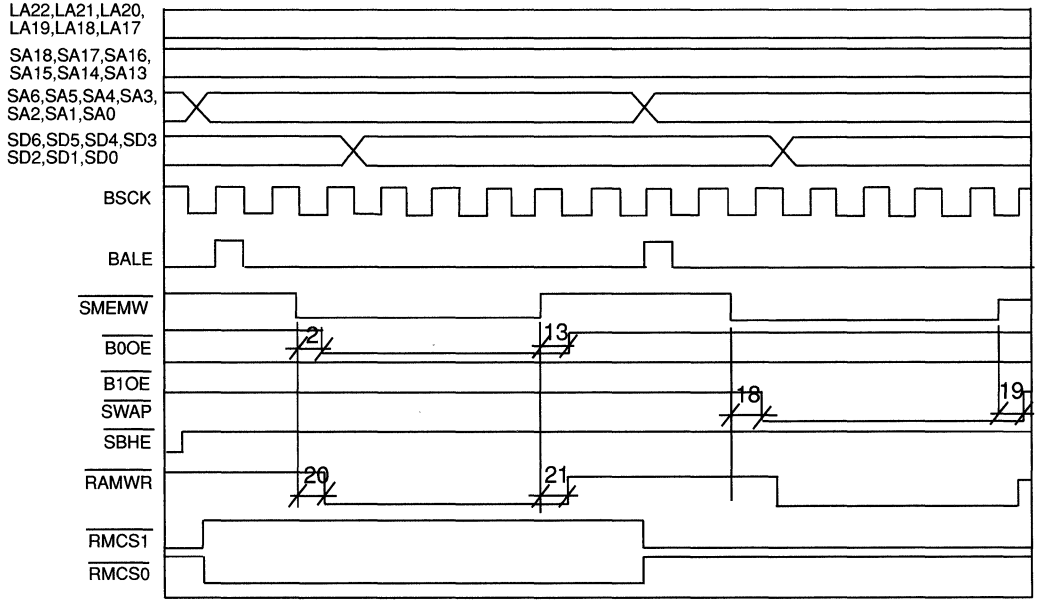


FIGURE 5-6. RAM WRITE, 8 BIT

38

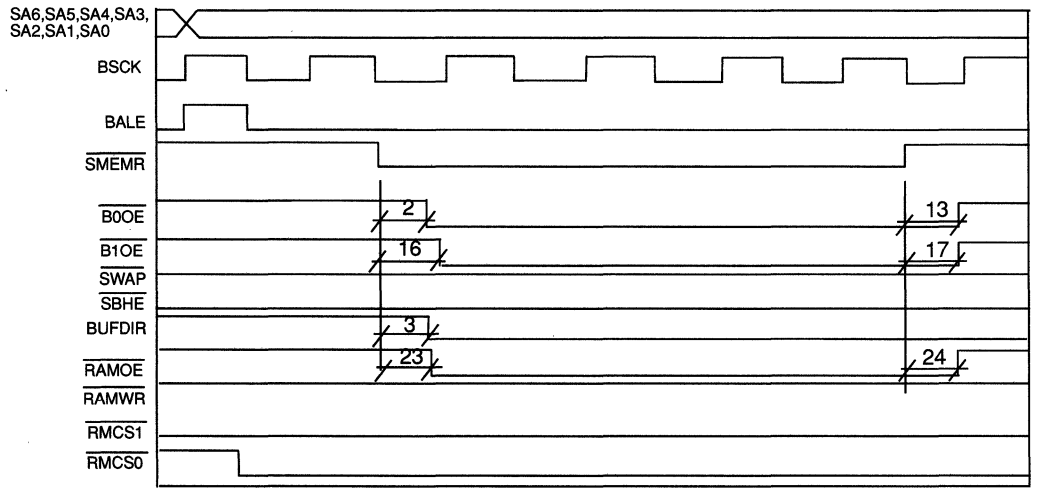


FIGURE 5-7. RAM READ, 16 BIT

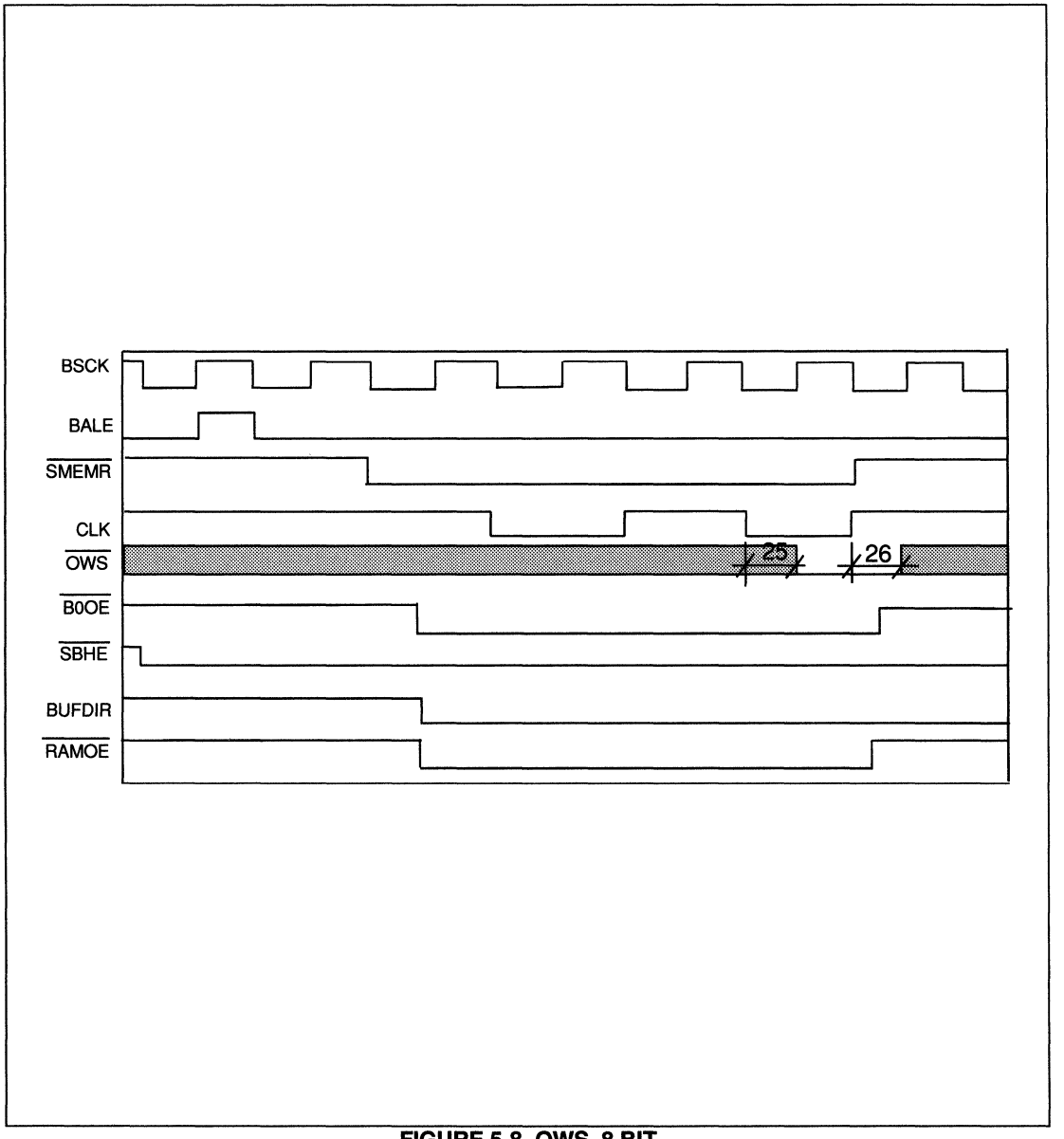


FIGURE 5-8. OWS, 8 BIT

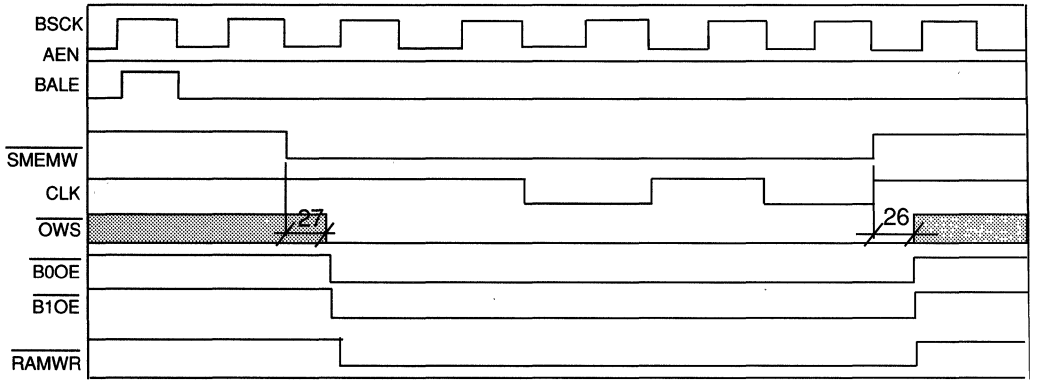


FIGURE 5-9. OWS, 16 BIT

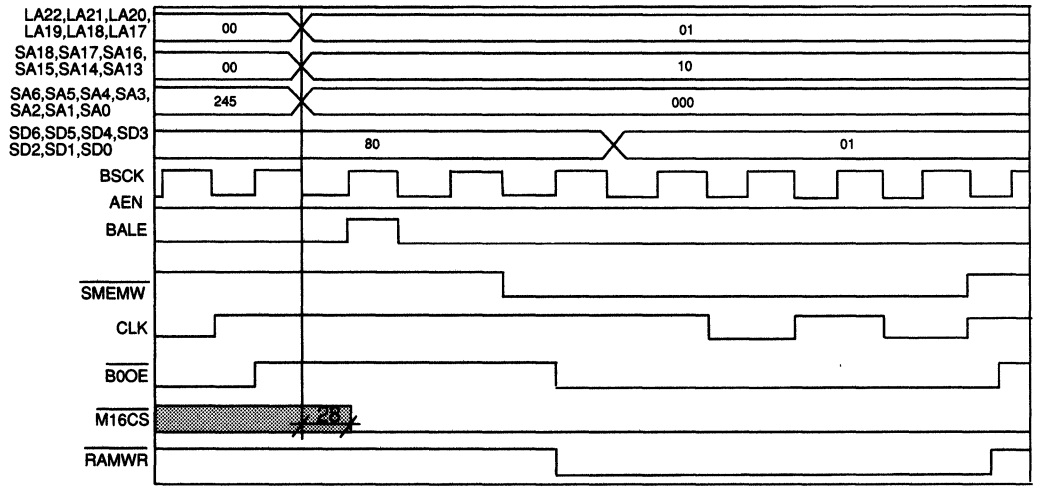


FIGURE 5-10. M16CS

38

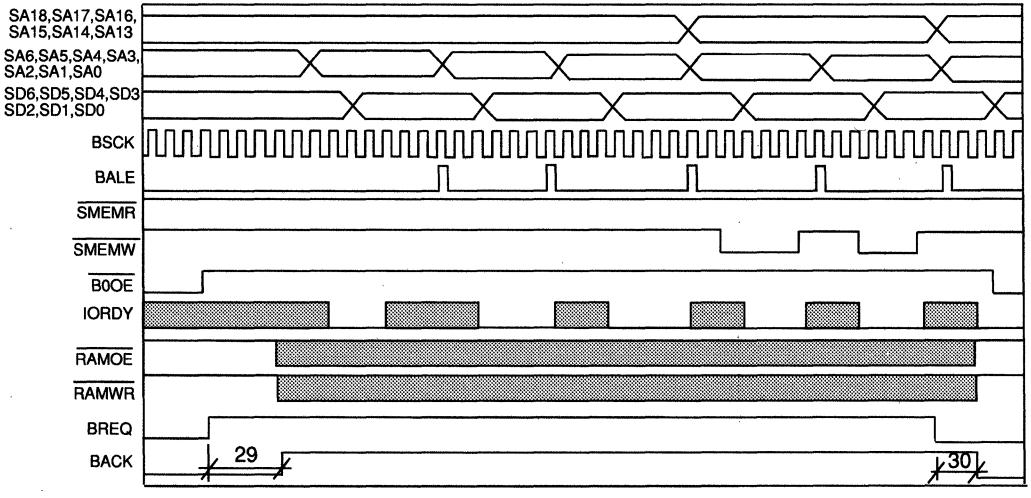


FIGURE 5-11. BREQ/BACK

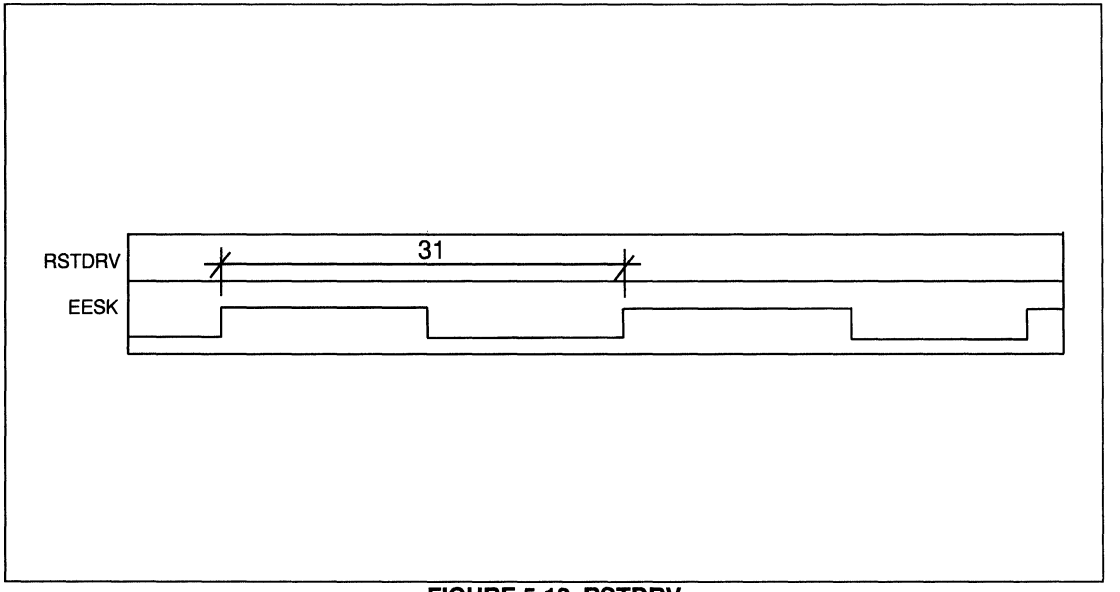


FIGURE 5-12. RSTDRV

t	DESCRIPTION	MIN	TYP	MAX
1	Read/Write Strobe to data valid	11		26 ns
2	Read/Write Strobe to $\overline{\text{BOOE}}$ low	8		21
3	Read/Write to BUFDIR change	9		17
4	Read/Write to IORDY low	9		23
5	BSCK to IORDY tri-state	14		34
6	Read Strobe to Data tri-state	6		17
7	Register Write Data Setup	5		
8	Register Write Data Hold			18
9	BSCK to $\overline{\text{CS}}$ low	12		30
10	ACK to IORDY tri-state	7		16
11	BSCK to $\overline{\text{ROMOE}}$ low	12		29
12	Read Strobe to $\overline{\text{ROMOE}}$ high	6		13
13	Read/Write Strobe to $\overline{\text{BOOE}}$ high	8		20
14	Read/Write Strobe to $\overline{\text{CS}}$ high	6		14
15	Address to ROM15, ROM14 change	7		18
16	Read/Write Strobe to $\overline{\text{B1OE}}$ low	8		19
17	Read/Write Strobe to $\overline{\text{B1OE}}$ high	8		21
18	Read/Write Strobe to $\overline{\text{SWAP}}$ low	9		23
19	Read/Write Strobe to $\overline{\text{SWAP}}$ high	10		24
20	Write Strobe to $\overline{\text{RAMWE}}$ low	6		16
21	Write Strobe to $\overline{\text{RAMWE}}$ high	6		15
23	Read Strobe to $\overline{\text{RAMOE}}$ low	12		16
24	Read Strobe to $\overline{\text{RAMOE}}$ high	6		14
25	CLK to $\overline{\text{OWS}}$ (8 bit) low	8		20
26	Read/Write Strobe to $\overline{\text{OWS}}$ tri-state	11		27
27	Read/Write Strobe to $\overline{\text{OWS}}$ (16 bit) low	7		17
28	Address to M16CS low	8		19
29	BREQ to BACK high	250		
30	BREQ to BACK low	50		
31	ESCK Period		6400	

TABLE 5-1. WD83C584 TIMING

APPENDIX A - SOFTWARE COMPATIBILITY

Compatibility of the WD83C584 with previous products is especially important. This section describes in what areas the WD83C584 is incompatible with the previous WD83C583. These incompatibilities are minor and should require little or no software changes. Changes to be made will be related to setup programs, since they are used to set up and configure the EEPROM data.

- The WD83C584 requires 2 ms to read all 16 registers after power-up or a RECALL instruction. Register 0x01 may be polled to determine the finish of this read. The WD83C583 reads its internal EEPROM within 5 ms.
- The WD83C584 requires 200 ms to store EEPROM and may be polled to determine finish, whereas the WD83C583 required 20 ms and gave no indication of finish.
- MSZ (ICR-D#) on the WD83C584 shows SRAM size, not total RAM size.
- ICR-D@ on the WD83C584 is used as IR2. It was DMA on the 83C583 and was always a 0.
- ICR-D0 on the WD83C584 is 16BIT. ITs function has totally changed. In the 83C583, it was WTS.
- IRR-D2 and D1 on the WD83C584 are not used. They were effectively not used in the 83C583.
- The user can select 1 of 8 groups of 8 bytes each to be loaded into the WD83C584 from the EEPROM at power up. To be compatible with previous WD83C583 setup programs, the WD83C584 setup program will need to be modified so that 1of the 8 groups represents the setup data used with the previous WD83C583 device.

38

APPENDIX B - ELECTRICAL OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
I_{dd}	VDD Supply Current			40	mA	
V_{dd}	Voltage Supply	4.75	5	5.75	V	
V_{ih}	Input High Voltage	2.0			V	
V_{il}	Input Low Voltage				V	
V_{ils}	Input High Voltage (Schmitt)	2.5	20,21,33 34,99	0.6		
V_{ihs}	Input Low Voltage (Schmitt)	2.5	20,21,33 34,99	0.6		
V_{oh}	Output High Voltage	V_{dd}-.4			V	I_{oh} = -2mA
V_{ol}	Output Low Voltage			V_{ss}+.4	V	I_{ol} = 6mA
V_{olc}	Output Low Voltage (Open Collector)			V_{ss}+.4		I_{ol}=24mA
I_{l}	Input Leakage Current	-10		10	µA	V_{ih}=V_{dd}
I_{oz}	Tristate High Current	-10		10	µA	V_{in}=V_{dd}
R_{pu}	Pull-up Resistor	-50	21,34,35 48,49,50 77,81,82 91-99	500	K	

TABLE B-1. DC PARAMETER CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Storage Temperature	-65		150	Deg.C
Voltage on any pin with respect to Vss	-0.6		Vdd+0.3	Volts
Voltage on Vcc with respect to Vss			7.0	Volts

TABLE B-2. NON-OPERATIONAL SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNIT
Ambient Temperature	0	25	70	Deg.C
Humidity	10		95	Percent

TABLE B-3. OPERATIONAL SPECIFICATIONS

WD83C593

Micro Channel Bus Interface

Controller Device

WESTERN DIGITAL

TABLE OF CONTENTS

FIGURES

TABLES

1.0 DESCRIPTION AND APPLICATION

The WD83C593 is a Micro Channel bus interface controller designed for non-intelligent Ethernet or StarLAN boards. The device is used as an interface to the LAN controller, BIOS ROM, buffer RAM (which functions as shared memory), and the host Micro Channel bus.

1.1 FEATURES

- Direct interface between a non-intelligent Ethernet or StarLAN LAN controller and a Micro Channel bus
- Ten bytes of internal electrically erasable programmable read only memory (EEPROM)
- 84-pin ASIC, 2.0 micron CMOS technology
- Programmable BIOS ROM size (16, 32, or 64 Kbytes)
- Programmable RAM size (16 or 64 Kbytes)
- Single, 5V power supply
- Four Vcc, ground, and program-selectable IRQ pins
- Testable/programmable before and after assembly

1.2 THEORY OF OPERATION

The WD83C593 non-intelligent interface device connects the Micro Channel bus (as a non-DMA slave) to the LAN controller, BIOS ROM, and buffer RAM. The WD83C593 satisfies all necessary interface requirements, performs all decoding for local I/O and memory spaces, and generates the necessary chip select control and handshake signals.

In order for the WD83C593 non-intelligent Micro Channel bus interface device to function properly, the mode select pin must be left open (internally pulled high).

This enables the WD83C593 to arbitrate between the host and WD83C690 LAN controller for the BD00-BD15 data bus. During local WD83C690 DMA bursts in and out of the buffer RAM, the device isolates the BD data bus from the Micro Channel via external buffering, and prevents the host from intervening until the process is complete. When a valid decode occurs, the device negates the CDCHRDY signal.

The remainder of the time, the device enables the external buffers so that the host can perform memory or I/O cycles (anywhere on the card). The host uses a 16-bit wide "move" string operation to transfer data to and from the buffer RAM. During this time, the WD83C593 generates the RAM control signals (tri-state during local RAM accesses).

2.0 POS REGISTERS AND DECODING

Designers of Micro Channel adapters are required by the Micro Channel architecture to use two read-only ID bytes and (up to) six read/write programmable option select (POS) registers. This arrangement accomplishes the following:

- eliminates switches and jumpers
- permits the installation of multiple identical cards
- allows the identification of any card by slot
- resolves resource assignment conflicts

Designers are also required to provide an adapter description file (.ADF) that reports the contents of the ID bytes, the number of POS registers used on the card, their purpose and contents, and their "alternate contents."

The Micro Channel bus defines the architecture of the following bits:

POS[2] bit 0.....Card enable (address 102h)

POS[5] bit 7.....CH CK active indicator (105h)

POS[5] bit 6.....CH CK status available indicator (105h)

The remaining POS registers are "free form" and can be used for space decoding, establishing arbitration levels, and so on. When the system is reset, each adapter must turn off the card enable bit, which in turn disables all outputs from the card, including the interrupt request lines.

The central configuration software checks all slots independently for ID bytes, and uses the .ADF files provided to resolve conflicts and set up the POS registers. It is during this time only that the POS registers can be accessed, and they can be accessed only by the configuration software.

The $\overline{\text{CDSETUP}}$ line, together with the least significant three address lines, is used for decoding POS register accesses.

2.1 Space Decodings

Three POS registers, POS[2], POS[3], and POS[4], are used to decode the card I/O space, shared RAM space, and BIOS ROM space, respectively. The mode select pin, as indicated previously, must be left open.

2.1.1 POS[2] Register

Bit	Bit Assignment
7	LA11
6	LA10
5	LA09
4	LA08
3	LA07
2	LA06
1	LA05
0	CDEN

If a 29h is written in POS[2], the WD83C593 I/O space is placed in the range 280h - 029Fh. This is one of 128 possible 32-Kbyte ranges. For each of the primary and alternate choices, one or more interrupt levels are defined in the .ADF file.

Bit (7:1)

These bits are used to decode the I/O space for the application.

Bit 0

Card Enable.
Bit 0 wakes up low and, until it is set by the configuration routine, keeps the card in "sleep" mode.

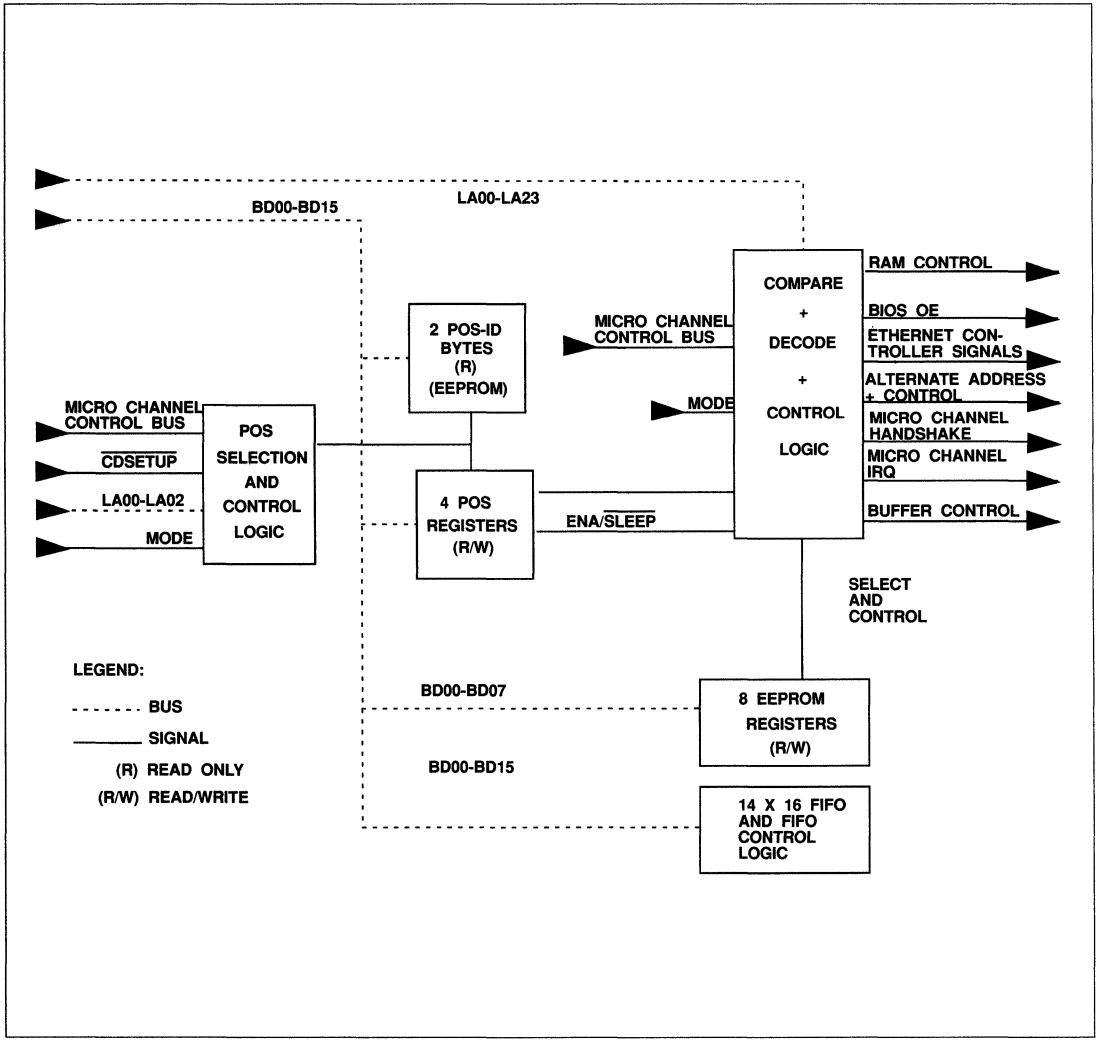


FIGURE 2-1. GENERAL SYSTEM BLOCK DIAGRAM

39

2.1.2 POS[3] Register

Bit	Bit Assignment
7	LA19
6	LA18
5	LA17
4	LA16
3	LA15
2	LA14
1	PME
0	CLAIM

If a C2h is written in POS[3], the shared RAM space is placed in the range 0C0000h - 0C3FFFh. This is one of 64 possible 16-Kbyte ranges. It is intended to place shared RAM in the general range, 0C0000h - 0DFFFFh.

Bit (7:2)

These bits are used to set the shared RAM space for the application.

Bit (1:0)

Memory Enable; Claim.
Bit 1 wakes up low and, until it is set by the configuration routine, keeps the RAM buffer disabled. Bit 0 is provided for use by the driver software (to identify availability when multiple cards are used in the same system).

2.1.3 POS[4] Register

Bit	Bit Assignment
7	LA19
6	LA18
5	LA17
4	LA16
3	LA15
2	LA14
1	BE1
0	BE0

If a D0h is written in POS[4], the BIOS ROM space is placed in the range 0D0000h - 0D3FFFh. This is one of 64 possible 16-Kbyte ranges. It is intended to place the BIOS ROM in the general range, 0C0000h - 0DFFFFh.

Bit (7:2)

These bits are used to set the BIOS ROM location for the application.

Bit (1:0)

BIOS Size/Enable.
Bits 1 and 0 are used to set the size of the BIOS ROM and, when necessary, to disable it as follows:

BE1	BE0	FUNCTION
0	0	BIOS is 16 Kbytes
0	1	BIOS is 32 Kbytes
1	0	BIOS is Disabled
1	1	BIOS is 64 Kbytes

2.2 Other POS Functions ! POS[5] Register

POS[5] provides bits that increase memory size, divide the BSCK clock by "2" (for internal use), and enable /disable interrupts to the host.

Bit	Bit Assignment
7	CH CK
6	CH CK
5	N/A
4	N/A
3	MSE
2	CDIV
1	IEN1
0	IEN0

Bit (7)

Active Indicator (Micro Channel defined).

Bit (6)

Status Available Indicator (Micro Channel defined).

Bit (5:4)

Not applicable.

Bit 3

Memory Size Enable.
When set to "1", this bit increases the memory size from 8 x 16 Kbytes to 32 x 16 Kbytes.

Bit 2

Clock Divider.
This bit, when reset, divides the BSCK clock by "2" for internal use. When the system is powered off, the bit is reset.

Bit (1:0)

Interrupt Enable.
Together, these bits enable/disable the interrupts to the host, and determine the level of the interrupt as follows.

IEN1	IEN0	FUNCTION
0	0	Interrupt level is IRQ0
0	1	Interrupt level is IRQ1
1	0	Interrupt level is IRQ2
1	1	Interrupt level is IRQ3

39

3.0 PROGRAMMING THE EEPROM REGISTERS

The WD83C593 contains ten, internal eight-bit registers implemented in EEPROM technology (see Table B-2). These registers contain random data when the device is shipped from the factory and must be programmed by you for your application. If they are not, the device will not function properly.

To initially program the EEPROM registers, you must write the data to be sorted to each register. Figure 3-1 illustrates a typical EEPROM register bit cell. Data is stored in the latch and its output is presented to the input of the EEPROM cell. Once the data is stored in the registers, you must write the following to the EEPROM control register: A5h (followed by) 00h. It is important that you write the numbers in the order given. This starts the programming process of all ten EEPROM registers with data stored in the latches. The program operation requires a maximum of 20 milliseconds to complete. During this time, it is important that you do not access any of the registers in the device. Refer to Appendix B for more information on the EEPROM registers.

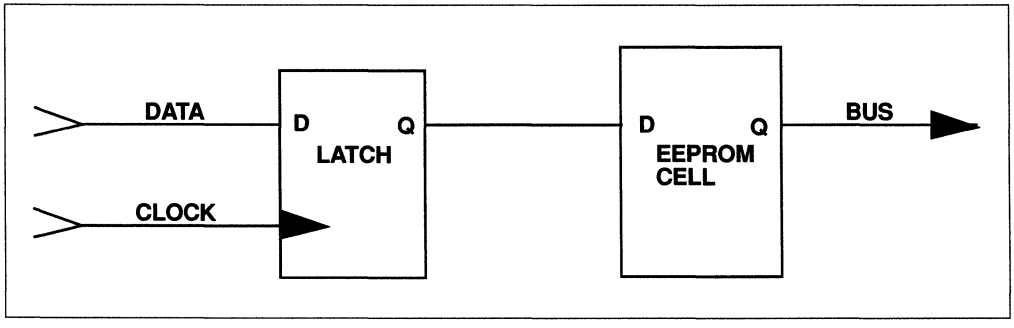


FIGURE 3-1. TYPICAL EEPROM REGISTER BIT CELL

APPENDIX A -- PIN DESIGNATIONS

Figure A-1 illustrates the 84-pin PLCC device.
Table A-1 lists all pin designations.

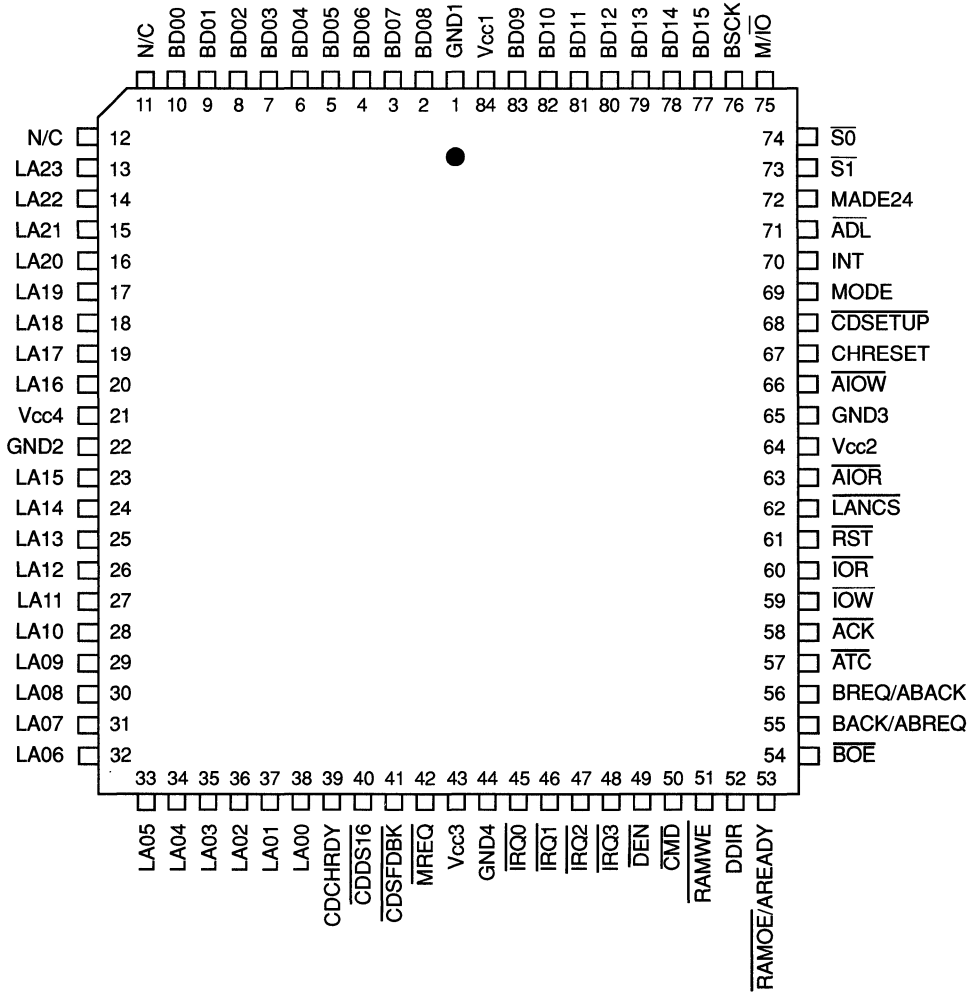


FIGURE A-1. 84-PLCC PINOUT

39

PIN NO.	PIN NAME	SIGNAL NAME/ DESCRIPTION
Host Micro Channel Bus Signals		
2-10 77-83	BD00-BDI5 (I/O)	HOST MICRO CHANNEL DATA BUS: This bus needs to be externally buffered.
11	$\overline{\text{REFRESH}}$ (I)	REFRESH CYCLE: Input from host system. Indicates when a system memory refresh cycle is taking place.
15-20 23-38	LA00-LA21 (I)	HOST MICRO CHANNEL ADDRESS LINES: These are the 20 bits of the host Micro Channel address lines.
39	CDCHRDY (O)	CHANNEL READY: This output, normally active, is pulled inactive to allow additional time to complete a channel operation.The maximum time that this line can be held inactive is 3.5 µsec.
40	$\overline{\text{CDDS16}}$ (O)	CARD DATA SIZE 16: This output is used to indicate to the host Micro Channel that the current data transfer is 16 bits wide. It is derived from a valid address decode.
41	$\overline{\text{CDSFDBK}}$ (O)	CARD SELECTED FEEDBACK: This output is asserted as an acknowledgement when an I/O or memory device on the LAN card is selected.
45-48	$\overline{\text{IRQ}}$0-3 (O)	INTERRUPT REQUEST: These outputs tell the host micro-processor that an interrupt has occurred and the LAN card needs attention.
50	$\overline{\text{CMD}}$ (I)	COMMAND: This input is used to define when data is valid on the data bus. The trailing edge of the signal indicates the end of the bus cycle.
67	CHRESET (I)	CHANNEL RESET: This signal is generated by the host when the host Micro Channel is powered up.
68	$\overline{\text{CDSETUP}}$ (I)	CARD SETUP: This input is generated by the host logic to individually select channel connectors during system configuration and error recovery procedures. This input, together with LA0-LA2, is used to access the POS registers. The $\overline{\text{CDSFDBK}}$ output is not asserted during configuration.

TABLE A-1. PIN DESCRIPTIONS

PIN NO.	PIN NAME	SIGNAL NAME/ DESCRIPTION
Host Micro Channel Bus Signals, Cont.		
71	$\overline{ADL}$ (I)	ADDRESS DECODE LATCH: This input is used to indicate that the Micro Channel addresses are to be latched. The trailing edge is used.
72	MADE24 (I)	MEMORY ADDRESS ENABLE 24: This input, when active, indicates that an unextended address space equal to or less than 16M is present on the address bus.
74, 73	$\overline{S0}$, $\overline{S1}$ (I)	STATUS BITS 0 AND 1: These inputs indicate the start of a channel cycle and also define the type of channel cycle as follows. M/$\overline{IO}$ $\overline{S0}$ $\overline{S1}$ TYPE 0 0 0 Reserved A 0 0 1 I/O Write 0 1 0 I/O Read 0 1 1 Reserved B 1 0 0 Reserved C 1 0 1 Memory Write 1 1 0 Memory Read 1 1 1 Reserved D
75	M/$\overline{IO}$ (I)	MEMORY/$\overline{INPUT\ OUTPUT}$: This input distinguishes a memory cycle from an I/O cycle.
LAN Controller Signals		
55	BACK/ABREQ (O)	LAN BUS ACKNOWLEDGE: This output is generated to acknowledge a LAN BUS REQUEST.
56	BREQ/ABACK (I)	LAN BUS REQUEST: This input is generated by the LAN controller to indicate that a DMA transfer is needed. It is automatically generated when the LAN controller's FIFO buffers need servicing.
58	$\overline{ACK}$ (I)	LAN SLAVE I/O ACKNOWLEDGE: This input is asserted by the LAN chip when it grants access to its internal registers. The input is used to insert wait states until the LAN is synchronized for a register read or write operation.
59	$\overline{IOW}$ (O)	LAN I/O WRITE: This output, together with $\overline{LANCS}$, is used to write to the internal LAN registers.

TABLE A-1. PIN DESCRIPTIONS (Continued)

39

PIN NO.	PIN NAME	SIGNAL NAME/ DESCRIPTION
LAN Controller Signals, Cont.		
60	$\overline{IOR}$ (O)	LAN I/O READ: This output, together with $\overline{LANCS}$, is used to read the internal LAN registers.
61	$\overline{RST}$ (O)	LAN RESET: This output places the LAN in reset mode immediately. No packets are received or transmitted by the LAN until the STA bit in the LAN is set.
62	$\overline{LANCS}$ (O)	LAN CHIP SELECT: This output places the LAN device in slave mode for access to internal registers.
70	INT (I)	LAN INTERRUPT: This input indicates that the LAN controller needs host attention (at the end of an operation, when an error occurs, etc.).
76	BSCK (I)	CLOCK: This input is the 40-MHz clock.
69	MODE (I)	ALTERNATE MODE SELECT: This input must be left open (internally pulled high). It signifies that the WD83C593 is being used on a non-intelligent board, directly interfacing the WD83C690 LAN controller to the buffer memory.
RAM Signals		
51	$\overline{RAMWE}$ (O)	RAM WRITE ENABLE: This output is used to write host data into the buffer RAM.
53	$\overline{RAMOE}$/ARDY (O)	RAM OUTPUT ENABLE: This output is used to gate the buffer RAM onto the data bus, BD00-BD15.
ROM Signal		
54	$\overline{BOE}$ (O)	BIOS ROM OUTPUT ENABLE: This output is the chip select for the BIOS ROM. It gates data onto BD0-BD7.
Buffer Control Signals		
42	$\overline{MREQ}$ (O)	MEMORY REQUEST: This output is provided for use in a possible memory mapped scheme. This is an unlatched memory decode indicator.
49	$\overline{DEN}$ (O)	DATA BUFFER ENABLE: This output is generated to enable or disable the external bidirectional data buffers.

TABLE A-1. PIN DESCRIPTIONS (Continued)

PIN NO.	PIN NAME	SIGNAL NAME/ DESCRIPTION
52	$\overline{\text{DDIR}}$ (O)	DATA DIRECTION: This output is generated to control the direction of the external bidirectional buffers between the host data bus and DB00-DB15 (local data bus).
Power		
21,43, 64,84	Vcc	+5V dc
1,22, 44,65	GND	GROUND.
No Connection		
11,12	N/C	Pins 11, 12 must be left open. They are used for factory testing.

TABLE A-1. PIN DESCRIPTIONS (Continued)

APPENDIX B -- REGISTER DESIGNATIONS

This appendix provides information on the WD83C593's internal registers. Table B-1 summarizes the I/O mapping, and the remainder of the appendix describes each register in detail.

Offset	Type	Name
0x00	R/W	Memory Enable, Reset Register (MER)
0x01	W	EEPROM Control Register (EEC)
0x02	R (EEPROM)	Reserved (PID0)
0x03	R (EEPROM)	Reserved (PID1)
0x05	R/W	Internal Mask and Command Control Register (IMCCR)
0x07	R/W	General Purpose Register (GPR)
0x08-0x0F	R (EEPROM)	LAN Address Registers (LAR)
0x10-0x1F	R/W	LAN Controller Registers (LAN)

TABLE B-1. INTERNAL REGISTER I/O MAP

Name: MEMORY ENABLE, RESET (MER) **Offset:** 0x00

Description: Only bits 7 and 6 in this register are used. Setting bit 7, and clearing it after 1 µsec, resets the LAN controller, as well as the other registers (except LAR, PID0, PID1 and FEX). Setting bit 6 enables the host Micro Channel to share the on-board buffer RAM. When bit 6 is cleared, RAM is disabled. A hard reset clears all bits in this register.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
REST	MENB	N/A	N/A	N/A	N/A	N/A	N/A

Name: EEPROM CONTROL (EEC) **Offset:** 0x01

Description: Writing A5h first and then 00h to this register starts the program process for the EEPROM registers. See the EEPROM programming instructions for a detailed description on how this register is used.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	0	1	0	0	1	0	1

Name: RESERVED (PID0) **Offset:** 0x02

Description: This write-only register is used only by manufacturing to set the Micro Channel POS ID numbers.

Name: RESERVED (PID1) **Offset:** 0x03

Description: This write-only register is used only by manufacturing to set the Micro Channel POS ID numbers.

TABLE B-2. REGISTER DESCRIPTIONS

Name: INTERNAL MASK AND COMMAND CONTROL REGISTER (IMCCR)	**Offset:** 0x05

Description: Bit 2 is cleared when the host Micro Channel is powered off or undergoes a soft reset.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
-	-	-	-	-	EIL	-	-

Note:

bit2 (EIL) This bit is used to enable or disable an interrupt from the LAN controller to the host Micro Channel. The host Micro Channel sets this bit to "1" to enable the interrupt.

Name: GENERAL PURPOSE REGISTER (GPR)	**Offset:** 0X07

Description: This is an 8-bit wide general purpose register.

Name: LAN ADDRESS REGISTERS (LAR)	**Offset:** 0X08 - 0X0F

Description: The values for these eight read-only registers are permanently stored in the internal EEPROM. See EEPROM programming instructions.

Name: LAN CONTROLLER REGISTERS (LAN)	**Offset:** 0X10 - 0X1F

Description: These sixteen registers are physically located on the LAN controller chip. Only the decode and control circuitry is internal to the WD83C593.

TABLE B-2. REGISTER DESCRIPTIONS (Continued)

APPENDIX C - ELECTRICAL CHARACTERISTICS

Table C-1 lists the dc electrical parameters for the WD83C593, Table C-2 lists the non-operational specifications, and Table C-3 lists the operational specifications.

Ta = 0°C (32°F) to 70°C (158°F), Vcc = 5V % 10%

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{DD}	V_{DD} Supply Current	-	8	10	mA	-
V_{DD}	Voltage Supply	4.5	5	5.5	V	-
V_{IH}	Input High Voltage	2.0	-	-	V	-
V_{IL}	Input Low Voltage	-	-	0.8	V	-
V_{OH}	Output High Voltage	2.4	-	-	V	note 1
V_{OL}	Output Low Voltage	-	-	0.5	V	note 2
I_{LH}	Input Source Current	-	-	0.1	µA	$V_{IN} = V_{DD}$
I_{LL}	Input Sink Current	-	-	-1.0	µA	$V_{IN} = 0$
I_{OZH}	Tri-state High Current	-10	-	10	µA	$V_{IN} = V_{DD}$
I_{OZL}	Tri-state Low Current	-10	-	10	µA	$V_{IN} = 0$
V_{OL}	Output Low Voltage (Pins IRQ0, IRQ1, IRQ2, and IRQ3)	-	-	0.5	V	note 3
V_{OL}	Output Low Voltage (All pins except IRQ0, IRQ1, IRQ2, and IRQ3)	-	-	0.4	V	note 4

TABLE C-1. DC PARAMETERS

NOTES

1. I_{OH} = -24 mA on IRQ0, IRQ1, IRQ2 and IRQ3.

   I_{OH} = -8 mA on all other outputs and I/O pins.

2. I_{OL} = 0.5V (and 24 mA) on IRQ0, IRQ1, IRQ2, and IRQ3.

   I_{OL} = 0.4V (and 8 mA) on all other outputs and I/O pins.

3. I_{OL} = 24 mA on pins IRQ0, IRQ1, IRQ2, and IRQ3.

4. I_{OL} = 8 mA on all other outputs and I/O pins.

PARAMETER	MIN	TYP	MAX	UNIT
Storage temperature	-65	-	150	Degrees Centigrade
Voltage on any pin with respect to V_{SS}	-0.6	-	Vcc + 0.3 (except Vpp)	Volts
Voltage on V_{CC} with respect to V_{SS}	-	-	7.0	Volts

TABLE C-2. NON-OPERATIONAL SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNIT
Ambient temperature	0	25	70	Degrees Centigrade
Humidity	20	-	95	Percent
V_{CC} supply voltage with respect to V_{SS}	4.50	5.0	5.50	Volts
I_{CC} supply current (full loading)	-	-	100	Milliamps
Power dissipation	-	-	500	Milliwatts

TABLE C-3. OPERATIONAL SPECIFICATIONS

39

APPENDIX D - AC OPERATING CHARACTERISTICS

This appendix provides information on the WD83C593's ac operating characteristics. Table D-1 lists the ac operating characteristics. Figures D-1 and D-2 illustrate timing information.

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_1	Status active low from ADDRESS, M/$\overline{IO}$, $\overline{REFRESH}$ valid	10	-	nsec
t_2	$\overline{CMD}$ active low from status active low	55	-	nsec
t_3	$\overline{ADL}$ active low from ADDRESS M/$\overline{IO}$, $\overline{REFRESH}$ valid	45	-	nsec
t_4	$\overline{ADL}$ active low to $\overline{CMD}$ active low	40	-	nsec
t_5	$\overline{CDDS16}$ active low from ADDRESS, M/$\overline{IO}$, $\overline{REFRESH}$ valid	-	55	nsec
t_6	$\overline{CDSFDBK}$ and CDCHRDY low from ADDRESS valid	-	60	nsec
t_7	$\overline{CMD}$ active low from ADDRESS valid	85	-	nsec
t_8	$\overline{CMD}$ pulse width	90	-	nsec
t_9	Write data setup to $\overline{CMD}$ active low	0	-	nsec
t_{10}	Write data hold time from $\overline{CMD}$ high (at the PS/2 bus)	30	-	nsec
t_{11}	Read data setup time to $\overline{CMD}$ high (at the PS/2 bus)	60	-	nsec
t_{12}	Read data hold time from $\overline{CMD}$ high (at the PS/2 bus)	5	-	nsec

TABLE D-1. AC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{13}	$\overline{CMD}$ high to $\overline{RAMOE}$ or $\overline{RAMWE}$ high	0	-	nsec
t_{14} WRITE CYCLE	$\overline{CMD}$ high to $\overline{DEN}$ high (during WRITE)	15	-	nsec
t_{14} READ CYCLE	$\overline{CMD}$ high to $\overline{DEN}$ high (during READ)	-	25	nsec
t_{15}	$\overline{CMD}$ high to DDIR low	0	-	nsec
t_{16}	DDIR low to pulse* (read cycles only)	0	-	nsec
t_{17}	BREQ active high to BACK active high	1 clk cyc time	-	
t_{18}	BREQ low to BACK low	1 clk cyc time	3 clk cyc time + 25 nsec	
t_{19}	$\overline{LANCS}$ active low to $\overline{IOR}$ or $\overline{IOW}$ active low	0	-	nsec
t_{20}	$\overline{ACK}$ active low from $\overline{IOR}$ or $\overline{IOW}$ active low	0	-	nsec
t_{21}	$\overline{ACK}$ high from $\overline{IOR}$ or $\overline{IOW}$ high	0	-	nsec
t_{22}	$\overline{CDSETUP}$ active low to $\overline{ADL}$ active low	15	-	nsec
t_{23}	$\overline{CDSETUP}$ hold from $\overline{ADL}$ high	25	-	nsec
t_{24}	CDCHRDY inactive low from $\overline{CDSETUP}$ active low	-	100	nsec
t_{25}	$\overline{CDSETUP}$ hold from $\overline{CMD}$ active low	30	-	nsec

TABLE D-1. AC OPERATING CHARACTERISTICS (Continued)

39

*The pulse occurs on the DEN line, when the DDIR signal goes low during read cycles.

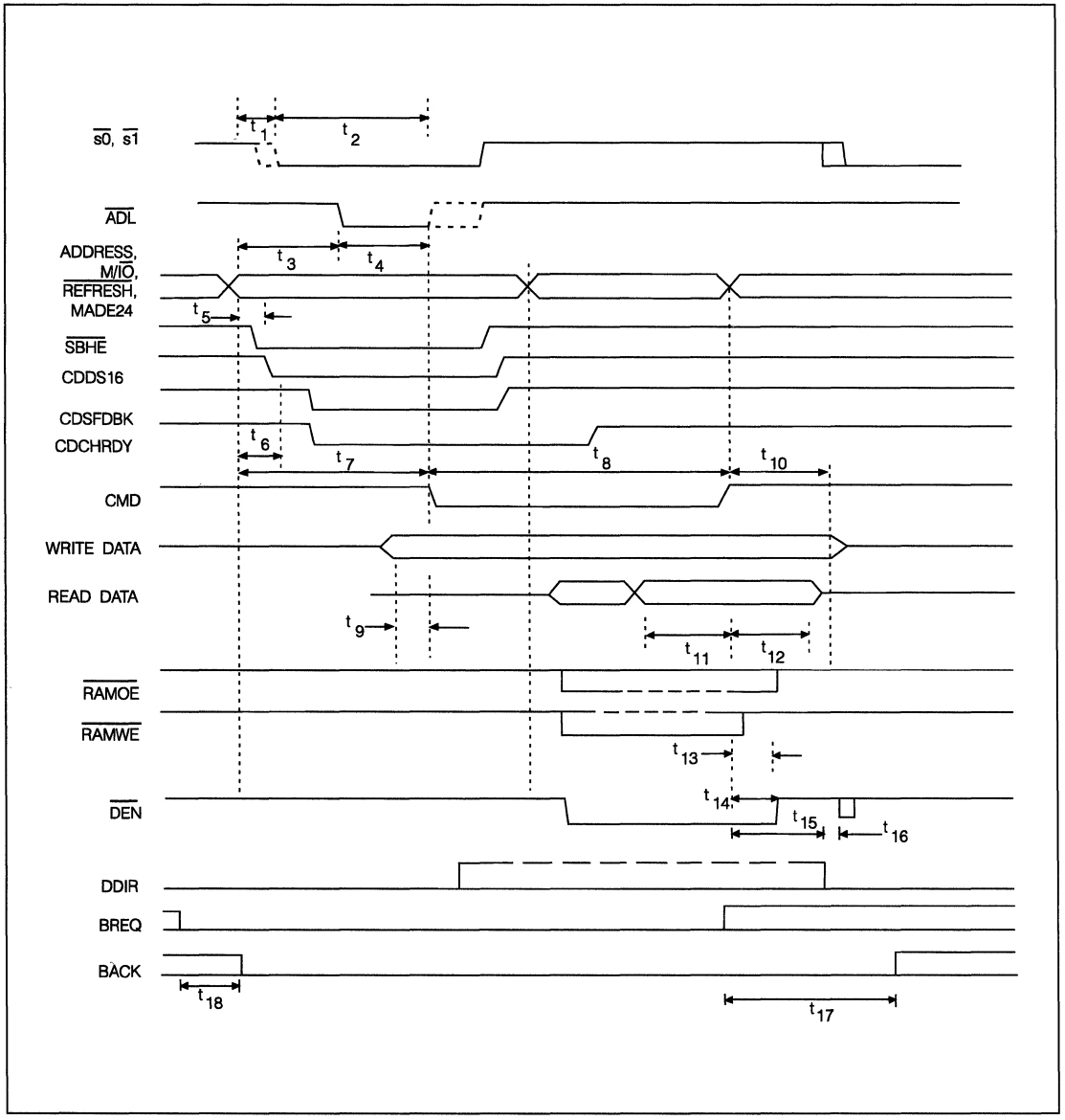


FIGURE D-1. HOST-MEMORY READ/WRITE TIMING

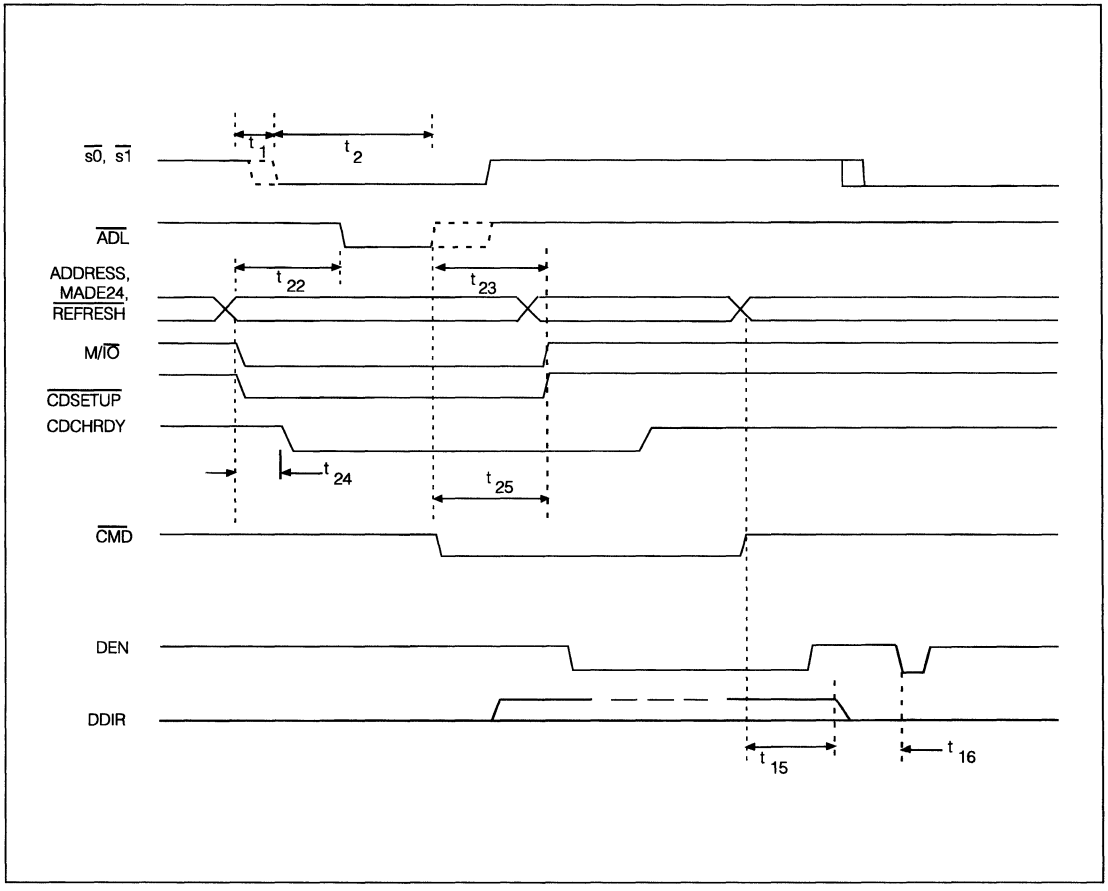


FIGURE D-2. SET-UP TIMING

WD83C690

Ethernet LAN Controller

WESTERN DIGITAL

TABLE OF CONTENTS

APPENDICES

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 DESCRIPTION AND APPLICATION

The WD83C690 Ethernet LAN Controller (ELC) is a VLSI device designed to interface with networks such as Ethernet, Cheapernet, and StarLAN. Functionally similar to the National DP8390 device, the WD83C690 incorporates an original architecture and provides several new registers (for en-hancements, block address, and test control). The device is implemented in a single-clock, single-phase synchronous design, with the exception of serial portions of the receiver and transmitter. The WD83C690's signal functions, polarity requirements, and timings are compatible with the WD83C583 and WD83C593 bus interface devices.

1.1 FEATURES

- Meets the IEEE 802.3 protocol for networks such as Ethernet, Cheapernet, and StarLAN
- Provides direct memory address (DMA) channel for transferring data between memory and the host
- Implements an original, sophisticated architecture in standard cell technology
- Provides programmable wait states and slot times
- Provides full duplex loopback capability
- Requires single, 5V power supply
- Supports physical, promiscuous, and broadcast address filtering
- Provides efficient, versatile buffer management

1.2 SYSTEM INTERFACE

The WD83C690 is part of a three-device set that implements the complete IEEE 802.3-compatible network node electronics. The WD83C691 Manchester Encoder/Decoder (MED) and the WD83B692 Ethernet Transceiver (ET) comprise the other two devices in the set. The WD83C691 provides the Manchester encoding/decoding functions, while the WD83B692 serves as a coaxial cable line driver/receiver. Figure 1-1 illustrates how the devices interface.

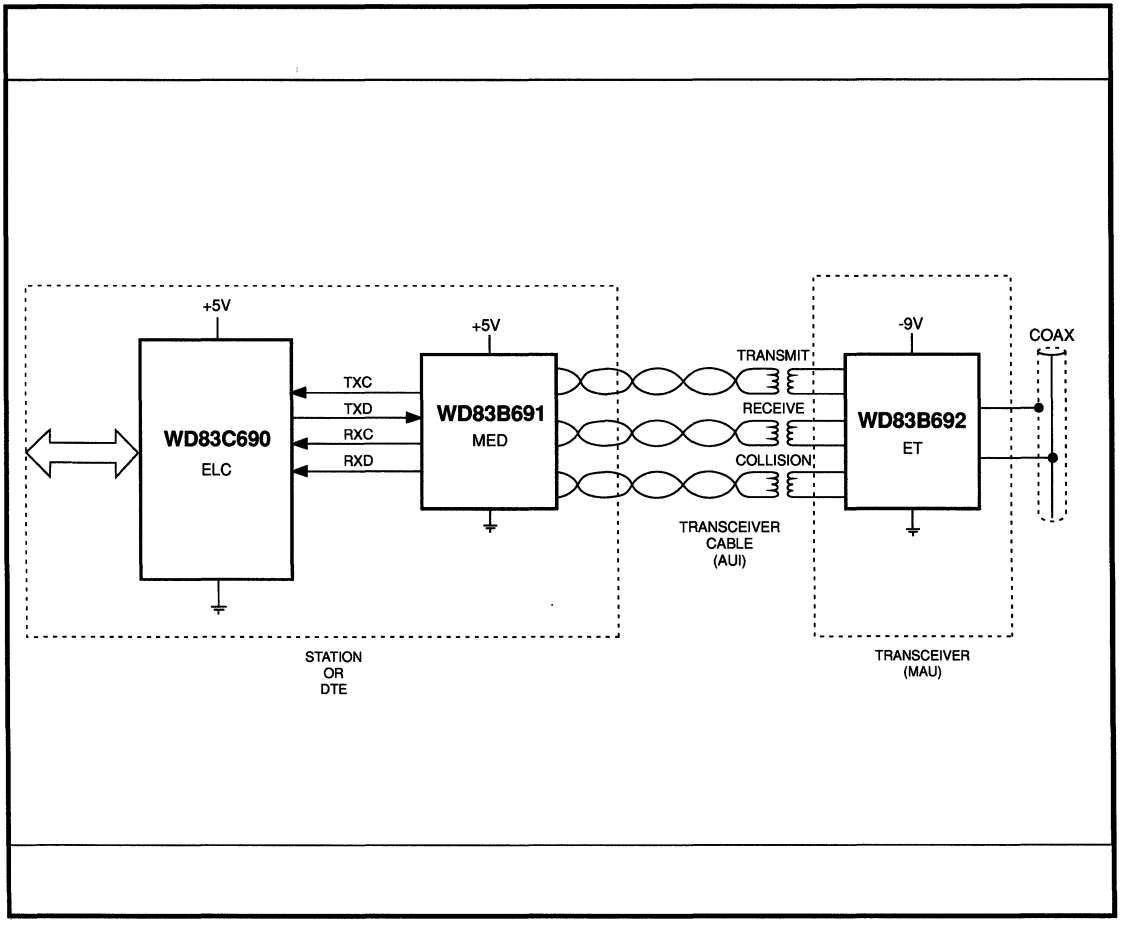


FIGURE 1-1. WD83C690 SYSTEM INTERFACE

2.0 OPERATIONAL DESCRIPTION

This section describes the functional blocks that comprise the Ethernet LAN controller. A general system block diagram is shown in Figure 2.1. Sections 3 and 4 provide more detailed explanations of the receive and transmit functions and memory interface.

2.1 RECEIVE FEEDBACK MULTIPLEXOR

For testing purposes, an internal multiplexor at the network interface end of the receiver permits the loopback of transmitted data, and the use of transmit enable as a carrier sense signal. The multiplexor can be programmed via the transmit configuration register.

2.2 CARRIER SENSING

Carrier sensing is done externally and brought into the WD83C690 through the CRS pin. Received data and clock are brought in through the RXD and RXC pins, respectively, and feed the CRC checker, the octet alignment circuit, and the serial-to-parallel converter.

2.3 CRC CHECKER

The receiver section performs the cyclic redundancy check (CRC) for the incoming serial data. The CRC computation includes the address, data, and CRC fields. It excludes the preamble and SFD.

The CRC polynomial used is AUTODIN II (X32 + X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 + X2 + X1 + 1).

2.4 RECEIVE DESERIALIZER

The receive deserializer clocks incoming bits into an eight-bit serial-to-parallel shift register, and, when an octet is complete, loads the parallel data into the receiver "first in, first out" buffer (FIFO). Octet alignment is determined by a synchronization circuit which detects the start of frame delimiter (SFD).

2.5 ADDRESS RECOGNITION LOGIC

The destination address is compared to a 6-byte station address stored in the internal registers, and, if all bytes match (or if promiscuous mode is enabled), the frame is received. When multicast addressing is enabled, only the individual/group bit of the destination address is checked. No filtering of group addresses is done. Broadcast frames are received when the broadcast enable bit is active.

If the address is rejected, the receive FIFO is cleared and none of the frame is stored. If the address is accepted, buffering of the frame begins.

2.6 RECEIVE PROTOCOL FINITE STATE MACHINE (RPFSM)

The Receive Protocol Finite State Machine (RPFSM) determines whether the incoming frame will be saved in memory, and coordinates the operation of all other blocks in the receiver section. This involves generating status information regarding each frame (the information is placed in the receiver status register) and keeping track of the length of the frame via a 16-bit-wide frame length byte counter attached to the state machine. The block is controlled by the receiver configuration register and the START and STOP bits from the command register. The receiver error counters are also under control of this circuit.

2.7 RECEIVER ERROR COUNTERS

There are three error counters in the receiver section: the CRC error counter, the frame alignment error counter, and the missed packet counter. Each counter is eight bits wide and can be incremented up to 255, where it remains until the counter clears (when the register is read or the device reset).

The CRC error counter, under control of the receive protocol finite state machine, is incremented when a received frame's computed CRC does not match the appended CRC.

The frame alignment error counter is advanced when a frame with too many dribble bits and a CRC error at the same time is received.

The missed packet counter is incremented when a frame that would ordinarily be stored in memory was not stored (either because the receiver was operating in monitor mode, or because there was insufficient memory to store the entire frame).

2.8 FIFOS

The transmitter and receiver sections have similar, but independent, 16-byte deep FIFOs. These FIFOs have a programmable threshold level that allows the transmit receive (TR) direct memory access controller (TRDMA) to determine when there is a need to move data between the WD83C690 and memory.

2.9 TRANSMITTER PROTOCOL FINITE STATE MACHINE (TPFSM)

The transmitter protocol finite state machine (TPFSM) coordinates the operation of all blocks that comprise the transmitter section. It decides when to transmit, when to defer transmission, and, in the event of a collision, when to back off and attempt to transmit again. The transmit configuration register controls the operation of this state machine, which updates the transmit status register after each attempt to send a frame.

2.10 TRANSMIT SERIALIZER

The transmit serializer converts the 8-bit parallel data from the transmit FIFO into serial data. Serial data is clocked out of the TXD pin (least significant bit first) by the rising edge of an external clock at the TXC pin.

2.11 TRANSMITTER CRC GENERATOR

Using the same polynomial as the receiver CRC checker, the transmit section generates CRC serially and appends it to each outgoing frame. (CRC is clocked-out most significant bit first.)

2.12 PREAMBLE GENERATOR

The preamble generator block generates a data pattern of alternating "1" and "0" bits.

2.13 JAM GENERATOR

This block generates a pattern of consecutive "1" bits. It drives the TXD pin when a collision is detected.

2.14 SERIAL STREAM MUX

Using the serial stream multiplexor, the TPFSM composes each frame from its constituent parts.

2.15 SYNC-TO-TXC

To ensure minimal output jitter, the transmit data stream is reclocked to the rising edge of TXC prior to driving the pin.

2.16 COLLISION DETECTION LOGIC

Collisions are sensed externally during transmission, then input through the COL pin.

2.17 DMA CONTROLLER

There is an internal direct memory access (DMA) controller, TRDMA, which moves packets between buffer memory and the WD83C690.

The DMA generates 16-bit addresses, supplemented by 8 bits of static address in the high order positions (A16-23). The DMA controller supports memory cycles as short as 200 nsec, which can be slowed down using the MEM-READY pin or by programming a default number of wait states into the configuration register.

2.18 ASSEMBLY AND DISASSEMBLY LATCHES

The TRDMA does all of its transfers as pairs of 8-bit bytes. The assembly and dissassembly latches match the internal 8-bit data path to the external data bus. When interfacing to a 16-bit bus, the assembly latches combine two 8-bit words to form a 16-bit word; when interfacing with an 8-bit bus, they supply the two consecutive bytes of a transfer. The disassembly latches perform the opposite function.

2.19 BUS INTERFACE AND INTERNAL BUS ARBITRATOR

The bus interface unit (BIU) and internal bus arbitrator control access to the WD83C690's internal registers and ensure that the device does not attempt a DMA transfer until it has access to the memory bus. The BIU transfers data from buffer memory to the internal disassembly latches and from the internal assembly latches to buffer memory. It generates the bus request (BREQ), memory strobes (MRD and MWR) and the address strobe (ALE).

To control the initiation of a transfer and insertion of wait states, the BIU observes the bus grant (BGRANT) and memory ready (MEMRDY) signals.

Until BGRANT becomes true, the memory strobes, address outputs, and ALE outputs are tri-stated. Once BGRANT is issued, the host must not drive the address, data, ALE, or memory strobes until BREQ is dropped and BGRANT taken away at the end of the DMA burst. Failure to adhere to this rule will result in contention on the lines and corruption of the data transferred. Refer to the timing diagrams in Appendix D for more details.

When the DMA bursts are complete and BGRANT is negated, the host can access the internal bus. Although BREQ may again become active in response to new DMA needs, the arbitration logic permits access until BGRANT becomes true. The internal arbitrator generates the READY signal to tell the host that the requested I/O access has been made and the internal bus is available.

The host may force the WD83C690 to interrupt a DMA burst by removing the BGRANT signal while BREQ is still active. When this happens, the BIU completes the current byte or word transfer, then relinquishes the bus by dropping BREQ for one clock. The internal bus arbitration unit disables the DMA until BGRANT is again true, at which time, the burst continues where it left off.

2.20 ACCESSING INTERNAL REGISTERS

To access an internal register, the host must assert the chip select (CS) signal and wait until READY is asserted before driving the bus. When the WD83C690 is not involved in a DMA operation, it is not necessary to wait for READY to be asserted prior to driving the address, ALE, and data lines. CS must be maintained throughout the access.

In multiplexed bus applications, ALE latches the register address into the WD83C690. In non-multiplexed bus applications, ALE should be driven high or pulled up during register access to allow the address to flow through the internal transparent latch.

To read from a register, IOR must be asserted by the host (either before or after CS). It is recognized by the internal bus arbitrator (BUSARB) circuit, which enables data flow from the addressed register to the AD00-07 pins. During read operations (which are always done through the AD00-07 pins), AD08-15 are tri-stated. READY indicates when the host can sample data and terminate the read operation.

To write to a register, IOW must be asserted by the host and recognized by the internal BUSARB. When the bus is free for the transfer, READY is asserted and the register address is latched internally. Data is latched into an intermediate transfer latch with the trailing edge of IOW, and, two clocks later, transferred to the destination register.

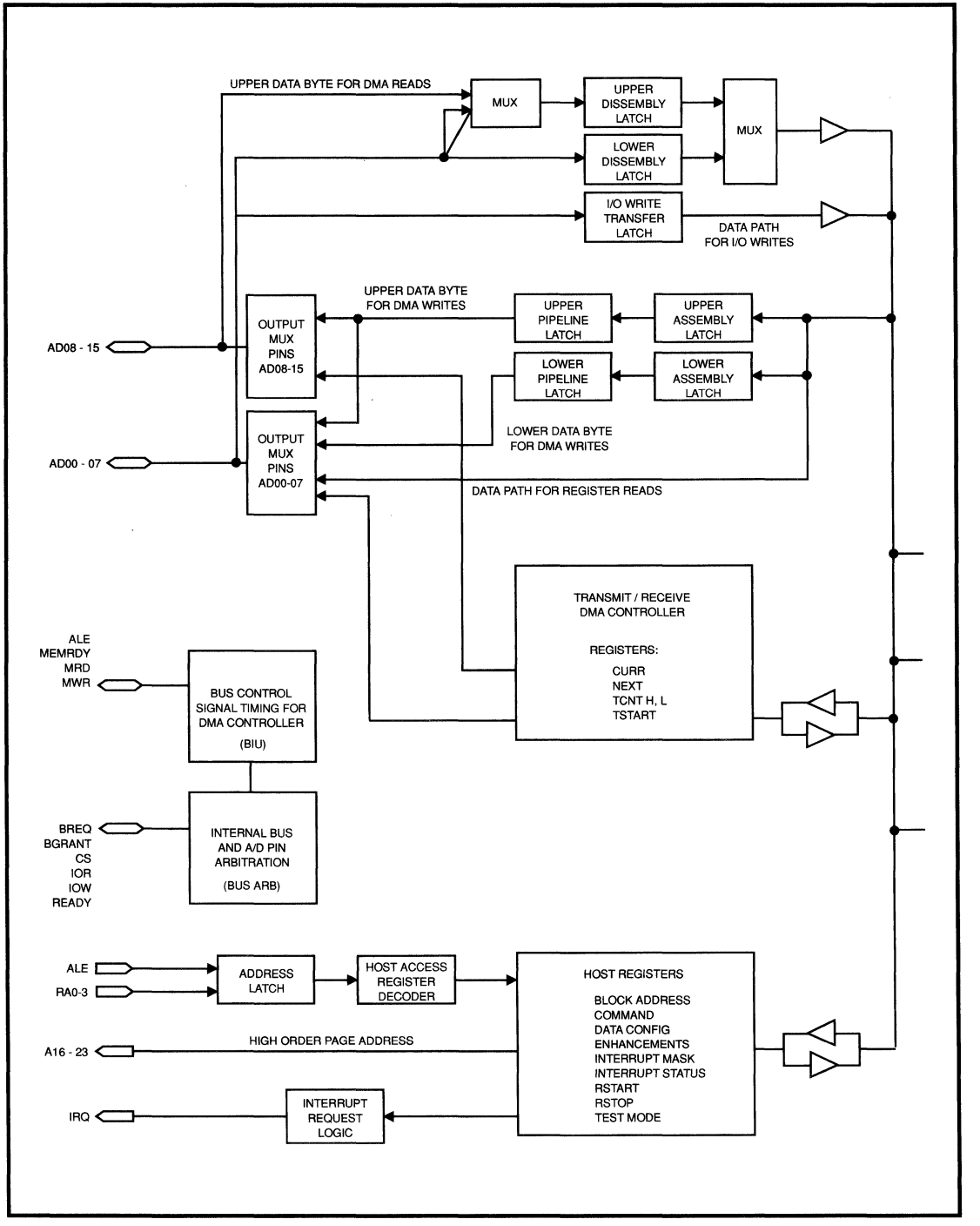


FIGURE 2-1. GENERAL SYSTEM BLOCK DIAGRAM

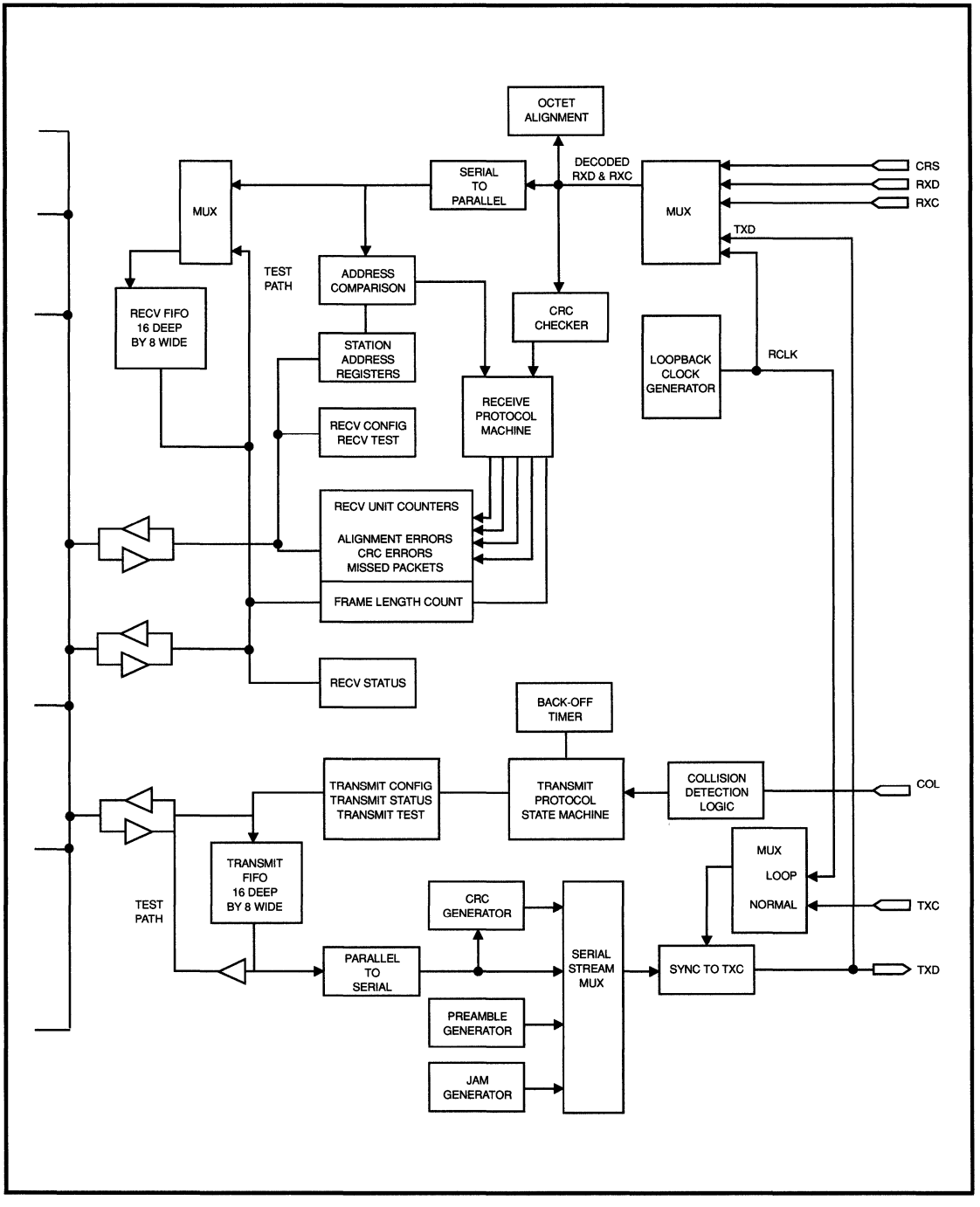


FIGURE 2-1. GENERAL SYSTEM BLOCK DIAGRAM (Continued)

40

3.0 OPERATION OF THE SERIAL INTERFACE SECTIONS

When the stop bit in the command register is cleared and the start bit is set, the transmit and receive sections are enabled. This permits the serial interface sections to recognize incoming frames and to act on requests for transmitting frames. Once enabled, the serial interface sections remain enabled until the stop bit is set. Clearing the start bit does not disable the serial interface.

If the stop bit is set while the transmit and receive sections are operational, they will finish handling the current frame, then go to a soft reset condition and ignore incoming frames and requests for transmission. Before the transmitter stops, however, it will complete the retransmission of any colliding packets. When both sections are stopped, the RST bit in the interrupt status register is set (although the DMA controller may remain active), and the receiver status registers are reinitialized.

3.1 RECEIVE FUNCTIONS

This section describes how the receiver section operates.

3.1.1 RECEIVING A FRAME

The preamble field is used to train the external Manchester decoder and to detect carrier. If carrier sense (CRS) is true, the preamble passes through the receive deserializer which discards it while searching for the consecutive "1" bits that mark the start-frame-delimiter (SFD). The deserializer loads the receive FIFO with octets (bytes), beginning with the first bit after SFD.

While the destination address (DA field) is being checked for recognition, the receive DMA is disabled. If the frame is accepted, the DMA is enabled, and when the FIFO fills to the programmed burst level, transfer to memory begins. If the frame's address is not accepted, the receive unit clears out the FIFO and waits for the start of the next frame.

The destination address, source address, and data fields are passed to buffer memory. In some protocols, the first 2 bytes of the data field denote a frame length. These bytes are not interpreted by the WD83C690, but treated as ordinary data.

3.1.2 END OF FRAME

Upon loss of carrier sense, dribble clocks (receive clocks that occur after the loss of carrier) on the RXC pin flush the remainder of the received frame through the deserializer and CRC checker. The CRC of all received octets is computed and compared to the CRC at the end of the frame, and the result is recorded in the receiver status register. The CRC from each received frame is sent to memory with the frame via DMA, and included in the byte count posted in the buffer header.

The deserializer counts the number of bits left over after the last complete octet. If the number is greater than 6, a frame alignment error is reported.

If the receive unit detects errors in the frame, it may abort reception, depending on how the bits, "save errored packets" and "accept runt frames", have been configured. If reception is aborted, the DMA controller stops sending bytes to the buffer, the receive unit clears out the FIFO, the receive status register (RSR) and the interrupt status register (ISR) are updated, and the receive unit waits for the next frame to begin.

For frames that are not accepted, a header is not posted, and the previous contents of the header location remain unchanged. We recommend that the header portions of recycled buffers be cleared out so that they are not subject to misinterpretation during subsequent host processing.

The received packet length must be less than 65,024 bytes, including DA, SA, data, and CRC. In addition, the buffer ring must have enough space for the entire frame and a 4-byte header. Packets larger than the available buffer space cannot be received, regardless of the SEP bit in the RECEIVE CONFIG register. Such frames are posted as ring over-writes and cause the over-write (OVW) interrupt to be set. Receiver interrupts (RXE, PRX) are posted after the frame has been completely posted to memory by DMA. If DMA aborts, these interrupts are not set for the current frame (if set previously, they remain unchanged). Packets shorter than 64 bytes are received only when the "accept runts" bit is enabled.

3.2 TRANSMITTER

This section describes how the transmitter section operates.

3.2.1 INITIALIZATION FOR TRANSMISSION

The host builds packets to be transmitted in buffer memory. These packets must include the DA, SA and data fields. CRC is not read from buffer memory unless CRC generation is disabled. If it is disabled, the user is expected to place the computed CRC in the last four bytes of memory with the bit order reversed so that when clocked out least significant bit first, the CRC is presented to the serial interface most significant bit first.

The transmit start and transmit length (TSTART and TLENGTH) registers must be properly programmed before the TXP bit in the command register is set by the host. Once the TXP bit is set, the transmit unit can request the frame from the TRDMA unit. TXP can be cleared only by the transmitter upon completion of an attempted transmission.

3.2.2 TRANSMISSION PROCESS

TRDMA fills the transmit FIFO with bursts of data until there is no room left for an entire data burst. Burst lengths of 2, 4, or 8 bytes are repeated until they result in a full FIFO. A burst length of 12 bytes stops TRDMA and leaves only 12 bytes in the FIFO. When all bursts are done, TRDMA notifies the transmit unit that the FIFO is ready for transmission to begin.

The transmit unit waits until the media is clear for transmission, then generates 62 bits of preamble and SFD. Following this operation, it pulls bytes out of the transmit FIFO, serializes them, shifts their bits to the TXD pin, and computes the packet's CRC. During this operation, the TRDMA monitors the condition of the FIFO to determine when there is room for other bursts of data. As soon as there is room, additional bursts are performed.

When the DMA has filled the transmit FIFO with the last byte of the packet, it sets a flag. The transmitter continues to pull data out of the FIFO until it becomes empty, which marks the end of the frame. CRC computation stops and the CRC is appended serially to the frame, most significant bit first.

3.2.3 TRANSMIT UNDERRUN

If the FIFO becomes empty before the internal flag is set, a transmit underrun condition results and a transmit error is posted. Transmission of the packet is aborted and an interrupt may be generated.

3.2.4 COLLISIONS

When a collision is reported on the COL pin, the transmitter sends thirty-two "1" bits as a jam signal, terminates transmission, then tries again (up to 16 times).

If there are fewer than 16 retries, the transmitter randomly selects a backoff delay, in slot-time units, from the range, $0 \leq R < 2^K$ (where K is 10 or the number of retries, whichever is less). The transmitter requests retransmission of the frame from memory and delay is initiated. Note: in accord with the 802.3 specifications, the carrier sense is ignored during the last third of the interframe gap.

When retransmitting a frame, the DMA controller clears out the transmit FIFO, loads its pointer to the start of the frame in memory, and waits for the abort signal to subside. The FIFO is then loaded in the same manner as it was initially. If the maximum number of collisions (16) is exceeded, transmission is aborted without further retries or back-off delay.

3.2.5 EXTENSIONS TO THE 802.3 10base5 PROTOCOL

The 802.3 10base5 protocol uses frame lengths between 64 and 4096 bytes, inclusive. The transmitter section can send frames containing more than 16 and fewer than 65,276 bytes in length. The ability to transmit shorter or longer frames may be useful in other variations of the 802.3 protocol.

To support these variations, the slot time is program-selectable (the choices are 256-, 512-, or 1024-bit times).

4.0 MEMORY INTERFACE

As previously noted, the DMA channel generates a 16-bit linear address which can be used with a static 8-bit upper address stored in a page register. This enables the WD83C690's 64-Kbyte address space to be positioned on any 64-Kbyte boundary within the host's 16-Mbyte address space.

4.1 MEMORY ACCESS TIME

Once granted control of the memory bus, the DMA channel can perform memory accesses in as little as 200 nsec. The actual cycle time depends on the number of wait states requested by memory. Wait states add 50 nsec each to the cycle time. For systems in which memory access time is known at design time, a choice of 0, 1, 2, or 3 automatic wait states can be programmed into the enhancement register. Automatic wait states apply to all memory cycles, regardless of the direction in which the data is moving.

Wait states are also inserted when the MEMRDY line is pulled high, even if the automatic wait states have expired.

4.2 DMA BURSTS

To economize on arbitration time, the TRDMA channel collects transfers into bursts of 2 bytes (1 word), 4 bytes (2 words), 8 bytes (4 words), or 12 bytes (6 words). The choices provide a trade-off between bus latency and efficiency. The same burst length applies to transmit and receive operations.

When a data burst is required, the BREQ line requests the memory bus. An external arbitrator drives BGRANT high, enabling the address pin drivers, and a multiplexed address is driven onto the bus. An ALE signal coordinates the external address latches. Data is then either driven out or read in. In byte mode operation, the evenly-addressed byte is always accessed first.

Provided that the BGRANT line remains high, the entire burst proceeds as back-to-back cycles without relinquishing the bus. The DMA controller, however, can be preempted on a word boundary by removing BGRANT. On completion of the present word transfer (or second byte of a paired-byte transfer), the WD83C690 tri-states its address and data drivers and suspends DMA operations. (While DMA is suspended, the device's registers can be accessed.) When BGRANT is asserted again the DMA process picks up where it left off.

Be careful when preempting DMA bursts. If memory is not regained soon enough, FIFO overflow or underrun can result.

4.3 TRANSMIT PACKET BUFFERING

A packet to be transmitted is placed by the host into buffer memory. The packet must include the DA, SA, and data fields. The preamble, SFD, and (normally) CRC are not included in the buffer. If CRC generation is suppressed, the CRC field for the packet is also supplied by the host. The packet is placed in a contiguous block of memory, starting on a 256-byte boundary.

Valid 802.3 packets have at least 48 bytes of data. If data with fewer bytes are to be transmitted on an 802.3 network, it is the host's responsibility to build a packet with pad data included. The WD83C690 can transmit frames of any programmed length, even those which are too short to be valid frames on an 802.3 network.

TRDMA transfers the number of bytes programmed into the transmit frame length high-and low-byte (TCNTH, TCNTL) register pair, starting from the address, TSTART, 00.

4.4 RECEIVE PACKET BUFFERING

All received packets are stored in a circular set of 256-byte buffers. The values written into the receive start and receive stop page registers (RSTART and RSTOP) by the host when the WD83C690 is initialized determine the number and location of the buffers in the ring. RSTART points to the first buffer in the ring, and RSTOP points to the buffer after the last one in the ring.

Each packet received is stored in one or more of these buffers, with a 4-byte header inserted at the start of the first buffer. Figure 4-1 illustrates the format of a received packet in memory.

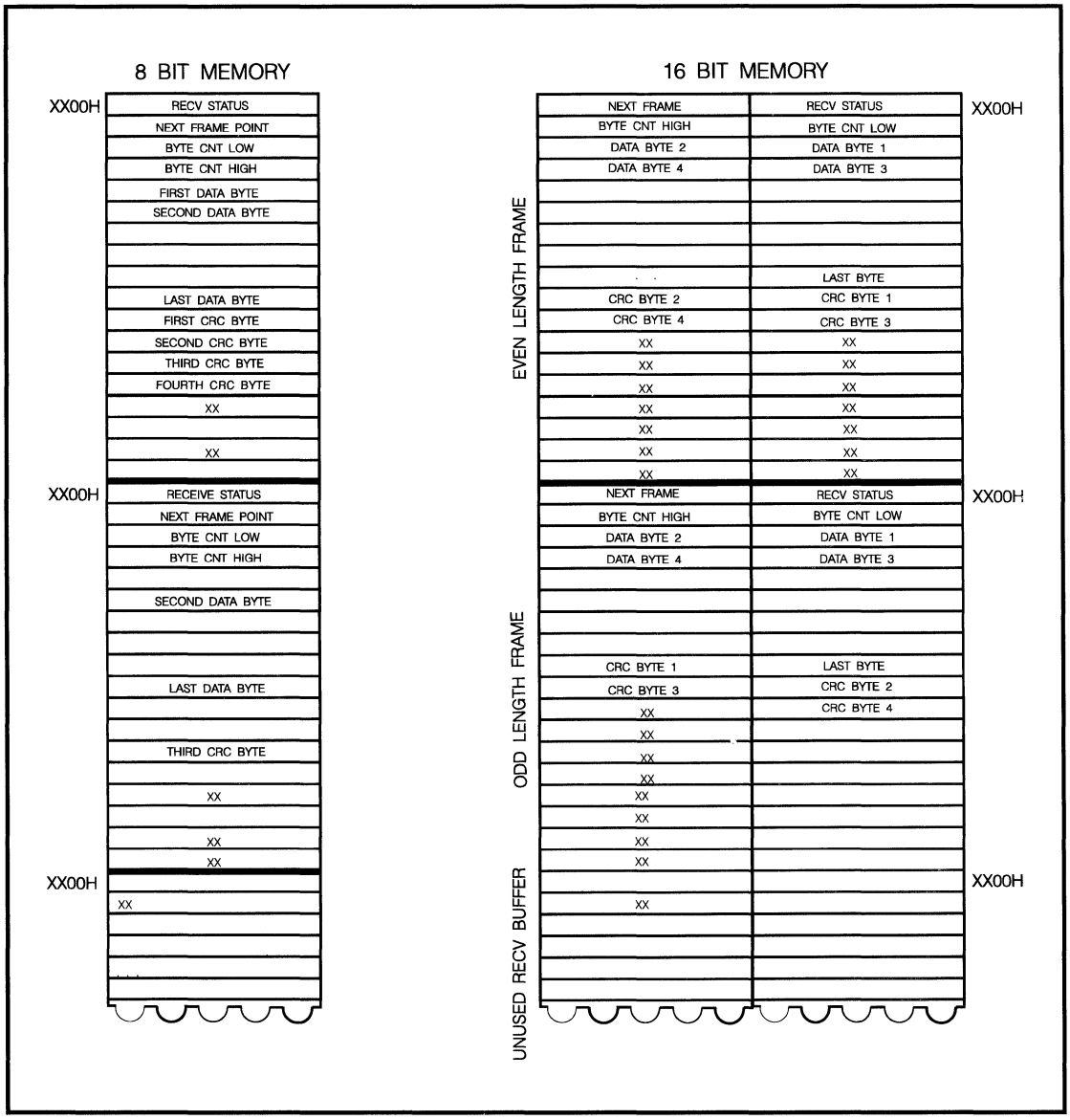


FIGURE 4-1. RECEIVER BUFFER FORMAT

Frames that extend to the buffer pointed to by RSTOP are continued in the buffer pointed to by RSTART. RSTOP can be either greater than RSTART + 1 or less than RSTART. Making RSTOP equal to RSTART or RSTART + 1 leads to unpredictable results. The relationship of these registers to ring placement in memory is illustrated in Figure 4-2.

Up to 254 buffers can be allocated to the ring. The receiver DMA uses as many as required to store a packet. This enables you to configure the device to receive frames nearly as long as 64K bytes, a

40

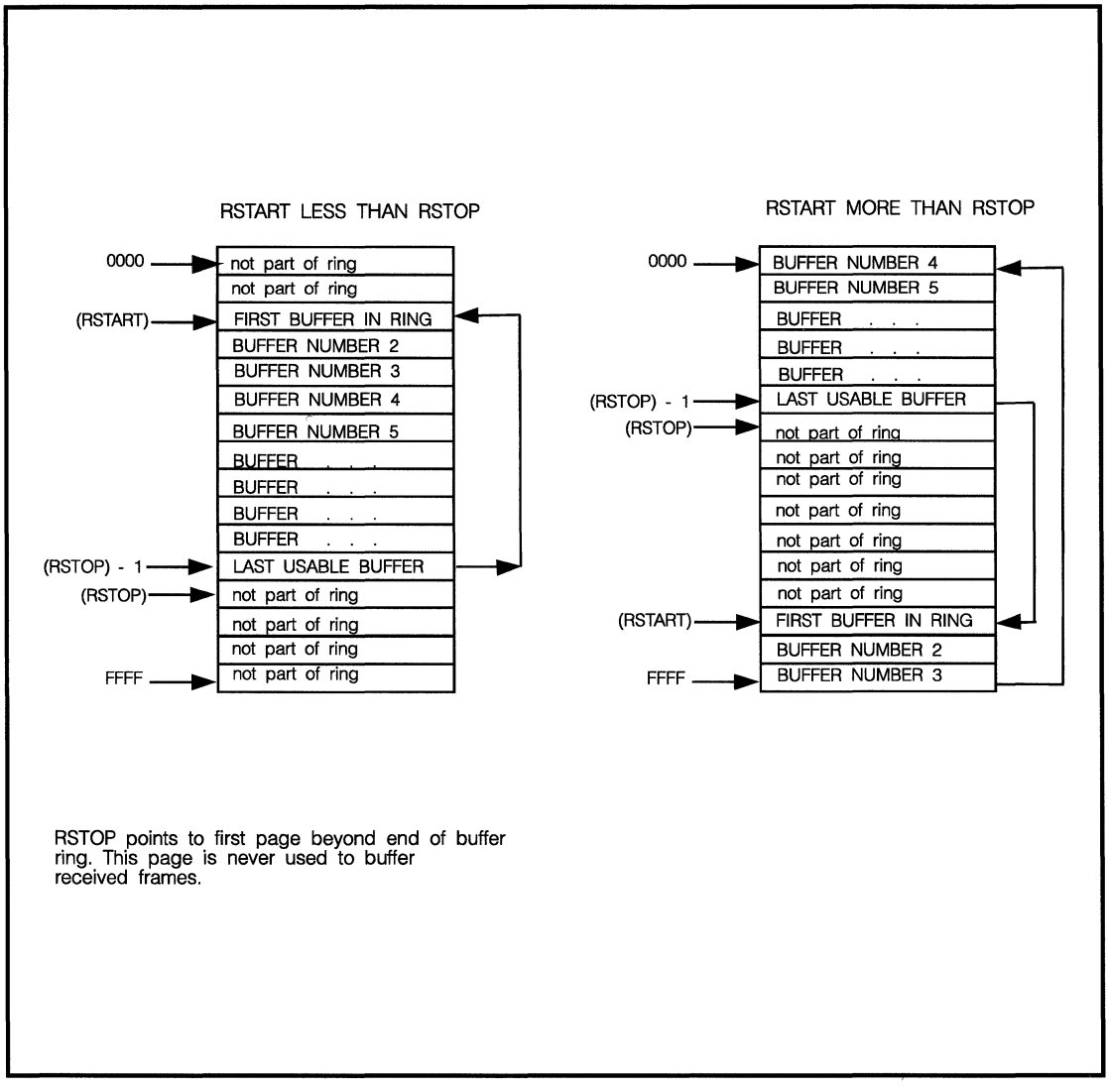


FIGURE 4-2. RECEIVER BUFFER STRUCTURE

feature that may be useful in customized CSMA networks.

The receive DMA uses two additional registers to manage the buffer ring: the current (CURR) page register and the boundary (BOUND) page register. CURR points to the first buffer that is not part of a completely-received packet. When TRDMA is storing a frame, for example, CURR points to the start of the frame being stored. When TRDMA is not storing a frame, CURR points to the first buffer that will be used for the next frame to be received.

The receive boundary page register (BOUND) protects received frames from being overwritten by later frames. It points to the first buffer in the ring that is not to be overwritten. When the receive DMA process attempts to open the buffer pointed to by BOUND, reception is aborted and the overwrite (OVW) flag in the receiver status register is set.

Normally, BOUND is set up to point to the oldest received packet in the ring. The pointer is managed by the host. To discard an unwanted frame, the host simply rewrites BOUND to point to the next packet. To prevent misinterpretation of the discarded packet as a received packet, it is advisable to write zeros into the first word.

CURR is updated by the receive DMA after a frame is received. Conversely, BOUND is updated by host software after data is removed from the ring. When the last frame has been removed from the ring buffer, BOUND has the same value as CURR, and the ring is considered empty by the WD83C690.

The WD83C690 distinguishes between empty, full, and partially-filled buffer rings on the basis of the BOUND and CURR pointer values. Whenever BOUND is not equal to CURR, the buffer ring is assumed to be partially filled, starting with the buffer pointed to by BOUND and ending with the buffer prior to that pointed to by CURR.

When BOUND equals CURR, the ring is full only if CURR was changed by the TRDMA controller more recently than BOUND was changed by the host. When BOUND is changed more recently than CURR, the ring is considered empty.

Note: you can initialize BOUND and CURR to point to any buffer within the ring, for example RSTART. Because RSTOP is outside the ring, the registers should not point to RSTOP. (This would result in the TRDMA storing frames outside the ring in an unpredictable manner.)

Provided the buffer is in the ring, you can give BOUND and CURR the same value. Figure 4-3 illustrates the relationship between pointers in a typical initialized ring. Figure 4-4 shows a ring that has received a few frames (this is its normal condition), and Figure 4-5 shows the same ring after proper removal of the oldest received packet. Figure 4-6 shows a ring that is completely full, and Figure 4-7 shows a ring on the verge of overflow.

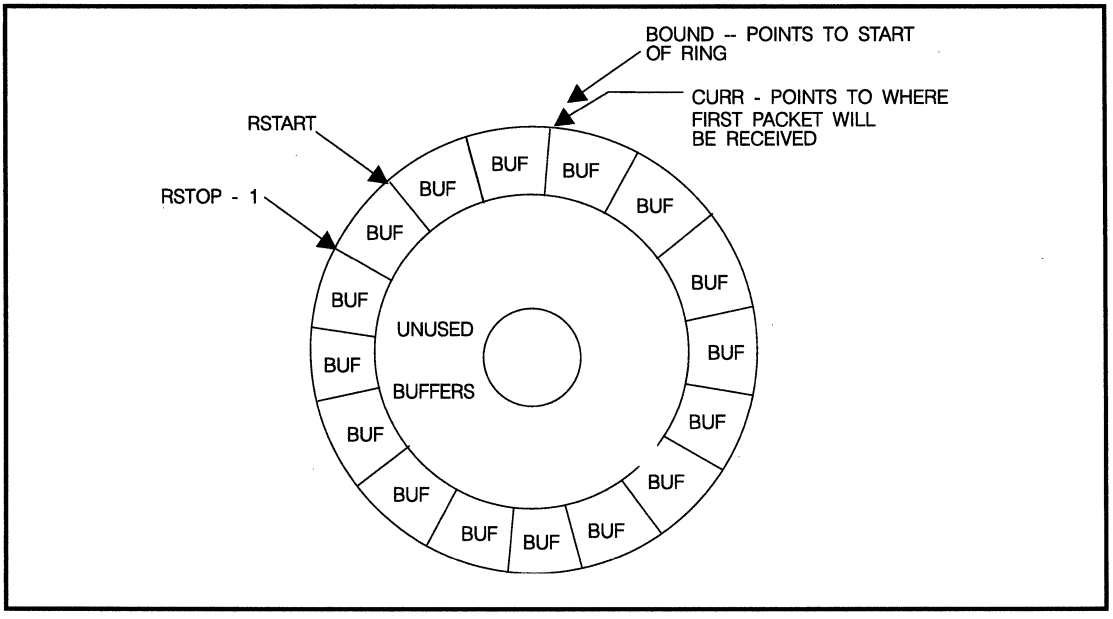


FIGURE 4-3. RECEIVER BUFFER RING,TYPICAL SETUP CONFIGURATION

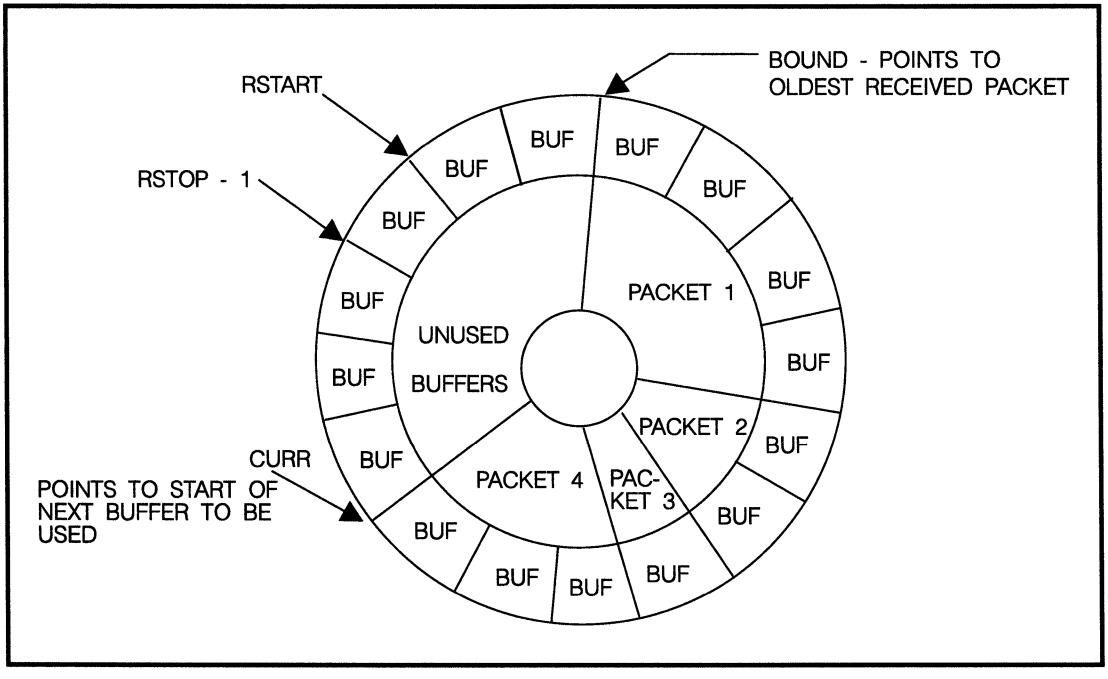


FIGURE 4-4. RECEIVER BUFFER RING, TYPICAL OPERATING CONFIG.

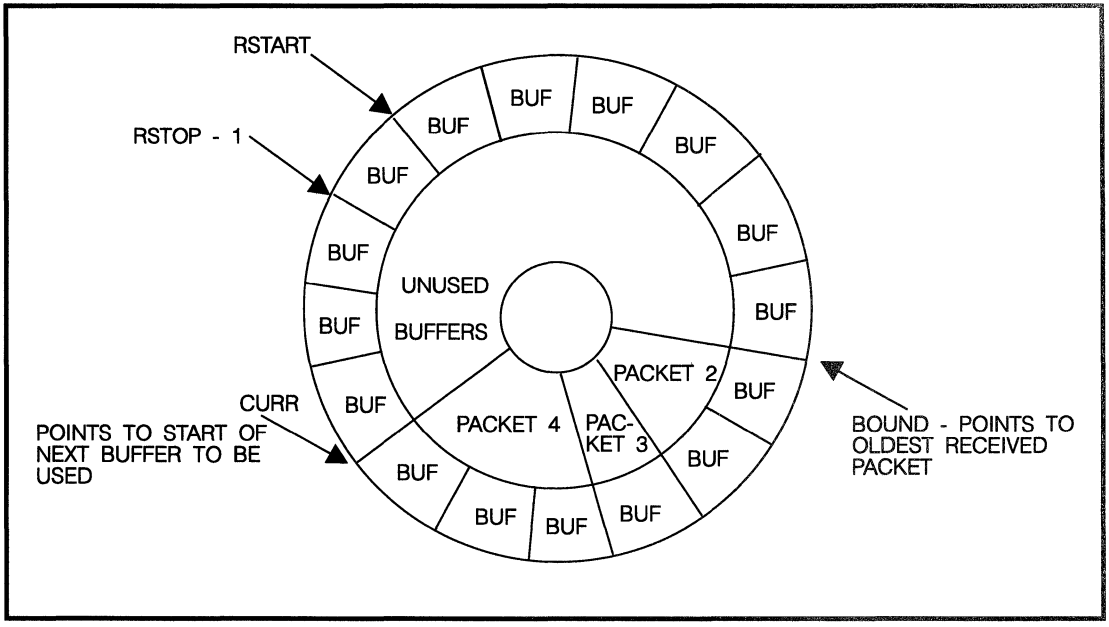


FIGURE 4-5. SAME BUFFER RING, AFTER REMOVING ONE PACKET

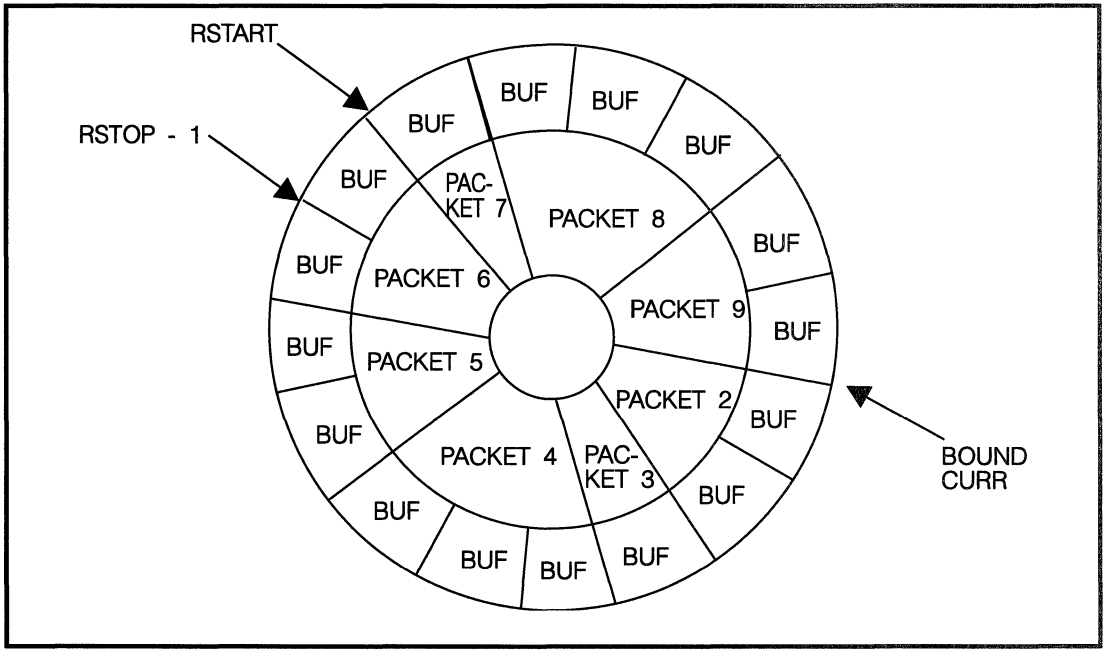


FIGURE 4-6. FULL RECEIVER BUFFER RING, NO OVERFLOW

40

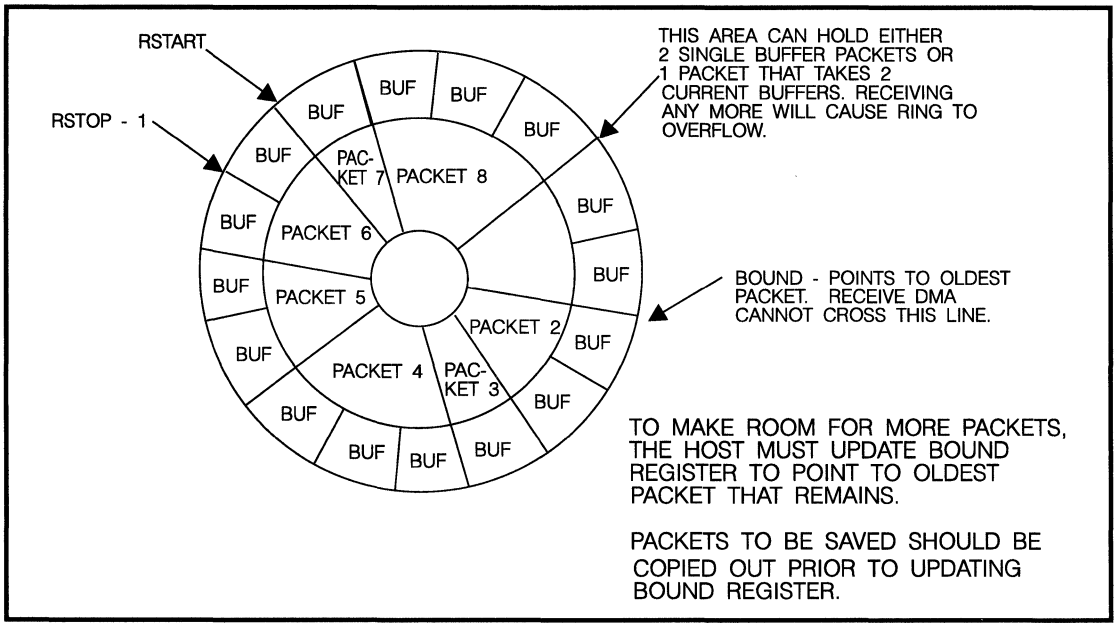


FIGURE 4-7. RECEIVER BUFFER RING VERGING ON OVERFLOW

A.0 APPENDIX A

A.1 HARDWARE CHARACTERISTICS

FEATURE	CHARACTERISTERIC(S)
Package	PLCC-68
Supplies	Single 5V supply
Technology	CMOS
IEEE 802.3 compatibility	Yes
Individual addresses	Filters completely
Group addresses	No filter; only enable/disable
Broadcast address	Enable/disable
Collision detection	External input
Buffer block size	Fixed at 256 bytes
Transmit buffers	One frame, contiguous blocks
Receive buffers	Circular buffer Many frames 65 Kbyte maximum frame size
DMA channel	Transmit/receive 8/16 bit data Full duplex operation Muxed address/data Interruptible bursts Programmable wait states Programmable burst size
Memory addressing	64 Kbyte buffer region within 16 Mbyte address space.
Loopback	Full duplex –allows reception of entire frame.
Clock relationships	Device and transmit clocks must be synchronous. RXC is asynchronous.
Clock frequency	Device clock must be 20 MHz. RXC and TXC may be 1,2, or 10 MHz.

TABLE A-1. SUMMARY OF HARDWARE CHARACTERISTICS

40

B.0 APPENDIX B

B.1 REGISTER DESIGNATIONS

REG ADDR	PAGE 0 READ	PAGE 0 WRITE	PAGE 1 READ	PAGE 1 WRITE
0	COMMAND	COMMAND	COMMAND	COMMAND
1	TRINCRL	RSTART	STA0	STA0
2	TRINCRH	RSTOP	STA1	STA1
3	BOUND	BOUND	STA2	STA2
4	TSTAT	TSTART	STA3	STA3
5	COLCNT	TCNTL	STA4	STA4
6	–	TCNTH	STA5	STA5
7	INTSTAT	INTSTAT	CURR	CURR
8	–	–	–	–
9	–	–	–	–
A	–	–	–	–
B	–	–	–	–
C	RSTAT	RCON	–	–
D	ALICNT	*TCON	–	–
E	CRCCNT	*DCON	–	–
F	MPCNT	INTMASK	–	–

TABLE B-1. REGISTER ADDRESSES

*Register contains new or modified bits.

REG ADDR	PAGE 2 READ	PAGE 2 WRITE	PAGE 3 READ	PAGE 3 WRITE
0	COMMAND	COMMAND	COMMAND	COMMAND
1	RSTART	*TRINCRL	*TEST	*TEST
2	RSTOP	*TRINCRH	–	–
3	–	–	–	–
4	TSTART	–	–	–
5	NEXT	NEXT	–	–
6	*BLOCK	*BLOCK	–	–
7	*ENH	*ENH	–	–
8	–	–	–	–
9	–	–	–	–
A	–	–	–	–
B	–	–	–	–
C	RCON	–	–	–
D	*TCON	–	–	–
E	*DCON	–	–	–
F	INTMASK	–	–	–

TABLE B-1. REGISTER ADDRESSES (Continued)

*Register contains new or modified bits.

40

Name:	**R/W Addr:**
ALICNT	OD/–

Description: This register is the alignment error counter. It is incremented by the receive unit when a packet is received with a frame alignment error. Only packets whose address is accepted are included in the tally. The counter increments to 255, then stops. It clears when read.

MSB	7	6	5	4	3	2	1	0
NAME	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
INIT	0	0	0	0	0	0	0	0

Name:	**R/W Addr:**
BLOCK	26/26

Description: This is a page register for the upper 8 bits of memory address. During each memory/transfer cycle, the contents of this register are driven out onto the A16-A23 pins, which are not multiplexed and need not be latched by the host system.

MSB	7	6	5	4	3	2	1	0
NAME	A23	A22	A21	A20	A19	A18	A17	A16
INIT	0	0	0	0	0	0	0	0

Name:	**R/W Addr:**
BOUND	03/03

Description: To prevent overflow in the buffer ring, the receive boundary page register points to the oldest used receive buffer. TRDMA compares the contents of this register to the next buffer address when linking together buffers to store a received frame. If the contents match the next buffer address, the TRDMA operation is aborted. Because all buffers are aligned on 256-byte boundaries, only A08–A15 are specified.

MSB	7	6	5	4	3	2	1	0
NAME	A15	A14	A13	A12	A11	A10	A09	A08
INIT	0	0	0	0	0	0	0	0

Name:	**R/W Addr:**
COLCNT	05/–

Description: This register contains the number of collisions detected during attempted transmission of the current (or most recent) packet. It is cleared at the start of transmission. For each collision encountered, the count is incremented. If no collisions are detected, the counter reads zero. If more than 15 collisions occur, the abort bit of TSR is set and the count is reset to zero.

MSB	7	6	5	4	3	2	1	0
NAME	0	0	0	0	CT3	CT2	CT1	CT0
INIT	0	0	0	0	0	0	0	0

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS

Name:	R/W Addr:
COMMAND	x0/x0

Description: The command register is used to initialize the device, start transmissions, and switch pages.

MSB	7	6	5	4	3	2	1	0
NAME	PS1	PS0	CMD.5	CMD.4	CMD.3	TXP	STA	STP
INIT	0	0	1	0	0	0	0	1

Notes:

PS1, PS0 — Page select, a two-bit field.

Bits 5,4,3 — These bits may be read and written to, but they control no hardware in the WD83C690. (They were used for remote DMA control in the National 8390.)

TXP — Transmit packet. Set this bit after loading transmit buffer and control registers to initiate transmission of a packet. The WD83C690 clears this bit upon completion, or abortion, of the transmission. The host can clear the bit by setting TESTMODE in the TEST CONTROL register and writing "0" into COMMAND.TXP. When TESTMODE is not set, writing "0" into COMMAND.TXP is ignored.

STA — Start bit. This bit is set by the user to activate the WD83C690 after power is applied or after the WD83C690 is reset. (Although the user's software should set the other registers prior to bringing the device on line, this is the actual command that allows normal operation of the transmit and receive portions of the device.) Until the register is set, no frames can be sent or received. Once set, this bit may be cleared and the WD83C690 will continue to remain online.

STP — Stop bit. Set this bit to stop the device via the software. The bit takes the device offline from the LAN. Frames partially transmitted or received are completed before reset occurs. ISR.RST is set high when the transmit and receive sections have completed all outstanding operations. No frames will be received until the start bit is set. Receiver status reqs are reinitialized when this command is executed.

Name:	R/W Addr:
CRCCNT	0E/–

Description: This register is the CRC error counter. It is incremented by the receive unit when a packet is received with a CRC error. Only packets whose address is accepted are included in the tally. The counter stops at 255, and clears when read.

MSB	7	6	5	4	3	2	1	0
NAME	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
INIT	0	0	0	0	0	0	0	0

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

40

Name:	**R/W Addr:**
CURR	17/17

Description: This register points to the first buffer used to store the current frame. It is used internally by TRDMA to facilitate the storage of buffer header information, and to provide a backup address for recovering buffers in case of a flawed packet. The register should be initialized after the device has been reset and thereafter not altered by the user unless the ring overflows. Note: Because all buffers are aligned on 256-byte boundaries, only A08 through A15 are specified.

MSB	7	6	5	4	3	2	1	0
NAME	A15	A14	A13	A12	A11	A10	A09	A08
INIT	0	0	0	0	0	0	0	0

Name:	**R/W Addr:**
DCON	2E/0E

Description: The data configuration register defines characteristics of the memory interface.

MSB	7	6	5	4	3	2	1	0
NAME	–	BSIZE1	BSIZE0	–	–	–	–	BUS16
INIT	0	0	0	0	0	0	0	0

Notes:

BSIZE1,0 This two-bit field determines the length of DMA bursts and the FIFO threshold at which they are triggered. As a rule, each FIFO triggers its DMA when there is adequate room for an entire burst to fit in.

TRANS

BSIZE1	BSIZE0	BURST	RECV TRIG LEVEL	TRIG LEVEL
0	0	2 bytes	R≥2	T≤4
0	1	4 bytes	R≥4	T≤12
1	0	8 bytes	R≥8	T≤8
1	1	12 bytes	R≥12	T≤4

Bits 7,4,3,2,1 Not used.

BUS16 "1" tells the WD83C690 to make all DMA transfers 16 bits wide. "0" tells the WD83C690 to make all DMA transfers 8 bits wide.

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

Name: ENH **R/W Addr:** 27/27

Description: This register enables features that are unique to the WD83C690.

MSB	7	6	5	4	3	2	1	0
NAME	WAIT1	WAIT0	–	SLOT1	SLOT0	–	–	—
INIT	0	0	0	0	0	0	1	0

Notes:

WAIT1
WAIT0 This two-bit field defines the default number of wait states the WD83C690 inserts into every DMA cycle.

WAIT1	WAIT0	WAIT STATES
0	0	0
0	1	1
1	0	2
1	1	3

SLOT1,
SLOT0 This two-bit field selects the slot time according to the following table.

SLOT1	SLOT0	SLOT TIME
0	X	512 bit times – Ethernet, StarLAN
1	0	256 bit times
1	1	1024 bit times

Name: INIT MASK **R/W Addr:** 2F/0F

Description: This register is used to selectively mask interrupt sources. Mask bits that are "1" allow the corresponding interrupts to cause an IRQ. Mask bits that are "0" block interrupt sources.

MSB	7	6	5	4	3	2	1	0
NAME	–	XDCE	CNTE	OVWE	TXEE	RXEE	PTXE	PRXE
INIT	0	0	0	0	0	0	0	0

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

40

Name:	**R/W Addr:**
INT STATUS	07/07

Description: This register enables the host to determine the cause of an interrupt and to evaluate pending or masked interrupts (which are visible in this register even though they do not generate an IRQ). Pending interrupts can be cleared by writing "1" into the associated bit of this register. The IRQ signal is active as long as any unmasked interrupt bit remains set.

MSB	7	6	5	4	3	2	1	0
NAME	RST	–	CNT	OVW	TXE	RXE	PTX	PRX
INIT	1	0	0	0	0	0	0	0

RST — Reset status. This bit, which does not generate an interrupt, is set by the WD83C690 when its transmit and receive sections are stopped in response to assertion of the RESET pin or the CMD.STP bit.

BIT 6 — This bit is unused in the WD83C690. It always returns 0 when read.

CNT — The counter overflow bit indicates that the MSB of one or more network error counters has been set.

OVW — The overwrite warning bit is set when the receive DMA attempts to write into the buffer pointed to by the boundary register.

TXE — Transmit error is set when there are excessive collisions, or when FIFO underrun prevents a packet from being transmitted.

RXE — Receive error is set when a packet is received with one or more of the following errors:

- CRC error
- Frame alignment error
- FIFO overrun
- Missed packet (monitor mode)

This interrupt is not posted if DMA abort occurs. (OVW interrupt indicates that condition.) If, however, the interrupt has been previously set, it will not be changed due to OVW.

PTX — Packet transmitted indicates that a packet was successfully transmitted.

PRX — Packet received indicates that a packet was received with no errors. This interrupt is not posted if DMA abort occurs. If previously set, it will not be changed due to OVW.

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

Name:	R/W Addr:
MPCNT	0F/–

Description: This register is the missed packet error counter. It is incremented by the receive unit when a packet cannot be received due to a lack of receive buffers, receive FIFO overflow, or because the receiver is in monitor mode. Only packets whose address is accepted are included in the tally. The counter stops at 255, and clears when read.

MSB	7	6	5	4	3	2	1	0
NAME	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
INIT	0	0	0	0	0	0	0	0

Name:	R/W Addr:
NEXT	25/25

Description: This is a working register of the TRDMA controller. It holds a pointer to the next buffer to be opened.

MSB	7	6	5	4	3	2	1	0
NAME	A15	A14	A13	A12	A11	A10	A09	A08
INIT	0	0	0	0	0	0	0	0

Name:	R/W Addr:
RCON	2C/0C

Description: The receive configuration register defines optional behavior of the receive unit. It controls both address recognition and the acceptance of abnormal packets. These bits can be set independently, although monitor mode takes precedence over the others.

MSB	7	6	5	4	3	2	1	0
NAME	–	–	MON	PROM	GROUP	BROAD	RUNTS	SEP
INIT	0	0	0	0	0	0	0	0

Notes:

MON — When set, this bit enables the receive unit to check addresses and CRC on incoming packets without buffering them to memory. The missed packet counter is incremented for each recognized packet. Under normal operation, this bit is cleared to "0".

PROM — When set to "1", this bit enables promiscuous reception of all frames having individual addresses.

GROUP — Setting this bit enables reception of all frames destined to multicast (group) addresses other than broadcast frames.

BROAD — Setting this bit enables reception of all frames having a broadcast destination address.

RUNTS — Setting this bit enables the WD83C690 to receive frames with fewer than 64 bytes, provided they meet the other requirements of the IEEE 802.3 protocol.

SEP — Setting the saved error packets bit to "1" causes the receive unit to save packets having CRC or frame alignment errors in the buffers.

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

Name:	**R/W Addr:**
RSTART	21/01

Description: The receive start page register points to the start of the receive buffer ring. Because all buffers are aligned on 256-byte boundaries, only A08 through A15 are specified.

MSB	7	6	5	4	3	2	1	0
NAME	A15	A14	A13	A12	A11	A10	A09	A08
INIT	0	0	0	0	0	0	0	0

Name:	**R/W Addr:**
RSTAT	0C/–

Description: The receive status register reports the status of the most recently received packet, categorizing any errors detected. At the start of reception, all bits are cleared except DIS.

MSB	7	6	5	4	3	2	1	0
NAME	DFR	DIS	GROUP	MPA	OVER	FAE	CRC	PRX
INIT	0	0	0	0	0	0	0	0

DFR — The deferring bit is set when the interframe gap state machine is deferring. If the transceiver asserts the CD line as a result of jabber, this bit remains set, indicating a jabber condition.

DIS — The receiver disabled bit is set when the receiver is in monitor mode. It is cleared when the receiver leaves monitor mode.

GROUP — This bit is set when the address is a group address (multicast) or broadcast. It is cleared to indicate an individual (physical) address match.

MPA — The missed packet address is set when a packet intended for this station cannot be accepted by the device due to a lack of receive buffers or because the device is in monitor mode. The missed packet counter is also incremented when this occurs.

OVER — The FIFO overrun bit is set when the receiver attempts to write into a FIFO that is already full. This can occur when the TRDMA fails to keep up with the received data.

FAE — A frame alignment error indicates that the incoming packet did not end on a byte boundary and the CRC did not match at the last byte boundary. Frames having 7 dribble bits are reported as alignment errors. The alignment error counter is incremented when this condition occurs.

CRC — When set, this bit indicates that the frame's computed CRC did not correspond to the CRC appended to the end of the frame. This error also causes the CRC counter to be incremented.

PRX — When the packet received intact bit is set to "1, it indicates that a packet was received without error. (This means that CRC, FAE, OVER, and MPA all equal 0.)

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

Name:	R/W Addr:
RSTOP	22/02

Description: Prior to wrapping around to the RSTART buffer, the receive stop page register points to the last receive buffer in the ring. Because all buffers are aligned on 256-byte boundaries, only A08 through A15 are specified.

MSB	7	6	5	4	3	2	1	0
NAME	A15	A14	A13	A12	A11	A10	A09	A08
INIT	0	0	0	0	0	0	0	0

Name:	R/W Addr:
STA 0	11/11
STA 1	12/12
STA 2	13/13
STA 3	14/14
STA 4	15/15
STA 5	16/16

Description: These six registers contain the node's individual station address.

STA0:	DA07	DA06	DA05	DA04	DA03	DA02	DA01	DALSB
STA1:	DA15	DA14	DA13	DA12	DA11	DA10	DA09	DA08
STA2:	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
STA3:	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
STA4:	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
STA5:	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40

Name:	R/W Addr:
TCNT H	–/06
TCNT L	–/05

Description: Together, the transmit frame length high- and low-byte registers hold the byte count for the frame to be transmitted. The byte count includes the DA, SA and data fields. If CRC generation is inhibited, the count also includes the CRC field in the buffer.

TCNT H:

MSB	7	6	5	4	3	2	1	0
NAME	L15	L14	L13	L12	L11	L10	L09	L08
INIT	0	0	0	0	0	0	0	0

TCNT L:

MSB	7	6	5	4	3	2	1	0
NAME	L7	L6	L5	L4	L3	L2	L1	L0
INIT	0	0	0	0	0	0	0	0

40

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

Name: TCON — **R/W Addr:** 2D/0D

Description: The transmit configuration register controls loopback options, data rate options, and Manchester codes.

MSB	7	6	5	4	3	2	1	0
NAME	TCON7	TCON6	TCON5	TCON4	TCON3	LB1	LB0	CRCN
INIT	0	0	0	0	0	0	0	0

Notes:

TCON7,6,5,4,3 These bits are writable and readable, but have no function in the WD83C690. They are reserved for future enhancements.

LB1,LB0 This two-bit field is for selecting loopback options.

LB1	LB0	OPERATION
0	0	Normal (no loopback)
0	1	Internal loopback just inside WD83C690 pins
1	0	External loopback with LOOP pin high
1	1	External loopback with LOOP pin low

CRCN Setting this bit inhibits generation of CRC during transmission of the frame. The user is responsible for calculating the frame's CRC and placing it in the buffer so that, when the last 4 bytes of the buffer are shifted out, they form the correct CRC for the frame. Note that the serializer shifts bytes out of LSB first, whereas the CRC shifts bytes out of MSB first.

The operation of the receiver is unaffected by this bit.

Name: TEST — **R/W Addr:** 31/31

Description: This register, which is reserved, enables various internal test modes of the WD83C690, as well as host access to sensitive internal registers. It is important that you do not write to this register.

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

Name:	R/W Addr:
TRINCRH	02/22
TRINCRL	01/21

Description: This register pair is the address incrementer for the TRDMA unit. Its value approximates the memory address associated with the next TRDMA operation. The information is approximate because the LSB of the address is not accessible when operating in 8-bit bus mode. Additional uncertainty arises because of an internal one-word-deep address pipeline in the memory data transfer logic.

The address obtained from these registers is usually the address of the lower half of the word just transferred, or the address of the lower half of the word to be transferred next. The word address applies even when the bus is being operated byte-wide.

If these registers are read during the beginning or end of either transmission or reception, meaningless values may be obtained. The incrementer is used for pointer update and length modification calculations during these periods.

TRINCR H:

MSB	7	6	5	4	3	2	1	0
NAME	A15	A14	A13	A12	A11	A10	A09	A08
INIT	1	1	1	1	1	1	1	1

TRINCR L:

MSB	7	6	5	4	3	2	1	0
NAME	A07	A06	A05	A04	A03	A02	A01	A00
INIT	1	1	1	1	1	1	1	1

Name:	R/W Addr:
TSTART	24/04

Description: The transmit start page register points to the assembled packet to be transmitted. Because all frames are assembled on 256-byte boundaries, only A08 through A15 are specified.

MSB	7	6	5	4	3	2	1	0
NAME	A15	A14	A13	A12	A11	A10	A09	A08
INIT	0	0	0	0	0	0	0	0

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

Name:	**R/W Addr:**
TSTAT	04/–

Description: The transmit status register reports events that occur on the media while a packet is transmitted. All bits are cleared prior to transmission of a packet and set as needed.

MSB	7	6	5	4	3	2	1	0
NAME	OWC	CDH	UNDER	CRL	ABORT	TWC	NDT	PTX
INIT	0	0	0	0	0	0	0	0

Notes:

OWC	The out-of-window-collision bit is set if a collision is detected more than one slot time after transmission begins. The transmission is not aborted when this occurs.
CDH	This is the collision detect heartbeat bit. It is set when heartbeat is detected.
UNDER	The FIFO underrun bit it set when the transmit unit attempts to read from an empty FIFO prior to receiving the TDONE flag from TRDMA. It means that the FIFO failed to supply enough data for the serializer to maintain the generation of a frame.
CRL	The carrier sense lost bit is set when the carrier is lost while a packet is being transmitted. Carrier sense is monitored from its rising edge at the start of the outgoing frame's echo. Transmission is not aborted upon loss of the carrier, but the event is reported for statistical purposes.
ABORT	This bit is set if the transmission is aborted because of excessive collisions.
TWC	The transmitted-with-collisions bit is set when a transmitted frame collides (at least once) with another frame.
NDT	The non-deferred transmission bit is set when the frame is transmitted successfully without deferring. A deferred transmission can occur only the first time an attempt is made to send a packet. Collisions are not deferred transmissions.
PTX	The packet transmitted bit is set to indicate (1) transmission of a packet without excessive collisions or (2) a FIFO underrun.

TABLE B-2. ALPHABETICAL REGISTER DESCRIPTIONS (Continued)

C.0 APPENDIX C

C.1 PIN DESIGNATIONS

Figure C-1 illustrates the 68-pin Ethernet controller.
Table C-1 lists all pin designations.

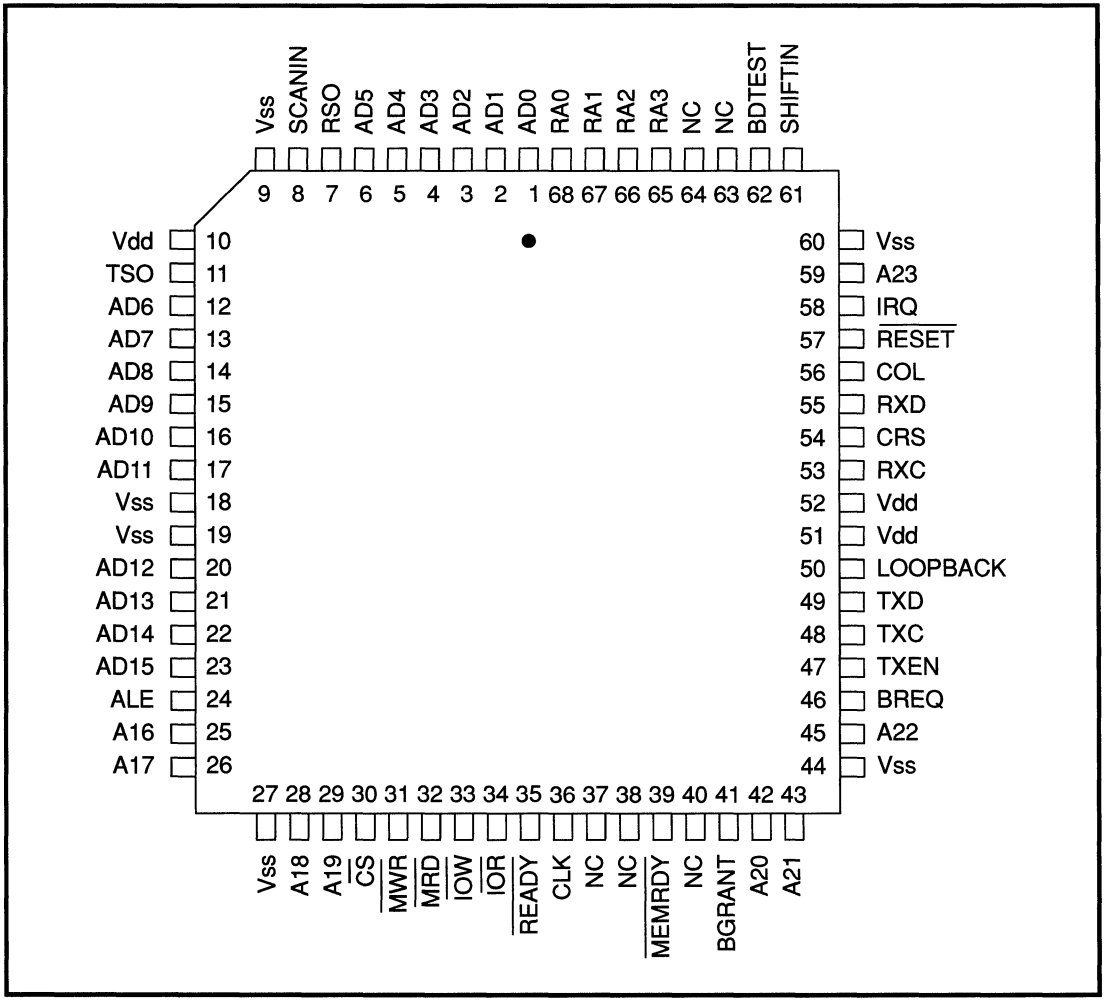


FIGURE C-1. 68-PIN ETHERNET CONTROLLER

40

PIN	DIR	NO.	DESCRIPTION
A16 A17 A18 A19 A20 A21 A22 A23	OUT TRI	25 26 28 29 42 43 45 59	Highest address lines. These are used to define the page address for the buffer memory block. In systems having 64 Kbytes or less of local memory, they are unused. The value of these pins is programmed into the BLOCK ADDRESS register.
AD00 AD01 AD02 AD03 AD04 AD05 AD06 AD07 AD08 AD09 AD10 AD11 AD12 AD13 AD14 AD15	BIDIR TRI	01 02 03 04 05 06 12 13 14 15 16 17 20 21 22 23	Multiplexed address/data lines when internal DMA channels are active and granted access to the local memory bus. When bus access is not permitted, AD00 – AD07 become input/output pins for host data bus, and AD08 – AD15 are tri-stated.
ALE	BIDIR TRI	24	Address latch enable goes high when DMA address is driven onto AD00 - AD15. It goes low to latch address externally. When accessed by the host, this pin is an input which serves to transparently latch the RA0-3 address lines internally on the falling edge.
$\overline{\text{BDTEST}}$	IN	62	This pin tri-states the following output pins when pulled low: BREQ, IRQ, LOOPBACK, READY, RSO, TSO, TXD, TXEN. It may also be used to facilitate in-circuit testing of boards. This pin is pulled up by an internal resistor.
BREQ	OUT TRI	46	Bus request (active high). This pin goes high for the WD83C690 to request access to the local memory bus. It stays high throughout the DMA burst.
BGRANT	IN	41	Bus grant (active high). When active, the internal DMA channels drive the AD pins and strobes as needed to perform DMA transfers. When inactive, any ongoing DMA transfers are completed, and the DMA strobe pins tri-state.

TABLE C-1. PIN DESIGNATIONS

PIN	DIR	NO.	DESCRIPTION
CLK	IN	36	Master clock input for the device. Internal operation is timed relative to this clock. In normal operation, the clock must be 20 MHz.
COL	IN	56	Collision detection input (active high). This pin must be pulled low when external circuit detects collision conditions on the network.
CRS	IN	54	Carrier sensed (active high). This pin is driven by an external decoder circuit.
$\overline{CS}$	IN	30	Chip select is active low.
$\overline{IOR}$	IN	34	I/O read (active low). Internal registers can be written to when CS and IOR are active.
$\overline{IOW}$	IN	33	I/O write (active low). Internal registers can be written to when CS and IOW are active.
IRQ	OUT TRI	58	Interrupt request (active high).
LOOP-BACK	OUT TRI	50	Loopback goes high when either of the external loopback modes is programmed in the TRANSMIT CONFIGURATION register.
$\overline{MEMRDY}$	IN	39	Memory ready (active low). Memory ready is negated externally to insert wait states into DMA transfers.
$\overline{MRD}$	OUT TRI	32	Memory read strobe output for the DMA channels (active low).
$\overline{MWR}$	OUT TRI	31	Memory write strobe output for the DMA channels (active low).
RA0 RA1 RA2 RA3	IN	68 67 66 65	Register address 0,1,2,3 (active high). RA0 is the least significant. These lines combine with two bits in the COMMAND register to select an internal WD83C690 register during host I/O access to the device.
$\overline{READY}$	OUT TRI	35	Register access ready (active low) is asserted by the WD83C690 when host access to the internal register is ready.

TABLE C-1. PIN DESIGNATIONS (Continued)

40

PIN NAME	DIR	NO.	DESCRIPTION
$\overline{\text{RESET}}$	IN	57	Active low. Asserting this pin forces the WD83C690 to a known (initial) state. The device remains in its initial state until the line is released.
RSO	OUT TRI	7	This pin is the data output for level-sensitive scan testing of the receiver section. The pin should be left open in board applications.
RXC	IN	53	Serial receive clock is active on its rising edge.
RXD	IN	55	Serial receive data (active high) is connected to decoded serial data from the network.
SCANIN	IN	8	This pin is used to gate the level-sensitive scanning clock during testing of the device. This pin must be left open or tied to ground in board applications.
SHIFT-IN	IN	61	This pin serves as data input for level-sensitive scan testing of the device. The pin must be left open or tied to ground in board applications.
TSO	OUT TRI	11	This pin is the data output for level-sensitive scan testing of the transmit section. The pin must be left open in board applications.
TXC	IN	48	Serial transmit clock is active on its rising edge.
TXD	OUT TRI	49	Serial transmit data (active high) is NRZ-encoded.
TXEN	OUT TRI	47	Serial transmitter enable is used to enable the LAN driver during transmission of a frame. This signal is active high.
Vdd (3)		10 51 52	+5 dc power inputs.
Vss (6)		09 18 19 27 44 60	Ground returns for power.

TABLE C-1. PIN DESIGNATIONS (Continued)

D.0 APPENDIX D

D.1 OPERATING CHARACTERISTICS

This appendix describes the dc and ac operating characteristics. Recommended operating conditiions are listed below.

D.2 RECOMMENDED OPERATING CONDITIONS

Minimum Ambient Temperature = 0°C (32°F)
Maximum Ambient Temperature = 85°C (185°F)
Minimum Vdd = 4.75V
Maximum Vdd = 5.25V

D.3 DC PARAMETERS

The input pins have the following parameters:

v_{IL}= 0.8V
i_{IL}= 50µA (except $\overline{BDTEST}$, which is 200 µA)

v_{IH}= 2.0V
i_{IH}= 50µA

AD00 – 15 have the following dc parameters:

v_{OL} = 0.4V
i_{OL}= 1.6 mA

v_{OH}= 2.7V
i_{OH}= 0.1 mA

All other outputs have the following dc parameters:

v_{OL}= 0.4V
i_{OL}= 0.8 mA

v_{OH}= 2.7V
i_{OH} = 0.1 mA

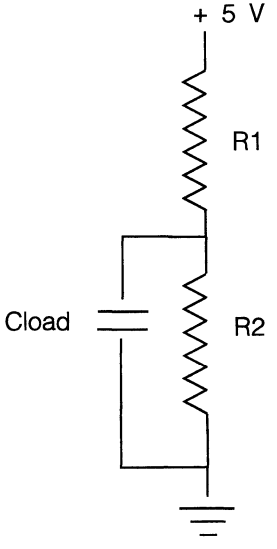
D.4 AC PARAMETERS (TIMING)

The test load for the AD00-15, MRD, and MWR outputs is:

Cload = 60 pF
R1 = 2.64 KOhms
R2 = 2.78 KOhms

The test load for all other outputs is:

Cload = 25 pF
R1 = 5.23 KOhms
R2 = 5.0 KOhms



40

REF	FROM	TO	MIN	MAX	NOTES
T01	CLK	ALE	0	40	–
T02	$\overline{CLK}$	$\overline{ALE}$	0	40	–
Tre11	ALE	$\overline{ALE}$	15	–	–
T03	CLK	Valid Address AD00 – AD15	0	35	–
T04	CLK	AD00 — AD15 (– AD07) high impedance	3	45	–
Tre12	ADxx valid	$\overline{ALE}$	8	–	–
T05	$\overline{CLK}$	MRD	3	35	–
T06	CLK	$\overline{MRD}$	0	35	–
T07	CLK	MWR	0	32	–
T08	$\overline{CLK}$	$\overline{MWR}$	3	30	–
T09	$\overline{CLK}$	Valid Data AD00 – AD15	0	45	–
T10	CLK	AD00 – AD15 (– AD07) high impedance	3	45	–
T14	CLK	BREQ	0	35	–
T15	CLK	$\overline{BREQ}$	0	35	–
T16	CLK	A16-23, ALE MRD, MWR low impedance	0	35	–
T17	CLK	A16-23, ALE, MRD, MWR high impedance	0	35	–
T20	CS	READY	100	200	1*
T21	IOR or IOW	READY	50	150	1

TABLE D-1. OUTPUT TIMING

*Refer to Notes on p. 40-40.

REF	FROM	TO	MIN	MAX	NOTES
T22	CLK	READY	0	35	–
T23	CLK after IOR	AD00-07 low impedance	0	45	–
T24	CLK after IOR	Data valid	0	95	2*
T25	$\overline{IOR}$	AD00-07 high impedance	0	45	–
T26	$\overline{IOR}$ and $\overline{IOW}$	$\overline{READY}$	0	45	–
T27	CLK	TXEN or TXD	0	45	–
T28	TXEN	$\overline{TXD}$	1 CLK	1 BT	–
T29	TXC	TXD valid	0	47	–
T30	CLK	$\overline{TXEN}$	0	45	–
T31	COL	First bit of JAM	4 BT	6 BT	–
T32	End of last TXD bit	$\overline{TXEN}$	50	100	–
T33	BDTEST	Outputs high impedance	0	95	–
T34	$\overline{BDTEST}$	Outputs low impedance	0	95	–
T35	CLK	IRQ or $\overline{IRQ}$	0	45	–
T36	CLK	LOOPBACK or $\overline{LOOPBACK}$	0	45	–
T37	CLK	TSO, RSO valid	0	45	–
T38	BREQ	ALE	2	2 CLKS	3
T39	BGRANT	A16-23, ALE, MRD, MWR low impedance	2	2 CLKS	–

TABLE D-1. OUTPUT TIMING (Continued)

*Refer to Notes on p. 40-40.

40

REF	FROM	TO	MIN	MAX	NOTES
T40	$\overline{\text{BGRANT}}$ $\overline{\text{BREQ}}$	A16-23, ALE, MRD, MWR high impedance	2	2 CLKS	–
T41	$\overline{\text{MRD}}$ and $\overline{\text{MWR}}$ (last transfer)	$\overline{\text{BREQ}}$	1	4 CLKS	–
T42	ALE	Next ALE in receive DMA burst on 16-bit bus.	7	8 CLKS	4*
T43	ALE	Next ALE in transmit DMA burst on 16-bit bus	5	5 CLKS	4
T50	IOW	$\overline{\text{IOW}}$	100	–	–
T51	RXC	$\overline{\text{RXC}}$	35	–	–
T52	$\overline{\text{RXC}}$	RXC	35	–	–
T53	RXC	RXC – clock period	99	–	–
T54	RXC of first preamble bit	First RXC of SFD (preamble length)	6 BT	–	–
T55	RXC of last data bit	Last RXC prior to CRS (dribble bits)	0 BT	6 BT	–
T56	Last RXC prior to $\overline{\text{CRS}}$	Last RXC (dribble bits)	5 BT	–	–
T57	$\overline{\text{CRS}}$	CRS and Start – of Frame	27 BT	–	8
T58	TXC	$\overline{\text{TXC}}$	35	–	–
T59	$\overline{\text{TXC}}$	TXC	35	–	–

TABLE D-1. OUTPUT TIMING (Continued)

*Refer to Notes on p. 4-40.

REF	FROM	TO	MIN	MAX	NOTES
T60	TXC	TXC – clock period	2 CLKS	20 CLKS	9*
T61	$\overline{CLK}$	TXC, $\overline{TXC}$	0	30	9
T62	$\overline{TXEN}$	COL (heartbeat detect)	0	59 BT	10
T63	COL	$\overline{COL}$ (collision width)	1 BT	–	–
T64	Vdd = 4.75V	$\overline{RESET}$	10 CLKS	–	–
T65	RESET	$\overline{RESET}$	10 CLKS	–	–
T66	CLK	$\overline{CLK}$	23	800	–
T67	$\overline{CLK}$	CLK	23	800	–
T68	CLK	CLK	50	1600	9
T69	ALE	$\overline{ALE}$	15	–	–

TABLE D-1. OUTPUT TIMING (Continued)

*Refer to Notes on p. 4-40.

REF	FROM	TO	MIN	MAX	NOTES
TS01	Data Valid	CLK	15	–	–
TS02	$\overline{\text{MEMRDY}}$ or MEMRDY	CLK #2	15	–	5
TS04	BGRANT, $\overline{\text{BGRANT}}$	CLK	15	–	–
TS05	DMA pins undriven	BGRANT	0	–	–
TS06	TXC	$\overline{\text{CLK}}$	10	–	–
TS07	CS, IOR, IOW	CLK	15	–	6
TS08	RA0-3 valid	CS and (IOR or IOW)	0	–	–
TS09	RA0-3 valid	$\overline{\text{ALE}}$	15	–	–
TS10	Data valid	$\overline{\text{IOW}}$	25	–	–
TS11	CRS or $\overline{\text{CRS}}$	RXC	15	–	–
TS12	RXD valid	RXC	15	–	–
TH01	$\overline{\text{MRD}}$	Data invalid	0	–	–
TH02	CLK #2	MEMRDY, $\overline{\text{MEMRDY}}$	15	–	–
TH03	$\overline{\text{CLK}}$	TXC edge	10	–	–
TH04	$\overline{\text{IOR}}$ and $\overline{\text{IOW}}$	RA0-3 invalid	0	–	7
TH05	$\overline{\text{IOW}}$	Data invalid	10	–	–
TH06	$\overline{\text{ALE}}$	RA0-3 invalid	10	–	–
TH07	RXC	RXD invalid	15	–	–

TABLE D-2. INPUT TIMING SETUP AND HOLD REQUIREMENTS

NOTES

1. These maximum times apply if, when the device is selected, there is no ongoing DMA. When there is ongoing DMA, the maximum times apply after BREQ = 0 and BGRANT = 0.
2. This applies after the first clock for which IOR meets the setup requirement.
3. This is the delay between the time the bus is requested and internal DMA is ready to use the bus. Timing T39 is also satisfied and usually controls when DMA uses the bus.

NOTES (continued):

4. These are the minimum durations of DMA transfers on 16-bit busses. The receive transfer requires 4 cycles, plus wait states, with an interval of 3 or 4 clocks after completion of a 16-bit transfer. The transmit transfer is the same except that the interval after completion is only 1 clock. Because some versions of the device do not have this gap, we recommend that you not use the bus during the interval between the 16-bit transfers.

   There is no interval between 8-bit transfers. They require 4 cycles, plus wait states.

5. This timing must be met to control insertion of wait states.

6. To minimize the delay to READY, this timing needs to be met. Failure to meet this timing may add an extra clock delay to the onset of the READY signal, but does not adversely affect access to the device.

7. This timing applies only when ALE remains high during host access, as is the case with non-multiplexed or externally-latched addresses and data. The addresses must be stable throughout access to the device.

8. This is the time required from the end of one frame to the reception of the SFD delimiter of the next frame. The limiting factor in reception of back-to-back frames is the time required for DMA to post the header of the received frame. This depends on memory speed and on access to the bus. The interval given here is based on memory with two wait states, and the ability to access the bus within 5 clocks after request.

9. Operation of this device in an 802.3 network requires a CLK period of 50 nsec $\pm$ 0.01%. TXC must be generated synchronously from CLK. The TXC period may be 2 CLKS, 10 CLKS, or 20 CLKS.

10. The maximum time is 63 bit times from CRS going low if that does not occur more than 4 bit times prior to TXEN going inactive.

D.5 TIMING DIAGRAMS

Table D-3 lists all timing diagrams. Figures D-1 through D-14 illustrate all timings.

Figure	Title
D-1	Host Access Timing
D-2	16 -Bit Bus, 4-Cycle DMA Read and Write Timing
D-3	16-Bit Bus, 5-Cycle DMA Read and Write Timing
D-4	8-Bit Bus, DMA Read and Write Timing
D-5	Bus Request Timing for Normal DMA Burst
D-6	16-Bit Bus DMA Burst Timing
D-7	DMA Burst Timing – Bus Busy
D-8	8-Bit Bus, Interrupted DMA Burst
D-9	Receiver Serial Timing , Start of Frame
D-10	Receiver Serial Timing , End of Frame
D-11	Transmit Serial Timing , Start of Frame
D-12	Transmit Serial Timing , End of Frame
D-13	Transmit Serial Timing , Collision
D-14	Other Timing

TABLE D-3. LIST OF TIMING DIAGRAMS

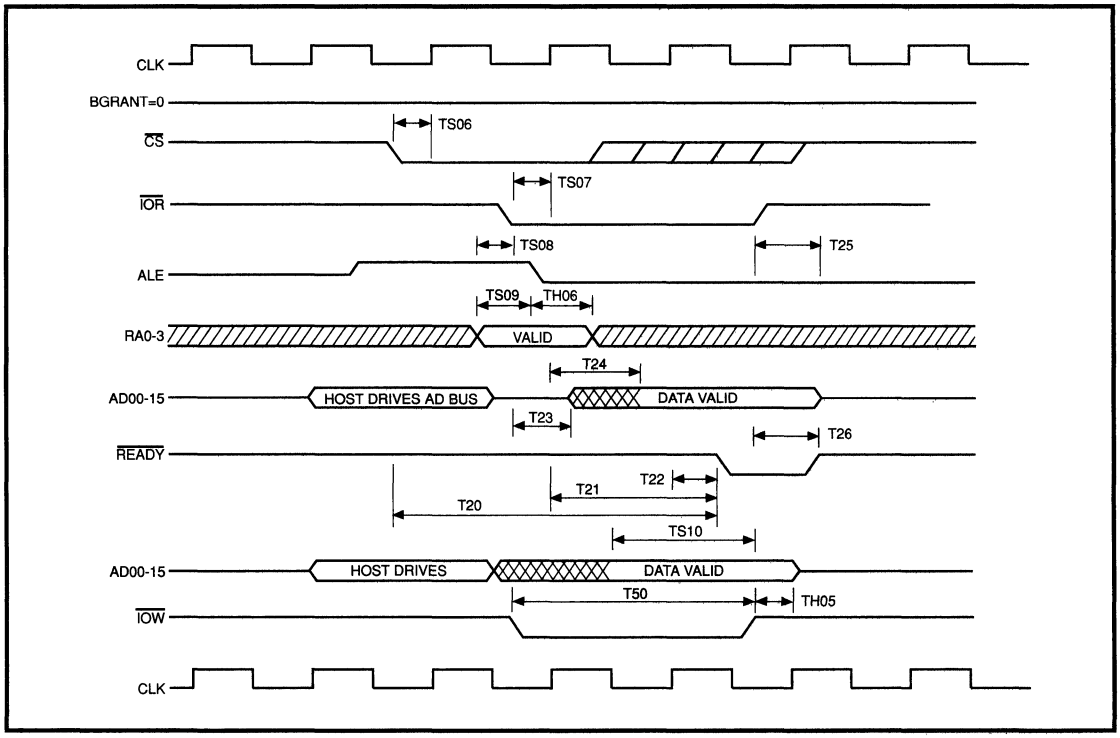


FIGURE D-1. HOST ACCESS TIMING

40

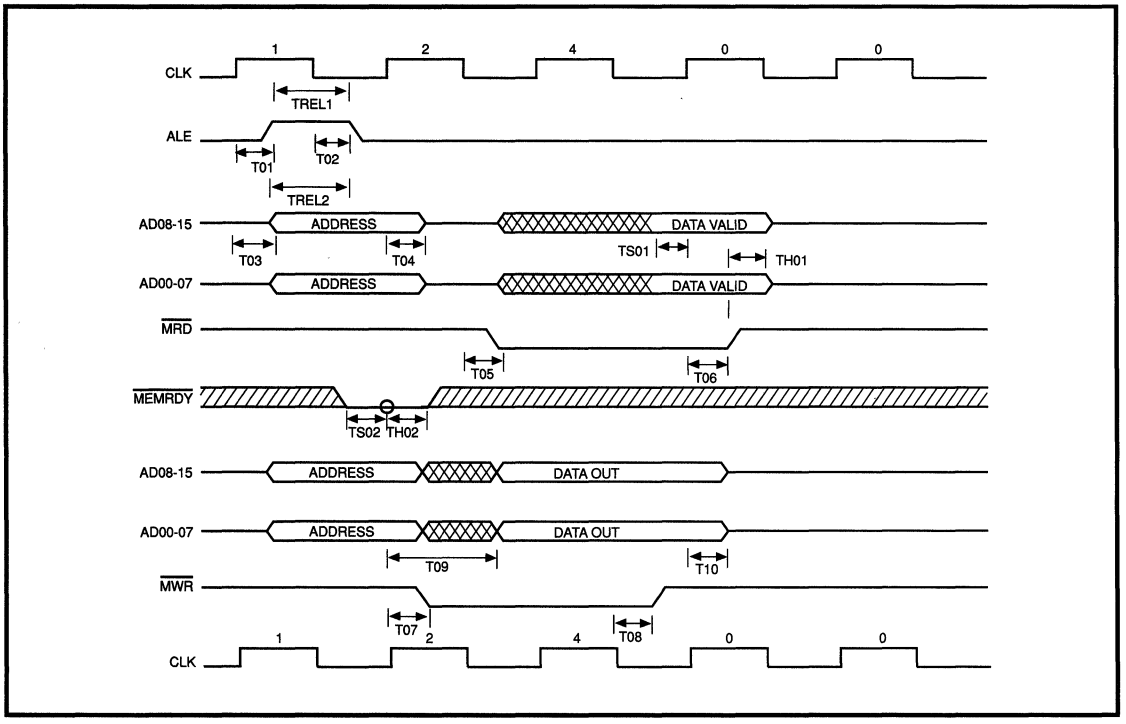


FIGURE D-2. 16-BIT BUS, 4-CYCLE DMA READ AND WRITE TIMING

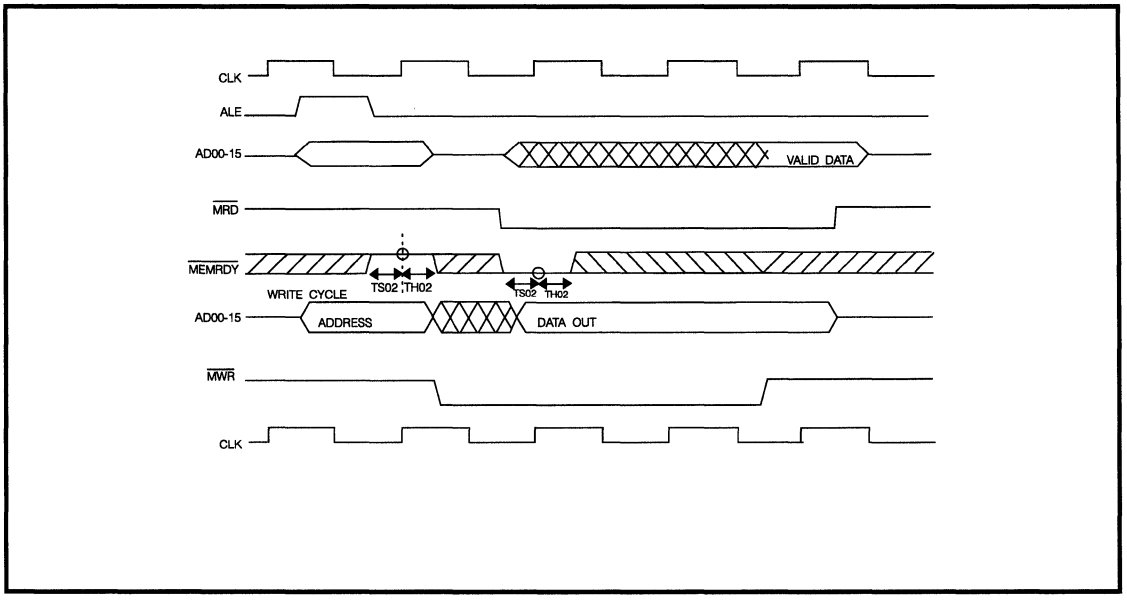


FIGURE D-3. 16-BIT BUS, 5-CYCLE DMA READ AND WRITE TIMING

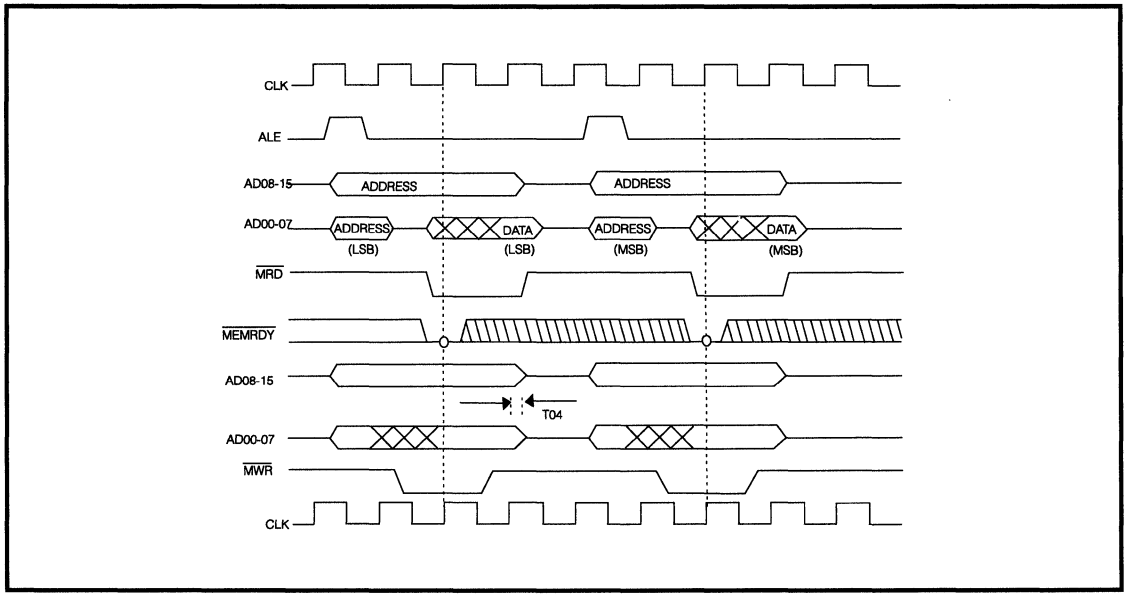


FIGURE D-4. 8-BIT BUS, DMA READ AND WRITE TIMING

40

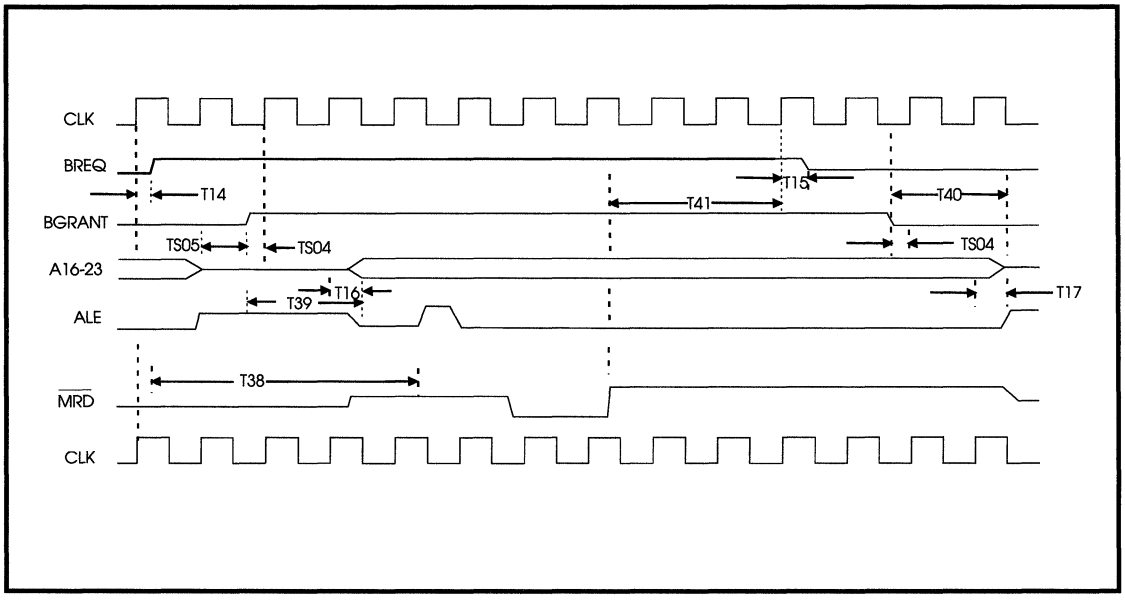


FIGURE D-5. BUS REQUEST TIMING FOR NORMAL DMA BURST

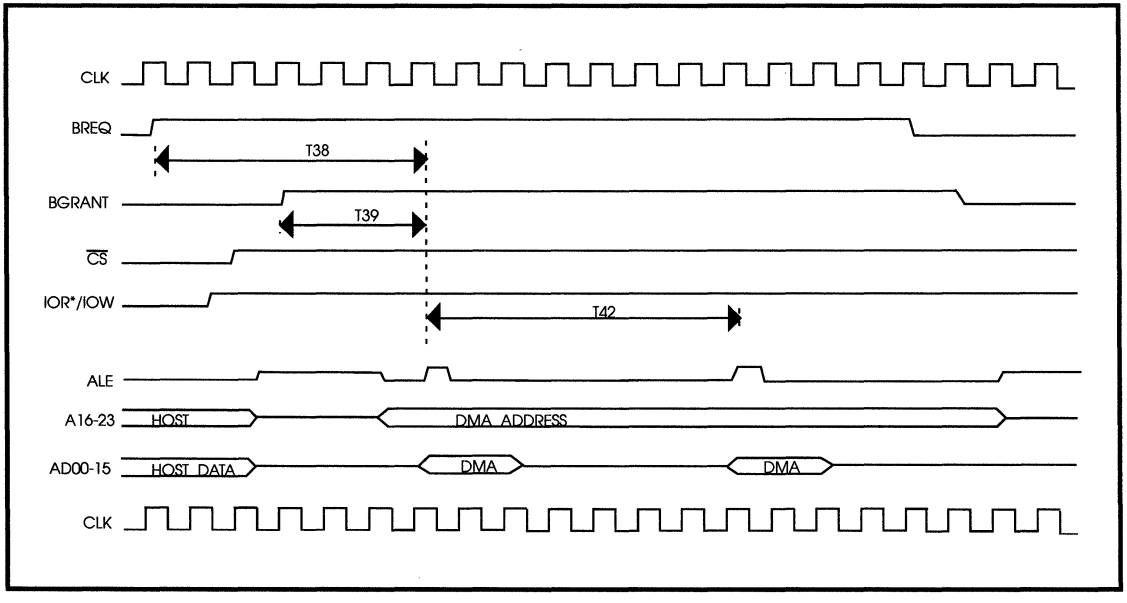


FIGURE D-6. 16-BIT BUS DMA BURST TIMING

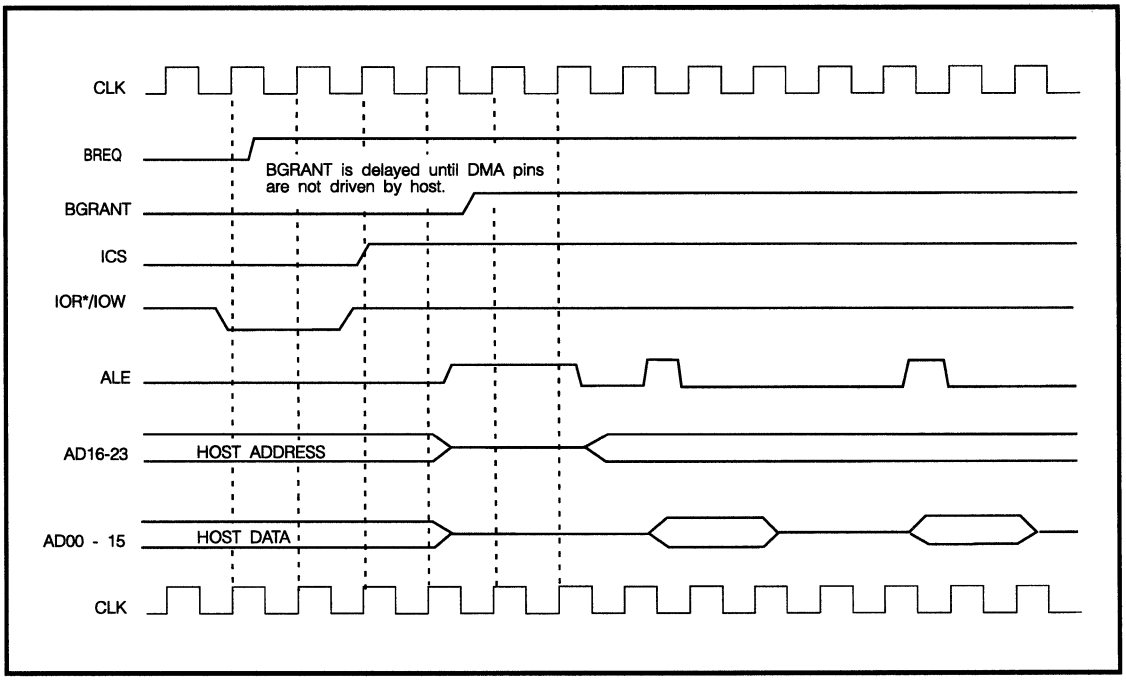


FIGURE D-7. DMA BURST TIMING, BUS BUSY

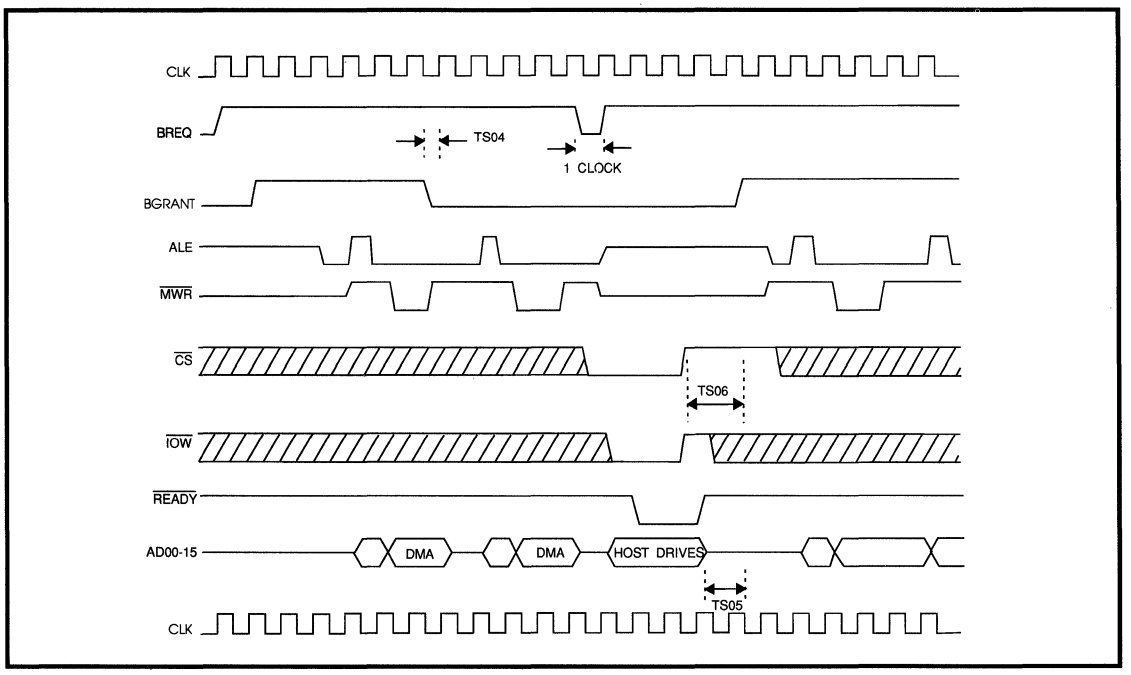


FIGURE D-8. 8-BIT BUS, INTERRUPTED DMA BURST

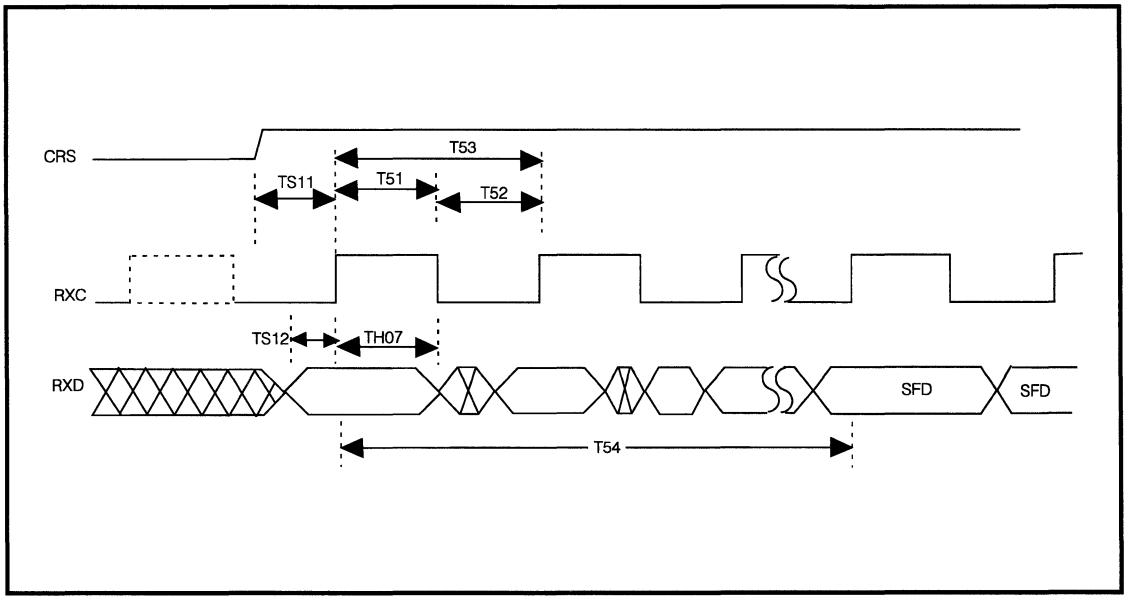


FIGURE D-9. RECEIVER SERIAL TIMING, START OF FRAME RECEPTION

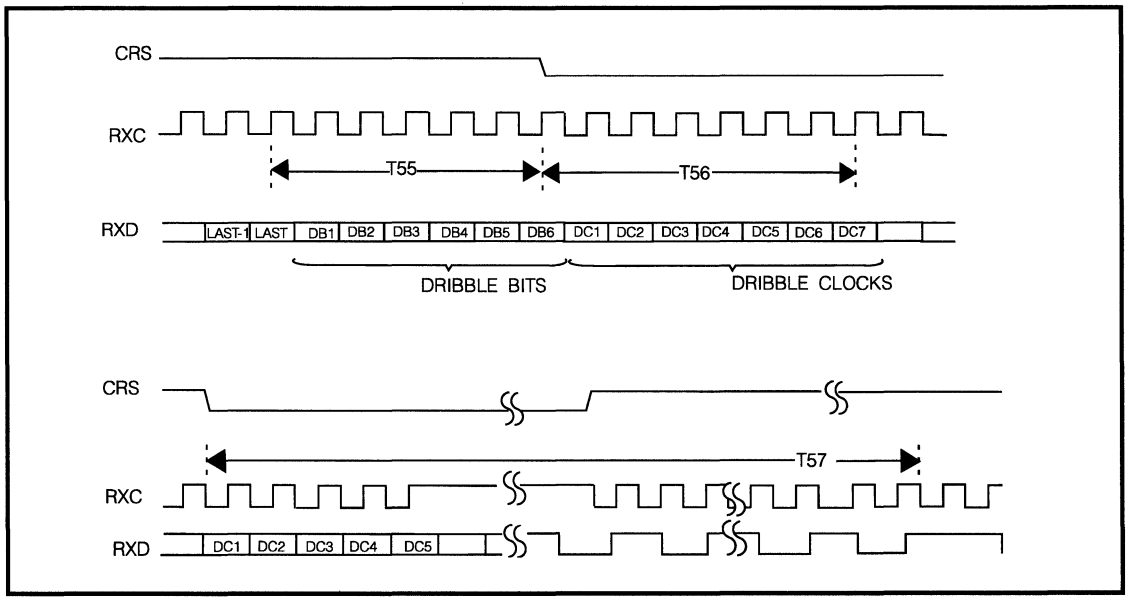


FIGURE D-10. RECEIVER SERIAL TIMING, END OF FRAME

40

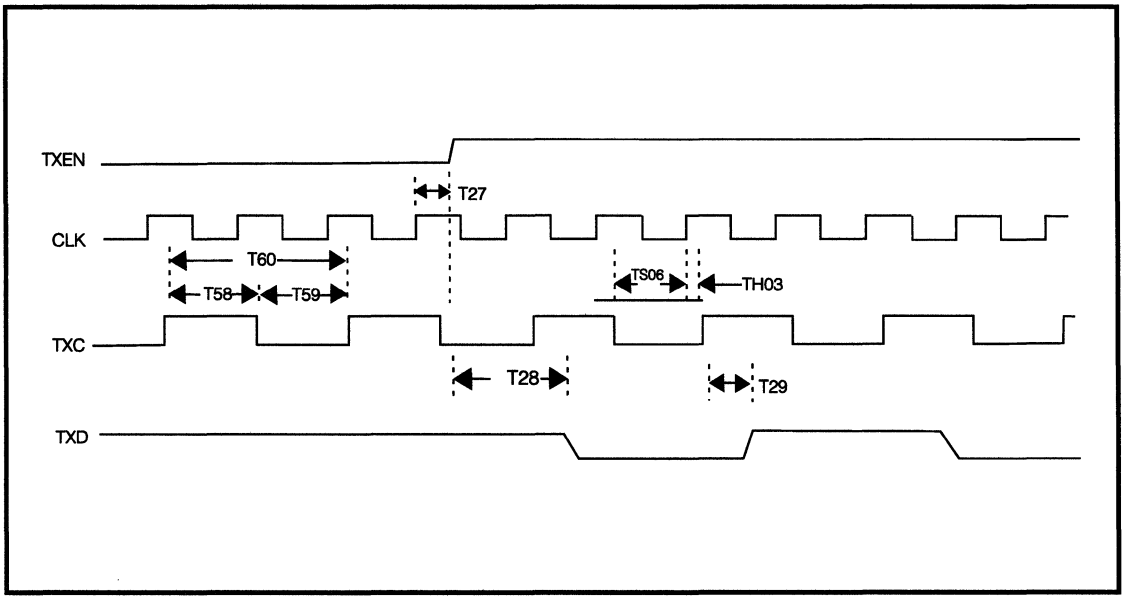


FIGURE D-11. TRANSMIT SERIAL TIMING, START OF FRAME

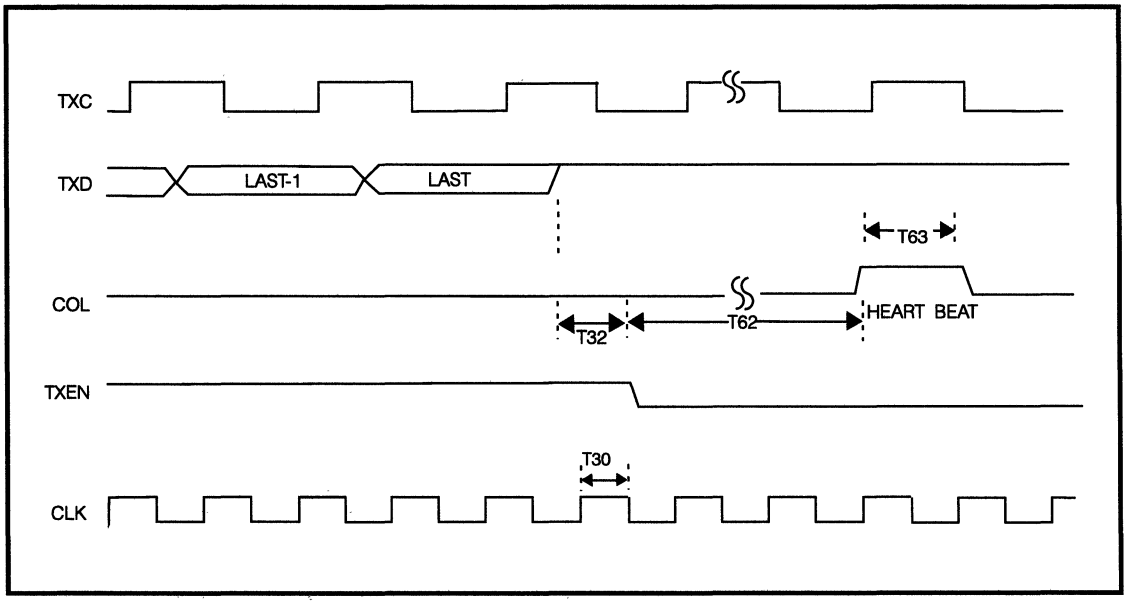


FIGURE D-12. TRANSMIT SERIAL TIMING, END OF FRAME

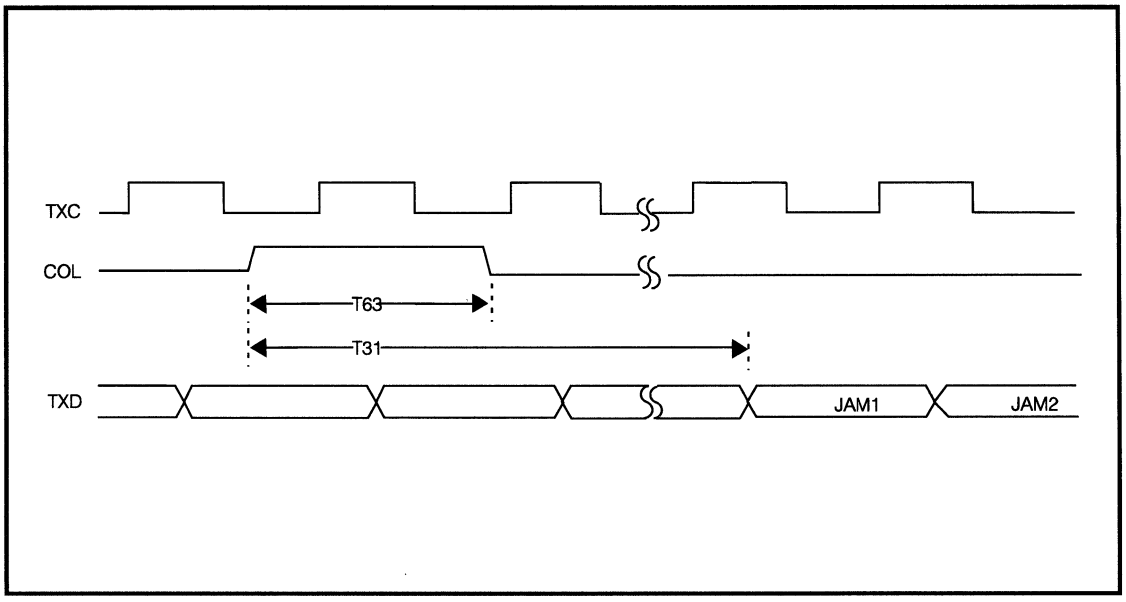


FIGURE D-13. TRANSMIT SERIAL TIMING, COLLISION

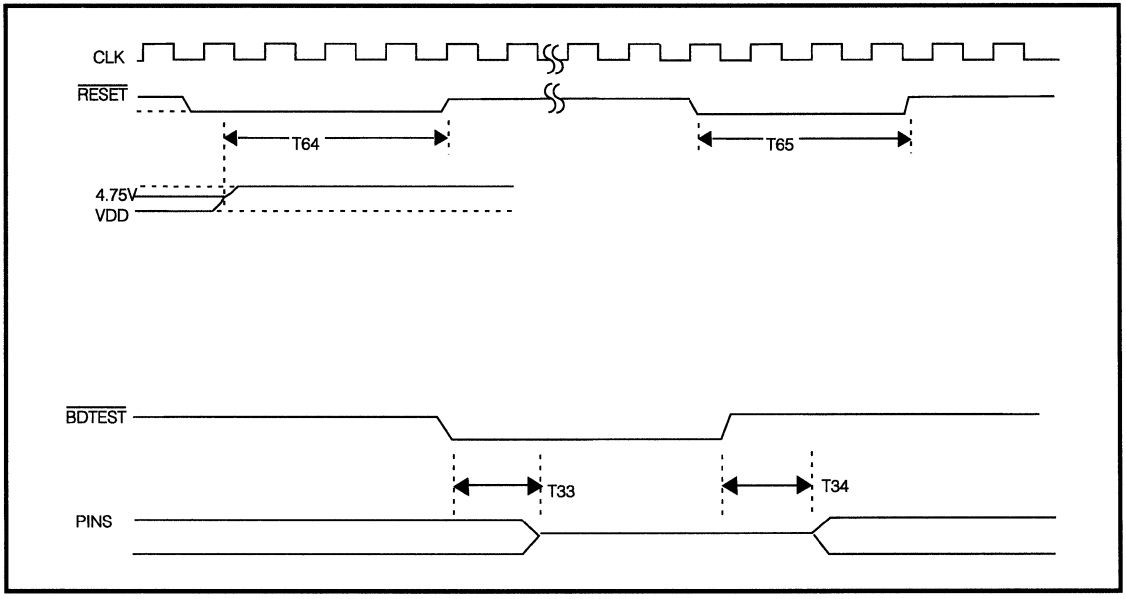


FIGURE D-14. OTHER TIMING

40

WD83C691A Manchester Encoder/ Decoder (MED)

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

APPENDICES

1.0 INTRODUCTION

1.1 DESCRIPTION

The Manchester Encoder/Decoder (MED) consists of balanced drivers and receivers, an on-board crystal oscillator, a signal translator, and a diagnostic loopback circuit. Manufactured using CMOS silicon gate technology, the device is functionally compatible with the National DP8391 Serial Network Interface (SNI).

The WD83C691A is part of a three-device set that implements the complete IEEE 802.3-compatible network node electronics (see Figure 1-1). The WD83C690 Ethernet LAN Controller (ELC) and the WD83B692 Ethernet Transceiver (ET) comprise the other two devices in the set. The WD83C690 provides media access protocol functions and performs buffer management tasks, while the WD83B692 serves as a coaxial cable line driver/receiver and collision detector.

The WD83C691A Manchester Encoder/Decoder provides the interface between the WD83C690 ELC and the WD83B692 ET. When transmitting, the device converts non-return-to-zero (NRZ) data from the controller into Manchester encoded data, then sends the data to the transceiver. When receiving, the device reverses the process using an analog phase-locked loop that decodes 10 Mbit/sec signals with up to 18 nsec of jitter.

This document describes the operation of the WD83C691A Manchester Encoder/Decoder, and provides information on the following functional blocks:

- Oscillator
- Manchester Encoder and Differential Driver
- Manchester Decoder
- Collision Translator
- Loopback Capabilities

The appendices provide pin designations, electrical operating and switching characteristics, and timing and package diagrams.

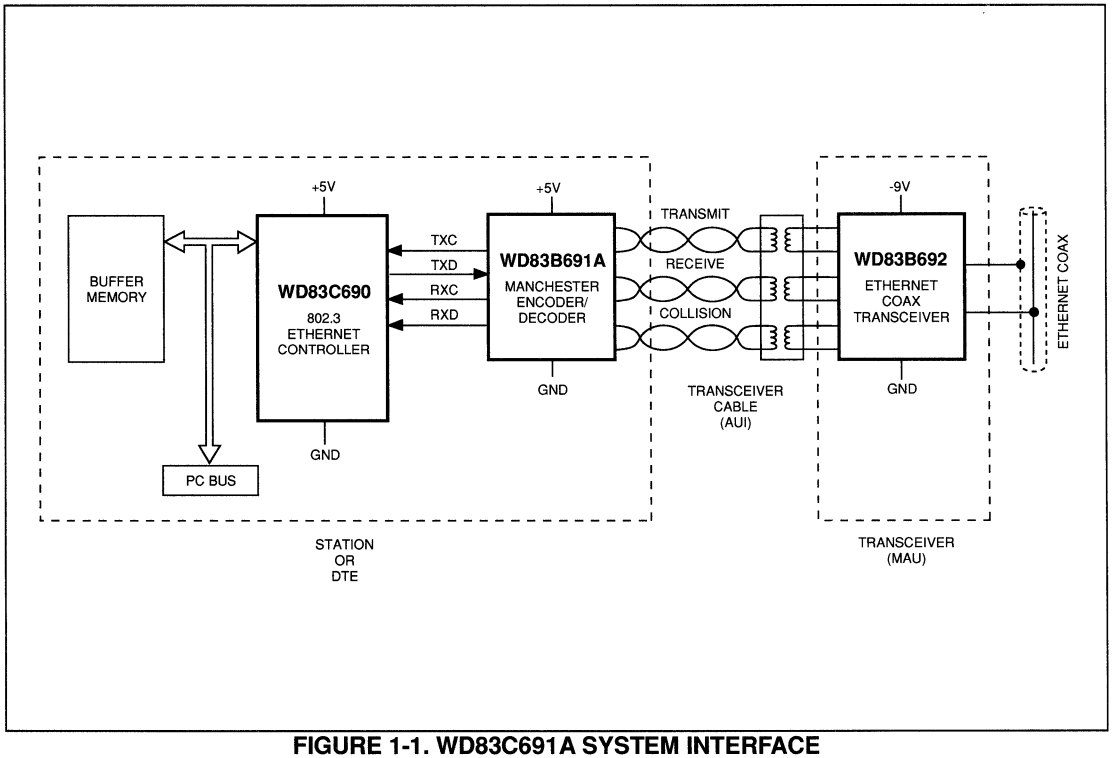


FIGURE 1-1. WD83C691A SYSTEM INTERFACE

41

1.2 FEATURES

- Compatible with Ethernet II (10BASE5) and Cheapernet (10BASE2) IEEE 802.3 standards
- Incorporates low power, 1.25 CMOS technology
- Provides 10 Mbps Manchester encoding/ decoding with receive clock recovery
- Connects directly to the transceiver (AUI) cable
- Provides 16V fault protection at the transceiver interface
- TTL/MOS-compatible controller interface
- Features externally-selectable half- or full-step modes of operation at transmit output
- Incorporates squelch circuits at receive and collision inputs to reject noise
- Provides loopback capability for diagnostics

2.0 OPERATIONAL DESCRIPTION

This section describes the five basic components of the WD83C691A.

2.1 Oscillator

Control is provided either by a 20 MHz, parallel resonant crystal connected between X1 and X2, or by an external clock connected at X1. The oscillator's 20-MHz output is divided in half to generate the 10-MHz transmit clock for the Ethernet LAN controller and to provide the internal clock signals for the encoding and decoding circuits.

The IEEE 802.3 standard requires 0.01% absolute accuracy on the transmitted signal frequency. Stray capacitance, however, can shift the crystal's frequency out of range, causing it to exceed the 0.01% tolerance. To remedy this, you may need to add extra load capacitance.

To determine the amount of capacitance to add, measure the board capacitance and the capacitance between the X1 and X2 pins. Then add these values together, and subtract them from the crystal's required load capacitance. (Refer to Figure 2-2.)

2.2 Manchester Encoder/Differential Driver

Data encoding and transmission begin when the transmit enable input (TXE) goes high, and continue as long as the TXE remains high. It is essential that the transmit enable and transmit data inputs meet the setup and hold time requirements in relation to the rising edge of the transmit clock. Transmission ends when the transmit enable input goes low. The last transition occurs at the center of the bit cell if the last bit is one, or at the boundary of the bit cell if the last bit is zero.

The differential line driver, which has the ability to drive up to 50 meters of twisted pair AUI/ Ethernet transceiver cable, provides the emitter-coupled logic (ECL) level signals. The outputs consist of current drivers that must be loaded with external 1602 pull-down resistors.

With the SEL input, one of two modes can be selected, full-step or half-step. When SEL is low, TX+ is positive in relation to TX- in the idle state. When SEL is high, TX+ and TX- are equal in the idle state. Figures C1 through C3 illustrate transmit timing.

2.3 Manchester Decoder

Decoding is accomplished by a differential input receiver circuit and an analog phase-locked loop that separate the Manchester-encoded data stream into clock signals and NRZ data. With the standard 782 transceiver drop cable, the differential input must be externally terminated. This requirement can be satisfied by connecting two 392 resistors in series with one optional common mode bypass capacitor.

To prevent noise at the input from falsely triggering the decoder, a squelch circuit rejects signals with pulse widths less than 20 nsec (negative going), or with levels less than -175 mV. When the input exceeds the squelch requirements, the analog phase-locked loop locks onto the incoming signal and the WD83C691A decodes a data frame. The carrier sense (CRS) is activated, and the receive data (RXD) and receive clock (RXC) become available within five bit times. At the end of a frame, when the normal mid-bit transition on the differential input ceases, carrier sense is deactivated. The receive clock remains active for an additional six bit times before subsiding. Figures C-4 through C-6 illustrate receive timing.

2.4 Collision Translator

The Ethernet transceiver detects collisions on the coaxial cable and generates a 10-MHz signal, which is monitored by the WD83C691A through the collision detect pins. The presence of the signal activates the collision detect (CD) pin connected to the WD83C690, and causes the controller to stop transmitting. The collision detect output is deactivated within 350 nsec after the absence of the 10-MHz signal. (Figure C-7 illustrates the collision timing.) Make sure that the collision differential inputs are terminated in exactly the same manner as the receive inputs.

2.5 Loopback Functions

A logic "1" on the loopback input causes the WD83C691A to send serial data from the transmit data input through the encoder, and back through the phase-locked loop decoder to receive the output data. The transmit driver is in the idle state during loopback mode and the receiver circuitry is disabled.

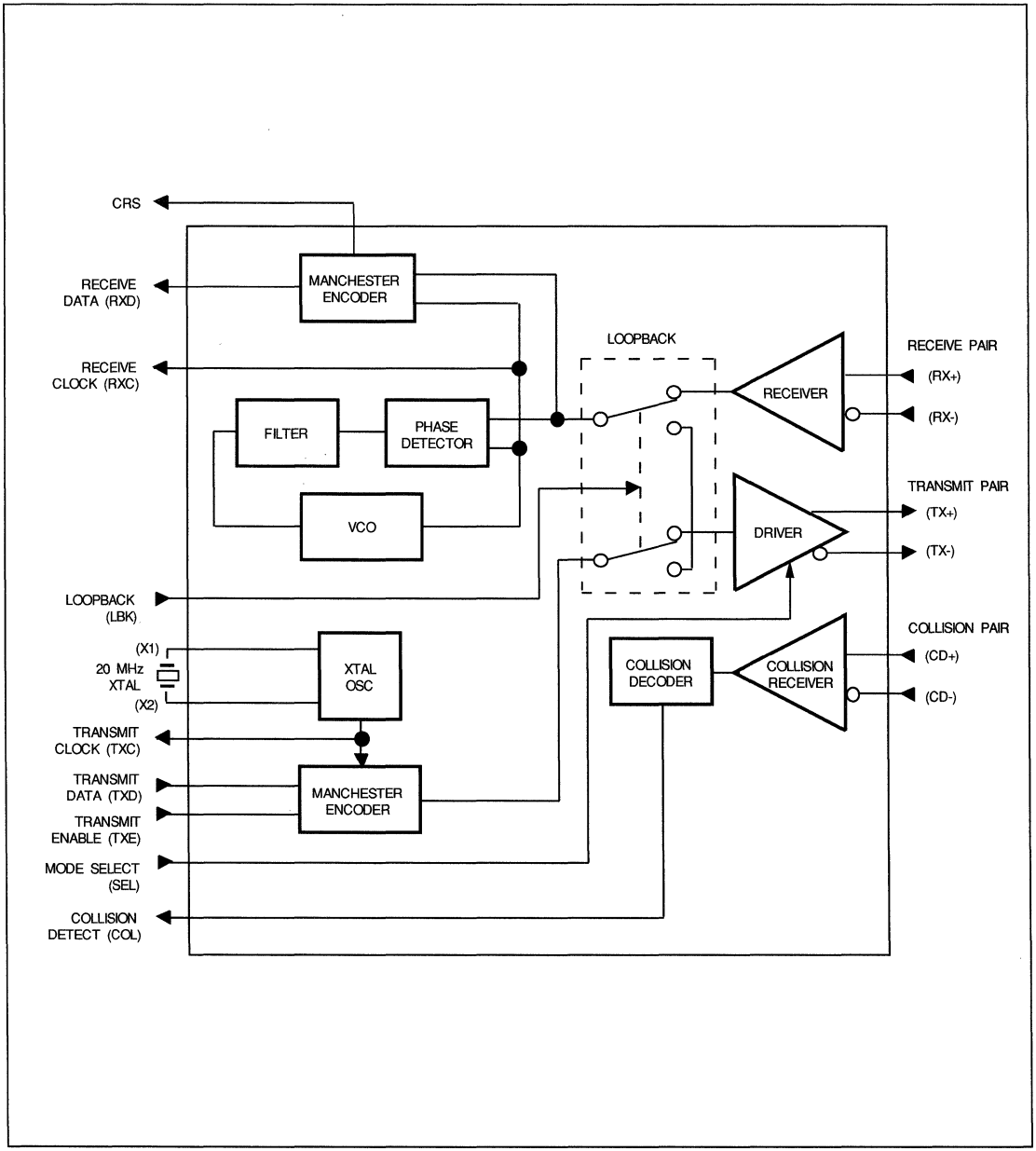
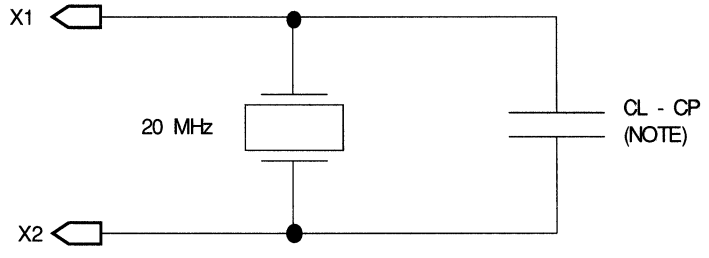


FIGURE 2-1. WD83C691A GENERAL SYSTEM BLOCK DIAGRAM

2.6 CRYSTAL SPECIFICATIONS

Resonant Frequency:	20 MHz
Overall Tolerance:	0.005% at 25°C (77°F)
Type:	AT-Cut
Temperature Tolerance:	0.005% 0°C (32°F) to 70°C (158°F)
Circuit Type:	Parallel resonance (refer to Figure 2-2 for crystal connection diagram).



CL = Load capacitance specified by crystal manufacturer.

CP= Total parasitic capacitance including:
a) WD83C691A input capacitance between X1 and X2 (typically 5 pF).
b) PC board traces, plated through holes, socket capacitances.

NOTE:
No external shunt capacitance (CL) is required if the crystal capacitance plus the parasitic capacitance matches the capacitance required to stabilize the crystal frequency.

FIGURE 2-2. CONNECTION DIAGRAM

41

APPENDIX A -- PIN DESIGNATIONS

This Appendix provides information on the 24-Pin DIP and 28-Pin PLCC devices. Figures A-1 andA-2 depict the devices, and Table A-1 lists all pin designations.

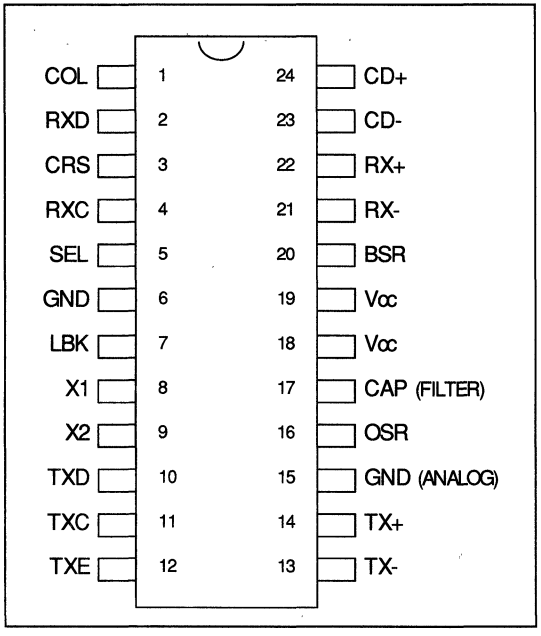


FIGURE A-1. WD83C691-PG 24-Pin DIP Manchester Encoder/Decoder

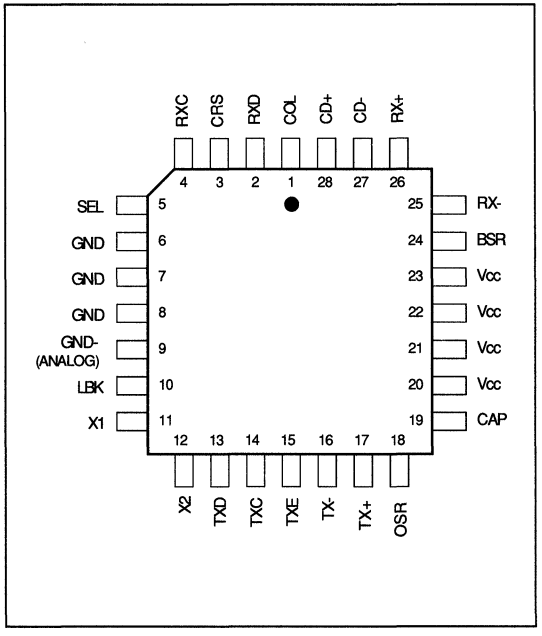


FIGURE A-2. WD83C691-JH 28-Pin PLCC Manchester Encoder/Decoder

DIP PINS	PLCC PINS	MNEMONIC	SIGNAL NAME	DESCRIPTION/FUNCTION
1	1	COL	COLLISON DETECT OUTPUT	TTL/MOS level active high output. A 10-MHz signal at the collision input produces a logic high at COL output. When there is no signal at the collision input, COL output is low.
2	2	RXD	RECEIVE DATA OUTPUT	TTL/MOS level output. This is the NRZ data from the analog phase-locked loop. This signal is sampled by the controller at the rising edge of the receive clock.
3	3	CRS	CARRIER SENSE	TTL/MOS level active high output. The output is activated when there is valid data from the transceiver at the receive input. It is deactivated two bit times after the last bit at receive point.
4	4	RXC	RECEIVE CLOCK	TTL/MOS level recovered clock output. When the analog phase-locked loop locks to a valid incoming signal, a 10-MHz clock signal is activated on this output, which remains low during idle (5 bit times after activity ceases at receive input.)
5	5	SEL*	MODE SELECT	When high, the TX+ and TX- outputs have the same voltage in idle state, providing a "zero" differential. When low, TX+ is positive with respect to TX- in idle state.
6	6-8	GND	GROUND	
7	10	LBK	LOOPBACK	TTL/MOS level active high on this input enables the loopback mode.
8	11	X1	CRYSTAL1	Crystal or external frequency source input (TTL).
9	12	X2	CRYSTAL FEEDBACK OUTPUT	This output is used only in the crystal connection, and must be left open when driving X1 with an external frequency source.
10	13	TXD	TRANSMIT DATA	TTL/MOS level input. When transmit enable input is high, this signal is sampled by the WD83C691A at the rising edge of the transmit clock. The WD83C691A combines transmit data and transmit clock signals to produce a Manchester-encoded bit stream, which is sent differentially to the transceiver.

TABLE A-1. PIN DESCRIPTIONS

41

DIP PINS	PLCC PINS	MNEMONIC	SIGNAL NAME	DESCRIPTION/FUNCTION
11	14	TXC	TRANSMIT CLOCK	Derived from the 20-MHz oscillator, This TTL/MOS level 10-MHz clock output is always active.
12	15	TXE	TRANSMIT ENABLE	TTL/MOS level active high data encoder enable input, sampled by the WD83C691A at the rising edge of the transmit clock.
13,14	16,17	TX-,TX+	TRANSMIT OUTPUT	These outputs are current drivers and require 160 ± 5.0% Ohm pull-down resistors to GND.
15	9	GND	GROUND	System analog ground.
16	18	OSR	VCO RESISTOR	A 31.6 ± 1.0% Kbyte, bias oscillator resistor connected between this pin and a VCC pin.
17	19	CAP	FILTER CAPACITOR	A ceramic capacitor must be connected from this output pin to ground as close to the part as possible. The capacitor must be .01μ F ± 10%.
18,19	20-23	VCC	VCC	+5V positive supply pins. A 0.1μ F ceramic decoupling capacitor must be connected across VCC and GND, as close to the device as possible.
20	24	BSR	BIAS RESISTOR	A 10.0 ± 1.0% Kbyte bias resistor connects beween this pin and a VCC pin.
21,22	25,26	RX-,RX+	RECEIVE INPUT	Differential receive input pair from the transceiver.
23,24	27,28	CD-,CD+	COLLISION OUTPUT	Differential collision input pair from transceiver.

TABLE A-1. PIN DESCRIPTIONS, Continued

*SEL is not a TTL/MOS level input. The VCO frequency can be observed at RXC when SEL is forced to one-half Vcc (for test purposes).

APPENDIX B -- ELECTRICAL OPERATING CHARACTERISTICS

Ta = 0°C (32°F) to 70°C (158°F), Vcc = +5V ±5% (Refer to note after table)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{IH}	Input High Voltage (TTL and X1)	2.0	-	V	
V_{IH}	Input High Voltage (SEL)	4.0	-	V	-
V_{IL}	Input Low Voltage (TTL and X1)	-	0.8	V	-
V_{IL}	Input Low Voltage (SEL)	-	1.0	V	-
I_{IH}	Input High Current (TTL) Input High Current (RX±, CD±)	- -	10 10	µA µA	Vin = Vcc Vin = Vcc
I_{IL}	Input Low Current (TTL) Input Low Current (RX±, CD±)	- -	-10 -500	µA µA	Vin = 0.5V Vin = 0.5V
V_{CL}	Input Clamp Voltage (TTL)	-	-1.2	V	Iin = -12mA
V_{OH}	Output High Voltage (TTL/MOS)	3.5	-	V	Ioh = -100 µA
V_{OL}	Output Low Voltage (TTL/MOS)	-	0.5	V	Iol = 8mA
i_{CS}	Output Short Circuit Current (TTL/MOS)	-40	-200	mA	-
V_{OD}	Differential Output Voltage (TX±)	±450	±120	mV	78Ω termination and 200Ω from each to ground
V_{OB}	Differential Output Voltage Imbalance (TX±)	-	±40	mV	78Ω termination and 200Ω from each to ground
V_{DS}	Differential Squelch Threshold (RX± CD±)	-175	-300	mV	-
V_{CM}	Input Common Mode Voltage (RX± CD±)	0	7.0	V	-
i_{CC}	Power Supply Current	-	80	mA	10 Mbit/sec

TABLE B-1. ELECTRICAL OPERATING CHARACTERISTICS

NOTE: All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

All typical values are given for Vcc = 5V and Ta = 25°C (77°F)

41

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Vcc)	6V
TTL Input Voltage	0 - 5.5V
Differential Input Voltage	-5.5 - 16V
Differential Output Voltage	0 - 16V
Differential Output Current	-40 mA
Storage Temperature	-65°C (-85°F) to 150° (302°F)

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not recommended; operation should be limited to conditions specified under DC Operating Characteristics.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (Vcc)	5V ±5%
Ambient Temperature	0°C (32°F) to 70°C (158°F)

APPENDIX C -- SWITCHING CHARACTERISTICS

Ta = 0°C (32°F) to 70°C (158°F), Vcc = +5V ±5% (Refer to note after table)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Oscillator Specification					
t_{XTH}	X1 to Transmit Clock High	8	-	20	nsec
t_{XTL}	X1 to Transmit Clock Low	8	-	20	nsec
Transmit Specification					
t_{TCD}	Transmit Clock Duty Cycle at 1.5V (10 MHz)	42	50	58	%
t_{TCR}	Transmit Clock Rise Time (1.1V to 2.9V)	-	-	10	nsec
t_{TCF}	Transmit Clock Fall Time (2.9V to 1.1V)	-	-	10	nsec
t_{TDS}	Transmit Data Setup Time to Transmit Clock Rising Edge	20	-	-	nsec
t_{TDH}	Transmit Data Hold Time from Transmit Clock Rising Edge	0	-	-	nsec
t_{TES}	Transmit Enable Setup Time to Transmit Clock Rising Edge	20	-	-	nsec
t_{TEH}	Transmit Enable Hold Time from Transmit Clock Rising Edge	0	-	-	nsec
t_{TOD}	Transmit Output Delay from Transmit Clock Rising Edge	-	-	40	nsec
t_{TOR}	Transmit Output Rise Time (20% to 80%)	-	-	7	nsec
t_{TOF}	Transmit Output Fall Time (80% to 20%)	-	-	7	nsec
t_{TOJ}	Transmit Output Jitter	-	±0.25	-	nsec
t_{TOH}	Transmit Output High Before Idle in Half Step Mode	200	-	-	nsec
t_{TOI}	Transmit Output Idle Time in Half Step Mode	-	-	800	nsec
Receive Specification					
t_{RCD}	Receive Clock Duty Cycle at 1.5V (10 MHz)	40	50	60	%
t_{RCR}	Receive Clock Rise Time (1.1V to 2.9V)	-	-	10	nsec
t_{RCF}	Receive Clock Fall Time (2.9V to 1.1V)	-	-	8	nsec

TABLE C-1. SWITCHING CHARACTERISTICS

41

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Receive Specification, continued					
t_{RDR}	Receive Data Rise Time (20% to 80%)	-	-	8	nsec
t_{RDF}	Receive Data Fall Time (80% to 20%)	-	-	8	nsec
t_{RDS}	Receive Data Stable From Receive Clock Rising Edge	40	-	-	nsec
t_{CSON}	Carrier Sense Turn on Delay	-	-	50	nsec
t_{CSOFF}	Carrier Sense Turn off Delay	-	-	160	nsec
t_{DAT}	Decoder Acquisition Time	-	-	700	nsec
t_{DREJ}	Differential Inputs Rejection Pulse Width (Squelch)	8	-	30	nsec
t_{RD}	Receive Throughout Delay	-	-	150	nsec
Collision Specification					
t_{COLON}	Collision Turn On Delay	-	-	50	nsec
t_{COLOFF}	Collision Turn Off Delay	-	-	350	nsec
Loopback Specification					
t_{LBS}	Loopback Setup Time	20	-	-	nsec
t_{LBH}	Loopback Hold Time	0	-	-	nsec

TABLE C-1. SWITCHING CHARACTERISTICS, Continued

NOTE: All typical values are given for Vcc = 5V and Ta = 25°C (77°F).

TIMING DIAGRAMS

Table C-2 lists all timing diagrams. Figures C-1 through C-9 illustrate all timings.

Figure Number	Title
C-1	Transmit Timing -- Start of Transmission
C-2	Transmit Timing -- End of Transmission (last bit = 0)
C-3	Transmit Timing -- End of Transmission (last bit = 1)
C-4	Receive Timing -- Start of Packet
C-5	Receive Timing -- End of Packet (last bit = 0)
C-6	Receive Timing -- End of Packet (last bit = 1)
C-7	Collision Timing
C-8	Loopback Timing
C-9	Test Loads

TABLE C-2. WD83C691A TIMING DIAGRAMS

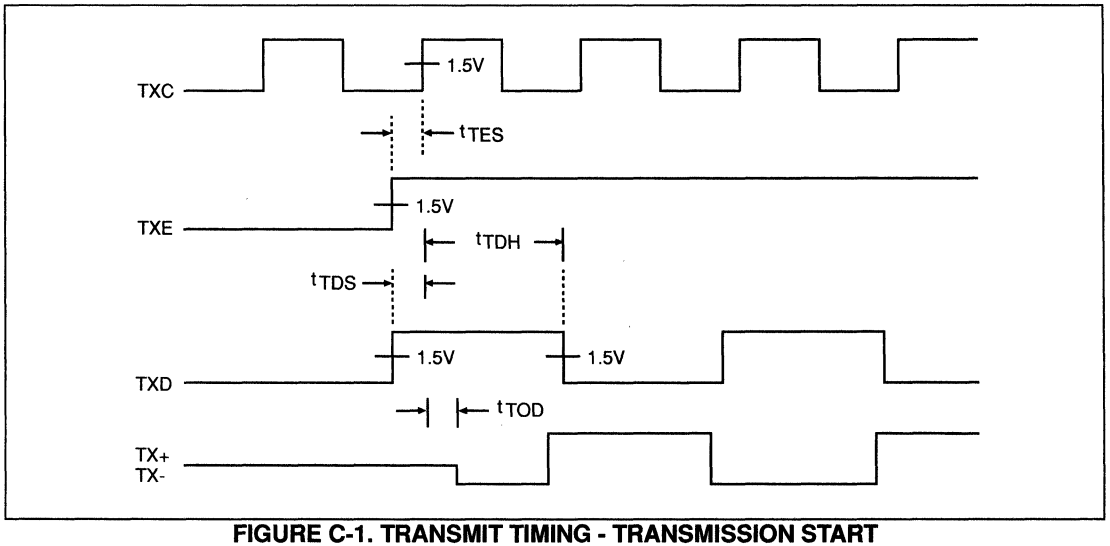


FIGURE C-1. TRANSMIT TIMING - TRANSMISSION START

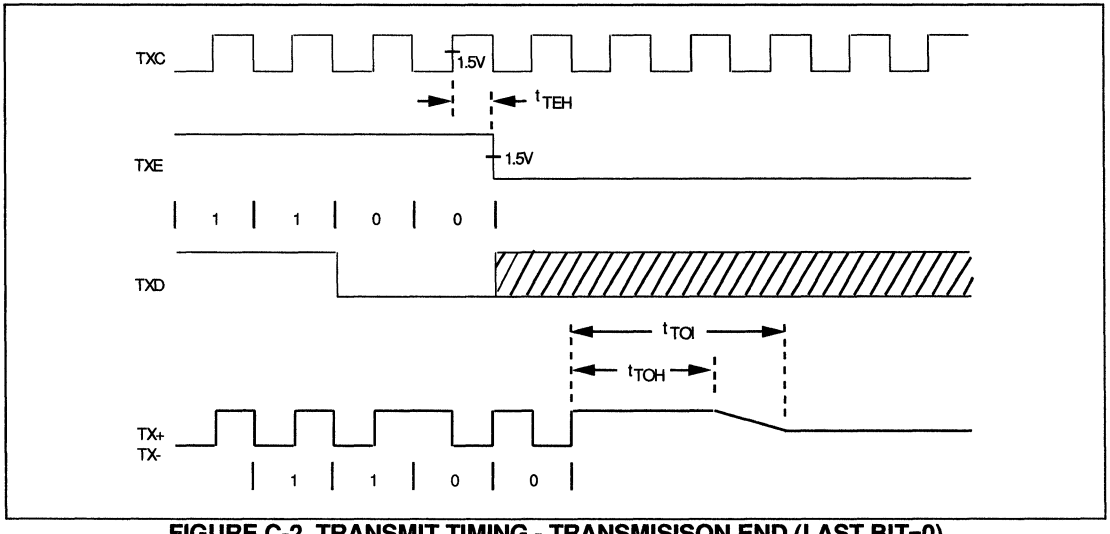


FIGURE C-2. TRANSMIT TIMING - TRANSMISISON END (LAST BIT=0)

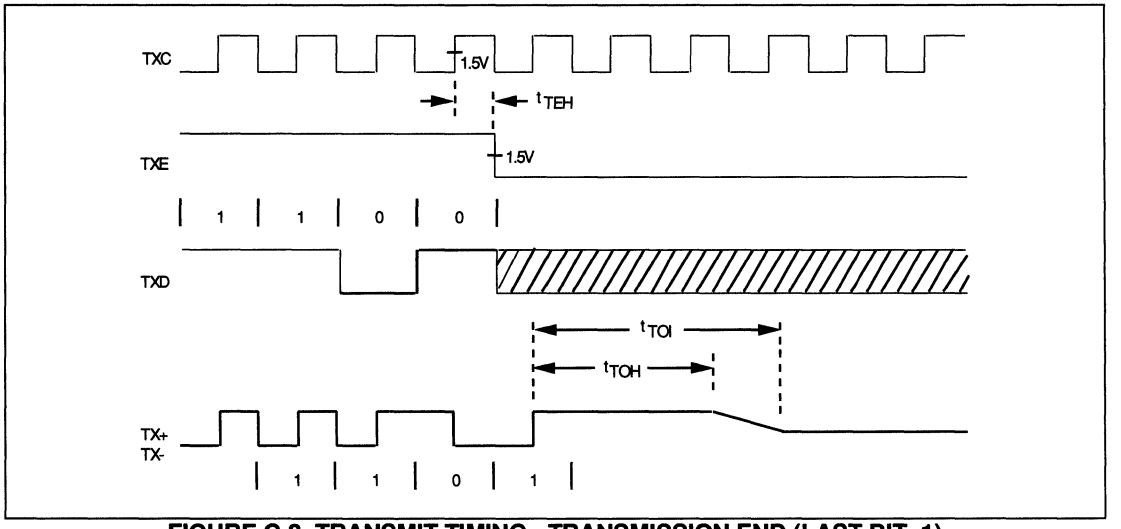


FIGURE C-3. TRANSMIT TIMING - TRANSMISSION END (LAST BIT=1)

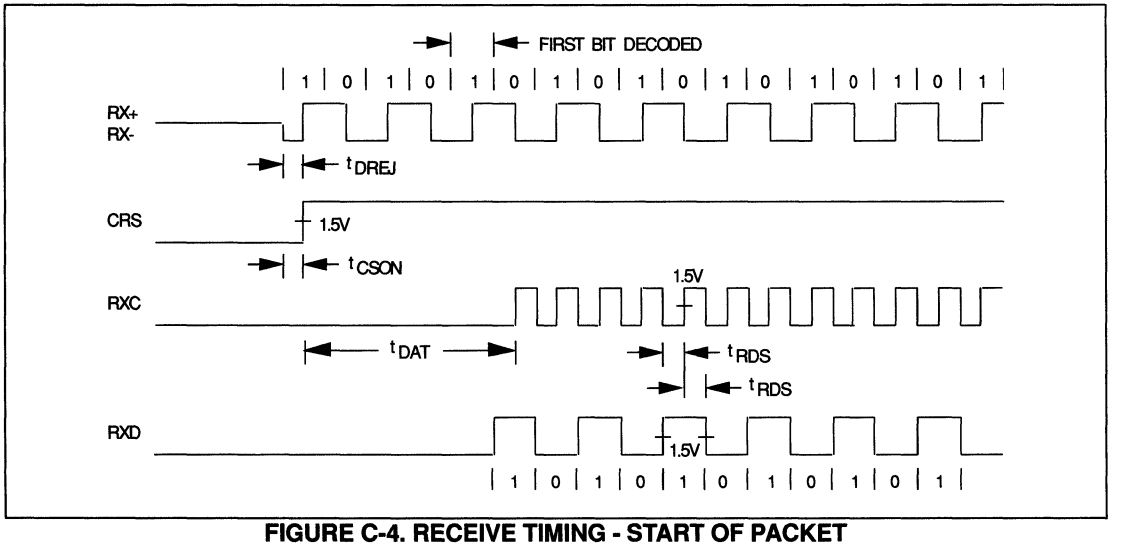


FIGURE C-4. RECEIVE TIMING - START OF PACKET

41

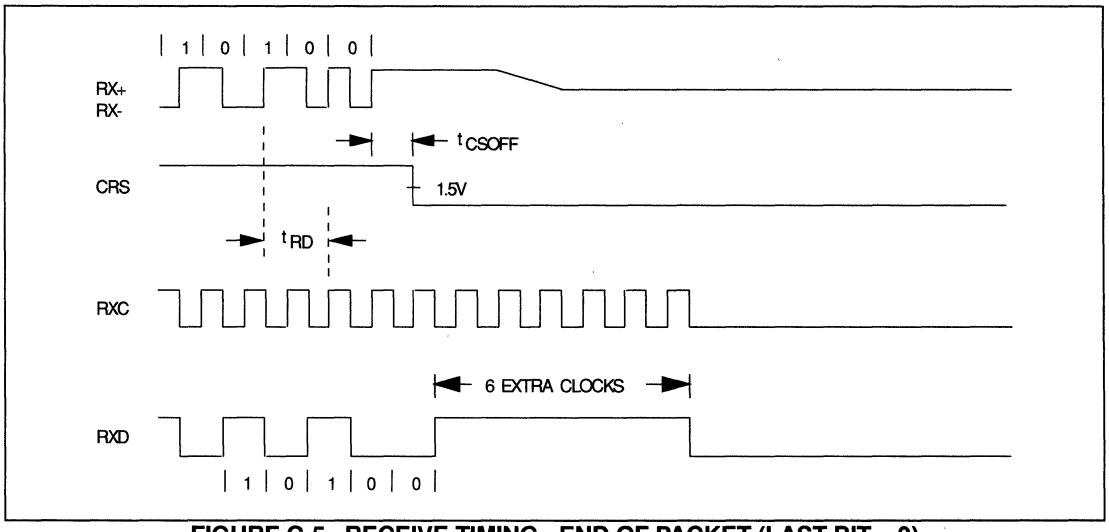


FIGURE C-5. RECEIVE TIMING - END OF PACKET (LAST BIT = 0)

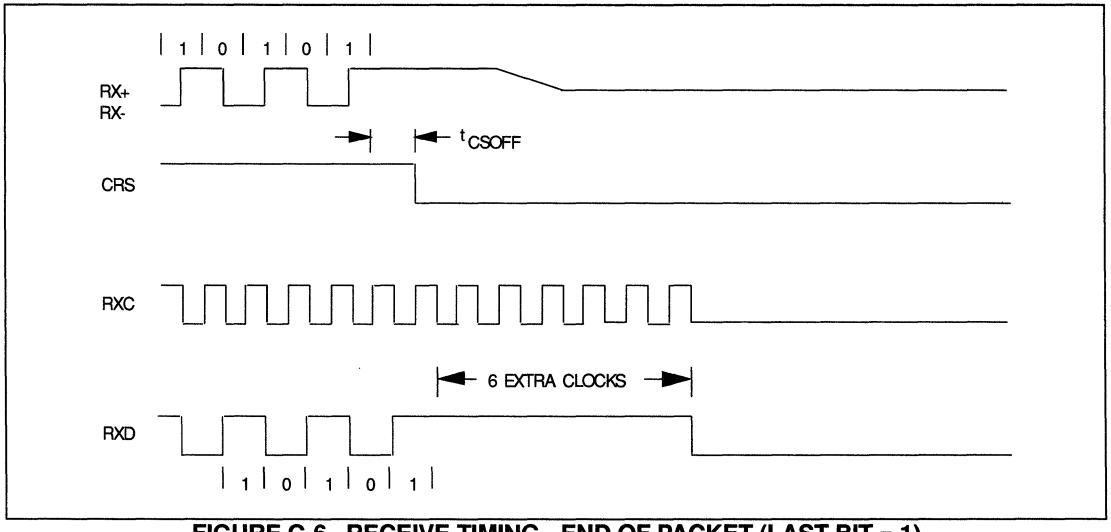


FIGURE C-6. RECEIVE TIMING - END OF PACKET (LAST BIT = 1)

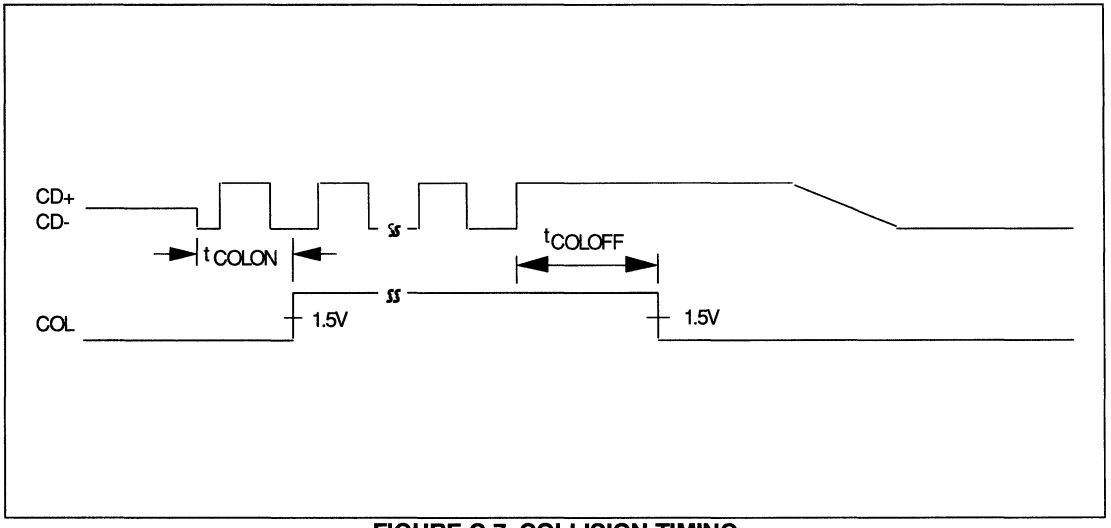


FIGURE C-7. COLLISION TIMING

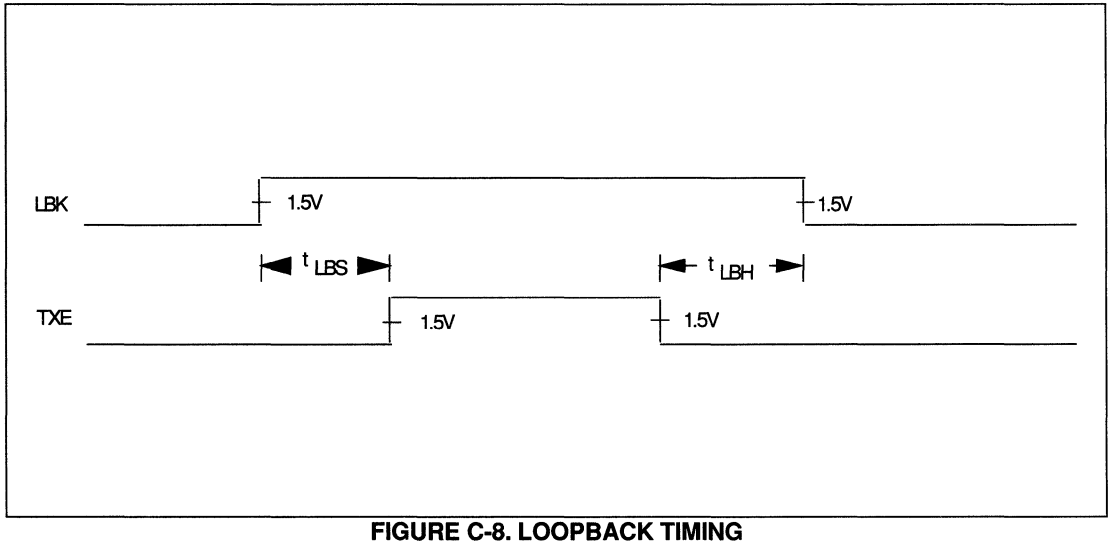
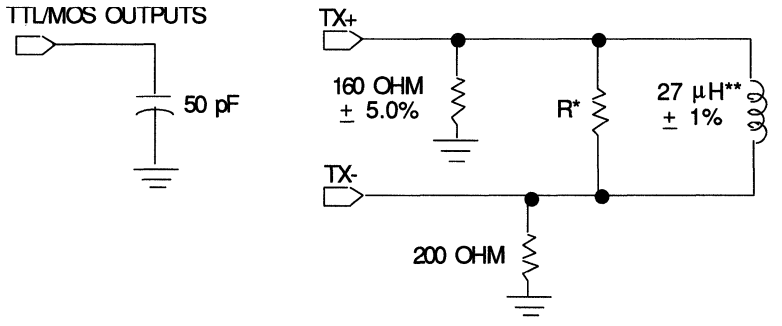


FIGURE C-8. LOOPBACK TIMING

41



* R = 73 OHM ± 1% and
R = 83 OHM ± 1%

** 27 µH ± 1% inductor is used for test purposes. 100 µH transformers (Valor LT 1101, or Pulse Engineering 64103) are recommended for application use.

FIGURE C-9. TEST LOADS

APPENDIX D - PACKAGE DIAGRAMS

Figures D-1 and D-2 are illustrations of the 24-Pin DIP and 28-Pin PLCC packages showing dimensions in inches.

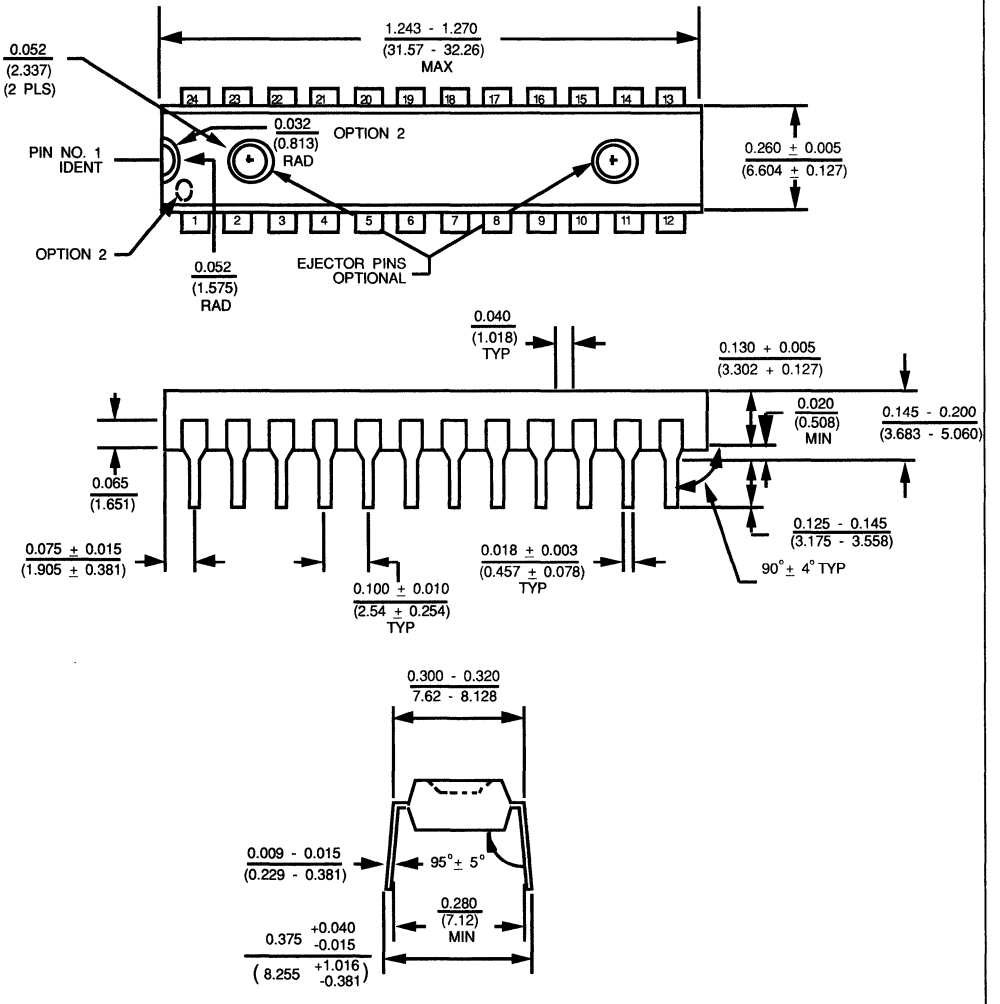


FIGURE D-1. 24-PIN DIP PACKAGE DRAWING

41

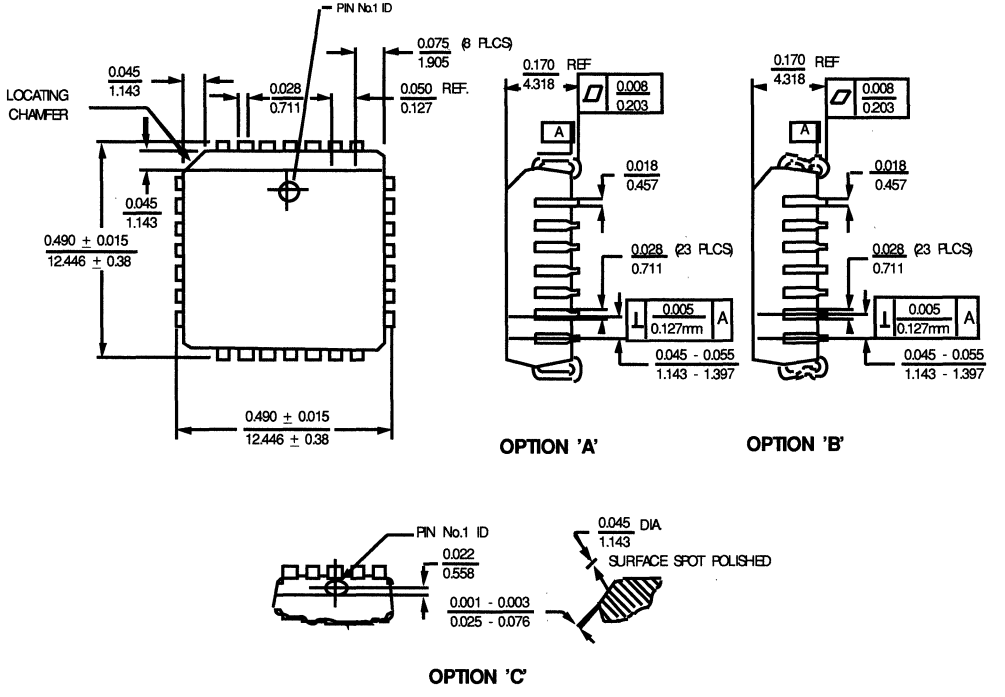


FIGURE D-2. 28-PIN PLCC PACKAGE DRAWING